

Habib University



Dhanani School of Science and Engineering

CE/CS 321/330 Computer Architecture

Final Lab Project

**5-Stage Pipelined Processor To Execute A
Single Array Sorting Algorithm**

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1 Introduction

The purpose of this project is to design a 5-stage pipelined processor to execute a single array sorting algorithm. We will be converting our single cycle processor to a pipelined one. The processor is designed in Verilog HDL and the sorting algorithm is written in RISC-V assembly language. The processor is first executed using single cycle processor, it is then implemented by adding in pipelining to the processor to increase efficiency in our processor. The report is divided according to each task that we had to implement according to the project rubrics.

2 Task 1 - Sorting Algorithm on a Single Cycle Processor

2.1 Selection Sort Assembly Code

```
1  addi x11, x0, 6 #an arbitrary value to append in array
2  addi x29, x0, 6 #initializing size of the array to be 6
3  addi x30, x0, 0 #initializing offset to store values in
   array after one another
4  addi x31, x0, 0 #initializing i = 0 to loop through array to
   enter values.
5  addi x28, x0, 6 #temporary reg for checking length
6
7  #The code below is to intialize random values in the array
8  Array:
9
10     sw x11, 0x100(x30) #store values in array
11     addi x31, x31, 1 #performs i = i + 1
12     addi x30, x30, 4 #offset + 4 to jump to next memory
   address to store value
13     addi x11, x11, -1 #subtracting 1 to add next value in
   array (6->5->4....)
14     beq x28, x31, filled #if i = size of array, stop.
15     beq x0, x0, Array
16
17 filled:
18
19 #After the above code, the array is [6,5,4,3,2,1]
20
21 addi x30, x0, 0 #i = 0 (for i loop)
22 addi x31, x30, 0 #j = 0
23 addi x29, x0, 0 #for offset calculation
24 addi x11, x0, 6 #condition to check if i = size of array
25
26 #Code below is for 1st i loop
27
```

```

28 I_Loop:
29
30     beq x11, x30, Sorted #if i = size of array, array has
        been sorted
31     add x10, x29, x0 #assigning min_index = i
32     addi x31, x30, 1 #j = j + 1
33     addi x28, x29, 4 #jump to next address
34
35 #Code below is for nested j loop
36 J_Loop:
37
38     beq x31, x11, Swap
39     lw x15, 0x100(x28) #load Array[j]
40     lw x16, 0x100(x10) #load Array[min_index]
41     blt x15, x16, If #if Array[j] < Array[min_index]
42
43     #The code below it to iterate through the jth loop
44
45     return:
46
47     addi x31, x31, 1 #perform j = j + 1
48     addi x28, x28, 4 #jump to next address
49     beq x0, x0, J_Loop #jump to nested j loop
50
51     #The code below is to iterate through ith loop.
52
53     jump_back:
54
55     addi x30, x30, 1 #perform i = i + 1
56     addi x28, x28, 4 #jump to next address
57     beq x0, x0, I_Loop #jump to first i loop.
58
59 #Code below is for min_index = j line.
60
61 If:
62
63     addi x10, x28, 0 #assign min_index = j
64     beq x0, x0, return #jump back to j loop
65
66 #Code below is to perform swapping
67
68 Swap:
69
70     lw x13, 0x100(x10) #load Array[min_index]
71     lw x14, 0x100(x29) #load Array[i]
72     sw x13, 0x100(x29) #Array[min_index] = Array[i]
73     sw x14, 0x100(x10) #Array[i] = Array[min_index]
74     addi x29, x29, 4 #add 4 in x29 so that it doesnot
        include sorted value
75     beq x0, x0, jump_back

```

```
76  
77 Sorted:
```

Listing 1: Selection Sort Assembly code

2.2 Selection Sort Python Code

```
1 def selectionSort(array, size):  
2  
3 for ind in range(size):  
4     min_index = ind  
5  
6     for j in range(ind + 1, size):  
7         # select the minimum element in every iteration  
8         if array[j] < array[min_index]:  
9             min_index = j  
10        # swapping the elements to sort the array  
11        (array[ind], array[min_index]) = (array[min_index],  
        array[ind])
```

Listing 2: Selection Sort Python Code (Taken from GeeksforGeeks)

2.3 Selection Sort on Venus Simulator

Address	+0	+1	+2	+3
0x00000120	00	00	00	00
0x0000011c	00	00	00	00
0x00000118	00	00	00	00
0x00000114	01	00	00	00
0x00000110	02	00	00	00
0x0000010c	03	00	00	00
0x00000108	04	00	00	00
0x00000104	05	00	00	00
0x00000100	06	00	00	00
0x000000fc	00	00	00	00
0x000000f8	00	00	00	00
0x000000f4	00	00	00	00
0x000000f0	00	00	00	00

Figure 1: Image of Memory before Sorting

Address	+0	+1	+2	+3
0x00000120	00	00	00	00
0x0000011c	00	00	00	00
0x00000118	00	00	00	00
0x00000114	06	00	00	00
0x00000110	05	00	00	00
0x0000010c	04	00	00	00
0x00000108	03	00	00	00
0x00000104	02	00	00	00
0x00000100	01	00	00	00
0x000000fc	00	00	00	00
0x000000f8	00	00	00	00
0x000000f4	00	00	00	00
0x000000f0	00	00	00	00

Figure 2: Image of Memory after Sorting

3 Changes to Single Cycle Processor

3.1 Changes to Control Unit

```

1  module Control_Unit
2  (
3      input [6:0] Opcode,
4      output reg Branch, MemRead, MemtoReg, MemWrite, ALUSrc,
5          RegWrite,
6      output reg [1:0] ALUOp
7  );
8
9      always @ (Opcode)
10     begin
11         case (Opcode)

```

```

11      7'b0110011: //R type (51)
12          begin
13              Branch = 0;
14              MemRead = 0;
15              MemtoReg = 0;
16              MemWrite = 0;
17              ALUSrc = 0;
18              RegWrite = 1;
19              ALUOp = 2'b10;
20          end
21      7'b0000011: //ld (3)
22          begin
23              Branch = 0;
24              MemRead = 1;
25              MemtoReg = 1;
26              MemWrite = 0;
27              ALUSrc = 1;
28              RegWrite = 1;
29              ALUOp = 2'b00;
30          end
31      7'b0010011: //addi (19)
32          begin
33              Branch = 0;
34              MemRead = 0;
35              MemtoReg = 0;
36              MemWrite = 0;
37              ALUSrc = 1;
38              RegWrite = 1;
39              ALUOp = 2'b00;
40          end
41
42      7'b0100011: // I type SD (35)
43          begin
44              Branch = 0;
45              MemRead = 0;
46              MemtoReg = 1'bx;
47              MemWrite = 1;
48              ALUSrc = 1;
49              RegWrite = 0;
50              ALUOp = 2'b00;
51          end
52      7'b1100011://SB type blt and beq 99
53          begin
54              Branch = 1;
55              MemRead = 0;
56              MemtoReg = 1'bx;
57              MemWrite = 0;
58              ALUSrc = 0;
59              RegWrite = 0;
60              ALUOp = 2'b01;

```



```

61         end
62         default:
63             begin
64                 ALUSrc    = 1'b0;
65                 MemtoReg = 1'b0;
66                 RegWrite = 1'b0;
67                 MemRead  = 1'b0;
68                 MemWrite = 1'b0;
69                 Branch   = 1'b0;
70                 ALUOp    = 2'b00;
71             end
72         endcase
73     end
74 endmodule

```

Listing 3: Changes to Control Unit

The input signals to the control unit, which are the OpCode bits 6:0, are used to set the seven control signals. Given that both instructions require jumping to a specific memory address without any reading or writing, the OpCode for beq and blt is the same, as are their signals.

3.2 Changes to ALU Control Unit

```

1 module ALU_Control
2 (
3     input [1:0] ALUOp,
4     input [3:0] Funct,
5     output reg [3:0] Operation
6 );
7
8     always @(*)
9     begin
10         case(ALUOp)
11         2'b00:
12             begin
13                 Operation = 4'b0010;
14             end
15         2'b01:                                     // branch type
16             instructions
17             begin
18                 case(Funct[2:0])
19                 3'b000:                             // beq
20                     begin
21                         Operation = 4'b0110; // subtract
22                     end
23                 3'b100:                             // blt
24                     begin
25                         Operation = 4'b0100; // less than operation
26                     end

```

```

26         endcase
27     end
28
29
30     2'b10:
31     begin
32         case(Funct)
33         4'b0000:
34             begin
35                 Operation = 4'b0010;
36             end
37         4'b1000:
38             begin
39                 Operation = 4'b0110;
40             end
41         4'b0111:
42             begin
43                 Operation = 4'b0000;
44             end
45         4'b0110:
46             begin
47                 Operation = 4'b0001;
48             end
49         endcase
50     end
51 endcase
52 end
53 endmodule

```

Listing 4: Changes to ALU Control Unit

ALU Control, which creates the 4-bit ALU Control input, has been modified. The Func Field [1-bit from funct7 field (bit 30) plus 3-bits from funct3 field (bits 14:12)] and a 2-bit control field known as ALUOp are inputs to the control unit. The output is a 4-bit signal that, depending on Func and the ALUOp field, selects one of the six operations to be executed in our example, directly controlling the ALU. According to ALUOp, the operation that has to be carried out will either be add (00) for loads and stores or will be determined by the operation that is encoded in the funct7 and funct3 fields (10, 01). When ALUOp was "01," that is, when there was a branch type instruction, we added an additional case structure.

3.3 Changes to ALU

```

1 module ALU_64_bit
2     (
3         input [63:0] a, b,
4         input [3:0] ALUOp,
5

```

```

6      output reg [63:0] Result,
7      output ZERO
8  );
9
10     localparam [3:0]
11     AND = 4'b0000,
12     OR  = 4'b0001,
13     ADD = 4'b0010,
14     Sub = 4'b0110,
15     NOR = 4'b1100,
16     Less = 4'b0100;
17
18     assign ZERO = (Result == 0);
19
20     always @ (ALUOp, a, b)
21     begin
22         case (ALUOp)
23             AND: Result = a & b;
24             OR:  Result = a | b;
25             ADD: Result = a + b;
26             Sub: Result = a - b;
27             NOR: Result = ~(a | b);
28             Less: Result = (a < b) ? 0 : 1;    //less than
                operation
29
30             default: Result = 0;
31         endcase
32     end
33
34 endmodule

```

Listing 5: Changes to ALU 64 bit

If first value is less than second value, Result is set to '0'. Similar to the beq instruction, '0' would be assigned to Zero if Result == 0. This eliminates the need for extra hardware modifications to check for additional branch type instructions. In accordance with our hardware structure, where a selection line of mux is Branch & Zero, the PC is unconditionally replaced with PC + 4 when the Branch control signal is 0, and the branch target is replaced with the PC if the Zero output of the ALU is high (when a < b or a == b = 0)

3.4 Data Memory

```

1 module Data_Memory
2 (
3     input [63:0] Mem_Addr,
4     input [63:0] Write_Data,
5     input clk, MemWrite, MemRead,
6     output reg [63:0] Read_Data

```

```

7 ,
8     output [63:0] element1,
9     output [63:0] element2,
10    output [63:0] element3,
11    output [63:0] element4,
12    output [63:0] element5,
13    output [63:0] element6
14 );
15
16    reg [7:0] DataMemory [1233:0];
17
18    assign element1 = DataMemory[256];
19    assign element2 = DataMemory[264];
20    assign element3 = DataMemory[272];
21    assign element4 = DataMemory[280];
22    assign element5 = DataMemory[288];
23    assign element6 = DataMemory[296];
24    integer i;
25
26    initial
27    begin
28        for (i = 0; i < 1233; i = i + 1)
29            begin
30                DataMemory[i] = 8'd0;
31            end
32    end
33
34
35    always @ (posedge clk)
36    begin
37        if (MemWrite)
38            begin
39                DataMemory[Mem_Addr] = Write_Data[7:0];
40                DataMemory[Mem_Addr+1] = Write_Data[15:8];
41                DataMemory[Mem_Addr+2] = Write_Data[23:16];
42                DataMemory[Mem_Addr+3] = Write_Data[31:24];
43                DataMemory[Mem_Addr+4] = Write_Data[39:32];
44                DataMemory[Mem_Addr+5] = Write_Data[47:40];
45                DataMemory[Mem_Addr+6] = Write_Data[55:48];
46                DataMemory[Mem_Addr+7] = Write_Data[63:56];
47            end
48    end
49
50    always @ (*)
51    begin
52        if (MemRead)
53            Read_Data = {DataMemory[Mem_Addr+7], DataMemory[
                    Mem_Addr+6], DataMemory[Mem_Addr+5], DataMemory[
                    Mem_Addr+4], DataMemory[Mem_Addr+3],
                    DataMemory[Mem_Addr+2], DataMemory[Mem_Addr

```

```

54         +1],DataMemory[Mem_Addr]};
55     end
endmodule

```

Listing 6: Changes to Data Memory

4 Task 2 - Introducing Pipeline Stages

A difficulty with implementation of single cycle processor is that the processor only executes one instruction at a time, and only after that instruction is finished is execution of the subsequent instruction begins, which is counter-productive. Given that the majority of the components in our processors would remain idle, it is immediately clear how wasteful this would be and how much processing power it would waste. This is why, in this section, we'll try to fix it by adding pipelining to our single-cycle processor.

Pipelining would allow us to execute numerous commands at once. An in-depth explanation of how this works will be provided in the following section, but for now, consider that one component will work on one portion of the instruction while the other will work on a different part at the same point, thus increasing the efficiency of the whole program. We'll be incorporating a five-stage pipeline into our Risc-V processor, allowing it to handle five instructions at once. The five stages we implemented for the processor are as follows:

1. IF: Instruction Fetch
2. ID: Instruction Decode
3. EX: Execution or address calculation
4. MEM: Data Memory Access
5. WB: Write back

We will be introducing four new registers to implement the pipelining stage and to make our program more efficient. These registers are as follows:

1. IF/ID register: This register will be used to store the instruction fetched in the IF stage and will be used in the ID stage.
2. ID/EX register: This register will be used to store the instruction decoded in the ID stage and will be used in the EX stage.
3. EX/MEM register: This register stores the result of the execution stage.
4. MEM/WB register: This register stores the result of the memory access stage.

These four newly introduced pipeline registers help in the pipelining process. These registers allow the pipeline to handle multiple instructions simultaneously and keep track of the progress of each instruction as it moves through the pipeline. The use of these registers helps to improve the performance of the processor by enabling the processing of multiple instructions in parallel.

An ideal pipeline would be one which continuously moves forward and the instructions are only provided and moved forward. However, this is not the case with the pipeline taught to us. e of the PC, choosing between the incremented PC and the branch address from the MEM stage.

Along with the four intermediate pipeline registers, we will also add a control line and a forwarding unit. We extend these registers to store the control lines passed from one stage to another. These registers would be timed to the clock and would either send the stored contents for additional processing or be flushed on each positive edge.

Let us now look at the changes made to the single cycle processor to implement the pipelining. In order to explain the changes made, we will be explaining each pipelining stage separately and the significance of the said stage.

4.1 Stage 1 - Instruction Fetch (IF)

Our processor's instruction fetch (IF) step is its initial operation. This stage, as its name implies, is responsible for reading the instruction from memory. To do this, it first determines the address of the instruction to be read through the PC counter, then reads the instruction from the Instruction memory module and sends it to the next stage through the IF/ID register. This also addresses the jump address if it is a problem.

The following is the module used in the stage.

```

1 module IF_ID(
2     input clk,
3     input reset,
4     input [31:0] instruction,
5     input [63:0] PC_Out,
6     input IF_write,
7     output reg [31:0] IF_ID_instruction,
8     output reg [63:0] IF_ID_PCOut
9 );
10
11 always @(posedge clk or reset)
12     begin
13         if (reset == 1'b1)
14             begin
15                 IF_ID_instruction = 0;
16                 IF_ID_PCOut = 0;
17             end
18         else if (clk==1 || IF_write == 1)
19             begin
20                 IF_ID_instruction = instruction;

```

```

21         IF_ID_PCOut = PC_Out;
22     end
23 end
24 endmodule

```

Listing 7: IF/ID Register

Before sending everything to the IF/ID register, which on the subsequent clock cycle would transfer the contents to the next step, the following connections are made. The intermediate connections between the Instruction Fetch stage and the Instruction decode stage are made by the outputs from this register.

4.2 Stage 2 - Instruction Decode (ID)

Our pipeline's second step is responsible for decoding the instruction, reading from registers, and writing to registers. Therefore, it begins by having the IF stage fetch the instruction. Once the 32-bit instruction has been decoded and its opcode, rd, rs1, and rs2 have been determined, it is then passed on to the instruction parser and the data extractor module. The RegisterFile then reads the contents of the registers or writes back to them (Note that writing back requires signals from the MEM/WEB register, indicating that it is a right-to-left operation, but it doesn't interrupt programme flow).

```

1 module ID_EX(
2     input clk,
3     input reset,
4     input branch,
5     input MemRead,
6     input MemtoReg,
7     input MemWrite,
8     input ALUsrc,
9     input RegWrite,
10    input [1:0] ALU_Op,
11    input [63:0] readdata1,
12    input [63:0] readdata2,
13    input [63:0] immediate,
14    input [63:0] pc_out,
15    input [4:0] rs1,
16    input [4:0] rs2,
17    input [4:0] rd,
18    input [3:0] func,
19    output reg branch_out, MemRead_out, MemtoReg_out,
20    MemWrite_out, ALUsrc_out, RegWrite_out,
21    output reg [1:0] ALU_Op_out,
22    output reg [63:0] readdata1_out, readdata2_out,
23    immediate_out, pc_out_out,
24    output reg [4:0] rs1_out, rs2_out, rd_out,
25    output reg [3:0] func_out
26 );

```

```

25
26     always @(*)
27     begin
28         if (reset==1'b1)
29             begin
30
31                 branch_out = 0;
32                 MemRead_out=0;
33                 MemtoReg_out=0;
34                 MemWrite_out=0;
35                 ALUsrc_out=0;
36                 ALU_Op_out=0;
37                 RegWrite_out=0;
38                 readdata1_out=0;
39                 readdata2_out=0;
40                 immediate_out=0;
41                 pc_out_out=0;
42                 rs1_out= 0;
43                 rs2_out=0;
44                 rd_out=0;
45                 func_out=0;
46
47             end
48         else if (clk==1)
49             begin
50                 MemRead_out=MemRead;
51                 MemtoReg_out=MemtoReg;
52                 MemWrite_out=MemWrite;
53                 ALUsrc_out=ALUsrc;
54                 ALU_Op_out=ALU_Op;
55                 RegWrite_out=RegWrite;
56                 readdata1_out=readdata1;
57                 readdata2_out=readdata2;
58                 immediate_out=immediate;
59                 pc_out_out=pc_out;
60                 rs1_out= rs1;
61                 rs2_out=rs2;
62                 rd_out=rd;
63                 func_out=func;
64             end
65         end
66     endmodule

```

Listing 8: ID/EX Register

4.3 Stage 3 - Execution (EX)

The third stage of our pipeline is the execution stage. This stage is responsible for performing the following two main tasks.

1. If the instruction is a branch instruction, the adder determines the offset value that must be added in order to determine the address of the subsequent location.
2. The ALU resides here, so all the operations are executed here.

The value that is to be sent to the registers is controlled by the two MUX after we obtained the ALUop from the Instruction Decode register, which is the control line for the ALU. We now shift our focus as to what exactly is the Execution stage carrying out.

```

1 module EX_MEM(
2     input clk, reset,
3     input [4:0] rd,
4     input [63:0] write_data ,
5     //input branch_MUX,
6     input [63:0] ALU_result, PC_out,
7     input zero, branch, MemRead, MemWrite, RegWrite,
8     MemtoReg,
9     output reg [4:0] rd_out,
10    output reg [63:0] write_data_out,
11    output reg [63:0] ALU_result_out,
12    output reg zero_out, branch_out, MemRead_out,
13    MemWrite_out, RegWrite_out, MemtoReg_out,
14    output reg [63:0] PC_out_out,
15    output reg branch_MUX_out
16);
17
18 always @(posedge clk ,posedge reset)
19     begin
20         if (reset==1)
21             begin
22                 PC_out_out=0;
23                 rd_out = 0;
24                 branch_out=0;
25                 MemRead_out=0;
26                 MemWrite_out=0;
27                 RegWrite_out=0;
28                 MemtoReg_out=0;
29                 write_data_out=0;
30                 ALU_result_out = 0;
31                 branch_MUX_out=0;
32                 zero_out=0;
33             end
34         else if (clk==1)
35             begin
36                 PC_out_out=PC_out;
37                 rd_out=rd ;
38                 write_data_out=write_data;

```

```

38         MemRead_out=MemRead;
39         MemWrite_out=MemWrite;
40         RegWrite_out= RegWrite ;
41         MemtoReg_out=MemtoReg ;
42         ALU_result_out=ALU_result ;
43         branch_MUX_out=ALU_result ;
44         zero_out= zero;
45         branch_out=branch;
46     end
47 end
48 endmodule

```

Listing 9: EX/MEM Register

4.4 Stage 4 - Memory Access (MEM)

The single module at this step is Data Memory, but it also serves as a register for sending back signals, so it checks to see if MemRead or MemWrite is high before carrying out the operation and setting the control lines to write data to or retrieve data from the memory. In order to handle data dangers, this also sends the register contents back to the Execution step for calculations. When the MemWrite signal is high, this register's primary function is to write data to the memory; when the MemRead signal is high, it reads data from the memory into the specified register. As a result, the MEM/WB transmits the register contents as well as additional control signals to the pipeline's final stage. The following stage is implemented into pipelining as follows;

```

1 module MEM_WB(
2     input clk,
3     input reset,
4     input reg_write,
5     input memtoreg,
6     input [4:0] rd,
7     input [63:0] ALU_result,
8     input [63:0] read_data,
9     output reg reg_write_out,
10    output reg mem_to_reg_out,
11    output reg [4:0] rd_out,
12    output reg [63:0] ALU_result_out,
13    output reg [63:0] read_data_out
14 );
15
16 always @(posedge clk or reset)
17     begin
18         if (reset==1'b1)
19             begin
20                 rd_out = 0;
21                 ALU_result_out = 0;
22                 read_data_out = 0;

```

```

23         reg_write_out= 0;
24         mem_to_reg_out= 0;
25     end
26     else if (clk)
27     begin
28         rd_out = rd;
29         ALU_result_out = ALU_result;
30         read_data_out = read_data;
31         reg_write_out= reg_write;
32         mem_to_reg_out= memtoreg;
33     end
34 end
35 endmodule

```

Listing 10: MEM/WB Register

5 Task 3 - Circuitry to Detect Hazards

5.1 Forwarding Unit

Let us say we have to run an arbitrary set of instructions on the pipelined version of the processor.

```

1 add x1, x2, x3
2 add x4, x1, x2

```

Listing 11: Arbitrary Set of instructions

Our processor would now execute the first instruction without issue, but let's try to analyse the second instruction. The second instruction would be in the Instruction decoding stage when the first instruction would be in the execution stage, and as we have seen, this stage is also responsible for reading the values of the register. Therefore, when reading the values stored in the register, the value in x1 for the second instruction should be the sum of the values in x2 and x3.

We refer to this as a data risk. We have methods like forwarding and stalling to get around this. The latter of the two is the more effective, and that is precisely what we use in our processor. In order to avoid waiting for the value to be loaded into the register before reading from it, forwarding delivers the value immediately after it has been calculated in the execution stage and is required in the ID stage.

A forwarding unit has been implemented in order to take care of hazards such as these. The following is the implementation of a forwarding unit in RISC-V.

```

1 module Forwarding_Unit(
2     input [4:0] ID_EX_Rs1,
3     input [4:0] ID_EX_Rs2,
4     input [4:0] EX_MEM_Rd,

```

```

5     input EX_MEM_RegWrite,
6     input [4:0] MEM_WB_Rd,
7     input MEM_WB_RegWrite,
8     output reg [1:0] Forward_A,
9     output reg [1:0] Forward_B
10 );
11
12     always @(*)
13     begin
14         if (EX_MEM_RegWrite == 1 && EX_MEM_Rd ==
15             ID_EX_Rs1 && EX_MEM_Rd != 0)
16         begin
17             Forward_A = 2'b10;    //10
18         end
19     else if (MEM_WB_Rd == ID_EX_Rs1 && MEM_WB_RegWrite
20         == 1 && MEM_WB_Rd != 0 &&
21             !(EX_MEM_RegWrite == 1 && EX_MEM_Rd != 0 &&
22                 EX_MEM_Rd == ID_EX_Rs1))
23     begin
24         Forward_A = 2'b01;    //01
25     end
26 else
27     begin
28         Forward_A = 2'b00;    //00
29     end
30
31 //FORWARD B LOGIC
32 if (EX_MEM_RegWrite == 1 && EX_MEM_Rd == ID_EX_Rs2
33     && EX_MEM_Rd != 0)
34     begin
35         Forward_B = 2'b10;    //10
36     end
37 else if (MEM_WB_Rd == ID_EX_Rs2 && MEM_WB_RegWrite
38     == 1 && MEM_WB_Rd != 0 &&
39     !(EX_MEM_RegWrite == 1 && EX_MEM_Rd != 0 &&
40         EX_MEM_Rd == ID_EX_Rs2))
41     begin
42         Forward_B = 2'b01;    //01
43     end
44 else
45     begin
46         Forward_B = 2'b00;    //00
47     end
48 end
49 endmodule

```

Listing 12: Forwarding Unit

Three scenarios should be taken into account for forwarding. The first one is EX Hazard, which sends the output of the preceding instruction to either of

the ALU's inputs. The multiplexor will select the value from register EX/MEM if the previous instruction was intended to write to the register file and the write register number was equal to the read register number of ALU inputs A or B. As was noted before, in the event of data hazard, the result is occasionally required directly from the MEM stage since, on occasion, the result is saved many times in a single register. As a result, to obtain the most current one, we take it directly from the MEM stage.

The forwarding logic for forwardA and forwardB is carried out according to the following table of conditions.

Mux control	Source	Explanation
ForwardA = 00	ID/EX	The first ALU operand comes from the register file.
ForwardA = 10	EX/MEM	The first ALU operand is forwarded from the prior ALU result.
ForwardA = 01	MEM/WB	The first ALU operand is forwarded from data memory or an earlier ALU result.
ForwardB = 00	ID/EX	The second ALU operand comes from the register file.
ForwardB = 10	EX/MEM	The second ALU operand is forwarded from the prior ALU result.
ForwardB = 01	MEM/WB	The second ALU operand is forwarded from data memory or an earlier ALU result.

```

1 module Four_MUX(
2     input [63:0] a, b, c, d,
3     input [1:0] sel,
4     output reg [63:0] mux_result
5 );
6
7     always @(*)
8     begin
9         if (sel==2'b00)
10            mux_result=a;
11        else if (sel ==2'b01)
12            mux_result=b;
13        else if (sel==2'b10)
14            mux_result=c;
15        else if (sel==2'b11)
16            mux_result=d;
17    end
18 endmodule

```

Listing 13: Four MUX

5.2 Hazard Detection Unit

Hazard detection unit is an essential component of pipelined processors that helps to detect and resolve hazards that can occur due to the pipelining of instructions. It enables the processor to handle instruction dependencies and avoid pipeline stalls or data hazards, thereby improving the performance of the

processor. The hazard detection unit is implemented in the following way in our processor.

```

1 module Hazard_detection_Unit(
2     input [4:0] if_id_rs1,
3     input [4:0] if_id_rs2,
4     input [4:0] id_ex_rd,
5     input MemRead,
6     output reg muxcontrolbit,
7     output reg PC_Write,
8     output reg If_id_write
9 );
10
11 always @(*)
12 begin
13     if ((if_id_rs2==id_ex_rd || if_id_rs1==id_ex_rd) &&
14         MemRead==1)
15     begin
16         muxcontrolbit=0;
17         PC_Write=0;
18         If_id_write=0;
19     end
20
21     else
22     begin
23         muxcontrolbit=1;
24         PC_Write=1;
25         If_id_write=1;
26     end
27
28 end
29 endmodule

```

Listing 14: Hazard Detection Unit

The hazard detection unit takes in input signals if_id_rs1, if_id_rs2, id_ex_rd, and MemRead, and outputs three signals muxcontrolbit, PC_Write, and If_id.write.

The inputs if_id_rs1 and if_id_rs2 represent the two source registers of the instruction that was fetched in the previous cycle. The input id_ex_rd represents the destination register of the instruction that was decoded in the previous cycle. The input MemRead is a control signal that indicates whether the current instruction is a load instruction that reads data from memory.

The hazard detection unit checks if any of the source registers of the current instruction match the destination register of the previous instruction, and whether the previous instruction was a load instruction that reads data from memory. If both conditions are true, then there is a data hazard, and the hazard detection unit sets the output signals accordingly. The muxcontrolbit output signal is set to 0, indicating that the multiplexer that selects the input to the register file should choose the result from the MEM/WB pipeline stage instead

of the EX/MEM pipeline stage. The PC_Write and If_id_write signals are set to 0, indicating that the current instruction should not update the program counter and the IF/ID pipeline register.

If there is no data hazard, then the hazard detection unit sets the output signals to 1, indicating that the current instruction can proceed without any stall or data forwarding. The muxcontrolbit output signal is set to 1, indicating that the multiplexer should select the result from the EX/MEM pipeline stage. The PC_Write and If_id_write signals are set to 1, indicating that the current instruction should update the program counter and the IF/ID pipeline register.

```

1 module Hazard_detection_MUX(
2     input sel,
3     input branch,
4     input MemRead,
5     input MemtoReg,
6     input MemWrite,
7     input ALUsrc,
8     input RegWrite,
9     input [1:0] ALU_Op,
10    output reg branch_eq_hazard,
11    output reg MemRead_hazard,
12    output reg MemtoReg_hazard,
13    output reg MemWrite_hazard,
14    output reg ALUsrc_hazard,
15    output reg RegWrite_hazard,
16    output reg [1:0] ALU_Op_hazard
17 );
18
19 always @ (*)
20 begin
21     if (sel==0)
22     begin
23         branch_eq_hazard=0;
24         MemRead_hazard=0;
25         MemtoReg_hazard=0;
26         MemWrite_hazard=0;
27         ALUsrc_hazard=0;
28         RegWrite_hazard=0;
29         ALU_Op_hazard=0;
30     end
31     if (sel==1)
32     begin
33         branch_eq_hazard=branch;
34         MemRead_hazard=MemRead;
35         MemtoReg_hazard=MemtoReg;
36         MemWrite_hazard=MemWrite;
37         ALUsrc_hazard=ALUsrc;
38         RegWrite_hazard=RegWrite;
39         ALU_Op_hazard=ALU_Op;
40     end

```

```

41     end
42 endmodule
43

```

Listing 15: Hazard Detection MUX

The multiplexer selects between two sets of input signals based on the value of the `sel` input. The output signals `branch_eq_hazard`, `MemRead_hazard`, `MemtoReg_hazard`, `MemWrite_hazard`, `ALUsrc_hazard`, `RegWrite_hazard`, and `ALU_Op_hazard` are set based on the selected input signals.

The input signals to the hazard detection unit are `branch`, `MemRead`, `MemtoReg`, `MemWrite`, `ALUsrc`, `RegWrite`, and `ALU_Op`. These signals represent various control signals that determine how an instruction should be executed.

The first set of input signals is selected when the `sel` input is 0. In this case, all the output signals are set to 0, indicating that there is no hazard. This is the default state of the hazard detection unit.

The second set of input signals is selected when the `sel` input is 1. In this case, the output signals are set based on the input signals. The `branch_eq_hazard` output signal is set to the value of the `branch` input, indicating that there is a branch hazard if the `branch` input is asserted. The `MemRead_hazard` output signal is set to the value of the `MemRead` input, indicating that there is a memory read hazard if the `MemRead` input is asserted. The `MemtoReg_hazard` output signal is set to the value of the `MemtoReg` input, indicating that there is a memory-to-register hazard if the `MemtoReg` input is asserted. The `MemWrite_hazard` output signal is set to the value of the `MemWrite` input, indicating that there is a memory write hazard if the `MemWrite` input is asserted. The `ALUsrc_hazard` output signal is set to the value of the `ALUsrc` input, indicating that there is an ALU source hazard if the `ALUsrc` input is asserted. The `RegWrite_hazard` output signal is set to the value of the `RegWrite` input, indicating that there is a register write hazard if the `RegWrite` input is asserted. The `ALU_Op_hazard` output signal is set to the value of the `ALU_Op` input, indicating that there is an ALU operation hazard if the `ALU_Op` input is asserted.

6 Results

We will now test our final design. We will check if the pipelined processor is working as intended.

Firstly, checking if the values are being loaded into the processor correctly.

Checking if the sorting is working correctly and the following is our final sorted result.

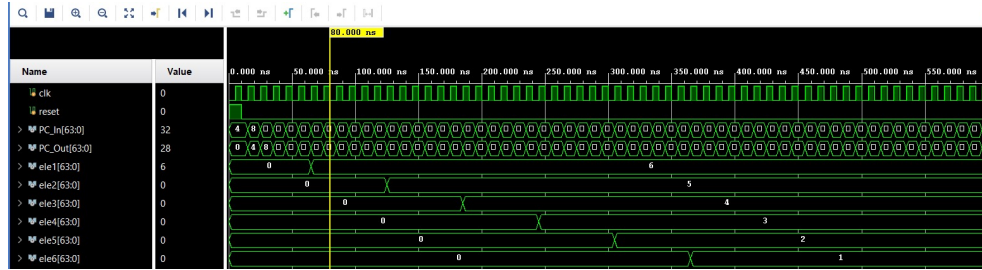


Figure 3: Loading the set of inputs

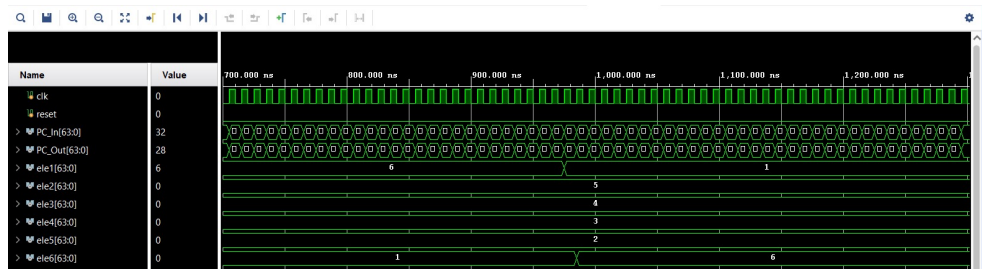


Figure 4: Sorting the set of inputs

The final thing is to check if the forwarding is working correctly according to the conditions put in place for the forwarding unit to work correctly.

6.1 Comparison between Pipelined and non-Pipelined Single Cycle Processor

Performance for a pipelined Single-cycle processor will be better when compared to a non-pipelined single cycle processor. A pipelined processor and a non-pipelined processor are both single processors, but they differ in how they handle instructions.

A non-pipelined processor executes each instruction in a sequential manner, meaning it completes one instruction before moving on to the next. This can lead to inefficiencies because there may be unused portions of the processor during the execution of an instruction. On the other hand, a pipelined processor breaks down the execution of each instruction into several stages and allows multiple instructions to be processed at the same time. As a result, there is no idle time for the processor, and instructions are executed more quickly.

A pipelined processor is generally faster and more efficient than a non-pipelined processor because it can process instructions simultaneously and this is exactly what we have seen over the course of this semester and the project. However, while designing a pipelined single-cycle processor, one has to keep in mind to not add bottlenecks and add remedies to data hazards for the processor

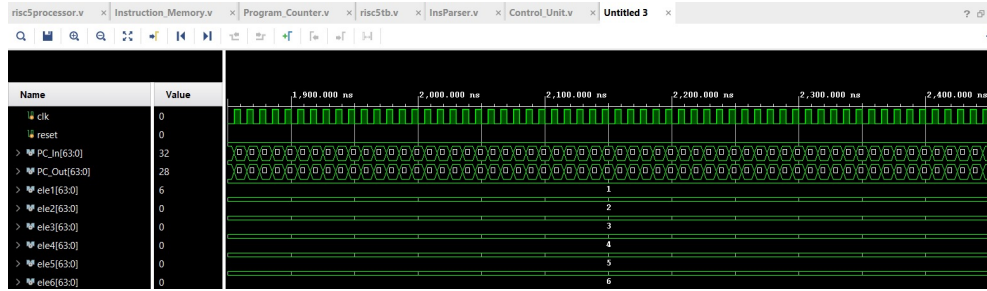


Figure 5: Final Sorted set of elements

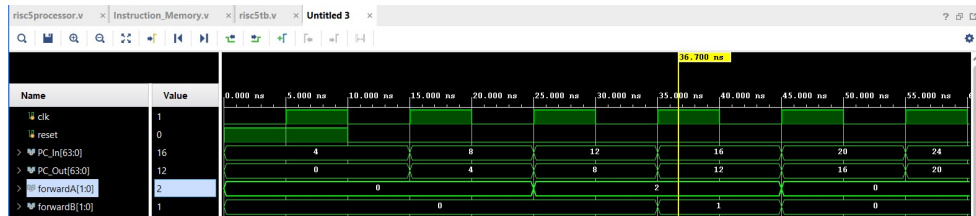


Figure 6: Result of Forwarding Unit

to work efficiently.

7 Final Comments

The project has been a unique challenge in a way that it required tedious amounts of debugging the code and modules to figure out what the problem is. At times even after hours of trying to figure out the problem, we could not reach to a correct conclusion. As a result, branching has not been implemented properly in our project, while forwarding unit and hazard detection is working. The failure to implement branching correctly is not down to a lack of effort and time, but guessing it is rather down to a very small error which is not visible to the eye.

8 Github Repository

<https://github.com/HammadxSaj/CA-Project>