EEE6206 Power Semiconductor Devices:

Section 2c: Power Diodes

Power diodes

- Used in applications which require current to flow in one direction
- Main application is rectification
  - Alternating current (AC) is converted to direct current (DC)
- Current ratings of individual device range from less than 1A to 1000’s A
- Voltage rating could vary from 10V to 1000’sV
- As well as ratings for continuous operation ratings device need to withstand surges of current that may last for a few tenth's of a second

- Most often power diode make us of the rectifying action of a P-N junction
  - Although high voltage rectifying Schottky contacts are now being used for wide band gap semiconductor (Silicon Carbide)
- As well as being capable of blocking the required reverse voltage in the off-state, power diodes require a low forward voltage drop in the on-state
- In many applications a rapid transition from the forward conducting to the reverse blocking is require

Fundamental differences between low voltage and high voltage

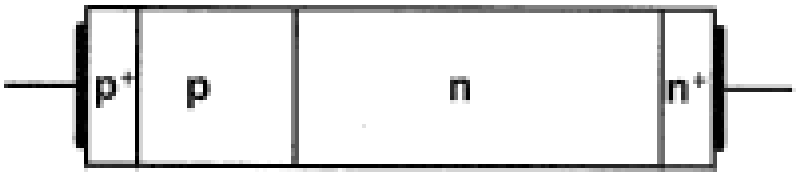
- Power device: Delivers more than 1W to a load
- A Power Semiconductor device must:
  - Support the designed voltage when it is ‘OFF’ with very low leakage current
  - Enable current conduction with minimum voltage drop
  - Scalable to deliver the designed current
  - Switch ON and OFF as quickly as possible
  - Be reliable for operation with wide safe operating area
  - Be able to operate at high and low temperatures
  - Be manufacturable

Forward biased diode

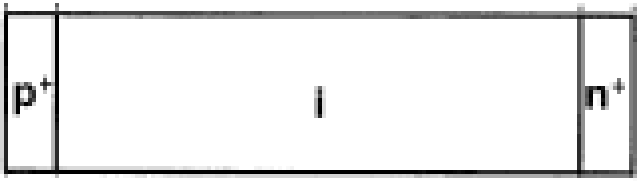
- When the p-n junction is forward biased
  - Holes are injected into the n-type region
  - Electrons are injected into the p-type region
- These regions are bounded by n+ and p+ layers in which the carrier concentration are several orders of magnitude higher (1e19-1e20 #cm^3)
  - Excess carrier concentrations injected into the p-n regions can be many times higher than the equilibrium majority carrier concentrations
- These excess carriers modify the conductivity of the n-type and p-type regions with such an extent
  - Termed **conductivity modulation**: Principle used in high power bipolar semiconductor devices (Power diodes, BJT's, ITBS's, SCR's and GTO's)
- Only at low current densities that a p^+pnn^+ junction behaves like a simple p-n junction
- At high current density levels
  - Theoretical analysis is made simpler by using a p-i-n diode approximation

Carrier distribution across a p-i-n diode

Power diode structure

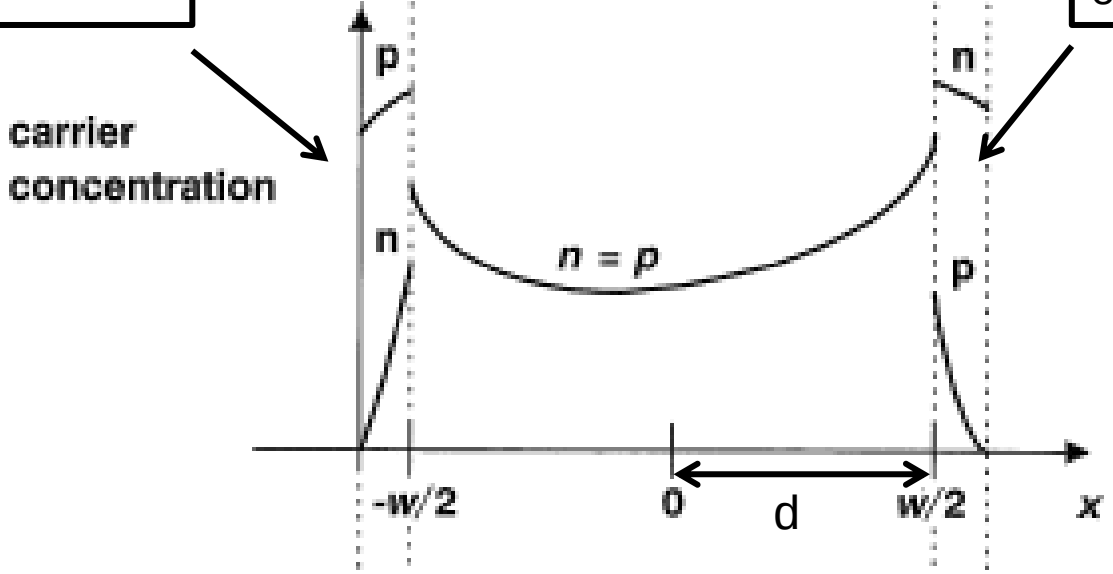


p^+-i-n^+ simplification



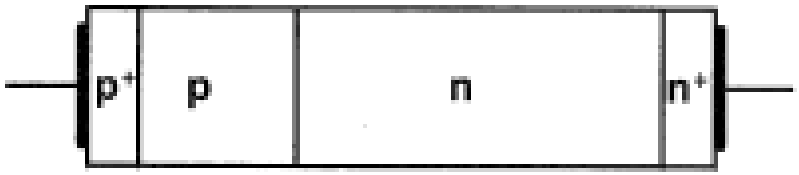
P+ region:
Current is carried almost entirely of holes

N+ region:
Current is carried almost entirely of electrons

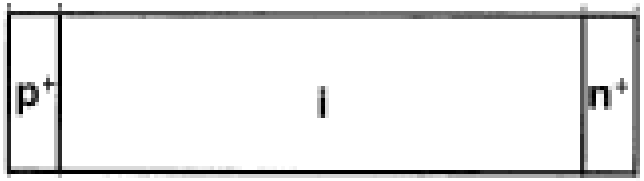


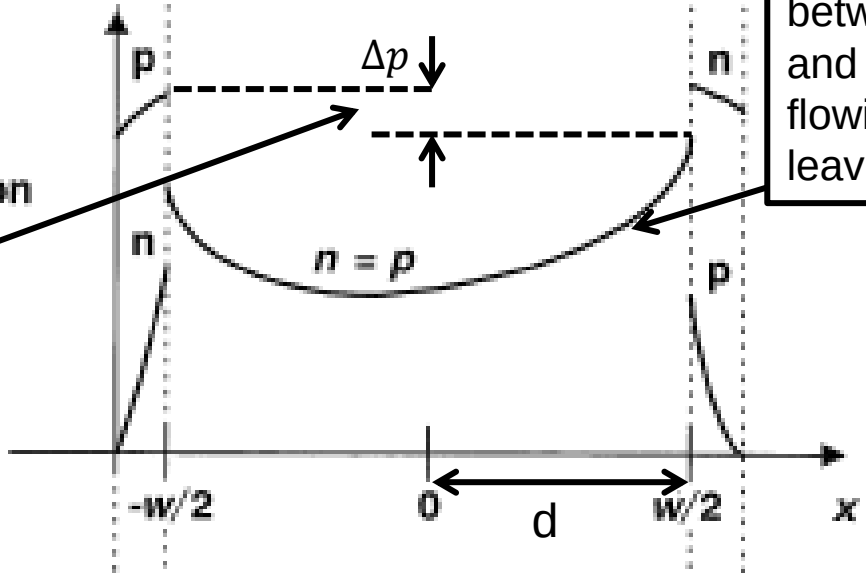
Carrier distribution across a p-i-n diode

Power diode structure



p^+-i-n^+ simplification



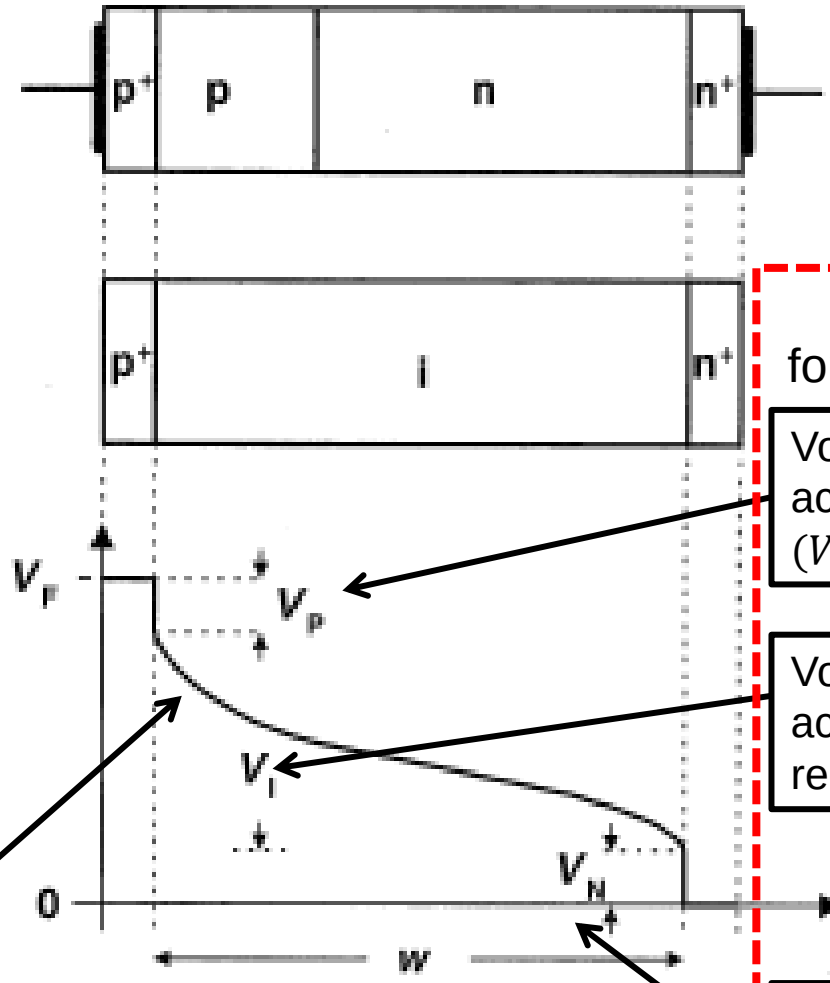


Carrier concentrations in the i region rise until recombination rate balances the difference between the electron and hole currents flowing into and those leaving the structure

The difference between the hole current injected from the p+ contact and continuing into the n^+ contact is accounted from by recombination within the i region (same is true when considering the injected electrons from the n^+ region)

Potential distribution across a p-i-n diode

A minute imbalance in carrier concentrations is sufficient to provide the variation of electric field that is required to control of the distributions of the electron and holes current in the i region



This gives rise to a potential distribution through the structure

Components of forward voltage drop

Voltage dropped across the p⁺ i junction (VP)

Voltage dropped across the middle region (Vi)

Voltage dropped across the n⁺ i junction (V_n)

Components of forward voltage drop

- Forward voltage drop can be expressed as

$$V_F = V_p + V_i + V_n$$

- V_p and V_n are the voltage dropped across the p^+/i and n^+/i junctions
- V_i is the voltage dropped across the middle region of the diode
  - Varies with current density and with the width (w) of the i (n-) region
  - What is important in this region is the ratio of width (w) to ambipolar diffusion length (La)

Ambipolar diffusion length

Ambipolar diffusion length → $L_a = \sqrt{D_a \tau_H}$ ← Minority carrier lifetime under high level injection conditions $(n(x) = p(x))$

Ambipolar diffusion constant

- Ambipolar diffusion length
  - Process of diffusion of negative and positive carriers due to their interaction with an electric field
    - Analogous to the electron and hole diffusion lengths

$$D_a = \frac{2D_n}{1 + \frac{\mu_n}{\mu_p}} = \frac{2D_p}{1 + \frac{\mu_p}{\mu_n}}$$

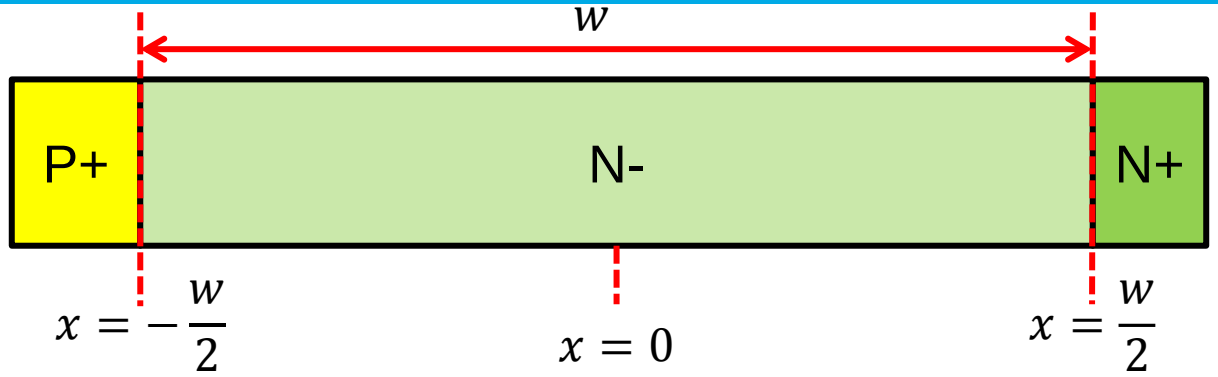
- Using the values of carrier mobility approximate to lightly doped silicon at room temperature

$$\mu_n = 1420\ cm^2/V\ s \qquad \mu_p = 470 cm^2/V\ s$$

$$\mu_n = 3\mu_p$$

Therefore: $D_a = 0.5D_n = 1.5D_p = 53.7cm^2\ s$

Co-ordinate system for analysis



- Starting from the continuity equation:

$$\frac{d\Delta n}{dt} = \Delta n \mu_n \frac{dE}{dx} + \mu_n E \frac{d\Delta n}{dx} + D_n \frac{d^2\Delta n}{dx^2} + G_n - \frac{\Delta n}{\tau_n}$$

- Assuming conditions for electrical neutrality ($\Delta n = \Delta p$), no carrier generation ($G_n = G_p = 0$) and diffusion driven current:
- For excess electron concentration:

$$\frac{d^2\Delta n}{dx^2} - \frac{\Delta n}{D_a \tau_H} = 0 \qquad \frac{d^2\Delta n}{dx^2} = \frac{\Delta n}{{L_a}^2}$$

Electric field distribution from the n side

- Boundary conditions are determined by the current density J
  - Fixed by the external circuit
- Assuming 100% injection efficiency at the n^+/n^- junction and that the hole current in this region is zero
- However in the i region carrier concentrations of both carrier types are equal (high injection condition $(n(x) = p(x))$
  - Therefore the electric field strength needed to reduce the flux of holes to zero at $x = d$
  - This is obtained by applying the current density equation for holes to our one dimensional situation:

$$J_p(x=d) = pq\mu_p E_{(x=d)} - qD_p \left.\frac{dp}{dx}\right|_{x=d} = 0 \qquad pq\mu_p E_{(x=d)} = qD_p \left.\frac{dp}{dx}\right|_{x=d}$$

$$E_{(x=d)} = \left.\frac{D_p}{p\mu_p}\frac{dp}{dx}\right|_{x=d} = \left.\frac{kT}{qp}\frac{dp}{dx}\right|_{x=d}$$

$$E_{(x=d)} = \left.\frac{kT}{qn}\frac{dn}{dx}\right|_{x=d}$$

Carrier distribution boundaries at the anode and cathode

- If we consider electron current flowing out of the system and substitute the previous equitation for $E(d)$ and re-applying Einstein's relation
  - The current density which is due to electron at the cathode ($x = d$) is given by:

$$J_e = q\mu_n n E_{(d)} + qD_n \left.\frac{dn}{dx}\right|_{x=d}$$

$$J_e = qn\mu_n \left.\frac{kT}{qn}\frac{dn}{dx}\right|_{x=d} + qD_n \left.\frac{dn}{dx}\right|_{x=d} = qn\mu_n \left.\frac{D_n}{\mu_n n}\frac{dn}{dx}\right|_{x=d} + qD_n \left.\frac{dn}{dx}\right|_{x=d}$$

$$J_e = qD_n \left.\frac{dn}{dx}\right|_{x=d} + qD_n \left.\frac{dn}{dx}\right|_{x=d} = 2qD_n \left.\frac{dn}{dx}\right|_{x=d}$$

- Hence:

$$\left.\frac{dn}{dx}\right|_{x=d} = \left.\frac{d\Delta n}{dx}\right|_{x=d} = \frac{\boldsymbol{J}}{\boldsymbol{2qD_n}}$$

- Applying the same arguments to the anode side ($x = -d$):

$$\left.\frac{dp}{dx}\right|_{x=-d} = \left.\frac{d\Delta p}{dx}\right|_{x=-d} = \frac{\boldsymbol{J}}{\boldsymbol{2qD_p}}$$

On-state carrier distribution

- The solution of the continuity has to satisfy the boundary conditions imposed by the previous two equations
  - The carrier distribution in the i region can be expressed as:

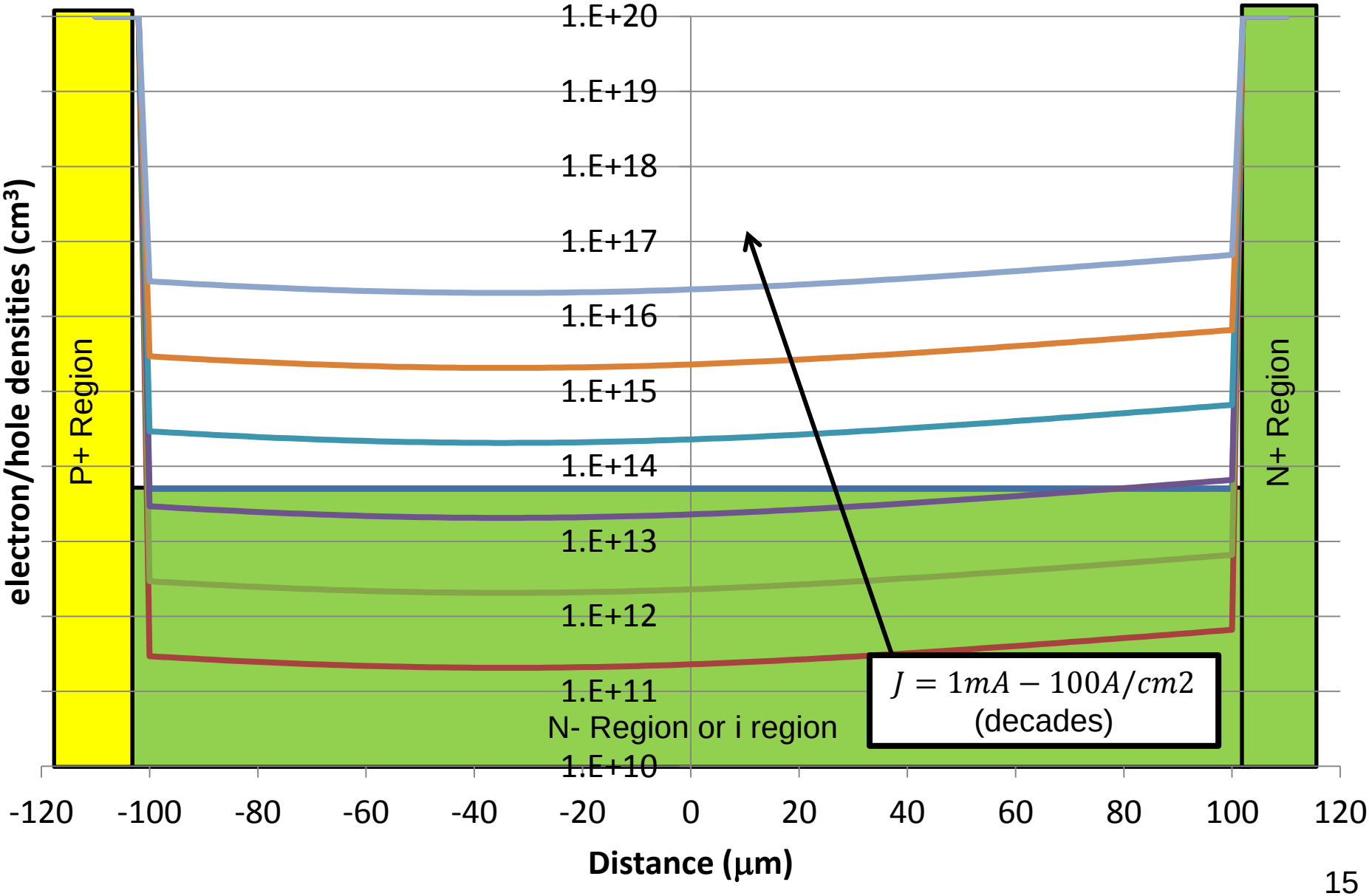
$$\Delta n(x) = \frac{J\tau_{HL}}{2qL_a}\left[\frac{cosh\left({}^{x}/_{L_a}\right)}{sinh\left({}^{d}/_{L_a}\right)} - \delta\frac{sinh\left({}^{x}/_{L_a}\right)}{cosh\left({}^{d}/_{L_a}\right)}\right]$$

- Where:

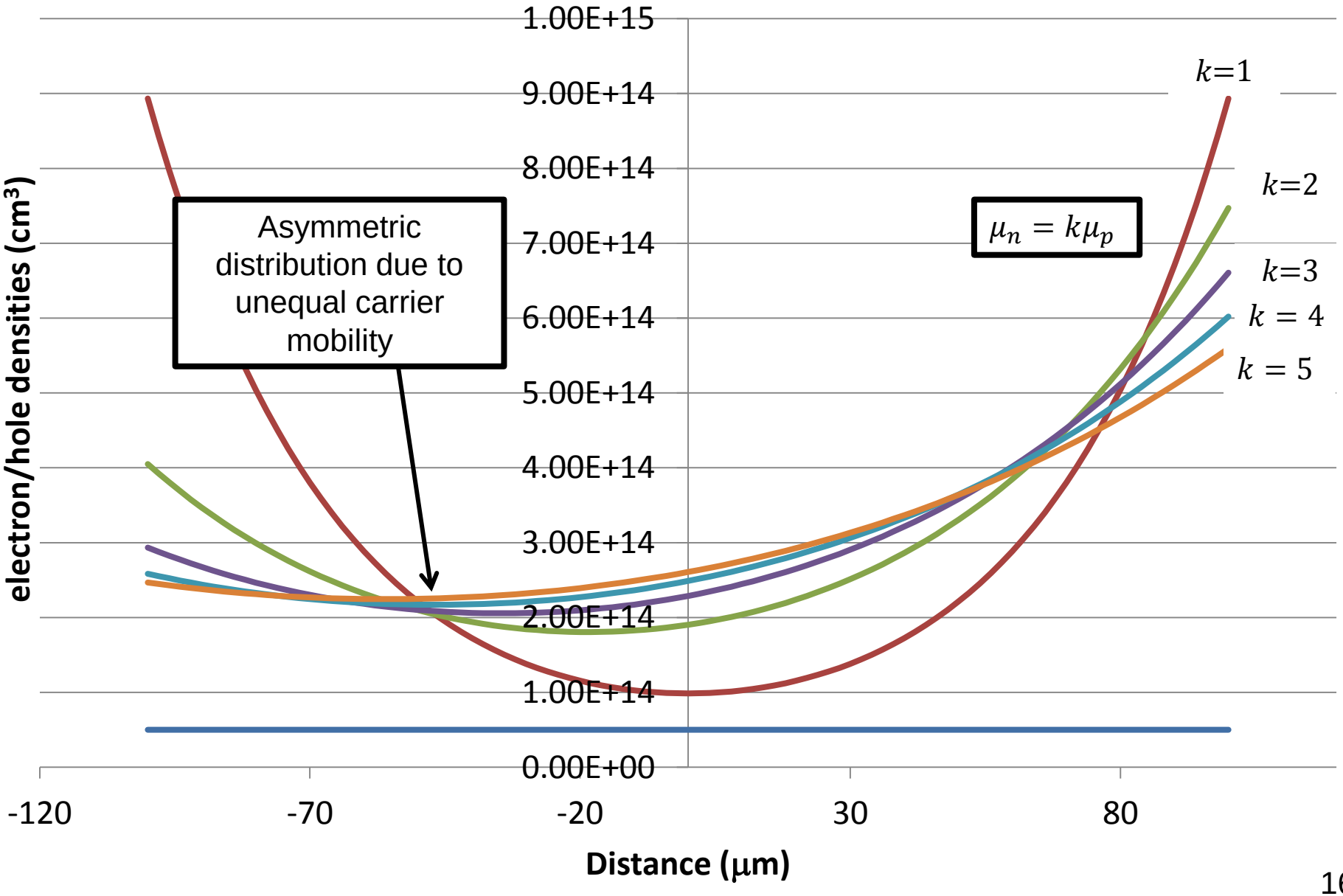
$$\delta = \frac{\mu_n - \mu_p}{\mu_n + \mu_p}$$

- Note: high carrier injection conditions exist
  - $\Delta n(x) = \Delta p(x)$

On-state carrier distribution with respect to current density: Conductivity Modulation



Effect of electron/hole mobility ratio upon carrier distribution



- At any point between $-d$ and d current density is given by the sum of the drift and diffusion components of each carrier type

$$J = J_n + J_p = \underbrace{q\left(n\mu_n + p\mu_p\right)E_{(x)}}_{\text{Current due to Carrier drift}} + \underbrace{q\left(D_n\frac{dn}{dx} - D_p\frac{dp}{dx}\right)}_{\text{Current due to Carrier diffusion}}$$

- Which can be written as:

$$J = q\Delta n\left(\mu_n + \mu_p\right)E_{(x)} + kT\left(\mu_n - \mu_p\right)\frac{d\Delta n}{dx}$$

- Assuming that the excess carrier concentrations in the n- region can be represented by the excess carrier concentration Δn
- Electric field strength can be expressed as:

$$E_{(x)} = \frac{J}{q\left(\mu_n + \mu_p\right)\Delta n(x)} - \frac{kT}{q\Delta n(x)}\delta\frac{d\Delta n}{dx} \quad where\ \delta = \frac{\left(\mu_n - \mu_p\right)}{\left(\mu_n + \mu_p\right)}$$

- The integral of the electric field distribution yield the voltage drop across the n- region

$$\frac{V_i}{kT/q} = \begin{cases} \dfrac{8b}{(b+1)^2} \dfrac{\sinh\left(d/L_a\right)}{\sqrt{1-\delta^2 \tanh^{2(d/La)}}} \\ \times \tan^{-1}\left[\sqrt{1-\delta^2 \tanh^2\left(d/L_a\right)}\sinh\left(d/L_a\right)\right] \end{cases}$$

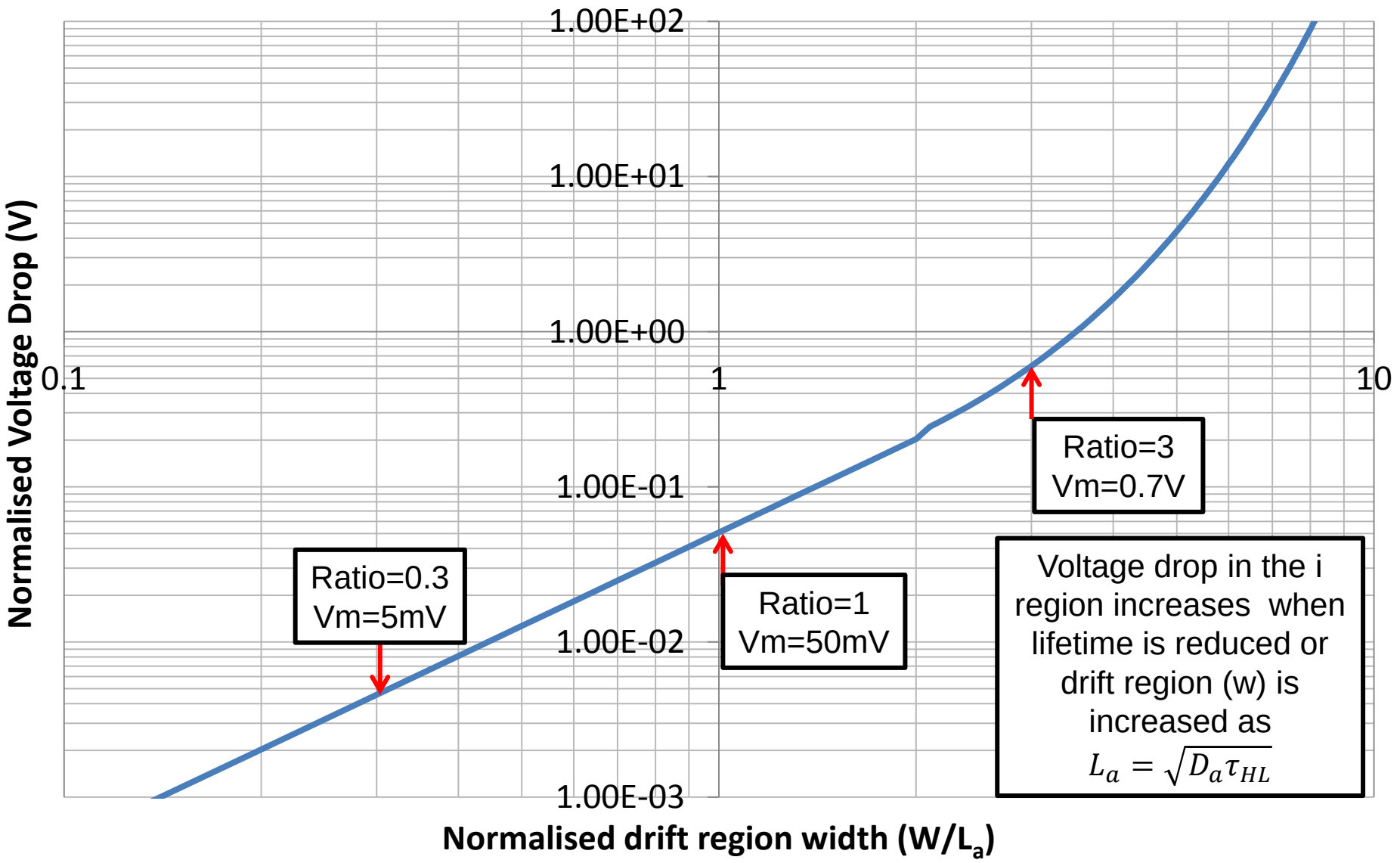
$$+ B\ln\left[\frac{1+\delta\tanh^2\left(d/L_a\right)}{1-\delta\tanh^2\left(d/L_a\right)}\right] \qquad where\ b = \frac{\mu_n}{\mu_p}$$

- This can be simplified to:

$\boldsymbol{V_i = \frac{2kT}{q}\left(\frac{d}{L_a}\right)^2}$ for $\frac{d}{L_a}$ ratio's up to 2 (short base diode)

$\boldsymbol{V_i = \frac{3\pi kT}{8q} e^{\left(\frac{d}{L_a}\right)}}$ for $\frac{d}{L_a}$ ratio's greater than 2 (long base diode)

Effect of lifetime and drift region width upon voltage drop



Voltage drop at the n+ p+ junctions

- The voltage dropped across the p^+ / i junction can be determined from the minority carrier density

$$p_{(-d)} = p_{on} exp^{\left(\frac{qV_{p+}}{kT}\right)}$$

- Relating the minority carrier density in equilibrium (p_{on}) to the doping level in the drift region (i)

$$V_{P+} = \frac{kT}{q} ln\left(\frac{p_{(-d)} N_D}{{n_i}^2}\right)$$

- Applying the "Junction Law" on the cathode side (n^+/i region)

$$n_{(d)} = n_{on} exp^{\left(\frac{qV_{n+}}{kT}\right)}$$

- Where n_{on} is the majority carrier density in the drift region (i) and V_{n+} is the voltage drop across the n^+/i junction which gives

$$V_{n+} = \frac{kT}{q} ln \frac{n_{(d)}}{N_D}$$

Power diode forward voltage drop

- The total voltage drop associated with the two end region is given by:

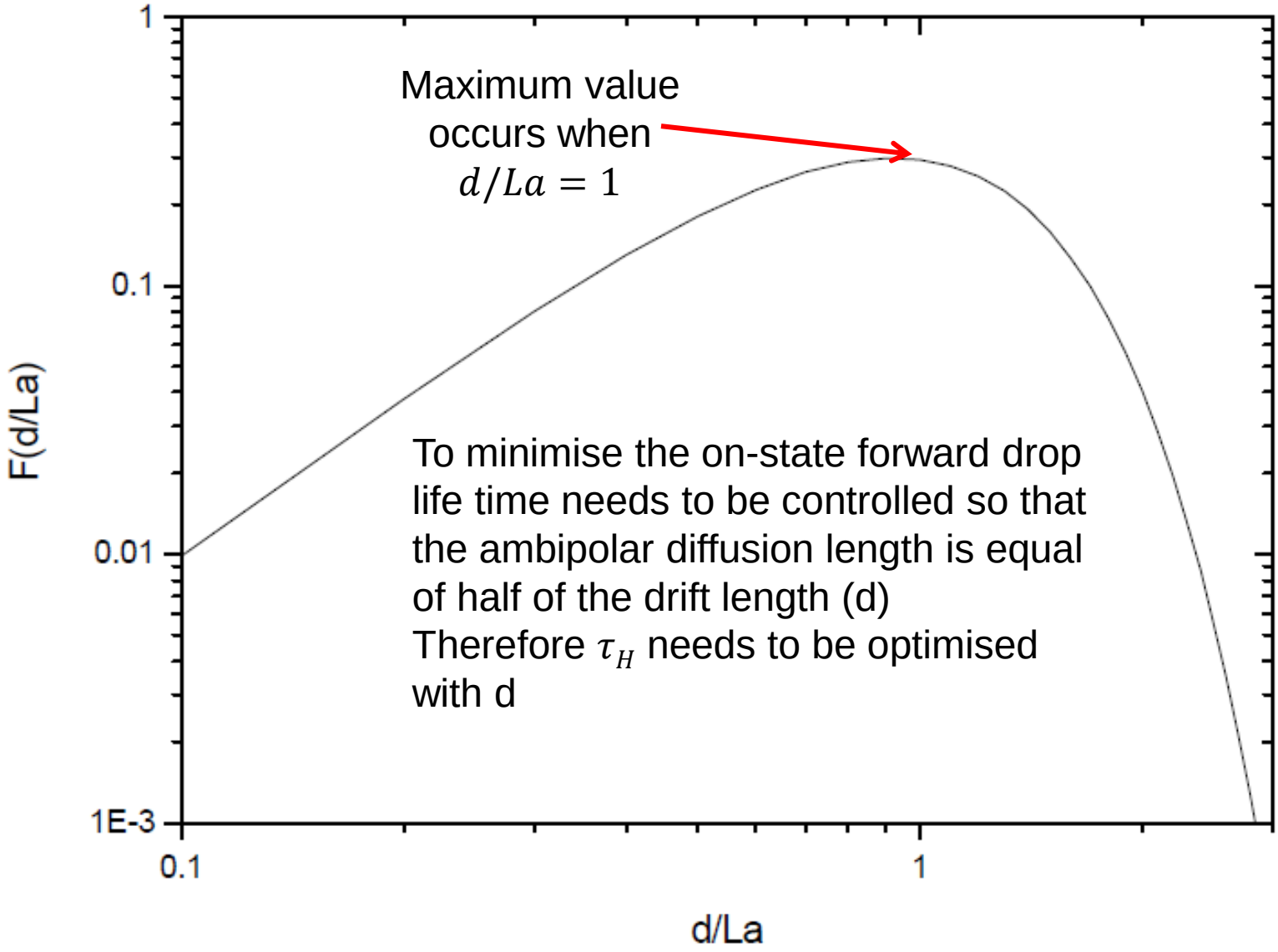
$$V_{P+} + V_{n+} = \frac{kT}{q} ln \left[\frac{n_{(w/2)} n_{(-w/2)}}{{n_i}^2} \right]$$

- Assuming charge neutrality under high carrier injection levels $(n(x) = p(x))$
- Combining this with the middle region gives the current voltage relationship of the p-i-n rectifier

$$J_T = \frac{2qD_a n_i}{d} F\left(\frac{d}{L_a}\right) exp^{\left(\frac{qV_{on}}{2kT}\right)}$$

Where: $F\left(\frac{d}{L_a}\right) = \frac{(d/L_a)\tanh(d/L_a)}{\sqrt{1-0.25tanh^4(d/L_a)}} exp^{-qV_m/2kT}$

Function F(d/La) for a PiN rectifier



Secondary effects: End region carrier injection

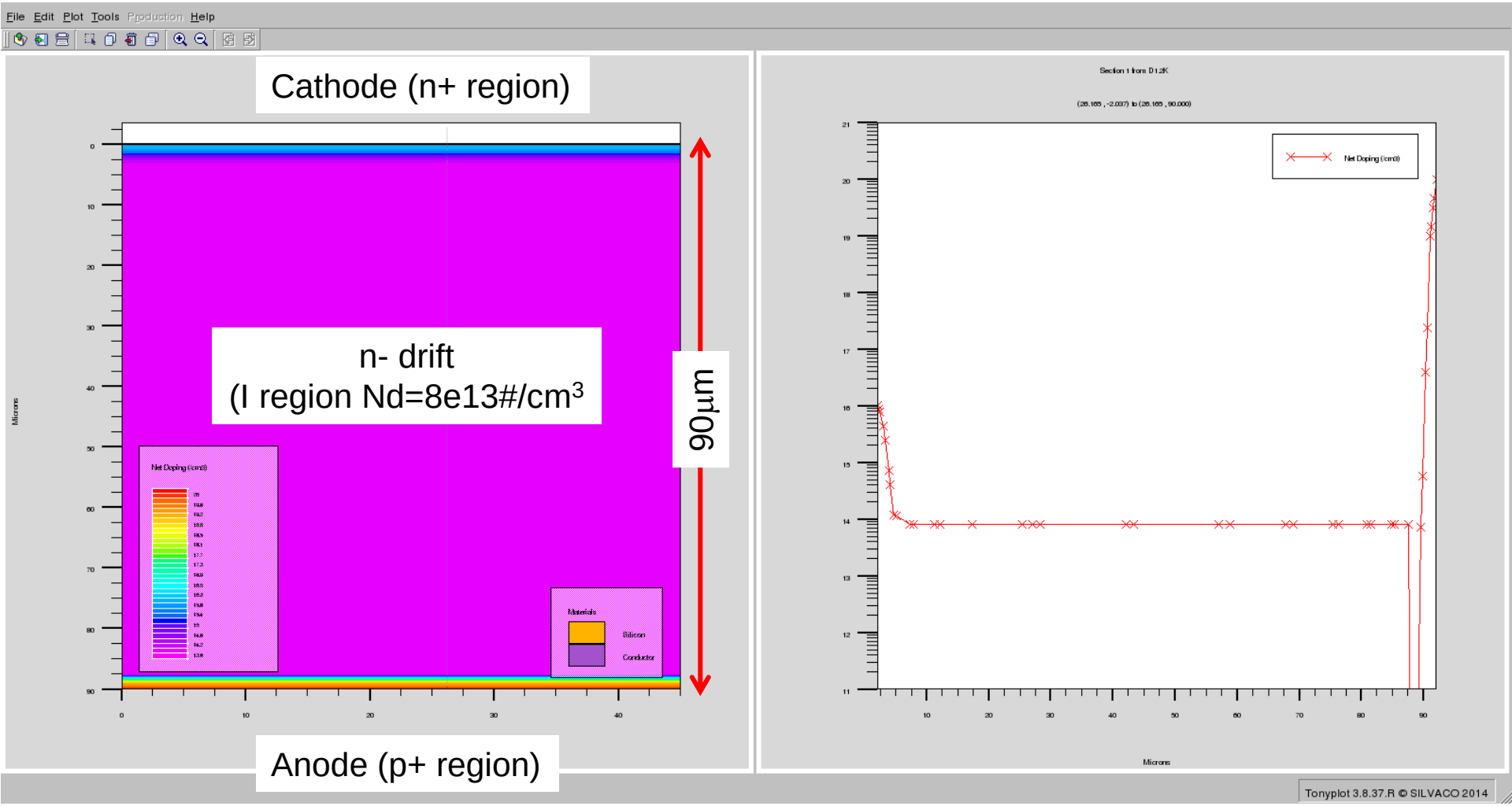
- The previous analysis describes the on-state forward voltage drop at a typical operating current density of 100-200A/cm^2
- As current increases secondary effects start to determine the on-state resistance
  - Carrier injection in the n+/p+ end regions
    - This reduces the injection level into the drift region
    - Reduces carrier density in the drift region resulting in an increased forward voltage drop

Secondary effects (increased scattering and recombination)

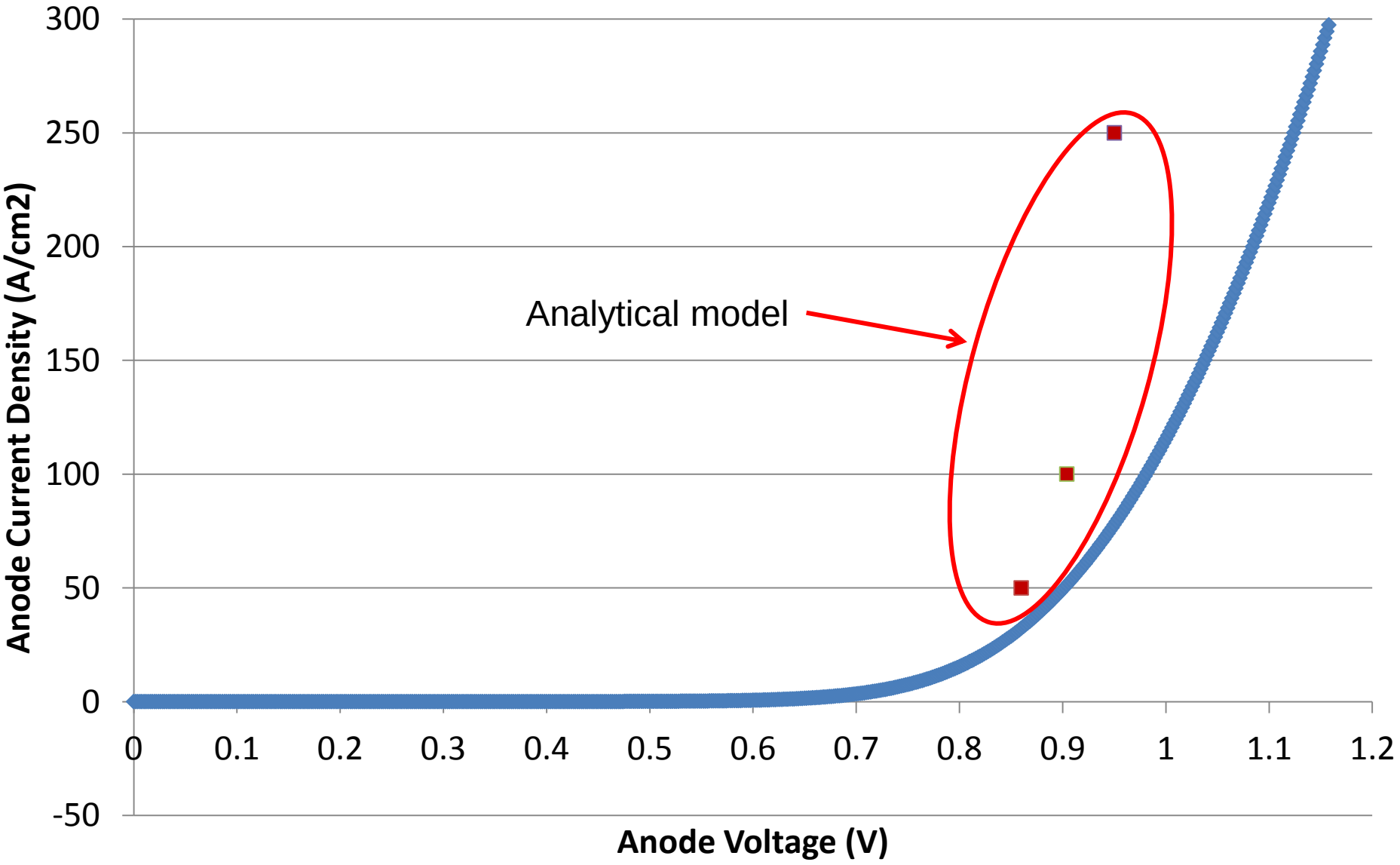
- Carrier-carrier scattering
  - High concentrations of injected electrons and holes within the drift region increases the probability of scattering between charge carriers and a reduction of mobility
- Auger recombination
  - Large carriers within the drift region increases the probability of Auger recombination
  - This can also occur in the highly doped anode and cathode regions due to the large minority carrier concentrations as a result of large current densities

- Both processes increase the recombination rate within the drift and end regions, increasing forward voltage drop

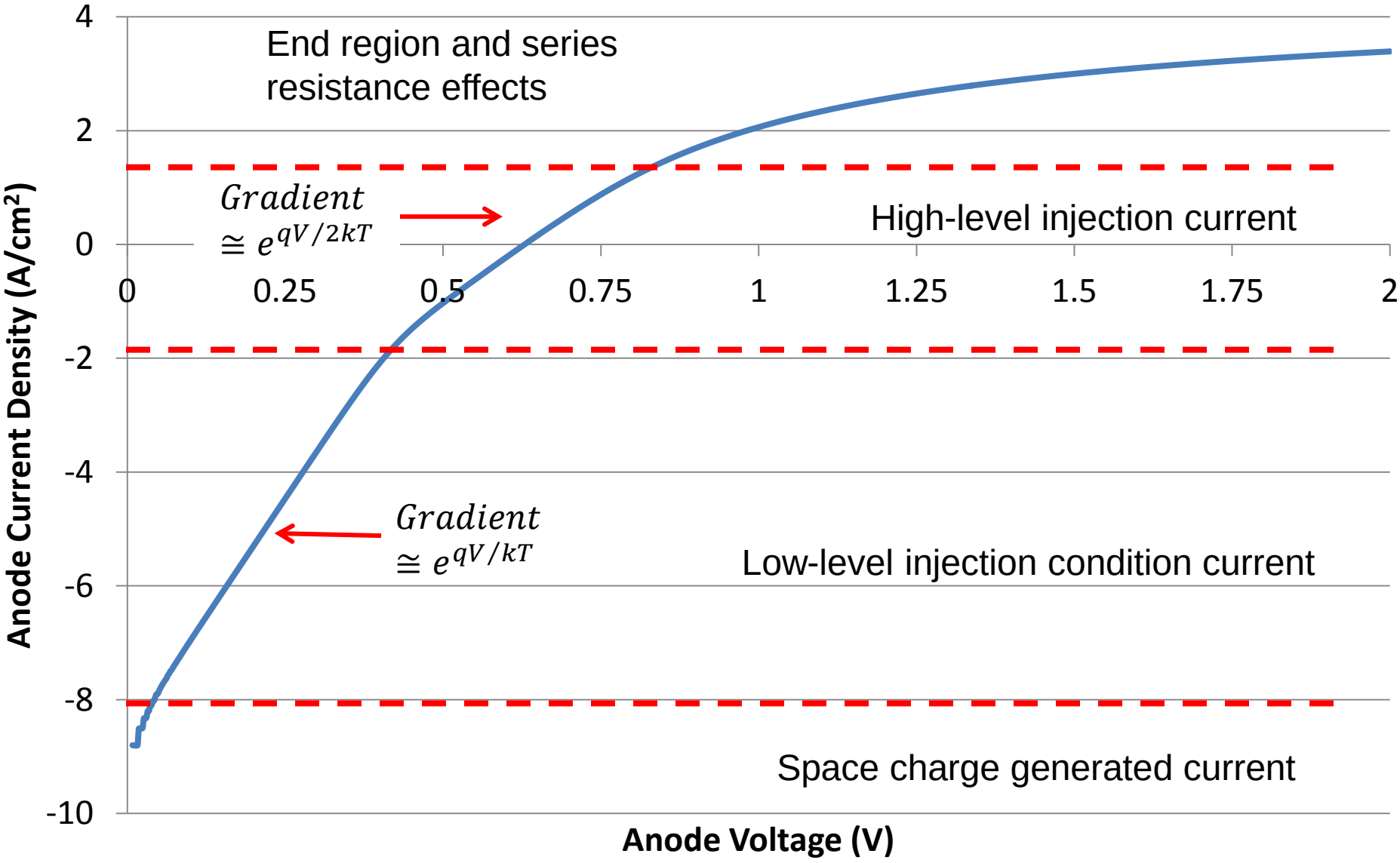
1200V PiN diode simulation example



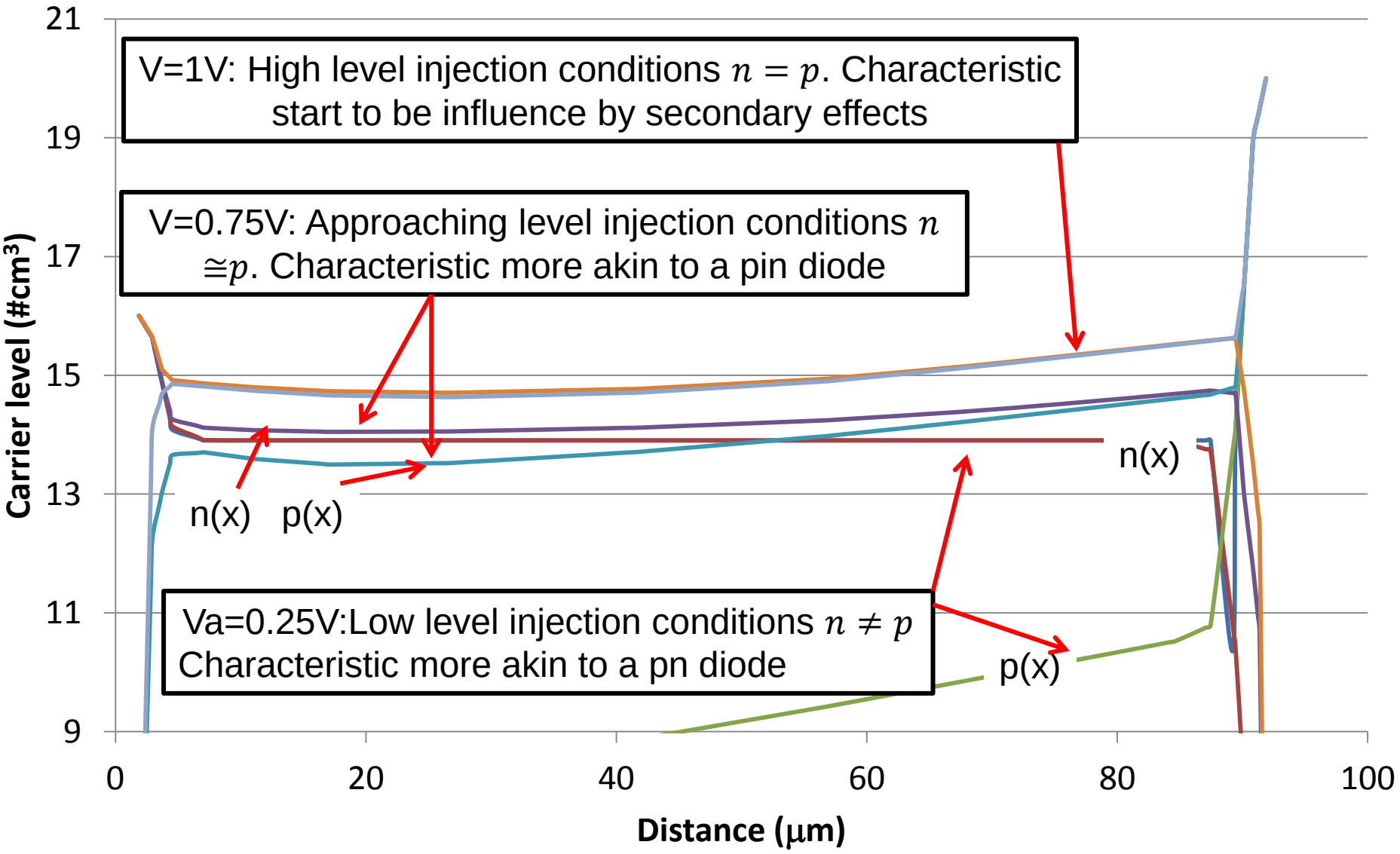
Simulated current voltage characteristics of a 1200V PiN diode τ_{HL}=0.1e-6μs



Simulated current voltage characteristics of a 1200V PiN diode τ_{HL}=0.1e-6μs (log, linear scale)



Simulated carrier profiles with respect to applied anode bias



Reverse bias PiN diodes

Power devices in contrast to memory

- Unique feature of power semiconductor devices is their ability to withstand high voltages
  - Transistors designed for microprocessors and semiconductor memories
    - Pressure to reduce feature sizes and increase integration and resulted in a reduction in size
  - In contrast
    - The desire to control large power levels in motor drives and power distribution system has encouraged the development of power devices with larger breakdown voltages

Breakdown requirement

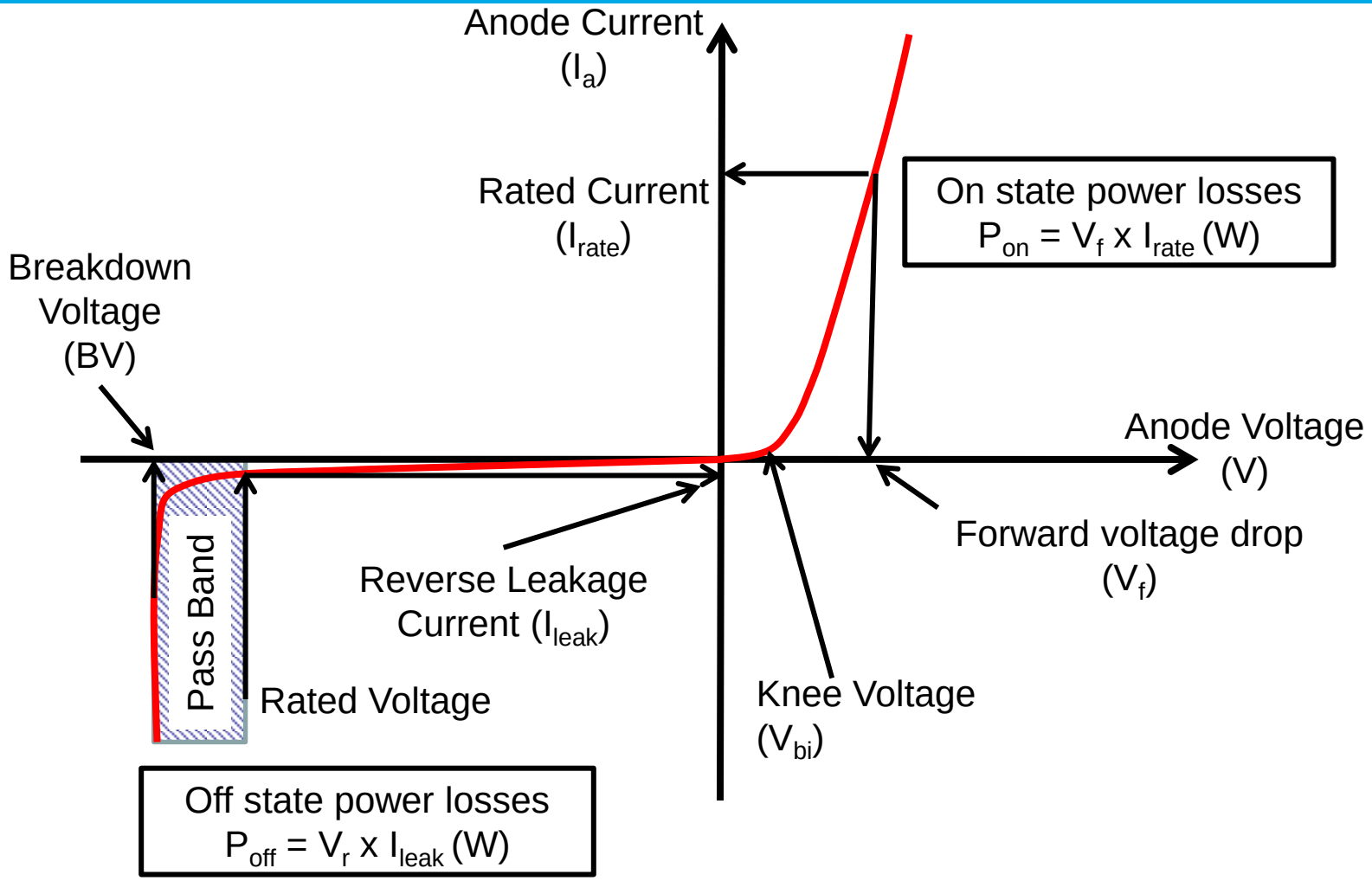
- In the semiconductor the ability to support high voltage without the onset of significant current flow is limited by the avalanche breakdown phenomenon
  - Dependent upon the electric field distribution in the structure
  - High electric fields can be created within the interior of power devices as well as their edges
- The design optimisation of power device must be performed to meet the breakdown voltage requirement for the target application whilst minimising the on-state voltage drop so that power dissipation is minimised

A note on doping concentrations and definitions

- Depending upon their doping concentration different abbreviations are used to define their doping concentrations

Short hand	Definition	General use
n+	Heavily doped n-type semiconductor (degenerate)	Ohmic contacts to n semiconductor regions
n	Normally doped n-type semiconductor (non-degenerate)	n doped regions
n- or (ν)	Lightly doped n-type semiconductor	n type voltage sustaining regions
i	Intrinsic semiconductor (fully compensated)	Generally not used apart for simplification of device characteristics
p- or (π)	Lightly doped p- type semiconductor	P type voltage sustaining regions
p	Normally doped p-type semiconductor (non-degenerate)	P type regions
p+	Heavily doped p-type semiconductor (degenerate)	Ohmic contacts to p type semiconductor regions

Diode characteristics

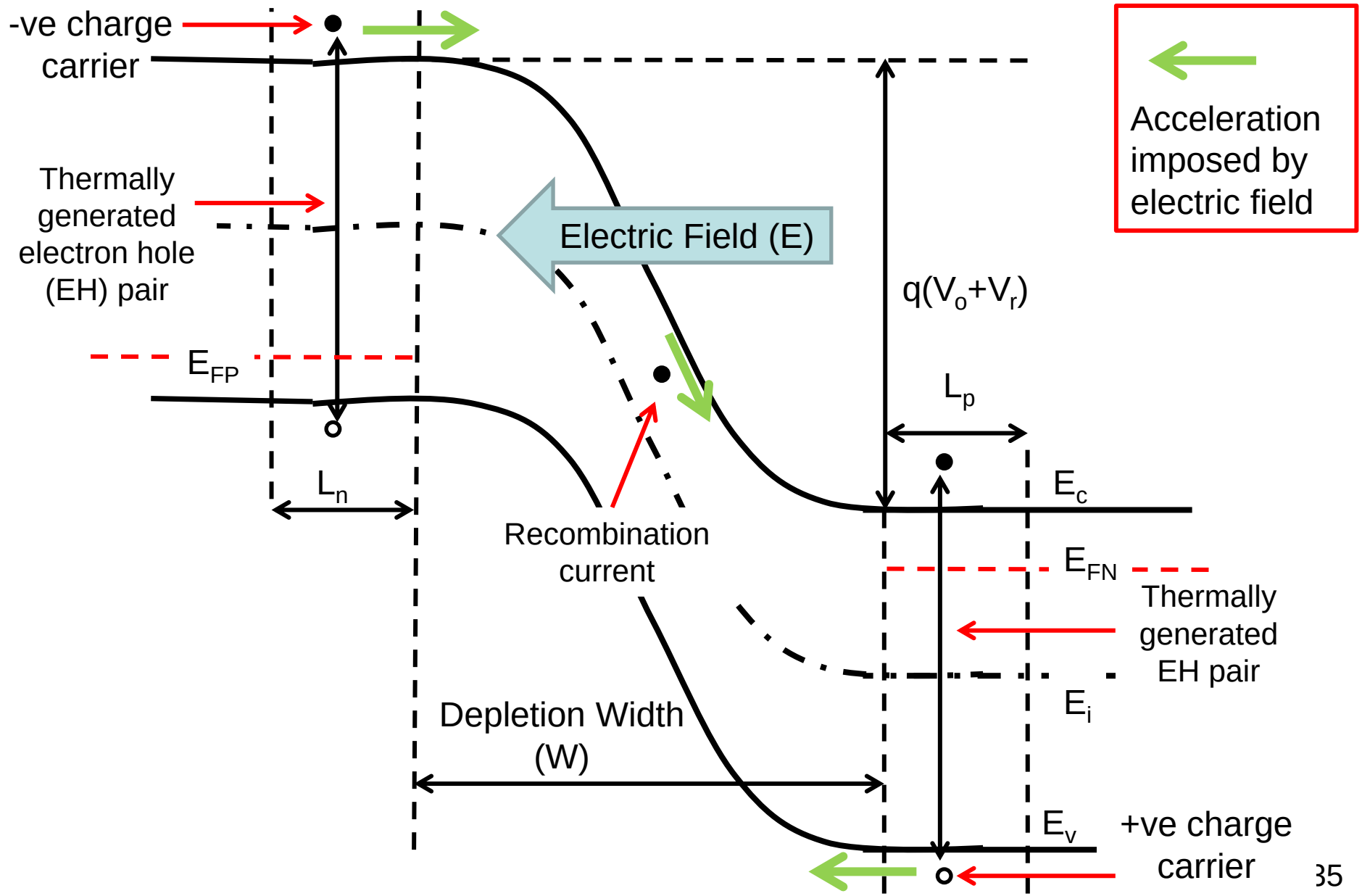


Pass Band: Difference between rated voltage and actual breakdown voltage of device. Used to ensure product rating due to variations in processing conditions such as changes in oxide charge, doping concentration and wafer specification. Can be set at 20% above rated voltage

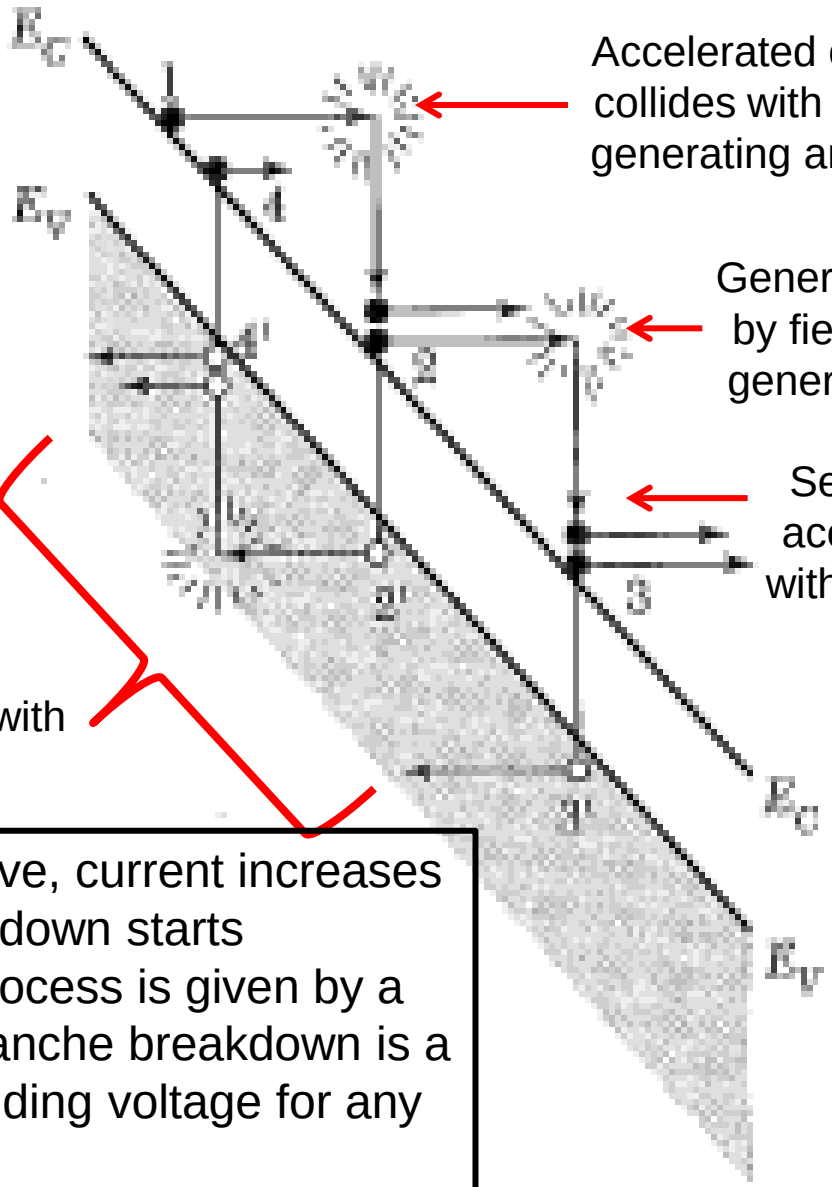
Impact ionisation

- Power device are designed to support high voltages within the depletion layer formed across either a p-n junction or a metal-semiconductor (Schottky) interface
- Any carrier that enters the depletion layer either due to space charge generation or by diffusion from adjacent neutral regions
  - Are swept out by the electric field produced in the region by the applied voltage
- Due to their relationship: electric field increase with applied voltage
  - This results in acceleration of the mobile carrier to higher velocities
- With further increase in the electric field the mobile carriers gain sufficient kinetic energy so that their interaction with lattice atoms produce the excitation of electron-hole pairs
  - This process is referred to as **impact ionisation**
- Since these generated electron hole pairs undergo acceleration by the electric field these can cause further generation of electron hole pairs
- Impact ionisation is a multiplicative phenomenon which produces a cascade of mobile carriers leading to significant current flow

Carrier flow across a reverse bias p-n junction



Avalanche process: Charge carriers moving within a depletion region



Accelerated carrier collides with lattice generating an EHP

Generated EHP accelerated by field collides with lattice generating secondary EHP

Secondary generated EHP accelerated by field collides with lattice generating tertiary EHP

Same process occurs with positive carriers

Avalanche is multiplicative, current increases significantly when breakdown starts
The impact ionisation process is given by a material constant. Avalanche breakdown is a physical limit to withstanding voltage for any material.

*** EHP: Electron Hole Pair

Critical electric field strength

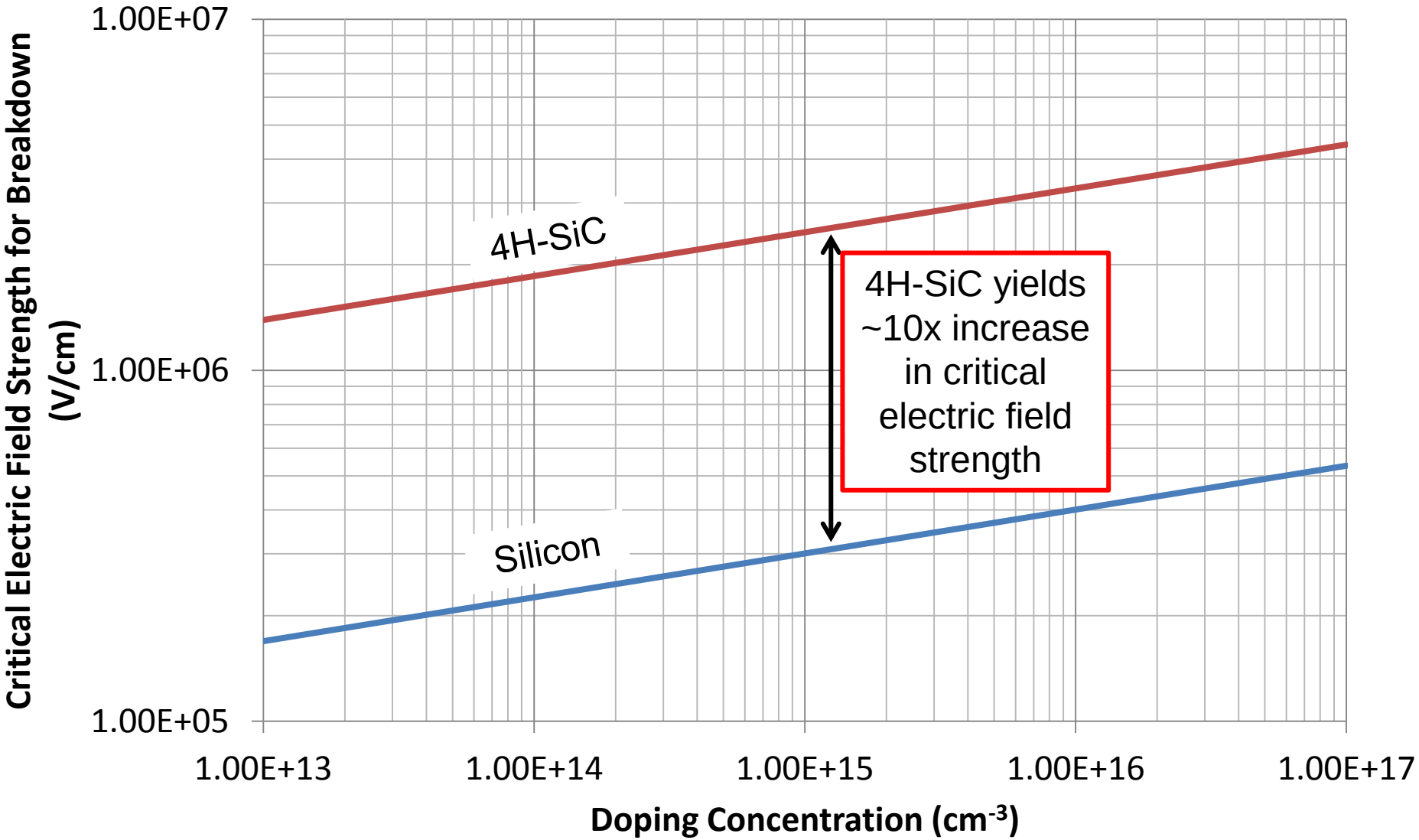
- The onset of avalanche breakdown for an abrupt plane-parallel junction is accompanied by a maximum electric field
  - This maximum electric field is referred to as the critical electric field for breakdown or the **critical electric field strength**
  - The critical electric field strength for silicon is given by:

$$E_c(Si) = 4010 N_D{}^{1/8}$$

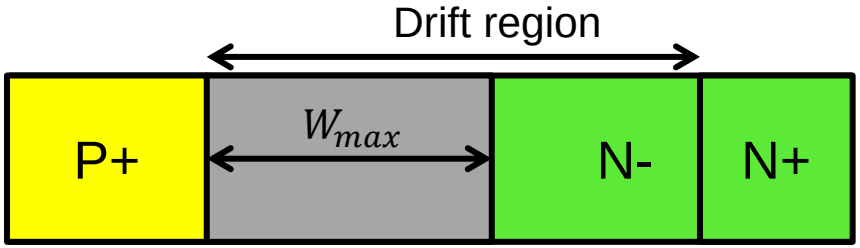
  - Whereas for 4H-Silicon Carbide:

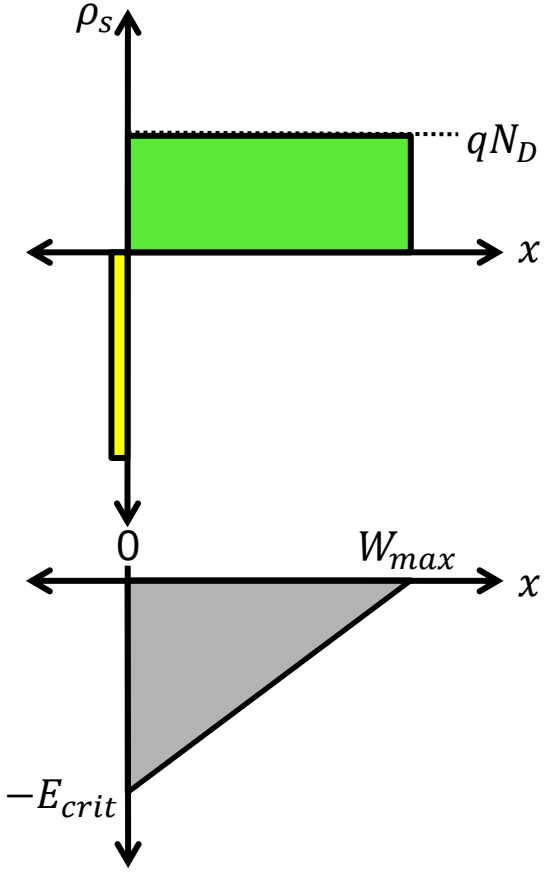
$$E_c(4H - SiC) = 3.3 \times 10^4 N_D{}^{1/8}$$

Comparison of electric field strength for Si and 4H SiC



Maximum plane parallel breakdown voltage





- From our previous analysis

$$E_{crit} = \frac{qN_D W_{max}}{\varepsilon_s}$$

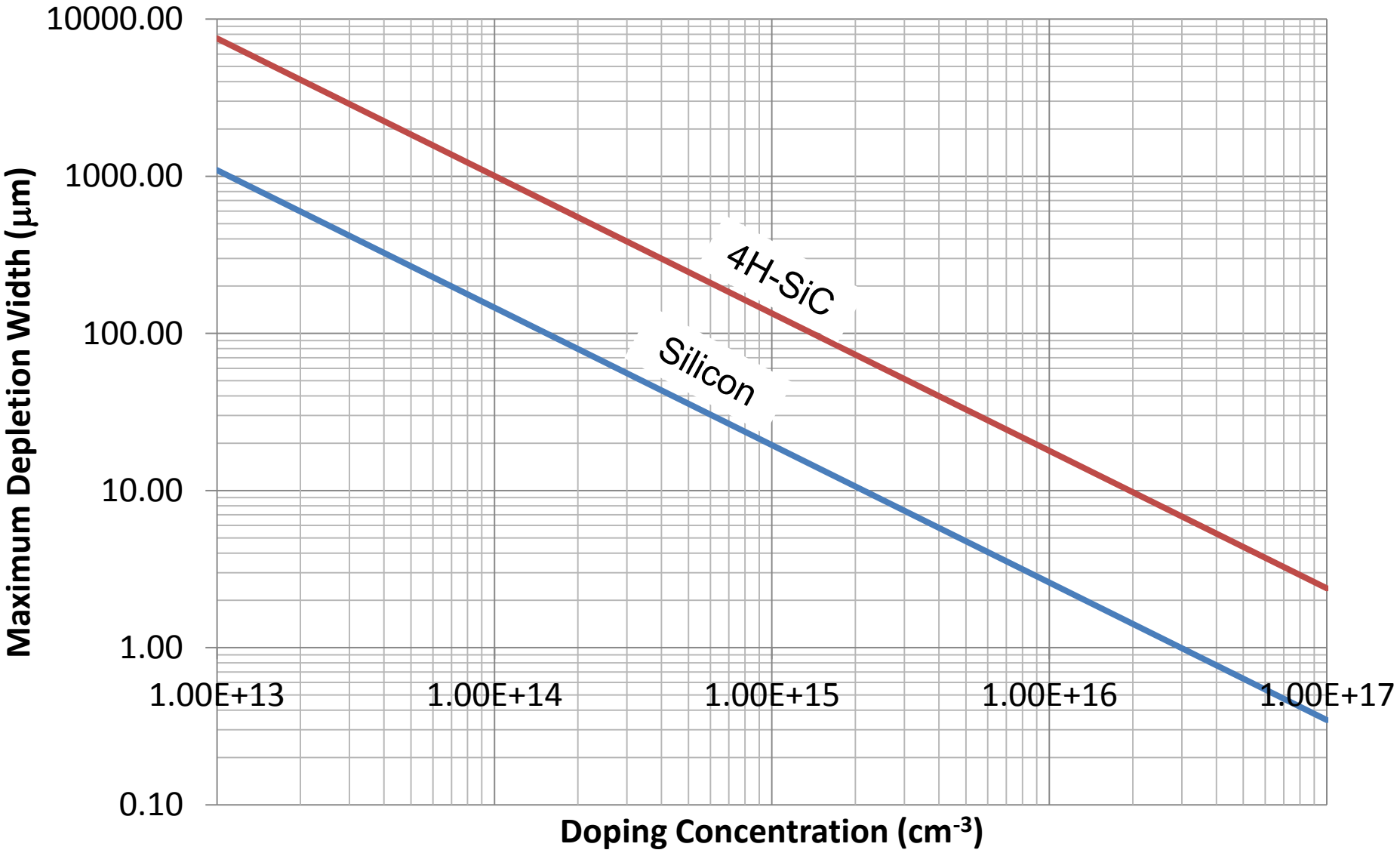
- Maximum depletion width

$$W_{max} = \sqrt{\frac{2\varepsilon_s V_{max}}{qN_D}}$$

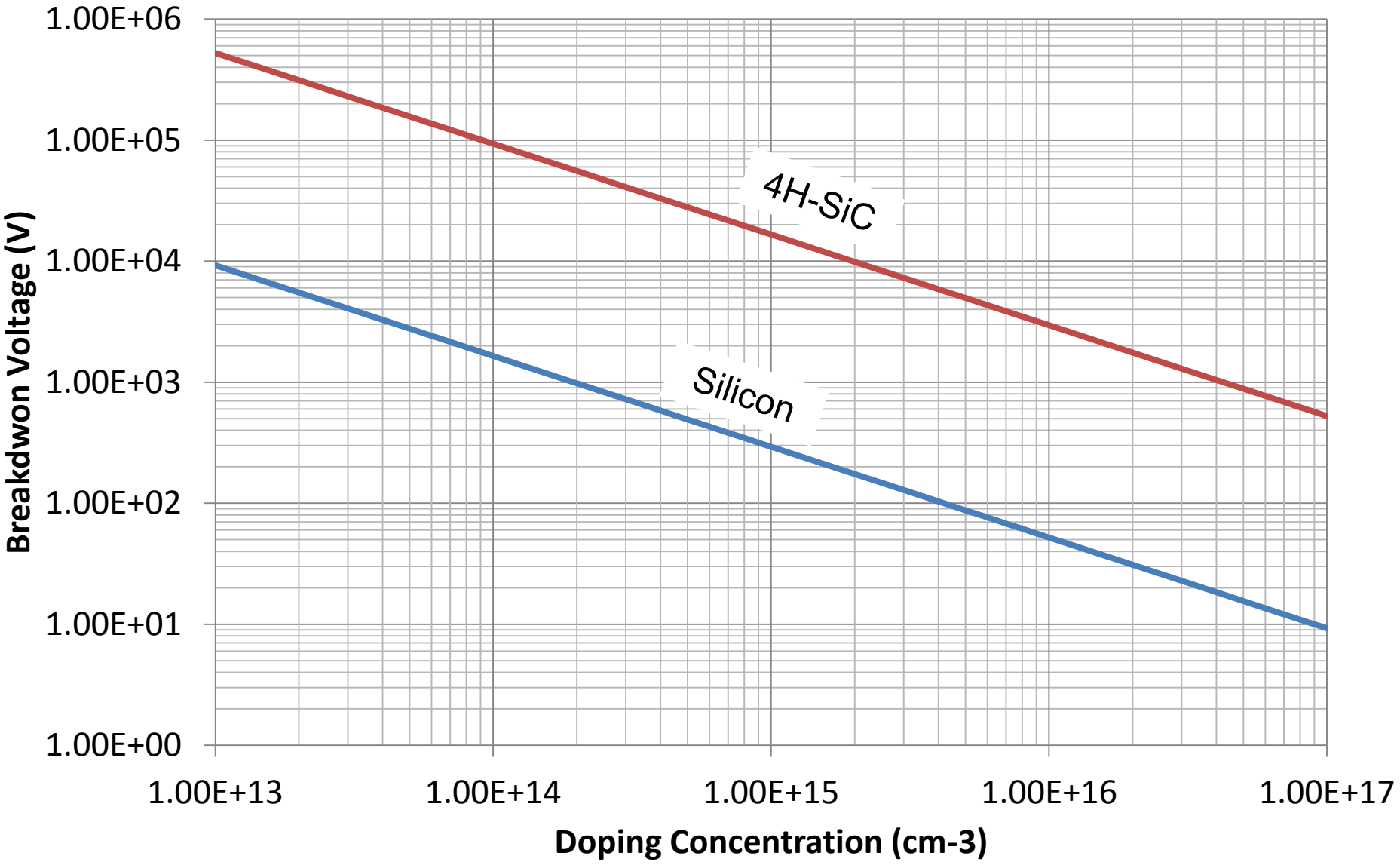
- Combining these obtains the maximum breakdown voltage for any drift region concentration

$$V_{max} = \frac{{E_{crit}}^2 \varepsilon_s}{2qN_D}$$

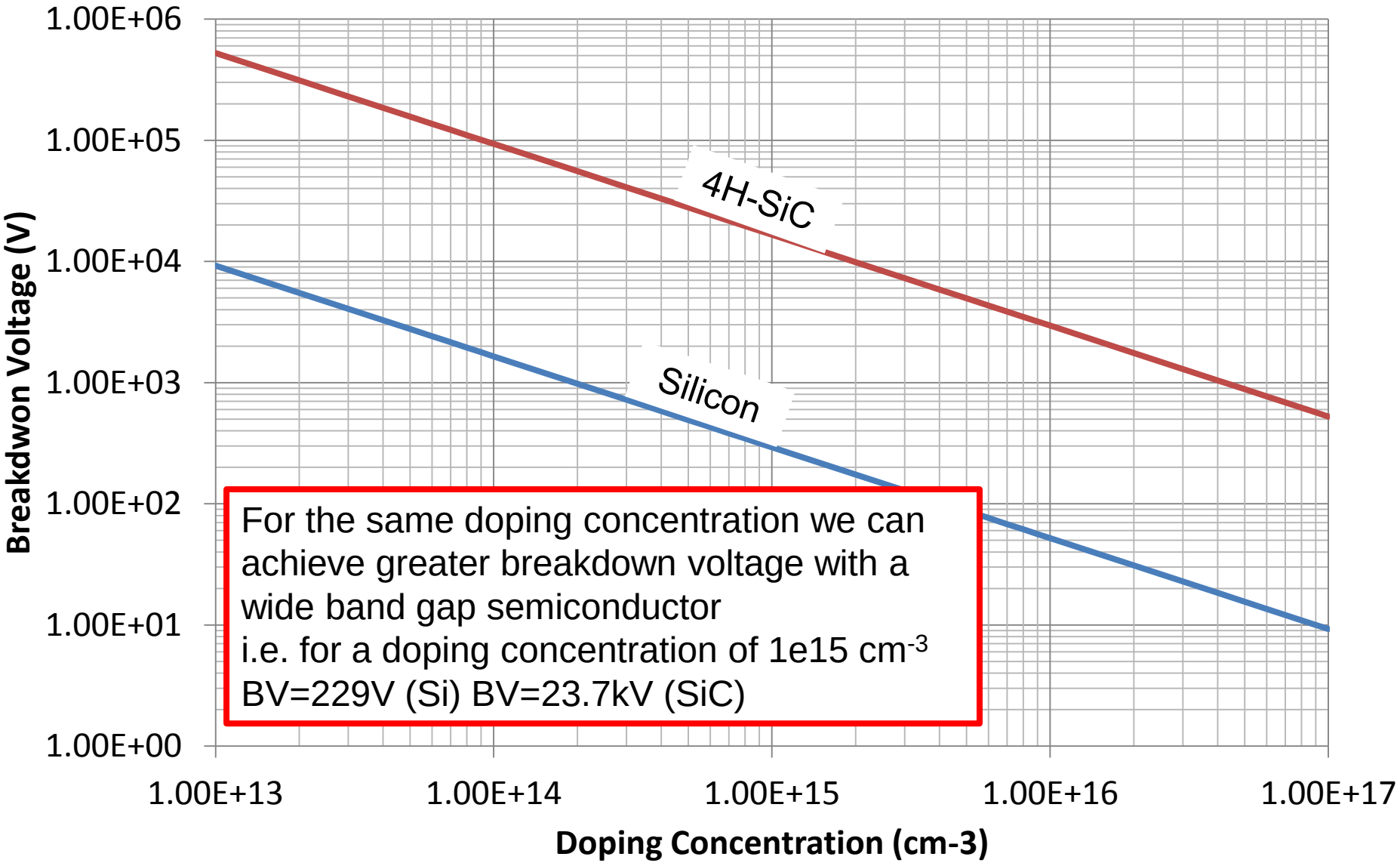
Maximum depletion region obtained for Si and SiC with respect to drift region doping



Maximum Breakdown Voltage with respect to drift region doping concentration

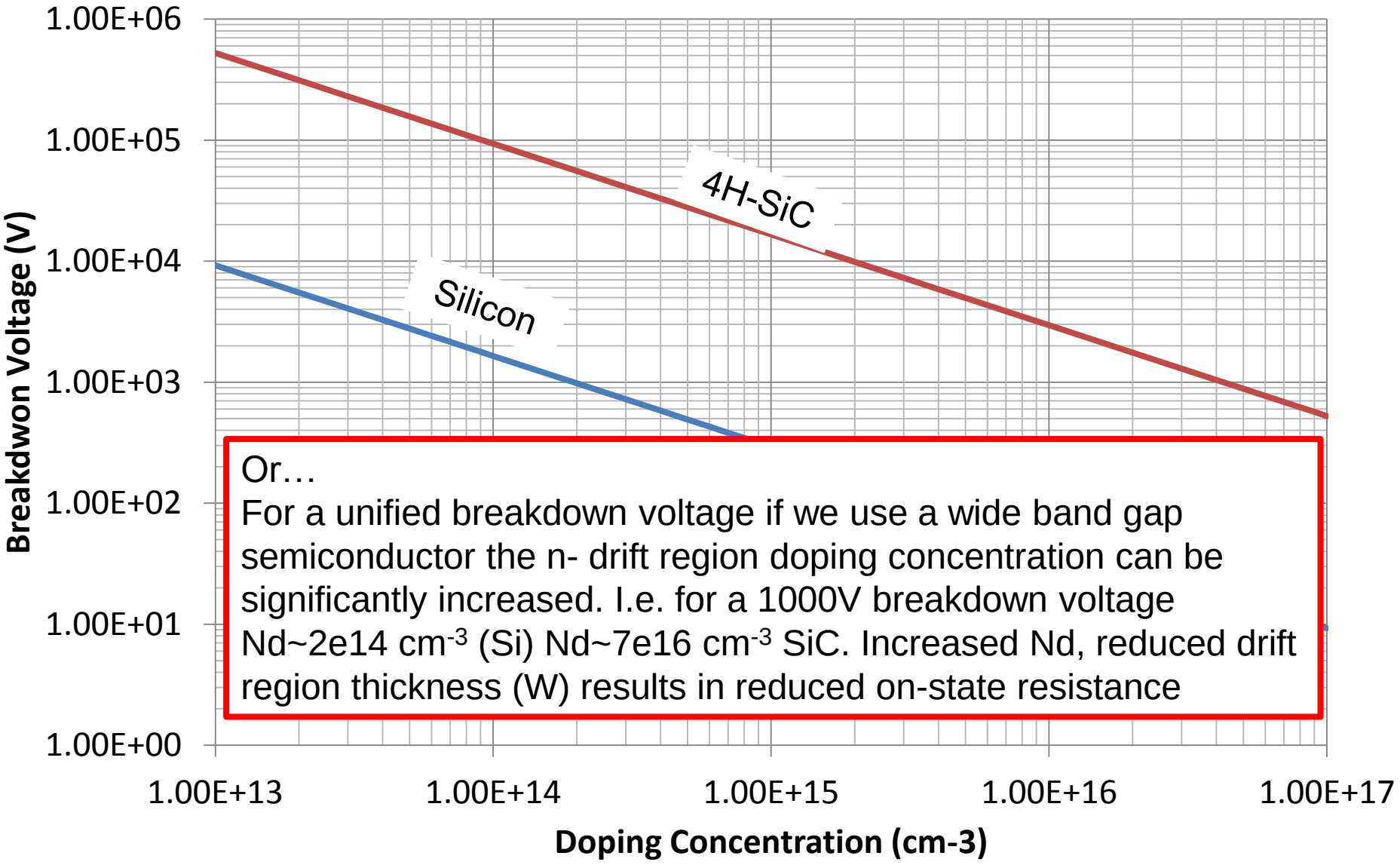


Maximum Breakdown Voltage



BV=Breakdown Voltage

Maximum Breakdown Voltage



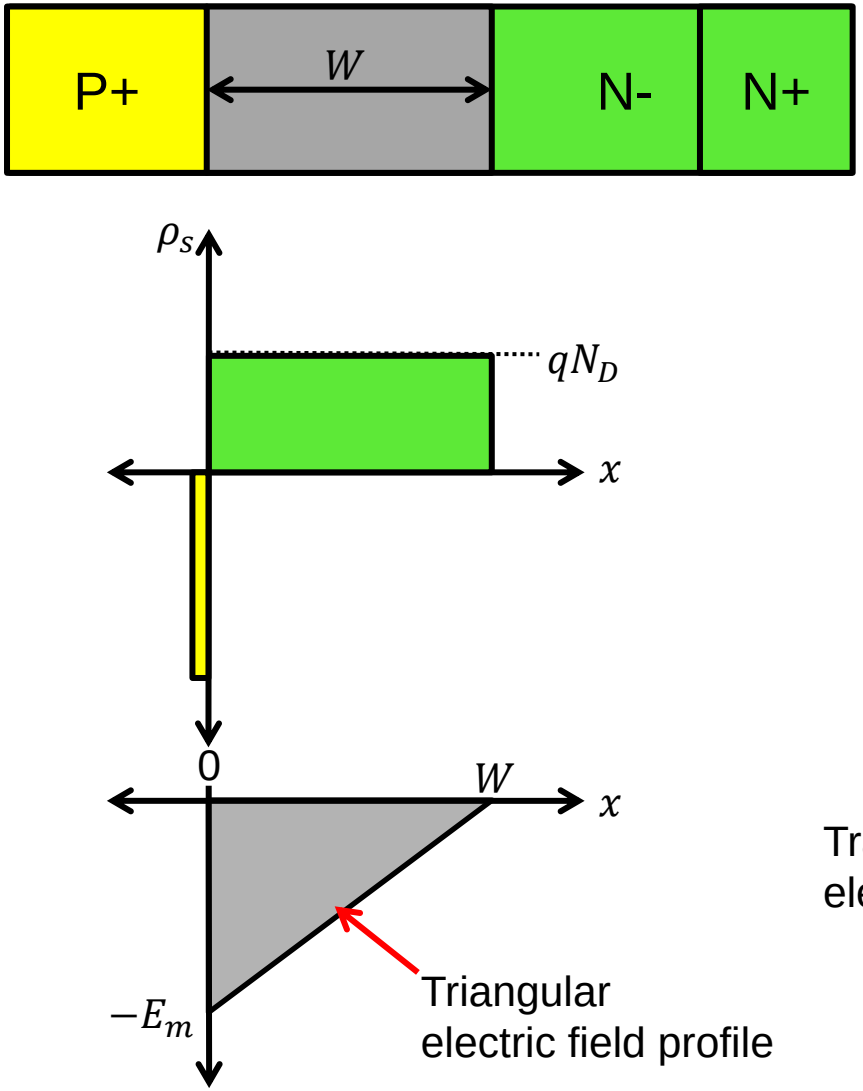
Or…
For a unified breakdown voltage if we use a wide band gap semiconductor the n- drift region doping concentration can be significantly increased. I.e. for a 1000V breakdown voltage Nd~2e14 cm^{-3} (Si) Nd~7e16 cm^{-3} SiC. Increased Nd, reduced drift region thickness (W) results in reduced on-state resistance

Abrupt punch through diode

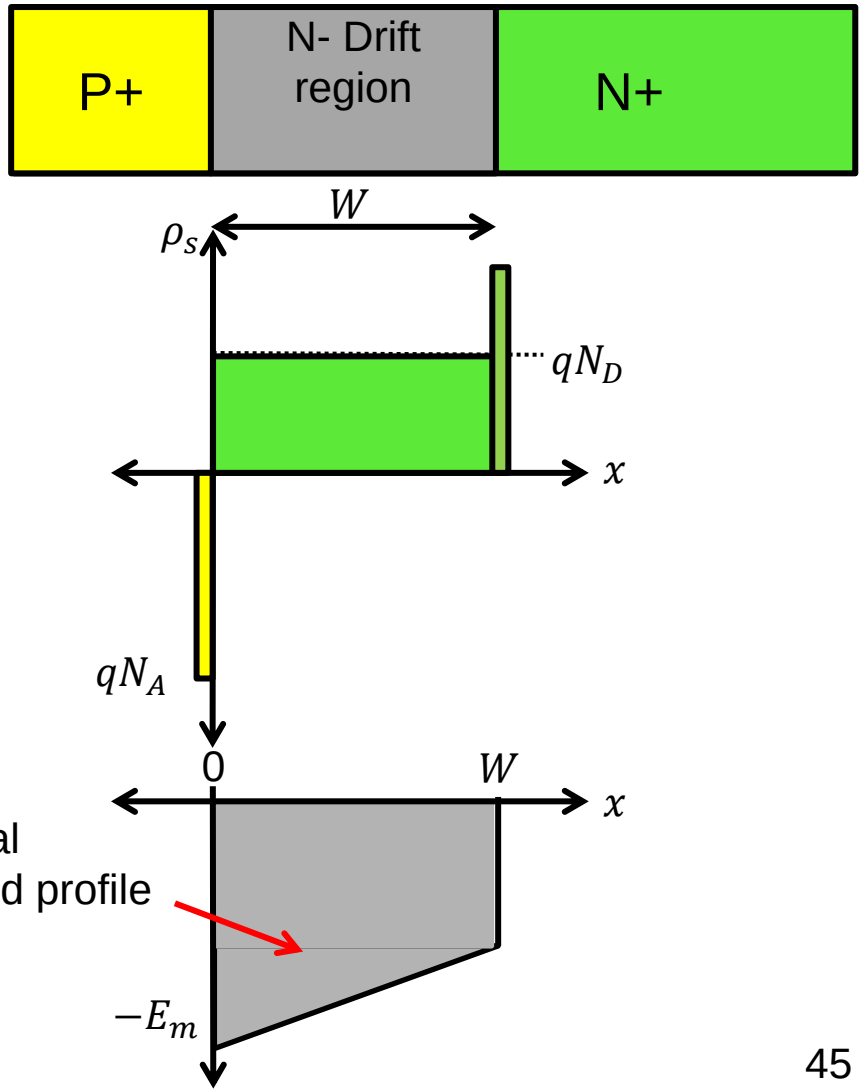
- In the case of PiN rectifiers the resistance of the drift region is greatly reduced in the on-state by the injection of a large concentration of minority carriers
  - In these cases the doping concentration of the drift region does not determine the resistance to the on-state current flow
    - Bipolar conduction (both electrons and holes) in contrast to metal-semiconductor Schottky diodes which are majority carrier devices i.e. n type Schottky diode conducts via electrons
  - It is desirable to use a thinner drift region with a reduced doping concentration to support the voltage
    - Called a **punch through** design

Punch through vs. non-punch through: Depletion widths and breakdown

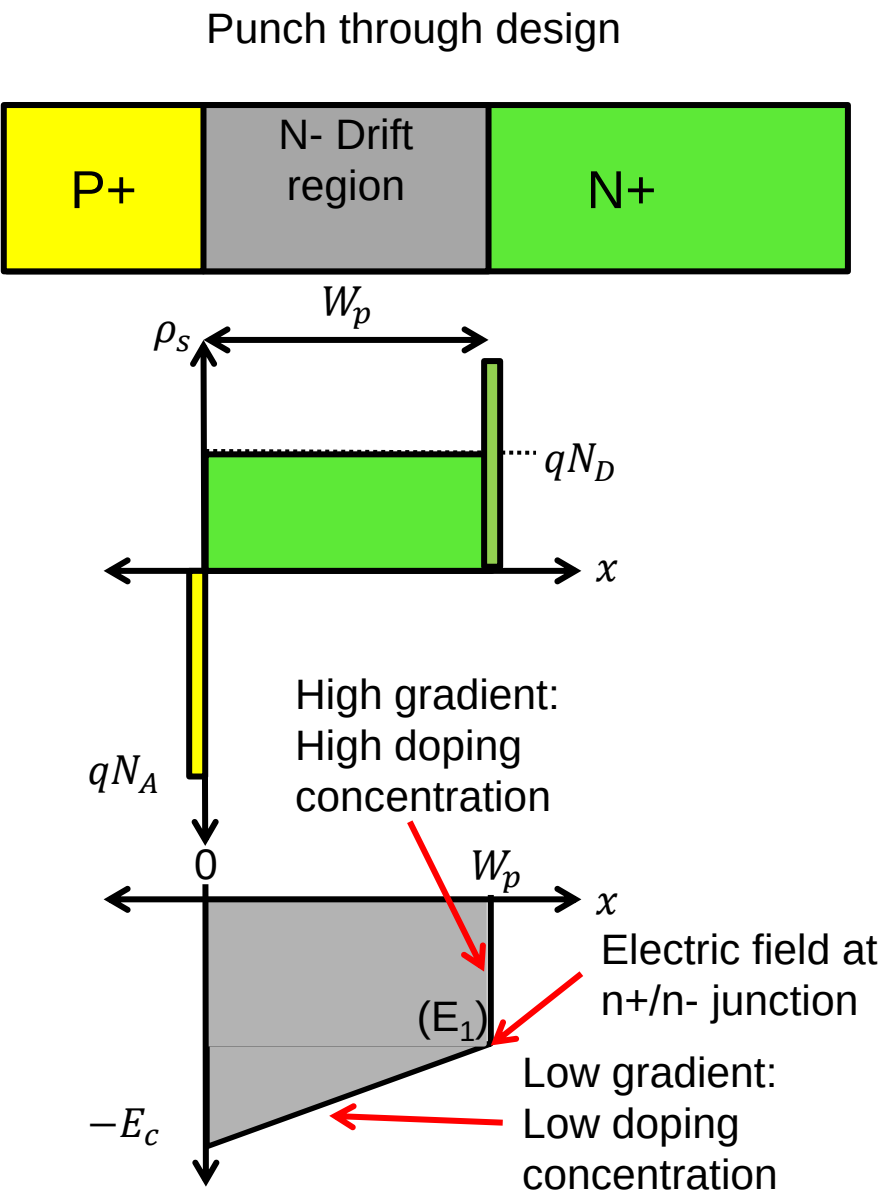
Non-punch through design



Punch through design



Punch through diode at breakdown



- The electric field at the n+/n- interface is given by:

$$E_1 = E_m - \frac{qN_D}{\varepsilon_s} W_P$$

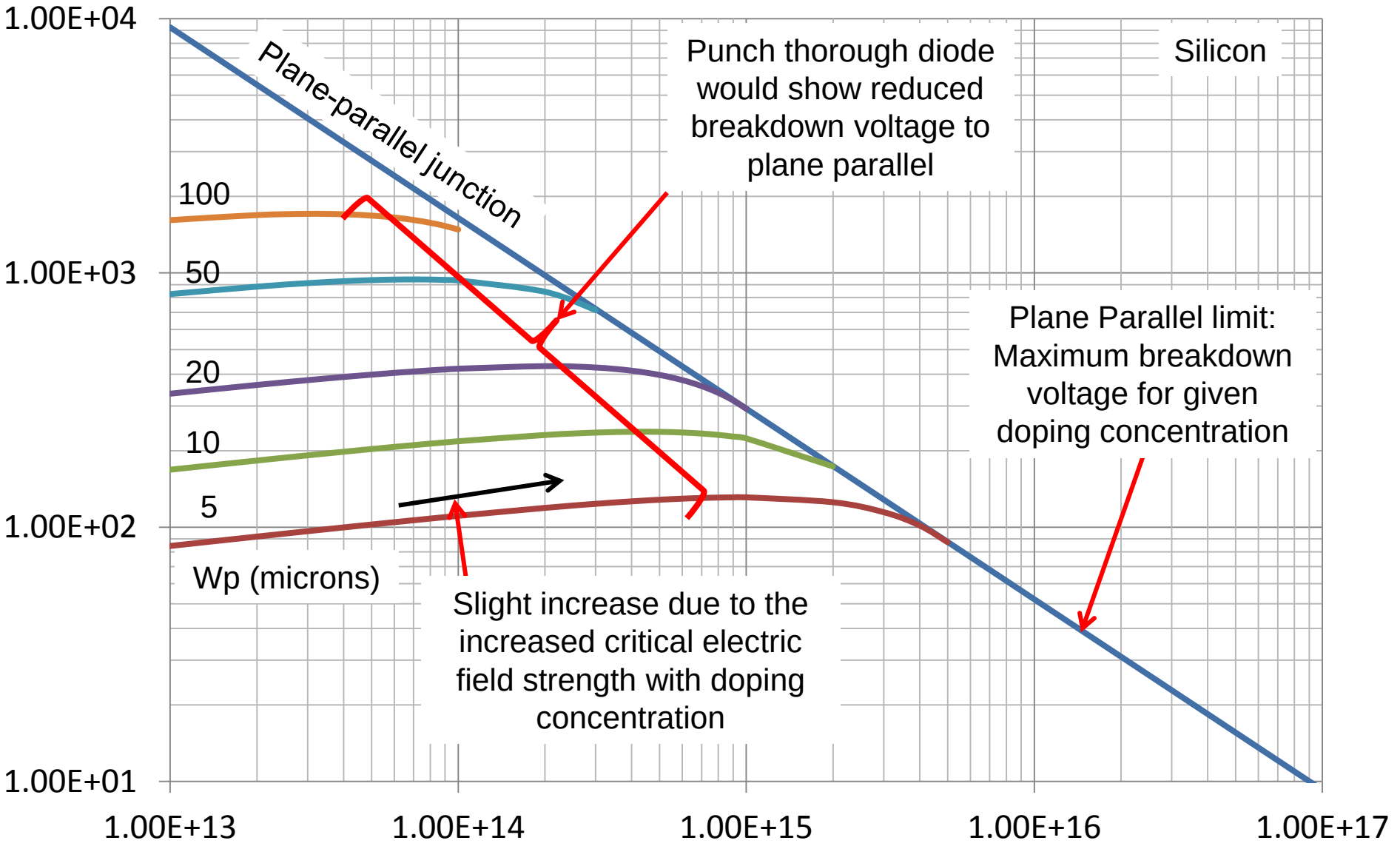
- Voltage supported by the punch through diode:

$$V_{PT} = \left(\frac{E_m + E_1}{2}\right) W_p$$

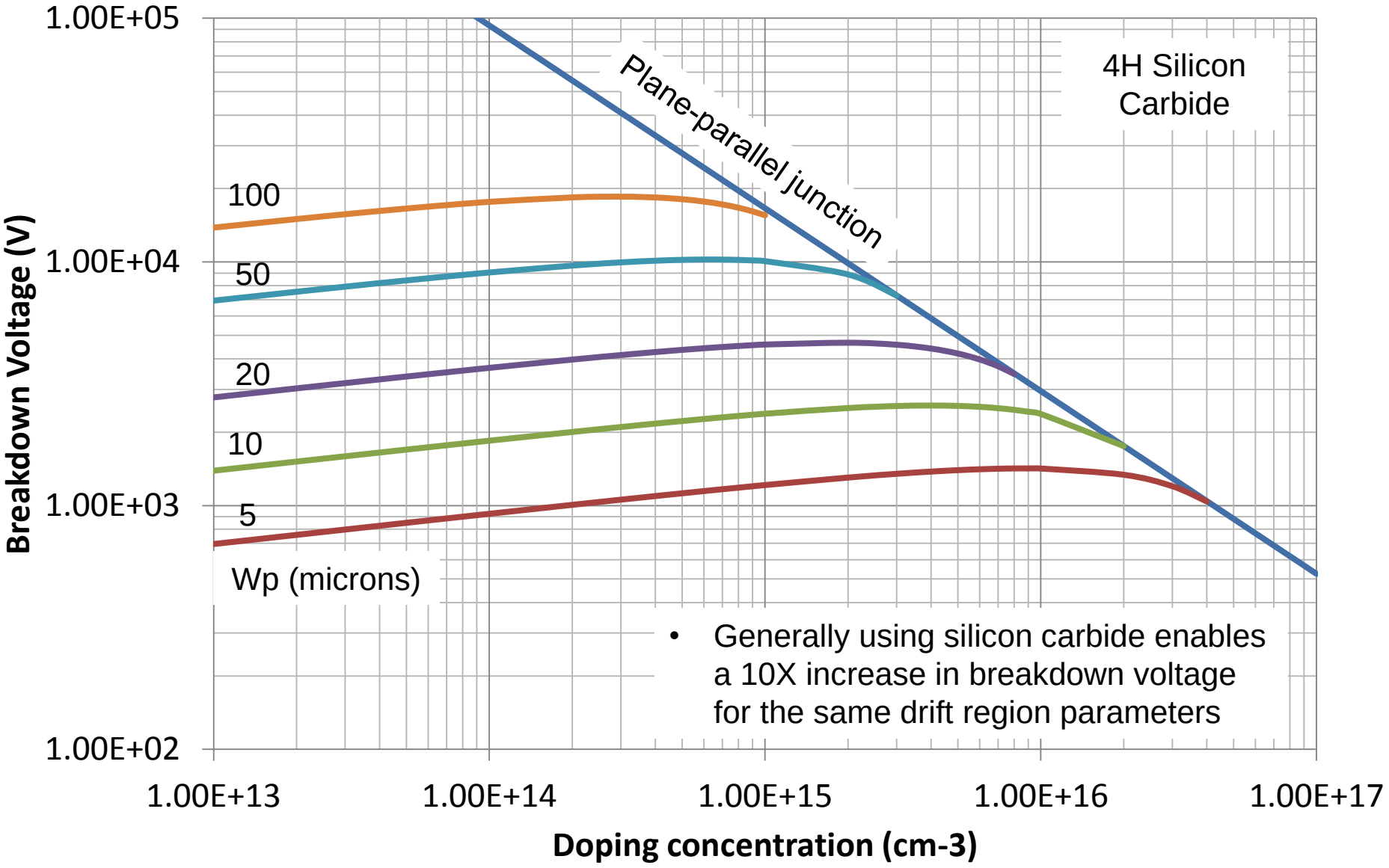
- If the voltage supported within the n+ region is neglected, breakdown occurs when E_m becomes equal to the critical electric field strength E_c. Combining these two equations:

$$BV_{PT} = E_c W_p - \frac{qN_D {W_p}^2}{2\varepsilon_s}$$

Punch through breakdown voltage for Silicon p-i-n diodes



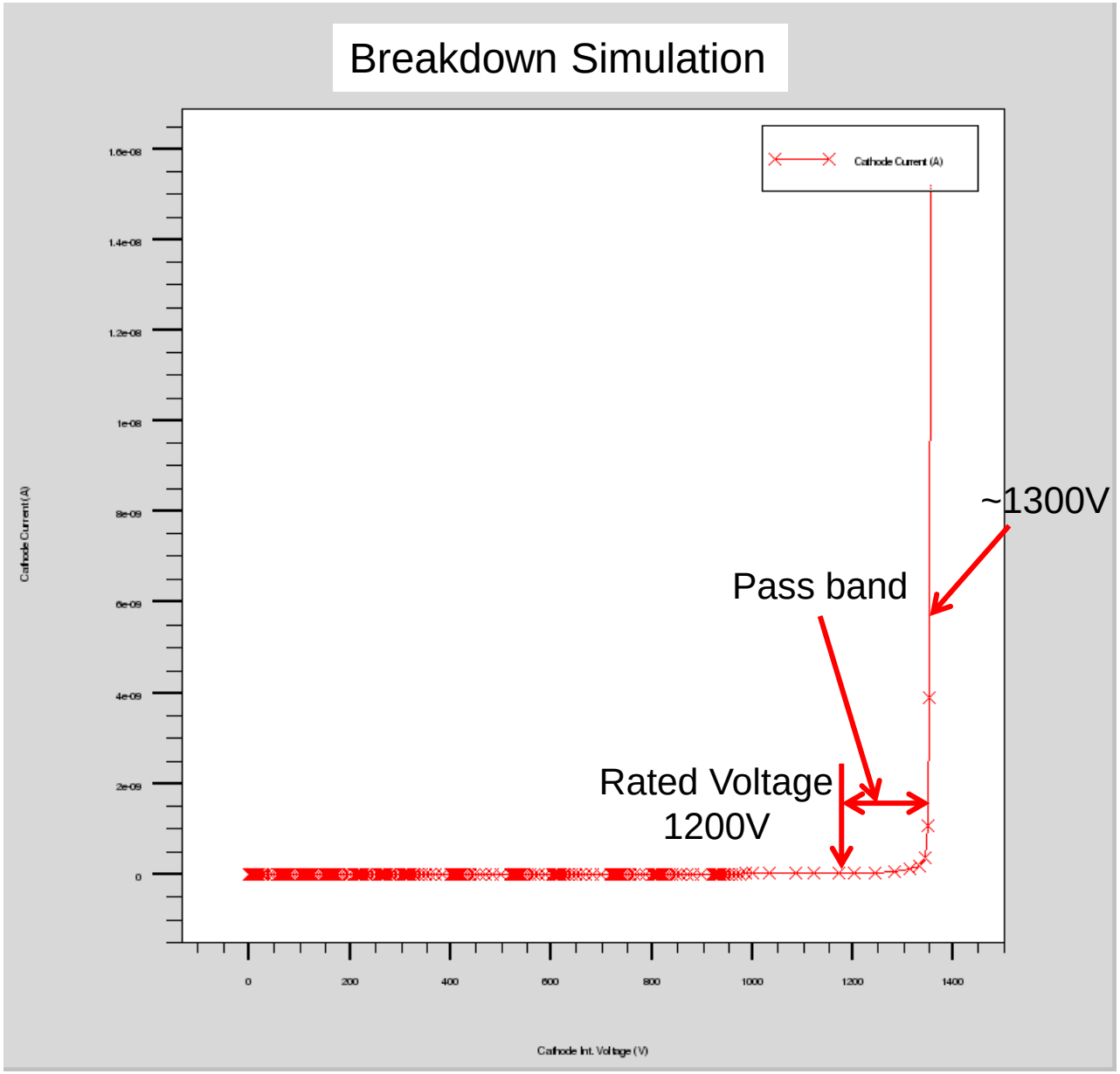
Punch through breakdown voltage for Silicon Carbide p-i-n diodes



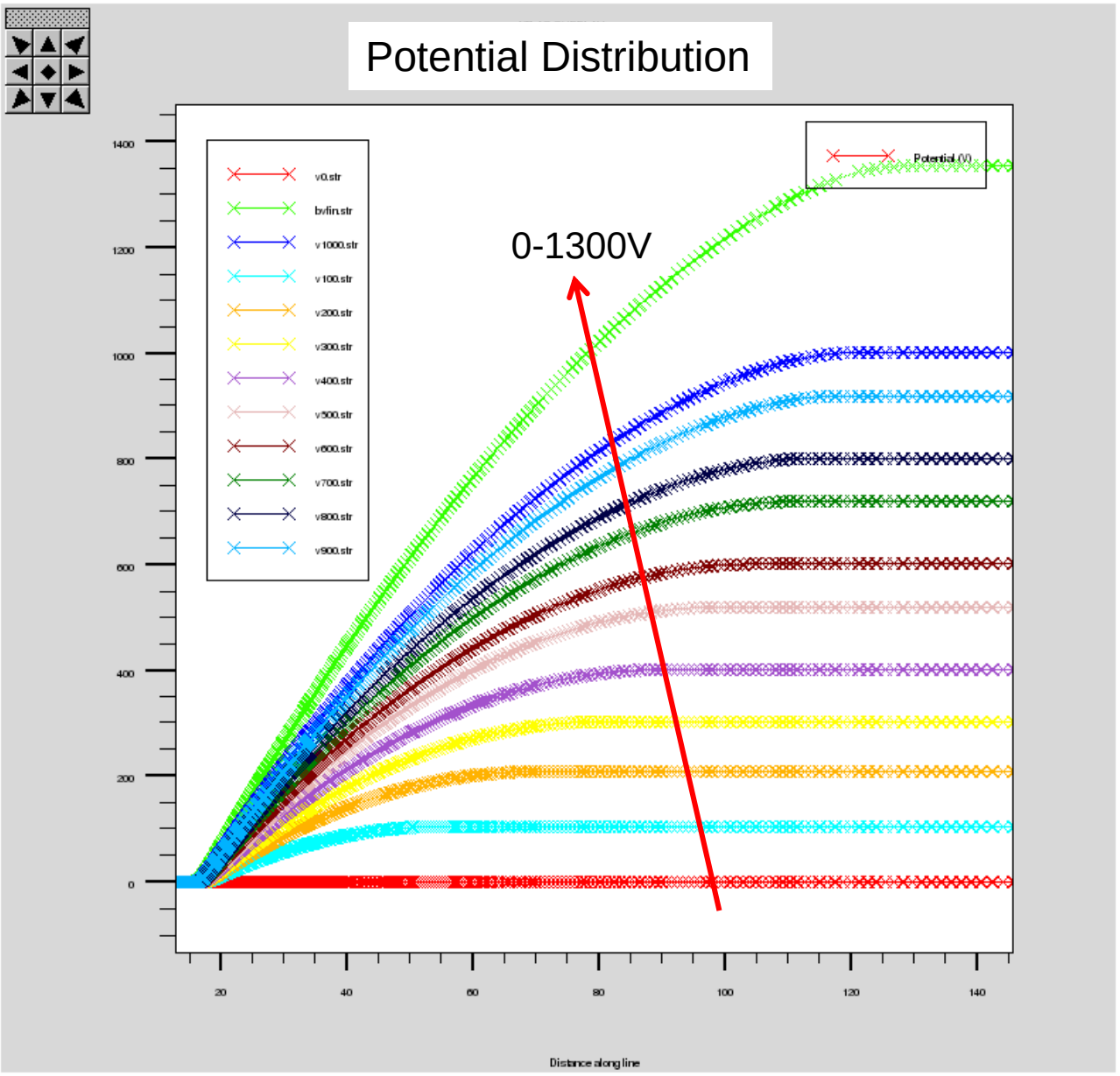
Non punch through vs. punch through designs

- For a punch through diode for a given doping concentration breakdown voltage would be lower than that of the plane parallel case
  - This is due to the truncation of the electric field at the n+ region
    - Electric field distribution changing from triangular to trapezoidal
- For the point of view of designing a drift region for a silicon p-i-n rectifier we can obtain a breakdown voltage of 1000V with a ~50μm drift region
  - In contrast to a drift region thickness of 80μm required using a non punch through design
- This reduction in drift region is beneficial for reducing on-state forward drop but also for reducing stored charge and consequently the reverse recovery power loss

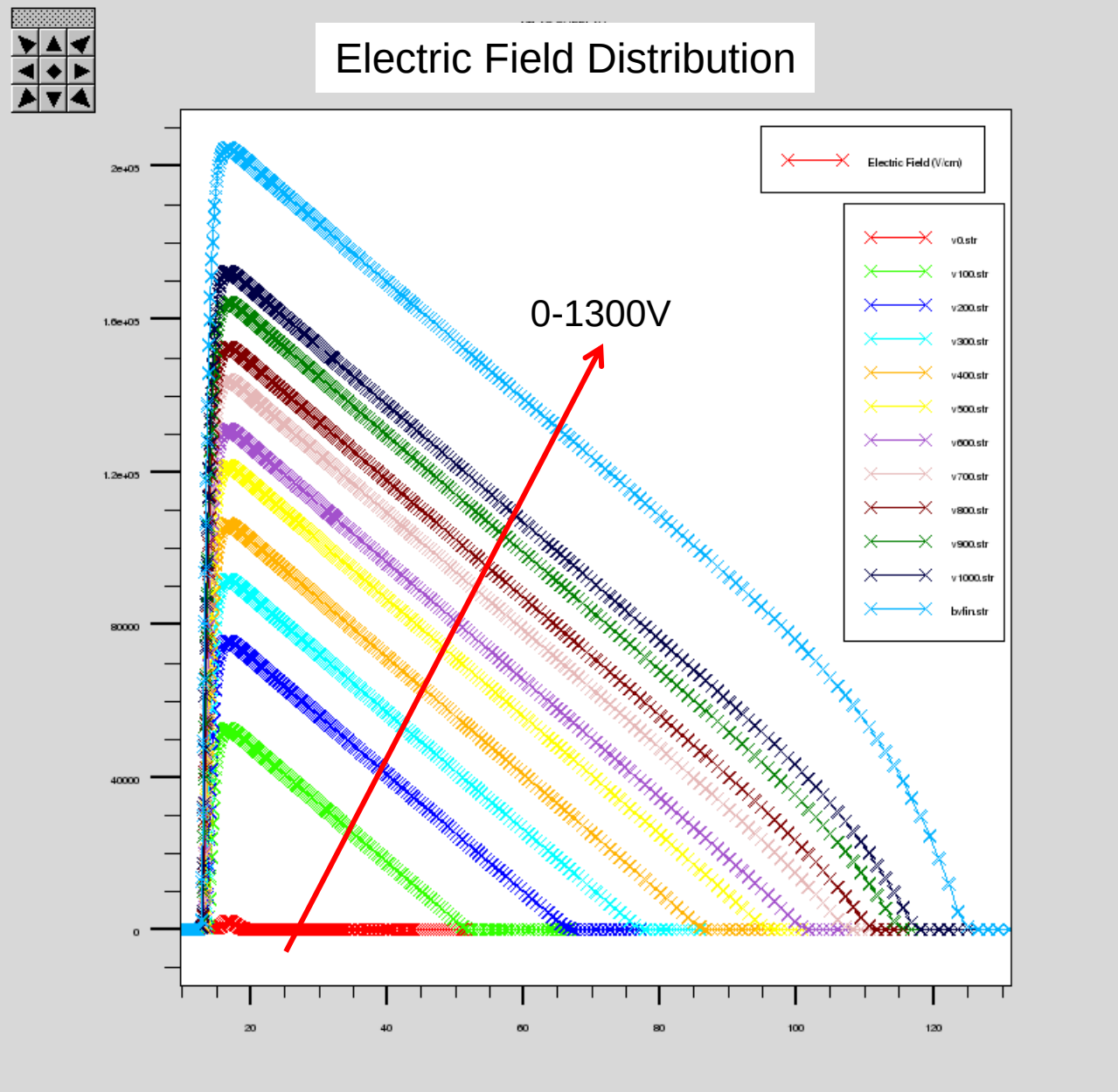
1200V Diode simulation example: Breakdown characteristics



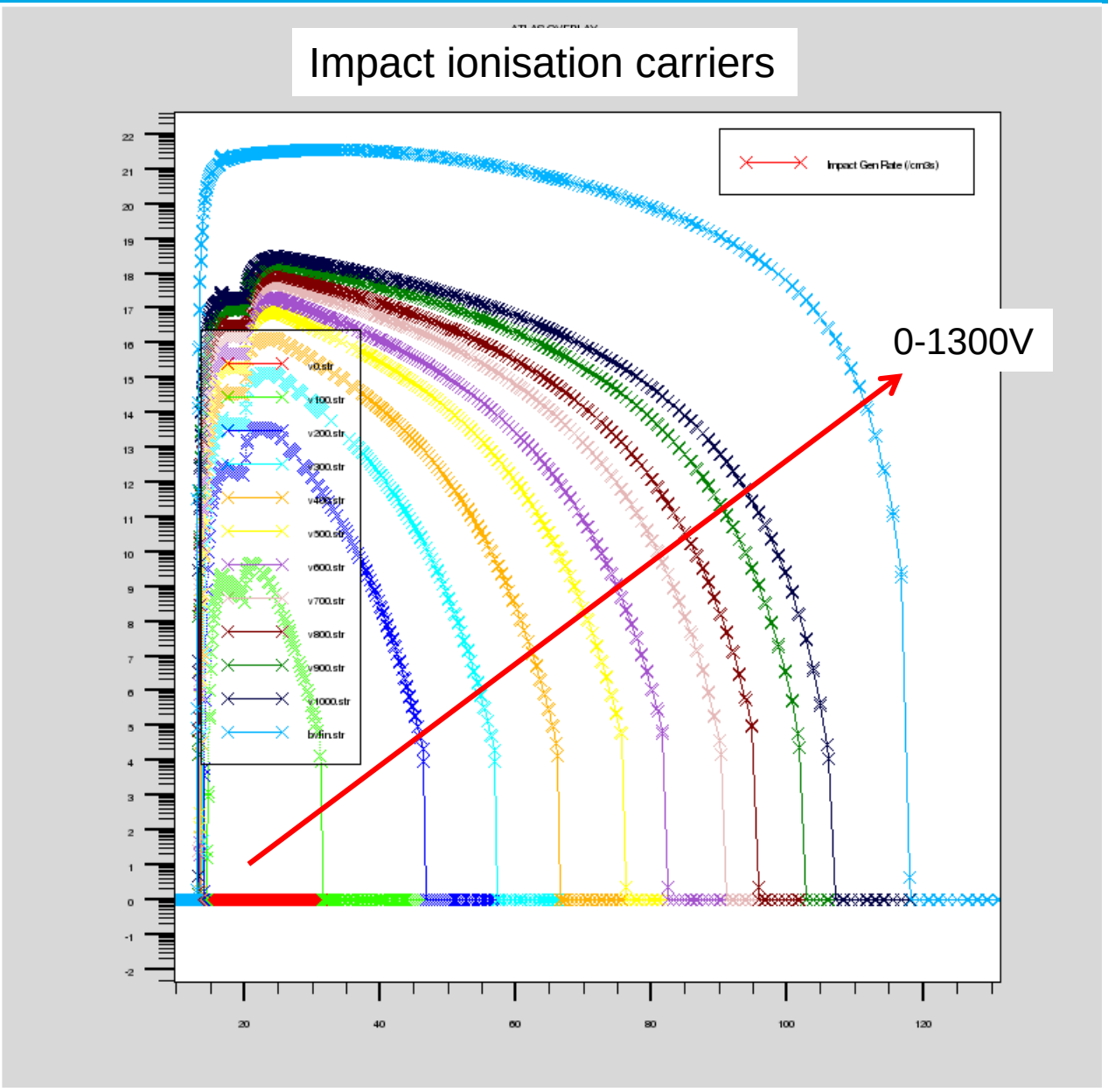
1200V Diode simulation example: Potential distribution



1200V Diode simulation example: Electric field distribution



1200V Diode simulation example: Electric field distribution



Transient Processes in Power Diodes

Transient processes in power diodes

- When the rate of change of current and voltage in a power diode is relatively slow
  - Their instantaneous values are well described by the steady state current voltage characteristics
- However when either the voltage or current changes abruptly
  - The carrier distribution in the device may be very different from the steady state conditions
  - Important dynamic processes during the transient leads to appreciable differences between the steady state and dynamic characteristics
- A theoretical solution of the equations describing the transient process requires the distribution of excess carriers within the semiconductor to be determined at any given point in time
  - The continuity equitation must be solved with the correct initial and boundary conditions
  - Generally these equation are too complex
    - Therefore device level simulators are used to fully optimise devices

Transition from the reverse bias to forward

- The most basic method of analysing transient phenomena in diodes is to assume the diode is subject to an abrupt change of current or voltage
  - In power semiconductor device applications changes in current are generally more important
  - The forward voltage drop of a diode under time varying conditions may be expressed as:

$$v_F(t) = v_p(t) + v_n(t) + v_i(t)$$

  - Using our previous analysis, this can be re-written to:

$$v_F(t) = v_p(t) + v_n(t) + v_{ohm}(t) + v_{mob}(t)$$

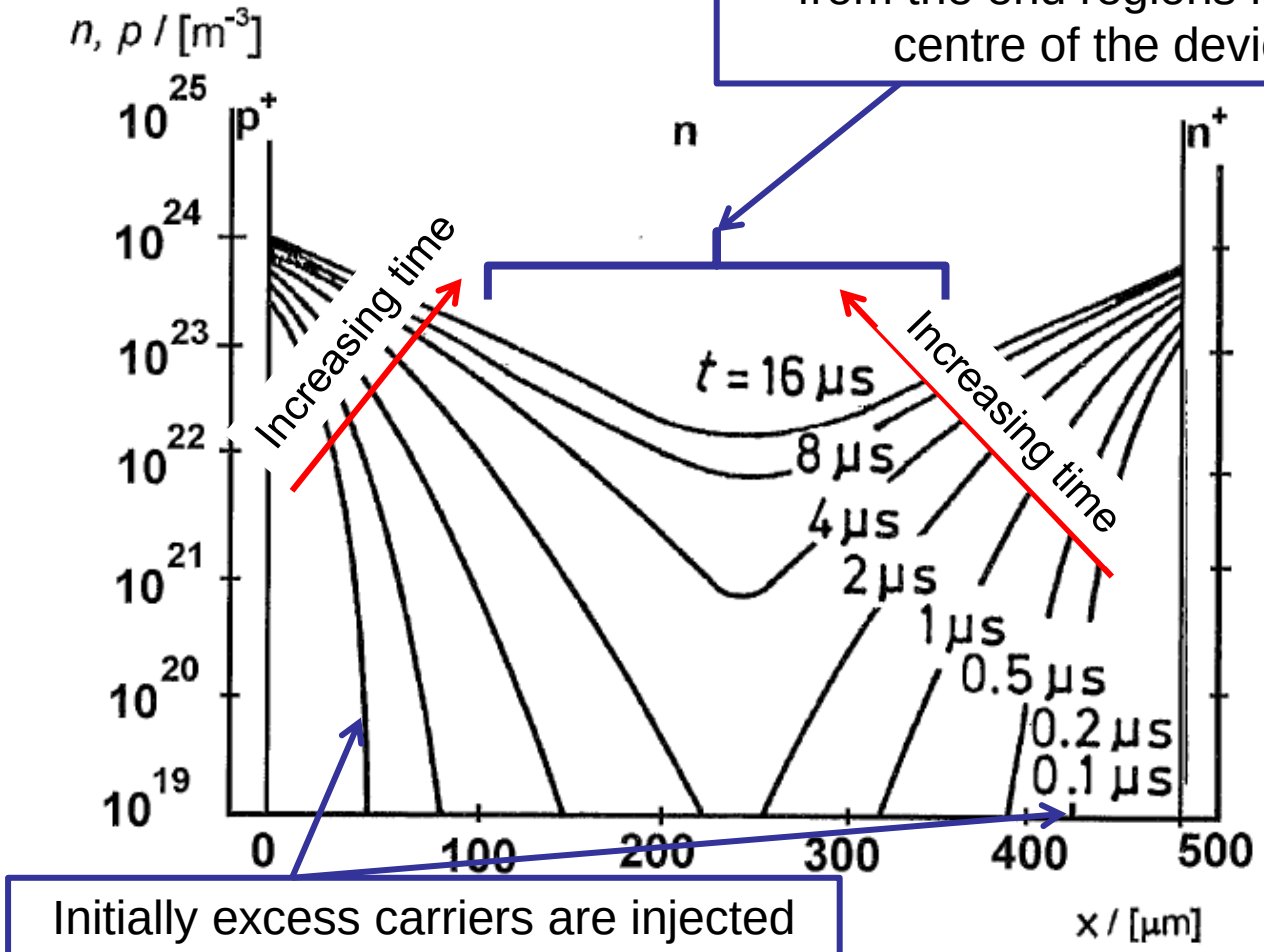
Voltage dropped across the p+-i and n+-i junctions

Representative of the instantaneous carrier distribution

Difference in the electron and hole concentrations where there is a carrier concentration gradient

Carrier distribution during turn on

- If a forward current increases from zero, with a rate of change $\frac{di_F}{dt}$

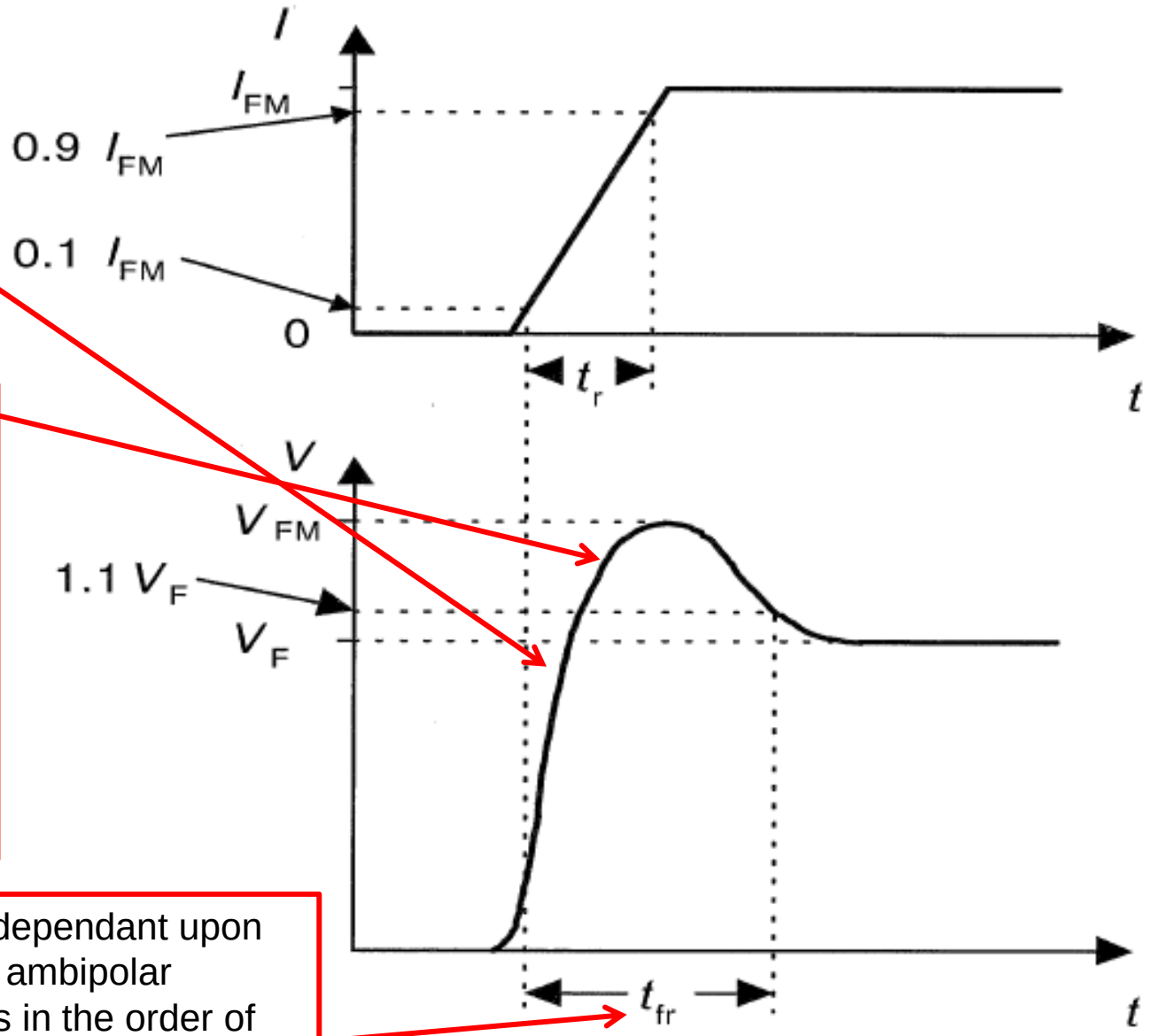


Variation of the forward current and forward voltage drop during the turn on process

Initially the increasing current causes an increasing forward voltage to be dropped across the across the resistance of the lightly doped region

As the number of excess carriers in the middle region increase it resistance decreases.
Therefore the forward voltage drop normally rises to a maximum after which it diminishes to a value corresponding to the steady state value

Forward recovery time (t_{fr}) is dependant upon drift region thickness (W) and ambipolar diffusion coefficient (D_a) and is in the order of 0.1-10μs for W values between 50 and 500μm



Forward recovery

- This transient phenomena may result in significant power dissipation
  - Especially in high voltage diodes are operating at high frequencies
  - The overshoot of forward voltage that occurs at turn-on when the current is high is practically undesirable in a freewheeling diode or one used in a snubber circuit
  - Furthermore: Device measurements are performed under transient conditions to minimise self heating
    - Forward recovery time could give incorrect results if pulses are too small

Transition from forward bias to reverse bias

- In many power electronic circuit a diode is called upon to switch quickly from the forward conducting to the blocking state
  - Usually a three terminal semiconductor switch is turned on (IGBT etc.)
    - This effectively reconfigures the power circuit and causing the diode to change from the on state to blocking
- At the beginning of the turn-off process the middle region of the diode between the p+ and n+ emitters are flooded with carriers
  - The distribution of this is a function of forward current density
- Initially the high excess carrier concentration in the vicinity of the n-p junction prevents the establishment of a space charge region
  - Voltage across the diode remains small and in the first part of the transition period current falls to zero and reverses at a rate determined by the external circuit

Junction recovery process

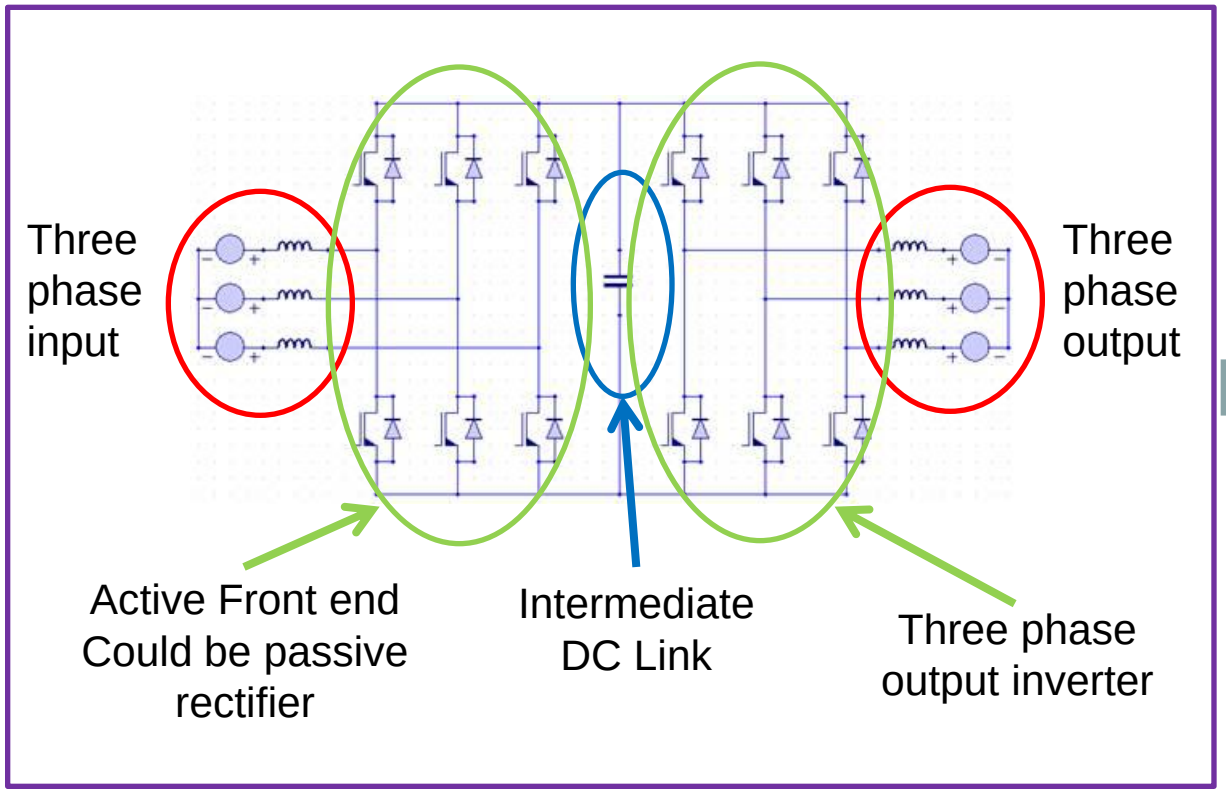
- Only when sufficient charge is removed by recombination or has diffused out as reverse current do the carrier concentrations at the p-n junction reach the levels of thermodynamic equilibrium
  - At this point the junction is said to be recovered and a space charge region starts to form
    - At this point the reverse current starts to fall away that is controlled by the diffusion and recombination processes in the base region of the diode
  - At this point the voltage across the diode is determined by the external circuit
    - In a circuit in which there is significant inductance in the diode electrical connections the change in di/dt at the peak of the reverse current can give rise to a large spike of reverse voltage

Reverse recovery characterisation

- Hard switching converters are examples of power electronic circuits that cause such a state change in a power diode
- The accompanying transient produces losses that have a significant effect on the maximum operating frequency
- Hard switching circuits can be emulated by considering a chopper circuit
  - Typical test circuit for power semiconductor device technologies

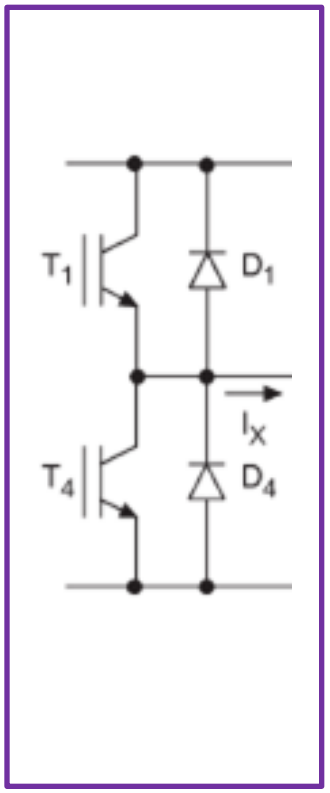
Typical converter layout

Typical Motor/Generator Configuration



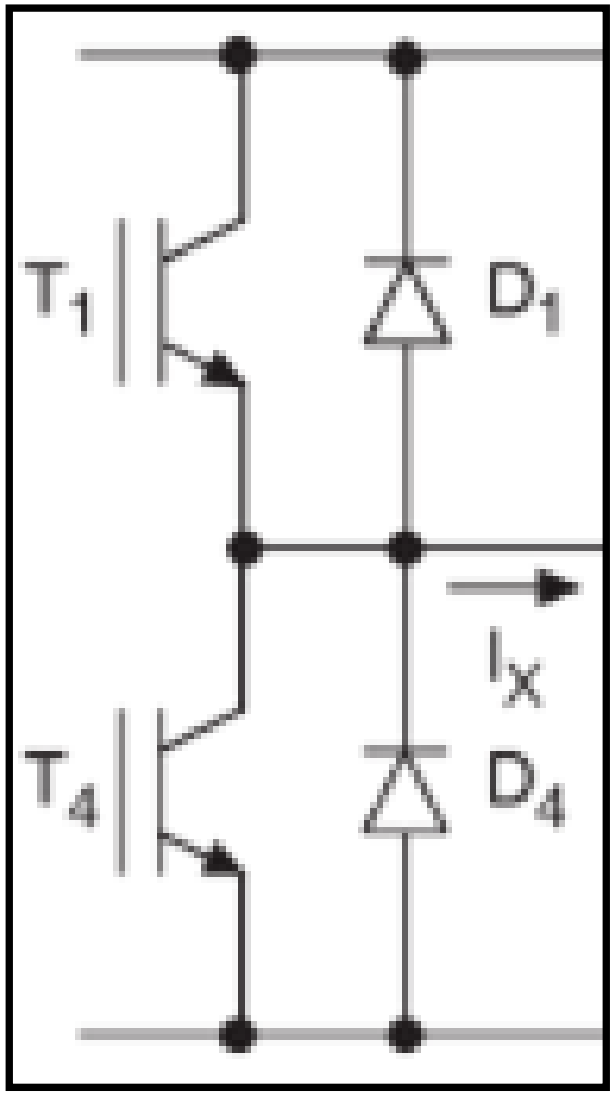
Could be simplified to

Single Phase

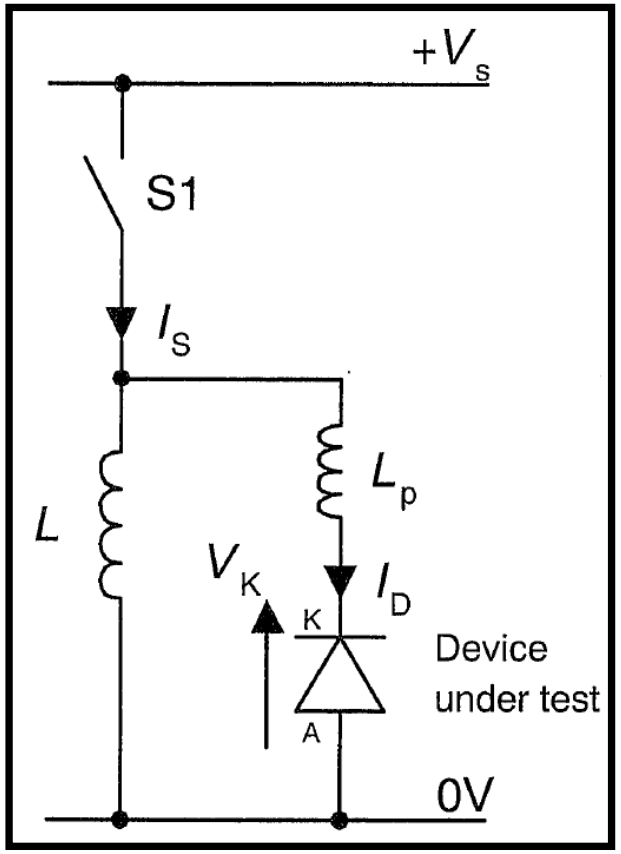


Typical power converter simplification

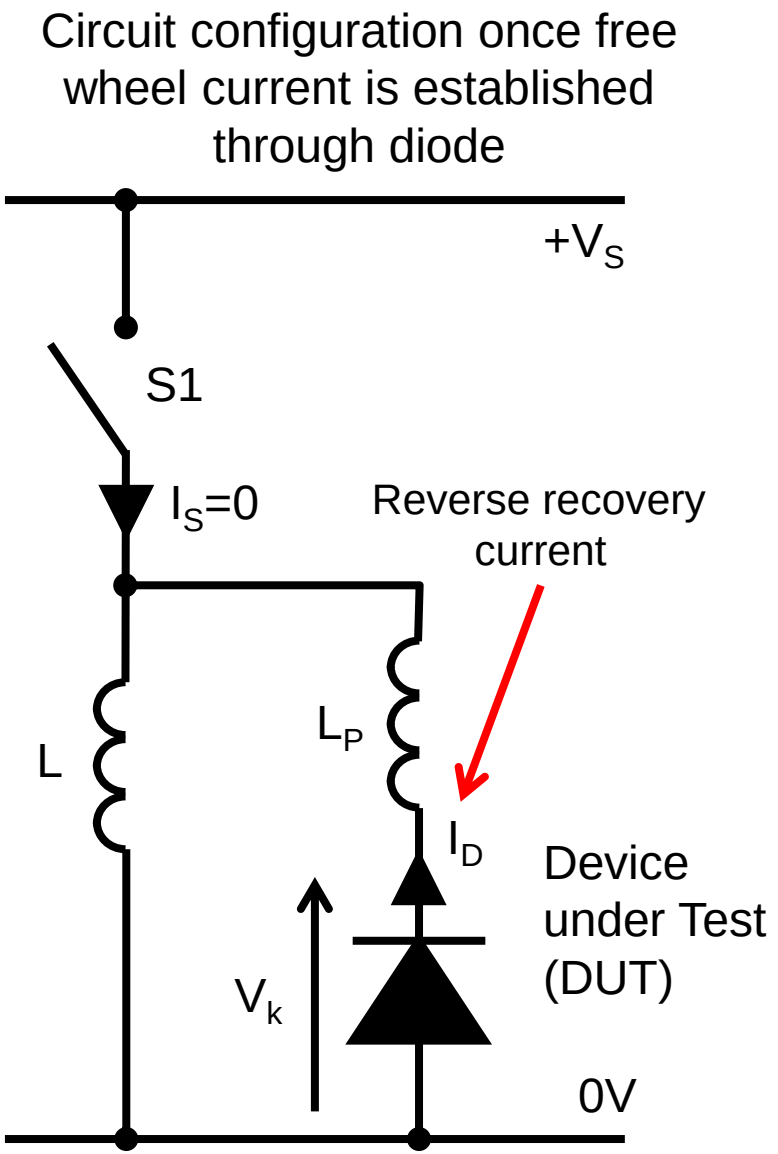
Single Phase



Chopper Representation used to emulate the switching converter for measurement of diode performance



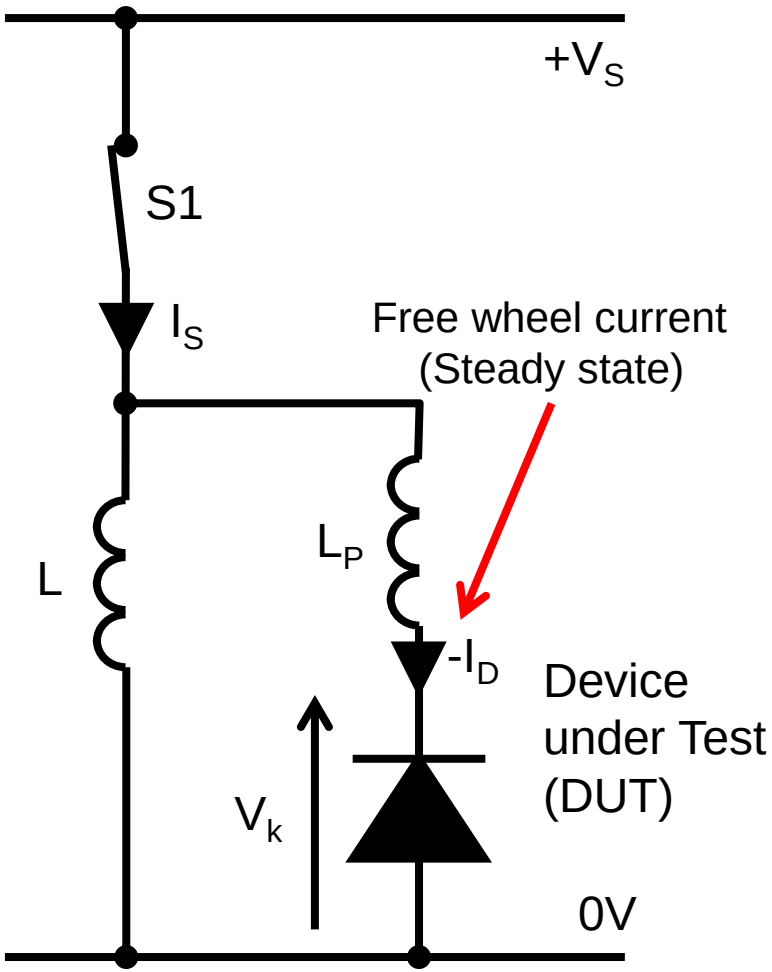
Chopper: Transient characteristic test circuit



- When S1 is in the on state current builds up in the inductor (L)
- When the desired current is obtained S1 is turned off
- The flux in the inductor attempt to collapse, causing the voltage at the K terminal to fall rapidly and the diode to become forward biased
  - Inductor current is allowed to circulate (free wheel) through the diode for long enough to establish steady state conditions

Chopper: Transient characteristic test circuit

Circuit configuration when the diode is under in initial period of reverse recovery

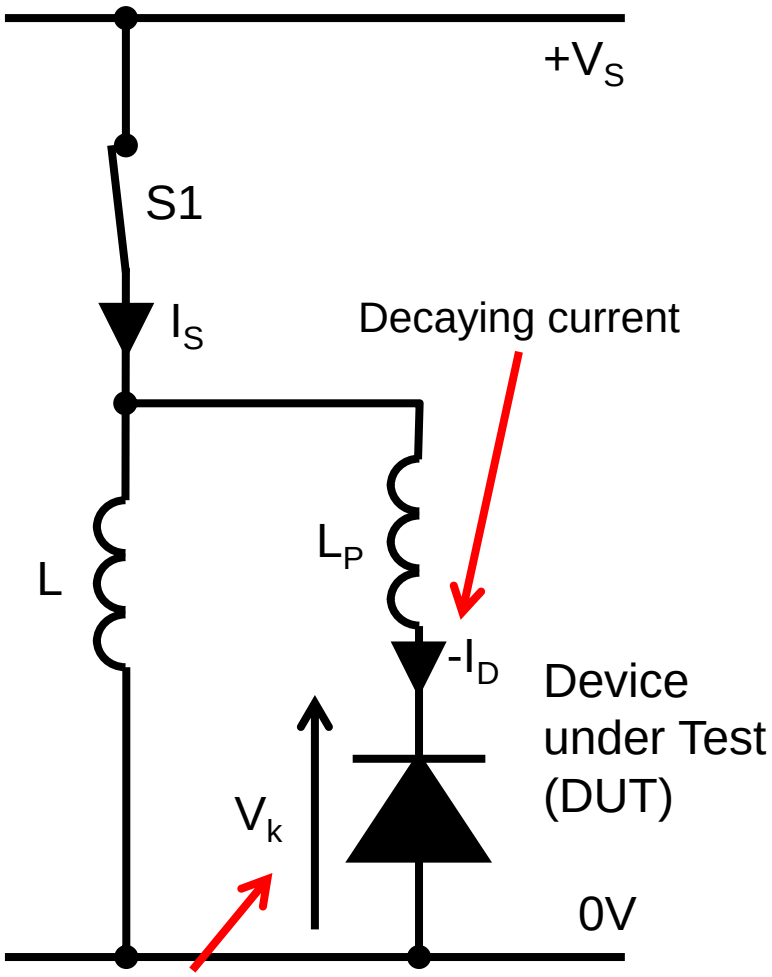


- After a steady state conduction condition is obtained through the diode
- S1 is then turned on again which attempts to reverse bias the diode
- Diode is flooded with excess carriers, a short circuit is created between the supply rails
- As S1 is turned on abruptly the rise of the short circuit current is limited by the parasitic inductance (L_P)
- With S1 turned on and the diode still conducting (reverse recovery), L_P supports the supply voltage (V_S) where:

$$-dI_D/dt = Vs/L_p$$

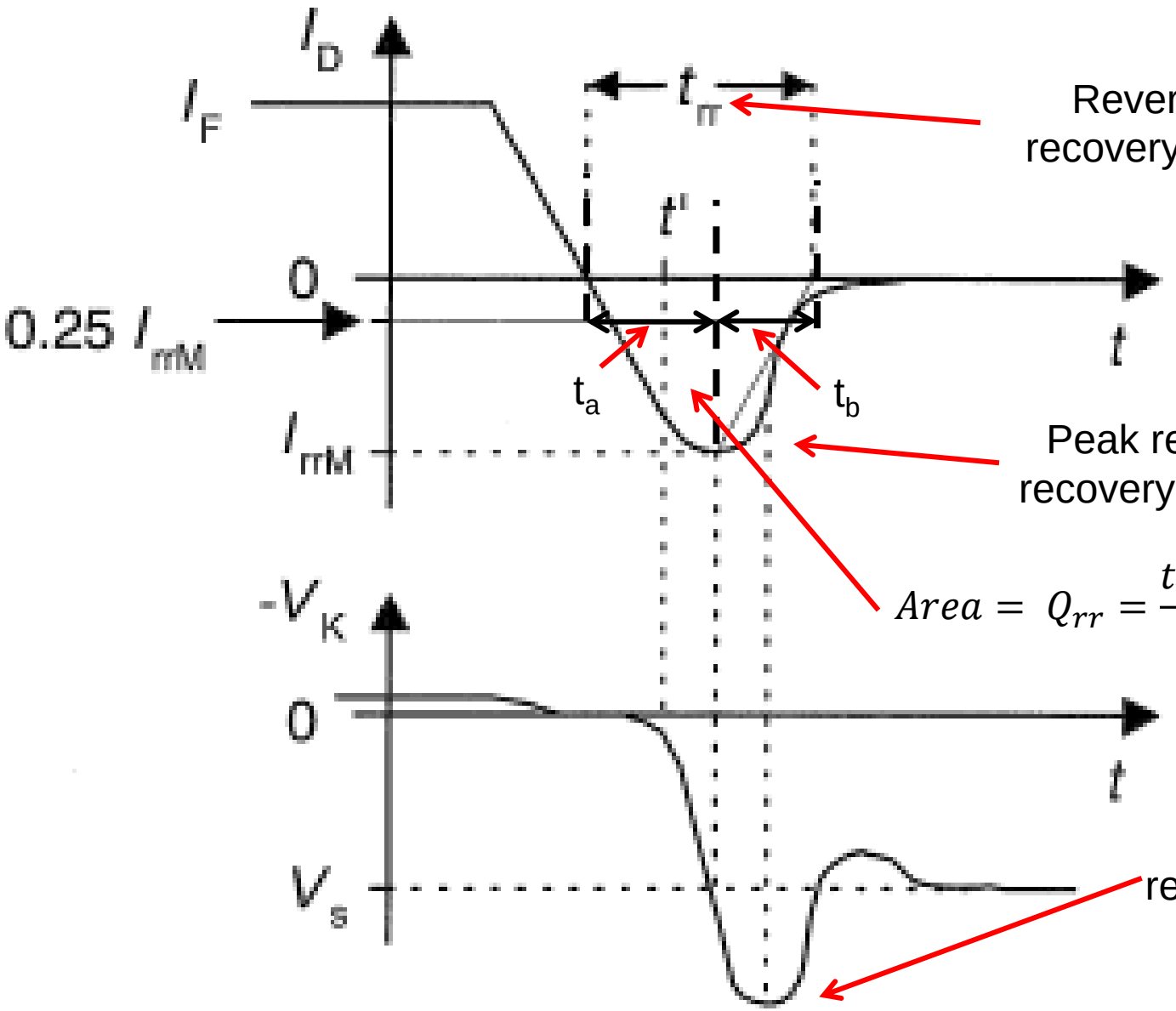
Chopper: Transient characteristic test circuit

Circuit configuration during over voltage of the diode



- Once a space charge layer forms
  - Reverse current is determined by the rate at which excess carriers continue to diffuse out from the base region of the diode
  - Reverse voltage starts to rise and the depletion layer expands accordingly
- When the reverse current reaches its maximum value I_{rrM} the reverse voltage across the diode is $V_R=V_S$
- Reverse current continues to fall to zero in the manor that reflects the distribution of any remaining carriers
- The further change in di/dt induces an overshoot of the reverse voltage as the energy stored in L_P is transferred to the diode

Diode current and voltage waveforms during reverse recovery



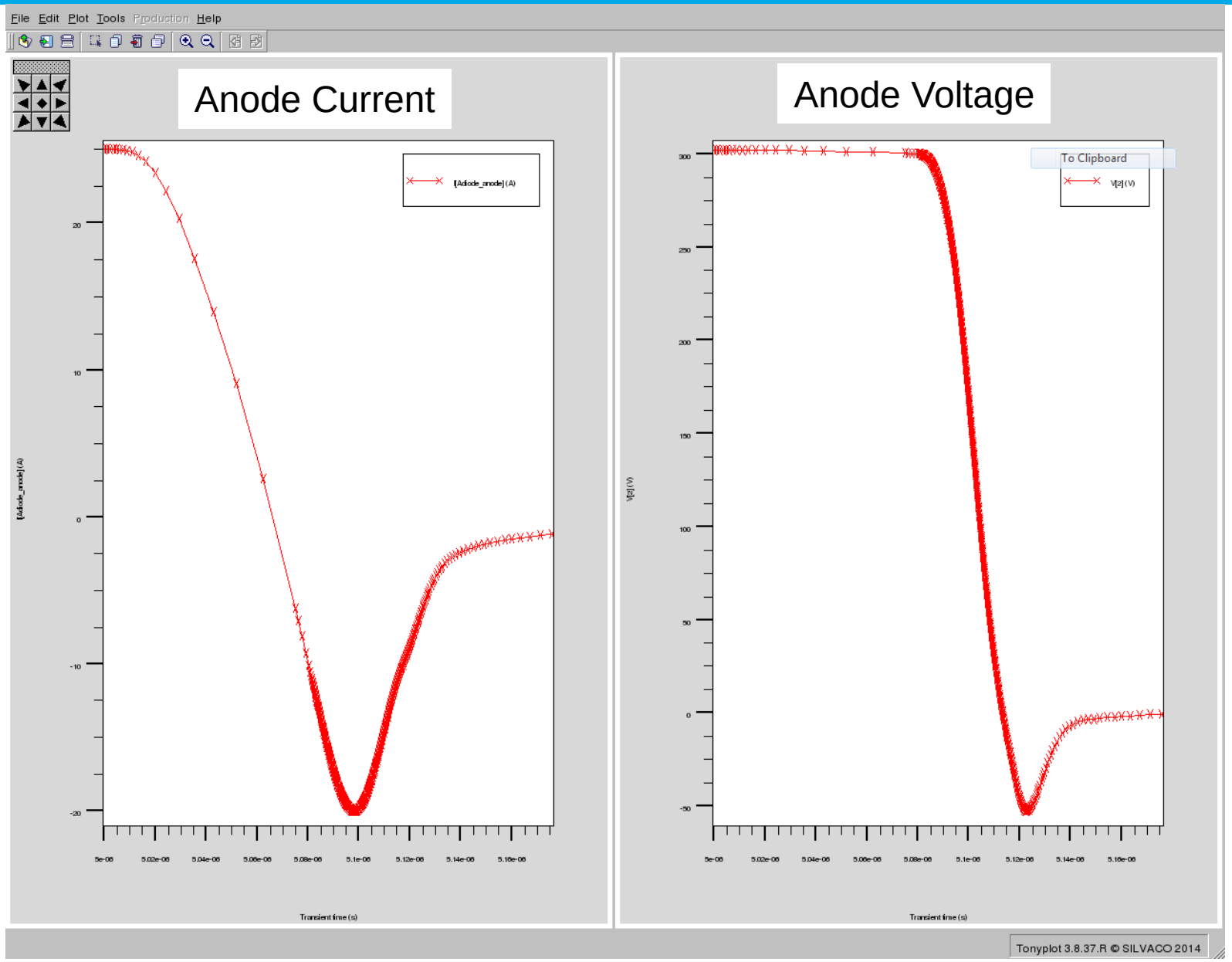
Reverse recovery time

Peak reverse recovery current

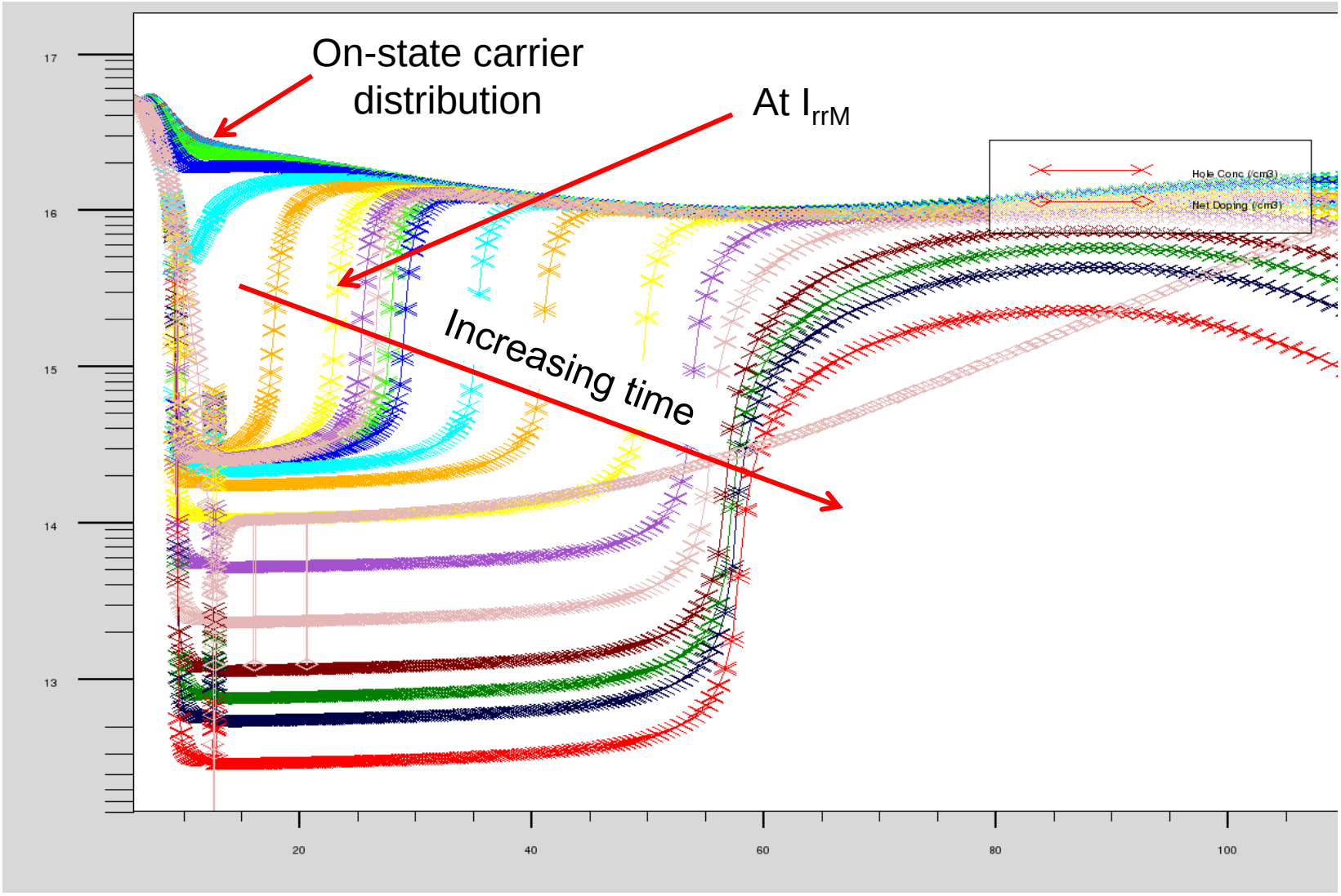
$$Area = Q_{rr} = \frac{t_{rr} I_{rrM}}{2}$$

Peak reverse recovery voltage

Reverse recovery characteristic of a 25A 600V diode



Transient carrier profile



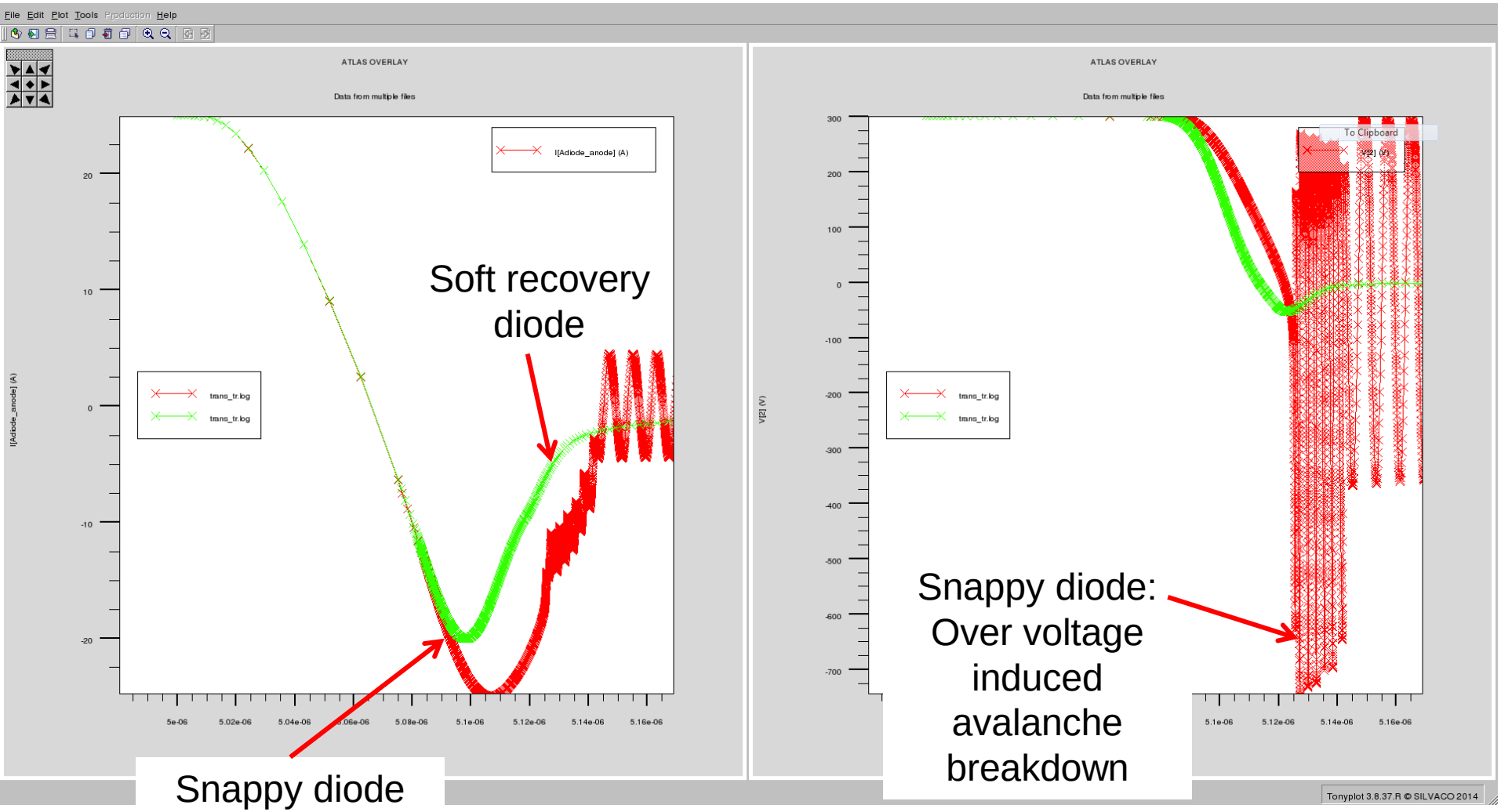
Diode transient characterisation

- The switching characteristics of power diodes are characterised by
  - The time taken for the reverse recovery process to complete (t_{rr})
  - Maximum peak reverse recovery current (I_{rrM})
  - Reverse recovery charge $Q_{rr} = \frac{I_{rrM} t_{rr}}{2}$
- Generally diodes are optimised with respect to forward voltage drop and reverse recovery losses (Q_{rr})
- However, not only the time for recovery is important but the shape of the turn off waveform (t_a and t_b)
- The softness of a diodes is determined by

$$Softness = \frac{t_b}{t_a}$$

- If the softness is less than 1 the diode is termed **snappy**
  - This results in a high over voltage causing detrimental oscillation in the circuit and giving rise to electromagnetic interference
- If softness greater than 1 it is termed **soft**

Comparison between soft and snappy recovery diodes

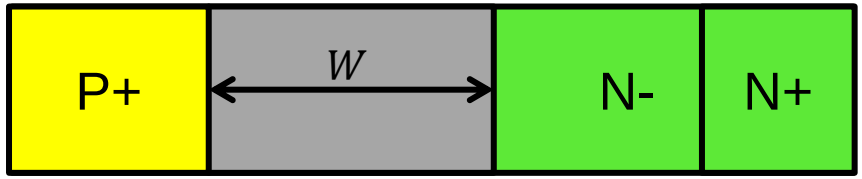


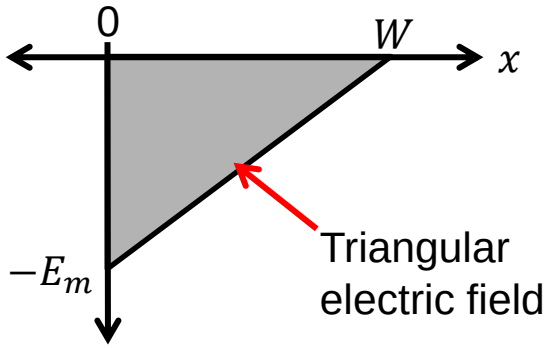
Design for soft recovery: Buffer layer diodes

- One approach to mitigate against a snappy recovery is by incorporating a buffer layer into the drift region of the diode structure
- This buffer layer is placed at the cathode side of the dope which is heavily doped compared to the n- region
  - Its doping concentration is chosen to be sufficiently large so that is cannot be depleted by the revere bias applied to the diode
  - At the same time its doping concentration is chosen to be low enough to allow conductivity modulation resulting is stored charge
- During the recovery period this stored charge is not rapidly removed as in the case of a PT design
  - This produces a much smaller change in reverse current and reduces the over voltage and oscillations associated with the hard recovery processes
- This structure provides improvements in terms of soft recovery characteristics, however forward voltage drop increases slightly due to the increased drift region thickness

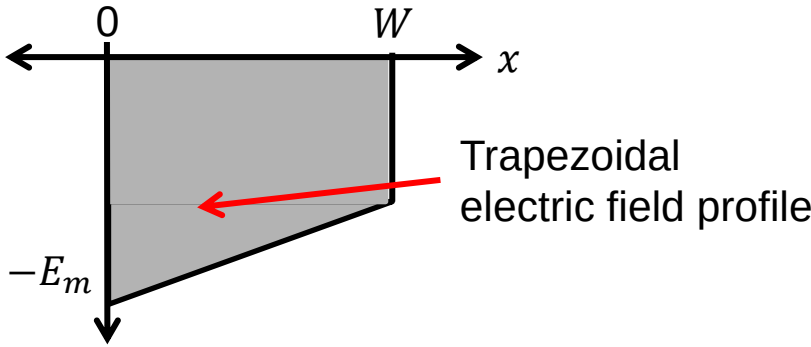
Diode drift region designs

Non-punch through design

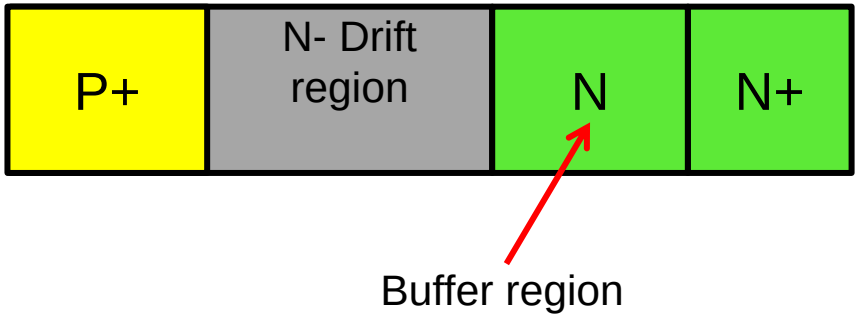


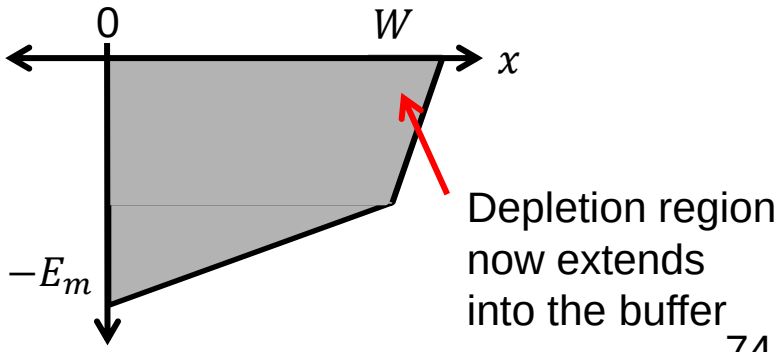


Punch through design

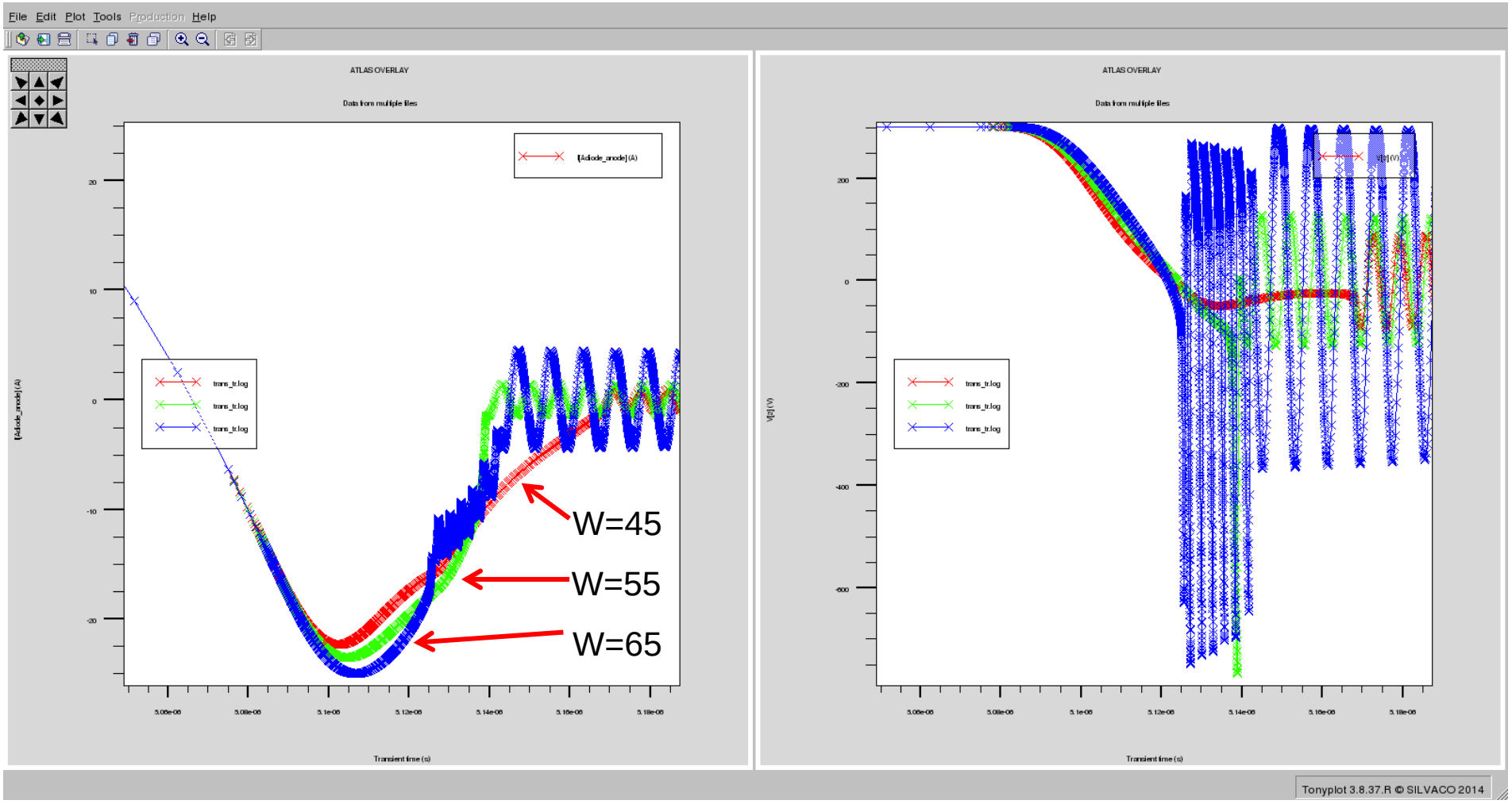


Buffer design

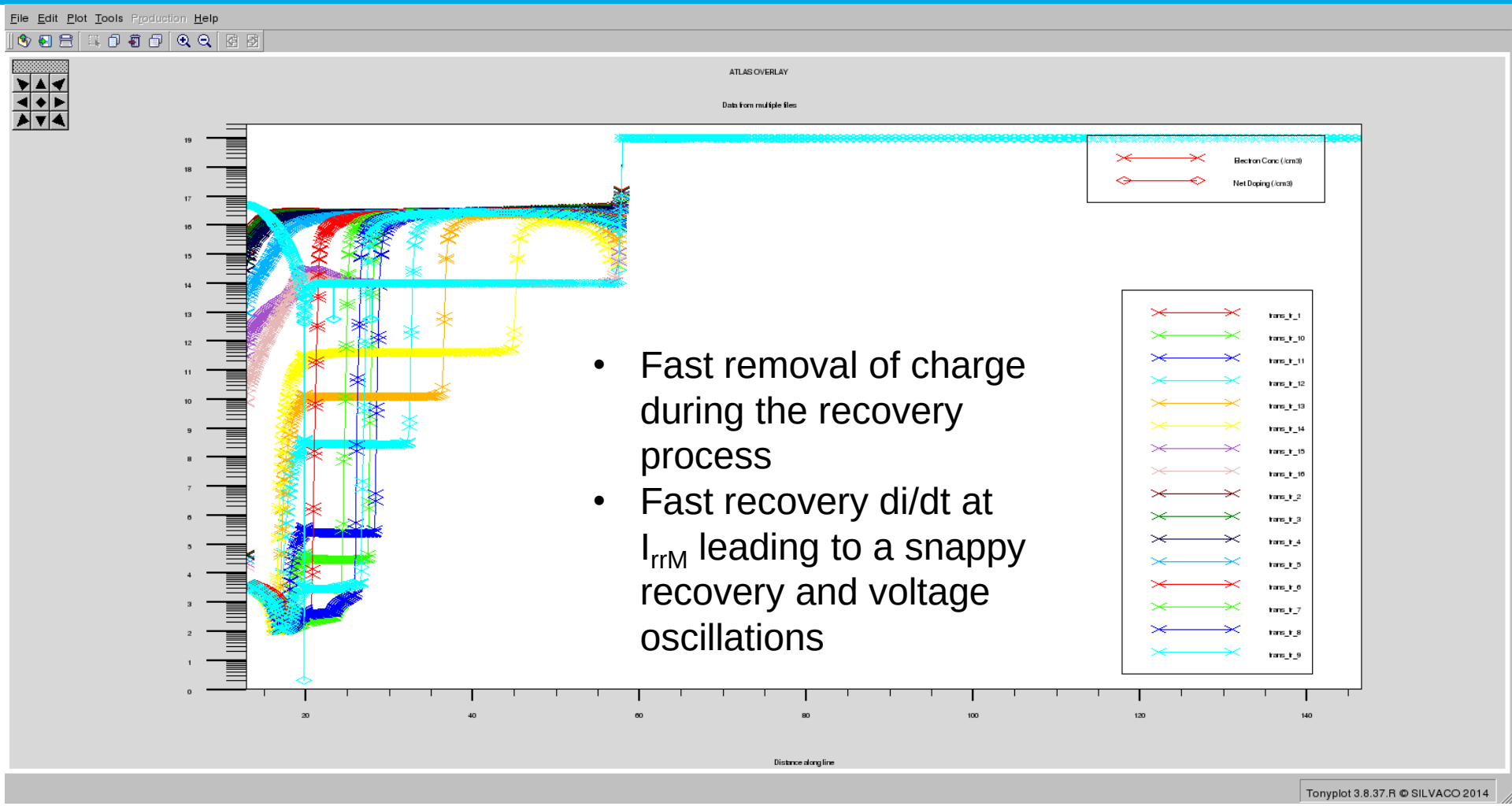




Influence of drift region design upon recovery characteristics

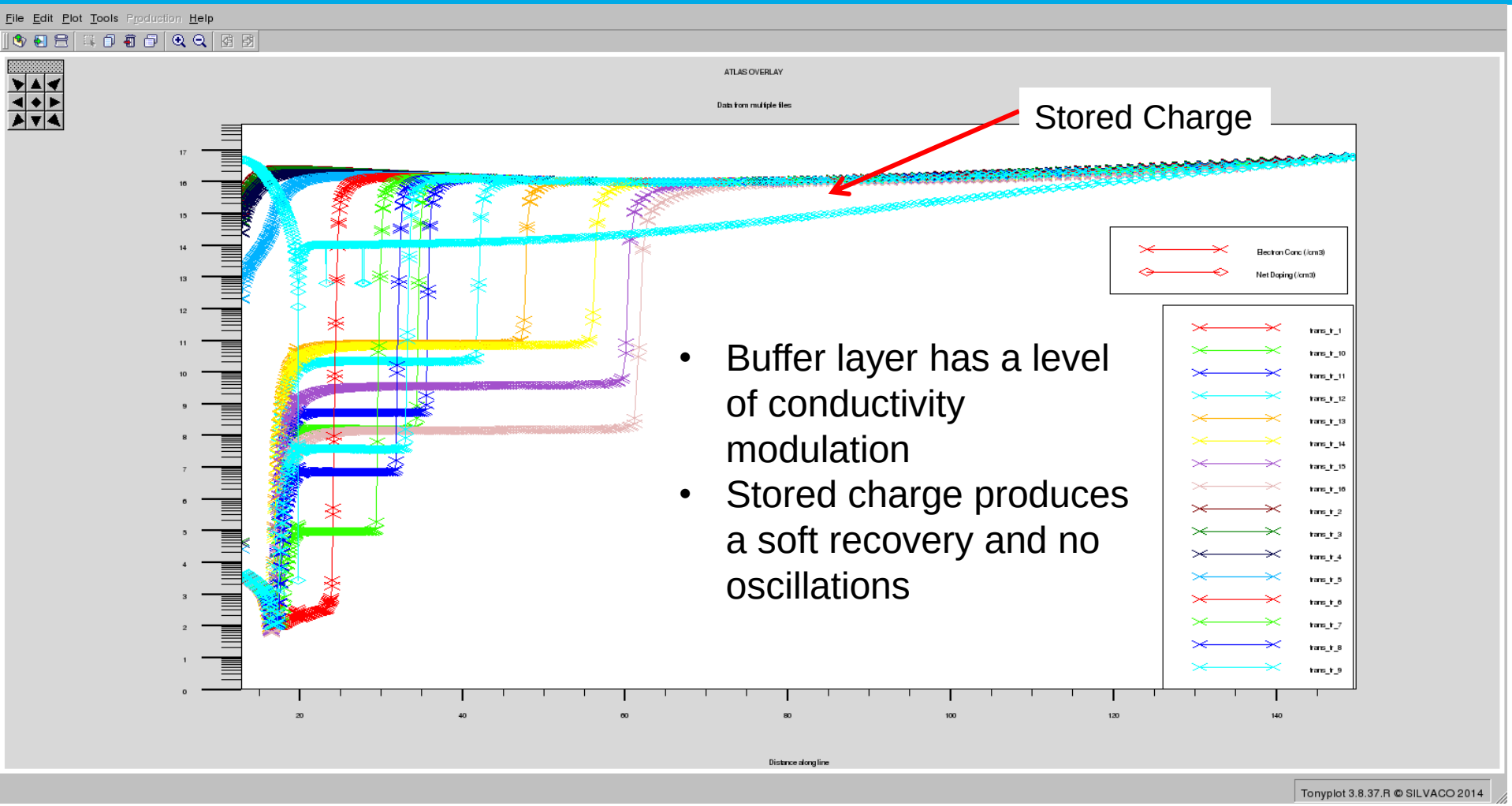


PT design: Carrier charge during recovery



- Fast removal of charge during the recovery process
- Fast recovery di/dt at I_{rrM} leading to a snappy recovery and voltage oscillations

Buffer layer diode: carrier profile during recovery (same time base)



- Buffer layer has a level of conductivity modulation
- Stored charge produces a soft recovery and no oscillations

Localised lifetime control

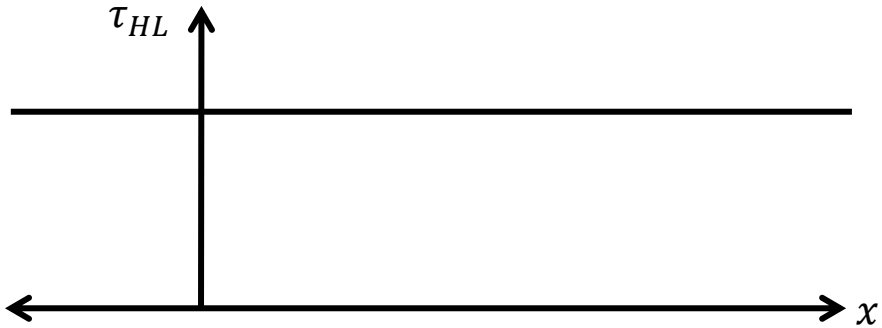
- By reducing the lifetime in the region of the p+n- junction can improve reverse recovery characteristics
- This shortens the time until peak reverse recovery current in reached (I_{rrM})
  - Less time is required until the junction recovers to support voltage
- This can be achieved by the diffusion of metals with low diffusivity such as Iridium
  - Making a diffusion profile of reduced carrier lifetime
- Or by bombarding the structure with heavy ions such as helium to break up the crystalline lattice creating localised recombination centres

Lifetime profiling

Buffer design

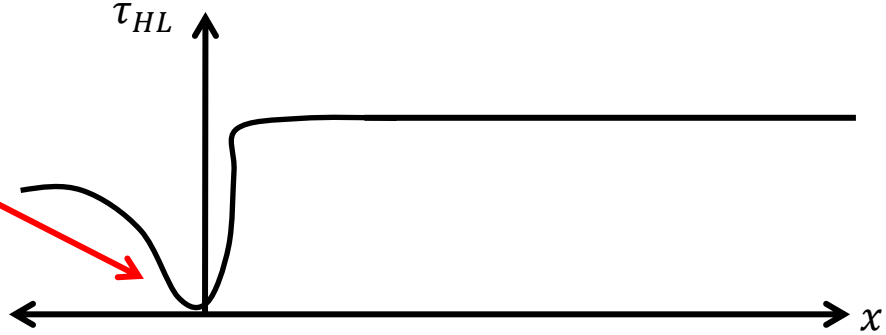
Uniform lifetime control via electron irradiation

Uniform lifetime control

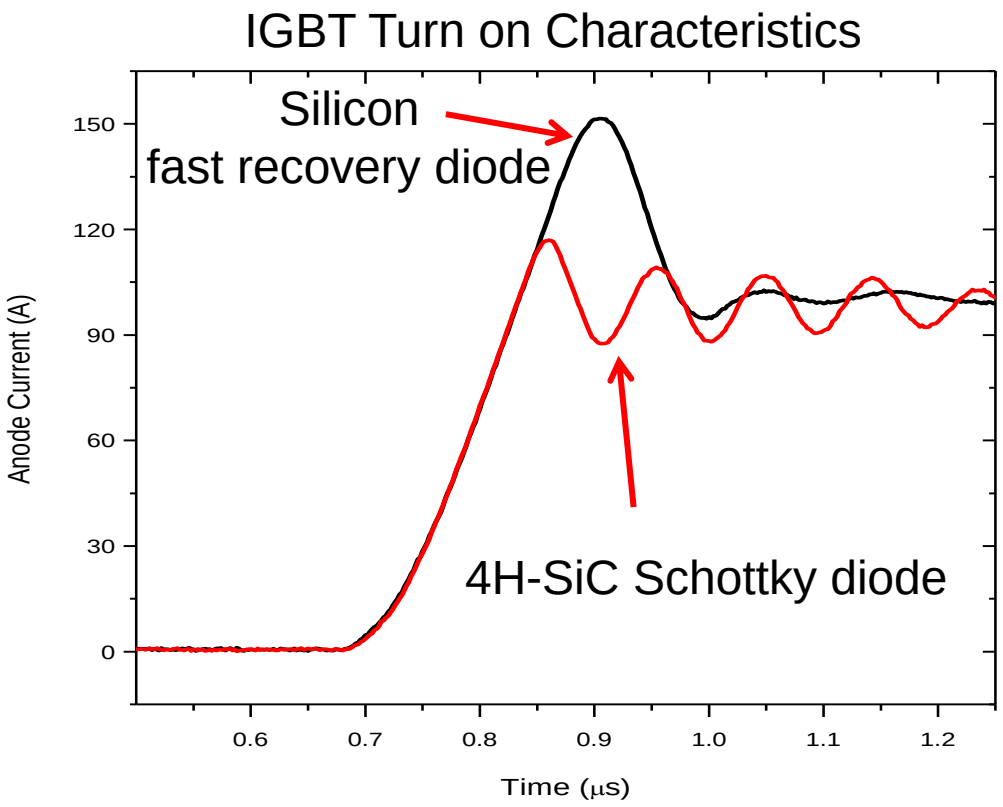


High density of recombination centres introduced by heavy atom bombardment or metal diffusion

Localised lifetime control



Comparison between 4H-SiC Schottky and Silicon Fast Recovery



- Even though the Schottky diode is a majority carrier device (no reverse recovery)
- Reverse current still flows due to the depletion region changing with voltage
  - Expanding depletion region results in displacement current as the charge is removed
- Recovery characteristic is hard causing significant ringing with the circuit parasitics

Summary

- Junction diodes operate under a condition of conductivity modulation
  - During the on-state the high resistivity n-drift region is flooded with carriers, significantly reducing its on-state resistance
- Three main drift region technologies are used to develop power diodes
  - NPT: Triangular electric field profile
    - Devices exhibit soft recovery characteristics, higher forward voltage drop
  - PT: Trapezoidal electric field profile
    - Device exhibit hard recovery characteristics, low forward voltage drop
  - Buffer: Trapezoidal electric field profile where the buffer layer supports a proportion of the voltage
    - Device exhibits a characteristic in-between NPT and PT device
- These simple drift region designs are repeated across the entire power device spectrum, i.e. IGBT's, MOSFETS etc.
- Generally modern diode structure are buffer type combined with electron (uniform) and localised lifetime killing techniques

Summary cont.

- Wide band gap semiconductor diodes are now available on the market
  - Schottky junctions
    - Majority carrier device: No conductivity modulation
  - These materials can significantly reduce drift region thickness and increase doping concentrations to significantly reduce on-state forward drop
  - These devices are majority carrier and therefore show no reverse recovery
    - Switching characteristics are snappy showing significant ringing when compared to Silicon fast recovery diode