Glossary

A

ABEL

Advanced Boolean Expression Lanaguage (ABEL) is a hardware description language (HDL) and compilation system owned and maintained by XILINX. Industry Standard Language (HDL Tool).

ABEL-HDL File

The ABEL-HDL (ABL) file is a file written in ABEL hardware description language that contains logic expressed as equations, truth tables, and state machine descriptions.

ABL File

The ABL file is a file written in ABEL hardware description language that contains logic expressed as equations, truth tables, and state machine descriptions.

accumulator

A register for adding, subtracting, or both.

adder

A combinatorial circuit that computes the sum of two or more numbers.

address

The identification of a storage location, such as a register or a memory cell.

Adobe PostScript

A page description language (PDL) developed by Adobe Systems Incorporated, and used on many high-end printers.

Adobe Type Manager (ATM)

A font management and rasterization program which converts Adobe Type 1 and Type 3 fonts to bitmaps for printing or display on a computer screen. ATM is available as a program to run in the

Windows environment to allow the display of PostScript fonts by Windows programs, and is built-in to some other graphical user interfaces.

ampere

A measure of electrical flow or current.

analog

Analog refers to a continuous numeric scale, as opposed to the digital scale of discrete values.

annotation

The insertion of simulation values into the schematic.

antifuse

A device in which connections are permanently programmed by burning out a fuse.

API

Applications Programming Interface. A set of software libraries, developed by a particular software vendor, that allows third party software programs to interface with programs from that vendor.

architecture

The common logic structure of a family of programmable integrated circuits. The same architecture can be realized in different manufacturing processes. Examples of Xilinx architectures are the Virtex, Spartan-II, and CoolRunner-II devices.

Architecture Wizard

A graphical application that allows you to customize Digital Clock Manager (DCM) and Rocket I/O™ transceivers. It generates HDL files for all supported synthesis tools. It also allows jitter calculation for DCMs and channel bonding for Rocket I/O transceivers. This application is available from the Project Navigator.

area constraints

Area constraints are created by the user or a process such as synthesis to direct the optimization process that takes place during design implementation.

area-and-speed calculator

A process that provides information about the area versus speed trade-offs for a design. The synthesis tools use this information to estimate the trade-offs accurately.

arithmetic equations

Equations which specify the special arithmetic capabilities of the Xilinx CPLDs.

Arithmetic Logic Unit (ALU)

A logic function that performs arithmetic computations, such as addition, multiplication, and comparison operations. The ALU is one component of the central processing unit (CPU).

ASIC

An application-specific integrated circuit (ASIC) is either a full-custom circuit in which every mask is defined by the user or a semi-custom circuit (gate array) where only a few masks are defined.

asynchronous debugging

A debugging mode in which you capture data without controlling your system clock.

asynchronous logic

Logic which changes state independently of clock changes.

A signal whose intended function is performed immediately when the signal is asserted without regard to a clock.

asynchronous register

A register whose state changes independently from the clock.

Asynchronous Transfer Mode (ATM)

A method of transmitting voice, data, and video in fixed-size packets over high-speed telecommunications channels.

attributes

Instructions placed on symbols or nets in an FPGA or CPLD schematic to indicate their placement, implementation, naming, directionality, or other properties.

B

back-annotation

Translation of a routed or fitted design to a timing simulation netlist.

bandwidth

A measure of a circuit's ability to carry or process information. More or greater bandwidth means more carrying capacity or greater processing power, usually achieved at greater cost.

baud rate

The rate of data transmission in bits per second.

behavior

A set of sequential statements specified within a process statement.

behavioral design

A technology-independent, text-based design that incorporates high-level functionality and high-level information flow.

behavioral design method

A method of defining a circuit in terms of a textual language rather than a schematic of interconnected symbols.

behavioral simulation

Also known as functional simulation. Behavioral simulation is usually performed on designs that are entered using a hardware description language (HDL).

This type of simulation takes place during the pre-synthesis stage of HDL design. Functional simulation checks that the HDL code describes the desired design behavior.

Behavioral simulation is a simulation process that is performed by interpreting the equations that define the design. The equations do not need to be converted to the logic that represents them.

BEL

Basic Element of Logic (BEL). Examples of BELs are flip-flops, MUXes, LUTs. Typically a BEL (but not always) corresponds 1:1 with an instance in the logical / structural (post synthesis) view of the design.

binary

A numbering system based on base 2 with only two digits, 0 and 1. Unsigned binary refers to non-negative binary representation.

binary counter

A counter implemented in base 2.

binary encoding

Binary or maximal encoding is a type of state machine encoding that uses the minimum number of registers to encode the machine. Each register is used to its maximum capability.

bit

A binary digit representing 0 or 1.

BIT file

A BIT file is the same as a bitstream file.

BitGen

Is a program that produces a bitstream for Xilinx device configuration. BitGen takes a fully routed circuit description (NCD) file as its input and produces a configuration bitstream, a binary file with a .bit extension.

bitstream

A bitstream is a stream of data that contains location information for logic on a device, that is, the placement of configurable logic blocks (CLBs), input/output blocks (IOBs), tristate buffer (TBUFs), pins, and routing elements. The bitstream also includes empty placeholders that are filled with the logical states sent by the device during a readback. Only the memory elements, such as flip-flops, RAMs, and CLB outputs, are mapped to these placeholders, because their contents are likely to change from one state to another. When downloaded to a device, a bitstream configures the logic of a device and programs the device so that the states of that device can be read back. A bitstream file has a .bit extension.

block

1. A group of one or more logic functions.
2. A schematic or symbol sheet. There are four types of blocks:
   - A Composite block indicates that the design is hierarchical. A composite block is a symbol representing an underlying schematic or netlist.
   - A Module block is a symbol with no underlying schematic. A module block is also referred to as a primitive.
   - A Pin block represents a schematic pin.
   - An Annotate block is a symbol without electrical connectivity that is used only for documentation and graphics.

block RAM

A block of random access memory built into a device, as distinguished from distributed, LUT based random access memory.

BMM file

A BMM file is a block RAM memory map file. It is in ASCII format and describes the organization of block RAM memory. The BMM file is used in PowerPC and MicroBlaze designs.

bonded

Connected by a wire.

bottom-up design

An HDL design methodology where already defined HDL blocks are merged into one overall desired design behavior.The lowest level portion of your design is completed first. Only after the low-level building blocks are complete do you finish higher-level hierarchical blocks in your design. This methodology is typically used with schematic capture programs.

boundary scan

A method used for board-level testing of electronic assemblies. The primary objectives are the testing of chip
I/O signals and the interconnections between ICs.

It is the method for observing and controlling all new chip I/O signals through a standard interface called a Test Access Port (TAP). The boundary scan architecture includes four dedicated I/O pins for control and is described in IEEE spec 1149.1.

bounds

The range of a LogiBLOX bus defined by the left and right indices of the bits on that bus.

breakpoint

A condition for which a simulator must stop to perform simulation commands.

buffer

An element used to increase the current or drive of a weak signal and, consequently, increase the fanout of the signal. A storage element.

BUFT

A tristate buffer.

bus

A group of two or more signals that carry closely-associated signals in an electronic design.

byte

A binary word consisting of eight bits. When used to store a number value, a byte can represent a number from 0 to 255.

byte-wide PROM

A programmable read-only memory (PROM) which supplies data one byte at a time.

C

CAE

Computer Aided Engineering. The original term for electronic design automation (EDA). Now, often refers to the sofware tools used to develop the manufacturing tooling for the production of electronic system such as for the panelization of circuit boards.

CAE tool

A Computer-Aided Engineering tool (CAE). Usually refers to programs such as Innoveda, Cadence, or Mentor Graphics that are used to perform design entry and design verification.

capacitance

A property that measures the storage of electrically separated charges.

The load on a net.

carry

A quantity that is transferred in addition and subtraction from one number to the next one of higher place value.

carry logic

Logic which is designed to speed-up and reduce the area of counters, adders, incrementers, decrementers, comparators, and subtractors. It is a special interconnect that speeds up the carry path of adders and counters from one CLB to another. This dedicated carry line runs along each column of CLBs as well as the top and bottom CLBs.

carry-logic modes

The forty-three specific carry-logic functions, such as decrement and increment, available in each CLB configuration.

carry look-ahead

A mechanism that enables the carries to be simultaneously applied to the sum bits in a parallel adder.

carry path

The computation of the carries in addition or subtraction from one CLB to another.

carry propagation time

The time it takes for a carry signal to traverse through the levels of component gates.

cascade

A circuit which connects the inputs of a module to the outputs of another.

cell

A hierarchical description of an FPGA device.

checksum

A summation of bits or digits generated according to an arbitrary formula used for checking data integrity. To verify that the data represented by a checksum number has been entered correctly, verify that the checksum number generated after processing is the same as the initial number.

chip

Another term for an integrated circuit (IC).

CLB

Configurable logic block. The basic FPGA cell. A CLB includes function generators (lookup tables, or LUTs), registers (flip-flops or latches), and reprogrammable routing controls (multiplexers).

CLBs implement macros and other designed functions. They provide the physical support for an implemented and downloaded design. CLBs have inputs on each side, and this versatility makes them flexible for the mapping and partitioning of logic.

clear preset

A synchronous reset.

clock

A signal that represents the time that a wave stays at a High or Low state. The rising and falling edges of a clock square wave trigger the activity of the circuits.

clock buffer

A circuit element used to increase the current or drive of a weak clock signal and consequently increase its fanout.

clock enable

A binary signal that allows or disallows synchronous logic to change with a clock signal. When enabled, this control signal permits a device to be clocked and to become active. There are four different states. The two active High states are CE 0 disabled and CE 1 enabled. The two active Low states are $\overline{\text{CE}}$ 0 enabled and $\overline{\text{CE}}$ 1 disabled.

clock input path

A path which starts at either an input of the chip or at the output of a flip-flop, latch, or RAM and ends at any clock pin on a flip-flop or latch enable. The clock input path time is the maximum time required for the signal to arrive at the flip-flop clock input. Clock input paths help to determine system-level design timing.

clock period

The time required for a periodic waveform to repeat itself.

clock skew

The time differential between two or more destination pins in a path.

clock-to-pad path (C2P)

A path which starts at the Q output of a flip-flop or latch and ends at an output of the chip. It includes the clock-to-Q delay of the flip-flop and the path delay from that flip-flop to the chip output. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and arrive at the output before the next clock edge occurs.

clock-to-setup path (C2S)

A path which starts at the Q output of a flip-flop or latch and ends at an input to another flip-flop, latch, or RAM, where that pin has a setup requirement before a clocking signal. It includes the clock-to-Q delay of a flip-flop, the path delay from that flip-flop to the next flip-flop, and the setup requirement of the next flip-flop. The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs.

CMOS

Complementary Metal Oxide Semiconductor. An advanced IC manufacturing process technology characterized by high integration, low cost, low power, and high performance.

CMOS transistors

CMOS transistors are used in pips (Programmable Interconnect Points) and switching matrices.

combinatorial input

Combinatorial input is the combination of a pad primitive and a function primitive.

combinatorial logic

Logic that has no storage capacity, that is, not controlled by a clock (asynchronous). For example, logic gates.

command file

In simulation, a command file is a file containing a list of commands that assign vectors, generate input waveforms and clocks, and display signals. It is submitted for execution during simulation. You can create a command file with a text editor or from a set of input waveforms.

comp

Comps are comprised of BELs. A slice is one example of a comp. The comp is the unit of granularity for placement and routing in the FPGA Editor. Also the comp is the level at which device timing is characterized.

compiler

A language interpreter. The Synopsys compiler interprets HDL and makes concurrent process implementations for target architectures.

complexity

The number of gates on a device.

component

A logical configuration that will, at some point, go into a physical site. Examples of components are CLBs, IOBs, tristate buffers, pull-up resistors, and oscillators.

component interface

A description of how a Mentor Graphics component interfaces with upper-level hierarchy. A port description with a model registry, roughly equivalent to an entity port listing (along with architecture declarations) in VHDL.

component interface browser (CIB)

A program that allows a designer to view and edit a component interface. In most cases, this is done to add or remove models from a component's model registry.

concurrent statements

The order of these statements is not important in architecture body.

configuration

The process of loading design-specific bitstreams into one or more devices to define the functional operation of the logical blocks, their interconnections, and the chip I/O.

configuration file

A configuration file is a file that contains the bitstream used to program an FPGA device or PROM. The format of that file can be binary (.bit) or ASCII format file (.mcs or .rst).

Configuration Modes

Configuration Modes are the modes available on the Xilinx configuration cables. They include JTAG, SelectMAP and Slave Serial.

configuration pins

Pins that are used to load design-specific programming data into one or more logic blocks to define the functional operation of a device's internal blocks and interconnections.

console log

A record of the commands that you invoked during a session.

constraints

Specifications for the implementation process. There are several categories of constraints: routing, timing, area, mapping, and placement constraints.

Using attributes, you can force the placement of logic (macros) in CLBs, the location of CLBs on the chip, and the maximum delay between flip-flops. PAR does not attempt to change the location of constrained logic.

Constraints Editor

A graphical user interface (GUI) tool for entering timing constraints and pin location constraints. The user interface simplifies constraint entry by guiding you through constraint creation without your needing to understand UCF file syntax.

constraints file

A file which specifies constraints (location and path delay) information in a textual form. An alternate method is to place constraints on a schematic.

contention

The state in which multiple conflicting outputs drive the same net.

CORE Generator

A design tool that delivers parameterized COREs optimized for Xilinx FPGAs. The tool provides a catalog of ready-made functions ranging in complexity from simple arithmetic operators such as adders, accumulators, and multipliers, to system-level building blocks such as filters, transforms, FIFOs, and memories.

counter

A circuit, composed of registers, that counts pulses, often reacting or causing a reaction to a predetermined pulse or series of pulses. Also called a divider, sometimes accumulator.

CPLD

Complex Programmable Logic Device (CPLD). A single-chip logic solution. Xilinx CPLD families include XC9500, XC9500XL, XC9500XV, CoolRunner XPLA3, and CoolRunner-II devices.

critical path

A signal in a section of combinatorial logic that limits the speed of the logic. Storage elements begin and end a critical path, which may include I/O pads.

cross probing

Interprocess communication between software tools.

D

daisy chain

A series of bitstream files concatenated in one file. It can be used to program several FPGAs connected in a daisy chain board configuration.

dangling bus

A bus which connects to a component pin or net at one end and unconnects at the other. A small filled box at the end of the bus indicates a dangling bus.

dangling net

A net which connects to a component pin or net at one end and unconnects at the other. A small filled box at the end of the net indicates a dangling net.

Data2Mem

This Xilinx program conveniently incorporates CPU software images into FPGA bitstreams, and executes that software from block RAM-built address space.

dataflow modeling

The use of concurrent signal assignment statements.

DCM

Digital Clock Manager. A design element which provides multiple functions. It can implement a clock delay locked loop, a digital frequency synthesizer, digital phase shifter, and a digital spread spectrum.

debugging

The process of reading back or probing the states of a configured device to ensure that the device is behaving as expected while in circuit.

decoder

A circuit that translates *n* input lines of binary information into 2*n* output lines. It is the opposite of an encoder.

Delay Locked Loop (DLL)

A digital circuit used to perform clock management functions on and off-chip.

density

The number of gates on a device.

design implementation

A design implementation is a design implementation specification as opposed to the functional specification of the design. The implementation specification refers to the actual implementation of the design from low-level components expressed in bits. The functional specification refers to the definition of the design or circuit function.

design methodologies

The techniques used to enter a design, either behavioral or schematic entry.

design rule check

A Design Rule Check (DRC) is a series of tests to discover logical and physical errors in the design.

design specification

The top-level of a design used to define its function. The specifications function is created in terms of behavioral or structural primitives. The two methods of entering a design are graphical descriptions (schematics) and textual descriptions (HDL).

destination

A sink node or stopping point for a timing analysispath, the data input of a synchronous element or a pad.

device

A device is an integrated circuit or other solid-state circuit formed in semiconducting materials during manufacturing. Each Xilinx architecture family contains specific devices, such as xc2vp2 and xc2s50. A complete Xilinx part number includes architecture (for example, Virtex-II Pro), device (for example, xc2vp2), package (for example, cs144), and speed (for example, -6).

device model

A VHDL description of the internal and external views of a digital device, including the structure and the communication interface of the device with its environment.

differential pairs

Differential pairs are identical to LVDS (Low Voltage Differential Signals) and LVPECL signals. Some devices incorporate differential signaling. Two pins are utilized for these signals to be connected to the device. These are known as differential pin pairs. Each differential pin pair has a positive (P) and a negative (N) pin. I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the differential pairs can be used for asynchronous output signals. Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous.

digital

Digital refers to the representation of information by code of discrete elements, as opposed to the continuous scale of analog representation.

DIN pin

An FPGA pin that loads a bitstream in serial mode. On the XChecker cable, it provides the bitstream data and connects to the DIN pin of the target FPGA.

direct interconnect

A net that aligns the carry with the CLB rows and columns, propagating and connecting the carry to the flip-flops of a counter.

distributed RAM

RAM (Random Access Memory) that is distributed throughout the programmable logic in the CLBs. Distributed RAM can be used to change the address values (16^1) of the function generator (lookup table, or LUT) that it is a part of.

distributed ROM

ROM (Read Only Memory) that is distributed throughout the programmable logic in the CLBs.

don’t-care

The value of a variable when the value of that variable has no effect on the output. Don’t-care values are represented by an X in truth tables.

double-length line

An interconnect line that is switched only every other switch matrix.

downloading

Downloading is the process of configuring or programming a device by sending data to the device.

drawn width

The machine-calibrated gate width.

DRC

Design Rule Checker. A program that checks the (NCD) file for design implementations for errors.

DSP

Digital Signal Processing. A powerful and flexible technique of processing analog (linear) signals in digital form used in CoreGen.

duty cycle

In digital electronics, this term describes the percentage that a digital signal is High during one cycle. For example, a 60% duty cycle means that the voltage is High (logical 1) for 60% of the cycle which means that the voltage is Low for 40% of the cycle.

E

ECS Schematic Editor

Engineering Capture System. The Xilinx graphical user interface (GUI) that allows you to create, view,and edit schematics and symbols. ECS is accessed from the Project Navigator.

EDA

Electronic Design Automation. A generic name for all methods of entering and processing digital and analog designs for further processing, simulation, and implementation.

edge decoder

A decoder whose placement is constrained to precise positions within a side of the FPGA device.

EDIF

Electronic Data Interchange Format. An industry standard file format for specifying a design netlist.

editor

A tool that allows you to view or modify an ASCII file.

effective width

The actual gate width after diffusion.

effort level

Effort level refers to how hard the Xilinx Design System (XDS) tries to place a design. The effort level settings are as follows:

- High, which provides the highest quality placement but requires the longest execution time. Use high effort on designs that do not route or do not meet your performance requirements.
- Medium, provides a trade-off between execution time and high quality placement for most designs.
- Standard, which is the default effort level, provides a lower quality placement but requires the shortest execution time.

enable input

A binary input that controls whether an output is enabled or disabled.

encoded state machine

A state machine which requires that you define the value of the state register for each state in the state table.

encoder

A symbol that translates 2*n* input lines of binary information into *n* output lines. It is the opposite of a decoder.

encoding

The data encoding scheme used for a design. The bit, unsigned binary, two's complement, and one-hot encodings are supported by X-BLOX.

end point

A node which acts as either the driver to begin a path or a load to end a path.

entity

A set of interconnected components.

EPROM

An erasable PROM, which can be reprogrammed many times. Previous programs are simply erased by exposing the chip to ultra-violet light.

An EEPROM, or electrically erasable PROM, is another variety of EPROM that can be erased electrically.

equation splitting

An automatic process performed by CPLDs to divide large behavioral equations into smaller functions that will fit within the available device macrocell resources.

equations files

Files that are used in behavioral designs.

EXORmacs

EXORmacs is a MotorolaPROM format supported by the Xilinx tools. Its maximum address is 16 777 216. This format supports PROM files of up to (8 x 16 777 216) = 134 217 728 bits.

external clock

The external clock is the system clock that is used from the target board during synchronous mode debugging. To use an external clock, connect the system clock to the CLKI pin and connect the download cable CLKO pin to the system clock loads.

F

fabless semiconductor companies

A class of semiconductor companies that design, test, market, and sell ICs, but subcontract wafer manufacturing by forming alliances with silicon wafer manufacturers.

FAE

Field Application Engineer. A field-resident engineering expert who provides onsite technical support for customer applications.

fanin

The number of parallel inputs a chip can absorb.

fanout

The maximum number of specified unit loads that a specified output can drive.

fast carry

Arithmetic carry functions that use the dedicated fast carry chain that interconnects macrocells (CPLDs) or CLBs (FPGAs). These signals do not pass through the universal interconnect matrix universal interconnect matrix (UIM).

fast function block (FFB)

A group of macrocells in a CPLD that can process very high-speed logic.

fast output enable (FOE)

A tristate control signal that uses the dedicated FOE wiring of the device, not the universal interconnect matrix (UIM) wiring.

FastCLK

A clock signal that uses the dedicated FastCLK wiring of the device, and not the universal interconnect matrix (UIM).

FastInput

An input to the device that connects directly to the function block inputs, bypassing the universal interconnect matrix (UIM).

FIFO

A serial-in/serial-out shift register.

fitting

The process of putting logic from your design into physical macrocell locations in the CPLD. Routing is performed automatically.

fitter

Software that maps a PLD logic description into the target CPLD.

flash memory

A type of programmable chip that retains data even when the power is turned off.

flat design

A flat design is a design composed of multiple sheets at the top-level schematic.

flattening

The process of resolving all of the hierarchy references in a design. If a design contains several instantiations of a logic module, the flattened version of that design will duplicate the logic for each instantiation. A flattened design still contains hierarchical names for instances and nets.

flip-flop

A simple two-state logic buffer activated by a clock and fed by a single input working in combination with the clock. The states are High and Low. When the clock goes High, the flip-flop works as a buffer as it outputs the value of the D input at the time the clock rises. The value is kept until the next clock cycle (rising clock edge). The output is not affected when the clock goes Low (falling clock edge).

floorplanning

1. The process of choosing the best grouping and connectivity of logic in a design.
2. The process of manually placing blocks of logic in an FPGA where the goal is to increase density, routability, or performance.

flow

An ordered sequence of processes that are executed to produce an implementation of a design.

footprint

The shape, pin names, and functionality of a library macro or component.

foundry

A silicon wafer fabrication facility. It is also called a fab.

FPGA

Field Programmable Gate Array. A class of integrated circuits pioneered by Xilinx in which the logic function is defined by the customer using Xilinx development system software after the IC has been manufactured and delivered to the end user. Gate arrays are another type of IC whose logic is defined during the manufacturing process. Xilinx supplies RAM-based FPGA devices.

FPGA applications include fast counters, fast pipelined designs, register intensive designs, and battery powered multi-level logic.

FPGA Editor

A graphical application for displaying and configuring Field Programmable Gate Arrays (FPGAs). The FPGA Editor requires a Native Circuit Description (.ncd) file. This file contains the logic of your design mapped to components (such as CLBs and IOBs). In addition, the FPGA Editor reads from and writes to a Physical Constraints File (PCF).

FPGA Compiler

A Synopsys product which constrains and synthesizes an FPGA.

frequency

Frequency, IC design speed, is defined by the longest path delay in a circuit from a synchronous element to another synchronous element.

FROM:TO timespecs

A style of specifying timing which allows point-to-point, group-to-group, one-to-many, and many-to-one path types to be specified.

function block

The high-density function block of the device, designed to provide the maximum logic density and containing several macrocells. The output pins associated with function blocks have the standard current drive capability.

function generator

A look-up table or black box with three or four inputs implementing any combinational functions of $(2^2)^4$ or 256 functions or $(2^2)^2$ or 65556 functions. The output is any value resulting from the logical functions executed within the box. The function generator implements a complete truth table, allowing speedy prediction of the output.

functional simulation

The process of identifying logic errors in your design before it is implemented in a Xilinx device. Because timing information for the design is not available, the simulator tests the logic in the design using unit delays. Functional simulation is usually performed at the early stages of the design process.

G

gate

An integrated circuit composed of several transistors and capable of representing any primitive logic state, such as AND, OR, XOR, or NOT inversion conditions. Gates are also called digital, switching, or logic circuits.

gate array

Part of the ASIC chip. A gate array represents a certain type of gate repeated all over a VLSI-type chip. This type of logic requires the use of masks to program the connections between the blocks of gates.

gigabyte

1,073,741,824 bytes.

generics

In VHDL, generics are used to pass certain types of information into a design description from their original environment.

global buffers

Low-skew, high-speed buffers that connect to long lines. They do not map logic.

There is one BUFGP and one BUFGS in each corner of the chip. Primary buffers must be driven by an IOB. Secondary buffers can be driven by internal logic or IOBs.

global Set/Reset net

A high-speed, no-skew dedicated net, which reduces delays and routing congestion. This net accesses all flip-flops on the chip and can reinitialize all CLBs and IOBs.

global tristate net

A global tristate net forces all device outputs to high-impedance state unless boundary scan is enabled and executes an EXTEST instruction.

GND pin

Ground (0 volts).

Gray Code

A type of binary code that represents numeric values in binary digits that differ from preceding digits in one place only. For example, in Gray code the integer 7 is implemented as 0100 and the integer 8 is implemented as 1100, instead of the binary representation of 0111 and 1000, respectively.

grey box methodology

Open box methodology uses Xilinx design system (XDS) interactively for the implementation process. It is traditionally referred to as the "manual flow."

ground bounce

The occurrence of voltage spikes on the ground or power levels inside a chip primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metalization. This problem frequently occurs when multiple outputs change state simultaneously.

group

A collection of common signals to form a bus. In the case of a counter, for example, the different signals that produce the actual counter values can be combined to form an alias, or group.

guide file

A previously placed and routed NCD file that can be used in a subsequent place and route operation.

guide mode

Specifies an optional guide design file to be fed into the place and route process. The guide file is an NCD file that is used as a template for placing and routing the input design. This is useful if minor incremental changes have been made to create a new design.

GUI Based Program

A graphical program used for accessing the implementation tools.

guided design

The use of a previously implemented version of a file for design mapping, placement, and routing. Guided design allows logic to be modified or added to a design while preserving the layout and performance that have been previously achieved.

H

hard macros

Macros created by the designer in the FPGA Editor and saved as NCD files. They can be instantiated in designs to maintain the exact placement and routing defined by the designer, but lack features for simulation and back-annotation since they do not have a corresponding logical representation in the design-capture netlist.

hardwire

A non-reprogrammable device that has the same structure as a FPGA except that the memory cells and logic controlled are replaced by metal connections. This type of device is usually used after prototyping with a FPGA. It is used for high-volume designs.

HDL

Hardware Description Language. A language that describes circuits in textual code. The two most widely accepted HDLs are VHDL and Verilog.

An HDL, or hardware description language, describes designs in a technology-independent manner using a high level of abstraction. The most common HDLs in use today are Verilog and VHDL.

HDL Editor

Project Navigator's editor for ABEL and VHDL. The HDL Editor also provides a syntax checker, language templates, and access to the XABEL and XVHDL synthesis tools.

HEX

A simple text dump of the PROM data in HEX format. It has unlimited data capacity.

hexadecimal

A numbering system with a base of 16 digits (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F).

hierarchical design

A design description in multiple layers, from the highest (overview) to the lowest (circuit details). An alternative is flat design, where everything is described at the same level of detail.

high-density function block (HDFB)

A group of macrocells in an CPLD that can efficiently perform complex logic such as arithmetic operations.

high impedance

The third state or floating state of a tristate component.

hold time

The amount of time required for a data input to to be stable after the triggering edge of a clock to reliably activate the device.

I

IBUF

A circuit which acts as a protection for the chip, shielding it from eventual current overflows.

IBIS

The Input/Output Buffer Information Specification. A device modeling standard. IBIS allows for the development of behavioral models used to describe the signal behavior of device interconnects.

IBISWriter

A Xilinx command line tool which outputs an .ibs file. This file consists of a list of pins used by a design; the signals internal to the device that connect to those pins; and the IBIS buffer models for the IOBs connected to the pins.

IC

Integrated Circuit. A single piece of silicon on which thousands or millions of transistors are combined. ICs are the major building blocks of modern electronic systems.

IEEE

Institute of Electrical and Electronics Engineers. Pronounced I triple E.

iMPACT

A Xilinx command line and GUI based tool that enables you to configure your PLD designs using Boundary-Scan, Slave Serial, and Select MAP configuration modes, as well as the MultiPRO Desktop Programmer. You can use iMPACT to download, read back and verify design configuration data as well as to create PROM, SVF, STAPL, System ACE CF and System ACE MPM programming files.

impedance

The sum of all resistance and reactance of a circuit to the flow of alternating current.

implement

The second step in the synthesis flow. In this stage, the analyzed HDL is expanded into gates.

implementation

The mapping, placement and routing of a design. A phase in the design process during which the design is placed and routed.

implementation tools

Tools which implement a design (macros and logic functions) into FPGA CLB and IOB cells.

include files

CPLD equation files that are specified by an INCLUDE_EQN statement in a top-level file.

Incremental Design

A flow that allows you to run more debug cycles when making small design changes. This flow improves place and route run times while keeping performance intact in unchanged modules. The changed module is the only module that is placed and routed. The unchanged modules are guided from a previous place and route run.

indexes

The left-most and right-most bits of a bus defining the bus range and precision.

INIT pin

A device pin indicating when a device is ready to receive configuration data after power-up.

input

The symbol port through which data is sourced.

input loading

The number of specified unit loads that a specified input represents.

input pad registers and latches

D-type registers located in the I/O pad sections of the device. Input pad registers can be used instead of macrocell resources.

Install

The Xilinx installation program used to place the Xilinx software on your hard disk or system.instance

An instance is one specific gate or hierarchical element in a design or netlist. The term "symbol" often describes instances in a schematic drawing. Instances are interconnected by pins and nets. Pins are ports through which connections are made from an instance to a net. A design that is flattened to its lowest level constituents is described with primitive instances.

instance

One specific gate or hierarchical element in a design or netlist. The term "symbol" often describes instances in a schematic drawing. Instances are interconnected by pins and nets. Pins are ports through which connections are made from an instance to a net. A design that is flattened to the lowest level constituents is described using primitive instances.

instantiation

The act of placing a symbol that represents a primitive or a macro in a design or netlist.

in-system programming

A methodology in which a complex programmable logic device can be programmed (customized) after it has been soldered or plugged into the user system.

interactive

Interactive describes a process or tool that requiring interaction with the user in order to execute or accomplish its objective.

interconnect

The metal in a device that is used to implement the nets of the design.

interconnect line

Any portion of a net.

interface program

Any of the Xilinx programs used to translate a design file into a Xilinx format file, an implementation file, or a simulation file.

IOB (input/output block)

A collection or grouping of basic elements that implement the input and output functions of an FPGA device.

I/O banks

Groups of IOB blocks.

I/O blocks

The input/output logic of the device containing pin drivers, registers and latches, and 3-state control functions.

I/O pads

Input/output pads that interface the design logic with the pins of the device.

IOSTANDARD

A basic mapping constraint and synthesis constraint. Use IOSTANDARD to assign an I/O standard to an I/O primitive. All components with IOSTANDARD must follow the same placement rules (banking rules) as the SelectI/O components.

ISE

Integrated Software Environment.

iterative design

The process of using a guide file to add changed logic to a design that has already been verified for timing. It implements logic that has not been changed using the same FPGA resources as in the guide file, which ensures that the timing on those paths is identical. For logic that has been changed, it uses the normal mapping, placement, and routing process.

J

JEDEC

A CPLD file format used for downloading device bitmap information to a device programmer.

JTAG Mode

A MultiLINX configuration mode supported by the following MultiLINX devices: Virtex, Spartan, XC9500, XPLA-3, and CoolRunner-II.

K

Karnaugh map

A binary representation of the sums of products of a function. The Karnaugh map is a type of truth table from which simplified equations that define a function are derived. The simplification of such equations is called minimization.

L

label

Text attached to a bus, pin, net, or component to identify it.

latch

A two-state buffer fed by two inputs, D and L. When the L input is Low, it acts as a transparent input; in this case, the latch acts as a buffer and outputs the value input by D. When the L input is High, it ignores the D input value.

latched input

An input which captures asynchronous inputs.

LCA

Logic Cell Array.

LCA file

FPGA implementation file.

LFSR

Linear feedback shift register. A shift register with connections from some of the stages to the input of the first element through an exclusive-OR gate (standard form), or a shift register with connections from the last stage to exclusive-OR gates at the inputs of the first and intermediate stages of the register (modular form).

library

A set of macros, such as adders, buffers, and flip-flops that is part of the Xilinx interface.

.ll file

The logic allocation file, which indicates the bitstream position of storage elements such as latches, flip-flops, and IOB inputs and outputs. The Hardware Debugger uses this file to locate signal values inside a readback bitstream.

load

An input port.

loading direction

The direction in which data is stored on your PROM. In the Up direction, the data is stored in ascending order. In the Down direction, the data is stored in descending order.

locking

A lock constraint in the PCF file locks a component. A lock routing constraint specifies that the current routing cannot be changed or unrouted. A lock placement constraint specifies that placed components cannot be unplaced, moved, or deleted.

logic

One of the three major classes of ICs in most digital electronic systems: microprocessors, memory, and logic. Logic is used for data manipulation and control functions that require higher speed than a microprocessor can provide.

logic allocation file

A file used for probing that has a .ll extension. The file provides bit locations of the values of RAM, I/O, latches, and flip-flops.

logic element

A building block defining the logic in a design. These elements are typically primitives — that is, flip-flops, AND gates, and such elements — or macros, higher level combinations of primitives.

logic icon

A graphical representation of a logic resource, such as a flip-flop, buffer, or register.

logic icons in transit

Selected logic that is being moved from one location to another in the Floorplanner.

logic optimization

The process that decreases the area or increases the speed of a design.

logic simulator

Foundation's gate-level simulator provided by Aldec.

logic synthesis

A process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library containing primitives.

long line

A long line connects to a primary global net or to any secondary global net. Long lines carry signals across the length or width of the chip with minimal delay and negligible skew.

look-ahead carry

A technique used to reduce the carry propagation delay in a parallel adder. All carries are added at the same time.

look-up table (LUT)

Look-up tables (LUTs) are used to implement function generators in CLBs. Four independent inputs are provided to each of two function generators (F1-F4 and G1-G4). These function generators can implement any arbitrarily defined Boolean function of four inputs. The H function generator can implement any Boolean function of four inputs.

low

Low is a logical state for which no output is generated.

LFP file

The Logical Floorplan File is created by PACE to store grouping and color settings. You should not edit this file. PACE reads this file automatically if one exists in the same directory as the UCF file.

logical constraints

Constraints are constraints that are attached to elements in the design prior to mapping or fitting.

low skew resources

Secondary routing resources on some devices which provide signal routing with high fanout and low skew. These resources are more flexible then the global routing resources (BUFGs) since they can route any signal, not just clock signals.

LSB

Least significant bit. The left-most bit of the bus bounds or indexes. In one-hot and twos-complement encoding, the LSB is the right-most bit.

LSSD (Level-Sensitive Scan Design)

Level-sensitive scan design. A scan-path technique for systems using latches as bistables and two or more independently controllable (two-phase non-overlapping) clocks. System design must also be level-sensitive: the clock rise and fall times should not affect correct operation, and the latches must be hazard-free.

LVDS

A sink node or stopping point for a timing analysispath, the data input of a synchronous element or a pad.

M

macro

A component made of nets and primitives, flip-flops, or latches that implements high-level functions, such as adders, subtracters, and dividers. Soft macros and Relationally Placed Macros (RPMs) are types of macros.

macros

The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives. For example, the FD4 flip-flop macro is a composite of 4 FD primitives.

A macro is also a file containing a sequence of keyboard commands that are executed in script form.

macrocell

The CPLD logic cell, which is made of gates only. A macrocell can implement both combinatorial and registered equations.

magnitude comparator

A component whose function is to compare quantities of numbers.

main window

The background against which windows are displayed.

mapping

The process of assigning a design's logic elements to the specific physical elements that actually implement logic functions in a device.

masked programmed gate array

A customizable device that is programmed during the IC manufacturing process.

master-slave flip-flop

Two flip-flops activated in turn and designed to avoid metastability conditions.

maximal encoding

Maximal encoding is a type of state machine encoding that uses the minimum number of registers to encode the machine. Each register is used to its maximum capability.

MCS-86

MCS-86 is an Intel PROM format supported by the Xilinx tools. Its maximum address is 1 048 576. This format supports PROM files of up to (8 x 1 048 576) = 8 388 608 bits.

memory unit

A collection of thousands of registers for the storage of digital information.

menu bar

The area located at the top of the main window that provides access to the menus.

metastability

Metastability refers to unknown states occurring when flip-flops change states before the next input. To prevent the problem, use a master-slave flip-flop or implement the flip-flop such that it responds to only one of the clock edges, either negative or positive.

micron

One millionth of a meter.

microprocessor

A silicon chip that contains a CPU. Microprocessors control the logic of almost all digital devices, e.g. PCs, workstations, clock radios, and fuel-injection systems for automobiles

migration

1. The conversion of a design from one device to another. The device may or may not be of the same family.
2. The conversion of design data files from an older version of the Xilinx development system to a more recent version.

minimization

The process of reducing a logic function to a sum-of-products expression consisting of the least number of product terms.

mixed mode design

A design that consists of both schematic and behavioral blocks.

model registry

A list (which may include schematics, Electronic Design Data Model (EDDM) single objects, and symbols) that identifies what models can be used to describe a component.

Modular Design

This Xilinx feature allows a team of engineers to independently work on different pieces or “modules” of a design and later merge these modules into one FPGA design.

module

1. Any block or symbol.

2. A bound design element where the bounds are defined with inputs and outputs. The module represents a logical function with outputs based on the value of the inputs.
3. A Module block or primitive that is a basic library element or building block. All designs must eventually be broken down to the primitive level by the implementation tools in order to represent the implemented hardware design.

MSB

Most Significant Bit. The right-most bit of the bus bounds or indexes. In one-hot binary and twos-complement encoding, the MSB is the left-most bit.

MultiLINX

A cable designed to function as a download, read back, verification and logic probing tool for the larger Xilinx devices. MultiLINX functions as a USB device to send and receive data from host.

multicycle path

A path between two registers with a timing requirement that is a multiple of the clock period for the registers.

multiplexer

A reprogrammable routing control. This component selects one input wire as output from a selection of wires.

N

nanosecond

One billionth of a second.

NCD

A Native Circuit Description.

NCD file

A Native Circuit Description file that represents a physical circuit description of the input design as applied to a specific device.

NCF file

Netlist Constraints File. This constraints file is commonly used to define constraints for schematic editors and third-party tools.

NGC file

The NGC file is a netlist that contains both logical design data and constraints This file replaces both EDIF and NCF files.

net

1. A logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.
2. An electrical connection between components or nets. It can also be a connection from a single component. It is the same as a wire or a signal.

netlist

A text description of the circuit connectivity. It is basically a list of connectors, a list of instances, and, for each instance, a list of the signals connected to the instance terminals. In addition, the netlist contains attribute information.

net name

A name that identifies a net.

network

A collection of logic elements and the wires (nets or connections) that define how they interconnect.

NGD

A Native Generic Database file that describes the logical design reduced to Xilinx primitives.

NGDAnno

A program that distributes delays, setup and hold times, and pulse widths found in the physical NCD design file onto the logic design view represented in the NGD.

NGDBuild

A program that converts all input design netlists and then writes the results into a single merged file.

NGD2EDIF

A program that produces an EDIF 2 0 0 netlist in terms of the Xilinx primitive set. It allows you to simulate pre-route and post- route designs.

NGD2VER

A program that translates your design into a Verilog HDL file containing a netlist description of the design in terms of Xilinx simulation primitives. The Verilog file can be used to perform a back-end simulation by a Verilog simulator.

NGD2VHDL

A program that translates your design into a VITAL 95 IEEE compliant VHDL file containing a net list description of the design in terms of Xilinx simulation primitives. The VHDL file can be used to perform a back-end simulation by a VHDL simulator.

NGM

A design file produced by MAP that contains information about the logical design and information about how the logical design corresponds to the physical design.

node

The junction of nets joined throughout the design hierarchy by pins on symbols.

number of clock cycles

The number of clocks that have been applied between snapshots during synchronous mode debugging. This value is displayed between the snapshot numbers on the horizontal axis.

O

offset

Defines the timing relationship between an external clock and its associated data-in or data-out pin.

ohm

A unit of electrical resistance.

one-hot encoding

A type of encoding in which an individual state register is dedicated to only one state. Only one flip-flop can be active, or hot, at a time. The bit position represents the value. For example, in state machine language, each state is assigned its own storage register (flip-flop) and only one state can be active at a time.

one-to-one logic

In Xilinx FPGA devices, one-to-one logic is the exact correspondence between the logic specified in the design entry phase and the logic implemented in the device. For example, if you draw three inverters in your design, there are three corresponding inverters in the programmed device. This correspondence makes back-annotation of timing delays very straightforward and ensures that there are no differences between your original design and the finished device.

open box methodology

Open box methodology uses Xilinx design system (XDS) interactively for the implementation process. It is traditionally referred to as the "manual flow."

optimization

The process that decreases the area or increases the speed of a design.

optimizer

A program which performs logic optimization.

options

Features that modify the way a program runs. Options are generally set by the user.

oscillator

A bi-stable circuit that can be used as a clock. The stable states are 0 and 1.

overflow

An indication that a value cannot be represented in a given number of bits. It is a signal that can be translated as an error or ignored. In a design, this error can be interpreted as a signal.

OVI

Open Verilog International. A non-profit organization that exists to promote, maintain, and support the use of Verilog HDL worldwide. OVI supports the IEEE 1364 standard for Verilog HDL.

P

PACE

Pinout Area Constraints Editor. A GUI tool that defines legal pin assignments and creates properly sized area constraints.

package

The physical packaging of a chip, for example, PG84, VQ100, and PC48.

pad

The physical bonding pad on an integrated circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an integrated circuit package.

pad-to-pad path (P2P)

A path which starts at an input of the chip and ends at an output of the chip. The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal.

pad-to-setup path (P2S)

A path which starts at an input of the chip and ends at an input to a flip-flop, latch, or RAM—wherever there is a setup time against a control signal. The pad-to-setup path time is the maximum time required for the data to enter the chip, travel through logic and routing, and arrive at the output before the clock or control signal arrives.

PAL

A programmable logic device that consists of a programmable AND matrix whose outputs drive fixed OR gates. This was one of the earliest forms of programmable logic. PALs can typically implement small functions easily (up to a hundred gates) and run very fast, but they are inefficient for large functions.

PAR

Place and route tool. PAR is a program for mapping, placing, and routing an FPGA design. The process is called design implementation.

parallel adder

An adder implementation in which the bits are added simultaneously. The carries of the parallel adders are connected, thus generating the sum simultaneously.

Parallel Cable III

A cable assembly which contains a buffer to protect your PCs parallel port and a set of headers to connect to your target system.

parameterized modules

LogiBLOX symbols in which the user can set the values of one or more inputs, such as the input bit width or whether to create RPMs.

PARTGen

A command which displays various levels of information about installed Xilinx devices and families depending on which options are selected.

Partial Reconfigurability

A form of Modular Design used for generating designs that can be actively reconfigured on a device while it is running. See Xilinx application note 290.

partitioning

1. The process of splitting a single design among multiple devices.
2. The maximum level of integration (density concern).

path

A connected series of nets and logic elements. A path has a start point and an end point that are different depending on the type of path. The time taken for a signal to propagate through a path is referred to as the path delay.

path delay

The time it takes for a signal to propagate through a path.

PCF files

Physical Constraints File. This file contains the physical constraints that are derived from the logical constraints after mapping. Any changes in constraints in the FPGA Editor are also written to the PCF.

period

A clock period specification checks timing between all synchronous elements within the clock domain as defined in the destination element group. The group may contain paths that pass between clock domains if the clocks are defined as a function of one or the other.

The period specification is attached to the clock net.

physical constraints

Constraints that are attached to design elements in the physical design, that is, the design after mapping has been performed. These constraints are defined in the Physical Constraints File (PCF), which is created during mapping.

PIM

Physically Implemented Module. A term used in modular design that refers to the individual modules that have been completed and are ready to be incorporated into the top-level design.

pin

A symbol pin or a package pin. A package pin is a physical connector on an integrated circuit package that carries signals into and out of an integrated circuit. A symbol pin, also referred to as an instance pin, is the connection point of an instance to a net.

pin feedback

Pin feedback specifies that the associated signal comes from the actual device pin and not from the universal interconnect matrix (UIM).

PIN2UCF

A Xilinx program that generates pin-locking constraints in a UCF file by reading a placed NCD file for FPGAs or GYD file for CPLDs. PIN2UCF writes its output to an existing UCF file. If there is no existing UCF file, PIN2UCF creates a new file.

PIP

Programmable interconnect points. The circuits which provide the routing paths used to connect the inputs and outputs of IOBs and CLBs into logic networks.

A PIP is made of a CMOS transistor, which you can turn on and off to activate the PIP.

placer

A utility that maps logic from your design into specific locations in the target FPGA chip.

placer effort

The user-controlled parameter that balances run-time with placement efficiency.

placing

The process of assigning physical device cell locations to the logic in a design.

PLD

Programmable Logic Device. An integrated circuit composed of two types of gate arrays: the AND array and the OR array, thus providing for sum of products algorithmic representations. PLDs include three distinct types of chips: PROMs, PALs, and PLAs. The most flexible device is the PLA (programmable logic array) in which both the AND and OR gate arrays are programmable. In the PROM device, only the OR gate array is programmable. In the PAL device, only the AND gate array is programmable. PLDs are programmed by blowing the fuses along the paths that must be disconnected.

FPGAs and CPLDs are classes of PLDs.

PLUSASM

A Xilinx-proprietary Boolean equation language for expressing behavioral designs mapped to Xilinx CPLDs.

polarity

1. The direction of the current flow from the negative pole to the positive pole.
2. The negative or positive expression of an equation. Negative expressions are prefaced with a slash (/). Polarity affects minimization.

port

A logical connector that associates signals across hierarchical boundaries. Port location refers to a package pin on the IC.

post-synthesis simulation

Simulation which is usually done after the HDL code has been expanded into gates. Post-synthesis simulation is similar to behavioral simualtion since design behavior is being checked. The difference is that in post-synthesis simulation the synthesis tool's results are being checked. If post-synthesis and behavioral simulation match, then the HDL synthesis tool has interpreted the HDL code correctly.

primitives

The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms". Macros can be created from the primitives. Xilinx examples of primitives are the simple buffer, BUF, and the D flip-flop, FD.

probing

The process of examining the states of a device.

process

A running concurrent block of logic.

The difference between hardware and software programming lies in the fact that hardware programming is for concurrent processes and software programming is for linear processes.

process technology

The procedure used to convert blank silicon wafers into finished wafers containing hundreds to thousands of chips. These chips are tested and assembled into plastic or ceramic packages before final use.

product of sums

The complement expression of a sum of products. Specifically, the outputs of a function for which the input combinations equal 0.

product term cascading

The process of passing groups of four product terms from one macrocell to another for the purpose of increasing the number of usable product terms.

programmable interconnect points (PIP)

Programmable interconnect points (PIP). The circuits which provide the routing paths used to connect the inputs and outputs of IOBs and CLBs into logic networks.

A PIP is made of a CMOS transistor, which you can turn on and off to activate the PIP.

programmer

A hardware box and its associated software that is used to program either the FPGA/CPLD devices themselves or the memory devices that will be used to store programming data.

programming

The process of configuring the programmable interconnect in the FPGA.

Project Navigator

The main window for ISE. All of the GUI design tools for ISE are accessed through the Project Navigator.

PROM

A programmable read-only memory.

PROM file

One or more BIT files (bitstreams) formed into one or more datastreams. The file is formatted in one of three industry-standard formats: Intel MCS86 HEX, Tektronics TEKHEX, or Motorola EXORmacs. The PROM file includes headers that specify the length of the bitstreams as well as all the framing and control information necessary to configure the FPGAs. It can be used to program one or more devices.

PROMGen

A program which formats a BitGen-generated configuration bitstream (BIT) file into a PROM format file.

propagation

The transmission of signal from one point in a design to other points.

Constraint propagation refers to all of the design elements and nets that apply to a specified constraint in a design.

prototyping

1. The first full-scale functional model of a new device.
2. The use of a model prior to the generation of a final version of a chip.

pull-down resistor

A device or circuit used to reduce the output impedance of a device, often a resistor network that holds a device or circuit output at or less than the zero input level of a subsequent digital device in a system.

pull-up resistor

A device or method used to keep the output voltage of a device at a high level, often a resistor network connected to a positive supply voltage.

pseudo logic

Logic that is temporarily inserted in a design to facilitate the relative placement of the connected logic within a module. Pseudo logic is used when performing modular design.

Q

R

race check

An analysis that compares the time it takes for data to propagate from a source register to a destination register with the amount of skew on the clock lines driving each register. A race condition exists if the clock skew is greater than the propagation time plus the hold time.

radix

The base—usually binary, octal, decimal, or hexadecimal— in which waveforms are displayed in a waveform viewer.

RAM

Random Access Memory. A read and write memory that has an access time independent of the physical location of the data.

RAM-based FPGA

An FPGA whose configuration data is programmed into random access memory. These devices are re-programmable.

ratsnest

A diagram consisting of lines that indicate connectivity between logic placed in the Floorplanner window.

RBT file

A raw BIT format file. The ASCII version of the BIT file.

readback

The process of reading the logic downloaded to an FPGA device back to the source. There are two types of readback.

1. A readback of logic usually accompanied by a comparison check to verify that the design was downloaded in its entirety.

2. A readback of the states stored in the device memory elements to ensure that the device is behaving as expected.

register

A set of flip-flops used to store data. It is an accumulator used for all arithmetic operations.

registers

Digital circuits that store bits (1s and 0s).

Relationally Placed Macros

Any "soft macro" that contains one or more RLOC constraints to specify relative placement. It can be as simple as "make sure these two flip-flops get placed in the same slice", to a full-blown specification of the relative placement every LUT, MUX, and flip-flop.

Relative Mins

Relative Minimum Delays. The minimum delay value(s) when operating at specified operation conditions (temperature and voltage).

resistance

1. The property — based on material, dimensions, and temperature of conductors — that determines the amount of current produced at a given difference in potential. A material's current impedance that dissipates power in the form of heat.
2. The drive of the output pins on a network.

resistor

A device that provides electical resistance.

resource graphics

Graphical representations of elements in the target FPGA Floorplan window, such as function generators, registers, and tristate buffers in the CLB and IOBs.

ripple counter

A series connection of complementing flip-flops. Ripple counters are also called asynchronous counters.

Rocket IO transceiver

A multi-gigabit serial transceiver that is integrated into the Virtex-II Pro device.

ROM

Read Only Memory. A static memory structure that retains a state indefinitely, even when the power is turned off. It can be part of a function generator.

router

The utility that connects all appropriate pins to create the design's nets.

router effort

Router effort refers to the user-controlled parameter that balances run-time with routing efficiency.

routing

Routing is the process of assigning logical nets to physical wire segments in the FPGA that interconnect logic cells.

routing layer

A routing layer is a conductive layer used for interconnections.

RPM

A Relationally Placed Macro (RPM) defines the spatial relationship of the primitives that constitute its logic. An indivisible block of logic elements that are placed as a unit into a design.

RS-232 Port

The RS-232 Port is where the MultiLINX cable connects to on the host computer. This is how the MultiLINX cable hardware communicates with the host.

RTL

Resistor Transistor Logic

S

scan test

A synchronized procedure for testing CLB and IOB blocks.

schematic

A hierarchical drawing representing a design in terms of user and library components.

script

A series of commands that automatically execute a complex operation such as the steps in a design flow.

SDF (standard delay format)

An industry-standard file format for specifying timing information. It is usually used for simulation.

seed

A random number that determines the order of the cells in the design to be placed.

seed-place

The act of initial placement with a seed.

selecting logic

In the Floorplanner, the process of using the mouse to choose logic in either the Design window or the Floorplan window for placement, movement, or processing.

SelectMAP Mode

A MultiLINX configuration mode supported by the MultiLINX device, Virtex.

semiconductor

A generic name for devices like transistors and integrated circuits that can control the flow of electrical signals. Silicon is the basic material of most semiconductors.

sequential logic

Digital circuits whose logic states depend on clocked sequences.

serial PROM

A PROM that is read one bit at a time.

set/reset

This operation is made possible by the asynchronous set/reset property. This function is also implemented by the Global Reset STARTUP primitive.

setup time

The amount of time required for a data input to be stable prior to the triggering edge of a clock device.

sheet

A page of a schematic.

shift register

A register in which data is loaded in parallel and shifted out of the register again. It refers to a chain of flip-flops connected in cascade.

signal

A wire or a net.

signal aliasing

The name of a net used to refer to all equivalent nets in a design. Signal aliasing is the process of assigning the name of a bus to a lesser bus or signal contained in the larger bus.

signal binding

The process of joining nets from a lower-level XNF file to pins in a top-level XNF file.

silicon wafer

A thin disk of extremely pure, crystalline silicon, typically six or eight inches in diameter.

simulation

The process of verifying the logic and timing of a design.

simulation network

A file submitted to the simulator for functional or timing simulation.

simultaneously switching outputs (SSO)

The occurrence of voltage spikes on the ground or power levels inside a chip primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metalization. This problem frequently occurs when multiple outputs change state simultaneously.

single-length line

A line which is switched at every switch matrix it crosses.

slack

The difference between the constraint and the analyzed value, with negative slack indicating an error condition.

skew

Clock delay.

slew

Transition time of an output signal. A fast slew rate has a quicker transition time and a slow rate a longer one. Limiting the slew rate reduces output switching surges in a device. Slew rate can be set to FAST or SLOW.

Slave Serial Mode

A MultiLINX configuration mode supported by the following MultiLINX devices: Virtex, Spartan, XCS5200, and XC3000.

slew rate

The speed with which the output voltage level transitions from high to low or vice-versa. The slew rate determines how fast the transistors on the outputs change states.

slice

Two slices form a CLB within Virtex and Spartan-II families. This is a specific example of a comp type that corresponds to the basic fabric of logic in all FPGAs.

soft macros

Library design element "macros" that are built hierachically from simpler library elements (for example, a counter built from flip-flops and gates). These are "soft" in the sense the tools are free to remap, place and route them as they see fit. Designers can also build "soft" macros, with or without RLOC constraints to specify relative placement. The tools are free to manipulate the mapping, placement and routing, within the boundaries of the specified constraints. It is possible to so completely constrain a "soft" macro with RLOCs, that every placement is specified and there is nothing left for the tools to decide, but since it still has a logical representation in the design capture, it is still considered "soft".

source

An output port.

source

An output pin that drives a path. Sources are input pads and the outputs of synchronous elements.

speed

Speed is a function of net types, CLB density, switching matrices, and architecture.

SPEEDPRINT

A command which lists block delays for a device's speed grade. This program supplements data sheets, but does not replace them.

speeds file

A Xilinx Design System (XDS) data file that contains information defining the timing for each speed grade available for a device.

SRAM

Static Random Access Memory or volatile memory. SRAM holds a value as long as power is continually supplied. It loses its contents when the power is turned off.

standard encoding

A type of state machine encoding that forms clusters of states and uses binary encoding for each cluster. One-hot encoding is a special case of standard encoding in which each cluster contains exactly one state. Binary encoding is a special case in which all states belong to a single cluster.

STARTUP symbol

A symbol used to set/reset all CLB and IOB flip-flops.

state

The set of values stored in the memory elements of a device (flip-flops, RAMs, CLB outputs, and IOBs) that represent the state of that device at a particular point of the readback cycle. To each state there corresponds a specific set of logical values.

state diagram

A pictorial description of the outputs and required inputs for each state transition as well as the sequencing between states. Each circle in a state diagram contains the name of a state. Arrows to and from the circles show the transitions between states and the input conditions that cause state transitions. These conditions are written next to each arrow.

state machine

A set of combinatorial and sequential logic elements arranged to operate in a predefined sequence in response to specified inputs. The hardware implementation of a state machine design is a set of storage registers (flip-flops) and combinatorial logic, or gates. The storage registers store the current state, and the logic network performs the operations to determine the next state.

state table

A table which shows the value of the outputs for all combinations of current states and inputs. It also defines the next state for each set of inputs.

static timing analysis

A point-to-point delay analysis of a design network withrespect to a given set of constraints. It does not include insertion of stimulus vectors.

This method used by the Interactive Timing Analyzer tool produces detailed timing constraint, clock, and path analysis for post-map or post-place-and-route implementations.

static timing analyzer

A tool that analyzes the timing of the design on the basis of its paths.

status bar

An area located at the bottom of a tool window that provides information about the commands that you are about to select or that are being processed.

step

The length of time that each value in a clock pattern is simulated.

step size

The length in nanoseconds of one step of a clock pattern.

stimulus information

The information defined at the schematic level and representing a list of nodes and vectors to be simulated in functional and timing simulation.

submicron technology process

A generic name for modern IC manufacturing methods where dimensions on the wafer can be controlled to tolerances well below one micron, which is one millionth of a meter.

sum of products

The outputs of a function for which the input combinations equal 1.

switch matrix

A collection of transistors located between CLB blocks that enables the connection of two interconnect lines. PAR uses the switch matrices and interconnects to connect CLB inputs and outputs. Switch matrices reduce some of the net delay. They have three possible directions: top, bottom, and left.

symbol

A graphical representation of one level of hierarchy.

symbolic state machine

A state machine that makes no reference to the actual values stored in the state register for the different states in the state table. The software determines what these values should be. All that is defined in a symbolic state machine is the relationship among the states in terms of how input signals affect transitions between them, the values of the outputs during each state, and in some cases, the initial state.

synchronous clock

Synchronous control in which flip-flops are set or reset on the rising edge of the clock. In LogiBLOX, the SYNC_VAL attribute value constant is loaded into the register if the SYNC_CTRL input on the module is High during the rising edge of the clock enable.

synchronous debug

A debug mode in which you use the XChecker cable to have full control of the clock.

Synopsys

Synopsys supports HDL, a behavioral language for entering equations. HDL also enables you to include LogiBLOX schematic components in a design.

synthesis

A process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library containing primitives.

synthesis package

A fixed library of cells, each cell containing the implementation details in terms of primitive logic.

T

Tcl

An acronym for Tool Command Language (Tcl), which is a scripting language used for rapid prototyping, scripted applications, graphical user interfaces, and testing. Tcl was created by John Ousterhout. A Tcl file has a .tcl extension.

TDO

An ASCII text file generated by Altera compilers. TDO files can be converted to ABEL using the TDO to ABEL convertor prcess found in the Design Entry Utilities in the Project Navigator.

TEKHEX

A Tektronix PROM format supported by Xilinx. Its maximum address is 65 536. This format supports PROM files of up to (8 x 65 536) = 524 288 bits.

testbench

An HDL netlist containing test vectors to drive a simulation.

three-state

Tristate buffer. A buffer that places an output signal in a high-impedance state to prevent it from contending with another output signal.

threshold

The crossover point when something occurs or is observed or indicated. The CMOS threshold and TTL threshold are examples.

time group

A collection of design elements, including nets, BELs, components, and so forth that can be used to constrain many objects in the same way.

time process

A process which takes the routed nets in the design and calculates the delays associated with each.

timespecs

Commands (which can be specified in a HDL flow or in an external file) that specify the timing requirements of a design to the place and route software.

timing

The process that calculates the delays associated with each of the routed nets in the design.

timing constraints

A series of constraints applied to a given set of paths or nets that dictate the desired performance of a design. Constraints may be period, frequency, net skew, maximum delay between end points, or maximum net delay.

timing simulation

Simulation that takes place after the HDL design has been synthesized and placed and routed. The purpose of this simulation is to check the dynamic timing behavior of the HDL design in the target technology.

Use the block and routing delay information from the routed design to assess the circuit behavior under worst-case conditions.

timing specification

Specifications which define the maximum allowable delay on any given set of paths in a design. Timing specifications are entered on the schematic.

TNM

The Timing attribute part of TIMESPEC and specification.

toolbar

A field located under the menu bar at the top of a tool window. It contains a series of icons that you click on to execute some of the most

commonly used commands. These icons are an alternative to the menu commands.

top-down design

An HDL methodology where overall design behavior is defined first and then HDL blocks. It is a process that starts a design with the highest level of abstraction and gradually designs underlying blocks until the complete design is implemented in the target technology. Top-down design is often technology-independent at the highest levels of design abstraction.

top-level file

The main file of a PLUSASM design. It contains design control information. It also contains either design equations or references to include files containing design equations.

TRACE

The Timing Reporter And Circuit Evaluator. A command line utility for performing static timing analysis of a design based on input timing constraints. Its two major functions are timing verification and reporting.

trace information

A list of nodes and vectors to be simulated in functional and timing simulation. This information is defined at the schematic level.

transceiver

A transmitter and receiver of signals. Xilinx uses the Rocket I/O transceiver in its Virtex-II Pro and Virtex-II Pro X devices.

transistor

A three-terminal semiconductor device that switches or amplifies electrical current. It acts like a switch: On is equal to 1, and Off is equal to 0.

translation tools

Programs that create Xilinx format files. For example, EDIF2NGD translates CAE designs into NGD format files.

trimming

The process of removing unconnected or unused logic.

tristate

Tristate buffer. A buffer that places an output signal in a high-impedance state to prevent it from contending with another output signal.

tristate condition

A high-impedance state. A tristate can act also as a normal output; i.e. it can be on, off, or not connected.

truth table

A table which defines the behavior for a block of digital logic. Each line of a truth table lists the input signal values and the resulting output value.

TTL

Transistor-Transistor Logic. A technology with specific interchange (communication of digital signals) voltages and currents. Other technologies include ECL, MOS, and CMOS. These types of logic are used as criteria to classify digital integrated circuits.

TTY

A textual command line interface.

U

UCF

The user constraints file (UCF) is an ASCII file specifying constraints on the logical design. These constraints affect how the logical design is implemented in the target device. You can use the file to override constraints specified during design entry.

UIM

Universal Interconnect Matrix. The routing matrix for CPLD devices. This fully populated switching matrix allows any output to be routed to any input, guaranteeing 100% routability of all designs. The UIM can also function as a very wide AND gate, which can allow more logic to be placed in macrocells.

UIM feedback

UIM feedback specifies that the associated signal comes from the macrocell and not from the device pin.

UIM_AND function

An AND gate created from the inherent wired-AND structure of the UIM. It requires no macrocell resources.

unbonded

An IOB used for internal logic only. This element does not have an external package pin.

Unified Libraries

A set of logic macros and functions that are used to define the logic of a design. The elements are compatible across families and schematic and HDL editors.

unit load

A measure of impedance presented to an input or output under specified conditions.

USB Port

Universal Serial Bus Port is where the MultiLINX cable connects to on the host computer.

The part on the computer to which you can connect a MultiLINX Cable.

V

VCC pin

The Power Pin. It is the supply voltage.

vector

1. The logical state of a set of nodes within a circuit as a function of time.
2. A group of signals that has been renamed for convenience during simulation. It is similar to a bus. “Bus” refers to a group of signals on the schematic, and “vector” refers to a group of signals during simulation.

verification

The process of reading back the configuration data of a device and comparing it to the original design to ensure that all of the design was correctly received by the device.

Verilog

A commonly used Hardware Description Language (HDL) that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level. It is IEEE standard 1364-1995. Verilog was originally developed by Cadence Design Systems and is now maintained by OVI.

A Verilog file has a .v extension.

VHDL

A VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits). A hardware description language which can be used to describe the concurrent and sequential behavior of a digital system at many levels of abstraction ranging from

the algorithmic level to the gate level. VHDL is IEEE standard 1076-1993.

A VHDL file has a .vhd or .vhdl extension.

VHSIC

Very High Speed Integrated Circuit.

VITAL

A VHDL Intitiative Toward ASIC Libraries. A VHDL-library standard (IEEE 1076.4) that defines standard constructs for simulation modeling, accelerating, and improving the performance of VHDL simulators.

VMH file

A file containing a fitted CPLD design.

volt

Unit of electrical potential, potential difference, or electronic force.

voltage

The potential difference between two points in an electrical circuit.

W

watch list

A list of nodes whose values are to be reported during simulation.

waveform

A graphical representation of a set of simulation transitions that depicts the digital or electrical values of a node.

wide decoder

A wired AND gate.

wire

A net or a signal.

wire segment

A metal interconnect track that is physically located on the surface of the chip. Typically connections between two cells uses multiple wire segments that are connected together to form an electrical connection.

wired-AND functions

AND gates and their DeMorgan equivalents produced by the inherent structure of the UIM.

wired-AND gate

A symbol, as opposed to a physical gate, representing a function generated from a wired connection of two NAND gates, for example.

wired logic

A wire connection between two gate outputs and providing a specific logic function.

wireload

The maximum number of specified unit loads that a specified output can drive.

X

XABEL

A Xilinx-specific version of the ABEL design entry software.

XCF

The XCF (Xilinx Constraints File) syntax allows you to specify a specific constraint for the entire device (globally) or for specific modules in your design. The syntax is basically the same as the UCF syntax for applying constraints to nets or instances, but with an extension to the syntax to allow constraints to be applied to specific levels of hierarchy. The keyword MODEL defines the entity or module that the constraint will be applied to. If a constraint is applied to an entity or module the constraint will be applied to the each instance of the entity or module.

XFLOW

A Xilinx command line tool that automates the Xilinx implementation and simulation flows. XFLOW reads a design file as input as well as a flow file and option files.

Xilinx ABEL

Advanced Boolean Expression Lanaguage (ABEL) is a hardware description language (HDL) and compilation system owned and maintained by XILINX. Industry Standard Language (HDL Tool).

XSI

Xilinx Synopsys Interface. A design tool kit.

XST

Xilinx Synthesis Technology. A Xilinx tool that synthesizes HDL designs to create Xilinx specific netlist files called NGC files. The NGC file is a netlist that contains both logical design data and constraints that replaces both EDIF and NCF files.

XST Command Line

With XST, you can run synthesis in command line mode instead of from the Process window in the Project Navigator. To run synthesis from the command line, you must use the executable file. If you work on a workstation, the name of the executable is "xst".

On a PC, the name of the executable is "xst.exe"

Y

yield

The yield is the percentage of defect-free (usable) die on a silicon wafer.

Z