Examination Feedback for EEE310/6036 – (Introduction to) VLSI Design
Spring Semester 2007-08

Feedback for EEE310/6036 Session:2007-2008

General Comments:

There was a fair amount of bookwork in this paper and so it was disappointing that people appeared not to have mastered the material. Marks suffered as a consequence of this. I believed it to be a relatively straightforward paper – except for question 2: with which I expected people to be less familiar. However, this was the question that people seemed to find the most straightforward!

Question 1:

This question was really quite badly attempted – despite there being a lot of bookwork in the question.
Part a) was done reasonably although some people did not bother to draw a diagram of a FET (or mislabelled it) and did not define when the FET operated ohmically.
In part b) what I was really looking for (along with the condition that gives rise to saturation) was pinch off and how, for a large enough drain voltage, there would not be sufficient voltage across the gate insulator to support inversion.
Nobody did part c) properly. I find this difficult to comprehend because I *actually* gave out a handout that had the proof on it. The attempts that people made showed a flawed understanding of simple conventions about voltages and currents – this is electronics 101!

Question 2:

Conversely, this question was very well done. A few people did not read the question properly where it said *without changing the way in which the existing transistors are connected*. This means, for example, that you cannot add an extra transistor between the drain of the p-FET controlled by D and the Y output.

Question 3:

A lot of the descriptions for the design flow in part a) were relatively basic and a few were just plain wrong – missing out entire sections of the design flow. In part b) the descriptions of the differences between the separate technologies were sometimes quite confused and identification of the relevant points was somewhat limited. The main problem with this question was in part c): some people merely restated the same points from part b). What was really required was the relationship between the problem in hand i.e. a multi-functional PDA and what particular constraints this placed on the design process.

Question 4:

Some people misinterpreted this question as being about testing: it was not – it was about clocking. Consequently, answers to part b) talked about defects, etc. when all that was being asked for was PVT – process, voltage, and temperature. Similarly, when asking about clock domains some people never mentioned metastability! The last part of the question was simply asking for metastable-resistant samplers but, instead, a number of answers were concerned with non-overlapping clock generators. How does this answer the question?