Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2010-2011 (2 hours)

Integrated Circuit Technology

Answer **THREE** questions. **No marks will be awarded for a solution to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

1. a. Explain with the aid of a diagram the difference between a metal, semiconductor and an insulator. Describe an experimental method to differentiate between a metal and a semiconductor. What is a semi-metal ? **(3)**

b Explain, with the help of a diagram and a formula how you would measure the resistivity of a material. **(3)**

c Name the crystal lattice system for silicon. Derive the packing density, assuming that the atom at the tetrahedral site (completely inside a unit lattice) is at a distance of ¼ along the lattice diagonal. **(6)**

d Draw diagrams for the (111), (100) and the (110) planes in silicon. What is the notation for describing a "family" of planes ? **(2)**

e Name any two types of dislocations. What is the burgers vector for the most common dislocations found in the diamond cubic lattice ? **(3)**

f Name (in Hexagonal Close Packed format) and show diagrammatically the two types of faults in a crystal. **(3)**

2. a. Describe the main differences between (1) MOCVD and (ii) MBE techniques for epitaxial growth. Show diagrammatically the MOCVD growth characteristics with time and the factors controlling each regime. **(5)**

b Name two modifications of the basic Czochralski technique required for growth of GaAs ingots ? Explain the reasons for these modifications. **(4)**

c Explain what is meant by autodoping. What is the condition to minimise autodoping ? **(2)**

d An amorphous layer 3×10^{-5} cm thick is produced in (001) Si by Si^{+} ion implantation. How long will the epitaxial regrowth of this layer take at 580ºC. (Assume that the activation energy for the regrowth process is 2.76eV, the preexponential factor (v_0) is 3.68×10^{8} cm/s and Boltzmann's constant (k) is 8.617×10^{-5} eV/K.) **(6)**

e Explain the key aspects of the growth process in MBE such as factors affecting **(3)**

the quality and growth rate

3. **a.** Starting from a basic p-type substrate, show diagrammatically the most important steps in a CMOS process (ie adjacent p and n MOS devices). **(10)**

b Transition element impurities are detected in a batch of wafers after epitaxial layer growth. Describe how the unwanted impurities may be removed from device regions by the process of external gettering ? **(3)**

c Describe the key reactions (with equations) for wet and dry oxidation. Describe the reaction kinetics in an oxidation process. **(5)**

d Name two methods currently used in industry to boost the channel mobility. **(2)**

4. **a** Explain the main differences between wet and dry chemical etching in terms of process and characteristics. Give an example of where each is most suitable? **(6)**

b What is meant by a pseudomorphic layer ? Explain what happens if the grown layer is under (i) tension or (ii) compression, if the lattice mismatch is > 1.5% **(4)**

c A stage in the fabrication of a particular transistor requires the formation of an n-type tub in an initial p-type wafer. An implant of As^{+} is first carried out using 12 keV ions to give a shallow As-containing layer. The impurity is then driven in by a 30min anneal at 1150°C. Calculate the characteristic diffusion length of the impurity as a result of this anneal. The diffusion pre-exponential factor (D_0) may be taken to be $12cm^2$/sec, with an activation energy for diffusion of 4.05eV: Boltzmann's constant (k) is 8.61×10^{-5} eV/K. **(6)**

d Between CMOS and bipolar, in general, which technology consumes more power ? What are the factors which affect yield ? Name a critical issue facing future 22 nm CMOS technology. **(4)**