Data Provided: None

The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2005-2006 (2 hours)

Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. A simplified layout for a standard cell library component is shown in Figure 1.

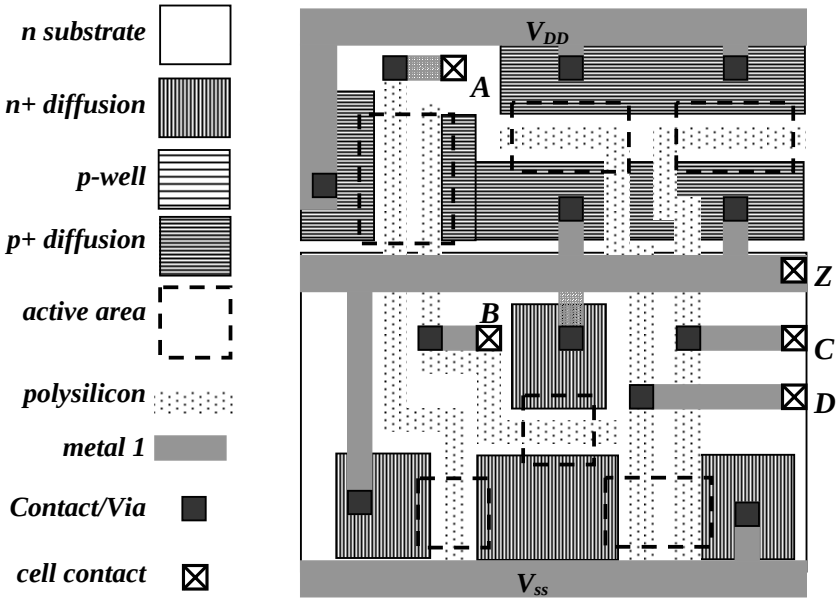

Figure 1: Cell Layout

From the layout:

i. Draw the corresponding transistor circuit; **(10)**

ii. Determine the logical function, *Z*, of the component. **(4)**

b. What is the significance of the active area, defined in Figure 1, and how is it formed. **(3)**

c. In the cell layout in Figure 1, V_{SS} is shown running along the bottom of the cell, and V_{DD} is shown running along the top of the cell. Why is this the case and what does it allow? **(3)**

2. **a.** Show how a CMOS, edge-triggered, master-slave flip flop might be constructed from transistors (your answer should include a schematic diagram). Ensure that you identify any important requirements for the clock **(4)**

b. **i.** How might a two-phase clock generator – with non-overlapping phases – be designed? **(4)**

ii. How can the amount of *underlap* be controlled? **(2)**

iii. Outline how the clock generator can be designed to drive a large capacitive load (you do not have to do a detailed analysis in this part of the question). **(3)**

c. **i.** State the expression for *upsets/second* as a consequence of metastability where a data signal with an effective frequency of f_{data} is sampled in a flip-flop being clocked at a frequency of f_{clk}. Please ensure that you explain what the terms in the equation are and how they arise. **(3)**

ii. It is calculated that each flip-flop, within an 8-bit register, sampling data from a data bus input, where f_{data}=25kHz and f_{clk} = 100kHz, will experience one upset every 10 minutes. Provide an analysis to find how often the 8-bit value read from the data bus will be upset and calculate this value (if you have to introduce an approximation to calculate the result then ensure that you identify what you have done). **(4)**

3. **a.** Identify the two conditions that must be met in the *pull-up* and *pull-down* networks in a standard CMOS logic circuit, for all combinations of inputs. **(4)**

b. For the *pull-down* network in **Figure 3** find:

i. The corresponding *pull-up* network. **(4)**

ii. The function, *Y*. **(4)**

iii. How would the function change if the points labelled *p* and *q* are connected? **(4)**

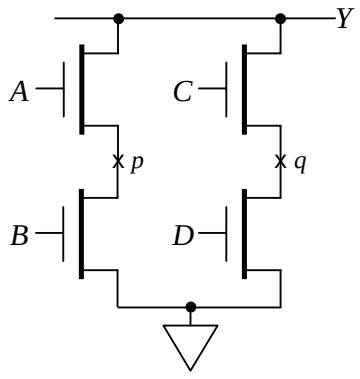

Figure 3: *Pull-Down* Network

c. What is the body effect and what limitation does it introduce for CMOS circuits? **(4)**

4. **a.** Identify the various *basic* steps or stages in an ASIC design-flow, showing how the various steps might be connected **(6)**

b. An IC design house sees a gap in the market for product that requires a digital ASIC to be designed. Initial analysis suggests that the IC will be approximately 500,000 gate equivalents and will need to run at a clock frequency of 50MHz. Market analysis suggests that the product can be sold for £600 once the market is developed and that, from this, the budget for the IC is £30-40. At this early stage, it is not possible to be sure how big the market will be but it *could* be 100,000 units per year. Furthermore, it is known that a competitor has also, possibly, seen this opportunity.

How might the development of the ASIC be undertaken? Ensure that you identify which type of implementation(s) might be chosen: when and why. **(14)**

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