EEE 163
System Design Analysis

Lecture 4
Electronics Packaging

Reasons for packaging

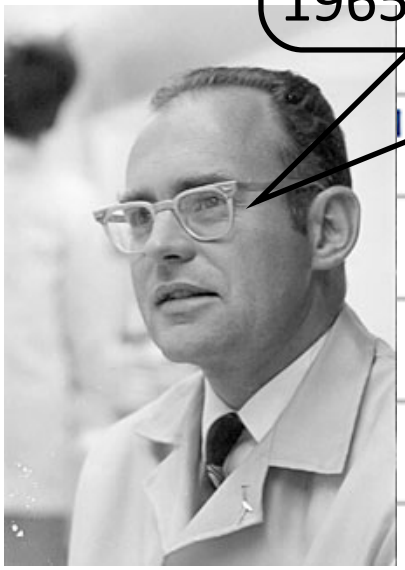
"Electronics packaging is often the critical limiting factor in the success of modern electronic systems"

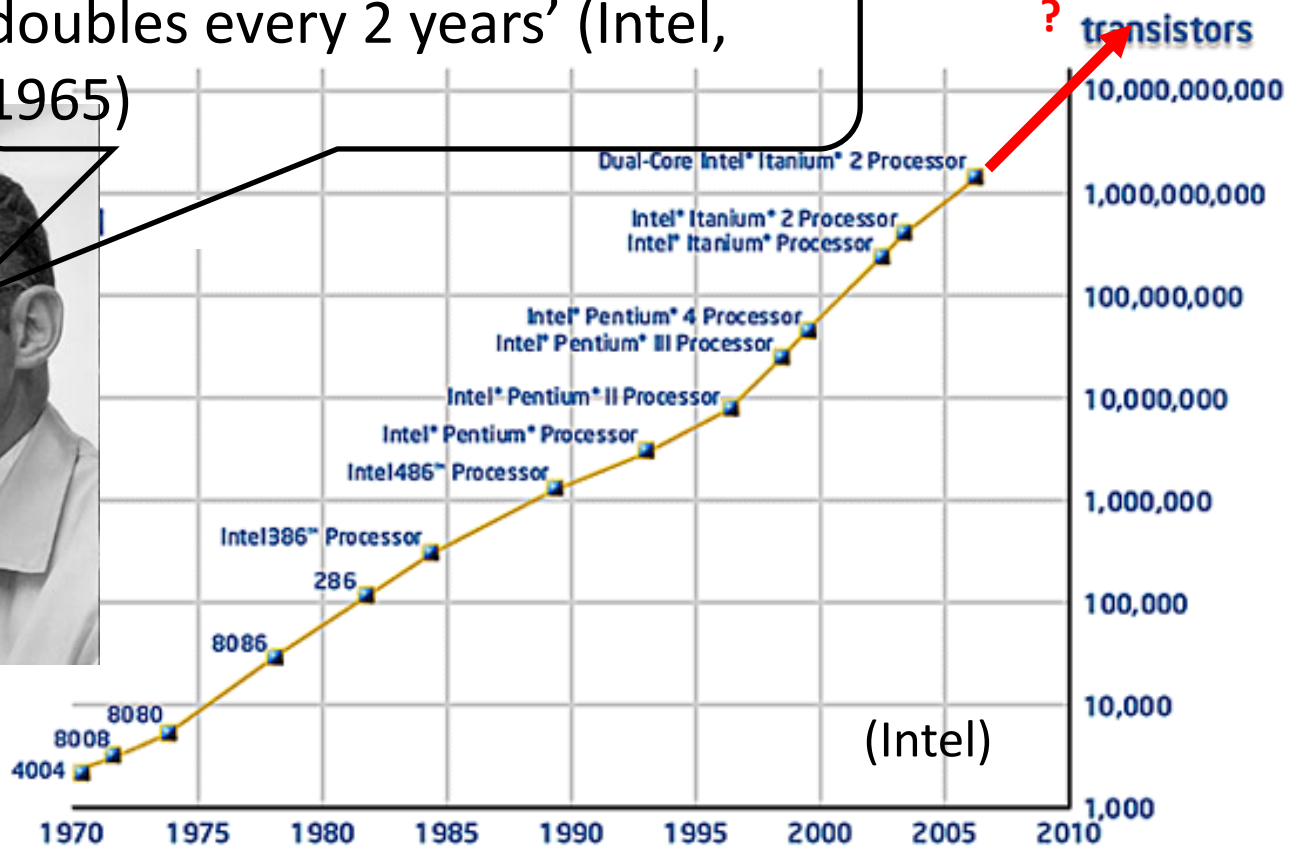
(Harper)

- Input/output from ICs
- Interconnection between ICs
- Input/output to user and other electronic systems
- Mechanical stability
- Thermal stability
- Environmental protection

George Moore's 'Law'

'Number of transistor on chip doubles every 2 years' (Intel, 1965)





If same rate of progress applied to air travel, then:
London-New York would cost 1p and take 1 second!

‘Level 1’ : Chip package

Connections to IC bond pads

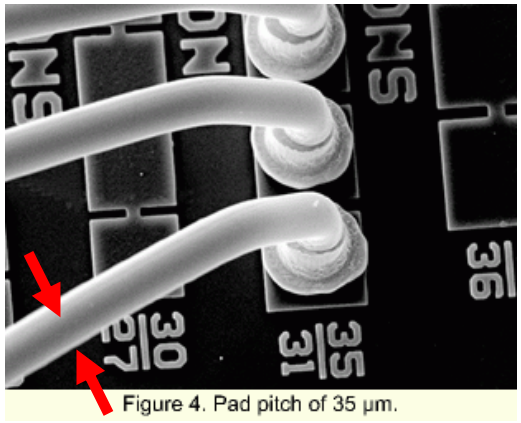
- Wire bonding
- Tape automated bonding
- Solder balls

Package types

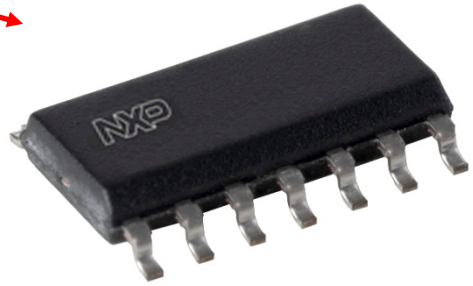
- Through hole
- Surface mount
- Flip chip

Encapsulation

- Hermetic
- Plastic

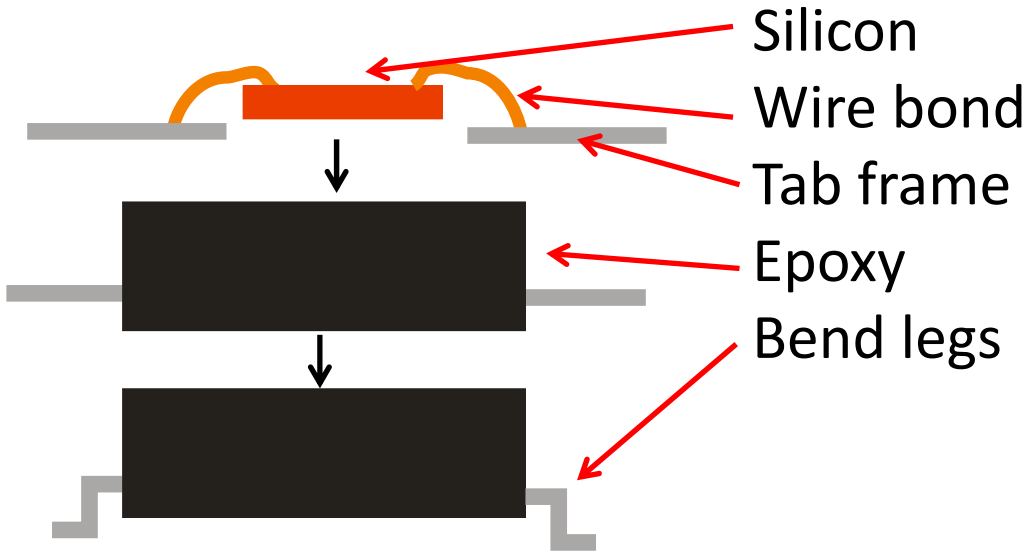


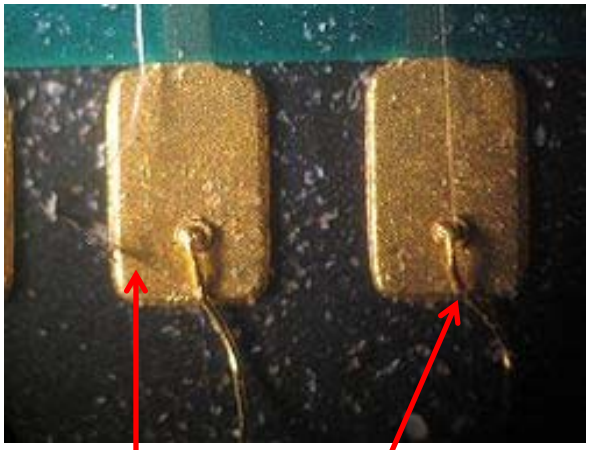
25 µm gold wire

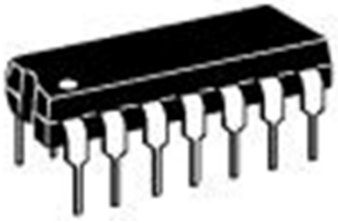


‘SOP14’ plastic
Small Outline Package

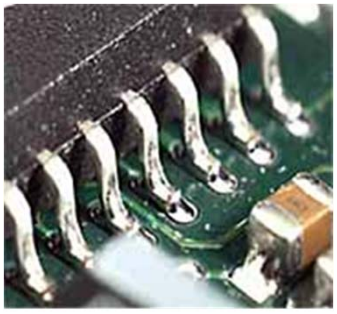
Tape automated bonding (TAB)







Through hole package

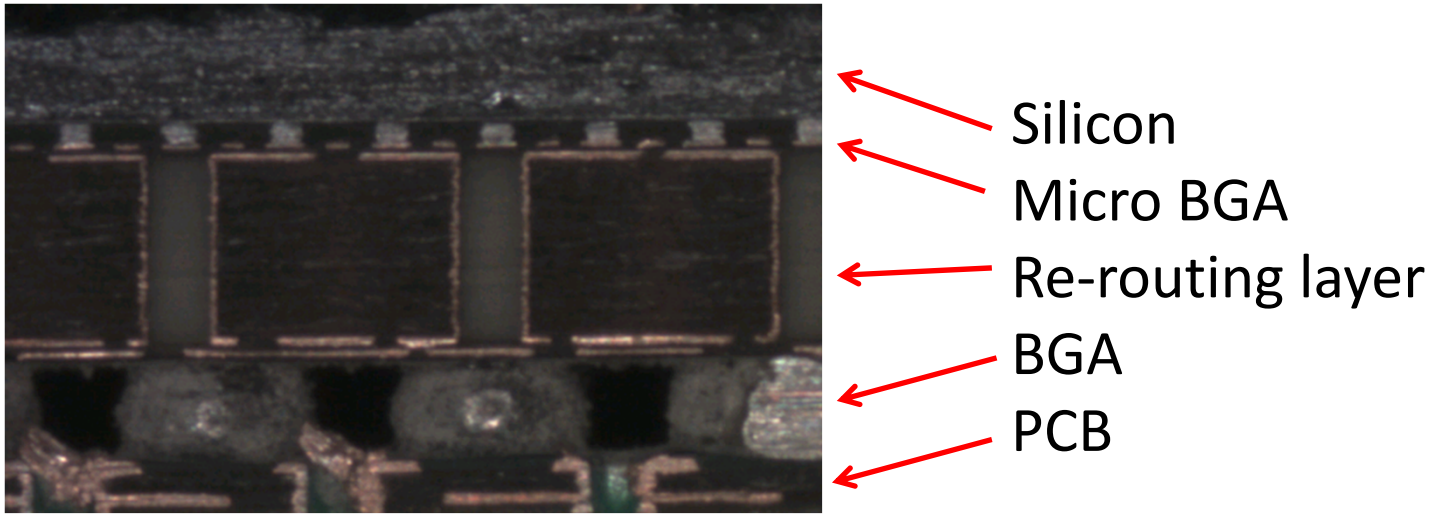


(TWI)

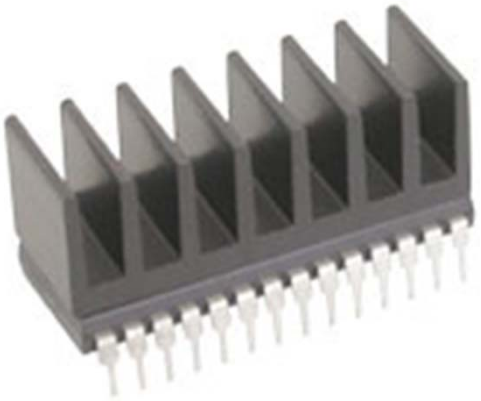
Surface mount package

Ball Grid Array

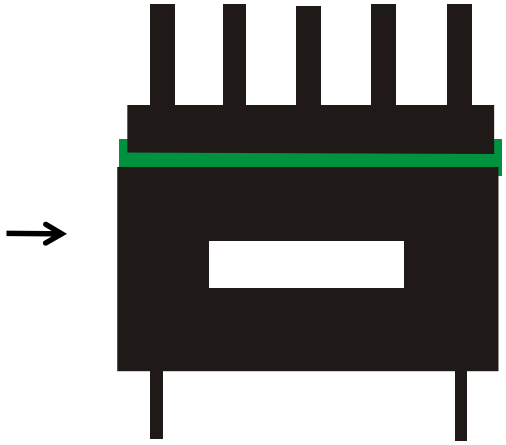
- Used for high I/O devices, e.g. Pentium

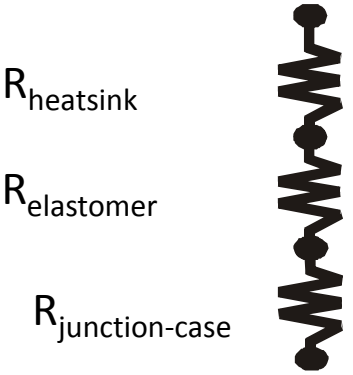


Thermal issues



Finned heat sink on DIP





Assume for silicon, T_{max} = 125°C, assume air temperature = 20°C

therefore $\Delta T = 125 - 20 = 105°C$

Assume elastomer sheet interface material: $R_{elastomer}$ = 0.4 W/m°C

$R_{total} = R_{jc} + R_{elastomer} + R_{heatsink} = \Delta T/Q$ (Q = power = 2W)

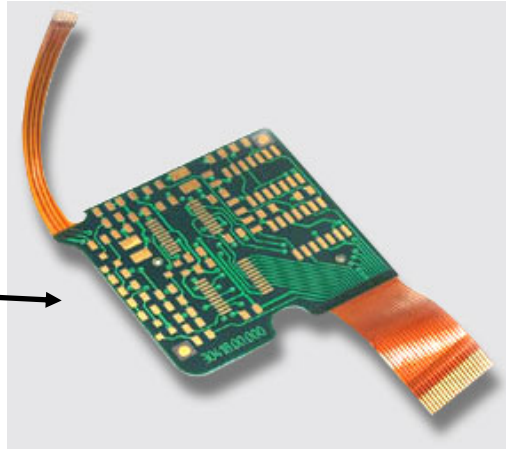
therefore:

$R_{heatsink} = \Delta T/Q - R_{jc} - R_{elastomer}$

$= 105/2 - 19 - 0.4$

= 33 W/°C

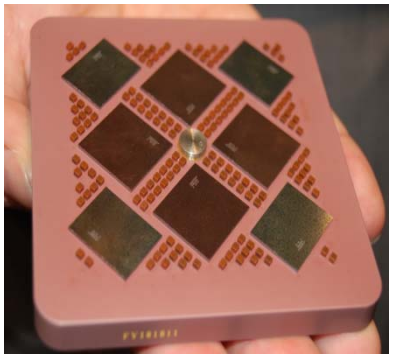
Substrates



- Printed Circuit Board - PCB

(or Printed Wiring Board - PWB)
Laminate construction
Circuit patterning (photolithography and metallisation)
Vias
Single and Multi-layer PCBs
Flexible PCBs

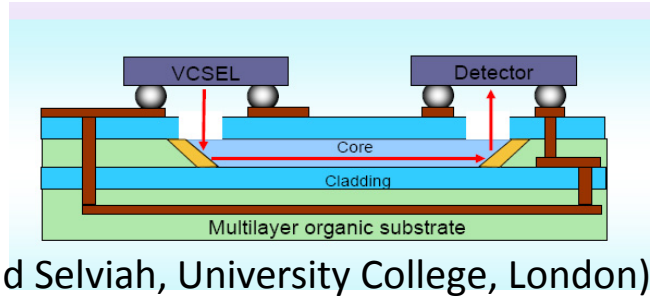
- Ceramic Substrate



Embedded passives

- Opto-electronic PCB

Embedded waveguides



David Selviah, University College, London)

PCB laminate construction

+

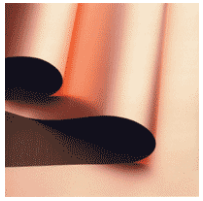
=

Woven glass-fibre cloth

Epoxy resin

Preimpregnated cloth ‘prepreg’

+



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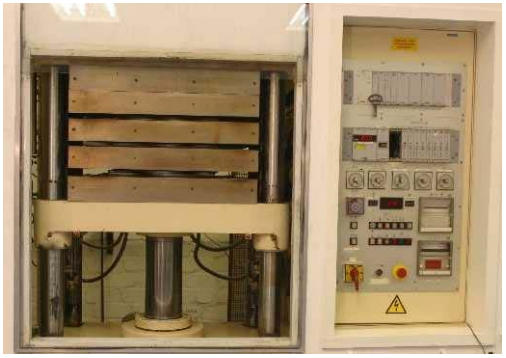


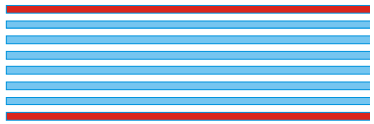
→

n x prepreg)

2 x copper

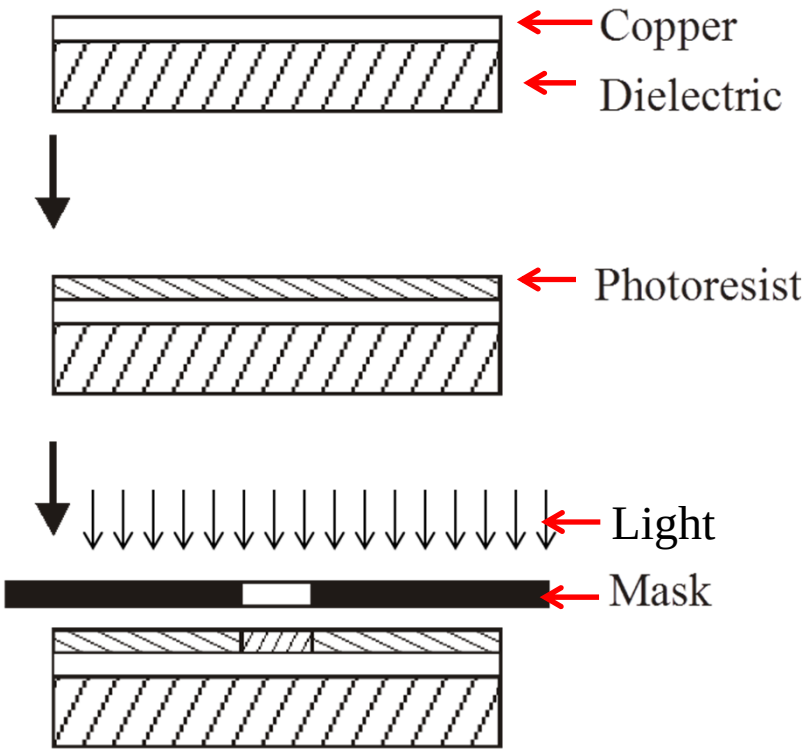
Press (180 °C, 20 bar)

Laminate



Photolithography

Photo – light
Litho – stone
Graphy – pattern
hence:
Patterning stone (silicon) using light

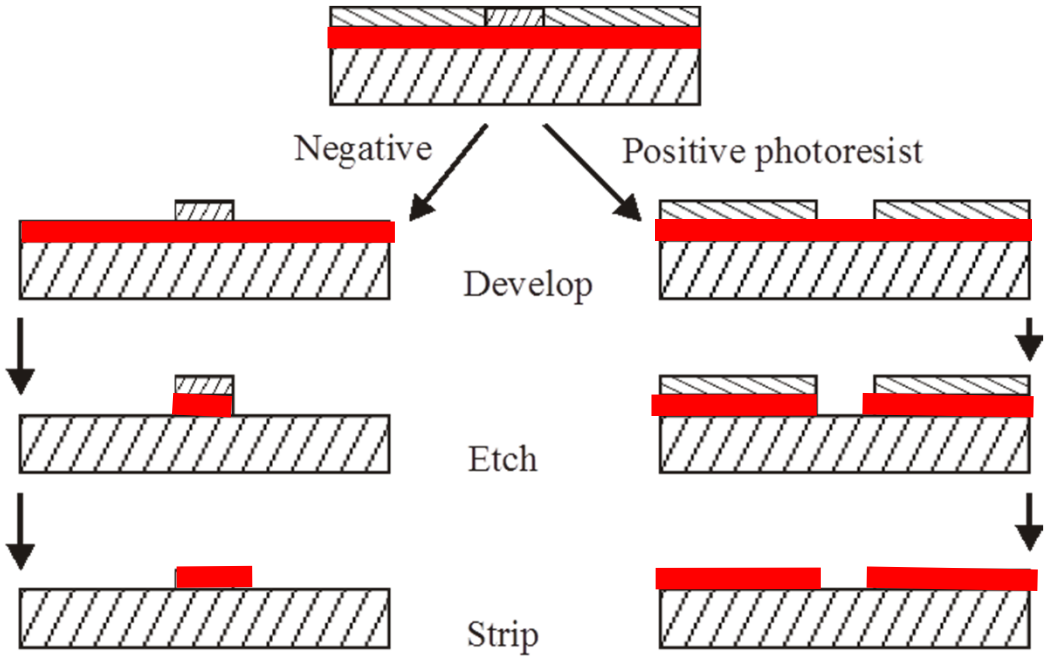


Photoresist – light-sensitive polymer
Two 'flavours':

Negative acting:
- light makes resist less soluble in developer
- light causes polymerisation of resist, hence *less* soluble in developer

Positive acting:
- light makes resist more soluble in developer
- light causes photo-acid generation, leading to depolymerisation of resist, hence *more* soluble in developer

Subtractive* process

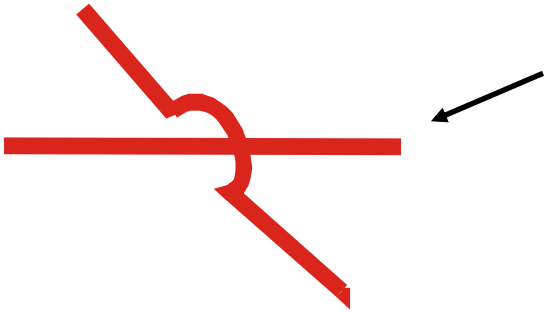


(* i.e. etching of exposed copper)

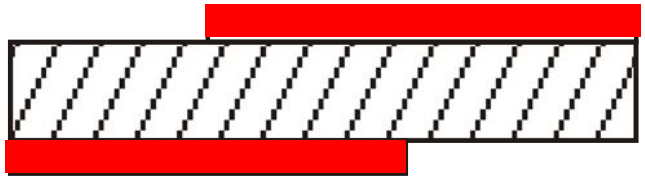
Copper thickness measured in ounces/foot^2
Standard thickness = 1oz/ft^2 = 35 µm

Additive process also possible, involving electroplating of copper onto exposed areas

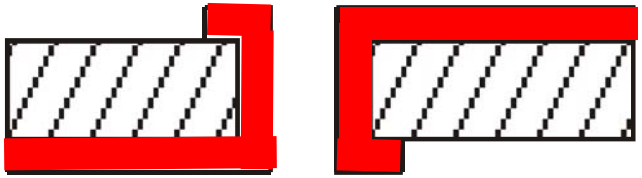
Two-layer PCBs



Cross-overs not possible in one layer, therefore, we need Vias



Double-sided PCB

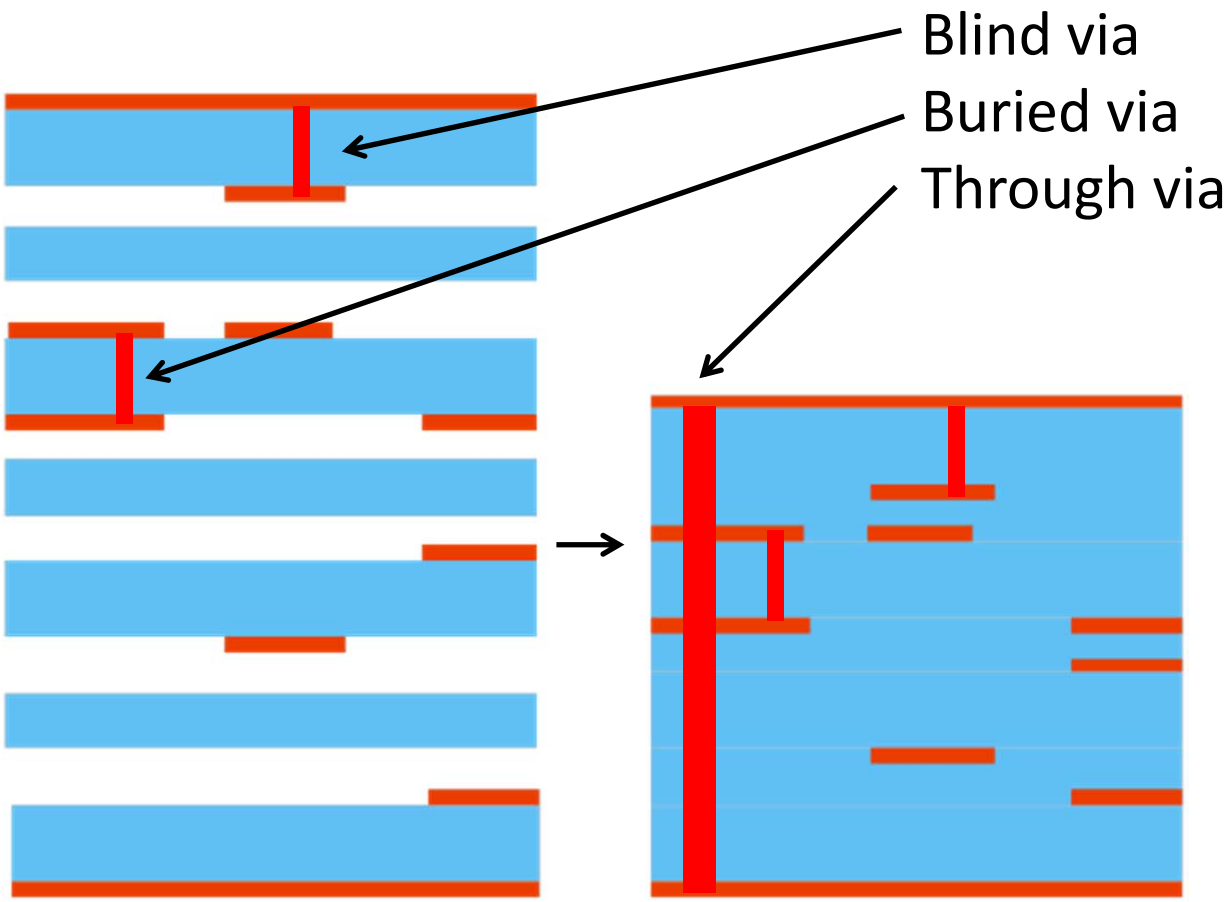


Through via

Sequence:

- Pattern top and bottom surfaces
- Drill through hole (‘via’)
- Plate hole

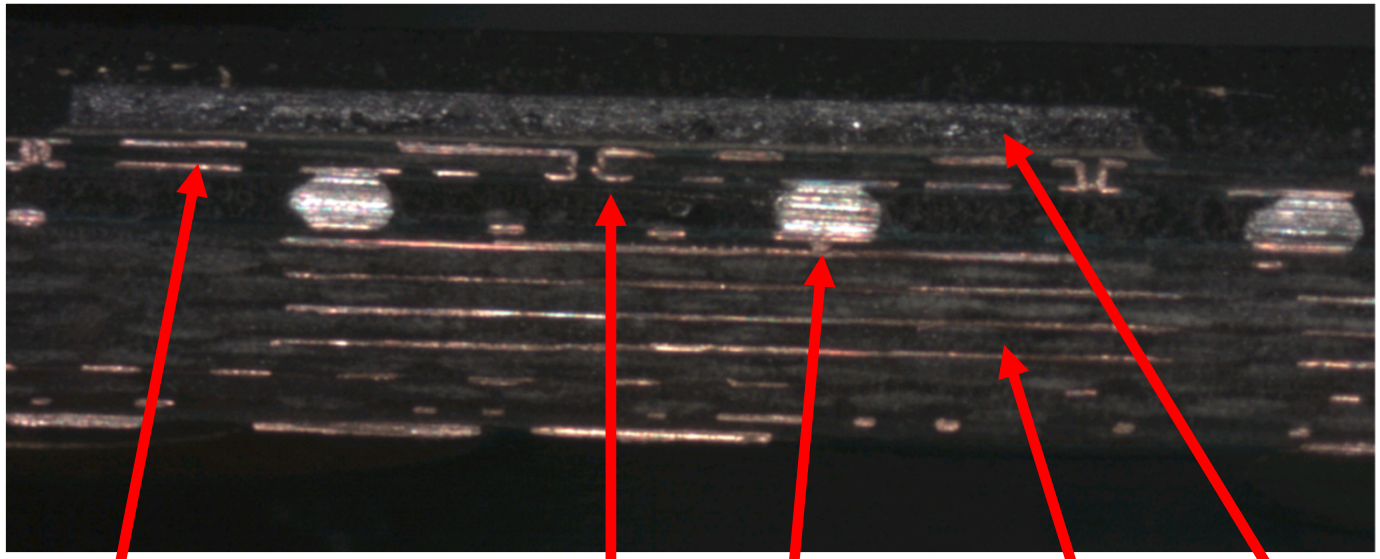
Multilayer PCB



Make 2-layer boards and interleave with prepreg

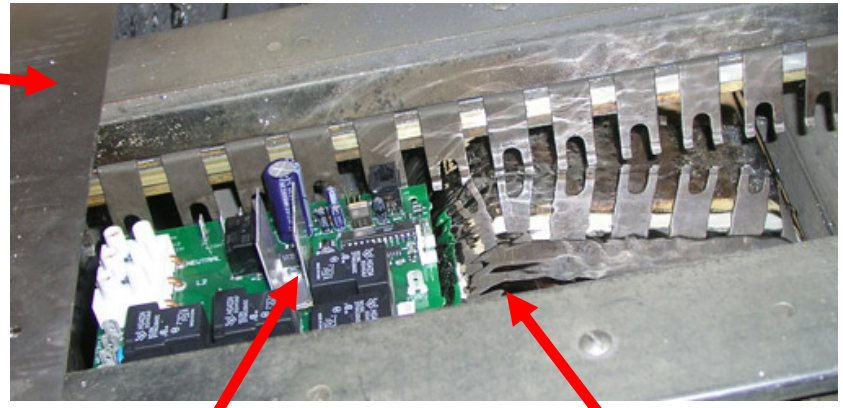
Press

Mobile phone cross-section



Level 2: Component-Substrate Interconnect

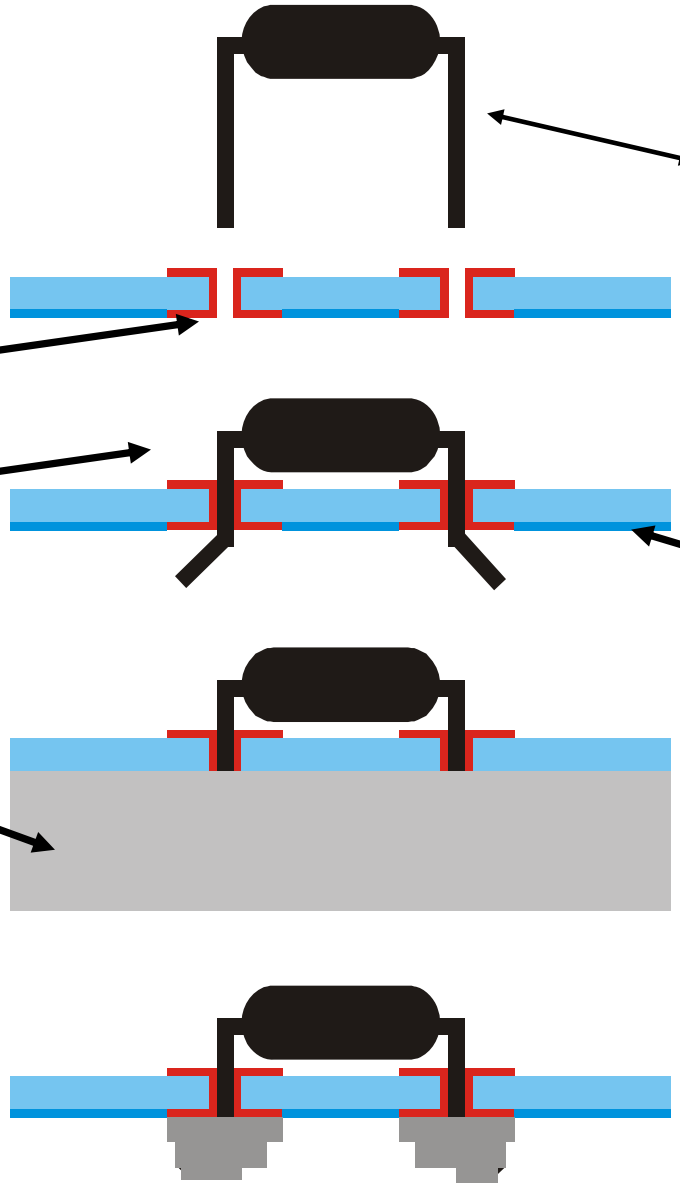
- Through hole – 'wave' soldering
- Surface mount - screen printing of solder paste followed by reflow soldering
- Lead-free solders
- Underfill for stress relief
- Conductive adhesive



Populated PCB

Wave

Wave soldering



Plated through hole (PTH)

Dual Inline Pin (DIP) Package

Insert, cut and clinch

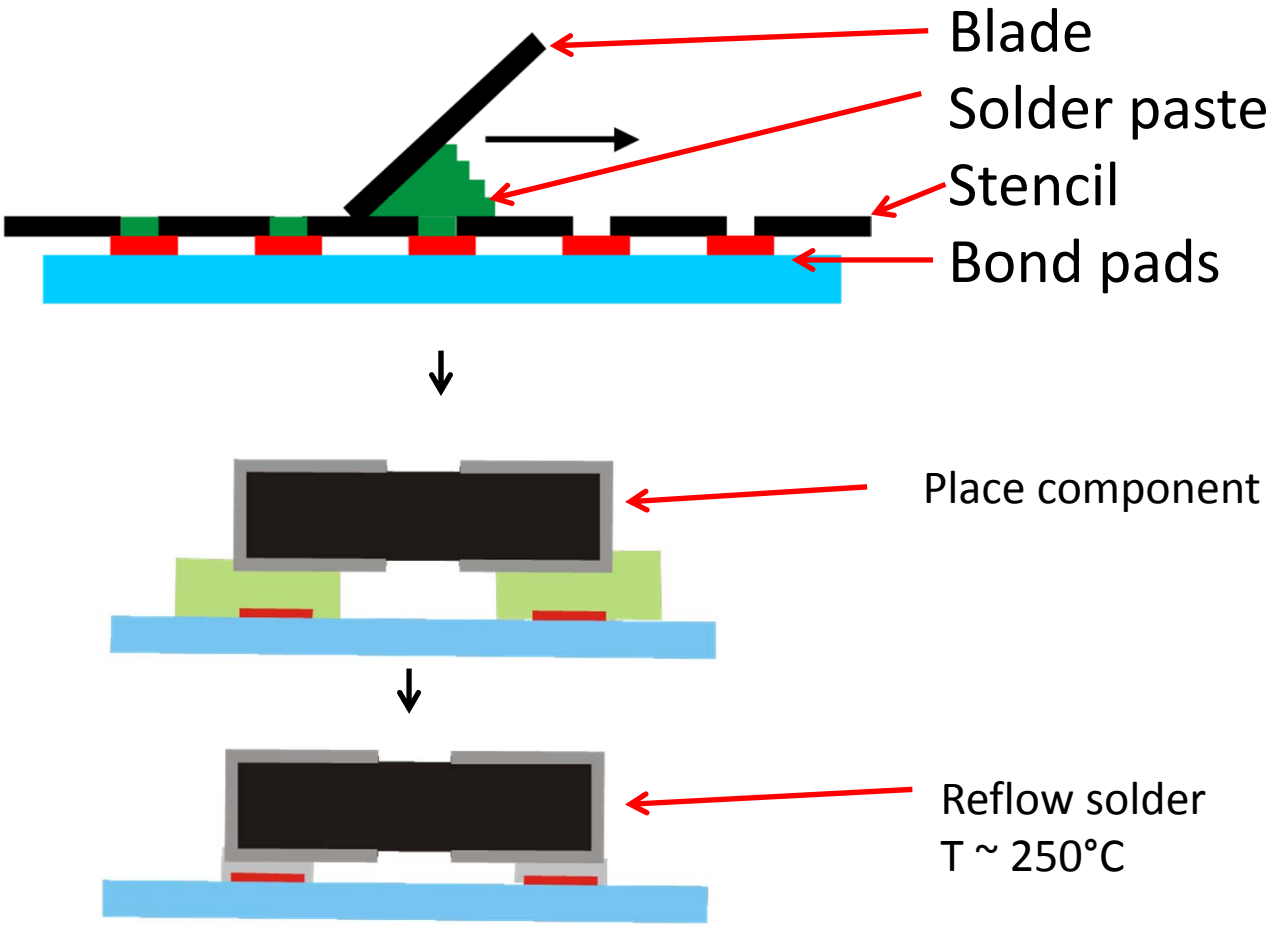
Solder mask

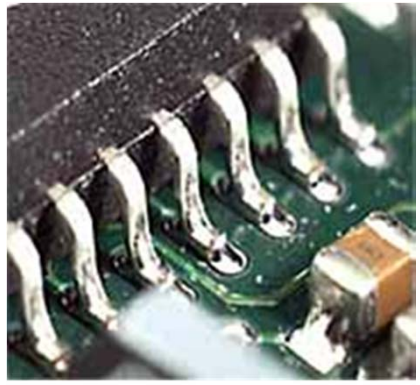
Immerse in ‘wave’ of molten solder

Solder and heat applied simultaneously

Components only on one side of PCB

Surface Mount

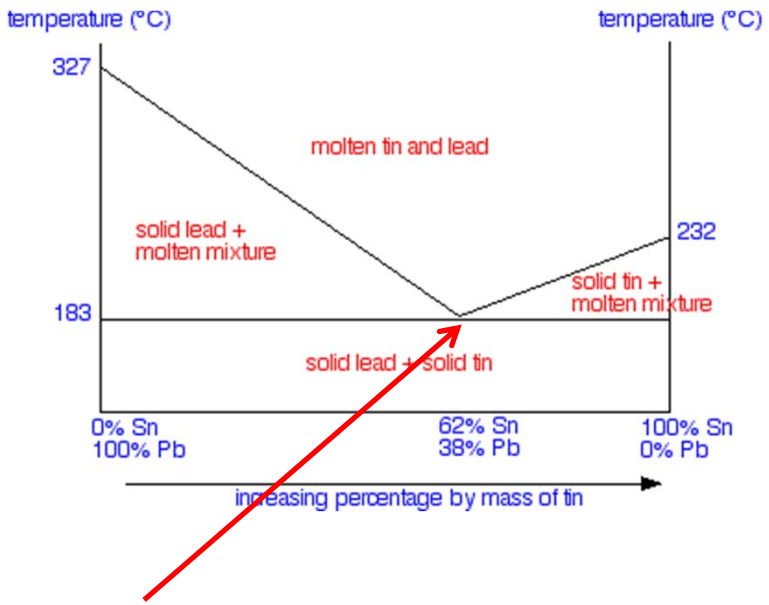




(TWI)

Solder

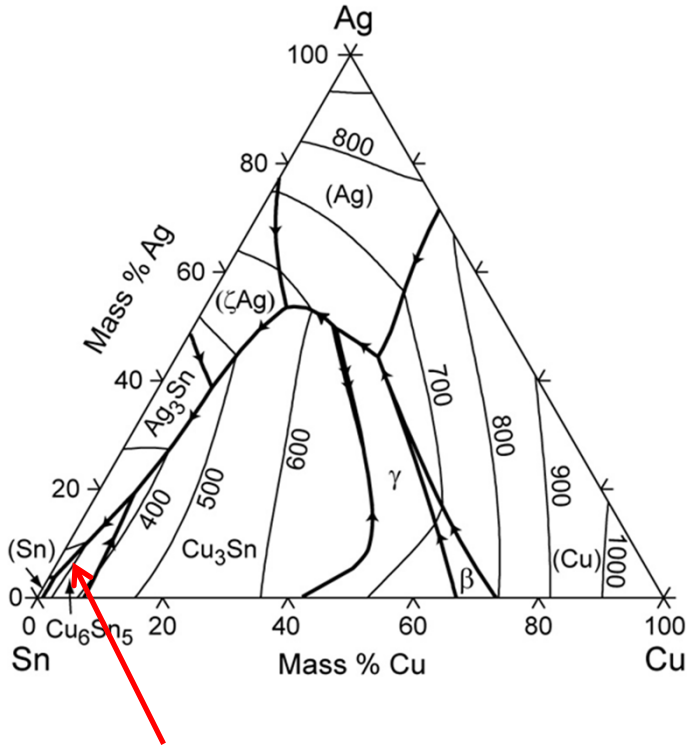
Tin-Lead phase diagram



62%Sn 38%Pb has lowest melting point ('eutectic')

T_m = 163 °C

Tin-Silver-Copper phase diagram



Eutectic 96.5%Sn 3%Ag 0.5% Cu

'SAC305'

T_m = 217 °C

‘Level 3’:
System-level assembly and design

Assembly

Connectors

Switches

Backplanes

Design

System partitioning between PCBs

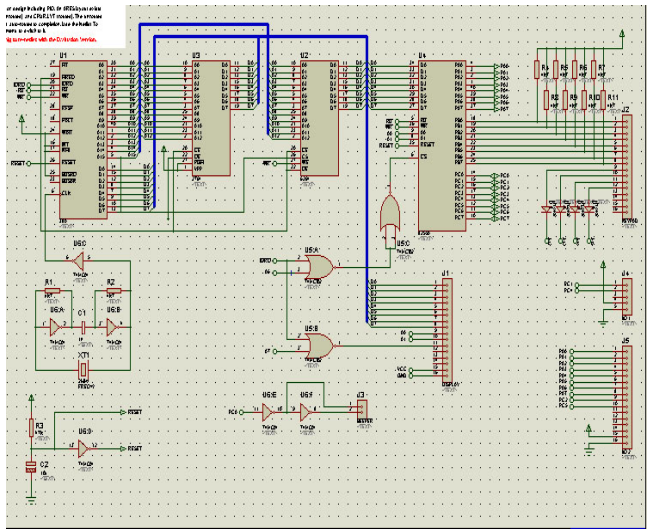
Placement of components on PCB

Routing between chips

Electrical constraints

Thermal management

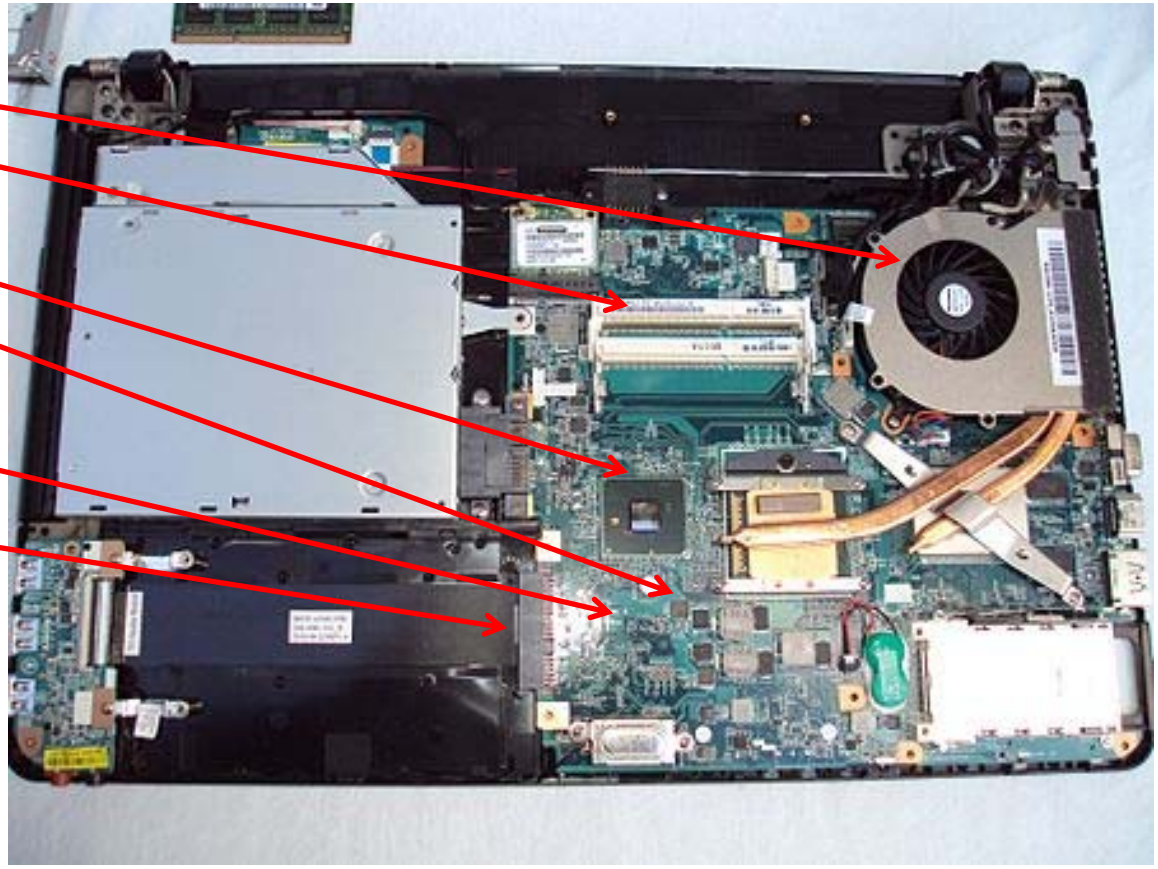
Mechanical constraints



Overview

Cooling
Through hole
BGA
Surface mount

Multilayer PCB
Connectors



Vaio motherboard