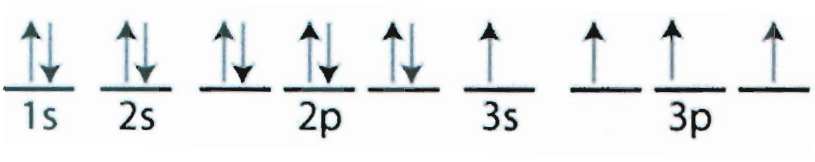
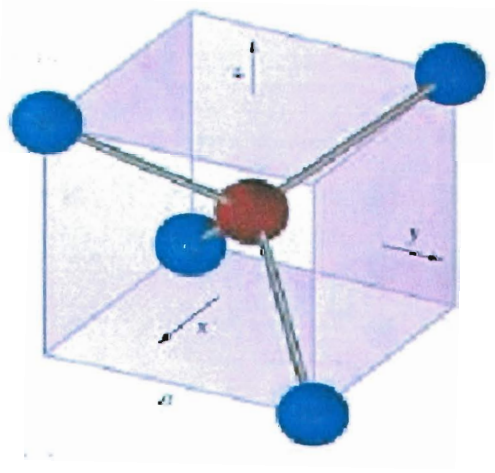
Solution to EEE 402/6042 2011-2012:

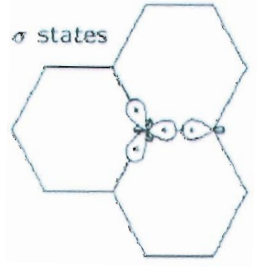
Q1a.

Silicon $1S^2$, $2S^2$, $2p^6$, $3s^1$ $3p_x^1$,$3p_y^1$, $3p_z^1$



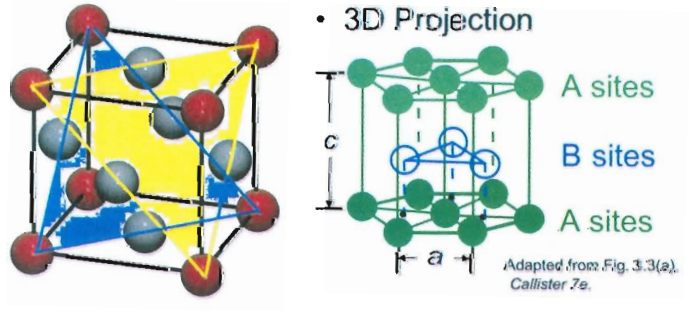


C6, $1S^2$, $2s^1$, $2p_x^1$,$2p_y^1$, $2p_z^1$.



5

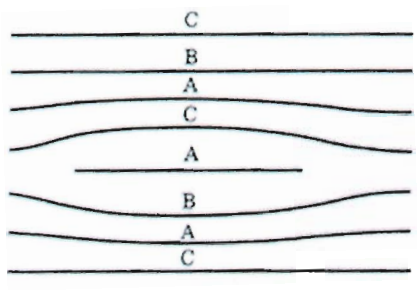
Q1b) Packing sequence for HCP: ABAB and FOR FCC: ABCABC.

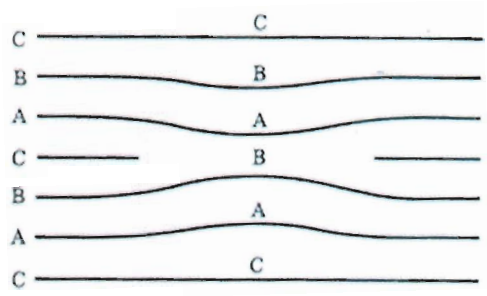


A diamond cubic is two interlocking fCC. 5

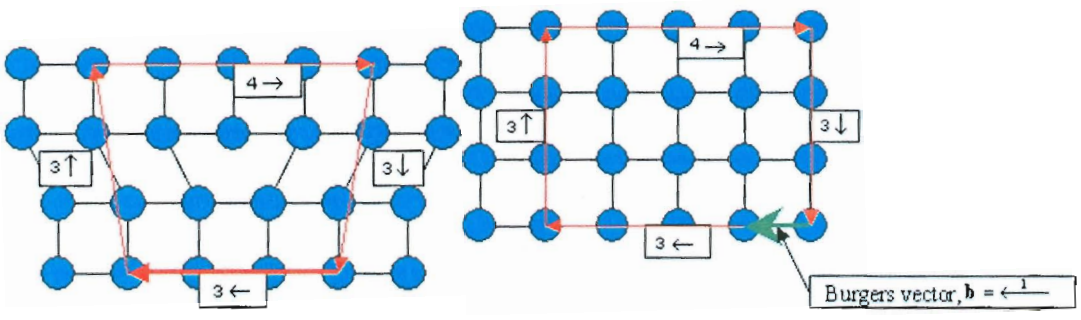
Q1c)

Two types of stacking faults, intrinsic and extrinsic.





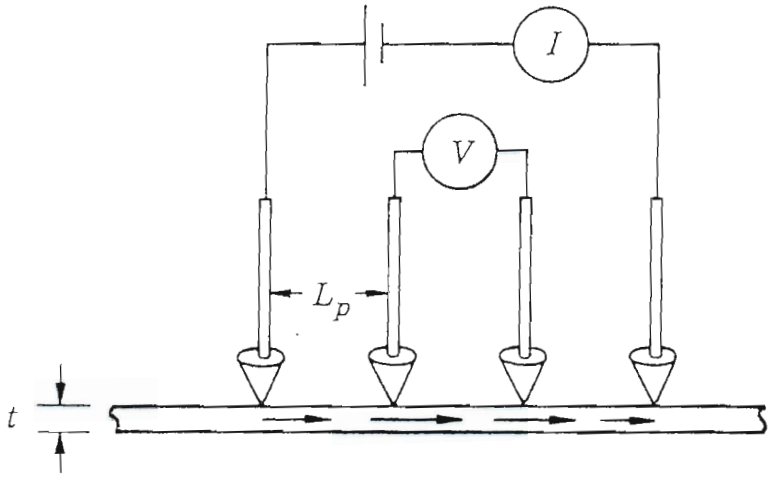
According to diagram: CBACABAC INTRINSIC: CBABAC.



Trace around the end of the dislocation plane to form a closed loop. Record the number of lattice vectors travelled along each side of the loop. (Numbers in the boxes shown here).

In a perfect lattice, trace out the same path, moving the same number of lattice vectors along each direction as before. This loop will not be complete and the closure failure is the Burgess vector. 5

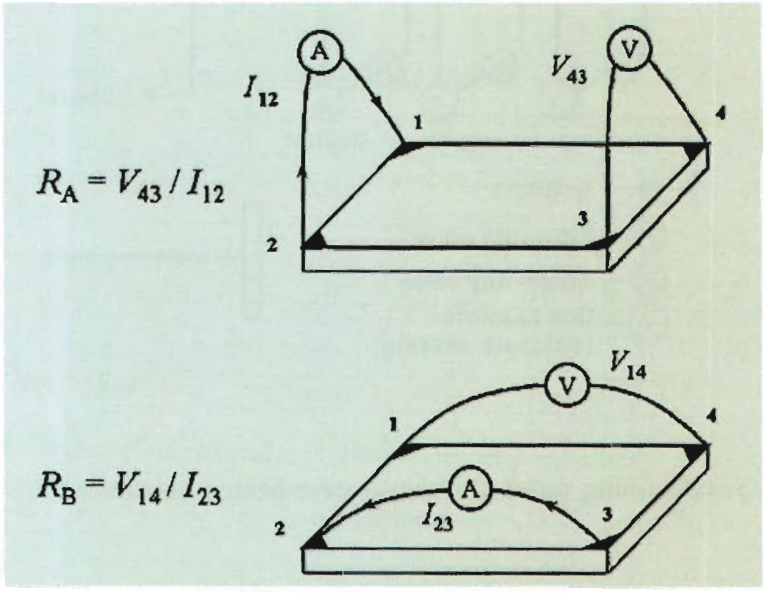
Q1d) Four point probe and Van der Paw (with diagram). 5



- **current (I) injected through outer probes**

- **voltage (V) measured by inner probes**
  - **$R_s = K_p(V/I)$ where K_p is a constant depending on configuration of probes and sample**
  - **$K_p = \pi / \ln 2 = 4.53$ if the film is effectively infinite in all directions**
- **this method avoids contact resistance problems at the current probe**

Van De Paaw



$$\exp(-\pi L \, R_A / R_S) + \exp(-\pi L \, R_B / R_S) = 1$$

Q2a)

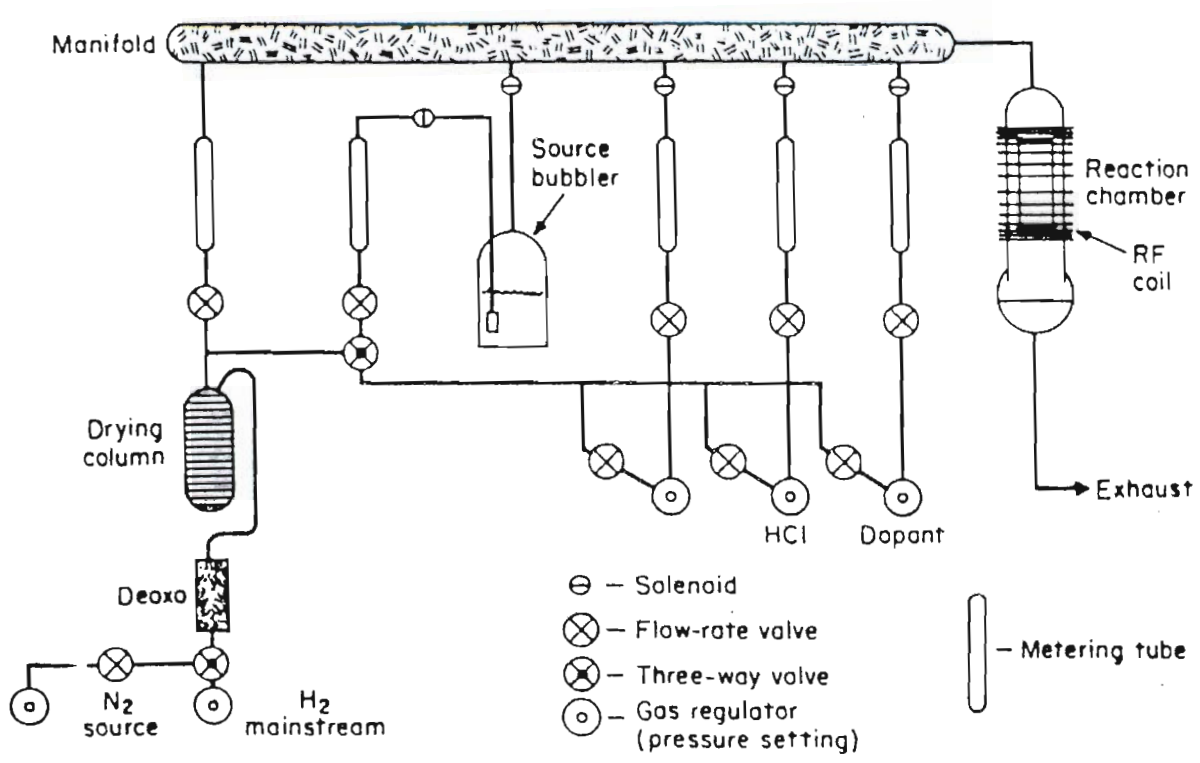
High vapour pressure of group V (100 kPa (1 at) for As in gallium arsenide) and ~ 3,500 kPa (35 at) for **P** in gallium phosphide.

It is dangerous to apply this pressure directly.

Solution: Layer of molten boric oxide is floated on top of the melt Pressure vessel is still used, but in an inert atmosphere of Argon.

Ingot diameter is largely a function of pulling speed and speed of rotation, controlled by in situ radiography or measuring change in ingot mass. 5

Q2b)



CVD apparatus.

Several types of reaction involving Si-containing gases flowing over a heated substrate are possible.

- Most important is the hydrogen reduction of silicon tetrachloride, which takes place on a heated surface

  $SiCl4 + 2\ H2 \rightarrow Si + 4\ HCl$

- Deposited Si atoms run around on a substrate and join steps at the edges of growing crystal planes extending across the surface

- The deposition temperature is generally in the range ~800-1200 C in order to give high quality, single crystal si layers, with good thickness uniformity at deposition rates in the range ~0.01-5 μm/min.

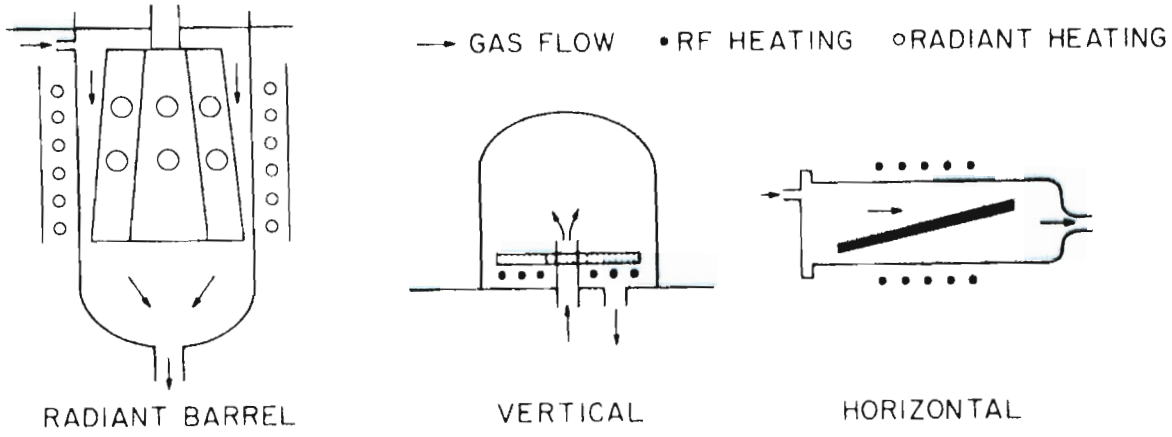
- Prior to deposition, substrates would typeically be given a vapour etch with flowing HCl or a bake in H2 gas to clean their surfaces.

Criteria for growth

- Gas flow in the chamber must be very uniform to give layer thickness uniformity on each of the substrate wafers.

- Autodoping must be avoided.

- Residual contamination present on substrate before epitaxy lead to stacking faults or pyramidal hillocks.
- Non uniform heating leads to slip and dislocations.



The three generic designs of a CVD reactor are (i) radiant barrel (ii) vertical barrel and (iii) horizontal barrel. (DIAGRAMS) 6

Q2c) Autodoping is when impurity diffuses out into a growing epitaxial layer during growth.

Diffusion of impurity from substrate must be outpaced by layer growth: can be checked by calculating the characteristic impurity diffusion length.

At 1120°C (1393K) $D = 0.76 \exp -[3.46/(8.62 \times 10^{-5} \times 1393]$

$= 2.32628 \times 10^{-13}$ cm/s

For 60s $2\sqrt{(Dt)} = 2\sqrt{(2.326 \times 10^{-13} \text{ cm} \times 60)}$ cm

$= 3.736 \times 10^{-6}$ cm

$= 0.03736 \mu m$

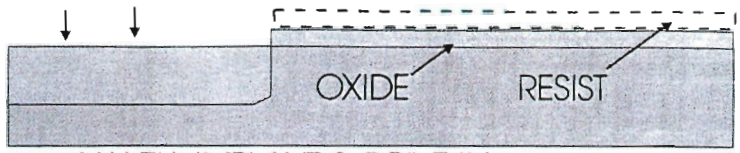
Then, autodoping is not a problem. 5

Q2d)

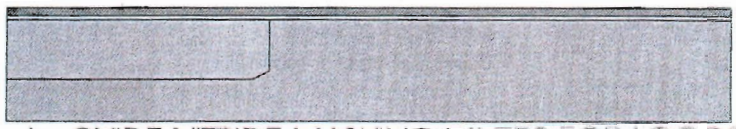
a) Potential issues with GaN on silicon are lattice mismatch, leading to high dislocation density and mismatch of thermal coefficients as well as poor thermal conductivity of the silicon substrate. Additional issues include antiphase domains, silicide formation, a 'difficult' heterojunction for transport etc.

Potential use: High Power electronic devices. 4

Q3a)

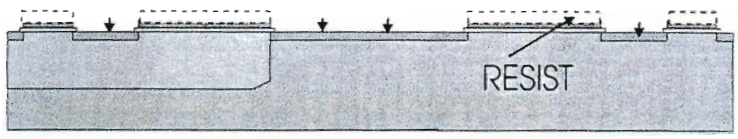


a. N-WELL IMPLANT & DRIVE IN

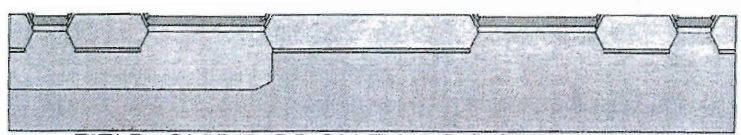


b. OXIDE/NITRIDE MASKING LAYERS FOR LOCOS

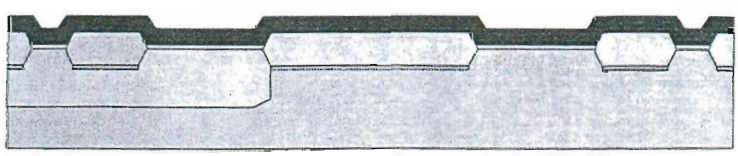
c. OXIDE/NITRIDE PATTERNING



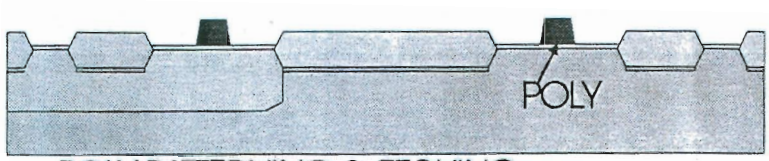
d. FIELD THRESHOLD ADJUST IMPLANT



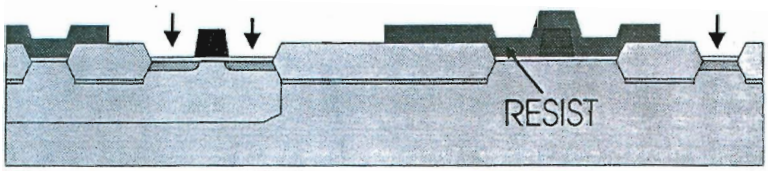
e. FIELD OXIDE GROWTH (LOCOS)



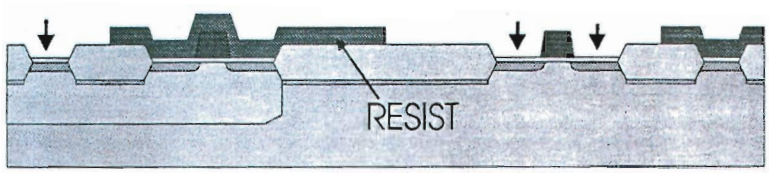
f. GATE OXIDE GROWTH FOLLOWED BY POLY DEP.



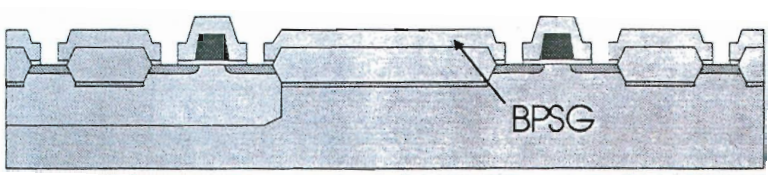
g. POLY PATTERNING & ETCHING



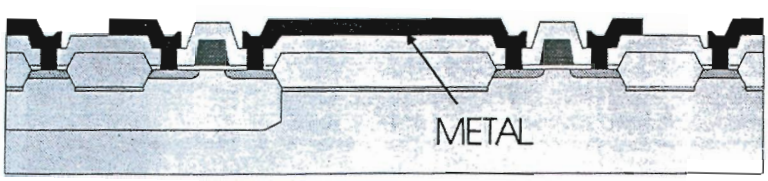
h. RESIST MASK FOR P+ SOURCE & DRAIN IMPLANT



i. RESIST MASK FOR N+ SOURCE & DRAIN IMPLANT



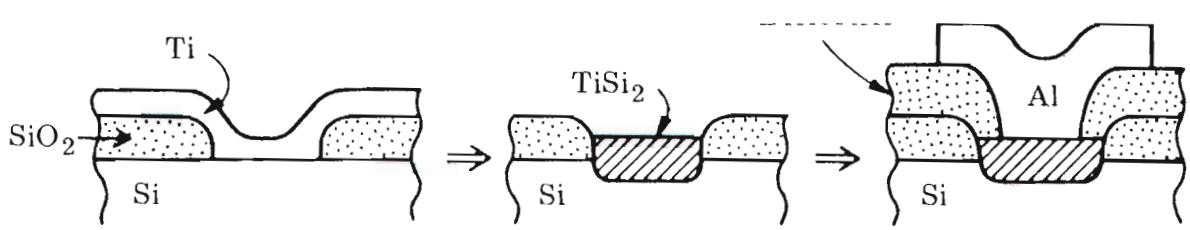
j. .BPSG DEPOSITION & CONTACT WINDOW ETCH



k. METAL DEPOSITION AND ETCH

CMOS flow with diagrams. 10

Q3b) 5

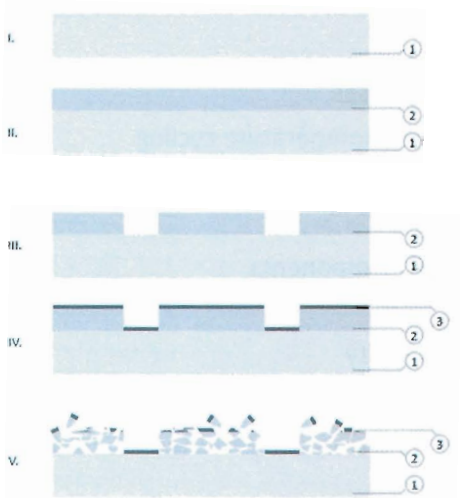


- More recent applications, with greatly reduced device dimensions, require even lower interconnect and contact resistances, together with ***lower processing temperatures***
  - encouraged the use of ***TiSi2 and CoSi2*** which can readily be formed at low temperature by ***direct reaction*** of, in each case, the metal and **Si**

        - at such temperatures, the metal does not react with surrounding oxide so that contact ***silicide formation is self-aligned*** - so-called ***salicide process*** **(Fig)**

- In the future, ***epitaxial silicides*** may become important because they offer potentially 'ideal' interfaces with **Si** and higher temperature stability
    - could be used as stable contacts to shallow junctions.
    - Future materials to replace silicon are InGaAs for n type and Ge for p type.
        - **NiAuGe`** alloy to **n**-type **GaAs**
        - **AuZn** alloy to **p**-type **GaAs.**

Q3c)



1. Substrate.
2. Photoresist on substrate.
3. Mask and patterning.
4. Deposit metal.
5. Etch PR- leaves metal behind. 5

Q4a) Failure Mechanisms.

- **SiO_2 *and* Si/SiO_2 *interface associated*** ***2.5***
  - surface charge accumulation - migration of mobile ions such as **Na+, K+**
    - impurities in oxidation gases

correct problem, use (more) **HCl**, etc

  - failure of passivation

improve quality / increase thickness of passivation

  - dielectric breakdown - failure of gate (or capacitor) oxide
    - nonoptimum gate oxide

improve gate oxide integrity

  - electrostatic discharge damage
    - improve input/output circuit protection networks (user must take appropriate precautions when handling devices)
- ***Metallization associated*** ***2.5***
  - electromigration - migration of interconnect material under current load
    - too high current densities or nonoptimum interconnect alloy

lower current densities, change alloys or use Cu

  - corrosion - degradation of metal tracks, etc
    - contamination in package

check purity of constituents and package integrity

  - contact degradation - metal / semiconductor interactions
    - too high operating temperature, presence of impurities

correct operating conditions

- ***Bonds and other mechanical interfaces*** ***1***

- intermetallic growth - interaction between metals
  - too high operating temperature, presence of impurities

correct operating conditions

- fatigue - change due to internal stresses
  - low bond strength, extreme temperature cycling

improve bonding and / or correct operating conditions

- ***Hermeticity*** ***1***
  - seal leaks - ingress of atmospheric components

(especially moisture)

- seal failure or package porosity

improve materials / processes.

Q4b)

Resistance of track= 0.5 (length/width)Ω

Resistance of (1 μm) = 0.5 $(4x10^{-1})/10^{-4})$ Ω

Resistance of (5 μm) = 0.5 $(4x10^{-1})/5x10^{-4})$Ω 3

Rs=kp V/I

Therefore V=Rs*I/kp= 2000*0.001/4.53= 2/4.53=0.44 V for first track

And V=400*0.001/4.53=2.22V for second track

Q4c) MOCVD versus MBE.
Explain what the growth characteristics of each depend upon. 6

- **General Comparison of MOCVD and MBE Techniques**
  - While there may be specific device and materials issues in certain cases, we can identify at least two key generic differences between the techniques
  - MBE layers can be grown at *lower temperatures* than for MOCVD
    - MBE is not limited by precursor decomposition kinetics
  - MOCVD employs a *simpler technology* than MBE
    - MOCVD does not require advanced DRV technology
    - but, MOCVD does need substantial toxic gas handling facilities 4