Feedback for EEE335 Session: 2013-2014

General Comments:

Question 1:

This question was generally well-attempted. In part a some people did not identify where the substrate would be connected (or showed it connected to ground). In part b, a number of people ended up with a non-inverting expression (correct in other respects)! In part c there were two possible answers: M1=4, M2=4, M3=2, M4=2, M5=2 OR M1=3, M2=3, M3=1.5, M4=3, M5=3. Nobody who chose the 2nd answer (the majority) got the right width for M3. If M4 or M5 is on, each contributes 1/3 and so M3 must contribute 2/3 so the path = 1. Hence the width of M3 = 1.5. In part d, I was looking for some clear points: you might want to connect the substrate to the source, the formation of wells forces transistors to share substrate connections, the substrate must be at least as negative as the most negative source (to avoid the source/body junction forward biasing). For a digital circuit this is going to be ground. In part e) some people did not read the question properly and removed transistors M4 and M5 rather than, as the question said, 'The wire connecting the drains of M4 and M5 is removed'.

Question 2:

This question was less well-answered. People seemed unable to give a reasoned list for part a.ii). The descriptions for what and why RTL is, b.i), were generally poor. RTL is where date is transferred from register to register with intervening logic 'processing' the information. Data clocked into a register will be data clocked into other registers on the previous clock edge, which has had one whole clock cycle to pass through the intervening logic. This ties in with the clock tree, which is designed to ensure that each FF is clocked at the same instant. By doing it this way, you minimize the risk of race hazards (which may be temp/voltage/process) dependent from disrupting the behavior of the design.

Question 3:

Reasonably well-answered. In part a(i), several students confused V_{GS} and V_{DS} so that they computed an incorrect value for the overdrive voltage. Most students had a good stab at the small-signal diagram in part a(ii), but in part b marks were lost for not showing the inversion of the output waveform with respect to the input. Part c(i) was answered quite well, but the importance of maximizing a current mirror's output resistance was not generally well explained in part c(ii). The crucial point was that the current mirror sinks an almost-constant current over a large range of output voltages provided its output impedance is high.

Question 4:

Parts a and b were comfortable ground for most students. Identifying the virtual ground node (at the source of M3/4) and the Q-point voltage at this node confused students: because the input was balanced the Q-point at the virtual ground was simply $V_{GS} = V_{OV}+V_{TO}$.

Part d was a struggle in general, and indeed this was the most difficult question in the analogue part of the exam. The answer required deriving an expression for the Miller capacitance, then substituting this into the expression for the cutoff frequency and rearranging.