[redacted] EEE6393

~~EEE 6393 20211 Model answers Q1 and 2~~

Data Provided:

Thermal conductivity of silica-loaded epoxy:	$k_{epoxy} = 1.40$ W m^{-1} K^{-1}
Thermal conductivity of thermal grease:	$k_{grease} = 0.80$ W m^{-1} K^{-1}
Stefan-Boltzmann constant:	$\sigma = 5.67\times10^{-8}$ W m^{-2} K^{-4}
Electronic charge:	$e = 1.60\times10^{-19}$ C
Boltzmann constant:	$k_B = 1.38\times10^{-23}$ m^2 kg s^{-2} K^{-1}
Permeability of free space:	$\mu_o = 1.26\times10^{-6}$ m kg s^{-2} A^{-2}

1. a. Assume negligible thermal conduction through wire bonds, since they are very thin.

Assume ambient temperature = 20 °C

Hence, maximum temperature difference $\Delta T = 100\text{-}20 = 80$ °C

Assume thickness of thermal grease $L_{grease} = 0.1$ mm

Area of die $A_{die} = (1\text{x}10^{-2})^2 = 1\text{x}10^{-4}$ m

Hence, thermal resistance of grease $R_{grease} = L_{grease} / k_{grease} A_{die}$

$= 0.1\text{x}10^{-3} / 0.8 \text{ x } 1\text{x}10^{-4} = 1.25$ °C/W

Assuming no heat spreading, thermal resistance of epoxy $R_{epoxy} = L_{epoxy} / k_{epoxy} A_{die}$

Hence $R_{epoxy} = 1\text{x}10^{-3} / 1.4 \text{ x } 1\text{x}10^{-4} = 7.1$ °C/W

Fourier's Law of Heat Transfer $\Delta T = QR$

Where, in this case $R = R_{epoxy} + R_{grease} + R_{heatsink}$

Hence $R_{heatsink} = \Delta T/Q - R_{epoxy} - R_{grease} = 80/4 - 7.1 - 1.25 =$ **11.65 °C/W** **(6)**

b. Silica-loading increases the thermal conductivity of the epoxy. This improves heat dissipation. Loading also reduces the thermal expansion coefficient, leading to a smaller mismatch to silicon. This helps to reduce the stresses induced by temperature changes. The loading material must be an electrical insulator, in order to avoid current leakage. Other suitable materials include various other oxides (e.g. alumina) and even diamond. **(3)**

c. There is a large difference between the thermal expansion coefficients of the heat sink (typically aluminium) and the package body (silica-loaded epoxy). If the two were rigidly connected (i.e. with epoxy), then large stresses would occur as the temperature changed from the bonding temperature. This would lead to possible cracking of the package and failure of the device. **(3)**

d. Reflow soldering: Screen printing of solder paste. Pick and place of components on top surface of PCB. Preheat (drive off solvent). Soak (activate flux, ensure isothermal board). Reflow (a few degrees above melting pint of solder (~200 °C) for a short time). Cool (control cooling rate to avoid thermal shock). Generally a series of infra-red oven s linked by conveyor belt.

Chips on underside limited to small components that will not fall off if done by reflow. Alternatively through hole components could be added by a previous wave soldering process, provided higher melting point solder were used. **(8)**

2. a. Hole formation: laser drilling (high rep. rate UV laser) or plasma drilling (Bosch process). Hole passivation. Seed layer deposition. Copper filling by electroplating.

They are being developed in order to aid further miniaturisation of electronics systems, since it is becoming ever more expensive / difficult to keep up with Moore's Law by simply shrinking feature size. **(8)**

b. Partition ICs between PCBs, with microprocessor and ASIC on different boards, to simplify power distribution. Choose IC package types, if available. Choose connectors. Simulate logic. Layout PCB. Route tracks. Verify design rules. Fabricate prototype and test (electrical, thermal, mechanical). **(6)**

c. P_{tot} = 20 W hence average power per board = 10 W

Hence average radiation power per board $P_{rad} = 10 \times 0.1 = 1$ W

$T_1 = 70\ °C = 70 + 273 = 343$ K

Board area $A = 0.1 \times 0.05 = 0.005\ m^2$

Assume: view factor $f = 1$ and emissivity $e = 0.8$

Assume that zero convective heat transfer from PCB to case.

Using Stefan-Boltzmann Law: $P_{rad} = \sigma feA(T_1^4 - T_2^4)$ hence

$$T_2 = (T_1^4 - (P_{rad} / \sigma feA))^{0.25}$$

$$= (343^4 - (1/(5.67 \times 10^{-8} \times 1 \times 0.8 \times 0.005))^{0.25} = 312\ K = \mathbf{38\ °C}$$ **(6)**

①

Q3-1

3a) System on a chip (SoC) - Integration of all (or most) of the discrete IC functions on to a single Si die. (1)

Advantages

Dense packing / routing - short, low parasitic interconnects compared to the off-package interconnects of the discrete IC approach. High speed / Low noise

Higher interconnect density, not limited by individual package. SoC has a special architecture to take advantage of this. Again leads to high speed / low noise improvements.

Reduction in PCB complexity + cost. Improvement in reliability due to overall system simplification. Major fab savings through economy of scale. (2)

Disadvantages

Difficult to integrate diverse technologies, eg: Digital with RF or Digital with MEMS.

Difficult to integrate with power amplification - power dissipation issues.

Noise isolation between different elements can be an issue (Crosstalk)

Expensive tooling (set up costs) - Especially in the IC design.. (2)

Elements of a digital SoC.

One or more ASIC processors.

DRAM + Flash-ROM (1)

Q3-2

(2) Timing sources - oscillators, counter, PLLs

ADC and DAC

Power management - Voltage regulation circuitry

SiP over SoC - lower development/tooling costs through utilisation of existing ICs, shorter time to market, more flexible in terms of use of diverse technologie (2)

b) Mutual Ind. $\frac{l}{d} = \frac{5}{1.2} = 4.17$ $\frac{d}{l} = 0.24$

$$\frac{\mu_0 l}{2\pi}\left[\ln\left(4.17+\sqrt{1+4.17^2}\right)-\sqrt{1+0.24^2}+0.2\right.$$

$$\ln(4.17+4.28) - 1.028 + 0.24$$

$\mu_0 = 1.256\times10^{-6}$ H.m^{-1}

$\ln(8.45) - 1.028 + 0.24$

$2.134 - 1.028 + 0.24 = 1.346.$

$\frac{\mu_0 l}{2\pi}$ l in Metres $\frac{1.256\times10^{-6} \times 5\times10^{-3}}{2\pi} = 1\times10^{-9}$.

$= 1\times10^{-9} \times (1.346)$

$L = \underline{1.35\,nH}$ (2)

Self Ind Leadframe $\frac{2L}{w+t} = \frac{2\times5}{0.2+0.1} = 33.3$

$\frac{w+t}{3L} = \frac{0.2+0.1}{3\times5} = 0.02$

$\ln(33.3) + 0.5 + 0.02 = 4.026.$

$L = 1\times10^{-9} \times 4.026 = 4.026\,nH$ (2) (1)

(3) $2l/r = \frac{2\times25}{25\times10^{-3}} = 200$. $\ln(200) - 0.75 = \frac{8.24}{4.55}$ Q3-3

$\frac{10\times25\times10^{-3}}{2\pi\times4.55} = 0.11nH$. (2) (1)

Bond wire leadframe is the biggest contributor, followed by leadframe and then the mutual inductance.

Bond wire – related to l/r reduce l increase r
inductance

l would mean a different package employing a small outline (SO) geometry. In these packages, the lead length can be reduced to ~3mm. (2)

Can increase bond wire diameter, but available space could be limited by pin-pin spacing

For leadframe – dominant term is $\frac{2l}{w+t}$

again need to reduce l – SOIC package.

For the mutual inductance one should consider if it is necessary to use 2 adjacent pins. This can be substantially reduced by separating the low noise pin outs

Flip chip – using solder bumps to connect to a 2D array (Ball or pin – BGA, PGA) offers substantial reduction in impedance. Bond length can be reduced down to ~50μm and the lead frame down to sub-1mm (2)

(4) Q3-4

IC Wafer area $= \pi r^2 = \pi \times 75^2 = 17663\,mm^2$

Defect Density $(D_0) = \frac{120}{17663}$ IC area $5 \times 5 = 25\,mm^2$ (A)

P_0 (zero defects) $= \exp(-D_0 A) = \exp\left(-\frac{120 \times 25}{17663}\right)$

Yield $= 0.844$ 84.4%. (2)

$P_1 = M e^{-M} = \frac{120 \times 25}{17663} e\left(-\frac{120 \times 25}{17663}\right)$

$= 0.144$.

New yield $= P_1 + \eta P_2 = 0.844 + 0.4 \times 0.144$

η: $40\% \rightarrow 0.4$

$= 0.902$

90.2%. (2)

5) Q4-1

a) Wire Bonding.

Gold (or Al) wire bonded between bond pads and lead frame. Single bonds - tends to be slow.

Tape Automated (TAB) (1)

Multiple bonds to a gold plated copper pre-form on tape. (1)

Flip chip - Solder bump in 3D array. Chip is flipped down onto package containing receptor pads for the solder bumps + re-flow takes place. (1)

(i) Processor - Flip chip - Short interconnection lengths gives low parasitics. Also allows for a very high interconnect density (2D array of solder bumps). (1)

(ii) Operational amplifier - Use TAB bonding. No need for the expensive tooling of Flip chip. Design of lead frame possibly unchanged for many years - initial tooling cost recovered many years ago. TAB is highly suited to high speed low cost production of volume products. (1)

(iii) Laboratory prototyping would use wire bonding. Tooling cost of TAB or flip chip cannot be justified (1) Need a fast and versatile method, which wire bonding can provide. Not interested in production cost at this stage

6)

b)

Power $P = \alpha C V^2 f$ for 4040 this is 0.63W

$$\frac{P_1}{P_2} = \frac{\alpha C_1 V_1^2 f_1}{\alpha C_2 V_2^2 f_2} \times \frac{n_{T_1}}{n_{T_2}}$$ C or area or 'node'2.

$$\frac{P_{17}}{P_{4040}} = \frac{(32\times10^{-9})^2 (0.9)^2 \; 3.4\times10^9}{(10\times10^{-6})^2 \cdot (5)^2 \cdot \; 740\times10^3} = \frac{2.82\times10^{-6}}{1.85\times10^{-3}}$$

$$\times \frac{73\times10^6}{2300} = 484$$

Estimated power $= 484 \times 0.62 \rightarrow$ 303W (actually ~250W). (2)

4004 Gates = 595

i2 Gates = 23×10^6

$T = k G^p$

4004 $T = (595)^{0.45} \times 0.8 = 14$.

$T = (23\times10^6)^{0.45} \times 0.8 = 1640$ (2)

Packaging material – Very high power dissapation – need ceramic to withstand this. Plastic unsuitable (1)

package type – Very high terminal count – requires a dense 2D array – Ball or pin grid array (actually uses a 1366 pin Land grid array) – largest (1)

(7) Q4-3

of its type presently available.

Interconnect method. This is high speed and very high interconnect density. Also power dissipation is very high. These criterion lead us to the use of flip chip (1)

Solder bumps on the reverse side of the IC are bonded on to the LGA package.

Thermal management needs to deal with high heat loading

Die attach to copper heatsink, using high conductivity epoxy (1)

Heat sink finned to increase surface area.

Forced air cooling via fan on heat sink or fan assisted air flow duct.

d) Accelerated testing

Tested under higher than normal conditions (one or more parameters) - high temp, Voltage, humidity, ESD, current, thermal stress etc.

Failure rate accelerated by enhanced conditions (2)

Enables life testing in a reasonable time for which

(a) Q4-5

we can then relate the failure rate back to that at normal operating conditions

Many semiconductor devices have lifetimes $\gg 10^4$ hours. This is more than 1 year. However if the dependences are known, or implied from previous work we can do accelerated testing over a much shorter timescale and imply from this the lifetime under normal operating conditions.

HAST - Highly accelerated steam and temperature

120°C, 85% Rel. Humidity, 100% Rated bias, 100 hours.

The test is particularly designed to accelerate corrosion

As the name suggests, this is highly accelerated (extreme) conditions - designed to show quickly any defective elements of the package assembly and provide rapid feedback such that corrective actions can be taken. If the device is degraded by corrosion, fundamental changes may be needed to the metallisation + interconnect scheme and it is better these are done sooner rather than later. (2)

Mean time to failure.

$$t_f = t_{f_0} \exp\left[-\frac{E_a}{kT}\right].$$

Two different temperatures T_1 and T_2

$$\frac{t_{f_1}}{t_{f_2}} = \exp\left[\frac{E_a}{k_B}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]\right] \qquad T_1 = 293K \quad T_2 = 393K$$

$\frac{e}{k_B} = 11604$ then use E_a in eV.

(10)

94-6

$= \exp\left[11604 \times 0.75 \left[\frac{1}{293} - \frac{1}{393}\right]\right]$

$\exp\left[11604 \times 0.75 \times 868 \times 10^{-4}\right]$

$\exp[7.558] = 1916.$

So 50 hours at 120°C → 95,800 hours at 20°C.

(2)