Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (2.0 hours)

EEE119 Digital System Engineering

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. i) Draw a truth table for the following Boolean function:

$$F(A,B,C) = AB + C$$

(2)

ii) Express the function **F** as a fundamental product of sums. **(2)**

b. i) Show how four D-Type flip-flops can be connected to form a ring counter. Describe, with a table of sequential values, the operation of this counter and any initial conditions required. **(4)**

ii) Show how the addition of a single logic inverter can be used to turn this into a twisted ring counter. Describe, with a table of sequential values, the operation of this counter. **(4)**

iii) The flip-flops used have a propagation delay of 20ns, a set-up time of 5ns and negligible hold-time, the inverter has a propagation delay of 15ns. What is the maximum theoretical frequency of operation for each counter? **(3)**

c. In a certain digital system, two square waves are required with a frequency of 10Mhz and a 75% duty cycle but phase shifted by 25ns. Show how this can be achieved using 4-bit ring counters. **(5)**

2. a. Describe the difference between:

i) Mealy and Moore type finite state machines.
ii) Binary and one-hot encoding.
iii) Setting and not-resetting sequence detectors. **(6)**

b. A Moore type state machine is required that can recognize certain sequences on its serial input line. It has a single bit output **Z** and a single bit input **I** which receives the serial input sequence. The circuit will recognize the pattern **101** and respond by setting **Z** = 1 for one clock cycle. It should not reset after finding a valid sequence.

Draw a state diagram for this system and a state transition table, clearly labelling the states. A circuit implementation and next state equations are **not** required. **(10)**

c. The sequence detector in part (b) uses a finite state machine to detect the pattern **101** with non-resetting behaviour. Show how this could be achieved using a shift register and some additional combinational circuitry. Could this circuit be used if resetting behaviour was required? Explain your reasoning. **(4)**

3. **a.** Write down the truth table for a two input OR gate and show how it can be implemented using only two input NAND gates. **(4)**

b. **i)** Explain, with the aid of a truth table, the function of a 2-to-1 logic multiplexer. **(4)**

ii) Derive a logic circuit for a 2-to-1 logic multiplexer and draw the circuit. Describe any static timing problems that may be present in your circuit. **(6)**

c. Draw the truth table for the Boolean function **F** given below. Hence, show how it can be implemented using only an 8-to-1 multiplexer and a logic inverter.

$$\mathbf{F(A,B,C,D) = \Pi\ (1,3,4,5,8,13,14)}$$ **(6)**

4. **a.** Derive the simplest Boolean equations that describe the operation of a single-bit full adder. Make sure that the two data inputs, *A* and *B*, the carry-in bit C_i, the sum output *So* and the carry-out bit C_o are clearly shown.

Show how this function could be implemented using a 3-to-8 line decoder with active low outputs and some simple logic gates. **(10)**

b. **i)** Draw the state diagram and state transition table for a 2-bit, binary synchronous down counter. **(4)**

ii) Describe the operation of a T-type flip-flop. **(2)**

iii) Hence, show with a circuit diagram, how the counter can be implemented using T-type flip-flops plus some combinational logic gates. **(4)**

NJP/RAH/PIR