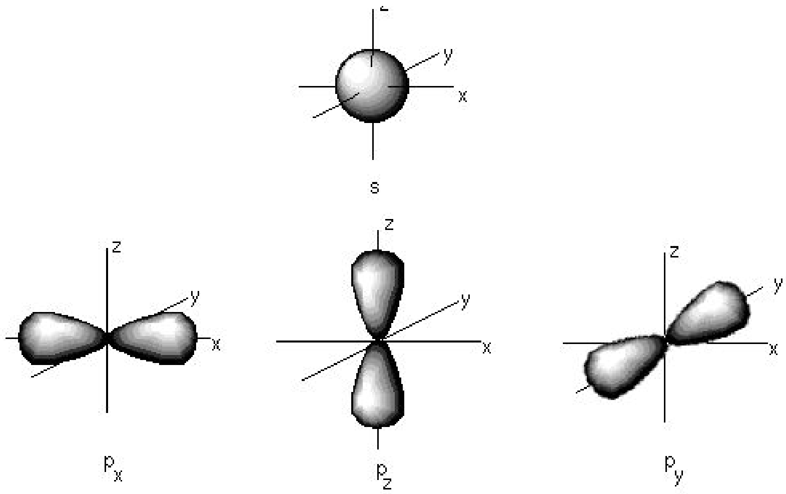
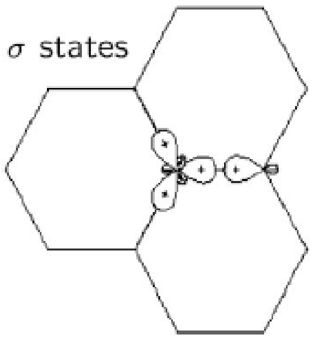
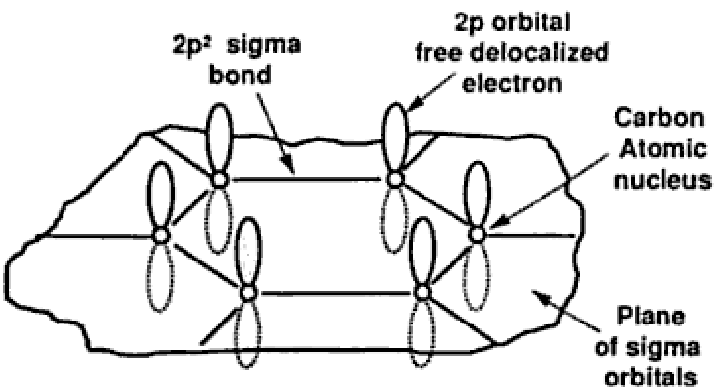
Solutions of EEE6213: 2015-16.

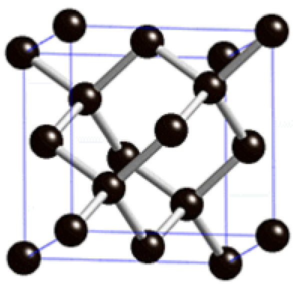
1a.



(1+1)

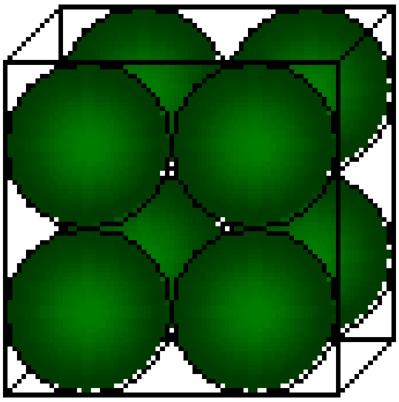
S and p orbitals respectively.

	
SP2 bonding (1)	Example: Graphene. (pic) or CNT (1/2)

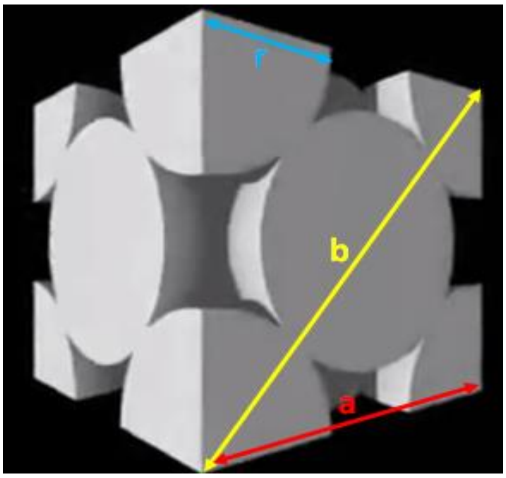
	
SP3 bonding (1)	Silicon, GaAs. (1/2)

b) Show diagram for calculations indicating the dimensions for r and “a” the lattice constant.

Simple Primitive:



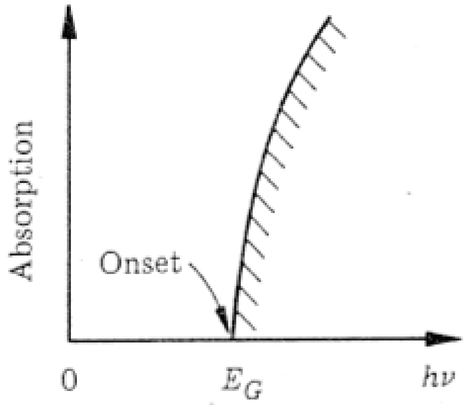
$$\frac{8\times\frac{4}{3}\pi r^3}{(4r)^3} = \frac{\frac{32}{3}\pi}{64} = 0.524 = 52.4\%$$

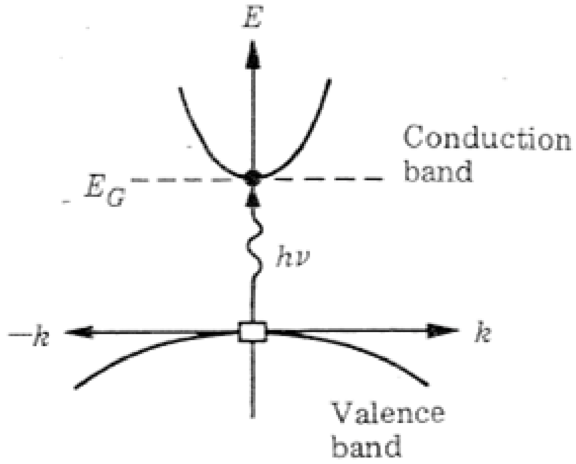


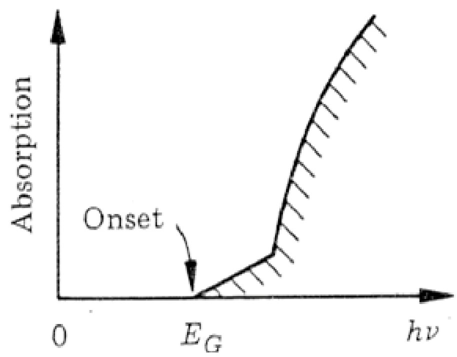
$$\frac{4\times\frac{4}{3}\pi r^3}{\left(2\sqrt{2}r\right)^3} = \frac{\frac{16}{3}\pi r^3}{16\sqrt{2}r^3} = \frac{\pi}{3\sqrt{2}} = 0.740 = 74.0\%$$

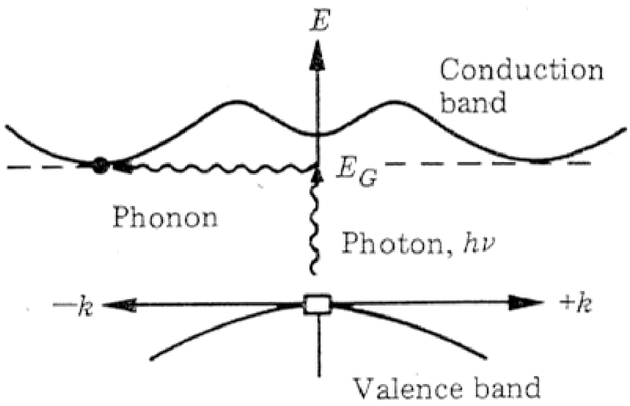
(5)

c). Energy versus momentum of carriers which shows the bandstructure of the material.

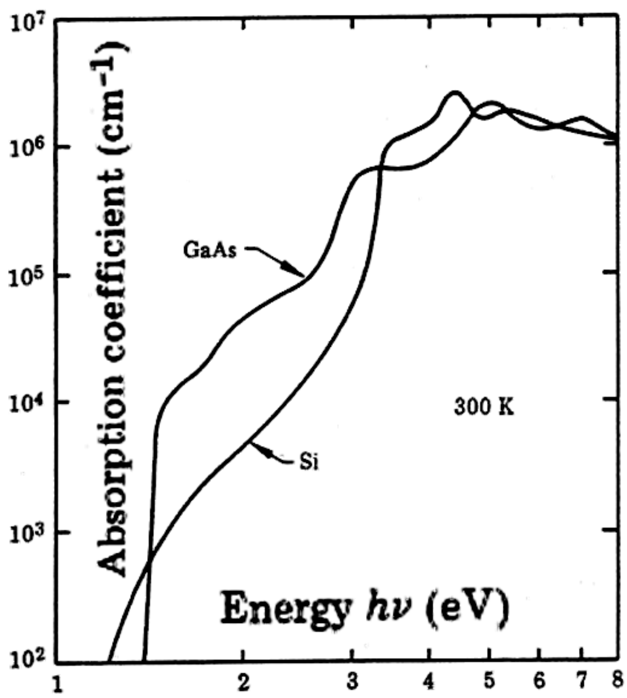








Direct and indirect bandgap materials identified by a response of the absorption spectra as shown in the diagrams for the onset in diagram below.



(5)

d) **i)** Boron is an acceptor in Si, so the material is **p-type** with $\boldsymbol{p = N_A = 2 \times 10^{16}}$ **cm^{-3}** and electron concentration $\boldsymbol{n = n_i^2/p = 5 \times 10^3}$ **cm^{-3}**. (2.5)

ii) Phosphorus is a donor in Si. Since $N_D > N_A$, the material is **n-type**.

The carrier concentrations are determined by the net dopant concentration,

$N_D - N_A = 4 \times 10^{16}$ cm^{-3}, so that $\boldsymbol{n = 4 \times 10^{16}}$ **cm^{-3}** and $\boldsymbol{p = n_i^2/n = 2500}$ **cm^{-3}**. (1.0)

The material is strongly n type. The resistivity is therefore approximated as

$$\rho = 1/(nq\mu_n + pq\mu_p) = 1/nq\mu_n$$

=1/(4x10^{16}x1.6x10^{-19}x820)= 0.19 ohm-cm. (1.5)

2.=

a) In order for the resistance ($R=\rho L/Wt$) of a semiconductor region to be no larger than 100 ohms, its **resistivity must not exceed** $100 \cdot Wt/L = 100\Omega \times 100\text{nm} \times 2\text{nm}/10\text{nm} = 2000\ \Omega\text{-nm} = \boldsymbol{2 \times 10^{-4}\ \Omega\text{-cm}}$.

For n type silicon, N_A=0.

$$\rho = \frac{1}{nq\mu_n + pq\mu_p} = \frac{1}{nq\mu_n}$$

2x10^{-4}=1/(nx1.6x10^{-19}x820).

n=3.8x10^{19}/cm^3. (5)

b. MBE layers can be grown at *lower temperatures* than for MOCVD; MBE is not limited by precursor decomposition kinetics;MOCVD employs a *simpler technology* than MBE;MOCVD does not require advanced DRV technology but, MOCVD does need substantial toxic gas handling facilities

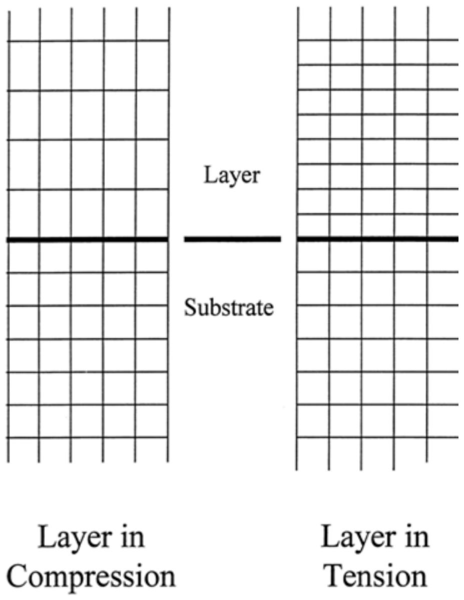
Properties required of reagent materials in an MOCVD

- Should have ***high volatility***-makes possible high layer growth rates
- Should have a ***low tendency to decompose homogeneously***-only decomposes heterogeneously on substrate (or it will form in gas and rain particles)
- Should ***eliminate carbon*** as completely as possible when cracking upon the substrate surface (certain temp regime, Si will be n type. Depends upon skill)-avoids problem of carbon doping (p) of grown material
- Should be available with very high purity-otherwise unwanted impurities can be incorporated into a growing layer

(5)

2c. Heteroepitaxial pseudomorphic growth is where two different epitaxial layers are grown on top of each other, such that the lattice contant of the layer at the top “fits” with the layer at the bottom, thus introducing strain.

If the lattice mismatch is relatively small <1.5%)- It results in tetragonal distortion of cells on the top layer. (1)



(5)

d) The crucible free technique gives wafers with very low O2 concentration. Melt zone stability is enhanced.

Molten Boric oxide seals the melt against loss of Gr V material.

Advantage: Very low dislocation densities. (5)

3.a

$$C_S = k_0 C_0 (1-x)^{k_0 - 1}$$

30*Co=0.3C0(1-x)^0.3-1; k0=0.3

Gives -2/0.7=log(1-x)

Gives x=1-0.00141=0.99859. (5)

3b.MOS Capacitor Energy Band Diagrams **(10 marks 2.5 each)**

Since the substrate is n-type, this is a PMOS capacitor, *i.e.* a sufficiently large negative gate voltage is required to deplete the semiconductor surface of mobile electrons and form an inversion-layer of holes there.

(i)Assuming that the n-type Si substrate is non-degenerately doped, its work function is the difference between the vacuum level and the fermi level.

The fermi level is 0.08 below Ec ie (0.56-0.08)=0.48 eV from midgap.

Therefore $\Phi_S = \chi + (E_C\text{-}E_F)$ = (3.1+0.95) + 0.08=4.05+0.08=4.13 eV. (2.5)

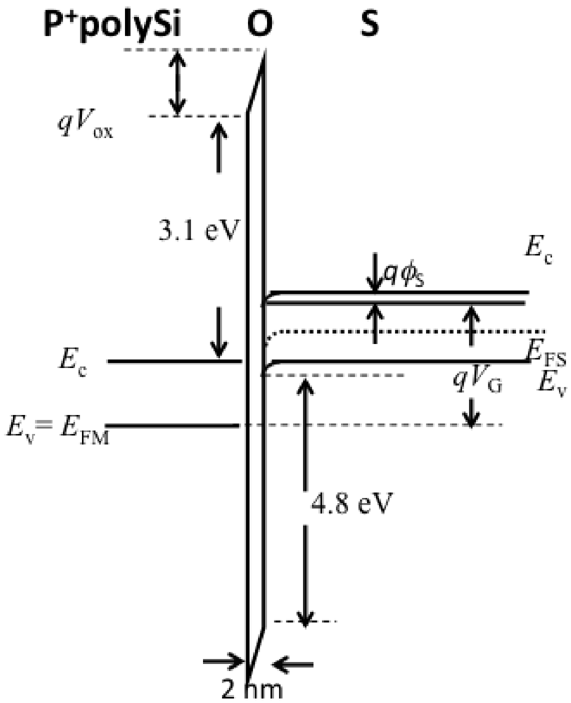
(ii)The flatband voltage is given by the difference between the gate and semiconductor work functions $qV_{FB} = \Phi_M - \Phi_S$

Thereofore 1.07= $\Phi_M - 4.13$

Gives Φ_M =1.07+4.13= 5.2 eV.
The gate material is heavily doped p-type silicon from the band diagram. (2.5)

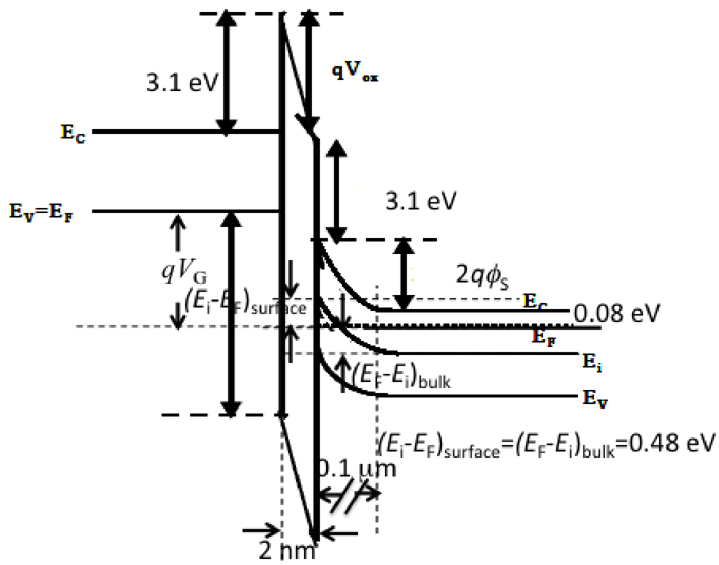
(iii)

i) Accumulation: $V_G > V_{FB}$ so that there are majority carrier electrons accumulated at the Si surface



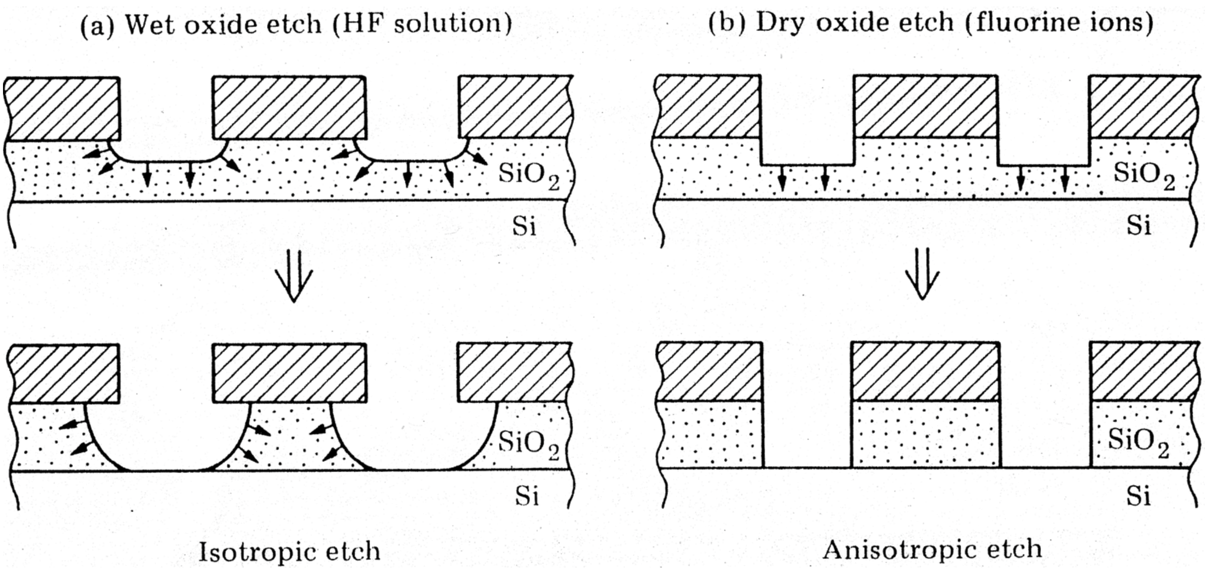
(2.5)

ii)Strong inversion: V_G is more negative than the threshold voltage V_T, so that the surface is strongly p-type, *i.e.* with a (mobile) hole density greater than the (immobile) density of ionized



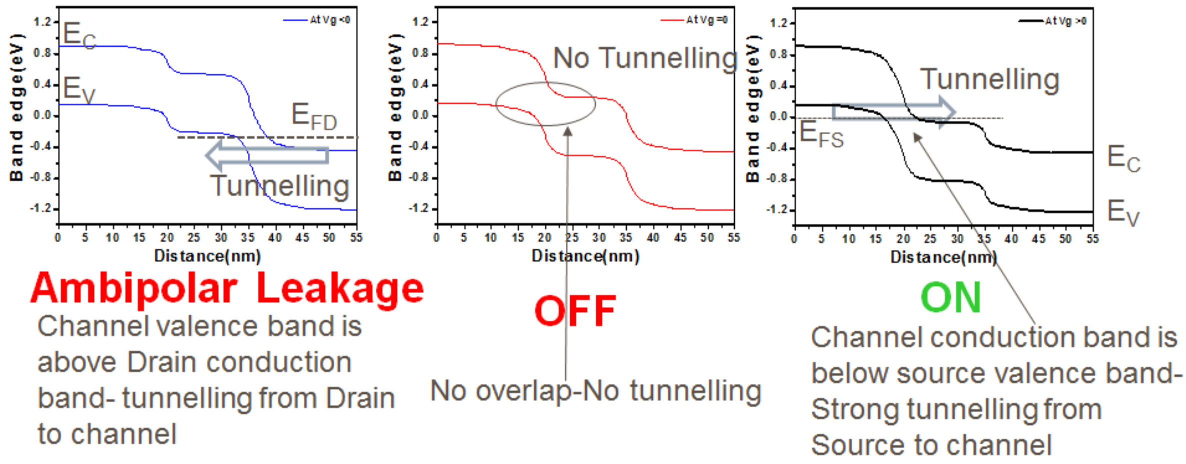
(2.5)

c) Wet etching is isotropic and undercuts the resist. Dry etching is anisotropic and has vertical walls closest to mask pattern. (5)



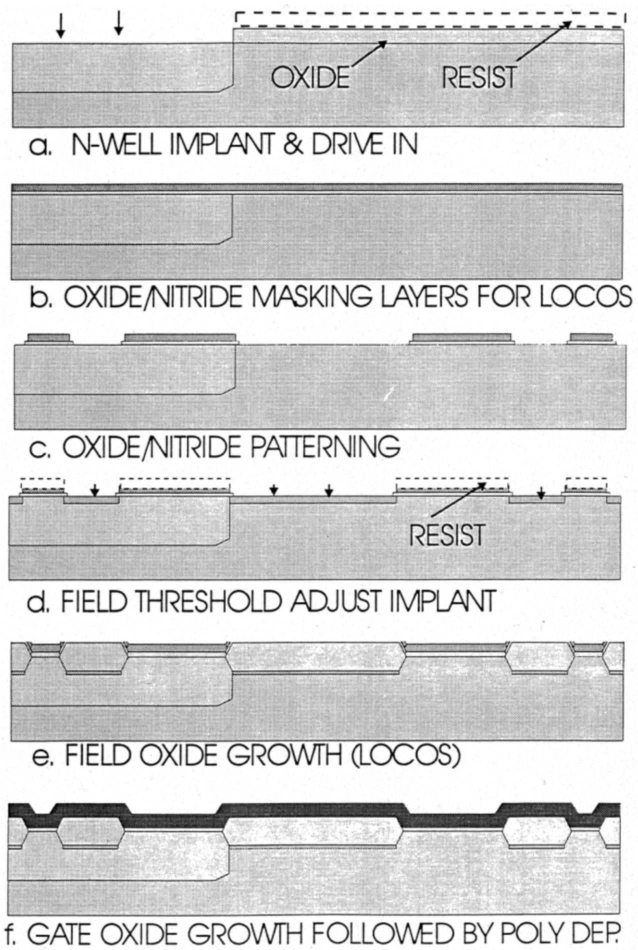
(a) Wet oxide etch (HF solution)
SiO2
Si
SiO2
Si
Isotropic etch
(b) Dry oxide etch (fluorine ions)
SiO2
Si
SiO2
Si
Anisotropic etch

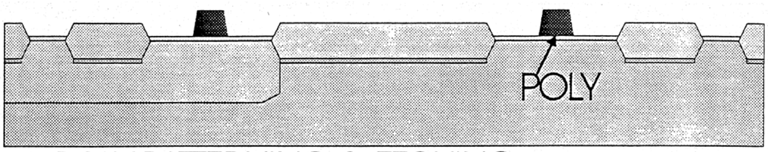
Q4.a



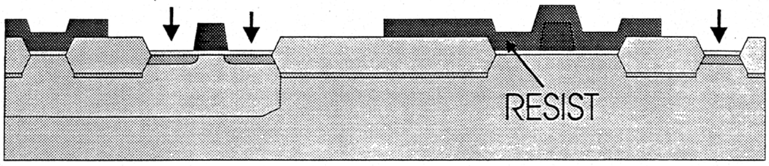
(10)

b) Conventional CMOS process as outlined.

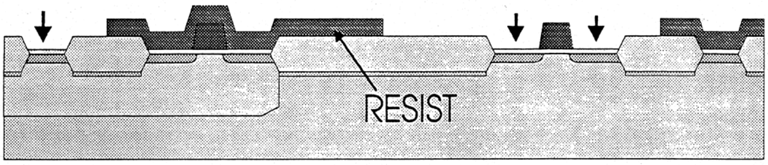




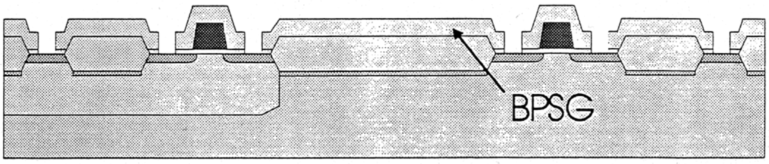
g. POLY PATTERNING & ETCHING



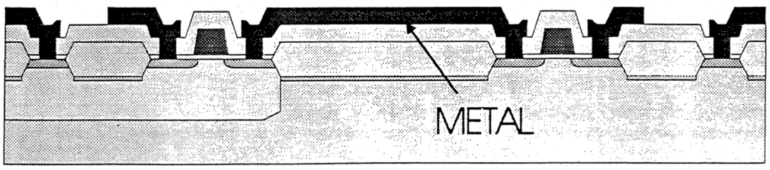
h. RESIST MASK FOR P+ SOURCE & DRAIN IMPLANT



i. RESIST MASK FOR N+ SOURCE & DRAIN IMPLANT



j. .BPSG DEPOSITION & CONTACT WINDOW ETCH



k. METAL DEPOSITION AND ETCH

N Well implant and drive in; Oxide/nitride masking layers for LOCOS; oxide nitride patterning, field threshold adjust implant, field oxide growth (locos);gate oxide growth and poly deposition ;poly patterning and etching;resist mask and p+ source and drain implants (B),resist mask and n+ source and drain implants (As);BPSG deposition and contact window mask and etch, metal deposition and etch.

(i) LOCOS thick oxidation layer for isolation.

(ii) Threshold adjust field implant to raise the threshold of parasitic MOS devices, across the field oxide, so that they will not become active during IC operation

(iii) Self aligned process: Source/drain implanted to gate as mask, no additional mask.

(10)- ***of which 3 marks for getting the sequence correct, 3 marks for diagrams and 4 for content, 1 each question right.***