EEE6070 Answers_06-07

1(a) The electronic configuration of the Si atom is $1s^2 2s^2 2p^6 3s^2 3p^2$. When the atom is bonded into the Si diamond cubic lattice, the outer electrons occupy four tetrahedrally disposed sp^3 hybrid orbitals. These overlap with orbitals of adjacent atoms and each bond, so formed, has two electrons, one each from the atoms on either end of the bond. The bond energy depends upon the interatomic separation as described by a Morse curve (diagrams needed).

1(b) Plane spacing $d_{hkl} = a_0 / \sqrt{(h^2 + k^2 + l^2)}$

For (002) $d_{002} = 0.5522/\sqrt{(0 + 0 + 4)}$nm
$= 0.2761$nm

For (112) $d_{112} = 0.5522/\sqrt{(1 + 1 + 4)}$
$= 0.2254$nm

For (212) $d_{212} = 0.5522/\sqrt{(4 + 1 + 4)}$
$= 0.1841$nm

For (114) $d_{114} = 0.5522/\sqrt{(1 + 1 + 16)}$
$= 0.1302$nm

1(c) Angle between planes $(h_1k_1l_1)$ and $(h_2k_2l_2)$ is given by
$\cos^{-1}[(h_1h_2 + k_1k_2 + l_1l_2)/\sqrt{((h_1^2 + k_1^2 + l_1^2)(h_2^2 + k_2^2 + l_2^2))}]$

$(001) \wedge (011) = \cos^{-1}[1/\sqrt{2}] = 45.0^o$
$(111) \wedge (112) = \cos^{-1}[4/\sqrt{18}] = 19.5^o$

1(d) Diagrams are required to show that an intrinsic stacking fault has a missing (111) plane section, whilst an extrinsic stacking fault has an extra (111) plane section. The twin diagram must show reversed stacking on a set of {111} planes.

1(e) A diagram of a tilt grain boundary showing edge type dislocations is required. Other types of grain boundary are the twist boundary and the mixed boundary. The twist boundary contains only screw dislocations.

1(f) Resistance of track $= 0.4(\text{length/width})\ \Omega$

Resistance (1μm) $= 0.4(3 \times 10^{-1}/10^{-4})\ \Omega$

$= 1.2 \times 10^3\ \Omega$

Resistance (5μm) $= 0.4(3 \times 10^{-1}/5 \times 10^{-4})\ \Omega$

$= 2.4 \times 10^2\ \Omega$

2 (a) **Chemical Vapour Deposition (CVD) of Epitaxial Si**

Several types of reaction involving Si-containing gases flowing over a heated substrate are possible

most important is the hydrogen reduction of silicon tetrachloride, which takes place on the heated surface

$$SiCl_4 + 2H_2 = Si + 4HCl$$

deposited Si atoms run around on the substrate and join steps at the edges of growing crystal planes extending across the surface

the deposition temperature is generally in the range 800-1200 C in order to give high quality, single crystal Si layers, with good thickness uniformity, at deposition rates in the range 0.01-5μm/min

prior to deposition, substrates would typically be given a vapour etch with flowing HCl or a bake in H_2 gas to clean their surfaces

A typical CVD apparatus has appropriate reagent and other gas lines feeding into a mixing manifold leading to the reaction chamber (diagram required)

the chamber generally has one of three generic designs, horizontal reactor, pancake (vertical) reactor and barrel reactor (diagrams required)

susceptor has wafers mounted upon it and is heated by RF coupling or by radiant heating from quartz halogen lamps

susceptor is often graphite coated with SiC since this will not react with any gases or introduce contaminants

gas flow in chamber must be very uniform to give layer thickness uniformity on each of the substrate wafers

Doping of grown layers is achieved by mixing a suitable hydride with the flowing hydrogen and $SiCl_4$ gases

arsine (AsH_3) or phosphine (PH_3) for n-type doping and diborane (B_2H_6) for p-type doping

must be careful to avoid so-called autodoping

diffusion of impurity from substrate must be outpaced by layer growth: can be checked by calculating the characteristic impurity diffusion length

The quality of epitaxial Si films must be high if they are to be employed for IC fabrication

if residual contamination is present on the substrate surface before epitaxy, stacking faults or even small pyramidal hillocks may be produced

nonuniform heating of the wafers can lead to slip and dislocation formation

(b) Diffusion coefficient (D) = $D_0 \exp -[E_A/kT]$

At 1100°C (1373K) $D = 0.76 \times \exp -[3.46/(8.62 \times 10^{-5} \times 1373)]$ cm^2/s

$= 1.53 \times 10^{-13}$ cm^2/s

For 60s $2\sqrt{(DT)} = 2\sqrt{(1.53 \times 10^{-13} \times 60)}$ cm

$= 6.06 \times 10^{-6}$ cm

$= 0.06\mu m$

This diffusion length is much less than the thickness of the Si layer grown per minute, therefore, autodoping of the layer should not be a serious problem

(c) Si and sapphire exhibit a very large misfit. The Si layer grows first in an islanded form and, due to the misfit, large numbers of strain-relieving defects are introduced. The latter include misfit dislocations, stacking faults and twins.

Si on sapphire can be employed where well isolated electronic devices are required. Isolation is produced by etching away the Si between the devices down to the level of the sapphire.

(d) (i) For the deposition of polycrystalline Si the growth temperature must be reduced towards about 600C.

(ii) For the deposition of amorphous Si the growth temperature must be reduced to somewhat below 600C.

3a) **Bipolar Transistor Fabrication**

The following fabrication steps are required:

- (a) n^+ buried layer formed by As^+ ion implantation followed by n-layer epitaxial growth
- (b) pad oxide/nitride growth with isolation resist applied
- (c) oxide/nitride etch and channel-stop B^+ implant (to overcome B depletion in the substrate during subsequent oxidation)
- (d) isolation oxide growth, remaining nitride removal
- (e)base B^+ implant through resist window
- (f) opening of base, emitter and collector contacts through resist window
- (g) emitter and collector contact areas selected by resist window for final As^+ implantation to give n^+ surface regions
- (h) finally, device passivated with layer of Si_3N_4, contact windows reopened and metallized

(diagrams required at the various stages)

- ***Special considerations*** for bipolar fabrication

- the initially-formed ***buried n^+ layer*** reduces the collector resistance

- the ***epitaxial layer*** should be as lightly doped as possible to minimise base-collector capacitance, with the constraint that the doping must be heavy enough to give low collector resistance

- the ***base width*** must be as narrow as possible to minimise the transit time for minority electrons (reducing hole-electron recombination and increasing transistor frequency response) while being doped heavily enough to withstand the reversed-bias collector/base voltage (avoiding punch-through current). The base contact area will also benefit from being more heavily p-doped, but this requires additional process steps

- the ***emitter*** must be as heavily doped and as shallow as possible to minimise emitter resistance. Also the transistor gain is determined by the minority carrier (hole) gradient in the emitter, since this establishes the base current. Thus, the gain can be increased by decreasing the hole gradient through use of heavily n-doped polySi to contact the emitter: this increases the hole lifetime compared to the use of metal and has been widely exploited for this purpose

▸Bipolar and CMOS transistor fabrication technologies are combined in BICMOS processing

- allows ICs with circuits containing both device types to be produced yielding advantages of merged functionality
  - however, processing is more complex and costly than for CMOS alone

3b) Diffusion coefficient (D) = $D_0 \exp -[E_A/kT]$

At 1200°C (1473K) $D = 12 \times \exp -[4.05/(8.61 \times 10^{-5} \times 1473)]\ cm^2/s$

$= 12 \times \exp -[31.94]\ cm^2/s$

$= 1.61 \times 10^{-13}\ cm^2/s$

For 30min $2\sqrt{(DT)} = 2\sqrt{(1.61 \times 10^{-13} \times 900)}\ cm$

$= 2.4 \times 10^{-5}\ cm$

$= 0.24\mu m$

4(a) **Thermal Oxidation of Si**

▸One of the key steps in the fabrication of Si semiconductor devices and ICs

▸Oxidation of Si is carried out in a ***furnace*** at, typically, 900-1200°C: two methods ***University of Sheffield***

- •oxidation with dry oxygen gas (***dry oxidation***)

  $Si + O_2 = SiO_2$

- •oxidation with steam (***wet oxidation***) - a faster process

  $Si + 2H_2O = SiO_2 + 2H_2$

▸Reaction kinetics

- •there are ***three steps*** in the oxidation process
  - ◦the oxidising species is ***transported*** from the bulk of the gas to the oxide/gas interface

    flux = $h_G (C_G - C_S)$ [h_G is mass-transfer coefficient]
  - ◦the oxidising species ***diffuses*** across the oxide layer already present

    flux = $D (C_0 - C_i)/x_0$ [D is diffusivity in oxide]
  - ◦the oxidising species ***reacts*** with the Si at the oxide/Si interface

    flux = $k_s C_i$ [k_s is reaction rate constant]
- •the rate determining step depends upon the oxide thickness (x_0)
  - ◦for ***small*** x_0, there is a large oxidising species flux across the oxide layer and the reaction at the oxide/Si surface is rate-limiting
  - ◦for ***large*** x_0, the flux across the oxide is small and this diffusion step is rate-limiting
- •combining the above equations and determining the rate of change of x_0, it is found that
  - ◦for small x_0, the rate of oxidation is ***linear***
  - ◦for large x_0, the rate of oxidation is ***parabolic***

- •MOSFET ***gate oxide integrity*** (GOI) is a vital parameter and it is adversely affected by
  - ◦***roughness/nonuniformities*** of the oxide thickness
  - ◦pre-existing ***particles*** of eg silica present in the Si which protrude into the gate oxide
  - ◦***transition element contamination*** giving deep levels in the Si or even precipitation/segregation at the Si/oxide interface

▸The effects of HCl additive

- •presence of HCl (giving Cl_2 by reaction $2HCl + ½O_2 = H_2O + Cl_2$) also ***increases*** the reaction rates
  - ◦HCl ***reduces metal contamination*** of the grown oxide due to the formation of volatile chlorides: both alkali metals (Na, K, etc which form charged ions that are mobile under bias even near room temperature) and transition elements are removed
  - ◦the use of HCl suppresses ***stacking fault formation*** in the Si during oxidation and also makes the precipitation of transition elements less likely.

4(b) **Deposition of Insulating Layers**

- ***Chemical vapour deposition*** of SiO_2 and Si_3N_4
  - at ***atmospheric pressure*** (APCVD) giving high deposition rates at relatively low temperatures
    - relatively poor layer uniformity and step coverage; higher contamination
  - at ***low pressure*** (LPCVD) with larger molecule mean-free-path giving better layer uniformity and step coverage, together with better purity
    - higher temperature deposition and lower deposition rates
  - with ***plasma enhancement*** (PECVD) giving fast deposition at low temperatures
    - some chemical and particulate contamination
- SiO_2 films
  - often formed by the ***pyrolytic oxidation*** of alkoxysilanes (eg tetraethylorthosilane (TEOS)) $Si(C_2H_5O)_4 + 12O_2 = SiO_2 + 8CO_2 + 10H_2O$
    - films may be poor quality due to incorporation of by-product water and are in compression
  - can be formed by reaction of silane with oxygen
    $SiH_4 + O_2 = SiO_2 + 2H_2$
    - better quality but may require densification: films are in tension
    - with simultaneous pyrolysis of phosphine, silica doped with phosphorus (***phosphosilicate glass***, PSG) is produced
      PSG has ***lower built-in stress*** and an increased thermal expansion coefficient giving a better match to underlying semiconductor and enhanced film stability
- Si_3N_4 films
  - typically deposited by LPCVD and PECVD by combination of either silane or dichlorosilane with ammonia
    $3SiH_4 + 4NH_3 = Si_3N_4 + 12H_2$
    $3SiCl_2H_2 + 4NH_3 = Si_3N_4 + 6HCl + 6H_2$
  - films often used for their ability to block diffusion of both water and sodium
    - widely used in both Si and GaAs technology
  - films may be ***highly stressed*** depending on method of deposition

5(a) **Structure of the Scanning Microscope**

- Electron-optical column, with electromagnetic lenses, maintained under high vacuum
  - extensive signal handling (processing) and display electronics
- Electron gun similar to that of TEM
  - typically W hairpin, LaB_6 or field-emission electron sources
  - accelerating voltages up to typically 30-50keV
- Electron beam formed into ***fine spot*** (sometimes down to <2nm) by lens and aperture system
  - passed through scan coils to deflect the spot in a raster over specimen held on high-accuracy goniometer stage
  - incident electrons in the spot interact with the specimen throughout a scattering volume which increases with increasing beam voltage
    - Monte Carlo simulations demonstrate this

- ***Signals generated*** by interaction of incident beam with specimen surface regions are principally:
  - secondary electrons
    - typically 0-50eV energy
    - detected using eg scintillator/PMT
  - backscattered electrons
    - typically near primary beam energy
    - detected using eg solid-state diode
  - induced currents
  - visible, UV or IR photons
  - X-rays
- Specimen can be imaged or analysed using any of these signals
  - image formed on CRT display modulated by signal and scanned in synchronism with the specimen
  - advantage of SEM is that specimens usually require little special preparation (ie no thinning as for TEM)
    - electrical charging may be problem for insulating materials: coating with very thin film of C or Au can overcome this

5(b)i) **Electron Emissive Mode**

- ***Secondary electron (SE) image*** shows surface structure and topography, often with excellent visualisation of ***3D relief***
  - very large ***depth of field***: up to 300x that of light optical microscope
    - due to relatively ***small beam divergence*** angle ($\sim 10^{-2}$-10^{-3} rad)
  - bright/dark shading in the image gives the ***3D appearance***
    - due to angle between the primary beam and detector directions: the object itself screens some emitted electrons from the detector
  - resolution down to ~2nm possible with ultrasmall spots and thin samples (to minimise size of scattering volume)
  - SE imaging used widely in electronics industry for routine imaging of devices
- ***Backscattered electron (BS) image*** also shows specimen surface topography and, in addition, carries information about sample ***atomic number*** and crystal structure
  - as the elemental atomic no (Z) increases, so does the efficiency of electron backscattering
    - the intensity of the BS image increases with specimen atomic no
    - local areas of different elements, in principal, can be distinguished (so-called ***Z-contrast***) and elemental maps can be produced
  - for a crystalline specimen, so-called channelling or Coates patterns useful for assessing crystallinity of sample can be produced

ii) Charge Collection Mode

- The basic current supplied by the beam, passing through the sample, can also be used for imaging
  - gives a so-called ***absorbed current*** image complementary to SE and BS images (these signals are removed from the measured current)

- If an electrical barrier, such as a p-n junction, a Schottky barrier (contact) or a heterojunction, is present in the specimen, a current is produced in an external circuit when the beam scans the barrier
  - ***electron beam-induced conductivity*** (EBIC) signal produced as beam-induced carriers (electrons and holes) are swept apart by the internal field
    - variations in barrier (junction) properties are revealed as contrast changes: important for ***device inspection***
    - electrically-active defects in the junction region lower carrier lifetime and, hence, reduced EBIC signal
      - ***defects give EBIC contrast*** in scanned image and can be detected and studied

iii) Voltage Contrast

- SE detector is modified in order to allow selection of electrons of different energies
  - possible to observe or measure small differences of electrostatic potential over probed surface
    - ***voltage contrast*** is obtained due to change in escape probabilities for secondary electrons across their energy range
    - ***quantitative*** variations in contrast allow measurement of voltages at specific points in operating ICs: ***e-beam testing***
  - when IC voltage is static, only a static measurement is needed
  - when IC voltage varies, observation/measurement must be electrically gated in-phase with the IC signal
    - ***stroboscopic voltage contrast***

iv) Cathodoluminescence Mode

- Optical photons ***(cathodoluminescence***) emitted by irradiated specimen collected and analysed
  - eg, a parabolic mirror over the specimen collects the light and directs it either into a PMT, or, into a spectrometer/detector system
    - system must have high efficiency since signals are often low
  - allows formation of 'total light' images or emission spectra and wavelength-selected images
    - provide detailed, spatially-localised assessment of semiconductor ***electronic and optical properties***
  - example of assessment of quantum wires formed by growth in V-grooves

v) X-Ray Microanalysis

- X-rays emitted by irradiated specimen collected and analysed
  - X-ray detector gives ***spectrum*** of photon intensity vs photon energy
    - ***energy-dispersive detector*** (in common use) gives parallel collection but with relatively poor energy resolution and peak/background ratios
      - cooled Li-drifted Si p-i-n diode
    - ***wavelength-dispersive detector*** gives only serial collection but with much higher spectral resolution and excellent peak/background ratios
      - crystal-diffraction spectrometer with proportional counter
  - presence of ***characteristic X-ray spectral peaks*** is used to detect presence of specific elements: peak amplitudes give quantitation

◦***spatial resolution*** ~0.1-1μm for bulk specimens
◦***sensitivity*** ~0.1-1% for energy-dispersive detector

6(a) **Stereographic Projection**

▸Enables crystal planes and, for cubic system, directions to be plotted and conveniently related to one another in a ***projection plane***

▸Projection is carried out by first constructing a sphere and inserting the ***projection plane*** as the horizontal diametrical plane

▸Next, the crystal (cubic) is placed at the centre of the sphere and normals to its lattice planes are constructed from the centre outwards to intersect the sphere at particular points

▸The latter points in the upper half of the sphere are then connected to the South Pole and where the resulting lines pass through the projection plane are the projected representations (***poles***) of the original crystal planes

▸points on the lower half of the sphere can be similarly projected upwards to the North Pole

6(b) ▸***Overall symmetry of crystal***
•on (001) projection, equivalent planes are separated by 90° rotations
◦four-fold symmetry as expected for cube face

▸***Arrangement of groups of planes***
•on (001) projection, eg (102), (101) and (201) lie between (001) and (100): also eg (112), (111) and (221) lie between (001) and (110)
◦each such set of faces constitutes a ***zone***: definition - a set of planes whose mutual intersections are all parallel
◦the common direction of the intersections in a particular zone is the ***zone axis***

▸***Measurement of angles between planes***
•use a ***Wulff net*** calibrated in angle placed over the projection
◦shows small circles and great circles graduated in degrees
•place net so that the two poles of the planes lie on the same ***great circle***
◦measure the angle between the poles

6(c) **X-Ray Sources**

▸In the laboratory, X-rays conveniently obtained by bombarding a metal target (anode) with electrons
•evacuated tube with water-cooled metal anode
◦rotating anode arrangement for very high intensity X-ray generation
•Cu typically target material, giving CuKα doublet with $CuK\alpha_1$ wavelength approx 0.154nm

- the intense X-ray emission from an electron synchrotron may also be employed
  - to reduce beam divergence beam passed through lead collimator and then diffracted off accurately planar and highly polished single crystal surfaces

X-Ray Diffraction

- When X-rays (wavelength λ) scatter from crystals, they diffract from crystal planes as determined by ***Bragg's law***
  - for planes {hkl} of spacing d_{hkl}

$$n\lambda = 2d_{hkl}\sin\theta_B$$

    - the Bragg angle (θ_B) will typically be at least tens of degrees (cf electrons)
  - X-rays detected typically using a proportional counter or scintillator/PMT, either situated behind a slit/collimator arrangement

(2 of the following four uses)

- ***X-ray powder diffraction*** is used to identify the crystalline phase(s) in a powder sample
  - X-ray powder diffraction plots obtained: intensity vs $2\theta_B$
    - related to d_{hkl} values and then phase(s) identified using tables
      examples for Si, ZnS (zinc blend) and ZnS (wurtzite)
- The ***crystallographic orientation*** of a single crystal surface can be determined
- ***Lattice parameter determination*** can be carried out
- ***Heteroepitaxial layer measurements*** can give the state of strain of a layer mismatched upon a substrate

X-Ray Topography

- The ***internal structure*** of semiconductors can be imaged using diffracted beams
  - ***Berg-Barrett topography*** (diagram required)
    - uses a static surface Bragg reflection
    - sample mounted on goniometer and oriented to obtain suitable Bragg reflection from surface: photographic plate exposed using diffracted X-rays
  - ***Lang transmission topography*** (diagram required)
    - camera synchronously scans the crystal and the photographic plate past a tall narrow beam of X-rays
  - ***Defect analysis***
    - defects in a crystal can be imaged and analysed using topography
      eg compare dislocations in LEC and Bridgman GaAs crystals

7(a) **Metal-Organic CVD (MOCVD)**

- layer growth takes place inside a ***reactor tube*** often made of quartz glass
  - substrate sits on a heated graphite susceptor
  - heating is by coupling of susceptor with RF
    coils may be asymmetrical to give uniformly heated zone

- ***Hydrogen high purity carrier gas*** passes through the reactor, transporting the reagent gases which it contains over the substrate

- flows of all gases and appropriate mixing is regulated by mass-flow controllers in a gas switching matrix
  - vent/run operation with zero differential pressure changes
- after initial in situ cleaning of the substrate by heating in flowing gas (with eg AsH_3 for GaAs), layer growth takes place at either atmospheric pressure or low pressure (perhaps approx150torr)
- ***reagent materials pyrolyse*** on the heated substrate to provide the epitaxial growth
- waste products from the reactor pass through various stages of processing, such that there are ***zero toxic emissions***

▸Properties required of reagent materials (precursors)
- should have ***high volatility***
  - makes possible high layer growth rates
- should have a ***low tendency to decompose homogeneously***
  - only decomposes heterogeneously on substrate
- should ***eliminate carbon*** as completely as possible when cracking upon the substrate surface
  - avoids problem of carbon doping of grown material
- should be available with ***very high purity***
  - otherwise unwanted impurities can be incorporated into a growing layer

▸***Group III precursors***
- most useful are trimethylaluminium
  trimethylgallium
  trimethylindium

▸***Group V precursors***
- most useful are: arsine (AsH_3)
  phosphine (PH_3)
  - the former is highly toxic and the latter is both toxic and pyrophoric

▸***Dopant precursors***
- the most general p-type dopant in III-Vs is ***Zn***: introduced as dimethylzinc
  - in Al-containing compounds, ***C*** dopant can be used: introduced as CCl_4
  - in GaN, only ***Mg*** is satisfactory: introduced as methylcyclopentadienylmagnesium
- the most general n-type dopant in III-Vs is ***Si***: introduced as SiH_4 or Si_2H_6

▸The ***MOCVD growth process*** involves interaction between the group III and group V species on the heated substrate surface after they have diffused across a stagnant gas boundary layer
- for the growth of GaAs:

  $$Ga(CH_3)_3 + AsH_3 \rightarrow GaAs + 3CH_4\uparrow$$

- the group V precursor is typically ***present in excess*** to compensate the high volatility of the element and to inhibit carbon incorporation
- MOCVD growth characteristics
  - growth rate is ***controlled*** by the group III precursor concentration
  - growth rate is ***little affected*** by the group V precursor concentration
  - growth rate depends upon the temperature in ***three regimes***
    increase at low temperatures due to speeding up of reaction kinetics
    intermediate regime limited by diffusion across boundary layer
    decrease at high temperatures due to desorption of group V element

7(b) Diagrams of compressive and tensile pseudomorphic layers required.

▸When the lattice parameters of the deposited layer and the underlying crystal cannot be accurately matched, the interface is then ***lattice mismatched***

▸If the lattice mismatch is relatively ***small*** (<1.5%), the growing layer can first adopt the in-plane lattice parameter of the crystal substrate

•however, the small difference in lattice parameter results in a ***tetragonal distortion*** of the unit cells in the growing layer

◦if the growing layer is compressed in-plane, the lattice constant normal to the plane increases slightly

◦if the growing layer is stretched in-plane, the lattice constant normal to the plane decreases slightly

•such epitaxial layers are described as ***pseudomorphi***c

▸Pseudomorphic layers can be grown only up to a certain thickness, due to the increasing excess energy stored in the distorted lattice

•above this ***critical thickness***, defects are introduced into the layer

◦these are often ***dislocations*** which may glide into the heterointerface to relieve the misfit and induce ***relaxation***

with a certain density of dislocations at the interface, the deposited layer can return to its equilibrium cubic lattice geometry

•for layers above the critical thickness dislocations can be introduced into the heterointerface by a number of different mechanisms

◦pre-existing threading dislocations are forced to bend over into the interface, whereupon they extend across the layer

the edge components of the Burgers vectors in the interface relax the strain - ***Matthews and Blakeslee mechanism***

◦if there are any inhomogeneities in the layer (precipitates, etc), local strain can produce dislocation loops which expand into the interface

so-called ***secondary sources***

▸If the lattice mismatch is relatively ***large*** (>1.5%), the sign of the lattice distortion determines the outcome

•if the grown layer is under ***tension***, it is likely to behave simply as already described

•if the grown layer is under ***compression***, it will become morphologically distorted

◦as layer growth proceeds, after a small number of uniform monolayers, there is often a transition to the growth of isolated, small islands (a ***Stranski-Krastanow transition***)

islands can be exploited as ***quantum dots*** in eg laser cavities

◦further growth leads to island overlap and the formation of undulating, ***wavy continuous layers***

islands and undulations are produced because ***lateral dilatation*** of the lattice in the growth crests (which are unconstrained) lowers the strain energy of the system

◦ultimately, for sufficiently thick grown layers, arrays of misfit-relieving dislocations will be introduced