EEE105 - Electronic Devices
Lecture 11

The p-n junction diode

(CAL: pn(b,)pn(c), pn(d), pn(e))

Last time we said that in a p-n junction there is a jump in the concentration of electrons and holes at the interface between the p- and n-type materials. This jump leads to diffusion of holes from the p-type material into the n-type material and electrons from the n-type material into the p-type material.

This diffusion is cause by the fact that the concentration of holes in the p type material is much higher that the hole minority carrier concentration in the n-type material and vice-versa for the free electrons.

Let us consider the holes diffusing into the n-type material.

The holes in the n-type material will become

Hence they will

Also when the holes leave the p-type material they will leave behind the acceptor atoms that brought them into the material. These acceptors that have lost their holes will be

Similarly the electrons moving into the p-type material, or indeed recombine with the diffused holes in the n-type material will leave behind their donors which will therefore be

We now have a situation where there is a density of oppositely charged donor and acceptor ions either side of the p-junction.

These will create an electric field, as we have a density of fixed charges in a region of space and we can use Poisson's Equation (see the first two lectures) to show this.

As more and more charges diffuse across the junction so the electric field will become larger as more and more acceptors and donors will have lost their charges through their diffusion giving a greater number of ionised acceptor and donor atoms in the material.

We call this electric field a ***built-in field*** across the p-n junction.

This built-in field acts to oppose the diffusion of electrons from the n-type material to the p-type material (and vice-versa for the holes).

Eventually the system will reach an equilibrium whereby he built-in field is sufficiently larger that it stops the diffusion process. In this situation we can say that the **drift** current exactly balances the **diffusion** current giving no net current flow.

Around the junction there is a region where all the free electrons and holes have recombined with each other leaving essentially no free carriers.

This region has been ***depleted*** of the free carriers and we call this region the ***DEPLETION REGION.***

Note here that we *must* have charge neutrality. Thus the number of positive donors and negative acceptors must balance.

This means that if $N_A > N_D$ then the thickness of the depletion region on the p-type side of the junction (d_1) will be less than the thickness of the depletion region on the n-type side (d_2).

It is clear we have a field in the junction region. This means that we have a ***potential difference*** across the junction which is the built-in potential, V_0. For Si the value of V_0 is about 1 V.

Now as we have charge neutrality, this built-in potential cannot be measured at the diode terminals. What we are looking at is a barrier for holes to overcome to get into the n-type material, or electrons to overcome to get into the p-type material.

So how do we calculate V_0?

Let us consider the situation for holes:

There will be a **diffusion current** given by:

$$J_{DIFF} = -D_h q \frac{dp}{dx}$$

The field due to the acceptor and donor ions will create a field, *E*, which will lead to a **drift current** given by:

$$J_{DRIFT} = \sigma E$$

Now in equilibrium we must have the situation where

$$J_{DRIFT} + J_{DIFF} = 0$$

Hence:

$$pq\mu_h E - D_h q \frac{dp}{dx} = 0$$

and this leads us to the relationship that $E = \frac{D_h}{\mu_h p} \cdot \frac{dp}{dx}$ We can now use the Einstein Relation:

giving $E = \frac{kT}{q} \cdot \frac{1}{p} \cdot \frac{dp}{dx}$ Now remember the relation between *E* and *V*:

and using this we can calculate the built-in voltage: $V_0 = -\frac{kT}{q}\int_{p_{(p)}}^{p_n} \frac{dp}{p}$

Integrating we will get: $\boxed{V_0 = \frac{kT}{q}\ln\left(\frac{p_{(p)}}{p_n}\right)}$

We can of course follow exactly the same procedure for electrons to show that $\boxed{V_0 = \frac{kT}{q}\ln\left(\frac{n_{(n)}}{n_p}\right)}$

We can plot the voltage against *x* as below:

Note we can rearrange the above two equations in terms of $p_{(p)}$ and $n_{(n)}$:

$$\boxed{p_{(p)} = p_n \exp\left(\frac{qV_0}{kT}\right)}$$

and

$$\boxed{n_{(n)} = n_p \exp\left(\frac{qV_0}{kT}\right)}$$

These relationships will be useful later

Example: Calculate the built-in voltage for Si

Let us use the relationship above that we have just derived: $V_0 = \frac{kT}{q}\ln\left(\frac{p_{(p)}}{p_n}\right)$

This can be modified to $V_0 = \frac{kT}{q}\ln\left(\frac{p_{(p)}n_{(n)}}{n_i^2}\right)$ using the relationship: $p_{(p)} = n_{(n)}$

Hence $V_0 = \frac{kT}{q}\left[\ln\left(p_{(p)}n_{(n)}\right) - \ln\left(n_i^2\right)\right]$

Now from before we said that $n_i = CT^{3/2}\exp\left(-\frac{W_g}{2kT}\right)$

Substituting: $V_0 = \frac{kT}{q}\left[\ln\left(p_{(p)}n_{(n)}\right) - \ln\left(CT^{3/2}\right)^2 + \frac{W_g}{kT}\right] = \frac{kT}{q}\left[\ln\left(p_{(p)}n_{(n)}\right) - \ln\left(CT^{3/2}\right)^2\right] + \frac{W_g}{q}$

Now let use say that $p = 10^{24}$ m^{-3} and $n = 10^{24}$ m^{-3} (Note $p_{(p)}$ and $n_{(n)}$ are just another way of writing p and n when there is potential for confusion, as there was above).

At room temperature $CT^{3/2} \approx 3x10^{25}$ and $\frac{kT}{q} \cong \frac{1}{40}\text{eV}$. Also $\frac{W_g}{q} = 1.1\text{eV}$.

Substituting in the equation above for V_0 we get V_0 = 0.025[110-117]+1.1 = 0.91 V

NOTE that W_g is the dominant term here. The value of V_0 is always close to W_g .

ALSO NOTE that V_0 is therefore not explicitly dependent on temperature. It is really only dependent on temperature in the sense that W_g has a temperature dependence.

Summary of Built in Voltage

What we have calculated here is the built-in voltage that we have to overcome if we are to get the diode to conduct in forward bias.

Next week we will look at the situation were we apply a bias to our p-n junction.

Key Points to Remember:

1. In a p-n junction electrons and holes will diffuse across the junction and recombine as minority carriers
2. The acceptor and donor ions are left behind and cannot move.
    a. They create an Electric field which acts to oppose the diffusion.
3. In equilibrium the diffusion and drift currents give a net current of zero.
4. From this we can calculate the built-in voltage of the junction.
    a. This built-in voltage is an internal barrier preventing current flow.
    b. You cannot measure it at the terminals of the p-n junction diode.
5. The built-in potential is closely related to the bond ionisation energy, of forbidden gap energy in band terms.