THE UNIVERSITY OF SHEFFIELD **EEE310**

The Final examination for the degree of:
B.Eng with Honours in Electronic and Electrical Engineering,

January 1999 (2 hours)

Introduction to VLSI design

Candidates should attempt **THREE** questions. **No marks will be awarded for solutions to any other question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out.

1.

(a) Outline the sequence of actions necessary for the efficient layout of a VLSI circuit. Without describing detailed algorithms, outline the objectives of the various phases, emphasising what is meant by good layout. **[6 marks]**

(b) Figure 1 shows the layout of a chip at an intermediate stage of the layout process. The next action is to consider the placement of the module labelled A.

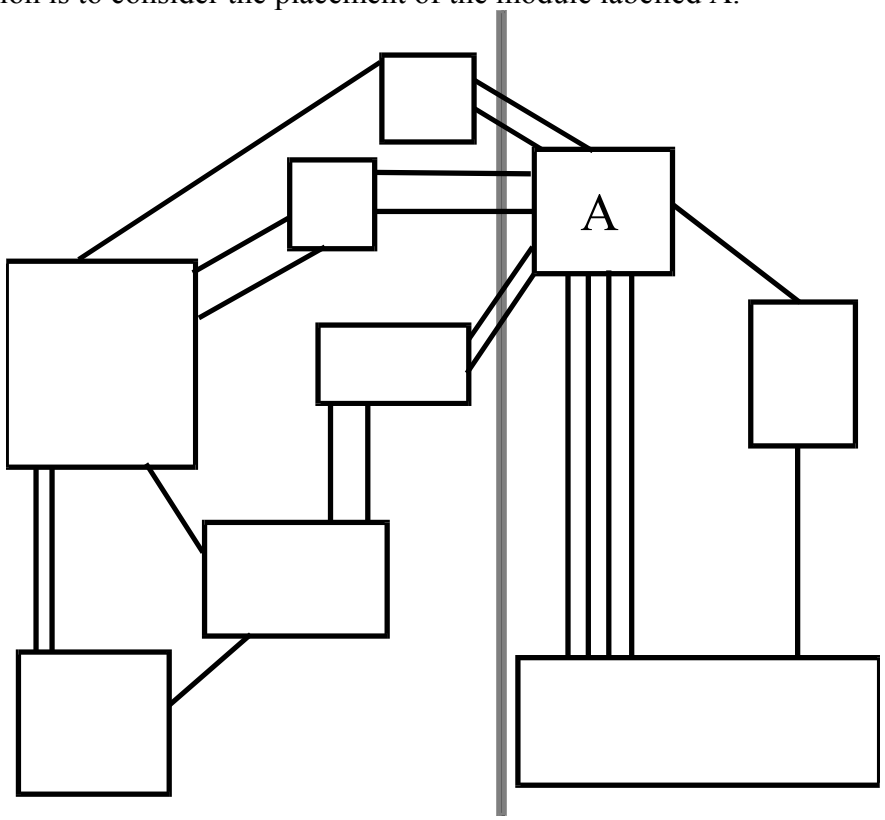

Figure 1

(i) Discuss, with an appropriate sketch the likely shift in the position of A as a result of this action, if the force directed placement (annealing) algorithm is used. *Your argument should be sufficiently detailed that it is clear that you understand the algorithm.* **[6 marks]**

(ii) Discuss the likely shift in the position of module A after this action if the min-cut algorithm is used. *As in part (i), the argument should be sufficiently detailed to make it clear that you understand the algorithm.* **[6 marks]**

(iii) In reality, it is unlikely that module A would be chosen for the next module to be considered if one were using a min-cut algorithm. Explain why this is the case. **[2 marks]**

2. Show how you can calculate the switching time of a multiple input NAND gate relative to an inverter, where the load capacitance is given by $C_L = mC_1 + C_2$ were m is the number of inputs to the NAND gate. (You may assume that the switching time of an inverter is 3CR and that $\beta_n = \beta_p$). **[5 marks]**

Show how the dynamic power dissipation can be calculated for such gates. **[5 marks]**

In a large scale VLSI circuit it is usual to assume that $C_2 >> C_1$. Briefly explain why this is so, indicating what is the most important contribution to C_2. **[3 marks]**

Figure 2 shows three designs that implement the same Boolean function. Calculate the relative switching speeds of these circuits if $C_2=2C_1$ for each logic gate. **[4 marks]**

For the circuits in this figure calculate the relative power dissipations if $C_2=2C_1$ for each logic gate, assuming that the switching rate is the same for each circuit, and (as a worst case analysis) that all logic gates change state at each switch. **[3 marks]**

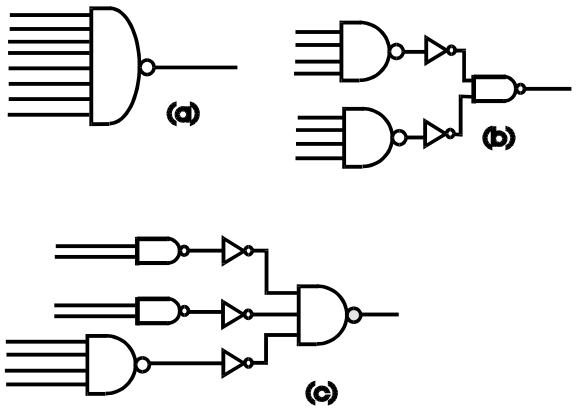

Figure 2

3. (a) In testing VLSI circuits it is normal to make assumptions about the type and number of faults that might be present. Briefly discuss these assumptions, the validity of the assumptions and why they are made.
[8 marks]

(b) For a particular design, the designers wish to make a different set of assumptions about the types of fault. They make the normal assumptions about the number of faults, but assume that each line can only be fault-free, shorted to ground, or floating. If the circuit has a total of Q lines, how many fault states must they consider? **[5 marks]**

(c) Making the usual assumptions about faults (<u>not</u> those in part (b)), identify a test vector that will test for a stuck-at-0 fault at J in the circuit shown in figure 3. What should we observe at which output under this test if the circuit is fault-free? **[7 marks]**

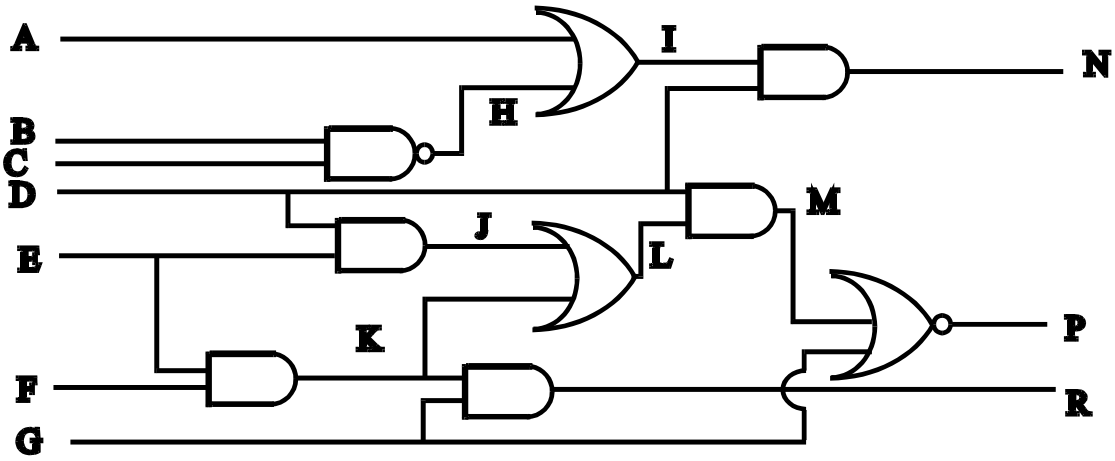

Figure 3

4. (a) What is meant by the term "noise margin" with respect to the input/output characteristics of a CMOS inverter? Briefly explain why noise margins are important to the operation of a system. **[6 marks]**

(b) Table 4 tabulates the transfer characteristics of an inverter. Determine the magnitude of the noise margins for this inverter, clearly outlining your working. **[6marks]**

(c) Calculate the relative sizes of the transistors that make up this inverter. (You may assume that the electron mobility is twice the hole mobility and that $V_{tn} = |V_{tp}| = 1V$).
[8 marks]

Input Voltage (V)	Output Voltage (V)
0.00	4.50
0.30	4.48
0.50	4.47
0.70	4.44
1.10	4.40
1.30	4.35
1.40	4.29
1.50	4.20
1.60	4.02
1.70	3.65
1.80	3.10
1.90	2.50
2.00	2.00
2.10	1.65
2.20	1.35
2.30	1.15
2.40	1.00
2.50	0.90
2.60	0.83
2.80	0.73
3.00	0.68
3.40	0.60
3.80	0.55
4.40	0.52
5.00 = Vdd	0.50

Table 4