Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (3.0 hours)

EEE225 Analogue and Digital Electronics

Answer **FOUR** questions including at least one question from each of sections **A**, **B** and **C**. **No marks will be awarded for solutions to a fifth or a sixth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

SECTION A

1. **a.** Explain, with the aid of diagrams, the operation of each of the following:
(i) A CMOS transmission gate. **(5)**
(ii) A two-input open-drain NAND gate. **(5)**

b. A CMOS NAND gate and a CMOS NOR gate are designed to occupy an equal area of silicon. Which gate is likely to operate faster? Explain the reasoning behind your answer. **(4)**

c. Describe the process of data transfer via Direct Memory Access (DMA). Why is DMA used and for what purpose is it typically used? **(6)**

2 **a.** With the aid of a diagram, explain the operation of a single Dynamic Random Access Memory (DRAM) storage cell. Describe how data is written to and read from the cell. **(7)**

b. Explain with the aid of a diagram the operation of a 4-bit successive-approximation Analogue-To-Digital Converter (ADC). **(6)**

A particular successive-approximation ADC uses reference values of 16 V for bit 2^3, 8 V for bit 2^2, 4 V for bit 2^1 and 2 V for bit 2^0. Determine the sequence of binary states in the register for the conversion of a constant input of 22.3 V. Explain each step. **(4)**

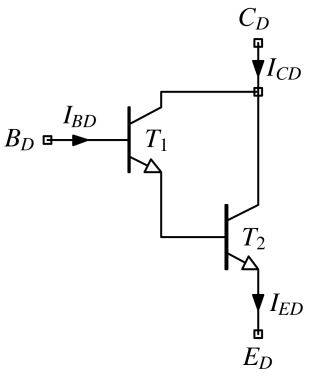
c. An Analogue-to-Digital Converter is to be used to convert a speech signal for digital signal processing. The analogue input signal is first passed through a low pass filter. Explain the reason for this filter. **(3)**

SECTION B

3. a. (i) Show that h_{FED}, the effective current gain, I_{CD}/I_{BD}, of the Darlington pair circuit in figure 3, is given by,

$$h_{FED} = h_{FE1} + h_{FE2} + h_{FE1}h_{FE2}$$

where h_{FE1} and h_{FE2} are the current gains of T_1 and T_2.



(3)

Figure 3

The circuit of figure 3 is to be used as a common emitter amplifier so E_D is connected to ground, B_D to an appropriate signal source and bias arrangement and C_D to a load resistor R_L, the other end of which is connected to the dc power supply.

(ii) Draw a small signal equivalent circuit of the common emitter amplifier connected Darlington pair assuming that r_{ce} in each transistor has a negligible effect on performance. **(4)**

(iii) Both T_1 and T_2 have an h_{FE} of 100 and both have an hfe (= β) of 200. The bias circuit defines I_{C2} as 1.00 mA. Find the input resistance of the common emitter amplifier from the signal source's point of view. **(5)**

The relationships $g_m = \dfrac{eI_C}{kT}$ and $r_{be} = \dfrac{\beta}{g_m}$ may be useful. $\dfrac{kT}{e} = 0.026$ V.

3. b. A particular op-amp with a gain bandwidth product of 40 MHz is connected in a non-inverting amplifier circuit. Resistor values are chosen to give an ideal circuit gain of 50.

(i) Is a –3 dB bandwidth of 2 MHz possible with this amplifier? **(1)**

(ii) What risetime would you expect to measure at the amplifier output in response to a step input voltage change from –50 mV to +50 mV? **(4)**

(iii) If the amplifier slew rate is 50 V μs^{-1}, what is the maximum peak to peak voltage of an undistorted 2 MHz sinusoid that can be obtained at the amplifier output? **(3)**

4. a. (i) Write down the high and low frequency gains of the circuit of figure 4 in terms of the appropriate circuit components. **(2)**

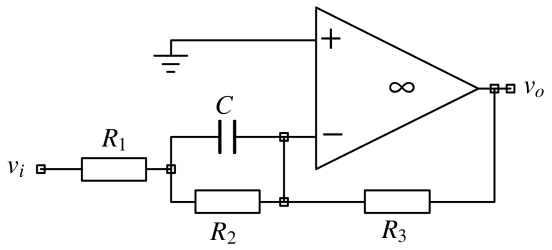


Figure 4

The transfer function, v_o/v_i of the circuit of figure 4 is given by:

$$\frac{v_o}{v_i} = -k\frac{1+j\dfrac{f}{f_0}}{1+j\dfrac{f}{f_1}} \quad \text{where } k=\frac{R_3}{R_1+R_2},\ f_0=\frac{1}{2\pi CR_2} \text{ and } f_1=\frac{R_1+R_2}{2\pi CR_1R_2}$$

(ii) If the required parameter values are f_0 = 50 Hz, f_1 = 1000 Hz and k = 10, find the ratios R_3/R_1, R_2/R_1 and the time constant CR_2 and suggest component values suitable for use with a typical operational amplifier. **(4)**

(iii) Sketch the magnitude response of the circuit ($|v_o/v_i|$ in dB as a function of log frequency) over a frequency range that will allow you to show the behaviour of the gain magnitude when f << 50 Hz and f >> 1 kHz. Label all key features of your sketch. **(4)**

4. b. (i) Define signal to noise ratio and explain briefly why signal to noise ratio is useless as a measure of system performance. **(2)**

A particular amplifier with an infinite input resistance, a noise equivalent bandwidth of 10 kHz and a gain of 100 V/V has equivalent input noise voltage and current generators of 8 nV $Hz^{-1/2}$ and 3 pA $Hz^{-1/2}$ respectively. The amplifier is driven by a signal source with a noisy Thevenin equivalent resistance of 1.8 kΩ.

(ii) A true rms voltmeter with a bandwidth considerably greater than the amplifier bandwidth is connected to the amplifier output. Calculate the reading you would expect to measure on the true rms meter in the absence of a signal input. **(5)**

(iii) What amplitude of sinusoidal signal input would give a signal to noise ratio of unity at the amplifier output? *(Assume that the input signal falls within the amplifier bandwidth such that it is operated on by the specified amplifier gain)* **(3)**

You can assume that the noise generated by a resistor R is $4kTR$ V^2 H^{-1} where T = 300 K and $k = 1.38\text{x}10^{-23}$ J K^{-1}

SECTION C

In this section you may need to use the following physical constants:

Charge on electron:	$e = -1.602 \times 10^{-19}$ C
Free electron rest mass:	$m_0 = 9.110 \times 10^{-31}$ kg
Speed of light in vacuum	$c = 2.998 \times 10^{8}$ m s^{-1}
Planck's constant:	$h = 6.626 \times 10^{-34}$ J s
Boltzmann's constant:	$k = 1.381 \times 10^{-23}$ J K^{-1}
Melting point of ice:	0^{o}C = 273.2 K
Permittivity of free space:	$\varepsilon_0 = 8.854 \times 10^{-12}$ F m^{-1}
Permeability of free space:	$\mu_0 = 4\pi \times 10^{-7}$ H m^{-1}

5. **a.** **(i)** A particular semiconductor sample contains known concentrations of both acceptors and donors. How would you determine whether the sample is extrinsically doped or is effectively intrinsically doped?

(ii) What is the normal relationship between the acceptor concentration and hole concentration in a semiconductor at room temperature?

(iii) In a semiconductor under equilibrium conditions, how are the electron and hole concentrations related to the intrinsic carrier concentration?

(iv) What is the Fermi-level in a semiconductor? **(6)**

b. An intrinsic layer of GaAs is initially uniformly doped n-type such that the intrinsic resistivity changes by a factor of 5×10^{5}. You wish to make a light emitting diode (LED) from this material so need to further dope the top part of this semiconductor layer. You have a choice of doing this with donor or acceptor atoms and each of this can be done to a level of 1×10^{21} m^{-3} or 1×10^{25} m^{-3}. Which dopant type would you chose and what is the minimum level of doping needed to make this LED? Justify your choices.

The intrinsic carrier concentration of GaAs at room temperature is 2×10^{12} cm^{-3}, and μ_e = 0.85 m^2 V^{-1} s^{-1}, μ_h = 0.04 m^2 V^{-1} s^{-1} and E_g = 1.42 eV. (Note: all the symbols have their usual meaning.) **(8)**

c. Draw and identify clearly the conduction band, valence band and Fermi-level of the LED made in part **b.** when it has no external bias and is in equilibrium. **(3)**

d. Sketch the shape of the output spectral response as a function of the wavelength expected from the LED designed in part **b**. Indicate the expected peak position and the typical width (in nanometers) of the spectral output. **(3)**

6 **a.** With the aid of a cross-sectional diagram of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST), describe briefly the conduction mechanism. Identify all the significant parts of the device in the diagram paying particular attention to the position of the gate with respect to the conducting channel. **(6)**

b. The unsaturated drain characteristic of such a MOST is given by:

$$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds}$$

where the symbols have their usual meaning. Using this relationship,

(i) state the condition for when the drain current saturates,

(ii) derive an expression for the drain current in the saturation region,

(iii) obtain an expression for the transconductance of the device in the saturation region. **(6)**

c. The source terminal of such a device is grounded and the drain terminal is connected directly to the gate terminal. When in the saturated drain current region and V_{ds} is 4 V, a current of 1 mA was found to flow. When V_{ds} was increased to 5 V the current increased to 2.77 mA. What will the drain current be when V_{ds} increases further to 6 V? **(6)**

d. The device described in part **c.** of this question has $\mu_e = 0.15$ m^2 V^{-1} s^{-1} and a gate capacitance of 1 pF. Estimate the channel length of the device. **(2)**

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