Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (2.0 hours)

EEE6213 Principles of Semiconductor Device Technology

Answer **THREE** questions. **No marks will be awarded for solutions to a forth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Show by means of an illustration the shape of an ‘s’ and ‘p’ orbital. Hence draw the 3D bonding structure of a material containing “sp3” hybrid orbitals and one containing “sp2” hybrid orbitals. Name clearly the materials you have chosen to illustrate each of the respective structures. Indicate x, y and z axes in all diagrams. **(5)**

b. Derive the packing efficiency for a simple primitive cubic lattice and a face centred cubic lattice. **(5)**

c. What is an *E-k* diagram? Draw E-k diagrams for a direct and an indirect semiconductor indicating the role of a photon and a phonon in initiating transitions electron transitions. How would you use this knowledge to practically determine if a semiconductor is direct or indirect? Use diagrams as necessary to explain your answers. **(5)**

d. Consider a Si sample maintained at T = 300K under equilibrium conditions, doped with boron to a concentration 2×10^{16} cm^{-3}. Given that $n_i = 10^{10}$ cm^{-3}.

i) What are the electron and hole concentrations (n and p) in this sample? Is it n-type or p-type?

ii) Suppose the sample is doped additionally with phosphorus to a concentration 6×10^{16} cm^{-3}. Is the material now n-type or p-type? What is the resistivity of this sample?

(5)

2. **a.** Ultra-thin semiconductor materials are of interest for future nanometer-scale transistors, but can present undesirably high resistance to current flow. How low must the resistivity of a semiconductor material be, to ensure that the resistance of a 2nm-thick, 10nm-long, 100 nm-wide region does not exceed 100 ohms? If this material is n-type Si, estimate the dopant concentration that would be needed to achieve this resistivity. Assume $\mu_n \cong 820$ cm^2/Vs, q = charge on an electron = 1.6 $\times 10^{-19}$ C. **(5)**

b. Name 2 key generic differences between the techniques: (i) Molecular Beam Epitaxy (MBE) and (ii) Metal Organic Chemical Vapour Deposition (MOCVD) employed for the growth of III-V compound semiconductors. What are the requirements of reagent materials in a MOCVD reactor? **(5)**

c. What is a hetero-epitaxial pseudomorphic layer? Draw two diagrams showing such layers, one with compressive and one with tensile strain. **(5)**

d. What is the advantage of the "crucible-free" needle-eye technique for float zone wafers? What is the role of the molten boric oxide in the Liquid Encapsulated Czochralski (LEC) technique? What advantage do GaAs crystals grown by the Bridgeman technique have over LEC technique? **(5)**

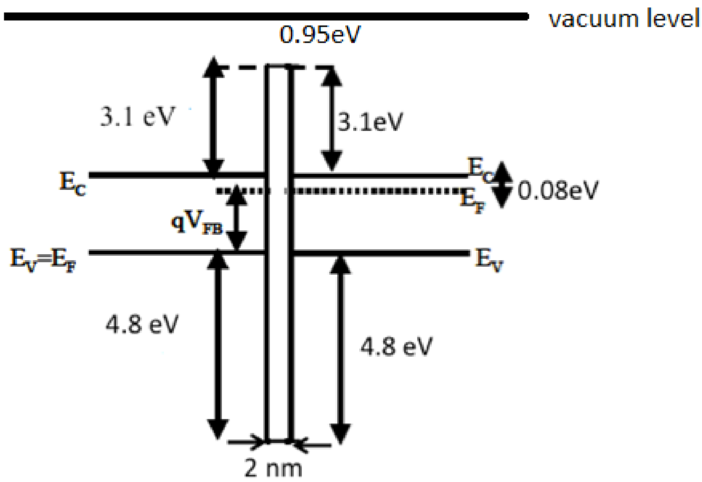
3. **a.** A silicon ingot is grown by the Czochralski technique. The ingot is doped with Arsenic whose segregation coefficient in Si is 0.3. If C_0 is the initial concentration of the impurity in the melt, C_s is the final concentration of the impurity in the crystal, x is the fraction of melt solidified and k_0 is the impurity segregation coefficient, then

$$C_S = k_0 C_0 (1-x)^{k_0 - 1}.$$

Calculate the fraction of the melt solidified when the concentration of arsenic in the ingot has risen by a factor of 30 from its initial value.

(5)

b.



The figure above shows the flatband condition of an ideal silicon MOS capacitor at 300K. For an oxide thickness of 2nm qV_{FB}= 1.07eV.

i) What is the value of the semiconductor workfunction Φ_S, of this capacitor?

ii) What is the value of the gate workfunction Φ_M of this capacitor ? Name a gate material with these characteristics.

iii) Sketch the energy-band diagrams, labeling qV_G, $q\psi_S$, qV_{ox} (no numerical values required), for accumulation and strong inversion. ψ_S represents the surface potential and V_G and V_{ox} represent voltages across the gate and oxide respectively. **(10)**

c. Name two methods of etching insulating films. What are the etch characteristics of each method? **(5)**

4. **a.** Show band diagrams to indicate the on-state, off-state and ambipolar leakage in a tunnel FET. Give one limitation of a tunnel FET in comparison to a MOSFET in applications for future CMOS.

(10)

b. Explain diagrammatically a CMOS process. Write a statement explaining what is meant by (i) LOCOS and why is it needed. (ii) Field threshold adjust implant and why it is needed. (iii) Self aligned process. **(10)**

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