EEE6214 solutions 2014-5 GLW/KG

Q1
a) 3d packaging drivers:
Form-factor i.e. higher density, since transistor/ device volume ratio reduced
Performance i.e. higer speed since interconnect lengths reduced
Heterogeneous integration e.g. CMOS + sensor, etc
Cost - Cheaper than buying next generation lithography tools

b) delta T for IC:

i) Rsolder = L/kA = $100x10^{-6}$ / 50 x 10^{-4} = 0.02
RFR4 = $600x10^{-6}$ / 0.2 x 10^{-4} = 30
Delta T = QR = 30.02 degrees

ii) Rvia = $740x10^{-6}$ / 400 x 10^{-4} = 0.0185
Rvias = Rvia/25 = 0.00074
DeltaT = QR = 0.02 + 0.00074 = zero!

c) Crosstalk at IOs
Use multiple ground pins on connectors in order to make better approx to coax.

d) Connectors in design process
Need to be considered early, so that they fit!

e)Laser diode packaging
Low thermal resistance (because of very high power density), transparent materials (so that light can get out!), temperature stabilization (to avoid wavelength shift).

Q2
a) Reflow profile

b)Oxidation reduction
Use inert (nitrogen) or even reducing (hydrogen) atmosphere

c)
i) Large thermal mass – increase length of soak period (see part a)) in order to ensure that all of board is thoroughly heated
ii) Non-eutectic solder – increase reflow temperature to account for higher melting point of non-eutectic composition.

d)
i) let t = 35 um (1 oz copper); w = 100 um
hence, by substituting into eqn. h = 131 um
At 90 degree bend, track width =100 x sqrt(2) = 141 um, hence Z_0 = 40 Ω

ii) impedance mismatch will cause reflections 11%
iii) avoid issue by making gradual curve (constant line width) rather than sharp bend. This makes CAD software more complicated.

Q3

a) shape parameter = ln32000 – ln18000 ~0.57 which describes the constant failure region of the bathtub (therefore suggest appropriate failure mechanisms in this region for LDs).

b)
MTTF (80degrees) from plot = 17,700 hours
i) AF=MTTF(T1)/MTTF(T2) = $\exp[E_a/k(1/T1 - 1/T2)$
$32000/17700 = 1.8 = \exp\{E_a/k[(1/333 - 1/353)]\}$
which gives $E_a = 0.3$
ii) MTTF (368K) = $A\exp(E_a/kT) = \exp(0.3/k368) = 12800$ hours , therefore just over half of the devices are still yet to fail after 12,000 hrs.

c)
i) Use EBIC, and describe its operation as per the lecture notes…..

ii) if you cannot electrically bias then EBIC cannot be used. CL would allow you to characterize the area around the junction by analyzing the spectral response from recombination of E-beam induced electron-hole pairs and show up defects.

d)
Describe COD as per lecture notes. Absorption at surface states created by defects on facet with E<Eg -> non-radiative recombination -> heating -> further absorption as Eg shrinks -> creates more point defects -> thermal runaway….. mechanical damage.
Eg of InP < AlGaAs so less E released to lattice by each non-radiative recombination. Also, AlGaAs oxidises readily, breaking bonds at surface -> more point defects.

Q4

a) PCB surface finishes
over dielectric and tracks: solder mask
over bond pads: corrosion protection layer (solder, noble metal, OSP)
Advantages / disadvantages…

b) Fan cooling

At sea level, case to ambient thermal resistance $R_{ca0} = \Delta T/Q = (50\text{-}20)/1 = \underline{30\ °C/W}$
$h \propto \rho^{0.5}$ hence: $h_0^2/\rho_0 = h_6^2/\rho_6$ hence: $h_6 = (\rho_6 / \rho_0)^{0.5} h_0$ hence, using data:
$h_6 = (0.66/1.35)^{0.5} \times h_0 = 0.7\ h_0$ hence: $(h_o / h_6) = \underline{1.4}$
Recall: $R_{convection} = 1/hA$ hence: $R_{conv}\, h$ = constant
Hence $R_{ca6} = R_{ca0}\ (h_0/h_6) = 1.4\ R_{ca0} = 1.4 \times 30 = \underline{42\ °C/W}$
Recall $\Delta T = T_c - T_a = QR$ hence, at altitude of 6 km:
$T_c = (1 \times 42) - 18 = \underline{24\ °C}$

c) 3 methods for IC-package connections
wire bond; tape automated bond; solder balls

d)
i) flip chip solder balls
ii) wire bond
iii) TAB