# EEE6208 2015/2016 Solutions – AM

***(X)*** *indicates allocation of marks.*

**1.a.**

An NMOS transistor has the following parameters: $K_n$=150µA/V$^2$, λ=0.05V$^{-1}$, W/L=10µm/0.5µm,

**i)** What drain current results when this transistor runs with an overdrive voltage of 0.5V and a drain-source voltage, $V_{DS}$, of 2V?(2 marks)

$$I_{D0} = \frac{K_n}{2}\frac{W}{L}V_{OV}^2 = \frac{150\times10^{-6}}{2}\frac{10}{0.5}0.5^2 = 375\mu A$$ **(1)**

With channel modulation included:

$$I_D = I_{D0}(1+\lambda V_{DS}) = 375\times(1+0.05\times2) = 412.5\mu A$$ **(1)**

**ii)** What is the transistor's drain-source resistance, $r_o$, under these conditions? (1 mark)

$$r_o = \frac{1}{\lambda I_{D0}} = \frac{1}{0.05\times375\times10^{-6}} = 53.3k\Omega$$ **(1)**

**iii)** If $V_{DS}$ increases to 2.5V, what is the corresponding change in drain current? (2 marks)

When $V_{DS}$ is increased to 2.5V:

$$I_D = I_{D0}(1+\lambda V_{DS}) = 375\times(1+0.05\times2.5) = 422\mu A$$ **(1)**

A change of 9.5uA. **(1)**

**OR**

Alternatively: $\Delta I = \frac{\Delta V}{r_o} = \frac{0.5}{53333} = 9.5\mu A$ **(2)**

**1.b.**

The transistor described in **part a** is to be used, together with a PMOS active load transistor (M2), in the common-source amplifier configuration shown in **Figure 1** *(see script)*. Transistor M2 has an output resistance, $r_o$=200kΩ, transconductance parameter, Kp=200µA/V$^2$, turn-on voltage $V_{TO}$= -0.25V and channel aspect ratio W/L=20µm/2µm. The amplifier is to be operated with a bias current of 150µA.

**i)** Calculate a suitable value for $V_{bias}$ - the voltage at the gate of transistor M2. (3 marks)

For a bias current of 150uA we have:

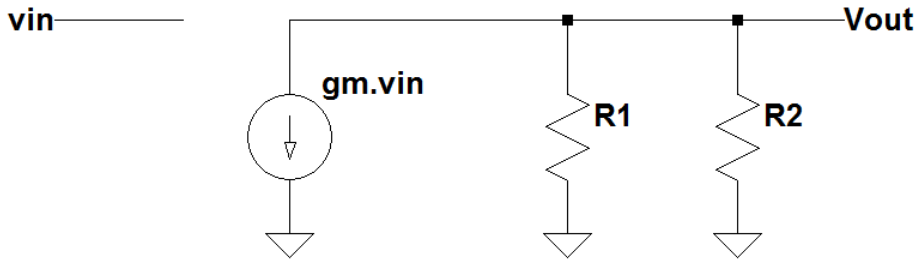
$$V_{OV} = \sqrt{\frac{2I_{D0}L}{K_P W}} = \sqrt{\frac{2\times150\times10^{-6}\times2\times10^{-6}}{200\times10^{-6}\times20\times10^{-6}}} = 0.39V \qquad \textbf{(1)}$$

The gate-source voltage for M2 is therefore:

|VGS|=|VTO|+|VOV|=0.39+0.25=0.64V **(1)**

and the value of Vbias should be: 5V-0.64=4.36V **(1)**

**ii)** Draw the small signal model of the circuit in **Figure 1** and calculate values of output resistance, $r_o$, and transconductance, $g_m$, to include in your diagram. (5 marks)




**(3)** *marks for: power supply to signal ground, active load modelled as a resistance, correct small signal model for amplifying transistor.*

$$V_{OV} = \sqrt{\frac{2I_{D0}L}{K_n W}} = \sqrt{\frac{2\times150\times10^{-6}\times0.5\times10^{-6}}{150\times10^{-6}\times10\times10^{-6}}} = 0.32V \qquad \textbf{(1)}$$

$$g_m = K_n \frac{W}{L} V_{OV} = 150\times10^{-6}\times\frac{10}{0.5}\times0.32 = 0.96mS \qquad \textbf{(½)}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05\times150\times10^{-6}} = 133k\Omega \qquad \textbf{(½)}$$

**iii)** Calculate the gain of the amplifier from the small signal model, showing your working. (3 marks)

$$V_{out} = 0 - i_D(R1||R2)$$

$$= -g_m v_{in}(R1||R2) \quad \textbf{(1)}$$

$$\therefore A_V = \frac{V_{out}}{v_{in}} = -g_m(R1||R2) = -0.96mS \times (133k||200k) = -76 \quad \textbf{(2)}$$

**iv)** To realise the biasing of transistor M1, a current mirror or a resistor could be attached at the point labelled 'S(M1)' in **Figure 1**. Briefly describe the advantages of biasing at point S(M1) rather than using a potential divider at the gate of M1. Also briefly describe the advantages of using a current mirror rather than a resistor. (4 marks)

By biasing at the source of transistor M1 rather than at its gate, *feedback* is introduced into the circuit **(1)**: if the operating point of M1 causes a drop in e.g $K_n$, the drain current will decrease, but this will cause a decrease in the voltage across the biasing circuit, leading to an increase in Vgs of M1, which will cancel out the initial change in current. **(1)**

A current mirror can have high output impedance without requiring a very large voltage 'headroom' **(1)**. This means that it can provide a stable operating point for low-voltage amplifiers, where the bias current does not vary with the input signal. When implementing a circuit on an IC, the transistors of a current mirror take up much less space on the wafer than would a large-value resistor. **(1)**

**2.a.**

**Figure 2** *(see script)* shows a simple n-channel current mirror, implemented using two identical NMOS transistors, M1 and M2. The transistors both have transconductance parameter $K_n$=200µA/V$^2$ and turn-on voltages of $V_{TO}$=0.6V. They have channel dimensions W/L = 8µm/1µm.

**i)** Ignoring channel length modulation effects, calculate the value of R required to set the drain current through M1 at 100µA. (4 marks)

$$V_{OV} = \sqrt{\frac{2I_{D0}L}{K_n W}} = \sqrt{\frac{2\times100\times10^{-6}\times1\times10^{-6}}{200\times10^{-6}\times8\times10^{-6}}} = 0.35V \qquad \textbf{(1)}$$

$$V_{GS} = V_{OV} + V_{TO} = 0.35 + 0.6 = 0.95V \qquad \textbf{(1)}$$

The voltage across the resistor R is therefore 5-0.95=4.05V **(1)**.

To give a reference current of 100uA the resistor should take the value 4.05/100uA=40.5kΩ.**(1)**

**ii)** What is the minimum value of the voltage across M2, $V_{out}$, in order that the mirror operates correctly? What region of operation will M2 fall into if $V_{out}$ falls below this value? (2 marks)

Because M2 and M1 are matched, the overdrive voltage for M2 is also 0.35V, and this is the minimum value of Vout **(1)**. If it falls below this level, M2 will fall into the triode region. **(1)**

**iii)** Given that the transistors have a channel length modulation parameter λ=0.04V$^{-1}$, find the change in the current through M2 if $V_{out}$ reduces by 1V. (3 marks)

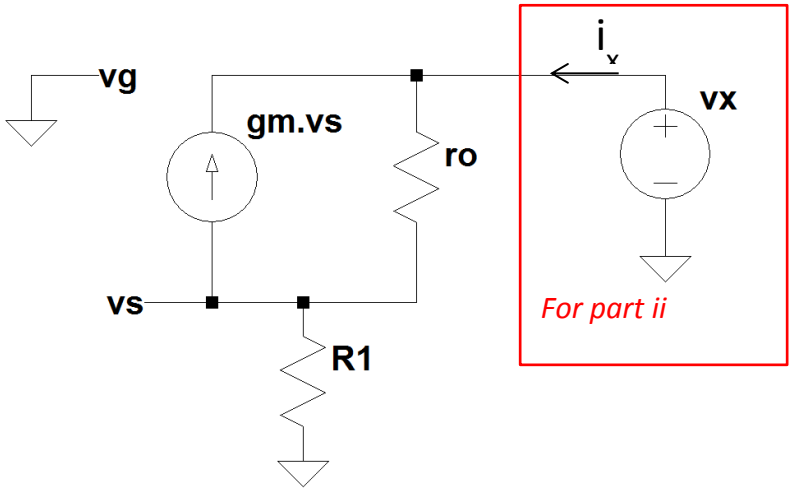
$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.04\times100\times10^{-6}} = 250k\Omega \qquad \textbf{(1 ½)}$$

Therefore the change in current for a 1V reduction in Vout is 1/250k=4uA. **(1 ½)**

**2.b.**

**Figure 3** *(see script)* shows the output side of a source-degenerated current mirror, with source resistance $R_1$.

**i)** Draw the small-signal model of this circuit. (4 marks)




**(3)** marks for: signal grounding of gate; correct small signal model for MOSFET.

**ii)** Use nodal analysis to show that the output resistance, $R_{out}$, of the current mirror in Figure 2 is given by:

$$R_{out} = \frac{1}{g_o}(1 + R_1(g_o + g_m))$$

Where $g_m$ is the transconductance of transistor M2, $g_o=1/r_o$ is the drain-source conductance of transistor M2. (6 marks)

Writing nodal equations

(1) $v_x g_o - v_s g_o - v_s g_m - i_x = 0$ **(1 ½)**

(2) $v_s(G_1 + g_o) - v_x g_o + v_s g_m = 0$ **(1 ½)**

Using 2:

$$v_s = \frac{g_o}{g_o + G_1 + g_m} v_x$$ **(1)**

Sub into 1:

$$v_x g_o - (g_o + g_m)\frac{g_o}{g_o + G_1 + g_m} v_x = i_x$$

$$\therefore R_{out} = \frac{v_x}{i_x} = \frac{1}{g_o} \cdot \frac{g_o + G_1 + g_m}{g_o + G_1 + g_m - g_o - g_m}$$ **(2)**

$$R_{out} = \frac{1}{g_o}\left(1 + R_1(g_o + g_m)\right)$$

**iii)** Give conditions under which $R_{out}$ can be approximated by: $R_{out} \approx g_m R_1 r_o$ (2 marks)

Expanding brackets:

$$R_{out} = r_o + R_1 + g_m R_1 r_o \qquad \textbf{(1)}$$

If $R_1$ and $r_o$ are large **(1)** compared to $g_m$, the final term dominates and the expression can be approximated by: $R_{out} \approx g_m R_1 r_o$

# EEE6208 2015/2016 Solutions – NJP

**3.a.**

(i) Explain what is meant by *strained silicon* technology. How does this improve the performance of CMOS transistors? (4 marks)

Mechanical strain is introduced to the channel (1). NMOS transistors are tensile strained and PMOS transistors are compressive strained (2). Carrier mobility is greatly increased improving speed and drive current (1).

(ii) Describe what you understand by the term *FinFET*. What are the advantages of FinFET technology? (4 marks)

FinFET technology creates a 3d structure that sits on top of the substrate. The *fins* form the source and drain (1). The gate wraps around the *fin* which allows better control of the channel. The thickness of the fin determines the effective channel length of the device (2). Static leakage currents are greatly reduced resulting in lower power consumption (1).

**3.b.**

Consider the circuit shown in **Figure 3.1**. You may assume that the inverter switches at $V_{DD}/2$.

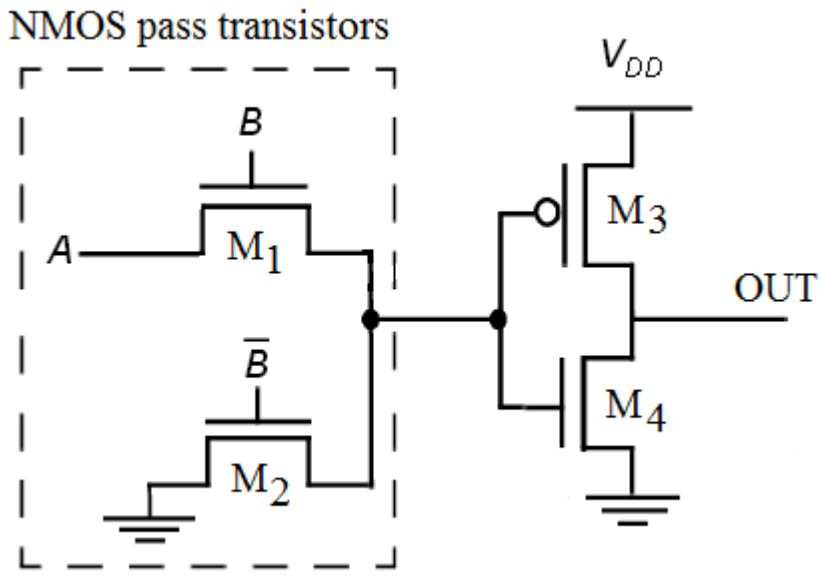



**Figure 3.1 Pass Transistor Circuit**

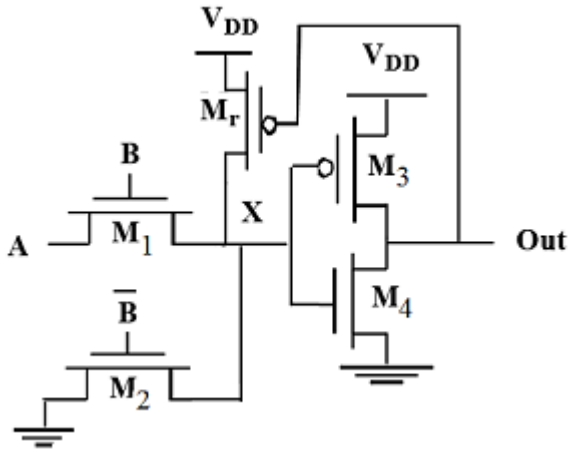
**i)** What is the logic function performed by this circuit? (3 marks)
The output is the NAND of A and B (3).

**ii)** Assuming that gate leakage can be ignored, explain why the circuit has non-zero static power dissipation. (4 marks)

The input to the inverter is not pulled up to $V_{DD}$ but to $V_{DD}$ - $V_{TN}$ and the PMOS transistor cannot be fully turned off (2). This results in static power consumption as $M_3$ may be weakly conducting forming a path from $V_{DD}$ to ground (2).

**iii)** Using only one additional transistor, show how the circuit can be modified so that there will not be any static power dissipation. (2marks)

A level restoring transistor should be added as shown (2).




**iv)** Explain how you would determine the size of the additional transistor. (3 marks)

$M_r$ must be sized small enough for the voltage at X to be brought below $V_{DD}/2$, the threshold voltage of the inverter, or $M_r$ cannot be turned off (3).

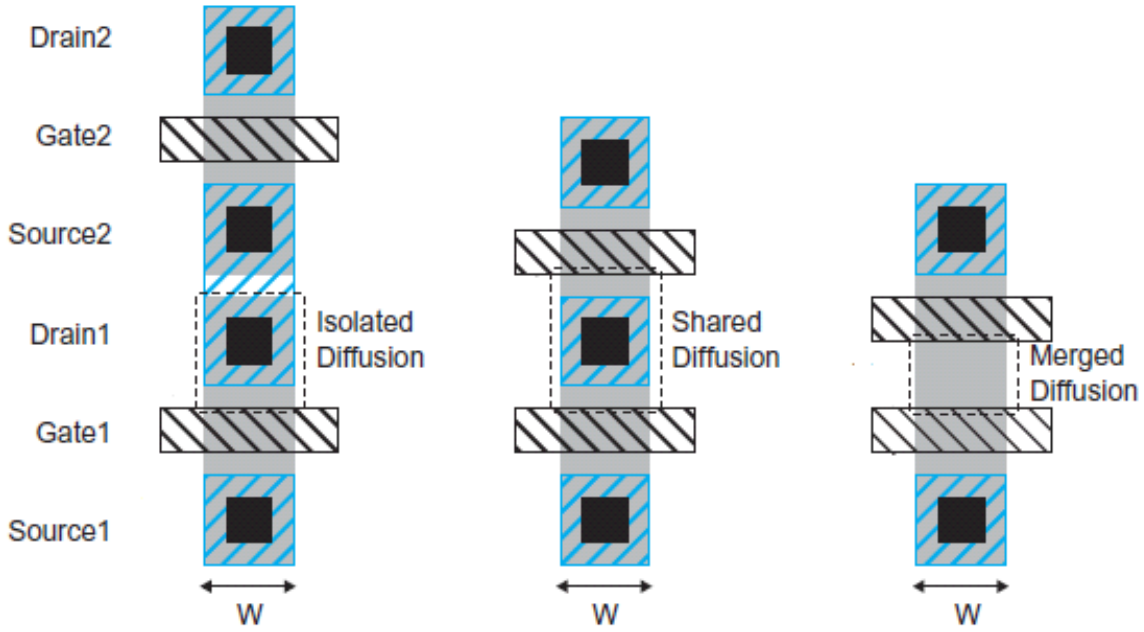
**4.a.**

Two NMOS transistors are to be connected in series using a bulk CMOS process. Describe with the aid of a diagram what is meant by: (6 marks)

**i)** Isolated contacted diffusion has separate contacted areas for source and drain. This is used for the connection (2).

ii) Shared contacted diffusion has a single shared contact for the source and drain (2).

iii) Merged diffusion has no contact. The source and drain share a merged diffusion (2).



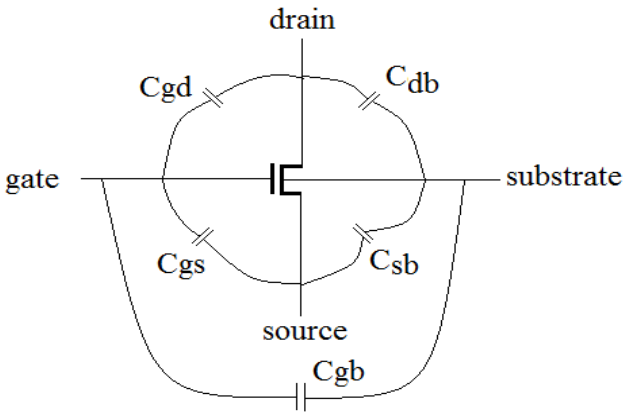

**4.b.**

**i)** Describe the capacitances associated with a MOSFET device. (3marks)

Cgs, Cgd : gate-to-channel capacitances, lumped at source and drain ends. (1 mark)

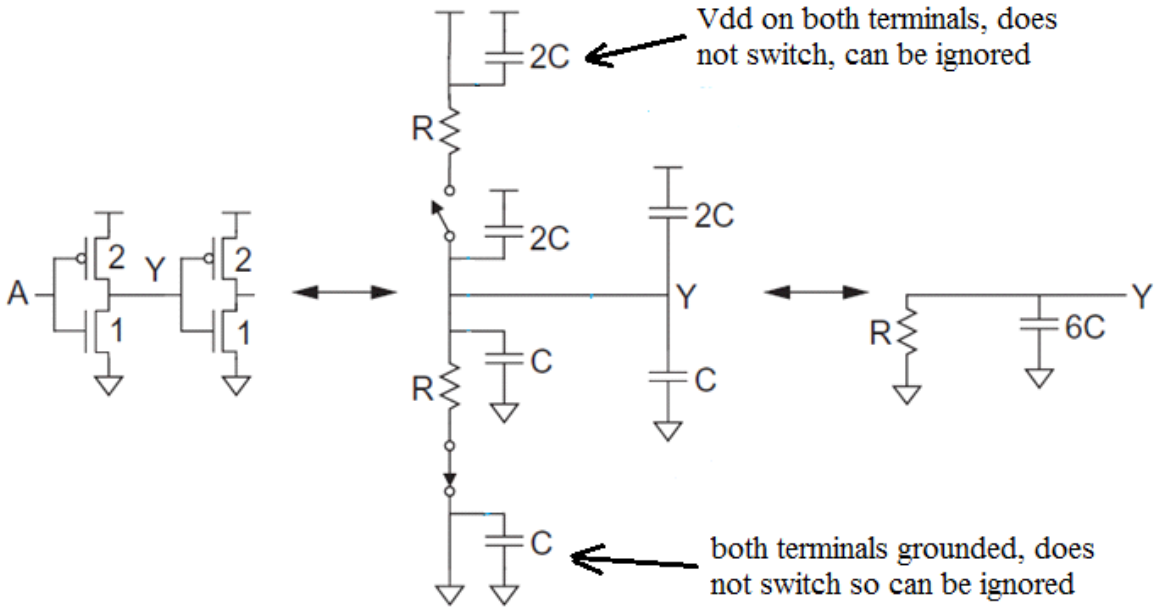
Csb, Cdb : source and drain diffusion capacitances to substrate. (1 mark)

Cgb: gate-to-bulk bulk capacitance. (1 mark)




Capacitances may be annotated on diagram.

**ii)** Explain with the aid of a diagram why the equivalent RC load of the driving inverter has a resistance of R and a capacitance of 6C. (4 marks)




For equal rise and fall time, pull-up and pull-down network should have equal resistance R (1 marks).

Non-switching capacitances from source to substrate can be ignored.

Driver: PMOS has 2C drain diffusion capacitance; NMOS has C drain diffusion capacitance. (1 mark)

Load: PMOS presents 2C gate capacitance, NMOS presents C gate capacitance. (1 mark)

Total driven capacitance 2C + C + 2C + C = 6C. (1 marks)

**4.c.**

(i) Draw the circuit diagram for a static CMOS 2-input NOR gate. Determine the transistor widths required to achieve effective rise and fall resistances equivalent to a unit size inverter (3 marks).

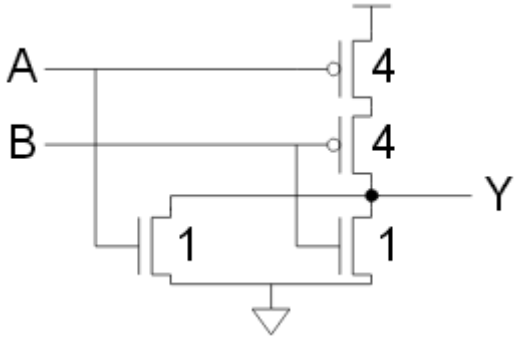
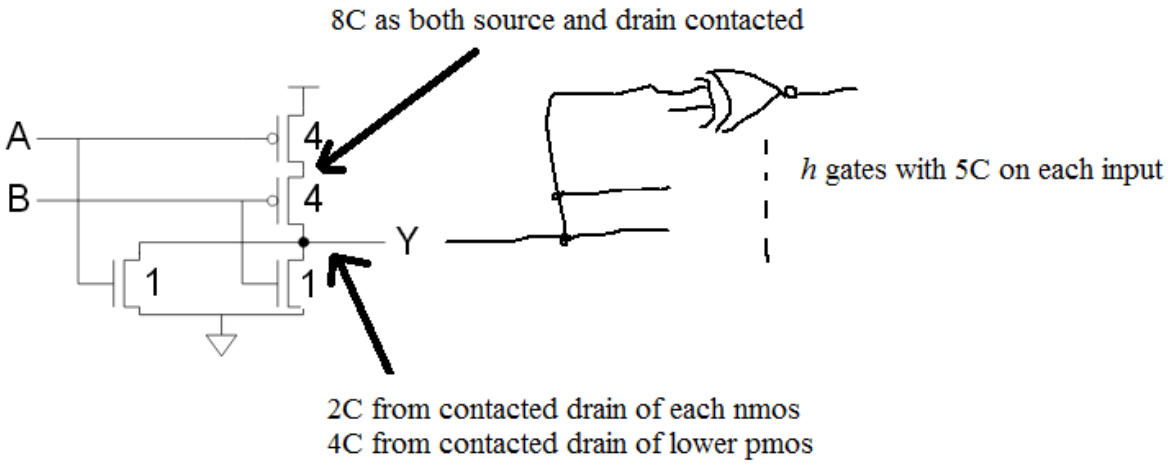



Diagram (1 mark)

NMOS parallel connection: each resistance must equal R for worst case when only one device is ON (1 mark)

PMOS series network: increase width by 4 (x2 to allow for hole mobility, x2 to allow for series connection (1 mark)

(ii) The NOR gate is required to drive *h* identical gates. Using the Elmore delay model, derive an expression for the RC delay of the circuit, for a rising transition on the driving gate output. Assume that isolated contacted diffusions are used for every source and drain (4 marks).




For a rising output at point Y:

The junction of the pmos devices has a capacitance of 8C and will charge through the top pmos which has a resistance of R/2 (1 mark).

Node Y has its own diffusion load of 2C + 4C = 6C (1 mark) and a fanout load of 5*h*C (1 mark) all of which is charged through both pmos devices which have a combined resistance of R.

Hence, Elmore delay = 8CxR/2 + (6C + 5*h*C)R = (10 + 5*h*)RC  (1 mark)