EEE105 - Electronic Devices
Lecture 15

Transistors

For the remainder of this course we will discuss transistors. In a transistor we are interested in using electronic signals to control current flow in a device.

There are two different generic types of transistor:

Junction Field Effect Transistor (JFET)

(CAL: Jfet(a), Jfet(b))

The Junction Field Effect Transistor is based on a p-n junction. However, we are not interested in this case in carriers crossing the junction.

In the transistor we have essentially three contacts.

In the JFET case two contacts are at either end of a piece of material that is uniformly doped either p-type or n-type. The third contact is to a piece of material that is doped with the opposite type. Let us consider the situation where the two contacts are to n-type material, as in the simplified model shown to the left.

The main current flow is in the n-type material in this case, between the two contacts to it. These contacts are called the ***"source"*** and the ***"drain"***. The charge carriers (electrons for n-type material in this case) are injected at the source and *drained off* at the other end.

The region between the source and drain is called the ***"channel"***. As the current flows along the channel there will be a voltage drop given by the channel resistance. This channel resistance will be given by the cross-sectional area of the channel, its length, and the resistivity of the n-type material.

The key point to the transistor is how can we change the current flow through the channel.

For a fixed voltage, we can change the current flow if we can change the channel resistance.

The question is how can we do this?

We can modify the depletion region thickness by applying a reverse bias to the p-n junction. Increasing reverse bias will increase the depletion region thickness and hence decrease the channel thickness. Reduced channel thickness means reduced channel cross-sectional area and a higher channel resistance. This means that the current is reduced for a fixed voltage.

To vary the reverse bias of the p-n junction we apply a voltage to the p-type contact, called the ***"gate"***.

Practical JFET

It is not normal to make a JFET as shown in the simplified model above. Normally the device is created on an insulating piece of Silicon. The n-type dopant is then diffused into the surface to make the channel. Subsequently a high density of p-dopant is diffused in a shallower region to create the gate semiconductor region and making a p^+-n junction.

The device is etched around the edge to provide isolation from neighbouring devices.

Finally metal is placed on the surface to form the source, gate and drain contacts. Wires can be bonded to these contacts to allow us to connect the JFET with the rest of the circuit.

Question: Above we said that we wanted a p+-n junction. Why is this the case?

JFET Operation (I) – Assuming the Gate is under zero bias.

To start we will consider that the gate is shorted to the source ($V_g = 0$) and that there is a voltage, V_d applied to the drain.

In this case we shall use an n-channel JFET again. Thus the current will only flow in the n-type material. We say that the device is a ***UNIPOLAR*** device.

Note that the current flows in the opposite direction to the electrons and that hence the electrons enter the JFET at the *source* and leave the JFET at the *drain.*

Now the channel can be represented as a resistance. Assuming it is of uniform cross-sectional area, the voltage will be dropped uniformly along the channel from source to drain.

However, this assumption is only really valid if the value of V_d is not too large, as is explained below.

Note that the channel is positively biased with respect to the gate. Hence the gate-channel p-n junction is REVERSE BIASED.

Now as we move along the channel from source to drain the resistance of the channel means that the voltage of a particular point in the channel is more positive with respect to the gate as we get closer to the drain end. This means that the gate-channel p-n junction is MORE REVERSE BIASED at the drain end compared to the source end of the device.

We said earlier that we wanted a p^+-n junction so that the depletion region will be mainly in the channel so that we can change the thickness of the channel effectively. Now from the last lecture we know that the depletion region width for a reverse biased junction, $d_j \sim V^{1/2}$.

Thus the depletion region is wider at the drain end of the device and consequently the channel width is narrower.

If V_d is increased further then the depletion region at the drain end will expand further and the channel resistance must increase. Eventually some point is reached where the depletion regions from both sides of the gate (using the simplified model device) almost touch and the current saturates.

This point is called the ***"pinch-off voltage"*** and occurs when $V_d = V_p$.

Increasing the drain voltage, V_d, still further causes the depletion region to extend laterally (along the device channel) and it is found that the value of current flowing through the transistor, I_d remains the same (or saturates). This gives us a current-voltage characteristic as shown:

As the current is constant the resistance must be increasing in proportion to the voltage drop in this region of operation of the device.

JFET Operation (II) – Varying the bias on the gate.

In the JFET we do not want significant current to flow through the gate, so we cannot forward bias the gate contact with respect to the source. Hence we will examine the case where a reverse bias is applied, by making the gate [ ] with respect to the source.

If the gate is reverse biased then the depletion region will [ ].

There will be an additional contribution to the depletion region thickness to that provided by V_d.

This means that as V_d increases the pinch-off condition will be reached earlier and that the saturation current will be reduced.

Looking now at the current-voltage characteristics a family of curves is obtained for various values of V_g.

Note that above the pinch-off voltage the saturation current is controlled only by the gate voltage, V_g. This means that a large current can be controlled by an electronic voltage signal (which does not require much current to maintain).

Key Points to Remember:

1. In a JFET we have a channel of n- or p-type material.
2. There is a depletion region round a p-n junction, which constricts the channel
   a. Increasing the depletion region (reverse bias the "gate") increases channel resistance.
3. At high drain bias the current saturates at some pinch off voltage.
4. The value of drain current when it saturates is reduced by reverse biasing the gate.
5. In the amplifier region the drain current is controlled exclusively by the gate voltage.