Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2011-12 (2.0 hours)

EEE340 Analogue and Switching Circuits

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. A transistor switch is used to energise a relay from a 48 V supply (V_s). The relay possesses a coil resistance of R = 40 Ω and an inductance of L = 0.08 H as shown in Figure 1. The relay switches on for currents of 0.4 A or greater but does not switch off until the current has fallen below 0.15 A or less. The transistor is controlled by the drive voltage v_B and you should assume that the transistor and the diode exhibits ideal instantaneous switching characteristics. The transistor T is protected from the effects of energy stored in the relay inductance by the diode resistor network D-R_s.

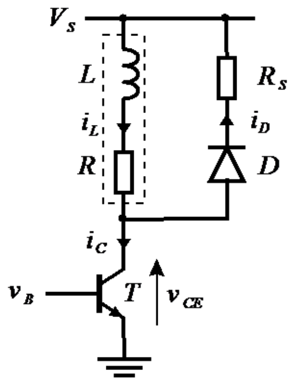

Figure 1

a. Draw waveforms for the relay current i_L, transistor current i_C and diode current i_D that you would expect to see if the transistor is driven by a square-wave control voltage v_B that is of sufficient duration for the currents to settle to their aiming levels after a switching event. Assume R_s = 0 Ω. **(6)**

b. Determine the time delay between the transistor T switching on and the relay's response action. Assume that T had been off for a long period before the switch on event. **(3)**

c. Find the time delay between the transistor T switching off and the relay's response action. Assume that T had been on for a long period before the switch off event and that R_s = 0 Ω. **(3)**

d. Determine the value of R_s that should be included in series with D to make the answer in part c equal to 2 ms. **(3)**

e. Using your solution from part d, determine the minimum collector-emitter voltage v_{CE} rating that T should have if resistor R_s is included.

Sketch the waveform you would expect to see for v_{CE} under these conditions. Show at least one complete period of the control voltage v_B. **(5)**

2. The circuit shown in Figure 2 is a simple series voltage regulator circuit, with an adjustable output voltage, V_{out}, which is controlled by varying R_v. The component values associated with this circuit are:

V_{dc} = 48 V, V_{ref} = 4 V, R_v = 10 kΩ,

R = 3.3 kΩ

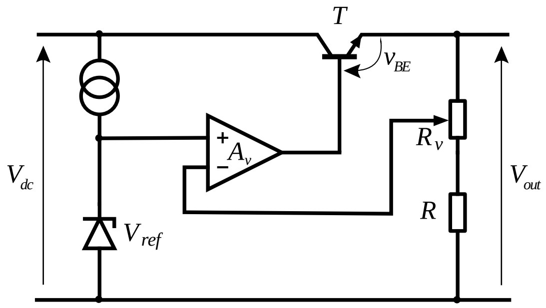

Figure 2

a. Derive an expression for the output voltage, V_{out}, of the circuit shown in Figure 2 in terms of V_{dc}, V_{ref}, R_v and R. You may assume that the setting of R_v can be modelled by two resistors R_{v1} and R_{v2} such that $R_v = R_{v1} + R_{v2}$ = 10 kΩ and that the gain of the error amplifier is ideal ($A_v = \infty$).

What are the minimum and maximum output voltages that can be obtained by adjusting R_v? **(4)**

b. By redrawing Figure 2, show how a current limiting capability could be added to the circuit. Explain how your current limiting circuit works.

Choose component values that would achieve a current limit level of 8A.

What power is dissipated in transistor *T* during a short circuit condition? **(7)**

c. Determine the efficiency of the regulator circuit if the input is connected across a 36 V DC supply and the regulator is to provide an output voltage of 12V across a 6 Ω load. You should include the effects of the power dissipated by your current limited circuit that you described in part b although you may assume that power dissipated by the feedback network R_v-R and the reference voltage generator are negligible. **(4)**

d. Derive an expression for the output voltage V_{out} of the circuit shown in Figure 2 if the error amplifier gain is not ideal ($A_v \neq \infty$).

Using your expression, determine the output voltage if A_v = 100 and the transistor base-emitter voltage drop is 0.7 V. **(5)**

3. a.

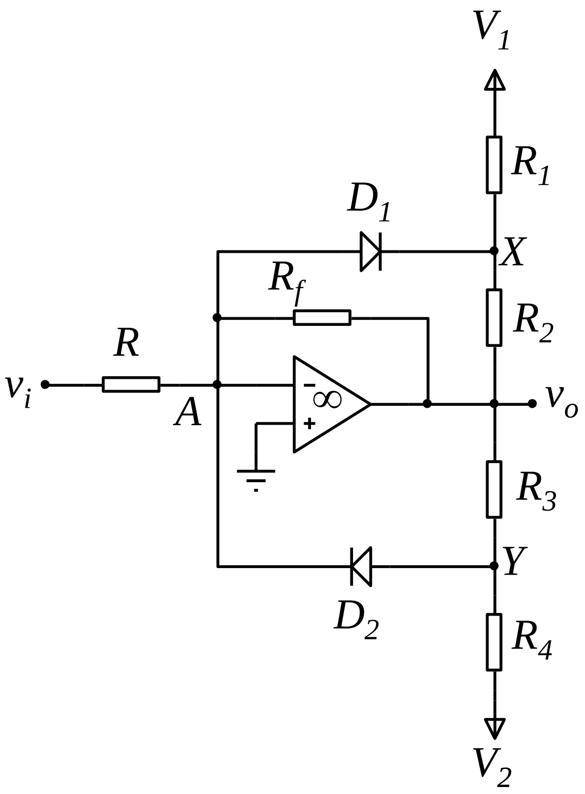

Figure 3: Waveform shaping circuit

Assuming R_1=R_4=R_a, R_2=R_3=R_b and V_1=-V_2=V_{ref}, sketch the v_o/v_i characteristic for the piecewise linear sections of the circuit shown in Figure 3, labelling the voltage transitions and the incremental gains of the circuit. **(6)**

b. Draw the circuit diagram of an op-amp based logarithmic amplifier using a diode as the logarithmic element. Derive an expression for the relationship between the input voltage v_i and output voltage v_o. **(3)**

c. Draw the circuit diagram of a logarithmic amplifier using 2 transistors and 2 operational-amplifiers.

Derive an expression for the relationship between the input voltage v_i and output voltage v_o. State any assumption you make in your derivation. **(6)**

d. Draw the circuit diagram of a bolometric RMS to DC converter. Explain the operating principles of your circuit. **(5)**

4. Figure 4 shows a buck-boost converter which can be provide output voltage magnitudes that are greater than or less than the input voltage. The output voltage is controlled by the ratio of the switch *S* on-time to off-time ratio.

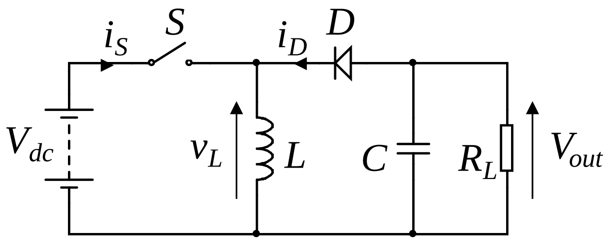

Figure 4: Buck-boost converter

V_{dc}	24 V
L	30 µH
C	47 nF
R_L	10 kΩ

Table IV

a. Draw the sub-circuits that represent the circuit behaviour when *S* is turned "on" and *S* is turned "off" paying particular attention the conduction states of the diode. Indicate the path of current flow on your diagrams. **(6)**

b. Sketch the waveforms of v_L, i_S and i_D as a function of time. On your waveforms label the switch on-time and off-time, t_{on} and t_{off} respectively. **(6)**

c. Derive an expression for the output voltage, V_{out}, as a function of V_{dc}, L, R_L, t_{on} and the switching period T. What output voltage would you expect if *S* was driven by a 150kHz square wave and the components used were as in Table IV. **(4)**

d. For the conditions given in part c., what is the value of peak-to-peak ripple voltage superimposed on V_{out}? **(4)**

MPF