EEE6042 Answers_06-07

1(a) The electronic configuration of the Si atom is $1s^2 2s^2 2p^6 3s^2 3p^2$. When the atom is bonded into the Si diamond cubic lattice, the outer electrons occupy four tetrahedrally disposed sp^3 hybrid orbitals. These overlap with orbitals of adjacent atoms and each bond, so formed, has two electrons, one each from the atoms on either end of the bond. The bond energy depends upon the interatomic separation as described by a Morse curve (diagrams needed).

1(b) Plane spacing $d_{hkl} = a_0 / \sqrt{(h^2 + k^2 + l^2)}$

For (002) $d_{002} = 0.5522/\sqrt{(0 + 0 + 4)}$nm
$= 0.2761$nm

For (112) $d_{112} = 0.5522/\sqrt{(1 + 1 + 4)}$
$= 0.2254$nm

For (212) $d_{212} = 0.5522/\sqrt{(4 + 1 + 4)}$
$= 0.1841$nm

For (114) $d_{114} = 0.5522/\sqrt{(1 + 1 + 16)}$
$= 0.1302$nm

1(c) Angle between planes $(h_1k_1l_1)$ and $(h_2k_2l_2)$ is given by
$\cos^{-1}[(h_1h_2 + k_1k_2 + l_1l_2)/\sqrt{((h_1^2 + k_1^2 + l_1^2)(h_2^2 + k_2^2 + l_2^2))}]$

$(001) \wedge (011) = \cos^{-1}[1/\sqrt{2}] = 45.0^o$
$(111) \wedge (112) = \cos^{-1}[4/\sqrt{18}] = 19.5^o$

1(d) Diagrams are required to show that an intrinsic stacking fault has a missing (111) plane section, whilst an extrinsic stacking fault has an extra (111) plane section. The twin diagram must show reversed stacking on a set of {111} planes.

1(e) A diagram of a tilt grain boundary showing edge type dislocations is required. Other types of grain boundary are the twist boundary and the mixed boundary. The twist boundary contains only screw dislocations.

1(f) Resistance of track $= 0.4$(length/width) Ω

Resistance (1μm) $= 0.4(3 \times 10^{-1}/10^{-4})\ \Omega$

$= 1.2 \times 10^3\ \Omega$

Resistance (5μm) $= 0.4(3 \times 10^{-1}/5 \times 10^{-4})\ \Omega$

$= 2.4 \times 10^2\ \Omega$

2 (a) **Chemical Vapour Deposition (CVD) of Epitaxial Si**

Several types of reaction involving Si-containing gases flowing over a heated substrate are possible

most important is the hydrogen reduction of silicon tetrachloride, which takes place on the heated surface

$$SiCl_4 + 2H_2 = Si + 4HCl$$

deposited Si atoms run around on the substrate and join steps at the edges of growing crystal planes extending across the surface

the deposition temperature is generally in the range 800-1200 C in order to give high quality, single crystal Si layers, with good thickness uniformity, at deposition rates in the range 0.01-5μm/min

prior to deposition, substrates would typically be given a vapour etch with flowing HCl or a bake in H_2 gas to clean their surfaces

A typical CVD apparatus has appropriate reagent and other gas lines feeding into a mixing manifold leading to the reaction chamber (diagram required)

the chamber generally has one of three generic designs, horizontal reactor, pancake (vertical) reactor and barrel reactor (diagrams required)

susceptor has wafers mounted upon it and is heated by RF coupling or by radiant heating from quartz halogen lamps

susceptor is often graphite coated with SiC since this will not react with any gases or introduce contaminants

gas flow in chamber must be very uniform to give layer thickness uniformity on each of the substrate wafers

Doping of grown layers is achieved by mixing a suitable hydride with the flowing hydrogen and $SiCl_4$ gases

arsine (AsH_3) or phosphine (PH_3) for n-type doping and diborane (B_2H_6) for p-type doping

must be careful to avoid so-called autodoping

diffusion of impurity from substrate must be outpaced by layer growth: can be checked by calculating the characteristic impurity diffusion length

The quality of epitaxial Si films must be high if they are to be employed for IC fabrication

if residual contamination is present on the substrate surface before epitaxy, stacking faults or even small pyramidal hillocks may be produced

nonuniform heating of the wafers can lead to slip and dislocation formation

(b) Diffusion coefficient $(D) = D_0 \exp -[E_A/kT]$

At 1100°C (1373K) $D = 0.76 \times \exp -[3.46/(8.62 \times 10^{-5} \times 1373)]$ cm^2/s

$= 1.53 \times 10^{-13}$ cm^2/s

For 60s $2\sqrt{(DT)} = 2\sqrt{(1.53 \times 10^{-13} \times 60)}$ cm

$= 6.06 \times 10^{-6}$ cm

$= 0.06\mu m$

This diffusion length is much less than the thickness of the Si layer grown per minute, therefore, autodoping of the layer should not be a serious problem

(c) Si and sapphire exhibit a very large misfit. The Si layer grows first in an islanded form and, due to the misfit, large numbers of strain-relieving defects are introduced. The latter include misfit dislocations, stacking faults and twins.

Si on sapphire can be employed where well isolated electronic devices are required. Isolation is produced by etching away the Si between the devices down to the level of the sapphire.

(d) (i) For the deposition of polycrystalline Si the growth temperature must be reduced towards about 600C.

(ii) For the deposition of amorphous Si the growth temperature must be reduced to somewhat below 600C.

3a) **Bipolar Transistor Fabrication**

The following fabrication steps are required:

- (a) n^+ buried layer formed by As^+ ion implantation followed by n-layer epitaxial growth
- (b) pad oxide/nitride growth with isolation resist applied
- (c) oxide/nitride etch and channel-stop B^+ implant (to overcome B depletion in the substrate during subsequent oxidation)
- (d) isolation oxide growth, remaining nitride removal
- (e)base B^+ implant through resist window
- (f) opening of base, emitter and collector contacts through resist window
- (g) emitter and collector contact areas selected by resist window for final As^+ implantation to give n^+ surface regions
- (h) finally, device passivated with layer of Si_3N_4, contact windows reopened and metallized

(diagrams required at the various stages)

- ***Special considerations*** for bipolar fabrication

- the initially-formed ***buried n^+ layer*** reduces the collector resistance

- the ***epitaxial layer*** should be as lightly doped as possible to minimise base-collector capacitance, with the constraint that the doping must be heavy enough to give low collector resistance

- the ***base width*** must be as narrow as possible to minimise the transit time for minority electrons (reducing hole-electron recombination and increasing transistor frequency response) while being doped heavily enough to withstand the reversed-bias collector/base voltage (avoiding punch-through current). The base contact area will also benefit from being more heavily p-doped, but this requires additional process steps

- the ***emitter*** must be as heavily doped and as shallow as possible to minimise emitter resistance. Also the transistor gain is determined by the minority carrier (hole) gradient in the emitter, since this establishes the base current. Thus, the gain can be increased by decreasing the hole gradient through use of heavily n-doped polySi to contact the emitter: this increases the hole lifetime compared to the use of metal and has been widely exploited for this purpose

▸Bipolar and CMOS transistor fabrication technologies are combined in BICMOS processing

- allows ICs with circuits containing both device types to be produced yielding advantages of merged functionality
  - however, processing is more complex and costly than for CMOS alone

3b) Diffusion coefficient (D) = $D_0 \exp -[E_A/kT]$

At 1200°C (1473K) $D = 12 \times \exp -[4.05/(8.61 \times 10^{-5} \times 1473)]\ cm^2/s$

$= 12 \times \exp -[31.94]\ cm^2/s$

$= 1.61 \times 10^{-13}\ cm^2/s$

For 30min $2\sqrt{(DT)} = 2\sqrt{(1.61 \times 10^{-13} \times 900)}\ cm$

$= 2.4 \times 10^{-5}\ cm$

$= 0.24\mu m$

4(a) **Thermal Oxidation of Si**

▸One of the key steps in the fabrication of Si semiconductor devices and ICs

▸Oxidation of Si is carried out in a ***furnace*** at, typically, 900-1200°C: two methods ***University of Sheffield***

- •oxidation with dry oxygen gas (***dry oxidation***)

  $Si + O_2 = SiO_2$

- •oxidation with steam (***wet oxidation***) - a faster process

  $Si + 2H_2O = SiO_2 + 2H_2$

▸Reaction kinetics

- •there are ***three steps*** in the oxidation process
  - ◦the oxidising species is ***transported*** from the bulk of the gas to the oxide/gas interface

    flux = $h_G (C_G - C_S)$ [h_G is mass-transfer coefficient]
  - ◦the oxidising species ***diffuses*** across the oxide layer already present

    flux = $D (C_0 - C_i)/x_0$ [D is diffusivity in oxide]
  - ◦the oxidising species ***reacts*** with the Si at the oxide/Si interface

    flux = $k_s C_i$ [k_s is reaction rate constant]
- •the rate determining step depends upon the oxide thickness (x_0)
  - ◦for ***small*** x_0, there is a large oxidising species flux across the oxide layer and the reaction at the oxide/Si surface is rate-limiting
  - ◦for ***large*** x_0, the flux across the oxide is small and this diffusion step is rate-limiting
- •combining the above equations and determining the rate of change of x_0, it is found that
  - ◦for small x_0, the rate of oxidation is ***linear***
  - ◦for large x_0, the rate of oxidation is ***parabolic***

- •MOSFET ***gate oxide integrity*** (GOI) is a vital parameter and it is adversely affected by
  - ◦***roughness/nonuniformities*** of the oxide thickness
  - ◦pre-existing ***particles*** of eg silica present in the Si which protrude into the gate oxide
  - ◦***transition element contamination*** giving deep levels in the Si or even precipitation/segregation at the Si/oxide interface

▸The effects of HCl additive

- •presence of HCl (giving Cl_2 by reaction $2HCl + ½O_2 = H_2O + Cl_2$) also ***increases*** the reaction rates
  - ◦HCl ***reduces metal contamination*** of the grown oxide due to the formation of volatile chlorides: both alkali metals (Na, K, etc which form charged ions that are mobile under bias even near room temperature) and transition elements are removed
  - ◦the use of HCl suppresses ***stacking fault formation*** in the Si during oxidation and also makes the precipitation of transition elements less likely.

4(b) **Deposition of Insulating Layers**

- ***Chemical vapour deposition*** of SiO_2 and Si_3N_4
  - at ***atmospheric pressure*** (APCVD) giving high deposition rates at relatively low temperatures
    - relatively poor layer uniformity and step coverage; higher contamination
  - at ***low pressure*** (LPCVD) with larger molecule mean-free-path giving better layer uniformity and step coverage, together with better purity
    - higher temperature deposition and lower deposition rates
  - with ***plasma enhancement*** (PECVD) giving fast deposition at low temperatures
    - some chemical and particulate contamination
- SiO_2 films
  - often formed by the ***pyrolytic oxidation*** of alkoxysilanes (eg tetraethylorthosilane (TEOS)) $Si(C_2H_5O)_4 + 12O_2 = SiO_2 + 8CO_2 + 10H_2O$
    - films may be poor quality due to incorporation of by-product water and are in compression
  - can be formed by reaction of silane with oxygen

    $SiH_4 + O_2 = SiO_2 + 2H_2$
    - better quality but may require densification: films are in tension
    - with simultaneous pyrolysis of phosphine, silica doped with phosphorus (***phosphosilicate glass***, PSG) is produced

      PSG has ***lower built-in stress*** and an increased thermal expansion coefficient giving a better match to underlying semiconductor and enhanced film stability
- Si_3N_4 films
  - typically deposited by LPCVD and PECVD by combination of either silane or dichlorosilane with ammonia

    $3SiH_4 + 4NH_3 = Si_3N_4 + 12H_2$

    $3SiCl_2H_2 + 4NH_3 = Si_3N_4 + 6HCl + 6H_2$
  - films often used for their ability to block diffusion of both water and sodium
    - widely used in both Si and GaAs technology
  - films may be ***highly stressed*** depending on method of deposition