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4^{th} lecture:

- 2 transistor circuit elements:
  - differential pair (continued)
  - current mirror (basics)
- multiple transistor circuit elements:
  - current mirrors (advanced)
  - output stages (introduction)

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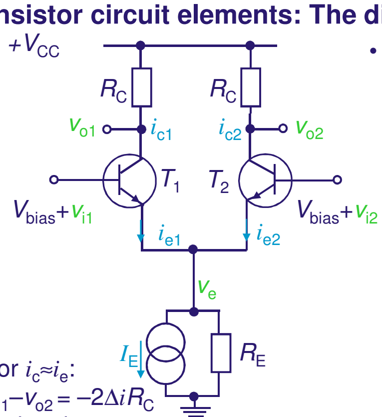
2 transistor circuit elements: The differential pair (emitter coupled pair)

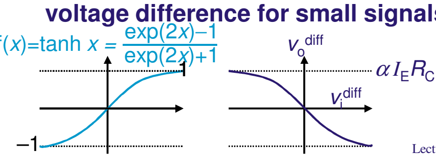


- $\boxed{v_o^{diff}=v_{o1}-v_{o2}}$
  $=-2\,½(i_{c1}-i_{c2})R_C$
  $=(i_{c2}-i_{c1})R_C$
  $=\alpha I_E R_C\,\{1/[1+\exp(+v_i^{diff}/V_{to})]$
  $-1/[1+\exp(-v_i^{diff}/V_{to})]\}$
  $\boxed{=\alpha I_E\,R_C \tanh(-v_i^{diff}/2V_{to})}$

where tanh x is a function that is symmetrical about the origin and converges to unity for $x\to\infty$, i.e. we have a **linear relationship between output voltage difference and input voltage difference for small signals**!

output for $i_c \approx i_e$:
$v_o^{diff}=v_{o1}-v_{o2}=-2\Delta i R_C$
is proportional to **current difference** through $T1$ and $T2$
problem: for BJT not proportional to **voltage difference**

$f(x)=\tanh x=\dfrac{\exp(2x)-1}{\exp(2x)+1}$



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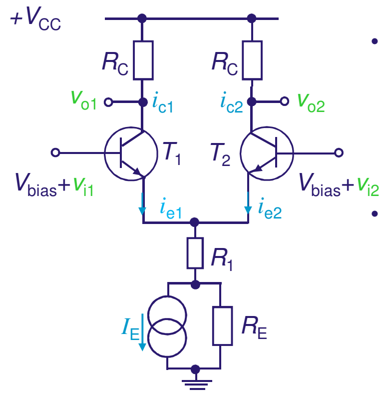
2 transistor circuit elements: The differential pair (emitter coupled pair)



- **note on emitter degeneration**: add R_1 to the joint emitters provides negative feedback: if i_c rises, i_e increases, thus also the voltage drop across R_1, which reduces the bias and thus drives i_b and i_c back.
- in detail: look at Ebers-Moll equation: $v_{be}=V_{to}\ln(i_c/i_s)$
  If one must provide higher base voltages to T_1 and T_2 to get the same i_c with R_1 present, then this also means the non-linear $i_c(v_{be})$ regime begins only at higher voltage; i.e. ***R*₁ effectively extends the linear region**!

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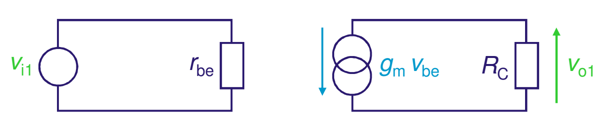
2 transistor circuit elements: The differential pair (emitter coupled pair)

calculation of differential mode gain A_{dm}:

- consider
  $v_{o1}\to v_{o1}+\Delta v$, $i_{c1}\to i_{c1}+\Delta i$, hence also
  $v_{o2}\to v_{o2}-\Delta v$, $i_{c2}\to i_{c2}-\Delta i$
- As total current I_E into current source and resistor R_E stays constant, no changes occur below the emitters of T_1 and T_2 and we can replace this part with a short circuit and only need to consider T_1 (no need to worry about T_2 since T_1's emitter is tied to ground from small signal point of view). Thus get the differential mode half-circuit:



$v_{o1}=-g_m v_{be} R_C=-g_m v_{i1} R_C$
with $v_{i1}=-v_{i2}=v_i^{diff}/2$ and $v_{o1}=-v_{o2}=v_o^{diff}/2$,
hence $\boxed{A_{dm}=v_o^{diff}/v_i^{diff}=2v_{o1}/2v_{i1}=-g_m R_C}$

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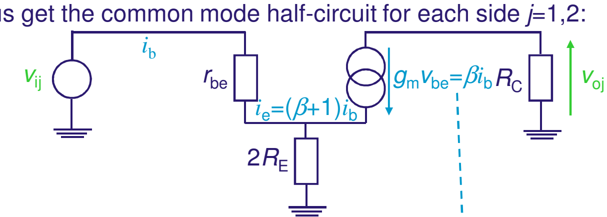
2 transistor circuit elements: The differential pair (emitter coupled pair)

calculation of common mode gain A_{cm}:

- replace single RE with two parallel branches, each with resistance 2RE
- As left and right halves of circuit are completely identical and the drives signals to both sides also, no large signal current will flow between emitters between T_1 and T_2. As there is no interaction between both halves, we can split circuit down the middle and consider just one half. Thus get the common mode half-circuit for each side j=1,2:



Kirchhoff's Law: $v_{ij} - i_b r_{be} - i_b(\beta+1)2R_E = 0$, thus $i_b = v_{ij}/[r_{be}+2R_E(\beta+1)]$

Also: $v_{oj} = -\beta i_b R_C$

Put together: $\boxed{A_{cm}} = v_{oj}/v_{ij} = -\beta R_C/[r_{be}+2R_E(\beta+1)] = \boxed{-g_m R_C/[1+2g_m R_E(1+1/\beta)]}$

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2 transistor circuit elements: The differential pair (emitter coupled pair)

common mode rejection ratio (CMRR):

- aim: for differential amplifier, maximise gain A_{dm} in differential mode (= gain for opposite voltage signals) and simultaneously, minimise gain A_{cm} for identical input voltages applied to both inputs
- use as a quality factor the common mode rejection ratio (CMRR) defined as the dimensionless ratio
  $\boxed{\mathrm{CMRR}=|A_{dm}/A_{cm}|=1+2g_m R_E(\beta+1)/\beta}$
- CMRR increases with g_m, and as $g_m v_{be}=\beta i_b$ it is best to use BJTs with large β and operate them at high current.
- **at high frequencies: Z=1/($j\omega C_{cb}$)** || R_C decreases R_C^{eff} for small signals, which thus **reduces A_{dm} (not A_{cm} !) and thereby CMRR**.
- notes on differential amplifiers using FETs:
  - ~ **JFETS are better than MOSFETs** for this as they have lower noise.
  - – **Differential gain of FETs is lower** than for differential amps based on BJTs, due to smaller g_m.
  - \+ **FETs give much wider linear operation** than BJTs as current varies only like the square rather than exponentially with voltage.

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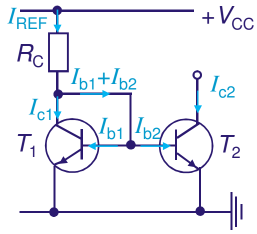
2 transistor circuit elements: The simple current mirror



- definition: two **identical transistors T_1 and T_2 connected at their base terminals and their emitters**
- work out current ratio from sum over currents at collector of T_1:
  $I_{REF}-I_{b1}-I_{b2}-I_{c1}=0$
  with identical transistors: $I_{b1}=I_{b2}$, same β
  hence: $I_{REF}-2I_{c1}/\beta-I_{c1}=0$
  thus:
  $I_{c2}=\beta I_{b2}=\beta I_{b1}=I_{c1}=I_{REF}/[1+2/\beta]$
  $\boxed{I_{c2}/I_{REF}=1/[1+2/\beta] \approx (1-2/\beta) \cong 1}$
  The current flowing down the left hand branch is mirrored approximately (within few %) in the right hand side. Note $I_{c2} \leq I_{REF}$ because $1/(1+2x) \approx 1-2x$ for small x. Also note the **strong β dependence**.

note 1: take β=100 [200, 400];
then I_{c2}/I_{REF}=0.98 [0.99, 0.995]

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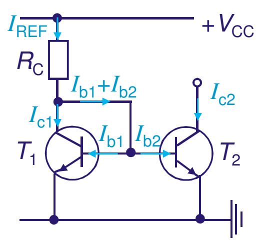
2 transistor circuit elements: The simple current mirror



- result: collector of T_2 provides constant **current source output with large output impedance** (= that of T_2) **and large output current simultaneously** (single transistor provides either large gain $g_m R_C$ or large $I_c \sim 1/R_c$)**.** These circuits are good in suppressing power supply ripples and have a footprint much smaller than an equivalent resistor.
- **consider Early effect** (due to base width reduction with increasing V_{cb}) which means I_c depends on $V_{ce}=V_{cb}+V_{be}$ via the Early voltage V_A:
  $I_c=I_S \exp(V_{be}/V_{to})(1+V_{ce}/V_A)$
  Assume identical transistors:
  $\boxed{I_{c2}/I_{c1}=[1+V_{ce2}/V_A]/[1+V_{ce1}/V_A] \geq 1}$

note 2: for $V_{ce2}>V_{ce1}$ this ratio is always a bit larger than unity, which more than counter-balances the previous tendency that I_{c2} is always a bit too small, e.g. for V_{ce1}=1V, V_{ce2}=15V, V_A=100V: I_{c2}/I_{c1}=1.139.

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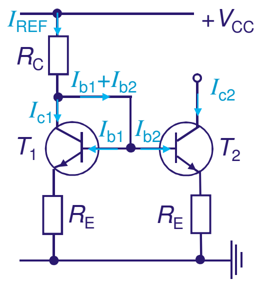
2 transistor circuit elements: current mirror with degenerated emitter



- use emitter degeneration with additional R_E's to compensate the Early effect by negative feedback stabilisation
- advantage: increases output impedance to $r_{ce}(1+g_m R_E)$
- disadvantage: sacrifices available output voltage swing by voltage drop across R_E

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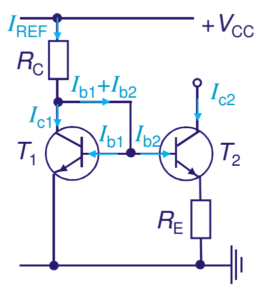
2 transistor circuit elements: Widlar current source



- use only **one** resistor R_E on transistor T_2 to determine output current
- advantages:
  - I_{c2} can now be adjusted by R_E:
    $V_{be1}=V_{CC}-I_{REF}R_C$ (if r_{ce} negligible)
    $V_{be2}=V_{be1}-I_{e2}R_E$, hence for $\beta>>1$
    $=V_{be1}-I_{c2}R_E$
    $= V_{CC}-I_{REF}R_C-I_{C2}R_E$,
    thus
    $\boxed{I_{c2}=[(V_{CC}-V_{be2})-I_{REF}R_C]/R_E}$
    is **ideal for low output currents**
  - if R_E=0 (normal current source) all the voltage $V_{CC}-V_{be1}$ drops across R_C, which for small currents would result in unrealistically large R_C values
  - output impedance is increased to $\boxed{r_{ce}[1+g_m(R_E||r_{be})]}$

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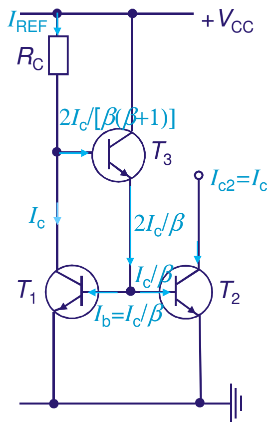
3 transistor circuit : current mirror with base-current compensation



- third transistor T_3 supplies the base currents to T_1 and T_2
- consider currents for matched T_1 and T_2 to get
  input current:
  $I_i=I_{REF}=I_C+2I_C/[\beta(\beta+1)]$
  output current:
  $I_o=I_{c2}=I_C$, hence
  current gain:
  $\boxed{I_o/I_{REF}=1/\{1+2/[\beta(\beta+1)]\} \approx 1/(1+2/\beta^2)}$
  is **better than simple current mirror**
- problem: output resistance $\approx r_{ce}$ is still low

note : take e.g. $\beta=100$ [200];
then $I_{c2}/I_{REF}=0.9998$ [0.99995]

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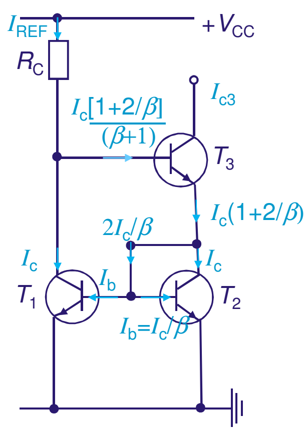
3 transistor circuit elements: Wilson current mirror



- third transistor T_3 acts as a common base element because it only transfers its emitter current to its collector
- input current:
  $I_i=I_{REF}=I_C\,[1+(1+2/\beta)/(\beta+1)]$
  output current:
  $I_o=I_{c3}=I_C\,(1+2/\beta)\beta/(\beta+1)$, hence
  current gain:
  $\boxed{I_o/I_{REF}} = (\beta+2)/[\beta+1+(\beta+2)/\beta]$
  $= (\beta+2)/(\beta+2+2/\beta)$
  $\boxed{\approx 1/(1+2/\beta^2)}$ as before

neglected so far: collector-emitter voltages of T_1 and T_2 are not equal, hence small current offset $I_{c1}\neq I_{c2}$ introduces systematic error that needs to be solved by adding diode in series with collector of T_2

note : take e.g. $\beta=100$ [200];
then $I_{c3}/I_{REF}=0.9998$ [0.99995]

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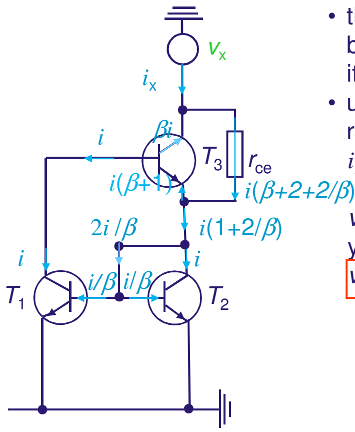
3 transistor circuit elements: Wilson current mirror



- third transistor T_3 acts as a common base element because it only transfers its emitter current to its collector
- use $i=I_c$ and consider improved output resistance for $R_C=\infty$ and load:
  $i_x=2i(1+1/\beta)$ and
  $v_x=(\beta+2+2/\beta)ir_{ce}+ir_{be}(1+1/\beta)$
  yields **increased output resistance** of $\boxed{v_x/i_x \approx \beta r_{ce}/2}$

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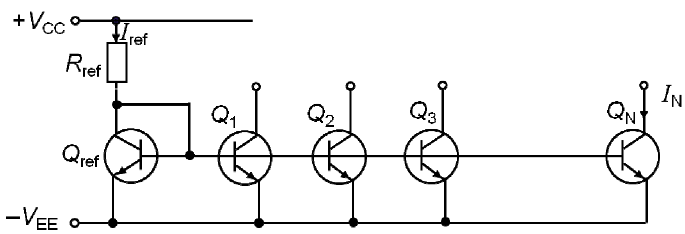
N-transistor circuit elements: extended current mirrors



- at the node just below R_{ref} apply Kirchoff's Law to the sum of currents:
  $I_{ref}= I_{C,ref} + I_{b,ref} + I_{b,1} + i_{b,2} +\ldots + I_{b,N}=(\beta+N+1)\ I_b$
- at the output: $I_o=I_{C,N}=\beta I_b$
- hence, the ratio: $\boxed{I_o/I_{ref}=\beta/(\beta+\underbrace{N}_{1\leq N<<\beta}+1)}$ (which for N=1 yields the former result)

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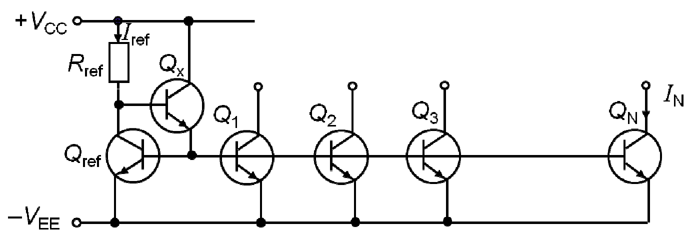
N-transistor circuit elements: extended current mirrors



- at the node just below R_{ref} apply Kirchoff's Law to the sum of currents: $I_{ref}= I_{C,ref} + (I_{b,ref} + I_{b,1} + i_{b,2} +\ldots + I_{b,N})/(\beta+1)=[\beta+(N+1)/(\beta+1)]\, I_b$
- at the output: $I_o=I_{C,N}=\beta I_b$
- hence, the ratio: $\boxed{I_o/I_{ref}=\beta/[\underbrace{\beta+(N+1)/(\beta+1)}_{(N+1)/(\beta+1)<<1\le N<<\beta}]}$

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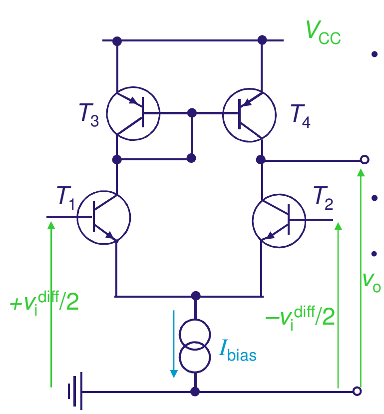
4 transistor circuit elements: differential amplifier



- use **differential pair T_1&T_2 plus current mirror T_3 & T_4**
- consider currents through T_1 and T_2: $I_{bias}/2\pm g_m v_i^{diff}/2$
- consider current at output node: $I_o=I_{c4}-I_{c2}$ where the collector current of T_1 is mirrored in T_4 such that we get $I_{bias}/2+g_m v_i^{diff}/2=I_{c1}=I_{c4}=I_o+ I_{bias}/2-g_m v_i^{diff}/2$, $\boxed{I_o=g_m v_i^{diff}}$
- for small load impedance $R_L<<r_{ce}$ the output voltage then is $\boxed{v_o=g_m v_i^{diff} R_L}$
- For simple resistors instead of T_3 & T_4 but with equal magnitude to the output resistance of the BJTs these would give, for same load R_L and change in collector current $g_m v_i^{diff}/2$ at T_2, only half that output voltage as the output of T_1 branch would be wasted. The current mirror transfers it to T_4 and uses this to **double the gain**.

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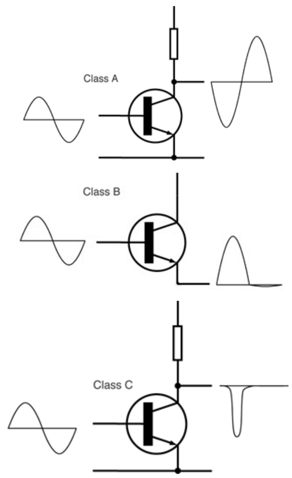
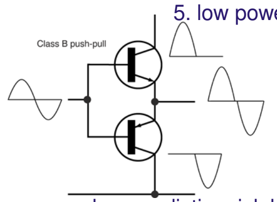
output stages: introduction



aims:
1. deliver power into the load
2. distort signal as little as possible
3. should not limit IC frequency response
4. low output impedance to ensure output voltage remains unaffected by load
5. low power consumption



classes: distinguish between different bias modes
- class A: V_{bias} large and positive so that BJT is always on: excellent linearity but poor efficiency
- class B: V_{bias}=0 so that BJT on only for one half: good linearity and efficiency
- class C: V_{bias}<0 so that BJT is just on near peak: poor linearity but excellent efficiency

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output stages: example of an audio amplifier