The University Of Sheffield.

Electronic & Electrical Engineering.

EEE6225 SYSTEM DESIGN

Credits: 15

Course Description including Aims

This unit is concerned with the management of complexity in system design. To learn the basics of structured approach to design of complex systems, students undertake a design project that requires the application of state of the art design tools that help to achieve appropriate error free design structures. The unit is continually assessed at various stages in the design process and these assessments combine to give a grade for the unit.

1. To demonstrate the importance of structured design for complex systems.
2. To provide a working understanding of a standard Hardware Description Language (HDL) which is an aid to structured, error-free design.
3. To provide an appreciation of the special restrictions imposed when using an HDL to design a realisable digital system via synthesis.
4. To give practical exposure to the refinement of a specification through partitioning and design to simulation against a defined set of constraints.

Outline Syllabus

Design Cycle : requirements, specification, design, simulation, implementation, test and integration. **Simulation :** functional v. circuit, concepts, advantages and disadvantages. **Description and Simulation Languages :** Verilog, VHDL & SystemC. **Verilog/VHDL** : concepts, syntax, behaviour and structure, hierarchy, portability, standards. **Verilog/VHDL for Synthesis:** The synthesisable subset, standard methodologies, register transfer level (RTL) design. **Design Exercise.**

Time Allocation

12 hours lectures, 12 hours hands-on tutorials, 40 hours of laboratory sessions

Recommended Previous Courses

Basic knowledge of Systems Engineering

Assessment

Assessment is by written report to be submitted by the end of the exercise and various milestones throughout the project. The report will contain the following:

1. a brief report on initial literature survey, current good practice, types of solutions available, solution complexity etc.
2. a copy of the design specification agreed with the supervisor near the start of the exercise, after the initial literature search.
3. a copy of the design schedule used to ensure that the project goals are achieved within the time and resource allowances.
4. a report on the final "product". This will include a complete description of the final system, simulation results, theoretical performance and an analysis of any deviation from expected

performance.

5. all code written to support the system.

Marks are rewarded on the basis of the following categories:

1. 20% Evidence of a design process throughout the project and in the report.
2. 20% Relationship with existing solutions and quality of choices made in fixing the specifications.
3. 20% Results obtained including achieved performance relative to initial specifications, and relative to expected performance. Analysis of performance.
4. 20% Communication skills in written report.
5. 20% Innovation and initiative.

Recommended Books

Vahid F, Lysecky R	*Verilog for Digital Design*	John Wiley
Zeimer & Peterson	*Introduction to Digital Communications*	McMillan

Objectives

By the end of the module successful students will have demonstrated

1. the specification, design and simulation of a complex digital system using FPGA technology.
2. working in a design team responsible for managing the HDL based design of a digital system.
3. the ability to gather a range of information and literature on a specific algorithm (AES) and prior implementations and to use those to inform the design and implementation of a digital system.
4. the use of industry standard design techniques and design tools.

Detailed Syllabus

1. Systems, design methodologies, concept of abstract design. Computer Aided Design, Hardware Description Languages (HDLs) and their benefits to the design process.
2. Modelling, hierarchies and partitioning. VHDL, Verilog and SystemC. Basic elements of VHDL, behavioural modelling and signals.
3. Design organisation, Verilog model of time, concurrency, and the simulator.
4. Data types. Packages. Structural Verilog, modules and configurations.
5. Subset of Verilog for synthesis. Methodologies for effective synthesis (Register transfer level {RTL}design, etc.).
6. FPGA implementation of synthesisable Verilog. Size and speed issues.

7-12. Tutorials covering Introduction to tools, basic Verilog simulation and synthesis. FPGA speed and area issues. GF arithmetic implementations.

13-24. Design exercise – AES on FPGA either high throughput or low area including lectures on cryptography, AES algorithm, GF arithmetic and design trade-offs in AES sub-blocks

UK-SPEC/IET Learning Outcomes

Outcome Code	Supporting Statement
SM1m / SM1fl	Producing a successful design in this module requires the student to understand and apply design trade-offs that stem from a deep understanding of the engineering/ science and mathematics behind the functionality required; specifically in terms of Galois Field mathematics, cryptography, Digital design methodology, FPGA implementation, system design and security application requirements.
SM2m	Students will use Galois Field arithmetic as the underlying arithmetic of their system and will adopt Verilog or VHDL as the HDL for the modelling and implementation of their system. The trade-offs in terms of high-throughput versus low area will provide the students with an appreciation of the practical limitations and the importance of early design decisions and their effect on what is produced.
SM4m	The students on this course will be exposed to selecting suitable FPGA platforms and will be aware of the latest AES designs they need to compete against based on the literature – they will use this knowledge to inform their own approach to the design.
SM2fl	The students on this course will be exposed to selecting suitable FPGA platforms and will be aware of the latest AES designs they need to compete against based on the literature they will use this knowledge to inform their own approach to the design.
EA1m / EA1fl	Knowledge of fundamental digital logic and arithmetic is necessary to allow students to comprehend (particularly) the implementation of GF arithmetic. Critical analysis will be required to allow the students to match with the constraints set for their problem
EA2m	Students use modelling and simulation to confirm the behaviour of their design against the specification and to assess its performance against defined metrics – speed, and area.
EA3m	In this case the engineering problem is to design an AES codec and students will use Galois Field arithmetic, Verilog and ISE/Modelsim, MATLAB etc.
EA4m	Students are encouraged to take a system-view when designing their AES component. In particular, they are provided with an environment in which it is expected to work and to which it must be interfaced. They are also expected to consider the scenarios for use of the component. In design terms, a top down hierarchical approach to design is encouraged.
EA5m	The module is concerned with advanced digital design in a realistic setting where the students will refine their system against high-level specification down to RTL level.
EA6m	The metrics for assessing their design and comparison to existing solutions in terms of throughput/slice for example
EA2fl	The module is concerned with advanced digital design in a realistic setting where the students will refine their system against high-level specification down to RTL level.
D1m / D1fl	The design is derived from a specification and, essentially, the constraints imply a particular use-case (i.e. customer requirement) and students are expected to consider the implications of this.
D2fl	Students follow well-defined design methodologies and processes. They recognise and appreciate that the cost of failing to do so is often failure. This is particularly the case because they design cooperatively and then have to ensure that the design meets the specification when integrated.

D3m / D3fl	Students are given a 'loose' specification and then have to work to interpret what this means. They are required to model the algorithms and decide on the best method to implement (based on design constraints). They recognise that decisions made at a relatively abstracted level and have a significant effect on the performance of the component that they design. They are expected to look for novel solutions to solve problems.
D4p	The project is entirely concerned with the creation of a new design and students are encouraged to think laterally about the possible solutions. Students are expected to consider context, reusability, etc.
D5m	Students work in groups and must jointly manage the design process and to ensure that the design as envisaged can be jointly worked on and integrated to yield a working component mindful of the contraints and the context in which it assumed to be implemented. Moreover, they are assessed in this process via regular milestones.
D7m	By the end of the exercise, the students would have a good understanding of a digital system design methodology and have the skills to apply this to a wide range of application. The AES exercise undertaken in this module is an excellent vehicle for illustration of the typical challenges encountered in a digital system design. Although they use FPGAs, some students may use timing analysis to improve performance and may well look at floor-planning.
D8m	The design exercise provides ample scope for innovative solutions; in fact in a number of occasions the students have been able to produce solutions that lead to published papers.
ET3p	The project is group based and whilst management is not a specific part of the brief they necessarily need to mange the process to achieve any result.
EP2m	The use of ISE, which provides a window onto a more general ASIC process (in part).
EP3m	Students use industry-standard tools: ISE and Modelsim.
EP4m	Students need to consider a range of technical literature e.g. FIPS-197 and academic papers to help derive their own solution.
EP7m	Students are expected to collaborate on a joint product, requiring a comprehension of planning, methodology and common standards. This extends to documenting and presenting their product.
EP9m	The students will understand in this module the current techniques and methodologies used in digital system design before undertaking the exercise.
EP10m	The students will use FPGA devices and technology as the implementation platform.
EP11m	Students work in teams and self-organise taking on appropriate roles.
EP1fl	The use of ISE, which provides a window onto a more general ASIC process (in part).
EP2fl	The students will understand in this module the current techniques and methodologies used in digital system design before undertaking the exercise.
EP3fl	The students will use FPGA devices and technology as the implementation platform.
EP4fl	Students work in teams and self-organise taking on appropriate roles.

All of these outcomes are assessed as part of the overall design process via the milestones:

1 Modelling of the problem
2 Initial sub-component designs and proposed organization
3 Integrated system and simulations
4 Group operation
5 Presentations
6 Log books