EEE 6393 Examination 2010

Worked solutions (Q1 and Q2)

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Question 2010GW1

1A

The incorporation of more than one integrated circuit (IC) inside a single package is now becoming commonplace. One production method for system in package (SiP) involves the vertical stacking of silicon wafers and the use of through-silicon vias (TSV) for vertical interconnections. Discuss the new technical challenges that have arisen as a result of the adoption of this technology and how they are being solved. (8)

1A ANSWER

Deep via etching: plasma (DRIE) or laser

Via isolation: thermal oxide (via first only), polymer

Seed layer deposition

3d photolithography

Via filling: copper, tungsten, poly-silicon

Wafer thinning: grinding, chemical-mechanical polishing, plasma clean.

Wafer handling: carrier wafer bonding/de-bonding.

Wafer bonding: thermo-compression, adhesive

Integration scheme: W2W, C2W, C2C

Interposer: silicon, glass (with possible embedded components/passives) for signal redistribution

Ball grid array for attach to substrate.

1B

The high pin count of a typical system in package (SiP) means that it is normally attached to the printed circuit board using a ball grid array (BGA). Describe how the array of solder balls is formed and how the BGA package it is attached to the substrate. (4)

1B ANSWER

Under bump metallization to prevent diffusion and brittle intermetallics formation.

Passivation

Solder mask

Screen print of solder paste

Reflow to form balls

Screen print of lower T_{melt} solder onto substrate

Pick and place of component

Reflow solder

Underfill for stress relief

1C

The yield for the fabrication of 200 identical flash memory ICs on a single wafer is 99% and the yield for interconnecting one wafer to another using TSV is 98%. What would be the yield for a vertical stack of 5 wafers? (4)

1C ANSWER

Final yield = $0.99^5 \times 0.98^4 = 0.877 =$ **88 %**

1D

A miniature camera module consists of a CMOS image sensor IC mounted on top of a controller IC which is in turn mounted on a signal redistribution substrate. Interlayer connections between all layers are made with TSVs. The wafer level yield for the manufacture of the image sensor is very low (80 %) compared to the other manufacturing steps. Suggest ways in which the yield of the finished module could be kept high. (4)

1D ANSWER

Dice camera chip module, then test, then only use known good die in assembly onto controller IC wafer (i.e. chip on wafer). Then dice populated controller IC wafer, then test again, then attach know good modules onto redistribution substrate.

Question 2010GW2

2A

A total of 5 W needs to be dissipated into a heat sink from a 20x20 mm quad flat pack (QFP) surface mount package containing a silicon integrated circuit. The junction-to-case thermal resistance of the package R_{jc} = 8 °C/W. What thermal resistance should the heat sink have in order to maintain the silicon at a safe working temperature? State the assumptions that you have made. (5)

2A ANSWER

Q = 5W

Assume: $T_{ambient}$ = 20 °C, T_{max} = 125 °C, therefore $\Delta T = T_{max} - T_{ambient}$ = 105 °C

$\Delta T = QR_{total}$, therefore $R_{total} = \Delta T/Q = 105/5 = 21$ °C/W

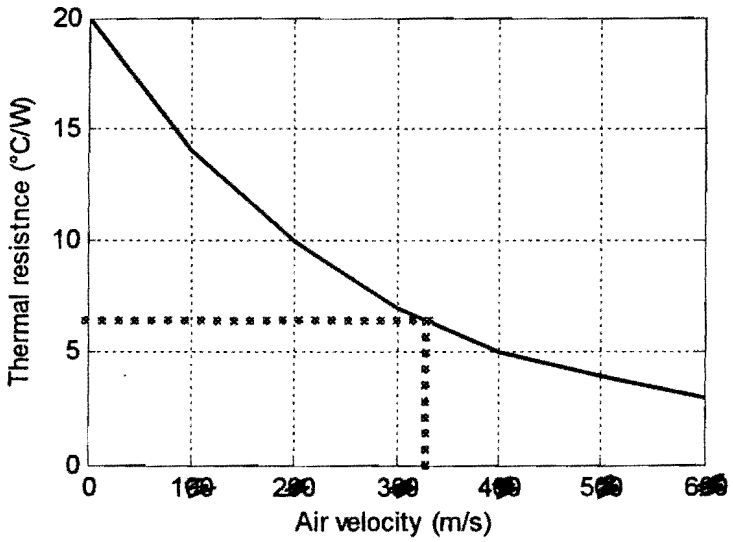
$R_{total} = R_{jc} + R_{heatsimk}$, therefore $R_{heatsink} = R_{total} - R_{jc} = 21 - 8 =$ **13 °C/W**

Note: Assume $R_{heatsink}$ includes interface resistance.

2B

A revision to the IC is packaged in the same QFP described above, however it must be operated at 110 °C or below, inside an enclose with an air temperature of 40 °C. It is decided that a finned heat sink plus a fan need to be mounted on top of the IC in order to ensure safe operation. Using the graph below, determine the minimum volume flow rate (m^3/hour) that the fan must deliver. (5)

2B ANSWER



Modified by GW. 9/4/10

Q = 5 W

ΔT = 110-40 – 70 °C

$R_{total} = \Delta T/Q = 70/5 = 14$ °C/W

Therefore $R_{heatsink} = R_{total} - R_{jc} = 14-8 = 6$ °C/W

Therefore, from graph: v = ~~330~~ 3.3 m/s

Assume area of fan = area chip = 2 x 2 cm = 4 cm^2 = 4 x 10^{-4} m^2

Therefore volume/s = ~~330~~ 3.3 x 4x10^{-4} = ~~0.132~~ 0.00132 m^3/s

Volume/hour = volume/s x 60 x 60 = ~~475~~ 4.75 **m^3/h**

2C

Why would it not be a good idea to use solder to attach the heatsink? (2)

2C ANSWER

Solder reflow temperature may exceed T_{max}.

Large TCE mismatch would result in stresses which would result in bowing or cracking of substrate.

2D

The QFP package contains a microprocessor that needs to be connected to a separate co-processor with a high speed 64-bit bus. Discuss the possible arrangement of a multilayer glass fibre/epoxy printed circuit board (PCB) that would allow this.

(5)

2D ANSWER

Controlled impedance tracks, preferably stripline - i.e. tracks enclosed by ground plane.

Rounded corners

Minimise track lengths

Maximise track separation

Separate power plane

2E

What new technology is proposed to further increase inter-chip communication speed on PCBs? (3)

2E ANSWER

Opto-electronic circuit board with wave guides embedded in PCB and laser diodes/ photodetectors for transmit and receive.

Q3 Worked solutions EEE6393 Q3 & Q4. 2010

Mark Hopkinson

a) System on a Chip (SoC)

Integration onto a single die (single piece of Si)
All (or most) of the components of an electronic system
- such as digital, analogue, low freq, high freq
with possible RAM (though normally off chip) +1 Mark

System in a package (SiP)

consists of a number of ICs (pieces of Si) enclosed
in a single package which then performs the majority
of operations of the system (similar to the above)
Planar ICs bonded to a substrate or (more recently
stacked ICs with ceramic insulators and interconnected
by flip-chip. 1 mark

SoC gives the highest density (smallest package)
and provides low parasitics for high speed / low noise
ICs can be fully optimised without the constraint
of external interconnects.
Configuration is very compatible with embedding
+ stacking approaches. (good compatibility with SiP.
Enables specialised devices ~~benefitting from the Si~~
1 mark

However SoC can be difficult to implement in the fab
- need for diverse technologies and architectures.
(eg: could be CMOS/Bipolar)
- performance can be compromised.

Particularly difficult to integrate high Power circuitry and high frequency (RF)

Noise isolation between elements of the SoC can be a major problem.

Above all, designing and implementing a full SoC layout is expensive in terms of development costs.
1 mark

SiP - Shorter development times / lower cost
- Better integration of diverse technologies (less compromises)
- Better isolation between function.
- flexibility in the choice of IC die including taking from existing designs.
- overall much lower tooling cost + risk.

But not the ultimate in miniaturisation or without the ultimate capabilities of the SoC approach if designed well.

1 mark.

b) $\text{Terminals} = k\,\text{Gates}^{p}$

$k = 0.25 \quad p = 0.5$

$T = 306.$

DIL - 2 sides $\frac{306}{2} = 153$ QFP 4 sides $\frac{306}{4} = 76.5.$

c) Si

minimum size. = chip size. = 10mm.

$\frac{10\times10^{-3}}{157} = 65$ $\frac{10\times10^{-3}}{76.5} = 130$

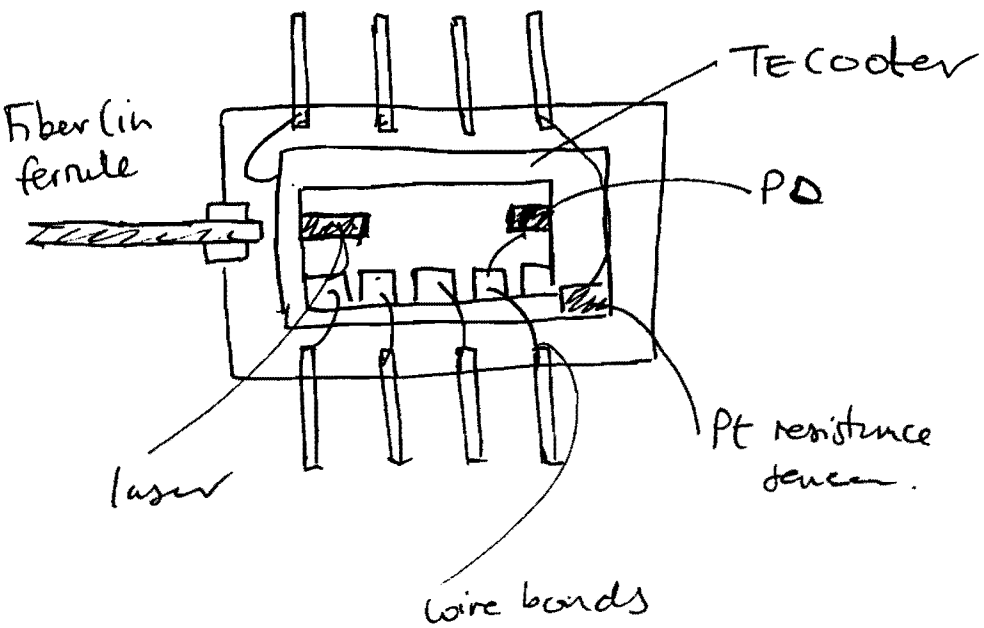
min bond pad dimension of 100μm rule of the DIP approach.

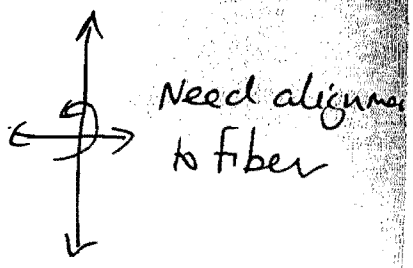
d). Edge emitting laser (Telecoms).

Normally In bonded to an alumina tile which is then bonded to a TE cooler (Peltier). A ~~ther~~ Pt resistance termometer is also bonded to the tile, as is usually a photodiode

Normally packaged in either metal (Gold plated Brass) DIP (Butterfly) or metal can ~~with~~ which has a ferrule for the insertion of the fibre

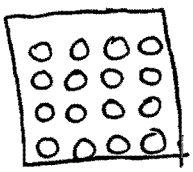
Laser in DIP (Butterfly)



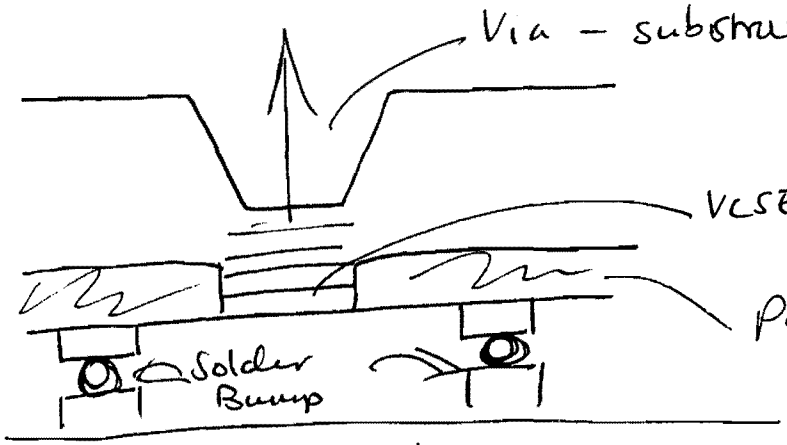


VCSEL

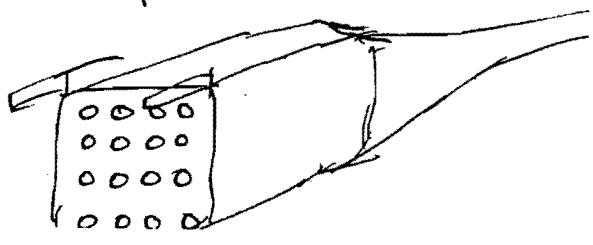
VCSEL is surface emitting - The device does not need to be cleaved and mounted edge on.



VCSEL Array - compatible with wire bonding or flip chip integration onto the Si substrate
eg: 4x4



Connector - usually plastic fiber bundle



1e)

1x1 mm chip - dissipating 850mW

$R = \ln(r_2/r_1)/2\pi kL$ — assuming radial spreading

$k = 30$

$R_1 = 0.5$ $\quad R = 8.8\,°C/W$

$R_2 = 12.5$

$2\pi kL = 0.377$

$P = 850mW \quad \Delta T = QR = 7.2\,°C$

$T = 20°C + 7.2°C = 27.2°C$

Use a peltier cooler with temperature feedback.

d) $\frac{R_2}{R_1} = \frac{R_0 \exp\left(-\frac{E_A}{kT_2}\right)}{R_0 \exp\left(-\frac{E_A}{kT_1}\right)} = 10$ Ten times faster.

Thermally activated process.

$k = 1.38 \times 10^{-23}$ $e = 1.6 \times 10^{-19}$

$E_a = 0.2\,eV$ $E_a/k = 2321$ (after conversion of eV → J)

$T_1 = 20^\circ C, 293K$

$\exp(-7.9) = 3.71 \times 10^{-4}$.

~~$\exp(-6.3)$~~

$10 \times 3.71 \times 10^{-4} = \exp\left(-\frac{2321}{T_2}\right)$

$\ln(3.71 \times 10^{-4}) = -\frac{2321}{T_2}$ $T_2 = \frac{-2321}{\ln(3.71 \times 10^{-4})}$

$T_2 = 414K \Rightarrow \underline{142^\circ C}$

(Q4)

a) Wire bonding.

Attach ultra-thin wire (Au, Cu, Al), typically 20-50μm diameter by thermocompression or ultrasonic means. (Ball or wedge shaped tool).

- Advantages

  Simple, low cost tooling, easy to inspect + test (eg: wire pull will confirm good contact)

  Generally preferred for low volume, one-off production or prototyping

- Disadvantages

  Sequential - each bond requires alignment and time to achieve bond. → Slow

  Difficult to apply to dense bond pads or to ~~low~~ large packages

  Possible mechanical, thermal, oxidation damage - built in stresses.

  Possible damage - delamination, extrusion of bond pads.

TAB - Copper (possibly gold plated) foil on polymer film. Etched to produce the required pattern to match with bond pads

All bond pads made at once - using large thermocompression tool.

Advantages - All bonds made at once - faster, cheaper
- Small bond pads can be accessed (higher density) compared to wire bonding
less variation in bond geometry
Stronger and more uniform bond than wire
Better parasitics than wire bond - high freq/ lower noise
Chip up or down configuration.

Disadvantages.

IC specific - Each die needs its own tape - low flexibility
Tooling cost - Tape + Equipment
Redundant - if significant layout changes are made.

Flip-chip

Solder 'bumps' fabricated onto the on-chip bond pads

Chip is flipped over and the solder allowed to reflo to make the interconnection

- Advantages

  Compatible with 2D bond pad geometry
  - no longer restricted to bonding at or near the periphery of the die.

  lead length very short - down to ~ microns due to small solder bump.

  Both the above are very important in reducing LCR parasitics - suitable for high freq circuits

- mechanically stable and relatively stress free

- Disadvantages

  - Additional processing steps to form solder bump

  - Die specific

  - Susceptible to metallurgical reaction between solder and bond pads - reliability

  - Alignment tools - tooling expensive.

  - Difficult to inspect and test

b)

$$M = \frac{\mu_0}{2\pi} l \left[\left(\frac{l}{d}\right) + \sqrt{1+\left(\frac{l}{d}\right)^2} - \sqrt{1+\left(\frac{d}{l}\right)^2} + \left(\frac{d}{l}\right) \right]$$

$l/d = 2.8 \quad d/l = 0.36. \qquad 2.8 + \sqrt{8.84} - \sqrt{1.129} + 0.3$

$[\ \ldots\ ] = 5.07 \ (5.02)$

$\frac{\mu_0}{2\pi} = 2.00 \times 10^{-7} \qquad l = \frac{0.005}{0.005} \cdot \frac{\mu_0 l}{2\pi} = 1 \times 10^{-9}$

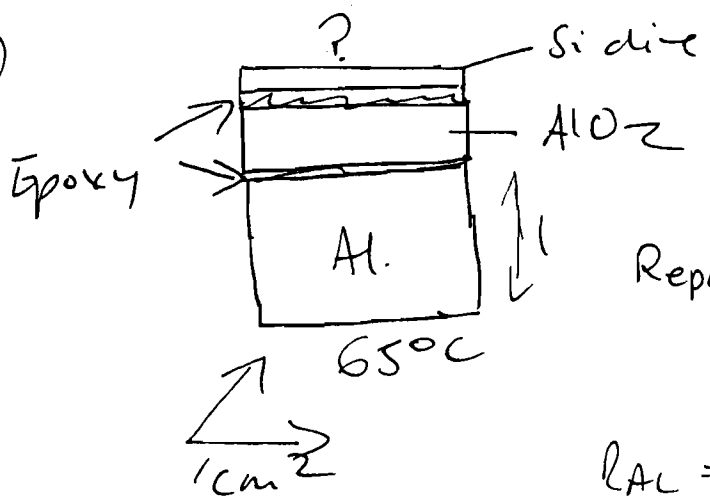
so $M = 5.07\,nH.$

$+1.2 + 3.5 = 9.77\,nH.$

$\tau = \frac{9.77}{0.55} = 17.76 \times 10^{-9} \quad 17.7\,nS.$

$f_T = \frac{1}{2\pi\tau} = 8.99\,MHz$

c)



$\Delta T = QR. \qquad R = \frac{l}{kA}$

$R_{epoxy} = \frac{100 \times 10^{-6}}{1.4 \times 1 \times 10^{-4}}$

$R_{AL} = \frac{10 \times 10^{-3}}{216 \times 1 \times 10^{-4}} = 0.71 = 0.462$

$R_{AlO_2} = \frac{1 \times 10^{-3}}{30 \times 1 \times 10^{-4}} = 0.33$

c) (cont)

from chip to Al heat sink

epoxy - Al_2O_3 - epoxy - Al

$R = 0.71 + 0.33 + 0.71 + 0.462$

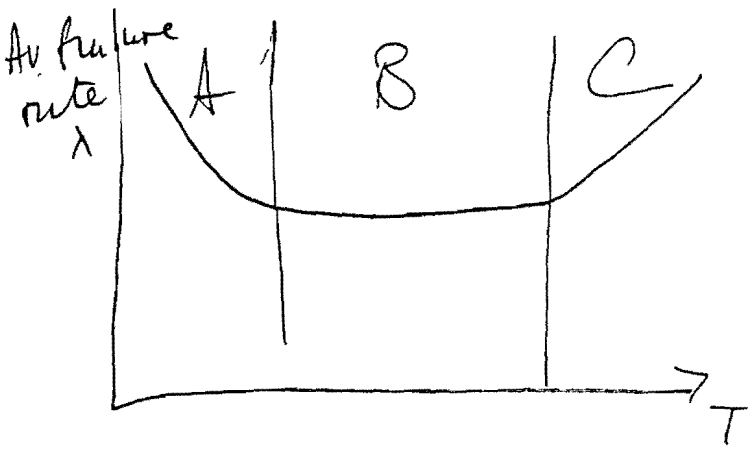
$R = 2.21\ ^\circ C/W$

$\Delta T = QR = 18 \times 2.21 = 39.8\ ^\circ C$

Chip temp $= 65\ ^\circ C + 39.8\ ^\circ C = 104.8\ ^\circ C$

OK.

4d



A - Infant mortality -- devices fail due to stresses (manufacturing defects)

B - Mid life/steady state
Low and generally constant failure rate

C - final or 'wear out' phase

4e) 4 principles

1) Power in – Needs power, probably at TTL voltages
probably minimal power dissipation
Needs high integrety of power
connection

2) Signal in – Signal in is a deflection of
a membrane due to g

Signal out – Digital logic.

3) Temperature

Minimal power dissipation –
can use plastic package for low cost.
In a reasonable temperature environment
(-20°C → 40°C). Needs some
consideration of stresses, but nothing
special

4) Environment

Membrane needs protection

Major issue – hiimicity - needs
hermetic package.
moisture will restrict membrane
movement
– needs mechanical protection
(damage, vibration)

An overmoulded pastic capped package
with hermetic seal or porous membrane should be
sufficient - Package cap should have sufficient
clearance and be robust