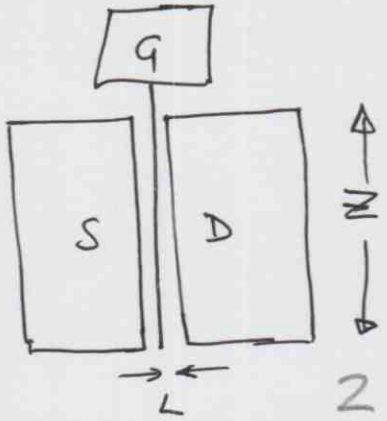
EEE 416/6040

2008

SOLUTIONS

Q1 (a) The transconductance, g_m, is the rate of change of drain current with respect to gate voltage. 2

Gate length L short to improve conductance of channel between S+D and hence increase the change in drain current for a given gate voltage change. 2



2

Gate width, Z, large to increase g_m since I_D increases in proportion to Z for a given gate voltage change. 2

(b) input (gate) current $\hat{i}_g = 2\pi f C_g V_g$ 2

output (drain) " $\hat{i}_D = g_m V_g$

$f = f_T$ when gain $= \dfrac{\hat{i}_D}{\hat{i}_g} = 1$

$$\Rightarrow f_T = \frac{g_m}{2\pi C_g}$$ 2

Physically this is a time constant $\frac{1}{g_m} \times C_g$, equivalent to the gate capacitance charging up through the resistance $\frac{1}{g_m}$. 2

Q1 (cont.)

(c) From the equation given

$$g_m = -\frac{0.25\times10^{-6}\times500\times10^{-6}\times5\times10^{22}\times0.4}{0.75\times10^{-6}}\left[1-\left(\frac{1.5}{2.14}\right)^{\frac{1}{2}}\right]$$

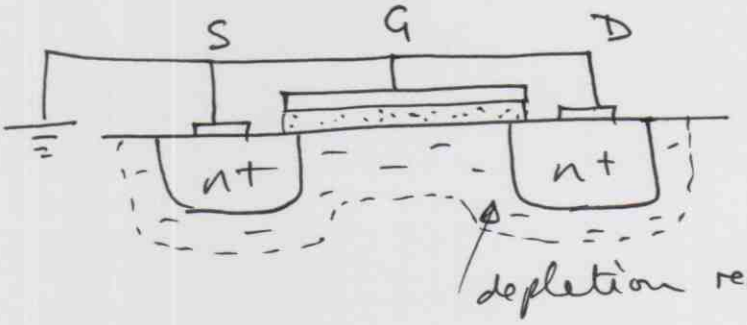
$$= 0.085\,S = -\underline{85\,mS} \qquad 3$$

$$f_T = \frac{g_m}{2\pi C_G} \;;\; C_G = \frac{\epsilon L Z}{a} = \frac{13.2\times8.85\times10^{-12}\times500\times0.75\times10^{-12}}{0.25\times10^{-6}}$$

$$= 1.75\times10^{-13}\,F$$

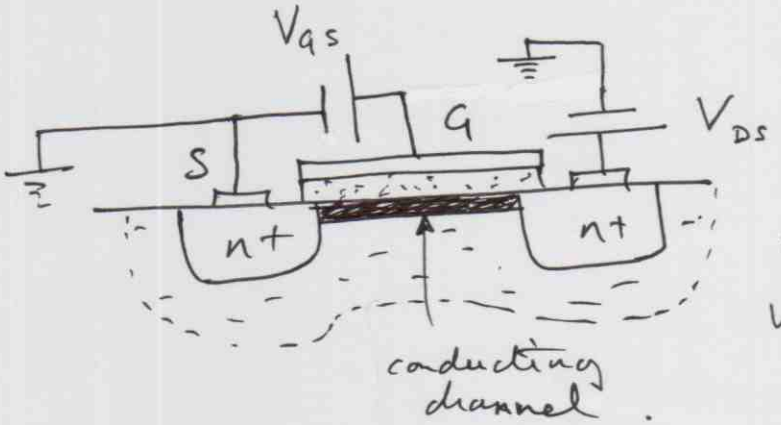
$$\Rightarrow \underline{f_T = 77.2\,GHz} \qquad 3$$

Q2. (a) (i)



3

(ii)

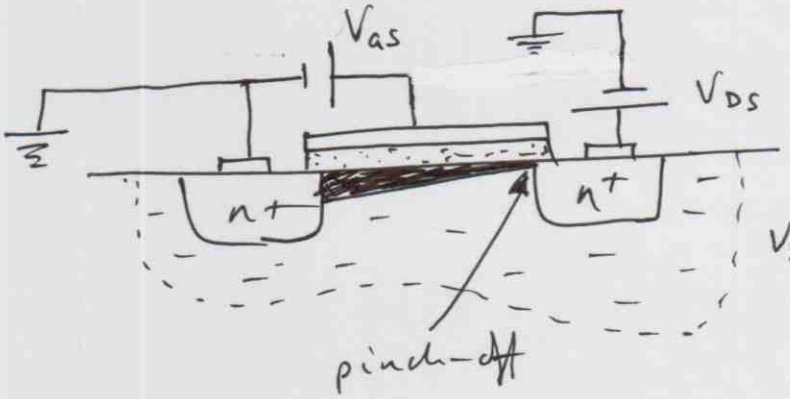


$V_{GS} > V_T$

$V_{GS} >> V_{DS}$.

3

(iii)

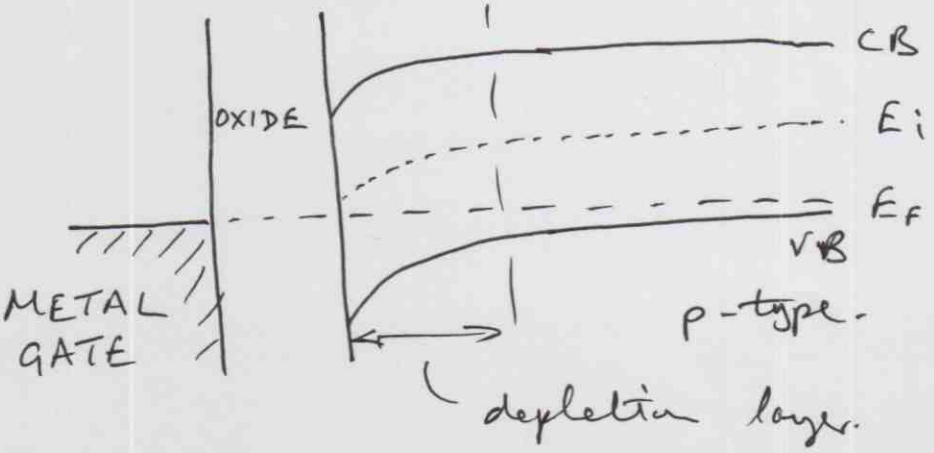


$V_{DS} = V_{GS} - V_T$

3

(b) (i)

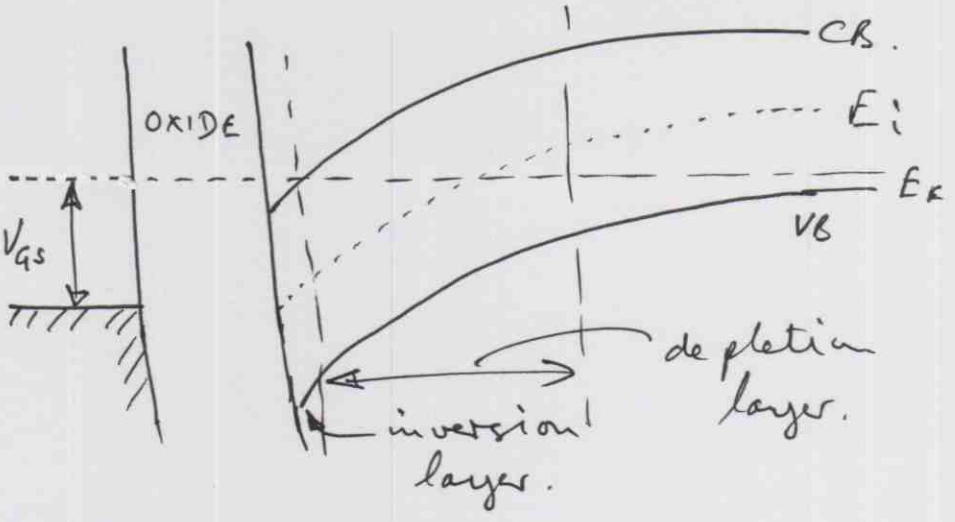
$V_{GS} = V_{DS} = 0$



3

Q2(cont.)

(ii)



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(c) $$I_D = \frac{Z\mu C_{ox}}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

$$I_D(2.5V) - I_D(1.5V) = \frac{Z\mu C_{ox}}{L}\left[2.5 - 1.5\right]0.1$$

2

$$= 60\mu A \quad (V_T \text{ is cancelled})$$

$$\Rightarrow \mu = \frac{60\times10^{-3}\times 0.2\times10^{-6}}{2\times10^{-3}\times 0.1\times 1\times 1\times10^{-6}}$$

$$= 0.06\ m^2\ V^{-1}s^{-1}$$

3

Q3 (a) $$g_m = \left.\frac{\partial I_c}{\partial V_{be}}\right|_{V_{CE}} = \frac{q}{kT} I_{E0} \exp\frac{qV_{BE}}{kT} = \frac{q I_c}{kT}$$

(transconductance) 2

r_π = input dynamic resistance of EB junction

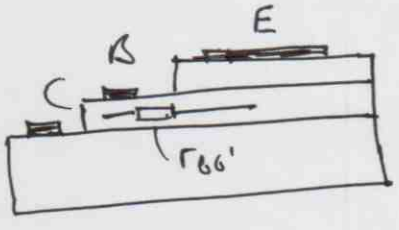
$$= \frac{\partial I_E}{\partial V_{be}} = \frac{kT}{qI_E}$$ (reduces with increased current drive). 2

$C_{b'e}$ – total depletion and diffusion charge in device 2

r_o – output conductance $\left(\frac{\partial I_c}{\partial V_{CE}}\right)^{-1}$ 1

– due to Early Effect.

$r_{b'b}$ – base access resistance 1



(b) $\hat{i}_b = \tilde{i}_{b0} + j\omega C_{b'e} \tilde{v}_{b'e}$ (from fig 3a) 1

$\hat{i}_c = g_m \tilde{v}_{b'e}$

$$\text{gain} = \frac{\hat{i}_c}{\hat{i}_b} = \frac{g_m \tilde{v}_{b'e}}{i_{b0} + j\omega C_{b'e} \tilde{v}_{b'e}} = h_{fe}$$

$$h_{fe} = \frac{\tilde{i}_c}{\tilde{i}_{b0} + j\omega C_{b'e} \tilde{v}_{b'e}}$$

$$= \frac{1}{\frac{\tilde{i}_{b0}}{\tilde{i}_c} + j\frac{\omega C_{b'e} \tilde{v}_{b'e}}{\tilde{i}_c}}$$

Q3 (cont.)

$$= \frac{1}{\frac{1}{\beta} + j\frac{\omega C_{b'e}}{g_m}}$$

at low frequency $\frac{1}{\beta} >> j\frac{\omega C_{b'e}}{g_m}$

$\therefore h_{fe} \rightarrow \beta$ (low frequency gain) 2

at high frequency $\frac{1}{\beta} << j\frac{\omega C_{b'e}}{g_m}$

$$\therefore |h_{fe}| = \frac{g_m}{\omega C_{b'e}}$$ 2

$$|h_{fe}| = \frac{g_m}{\omega C_{b'e}} = 1 \quad \text{at } \omega_T = 2\pi f_T$$

$$\Rightarrow f_T = \frac{g_m}{2\pi C_{b'e}}$$

$$= \frac{i_c}{2\pi C_{b'e} v_{b'e}} = \frac{i_c}{2\pi Q_T}$$

$$= \frac{1}{2\pi \tau_{Ec}}$$ 3

(c) $r_{bb'}$ not involved therefore has no effect on f_T.

Q 4 (a)

(i) Voltage – The supply and threshold voltage are scaled to maintain electric field (avoid breakdown problems) and reduce power density ($\propto V^2$).
Limits – $V_T \gtrsim 120mV$ to maintain low "off" currents
Logic swing $\geq 4kT$ to maintain 2 distinct logic states. 3

(ii) Oxide Thickness – to maintain capacitance and hence I_D and g_m, oxide thickness needs to be reduced, i.e. $I_D, g_m \propto \frac{1}{d_{ox}}$. ✓
Limit – tunnelling leakage currents limits thickness possible due to excess power.
can use "high k" dielectrics to maintain oxide thickness and increase capacitance. 3

(iii) Gate Length – reducing gate length increases g_m, I_D, and f_T.
Limits – need to use U-V, electron beam, X-ray to define. limits at ~10nm, when direct tunnelling occurs between source and drain. 3

(iv) Junction Depth – implanted n^+ & p^+ contact regions need to be reduced in size ~~and~~ together with an increase in doping level for for both contacts and channel. ✓
Limits – solubility of dopant, out diffusion, implant damage, minimum implant depth, reduced mobility due to 3

Q 4 (cont.)

(v) Interconnects - get narrower

Limits - increased resistance, inductance, capacitive coupling

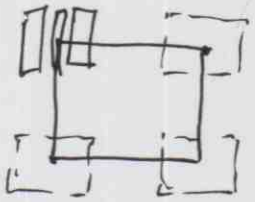
use copper and "low k" dielectric between interconnect layers. 3

(b) $C_g = \frac{\epsilon A}{d} = \frac{3.45\times10^{-11} \times 5 \times 0.09\times10^{-12}}{10^{-8}}$

$= 1.55\times10^{-15}\ F$

$P_D = \frac{1}{2} \times 0.5 \times 1.55\times10^{-15} \times 1 \times 3\times10^{9}$

$= 1.16\times10^{-6}\ W$ 2



i.e. $4 \times \frac{1}{4}$ devices within $10 \times 10\ \mu m^2$

$\therefore$ Power density $= \frac{1.16\times10^{-6}}{10 \times 10 \times 10^{-12}}$

$= 1.16\times10^{4}\ W/m^2$

$= 1.16\ W\ cm^{-2}$ 2

This power density would not cause problems as cooling in lap top applications 1