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5th lecture:

MOSFETs

- comparison: BJT vs. MOSFET
- transistor design in CMOS
- latchup problems
- current-voltage characteristic
- biasing a MOSFET
- frequency behaviour

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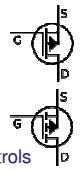
Comparison of transistor types: BJT vs. MOSFET



criterion	BJT 	JFET 	MOSFET
principle	**diffusion** through one one forward and one reverse biased diode (depletion region)	reverse-biased pn-junction isolates gate from substrate	gate bias controls source-drain current by **electrostatic** interaction across insulating gate
input current	$i_B=i_C/\beta$ (μA)	small	$i_G\approx 0$ (pA)
input impedance	low	high	very high
I/V transfer character.	exponential (exact)	modified square law	square-law (approx.)
transcoductance	high	medium	low
carrier type	minority	minority (depletion mode)	majority
radiation resistance	low	?	high
zero-offset of $I_C(V_{CE})$ or $I_{DS}(V_{DS})$	yes	?	none
gate-channel breakdown	-	partly reversible	irreversible=destructive
applications	audio amplifiers, phototransistors	high power radio transmitters, low-noise diff. amps	switches, charge measurement devices

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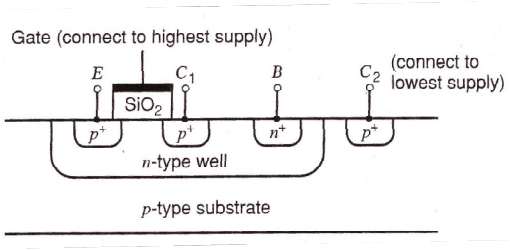
Design of BJTs in CMOS technology



- if collector C_1 is incorporated into the well, then a **lateral pnp BJT** is formed by E-B-C_1 where the additional MOSFET gate ensures reverse biasing (i.e. corresponding source drain-contacts operate in the cut-off region) ***but***
- a biased substrate forms collector of a **parasitic vertical pnp BJT** formed by E-B-C_2 for some electrons diffusing out of the n-well

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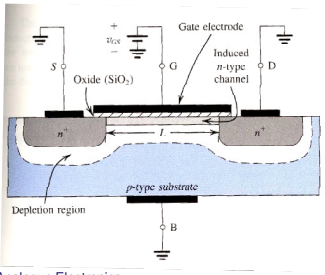
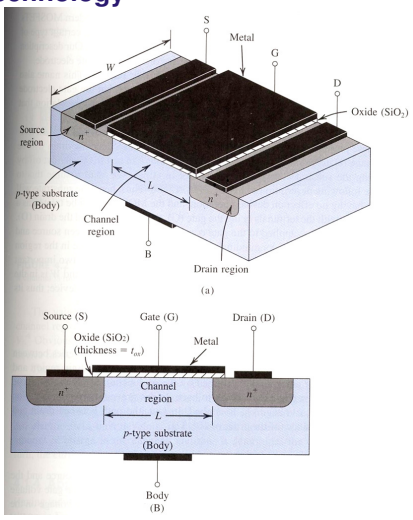
Design of MOSFETs in CMOS technology

right: enhancement-type nMOSFET
bottom right: cross-section
bottom left: n-channel
for positive gate bias





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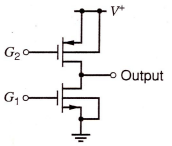
Latchup in CMOS technology

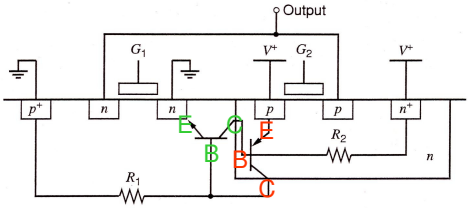
typical n-channel and p-channel MOSFET device pair involves several pn-junctions to implement (e.g. as inverter)

(a)



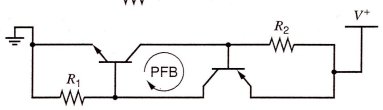
formation of two parasitic BJTs by the n-well MOSFETs, a lateral npn a vertical pnp BJT

(b)



positive feedback occurs if the BJTs enter the active region, have $\beta > 1$ and start to conduct. This can destroy the circuit.

(c)



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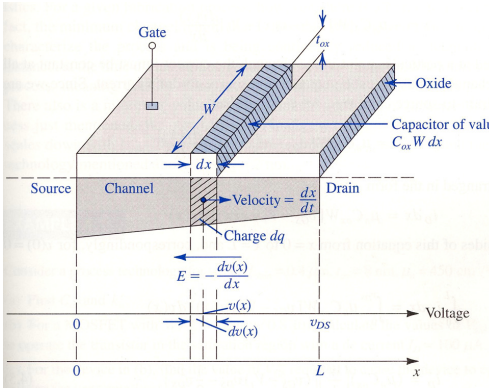
Derivation of MOSFET output characteristic



- capacitance of gate oxide per unit area: $C_{ox}=\varepsilon_{SiO_2}\varepsilon_0/t_{ox}$
- capacitance of infinitesimal strip of gate at distance x from source contact: $C_{ox}W\mathrm{d}x$
- effective voltage here: $V = V_{GS}-V_{to}-v(x)$
- charge in infinitesimal strip of n-channel: $\mathrm{d}q=-C_{ox}\,W\,\mathrm{d}x\,[V_{GS}-V_{to}-v(x)]$ (negative)
- electric field at this point: $E(x)=-\mathrm{d}v(x)/\mathrm{d}x$
  This causes the charge $\mathrm{d}q$ to drift towards the drain with a velocity given by the mobility of the electrons μ_n:
  $\mathrm{d}x/\mathrm{d}t = -\mu_n E(x) = \mu_n\,\mathrm{d}v(x)/\mathrm{d}x$
- resulting drift current:
  $i = \mathrm{d}q/\mathrm{d}t = \mathrm{d}q/\mathrm{d}x\;\mathrm{d}x/\mathrm{d}t$
  $= -\mu_n C_{ox} W [V_{GS}-V_{to}-v(x)]\; dv(x)/dx$
- drain-source current:
  $i_D = -i = \int_0^L i_D\,\mathrm{d}x$
  where $v(0)=0$ at $x=0$ and $v(L)=v_{DS}$ at $x=L$
  $i_D = \mu_n C_{ox}\,(W/L)\,[(V_{GS}-V_{to})v_{DS} - \tfrac{1}{2}v_{DS}^2]$

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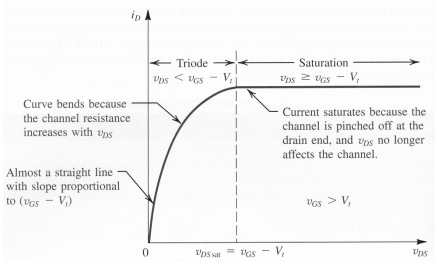
Derivation of MOSFET output characteristic



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triode region:
$i_D\approx\mu_n C_{ox}(W/L)(v_{GS}-V_{to})v_{DS}$

saturation region:
$v_{DS}=v_{GS}-V_{to}$, hence:
$i_D\approx\frac{1}{2}\mu_n C_{ox}(W/L)(v_{GS}-V_{to})^2$

overdrive voltage V_{ov}

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Derivation of MOSFET output characteristic

in the saturation region: $i_D \approx \frac{1}{2}\mu_n C_{ox}(W/L)(v_{GS}-V_{to})^2$

differentiating yields transconductance:
$g_m= \mathrm{d}i_D/\mathrm{d}V_{GS} = \mu_n C_{ox}\ W/L\ (V_{GS}-V_{to}) = 2i_D/V_{ov}$

is much lower than for BJTs,
as i_D is usually up to a few A, while $V_{ov}=v_{GS}-V_{to}$= 0.2 - 0.5V.
Hence, use the ratio i_D/V_{ov} as operational design parameter.

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Biasing of a MOSFET

- bad idea: fixing V_{GS}

  i_D depends on a number of parameters that vary from device to device (V_{to}, C_{ox}, sometimes also W/L) and strongly depend on the temperature (V_{to} and μ_n)

- good idea: fixing V_G and connecting a resistance parallel to source

  Connecting a resistor R_S to the source yields $V_G=V_{GS}+R_S i_D$, i.e. a negative feedback that stabilises i_D, analogous to emitter degeneracy in BJTs

- less good: using a drain-to-gate resistor R_G. This yields $V_{GS}=V_{DS}=V_{DD}-R_D i_D$, i.e. also negative feedback that stabilises i_D, but the output voltage swing would be limited

- best: use current mirrors to provide constant current source, e.g. for a 2-MOSFET current mirror: $i_{D2}/i_{REF}=i_{D2}/i_{D1}=(W_2/L_2)/(W_1/L_1)$

aspect ratio as layout design parameter

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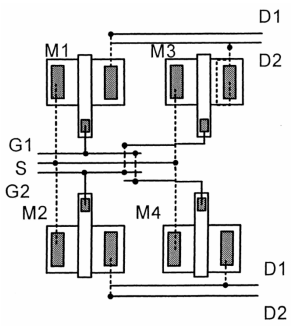
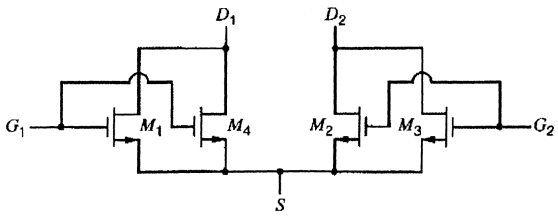
Example of a typical MOSFET circuit: centroid layout

- The circuit is a differential amplifier, as the source electrodes are connected to a common current source and the diff. signals are fed into opposite base electrodes.
- Problem: diff. amplifiers are very sensitive to any mismatch between the two signal paths, which would increase the common-mode and decrease the diff. mode signal.



- Solution: replace single transistors by pairs of transistors at opposite positions on the substrate to eliminate linear process gradients, such as variations of t_{ox}, that can be decomposed into x- and y- components.
- Disadvantage: longer lines for cross-connection



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Body effect in MOSFETs

- problem: substrate acts as 4th terminal (called body) which results in another pn-junction between the induced channel and the substrate
- substrate is usually common to many MOSFETs within a device and connected to most negative [positive] supply voltage in NMOS [PMOS], hence resulting reverse bias V_{SB} between source and body (in NMOS) will affect device operation by widening the depletion region and reducing the channel depth, so that V_{GS} has to be increased to maintain constant operation conditions and keep i_D constant.

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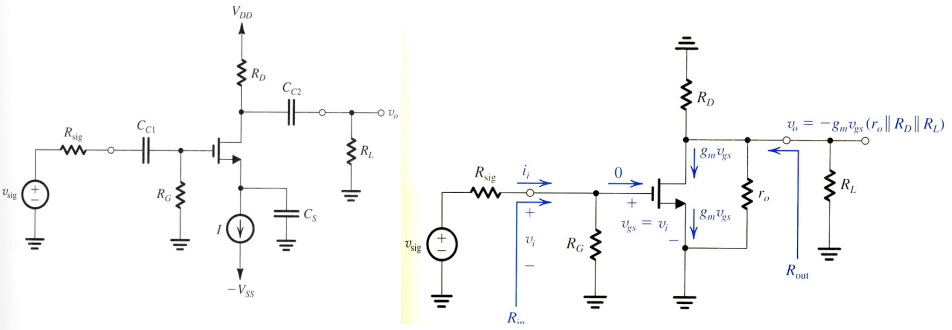
Mid frequency behaviour of MOSFET common source (CS) amp.



general CS amplifier circuit (left) and small signal equiv. circuit (right)
at input: i_G=0, R_{in}=R_G, v_i=v_{sig} $R_G/(R_G+R_{sig})\approx v_{sig}$ (for large R_G)
at output: v_o=$-g_m v_{GS}$ $(r_o||R_D||R_L)$
hence voltage gain of signal to load: $G_{mid} = v_o/v_{sig} = -R_G/(R_G+R_{sig})\ g_m(r_o||R_D||R_L)$

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High frequency behaviour of MOSFET common source (CS) amp.

now take capacitors into account to obtain voltage gain of signal to load:

$$G_{high} = V_o/V_{sig} = -R_G/(R_G+R_{sig})\; g_m(r_o||R_D||R_L)\; 1/(1+j\omega/\omega_H)$$

G_{mid} × frequency dependence

where

$\omega_H = 1/\{(R_G \,||\, R_{sig})(C_{GS}+C_{GD}[1+ g_m(r_o||R_D||R_L)]\}$

is the high frequency 3dB-bandlimit

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Gate capacitance and high frequency behaviour of MOSFETs

Gate capacitance can be modelled by three capacitances C_{GS}, C_{GD} and C_{GB}

- MOSFET is **cut off**: channel disappears, thus

  $C_{GS}=C_{GD}= 0$, but $C_{GB}\approx WLC_{ox}$
- MOSFET operates in **triode region** with small v_{DS}: channel will be uniform in depth and total gate capacitance WLC_{ox} is distributed equally between source and drain ends:

  $C_{GS}=C_{GD}= \frac{1}{2}WLC_{ox}$
- MOSFET operates in **saturation** where the channel has a tapered shape and is pinched off near the drain, so

  $C_{GD}=0$, $C_{GS} \approx 2/3\,WLC_{ox}$

Note: An additional small capacitance component should be added to C_{GS} and C_{GD} in all above equations due to **spatial overlap of regions where source and drain diffusion extend slightly under the oxide gate**, typically <10%

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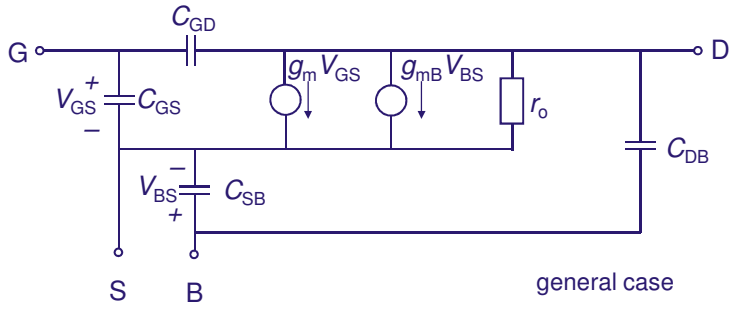
Gate capacitance and high frequency behaviour of MOSFETs

Hybrid-π model for small high-frequency signals of MOSFET



general case

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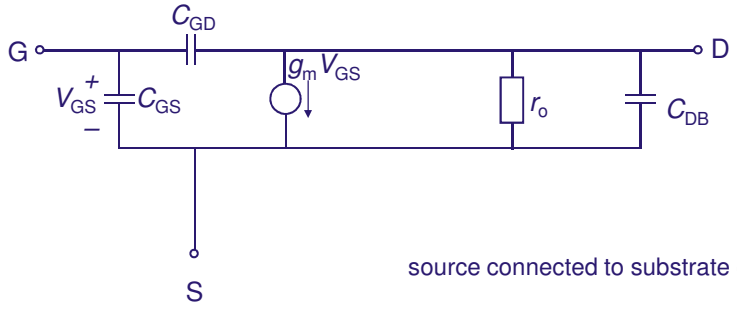
Gate capacitance and high frequency behaviour of MOSFETs

Hybrid-π model for small high-frequency signals of MOSFET



source connected to substrate (V_{BS}=0)

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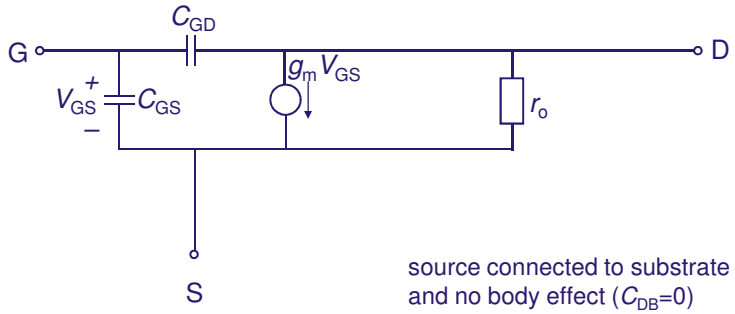
Gate capacitance and high frequency behaviour of MOSFETs

Hybrid-π model for small high-frequency signals of MOSFET



source connected to substrate (V_{BS}=0)
and no body effect (C_{DB}=0)

inject test current at gate: $i_i = j\omega(C_{GS}+C_{GD})V_{GS}$
output current at drain: $i_o = g_m V_{GS} - j\omega C_{GD} V_{GS} \approx g_m V_{GS}$
short-circuit current gain: $i_o/i_i \approx g_m/[j\omega(C_{GS}+C_{GD})]$
unity gain at frequency $f_T = g_m/[2\pi(C_{GS}+C_{GD})] = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$

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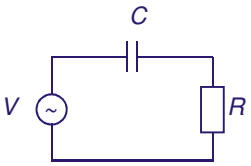
Bode plots, part 1: double logarithmic frequency plots

voltage gain: $G = V_o/V_i$
definition: gain [dB] = $20 \log_{10} G$



example: **simple RC-network (filter)**
consider sinusoidally driven RC circuit and its phasor diagram:
$V_R = IR$
$V_C = I/(j\omega C) = -j\, I/(\omega C)$
-> circuit impedance: $Z = R + 1/(j\omega C)$
-> transfer function: $T = V_o/V_i = V_R/(V_R+V_C) = R/[R+1/(j\omega C)]$
$= 1/[1 - j(\omega_c/\omega)]$
with cut-off frequency $\omega_c = 1/(RC)$
-> amplitude: $|T| = 1/\sqrt{1+(\omega_c/\omega)^2}$
phase angle: $\angle T = \tan^{-1}(\omega_c/\omega)$

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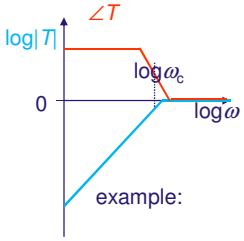
Bode plots, part 1: double logarithmic frequency plots



1. $\omega << \omega_c$: $T = j\omega/\omega_c$,
   $|T|_{dB} = 20(\log\omega) - 20\log\omega_c$ is a linear function of $\log\omega$
   with slope of +20dB/decade (6dB/octave), $\angle T = 90°$
1. $\omega = \omega_c$: $T = 1/(1-j)$, $|T| = 1/\sqrt{2} \approx -3$dB, $\angle T = 45°$
2. $\omega >> \omega_c$: $T = 1$, $|T| = 1 = 0$dB, $\angle T = 0°$

example:

simple RC-network (low-pass filter: $|T| \leq 1$)
consider sinusoidally driven RC circuit and its phasor diagram:
$V_R = IR$
$V_C = I/(j\omega C) = -j\, I/(\omega C)$
-> circuit impedance: $Z = R + 1/(j\omega C)$
-> transfer function: $T = V_o/V_i = V_R/(V_R + V_C) = R/[R + 1/(j\omega C)]$
$= 1/[1 - j\,(\omega_c/\omega)]$
with cut-off frequency $\omega_c = 1/(RC)$
-> amplitude: $|T| = 1/\sqrt{1 + (\omega_c/\omega)^2}$
phase angle: $\angle T = \tan^{-1}(\omega_c/\omega)$

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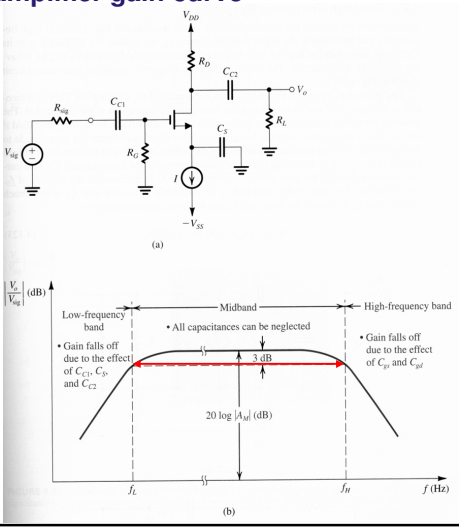
Bode plots, part 2: typical amplifier gain curve

capacitatively coupled common-source amplifier



Bode plot of the three main frequency bands that dominate the frequency response

3dB bandwidth (BW) = $f_H - f_L \approx f_H$ can be traded off against gain, as their product is approx. constant.