Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2008-2009 (2 hours)

Integrated Circuit Technology 6

Answer **THREE** questions. **No marks will be awarded for a solution to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

1. a. Consider the isolated Ga and As atoms and give their outer electronic configurations. What hybrid orbitals are formed when these atoms bond together in the diamond cubic lattice and, with the aid of a graph, briefly describe the energetics of bond formation as the Ga and As atoms come together. **(4)**

b Crystalline diamond is cubic and has a lattice parameter of $a_0 = 0.3567$nm. Determine the spacings of the following planes: (110), (211), (310) and (422). **(4)**

c Calculate the angles between the following pairs of planes in the diamond cubic lattice: (100) and (110)

(111) and (311) **(3)**

d Deduce which of the following pairs of planes in a cubic crystal are perpendicular to one another:

$(0\bar{1}1)$ and $(31\bar{1})$

$(\bar{1}00)$ and $(0\bar{1}4)$

$(\bar{1}10)$ and (224) **(3)**

e Give the close-packed plane stacking sequences for intrinsic and extrinsic stacking faults and also for a twin in the diamond cubic lattice. **(3)**

f Why do {111} type surfaces exhibit 'polarity' for crystals with the Zinc Blende structure? Why do {111} surfaces on Si crystals not exhibit polarity? **(3)**

2. a. Describe the way in which photolithography is used to define patterns in oxide layers. Include all the detailed steps in the process, from choice of the optical radiation to the nature of the resists themselves. **(10)**

b With the aid of a diagram, describe how metal tracks can be defined using the lift-off process. **(5)**

c Outline the ways in which lithographic techniques, which use radiation other than light, are used in processing at the present time: indicate also how they may be used in the future. **(5)**

3. **a.** Describe the apparatus and processes required for the chemical vapour deposition of epitaxial Si. Indicate the way in which the deposited material is doped and comment on factors that affect layer quality: include diagrams of the apparatus and of the range of deposition chamber designs. **(10)**

b A Si substrate wafer has a Si epitaxial layer grown upon it at a temperature of 1150°C. If the layer growth rate is 0.1μm/min and the substrate is heavily doped with boron, deduce by calculation whether autodoping of the layer would be expected to be a problem. You may assume that the activation energy for boron diffusion (E_A) is 3.46eV, the boron diffusion pre-exponential factor (D_0) is $0.76cm^2/s$ and Boltzmann's constant (k) is $8.62x10^{-5}eV/K$. **(6)**

c The Si wafers used for a particular device processing sequence have been subjected by the suppliers to internal gettering of unwanted transition element impurities. Describe the way in which the process of internal gettering is carried out with reference to a diagram of the wafer cross-section. **(4)**

4. **a** Describe the three main areas where metallization is employed in Si integrated circuit processing. Where appropriate, provide examples of important problems that may occur and explain the ways in which these can be overcome. **(9)**

b For what are silicides used during Si processing? Which are the most important silicides and why are they employed? With the aid of diagrams, describe the 'Salicide Process' for silicide formation. **(5)**

c Describe, with the aid of diagrams, two important techniques used during packaging of ICs for bonding contact pads on the IC die to those on the package itself. One of the techniques should be suitable for high frequency devices. **(6)**