The University Of Sheffield.

Electronic & Electrical Engineering.

EEE6214 PACKAGING AND RELIABILITY OF MICROSYSTEMS

Credits 15

Course Description including Aims

The unit describes the methods used to fabricate microsystems from electronic, opto-electronic and micro-electromechanical (MEMS) devices. It also introduces and develops an understanding of the reliability and failure mechanisms in the devices and resulting microsystems.

The aims are as follows:

Develop an understanding of the key aspects of microsystem packaging at three levels: individual component; circuit board and complete system. Emphasis will be on practical industrial solutions to modern microsystem packaging challenges.

Model the thermal behavior of microsystems.

Understand the thermal, mechanical, electrical and chemical degradation mechanisms that affect the reliability of microsystems.

Use statistical techniques to model reliability.

Appreciate microsystem test and characterization techniques.

Outline Syllabus

Résumé of electronic device evolution. General packaging principles. Component packaging (including integrated circuits, opto, MEMS, RF and power devices). Substrates (including printed circuit boards). Interconnection (including solder technologies). System-level packaging. Electrical and thermal considerations (including finite element thermal modelling). Test strategies. Reliability modelling. Degradation and failure mechanisms: thermal, chemical, electrical and mechanical. Failure characterization techniques.

Time Allocation

36 hours lectures
25 hours reverse engineering exercise, incorporating finite element thermal modelling
15 hours statistical exercise
74 hours independent study

Recommended Background Knowledge

A first degree in Engineering, Physics or knowledge equivalent to 3rd year EEE undergraduate degree programmes. Knowledge of basic semiconductor theory, elementary thermal physics and elementary optics would be an advantage.

Assessment

Formal examination (2 hours duration; answer any 3 questions from 4)	75 %
Reverse-engineering exercise (written report using data from FE thermal analysis)	15%
Statistical analysis of commercial reliability data (computer-based test)	10 %

Recommended Books

Tummala R	*Fundamentals of Microsystem Packaging*	McGraw Hill, 2001 and eBook via TuOS Library
Ohring M	*Reliability and Failure of Electronic Materials and Devices*	Academic Press, 1998 and eBook via TUoS Library

Other books

Wu B	*3D IC Stacking Technology*	McGraw Hill 2011
Sergent JE	*Hybrid Microelectronics Handbook*	McGraw Hill, 1995
Martin PL	*Electronic Failure Analysis Handbook*	McGraw Hill, 1999
Pascoe N	*Reliability Technology*	Wiley, 2011
Hannermann RJ	*Physical Architecture of VLSI Systems*	Wiley, 1994
Lau JH	*Flip Chip Technologies*	McGraw Hill, 1995
Amerasekera E	*Failure Mechanisms in Semiconductor Devices*	Wiley, 1998
Pecht M	*Guidebook to Managing Silicon Chip Reliability*	CRC, 1999
Lall P	*Influence of temperature on Microelectronics and System Reliability*	CRC, 1997

Objectives

On completion of the module, successful students will be able to:

- Describe the range of technologies available for microsystem manufacture and design and select appropriate methods for given industrial scenarios.
- Assess the needs of a particular design – being able to choose and justify packaging options (both technologically and economically).
- Model the thermal, electrical, optical signal behavior of various component / interconnect / substrate combinations.
- Identify and explain the various types of defect in microelectronic devices.
- Identify and explain the degradation and failure mechanisms in electronic and optoelectronic devices and systems.
- Apply appropriate statistical models to analyze reliability data.
- Interpret the results from the common characterization techniques used in reliability and failure analysis of electronic and optoelectronic devices.

Detailed Syllabus

- Outline of course contents and objectives. Basic principles of device packaging and overview of practical examples. Introduction to integrated circuits, including historical development with emphasis on monolithic integration. Overview of reliability modelling and failure mechanisms.
- Principles of IC packaging. Electrical interconnection methods: Wire bond, TAB, Flip chip. Power and signal requirements. Resistance, capacitance and inductance of bond wires. Parasitics: noise and cross-talk.
- Package material and metallization issues. Description of common types and historical trends in packaging. Interpreting manufacturer’s data sheets.
- Modern packing approaches. The packaging bottleneck. Multichip modules, system on

chip. Future trends. Special considerations in the packaging of RF devices.

- Principles of optoelectronic packaging. Resume on optoelectronic devices. Types of optoelectronic packaging: LED, photodiode. Choice of packaging materials and practical implementation (with examples).
- Fibre optic device packaging of telecommunications lasers. Heat dissipation and temperature control. Laser to fibre alignment. Fibre pigtailed packages. Use and advantages of VCSELs. Telecoms MCM modules.
- Packaging of MEMS modules. Special considerations and manufacturing issues. Types of package: cap-on-chip, machined silicon/ceramic sandwich, indent reflow sealing. Use of local bonding and flip chip. Self assembly methods. Practical MEMS examples: Ink jet printer head, accelerometer and pressure sensor.
- Power device packaging, focusing on mitigation of thermal effects.
- Device reliability. Bathtub curve. Mean time to failure and average failure rate. Typical device reliability curves.
- Physics of failure of semiconductor materials: defects and contaminants.
- Electrically induced failures: electrostatic, electrical stress, hot carriers, dielectric breakdown, electrochemical corrosion, atmospheric corrosion.
- Thermally induced failures: interdiffusion, Arrhenius equation, compressive/tensile stresses.
- Degradation in electro-optical devices.
- Testing methodology. Use of accelerated stresses, such as temperature, humidity etc. Experimental set ups and standard test methods. Use of burn in.
- Failure characterization techniques, including optical and electron microscopy, focused ion beam, X-ray and thermography.
- Printed circuit board fabrication. Bare board fabrication. Lithography. Plating and etching. Through, blind, buried and micro vias. Embedded passives. Solder mask. Flexible PCBs. Opto-electronic circuit boards.
- Printed circuit board design. Design flow: partitioning, IC and connector choice, simulation, schematics, layout, design rule verification, prototype fabrication.
- Printed circuit board assembly. Solder. Flux. Solder paste. Screen printing. Wave soldering. Reflow soldering. Hand soldering. Laser soldering. Phase diagrams. Implications of removal of lead from solder. Underfill. Tin whiskers. Conductive adhesive (isotropic and anisotropic).
- Heat transfer. Fundamental principles of conductive, convective and radiative heat transfer. Thermal resistance networks. CAD systems (finite element and fluid dynamics).
- Electronics cooling. Heat sinks. Fans. Heat pipes. Peltier coolers. Thermal interface materials. Thermal vias.
- Practical exercise on finite element modelling of thermal and mechanical effects.
- Manufacturing process modelling, including yield. Issues affecting yield and mathematical models.
- Electronic system design
- Economic, environmental and legal issues. Reuse, recycling and end-of-use disposal of electrical systems.

UK-SPEC/IET Learning Outcomes

SM1m / SM1fl	Knowledge and understanding of the underlying scientific principles and methodology relating to device & systems packaging technologies, such as electrical interconnection issues, thermal constraints. Understanding of chemical, mechanical and electrical issues contributing to premature device failure. Assessment: exam.
SM2fl	An awareness of recent and future developments in packaging methods and technologies (eg System-on-Chip, System-In-Package, heterogeneous integration, wafer-level packaging, vertical integration). Assessment exam.
SM4m	An awareness of recent and future developments in packaging methods and technologies (eg: System-on-Chip, System-In-Package, heterogeneous integration, wafer-level packaging, vertical integration). Assessment: exam.
SM5m	Full treatment of statistical methods for reliability assessment and manufacturing process yield. Assessment: computer-based test.
EA1p	Understanding of the engineering principles related to the packaging of components and the assembly of electronic systems. Using these principles to analyze current methods or to suggest appropriate packaging schemes devices based on particular characteristics. Assessment: exam.
EA2p	Thermal and electrical models will be used to determine the performance of electronic microsystems. The use of test and characterization equipment will be introduced. Assessment: exam and written report.
EA2m	the course includes a detailed thermal analysis of a microsystem, using both ‘back of fag packet’ calculations and finite element analysis. Assessment: exam and written report.
EA6m	Use knowledge of packaging issues to reverse-engineer a commercial electronic system using computer-based methods. Assessment: written report.
D2p	Understand the constraints imposed by environmental and sustainability limitations, health and safety and risk assessment issues. This will include discussion of RoSHH, including move to Pb-free solder. The student will be introduced to life-cycle management of electrical systems. Assessment: exam.
D3p	many assumptions need to be made when performing thermal analysis. Assessment: written report.
D5m	Understand and manage cost versus performance issues in packaging. Assessment: exam.
D7m	Knowledge and experience of using PCB design tool. Assessment: exam.
D2fl	Knowledge and experience of using PCB design tool. Assessment exam.
ET2m / ET2fl	Knowledge and understanding of the commercial and economic context of device and systems packaging in the production of electronic devices Assessment: exam.
ET3p	Awareness of the relevant legal requirements involved in packaging activities, in particular of the health, safety, and environmental impacts. Yield modelling. Assessment: exam.

EP2m / EP2fl	Extensive knowledge and understanding of a wide range of engineering materials and components used in current packaging methods, in particular the mechanical and thermal properties of packaging materials. Extensive knowledge of the practical issues relating to device failure. Assessment: exam and computer-based test.
EP3m	Some workshop/lab skills developed when reverse-engineering a microsystem. Assessment: written report.
EP6m	Commercial data sheets will be used. Assessment: written report.
EP8m	Being able to cope with statistical uncertainty is the basis of the failure rate methods. Assessment: computer-based test.
EP9m	A thorough understanding of current practice in microsystems packaging and its limitations, together with an appreciation of future trends and possible new developments. Assessment: exam.
EP1fl	Extensive knowledge and understanding of a wide range of engineering materials and components used in current packaging methods, in particular the mechanical and thermal properties of packaging materials. Extensive knowledge of the practical issues relating to device failure. Assessment exam and computer-based test.