The University Of Sheffield.

Data Provided:

Thermal conductivity of silica-loaded epoxy:	$k_{epoxy} = 1.40$ W m^{-1} K^{-1}
Thermal conductivity of thermal grease:	$k_{grease} = 0.80$ W m^{-1} K^{-1}
Stefan-Boltzmann constant:	$\sigma = 5.67\times10^{-8}$ W m^{-2} K^{-4}
Electronic charge:	$e = -1.60\times10^{-19}$ C
Boltzmann constant:	$k_B = 1.38\times10^{-23}$ m^2 kg s^{-2} K^{-1}
Permeability of free space:	$\mu_o = 1.26\times10^{-6}$ m kg s^{-2} A^{-2}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2010-2011 (2 hours)

EEE6393 Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Consider the chip package shown in Figure 1. The silicon die has dimensions of 10×10×0.5 mm and dissipates a maximum power of 4 W. The encapsulating material is silica-loaded epoxy resin. The thickness of the package (not including the leads) is 2.5 mm. Calculate the thermal resistance of the heat sink that is required to maintain the die temperature below 100 °C when in operation. State any assumptions that you have made.

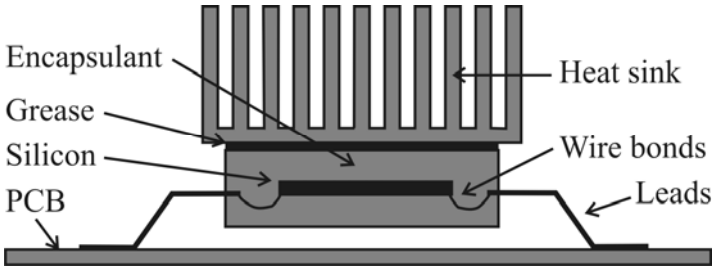

Figure 1 Schematic cross-section of chip package with heat sink **(6)**

b. Why is the epoxy encapsulant in Part 1.a. loaded with silica? **(3)**

c. Explain why epoxy resin is *not* used to attach the heat sink to the package in Part 1.a. **(3)**

d. Explain in detail the assembly method by which the surface mount package in Figure 1 is attached to the PCB. Include a discussion of how components could be added to the underside of the PCB. **(8)**

2. a. Describe the method by which through silicon vias (TSVs) are formed, with emphasis on new manufacturing techniques that have been developed.

Why are TSVs being developed? **(8)**

b. A complex electronic system includes a microprocessor that operates at 2.5 V and an ASIC that operate at 3.3 V. The maximum PCB dimensions are limited to 10×5 cm, hence it is decided to implement the system on two PCBs. Discuss the procedure by which the PCBs are designed. **(6)**

c. The two PCBs of Part 2.b. are enclosed in a cabinet that is ventilated with a fan. In operation, the total power dissipated is 20 W and the average temperature of the PCBs is found to be 70°C. Assuming that ten percent of the power is dissipated by radiation, what is the temperature of the cabinet wall? State any assumptions that you make. **(6)**

3. a. Describe what is meant by the term 'System on a Chip' (SoC). **(1)**

What are the advantages and disadvantages of this approach, compared to using multiple integrated circuits (ICs)? **(4)**

Describe the typical elements within a digital SoC found within a smartphone. **(1)**

Why in some case might a 'System in Package' (SiP) be preferred to the SoC approach? **(2)**

b. A 64 pin DIP package is being considered for high frequency digital applications. Two low voltage signals are initially considered to be applied to two adjacent pins. Using the parameters in Table 1 and the equations supplied below, calculate:

(i) the self inductance of the lead frame, **(1)**

(ii) the mutual inductance between two pins of the lead frame, and **(2)**

(iii) the self inductance of the wire bond. **(1)**

Comment on the relative parasitic inductances. What can be done to reduce each of these? **(2)**

Finally, describe a different packaging method which results in substantially reduced parasitics. **(2)**

Mutual inductance $M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\left(\sqrt{1+\left(\frac{d}{l}\right)^2}\right)+\left(\frac{d}{l}\right)\right]$

Self inductance (lead frame) $L_{LF} = \frac{\mu_0 l}{2\pi}\left(\ln\left[\frac{2l}{w+t}\right]+0.50+\left(\frac{w+t}{3l}\right)\right)$

Self inductance (wire bond) $L_{WB} = \frac{\mu_0 l}{2\pi\left(\ln\left[\frac{2l}{r}\right]-0.75\right)}$

Table 1 Parameters for a DIP64 package

Parameter	Dimension
Lead frame length (l)	5 mm
Lead frame width (w)	0.2 mm
Lead frame thickness (t)	0.1 mm
Separation of adjacent pins (d)	1.2 mm
Bond wire length (l)	2.5 mm
Bond wire radius (r)	25 μm

c. Microwave ICs of size 5×5 mm are fabricated onto 150 mm diameter GaAs wafers. Before fabrication, the wafers are inspected and found to have typically 120 point defects per wafer. Assuming only one point defect can cause the IC to fail, what is the estimated yield of the ICs?

On closer investigation, 40% of the ICs are observed to be tolerant of one defect, but none are tolerant of more than one defect. What is the value of the improved yield? **(4)**

4. a. Describe the three main methods of integrated circuit (IC) to package interconnects. State which method would be most suitable for the following devices, justifying your reasons: **(3)**

(i) high speed digital processor IC **(1)**

(ii) operational amplifier ICs **(1)**

(iii) laboratory prototype MEMS device. **(1)**

b. The first Intel processor was called the 4004. This dissipated 0.63 W, used a 40 pin plastic DIL package and did not require a heatsink. Some important parameters of this IC are compared in Table 2 *(overleaf)* with one of the latest processors: the Intel Core i7.

Assuming all the power (P) dissipated is due to dynamic switching in the transistors; estimate the power dissipation of the Core i7 through a comparison with the 4004. **(2)**

Dynamic switching power $P = \alpha C V^2 f$

where α is the switching probability, C the gate capacitance, V the supply voltage and f the clock frequency. You may assume the same value of α for both ICs and that all dimensions scale with the technology 'node'.

For both ICs, apply Rents rule to calculate the number of output terminals based on the number of gates. **(2)**

You may use a rent exponent of 0.45 and a rent coefficient of 0.8 for both devices

Using the information gained above, suggest a suitable: (i) packaging material, (ii) package type, (iii) interconnect method and (iv) thermal control scheme for the Core i7 processor. Justify your answers.

(4)

Table 2 Comparison of two different types of Intel processor ICs

Processor	Year of introduction	CMOS gates	Technology node	Clock speed	Supply voltage
4004	1971	575	10 μm	740 kHz	5.0 V
Core i7	2008	23×10^6	32 nm	3.4 GHz	0.9 V

c. Many packaged devices, including lasers, are subjected to 'accelerated testing'. What does this term mean? Why is it useful if we only have limited time for the lifetime testing of new components? **(2)**

Describe conditions for the HAST test. What elements of the package is this particularly designed to test? Why is this test often performed in the early stages of packaged device development? **(2)**

Under testing at 120°C, the mean time to failure of such a laser is observed to be 50 hours. The failure mechanism is known to be thermally activated, with an activation energy of 0.75eV. What is the mean time to failure at 20°C? **(2)**

GLW / MH