Data Provided:

n-FET *I*/*V* characteristic

$$I_{DSN} = \frac{m_E \cdot C_{OX} \cdot W}{2L} \cdot (V_{GSN} - V_{TN})^2 \qquad (V_{TN} \le V_{GSN},\ V_{DSN} \ge V_{GSN} - V_{TN})$$

$$= \frac{m_E \cdot C_{OX} \cdot W}{L} \cdot \left(V_{GSN} - V_{TN} - \frac{V_{DSN}}{2} \right) \cdot V_{DSN} \qquad (V_{TN} \le V_{GSN},\ V_{DSN} < V_{GSN} - V_{TN})$$

$$= 0 \qquad (0 \le V_{GSN} < V_{TN})$$

p-FET *I*/*V* characteristic

$$I_{DSP} = -\frac{m_H \cdot C_{OX} \cdot W}{2L} \cdot (V_{GSP} - V_{TP})^2 \qquad (V_{TP} \ge V_{GSP},\ V_{DSP} \le V_{GSP} - V_{TP})$$

$$= -\frac{m_H \cdot C_{OX} \cdot W}{L} \cdot \left(V_{GSP} - V_{TP} - \frac{V_{DSP}}{2} \right) \cdot V_{DSP} \qquad (V_{TP} \ge V_{GSP},\ V_{DSP} > V_{GSP} - V_{TP})$$

$$= 0 \qquad (0 \ge V_{GSP} > V_{TP})$$

The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2003-2004 (2 hours)

Introduction to VLSI Design

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Explain why manufacturing test is so important for ICs and what is meant by *design for test* **(3)**

b. Identify the different types of fault that might be encountered in a manufactured IC and identify the type of fault that is predominantly assumed to occur in testing ICs. **(3)**

c. Describe the organisation and operation of the following:

i) scan testing **(4)**

ii) Built-in Self-Test **(4)**

d. The logic shown in **Figure 1** is to be tested for a fault at node X. Describe how this would be done. Ensure that you identify *sensitisation* and *propagation* in your explanation and any changes to the logic that you might need to make to allow node X to be tested. **(6)**

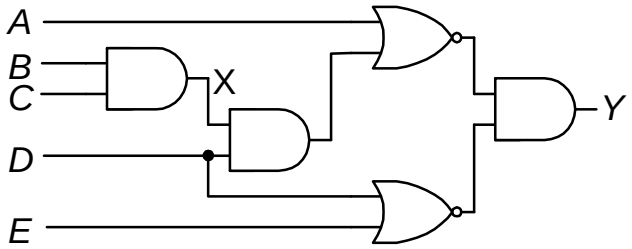

Figure 1

2. **a.** Describe the attributes of CMOS logic that make it the dominant logic style used in digital ICs. **(4)**

b. For the function, $Y = \overline{A.\overline{(B+C)}+\overline{A}}$:

i) Draw a CMOS circuit that minimises the number of transistors used; **(6)**

ii) Size the transistors to form a minimum-sized gate (you may assume that the mobility of holes is 0.5 that of electrons); **(2)**

iii) Estimate, simply, the delay of the circuit relative to a minimum-sized inverter. **(4)**

c. The circuit in part **b.** is to be used to drive a load whose capacitance is equivalent to 44 times the capacitance of a minimum-sized n-type transistor. How would you alter the circuit to drive this load effectively? **(4)**

3. **a.** The drain (V_d) of the n-type pass transistor in **Figure 3** is driven from a perfect voltage source. Estimate, the small-signal, *quiescent*, on-state resistance of the FET (as V_s varies) for:

i) $V_d = V_{dd}$ **(3)**

ii) $V_d = 0$ **(3)**

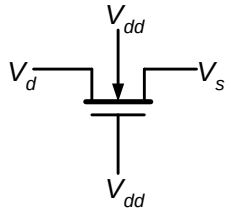

Figure 3

b. The point labelled V_s in **Figure 3** is loaded with a capacitance of C_L that, initially, has 0V on it. At t=0, the voltage V_d is raised from 0V to V_{dd}. Determine the voltage, V_s, as a function of t. **(8)**

c. You are told that, especially for small values of t, the equation:

$$\frac{XY^2t}{1+XYt} \approx Y\left(1-e^{-XYt/1.5}\right)$$

is satisfied. From this fact, and the answer in part **b.**, estimate, approximately, the effective resistance of the FET in this situation. **(6)**

4. **a.** Show that the dynamic power consumption of a CMOS IC, due to switched capacitance, can be modelled by:

$$P_{sw} = a \cdot f_{clk} \cdot V_{DD}^2 \sum_{i=1}^{n} C_i$$

where the terms have their usual meaning. **(4)**

What gives rise to C_i? **(2)**

b. How does the leakage power consumption of a CMOS circuit arise and, in the future, what will the factors be that will affect this leakage power consumption. **(2)**

c. Give one example of a technique that could be used to reduce power consumption at each of the following levels of circuit/system design – identifying how the reduction in power consumption comes about.

i) Architecture **(4)**

ii) Logic **(4)**

d. A 2-input, minimum-sized NAND gate is driven by two random, unrelated input signals. These signals are derived from a circuit that is clocked at 400MHz. It is estimated that the probability of each input signal changing state is 0.25. The NAND gate is driving a load capacitance of 10fF. Estimate the dynamic power consumption associated with switched capacitance in the NAND gate and the load that it drives (you may assume that other interconnect capacitance can be neglected).

(For the CMOS process: $m_E=0.08m^2/Vs$, $m_H=0.04m^2/Vs$, $t_{OX}=10nm$, $W_{min}=1mm$, $L_{min}=0.25mm$, $e_0e_r=3.45x10^{-11}F/m$, $V_{DD}=3.3V$, $V_{TN}=-V_{TP}=0.6V$) **(4)**

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