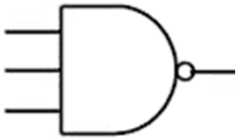
CMOS Characteristics

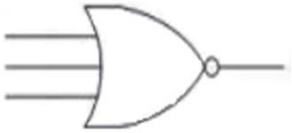
- Fan-in
- Logic Levels & Noise Margin
- Power Dissipation
- Practical Considerations

Fan-In

For a particular logic family, the number of inputs that a logic gate can have is known as the fan-in.

symbol transistor network symbol transistor network





For NAND and NOR gates, more inputs can be obtained by expanding the number of transistors in the pull-up and pull-down networks.

Fan-in is limited by the ‘on’ resistance of the series transistors.

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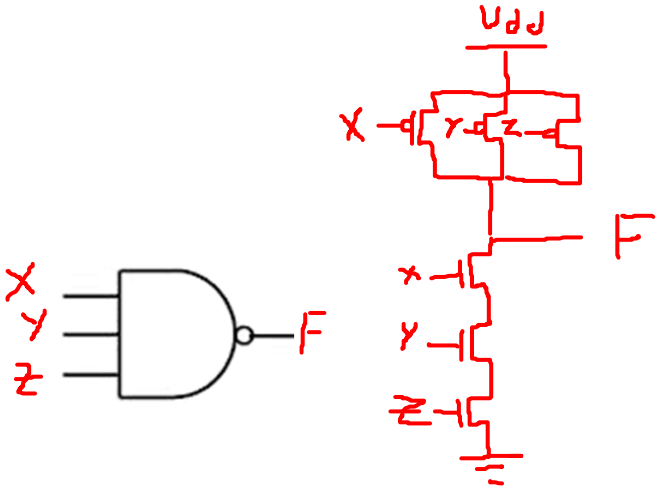

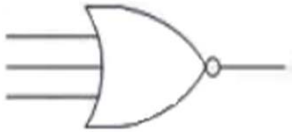

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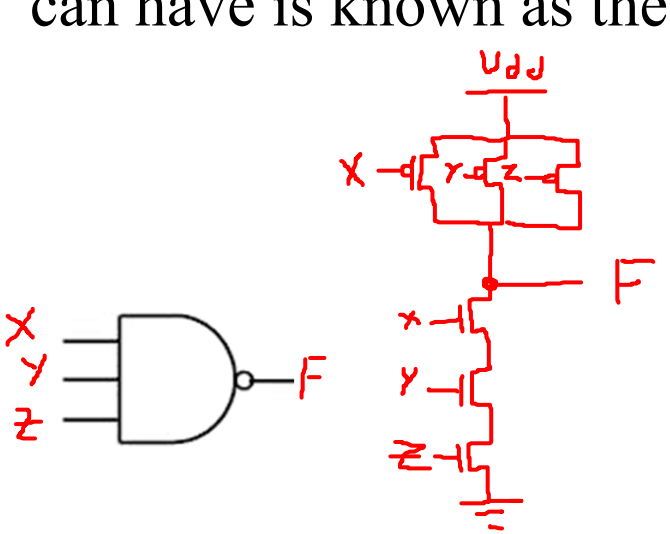
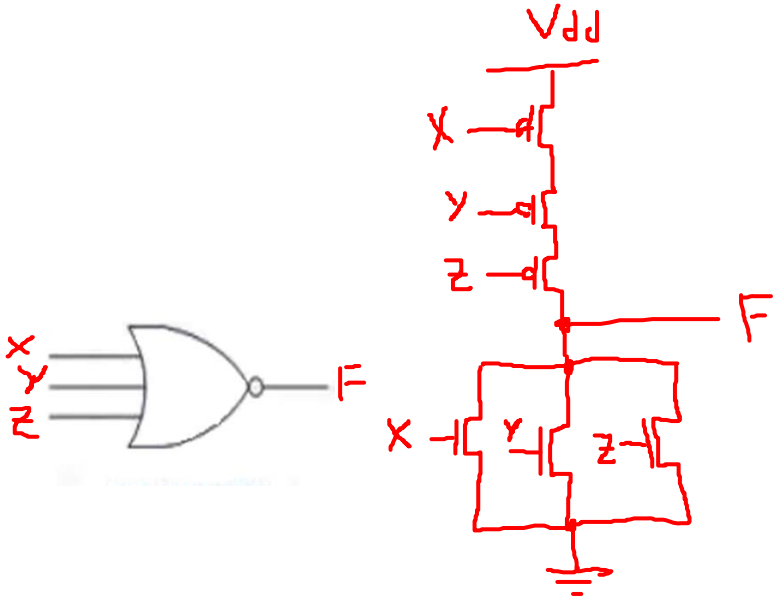


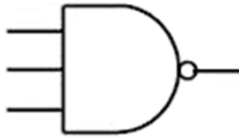


For NAND and NOR gates, more inputs can be obtained by expanding the number of transistors in the pull-up and pull-down networks.

Fan-in is limited by the ‘on’ resistance of the series transistors.

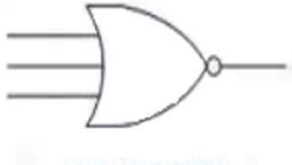
NAND ≡ NOT AND

X	Y	$\overline{X.Y}$
0	0	1
0	1	1
1	0	1
1	1	0

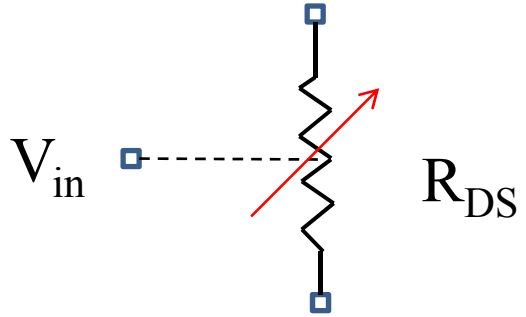


NOR ≡ NOT OR

X	Y	$\overline{X + Y}$
0	0	1
0	1	0
1	0	0
1	1	0



MOS transistor can be viewed as a voltage controlled resistance.



- nmos transistors have a lower ‘on’ resistance than pmos transistors.
- A series connection of *k* nmos devices will have a lower ‘on’ resistance than *k* pmos devices for a given silicon area.
- *k*-input NAND gate generally faster and preferred to *k*-input NOR gate.
- Fan-in typically 4 for NOR gates and 6 for NAND gates.

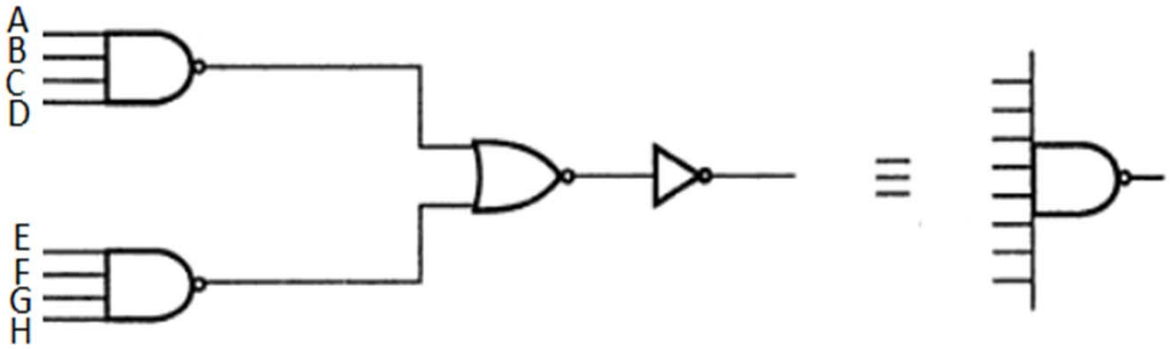
How can we increase the fan-in further ?

Consider the 8-input NAND function:

$$F = \overline{A.B.C.D.E.F.G.H}$$

By De Morgan $$F = \overline{A.B.C.D} + \overline{E.F.G.H}$$

By Involution $$F = \overline{\overline{A.B.C.D} + \overline{E.F.G.H}}$$



Cascading gates with fewer inputs will generally result in smaller faster circuits.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

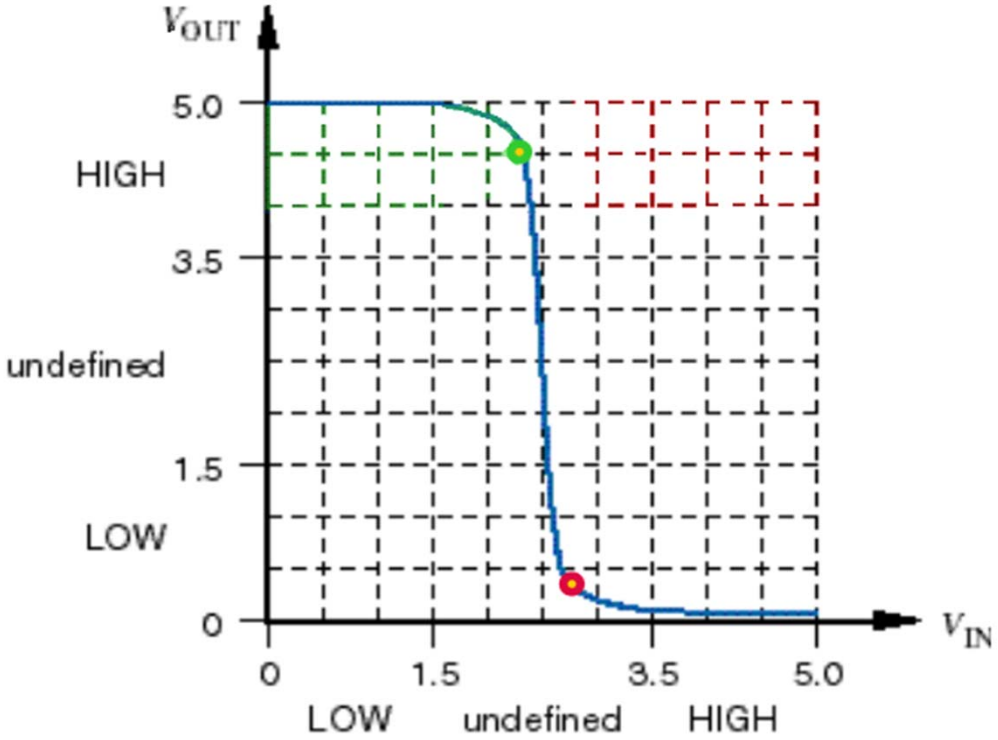
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	–1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	–0.7	–1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ µA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ µA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	µA

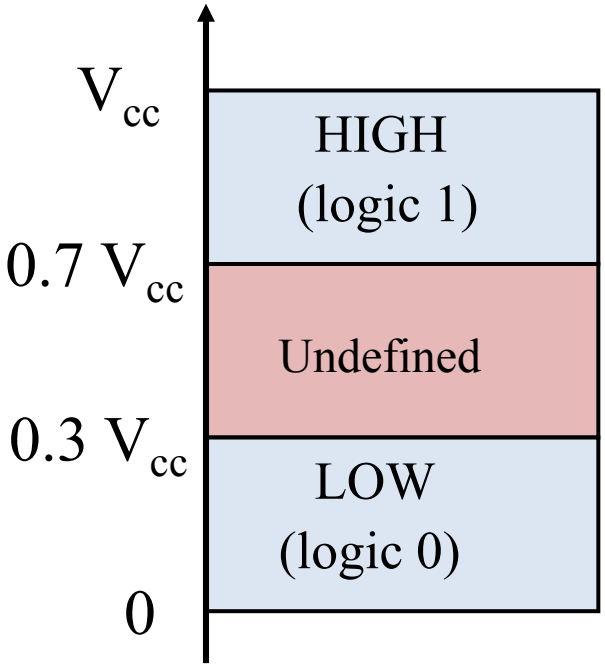
SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

CMOS Logic Levels and Noise Margin



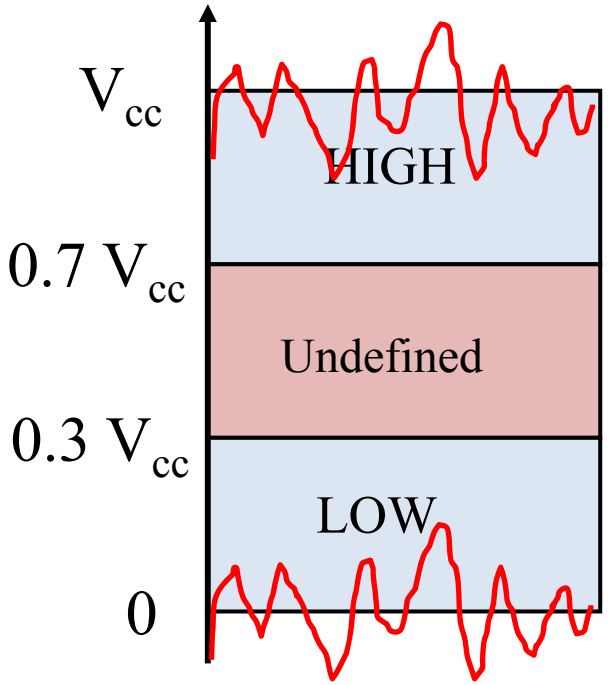
This is the typical transfer characteristic for a CMOS inverter. It may vary due to power supply variation, temperature, load, fabrication conditions etc.



CMOS logic levels

CMOS voltage levels are typically a function of the power supply rails.

The input levels are dictated by the switching thresholds of the transistors. The output levels are decided by the 'on' resistance of the transistors.



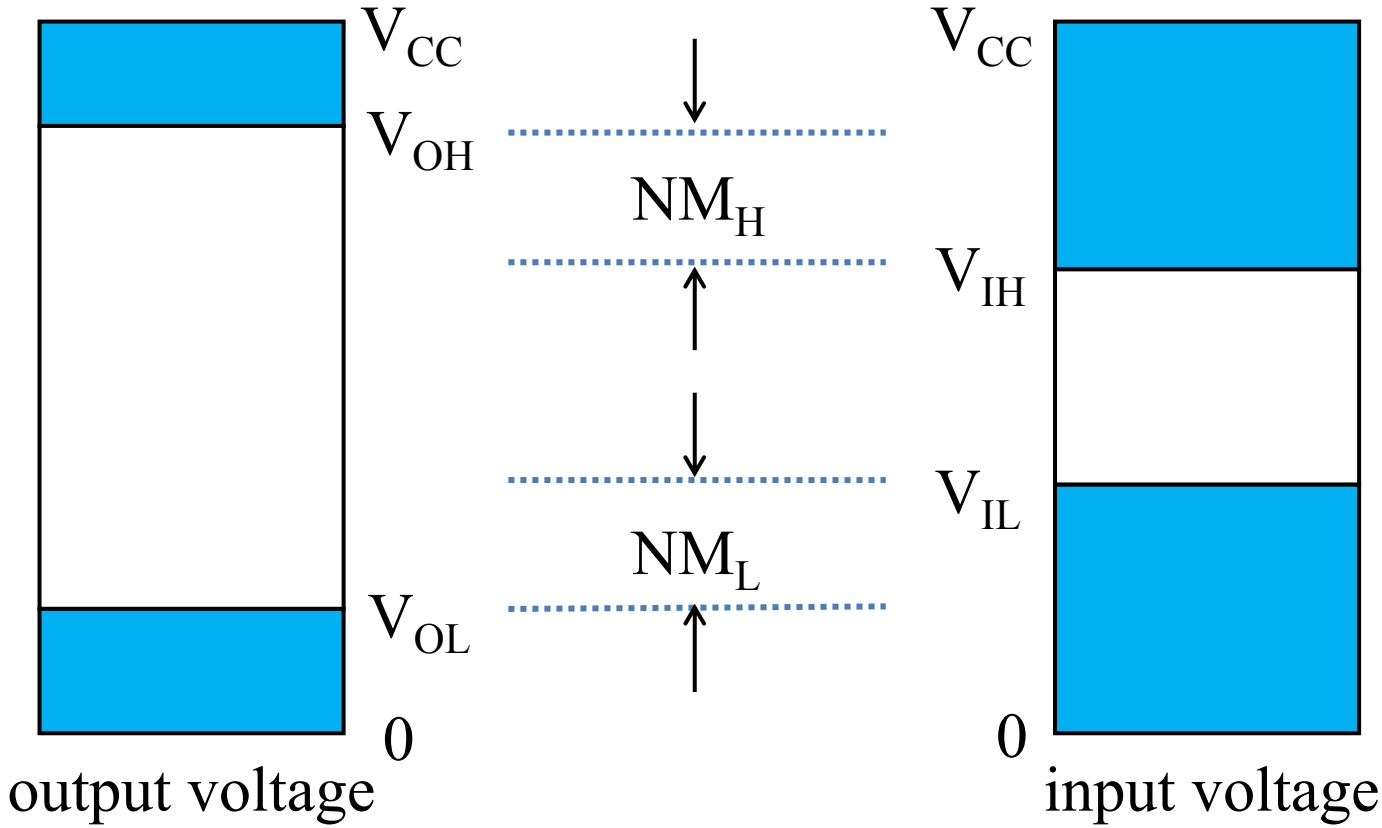
V_{OHmin} minimum output voltage produced for HIGH

V_{IHmin} minimum input voltage recognised as a HIGH (70% of V_{cc})

V_{ILmax} maximum input voltage recognised as a LOW (30% of V_{cc})

V_{OLmax} maximum output voltage produced for LOW

The noise margin shows the level of noise that can be tolerated on an output before it is not recognized by an input.



High-state noise margin $NM_H = V_{OH} - V_{IH}$

Low-state noise margin $NM_L = V_{IL} - V_{OL}$

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Power Consumption

There are two components to power consumption in CMOS circuits:

- Static power consumption
- Dynamic power consumption

Static Power Consumption : CMOS circuits consume little power when the outputs are not switching as leakage currents are very small.

$$P_S = I_{CC} \times V_{CC}$$

Where: V_{CC} = supply voltage , I_{CC} = leakage current

However, leakage power is becoming more important with decreasing device sizes.

Dynamic Power Consumption in CMOS circuits has two parts:

- Transient power consumption P_T
- Capacitive-load power consumption P_L

P_T is the power due to the partial short-circuiting of the transistors during switching. At this point, both transistors can be partially *on* allowing current flow from V_{DD} to ground.

$$P_T = C_{PD} \times V_{CC}^2 \times f$$

C_{PD} is the power dissipation capacitance (specified by manufacturer) and *f* is the switching frequency.

$\mathbf{P_L}$ is the power consumed in charging external load capacitances.

$$P_L = C_L \times V_{CC}^2 \times f$$

$\mathbf{C_L}$ is the external load capacitance.

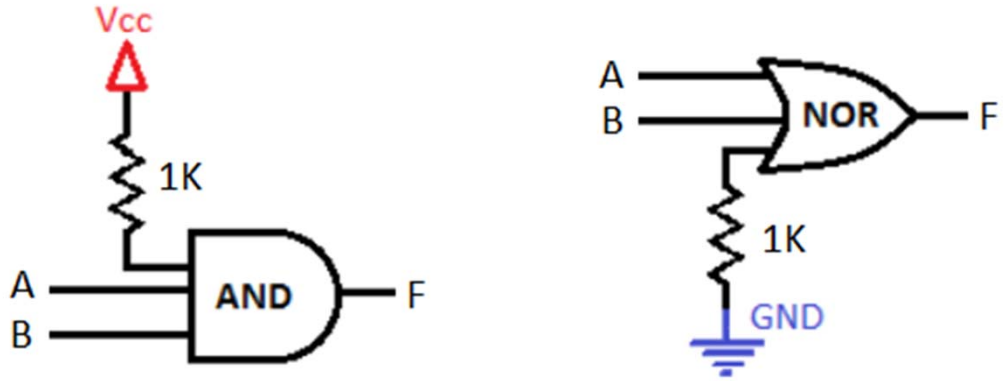
Not all gates will be switching every clock cycle so the dynamic power is often multiplied by α which is a switching activity factor. A system clock has an activity factor α = 1 as it rises and falls every cycle. A typical activity factor for data would be α = 0.1.

$$P_{total} = P_{static} + P_{dynamic}$$

Practical Considerations

Unused CMOS inputs should not be left unconnected (floating).

- tie to another input
- tie HIGH for AND/NAND gates
- tie LOW for OR/NOR gates



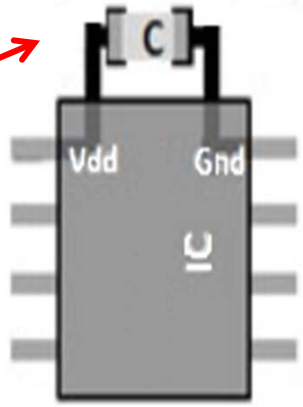
CMOS devices are easily damaged by static. Ensure you are 'earthed' before handling, hold boards by the edges.

Decoupling Capacitors

When a CMOS output switches, both n-channel and p-channel transistors are partially on at the same time. This leads to current spikes which appear as noise on the power supply connections.

On a PCB, decoupling capacitors should be used to provide a reservoir of charge. This helps to reduce the noise in the power distribution network.

Place between V_{dd} and ground as close as possible to IC.



Use 0.1 µF up to 15MHz, above use 0.01 µF. Check application notes.