Analog-to-Digital Conversion (ADC)

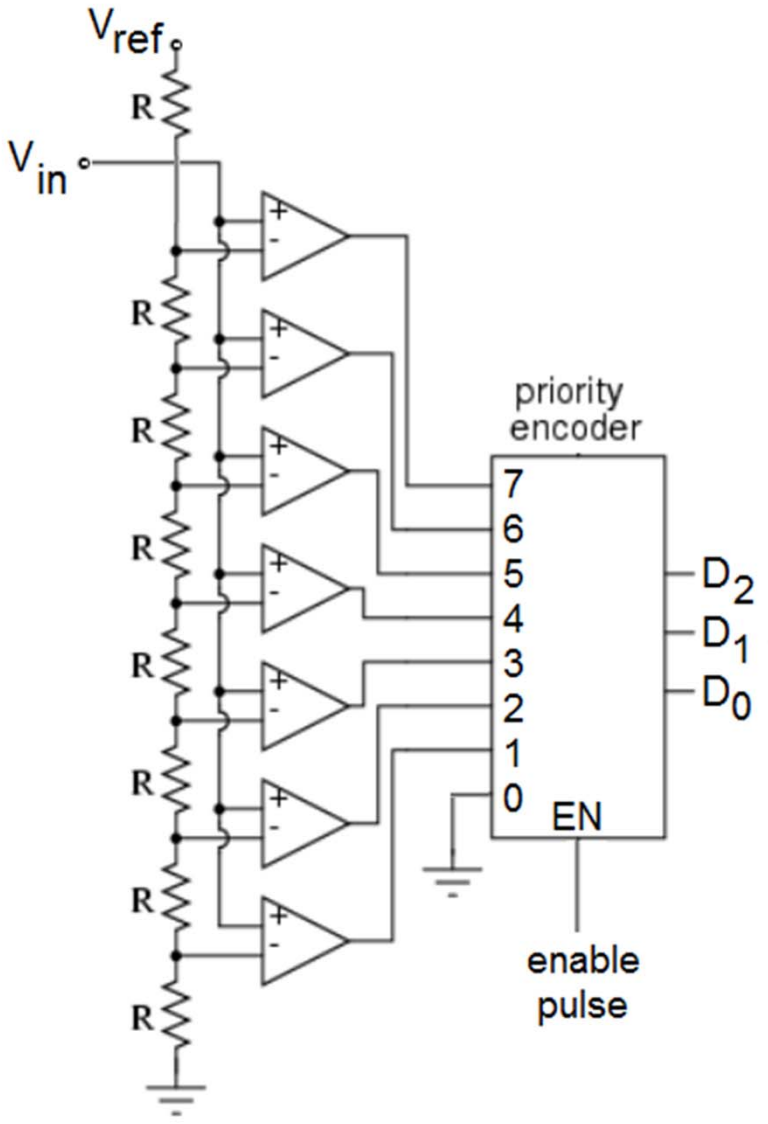
- Flash (Parallel) Converter
- Successive Approximation ADC

Flash (Parallel) ADC

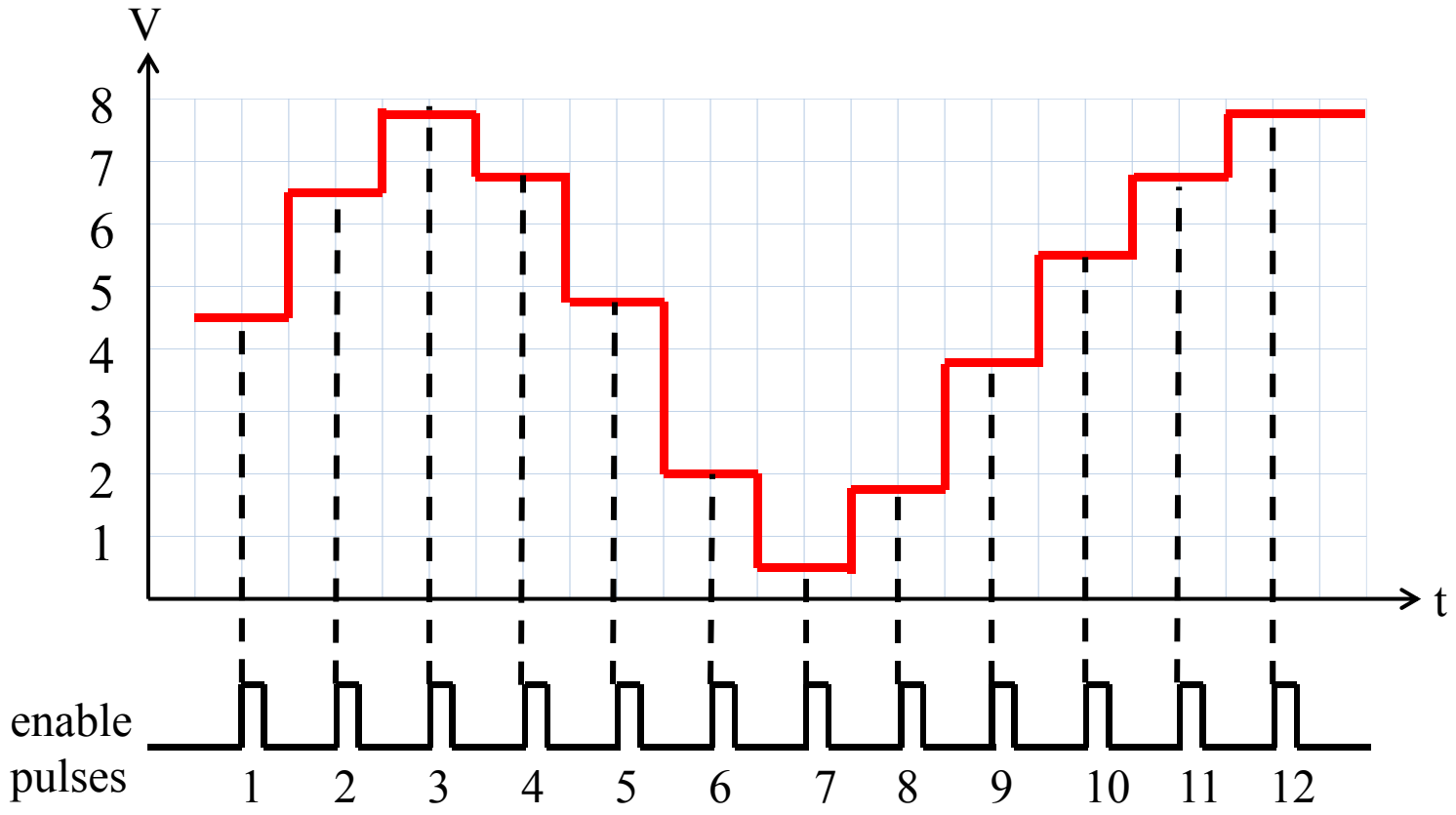
Comparators are used to compare a reference voltage with the analog input voltage V_{in}. If the input to a certain comparator is greater than the reference voltage, then a 'HIGH' is output from that comparator.

The reference voltage for each comparator is obtained from the resistor voltage-divider circuit.

When the priority encoder is enabled by a 'HIGH' enable pulse, a 3-bit code representing the input voltage is produced. It is obtained from the highest order input having a 'HIGH'.

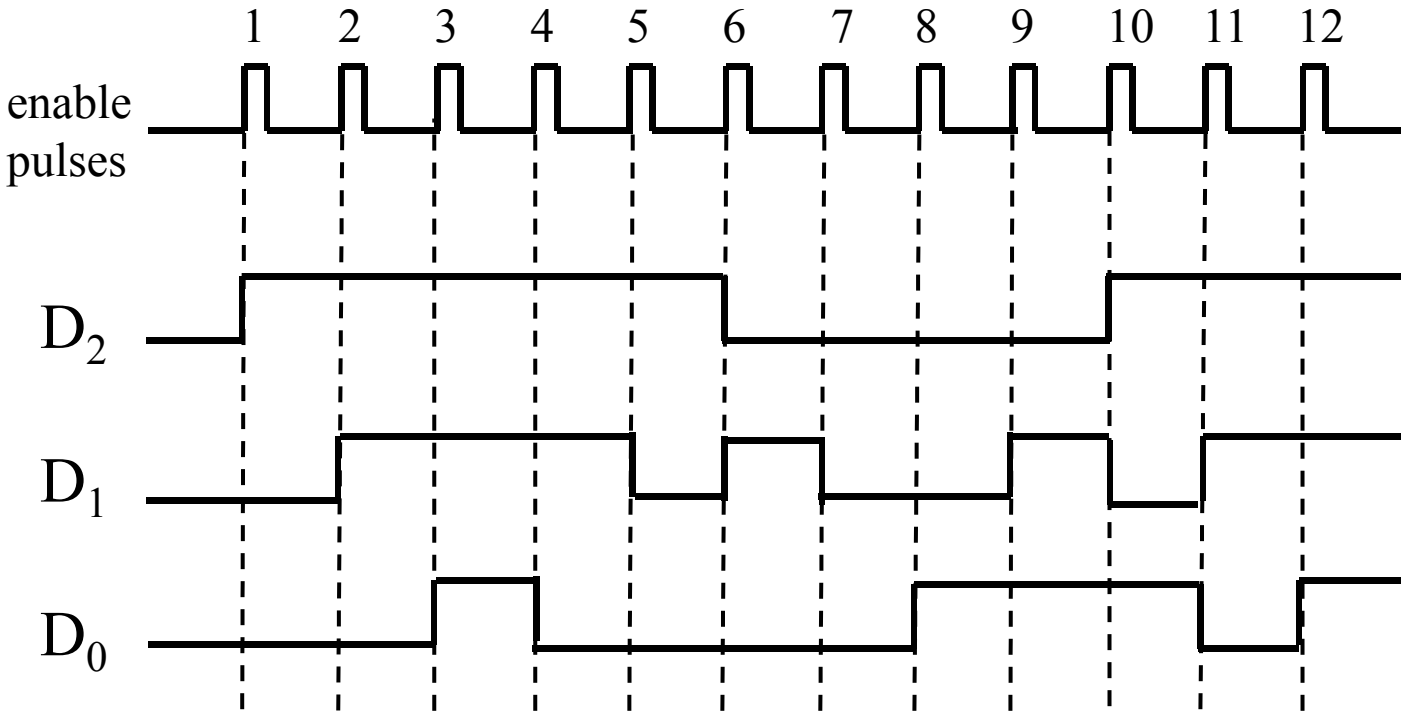


Example: A 3-bit flash ADC takes the analog input shown from a sample-hold circuit. What is the output from the ADC using the enable pulses shown and reference voltage of +8V .



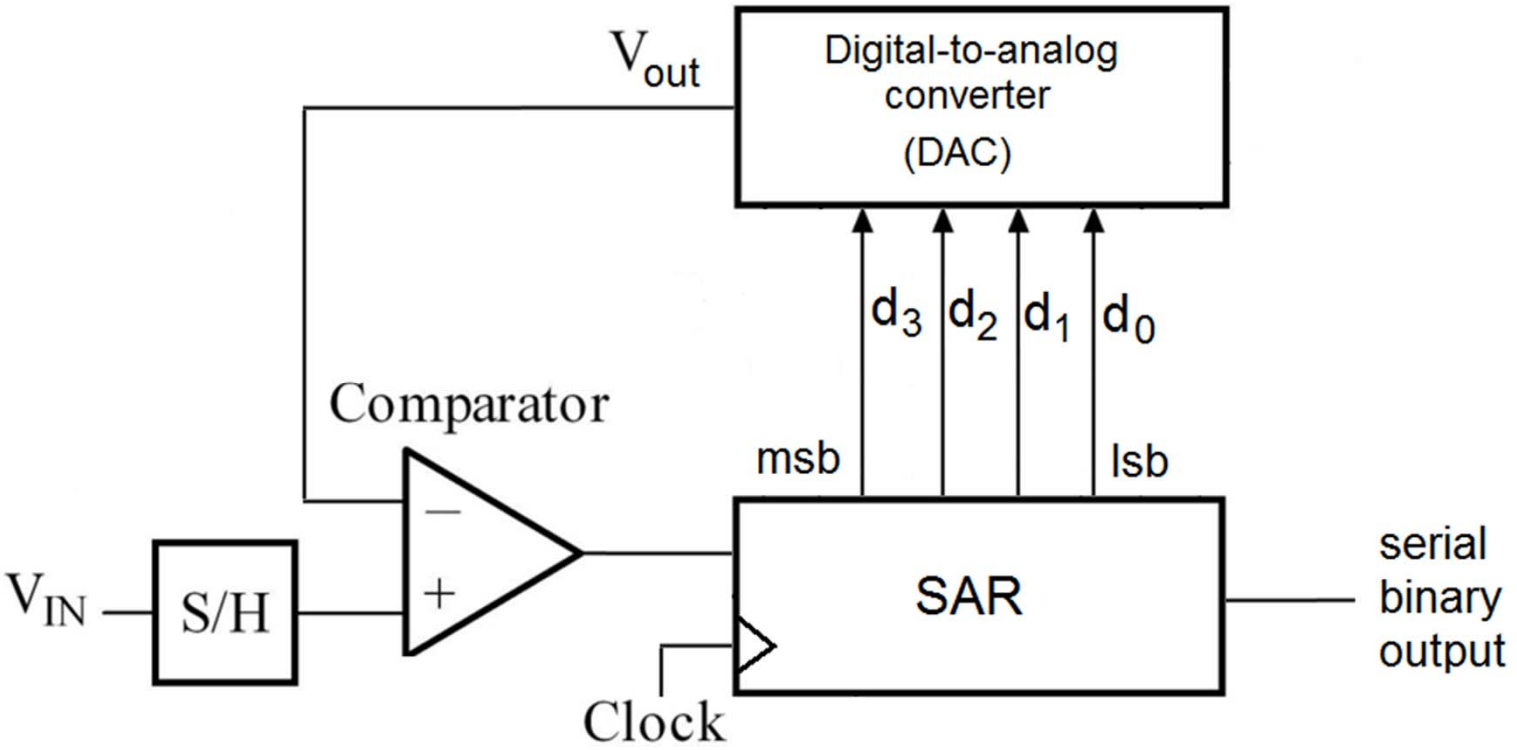
The digital output sequence is:

100, 110, 111, 110, 100, 010, 000, 001, 011, 101, 110, 111



Flash converters have the advantage of being fast but a disadvantage is the large number of comparators required.

Successive-Approximation ADC

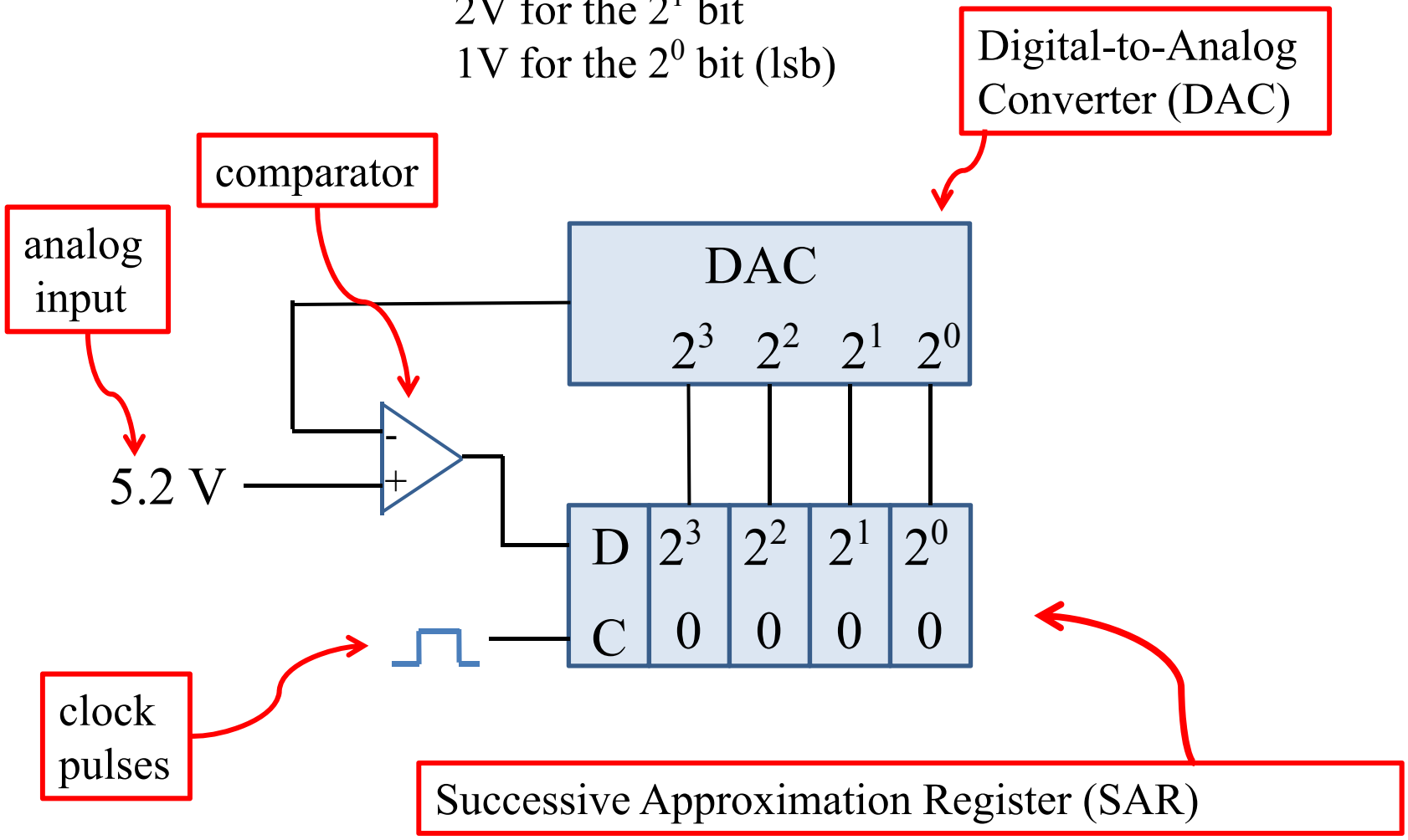


SAR – Successive Approximation Register

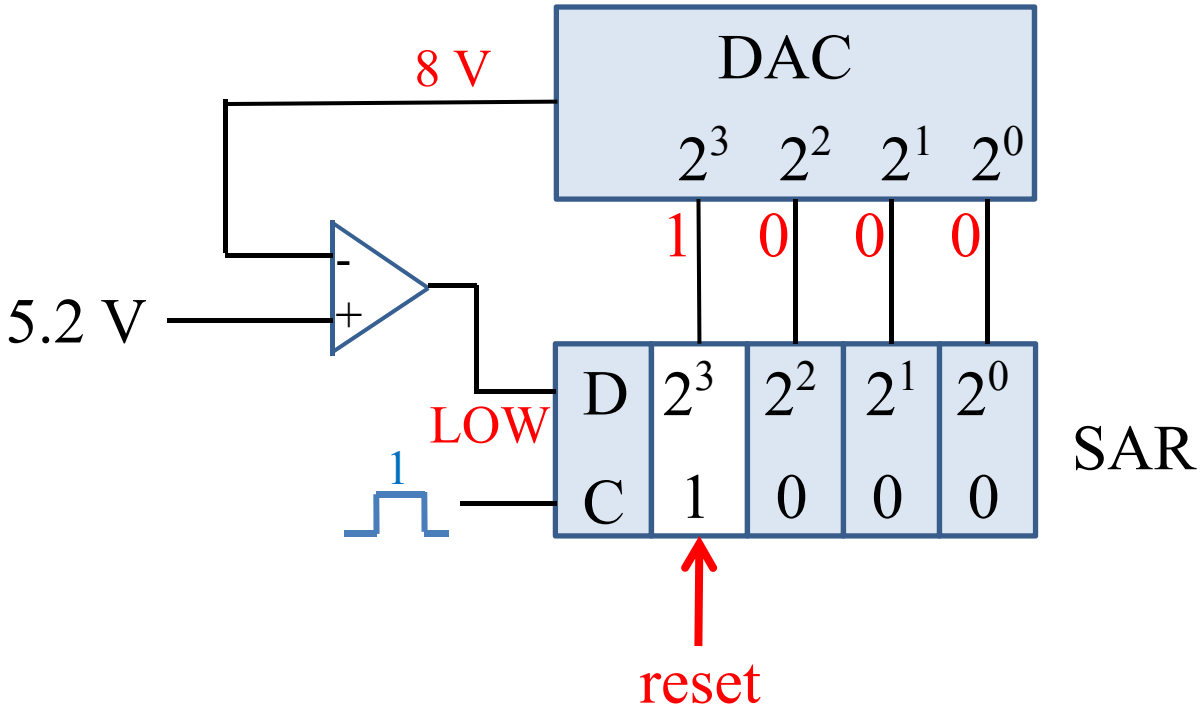
- Starting with the msb, set each input to the DAC to a ‘1’ one at a time
- For each setting, the DAC produces an output V_{out}
- Compare V_{out} with the input voltage V_{in}
- If the DAC output is greater than the input ($V_{out} > V_{in}$) the comparator will give a low output
- A low on the comparator output resets the set bit in the register
- If the DAC output is less than the input ($V_{out} < V_{in}$) the comparator will give a high output and the set bit in the register is retained.
- The msb is examined first, then the next most significant bit, then the next until all bits have been tried.
- When all bits have been tried, the conversion is complete

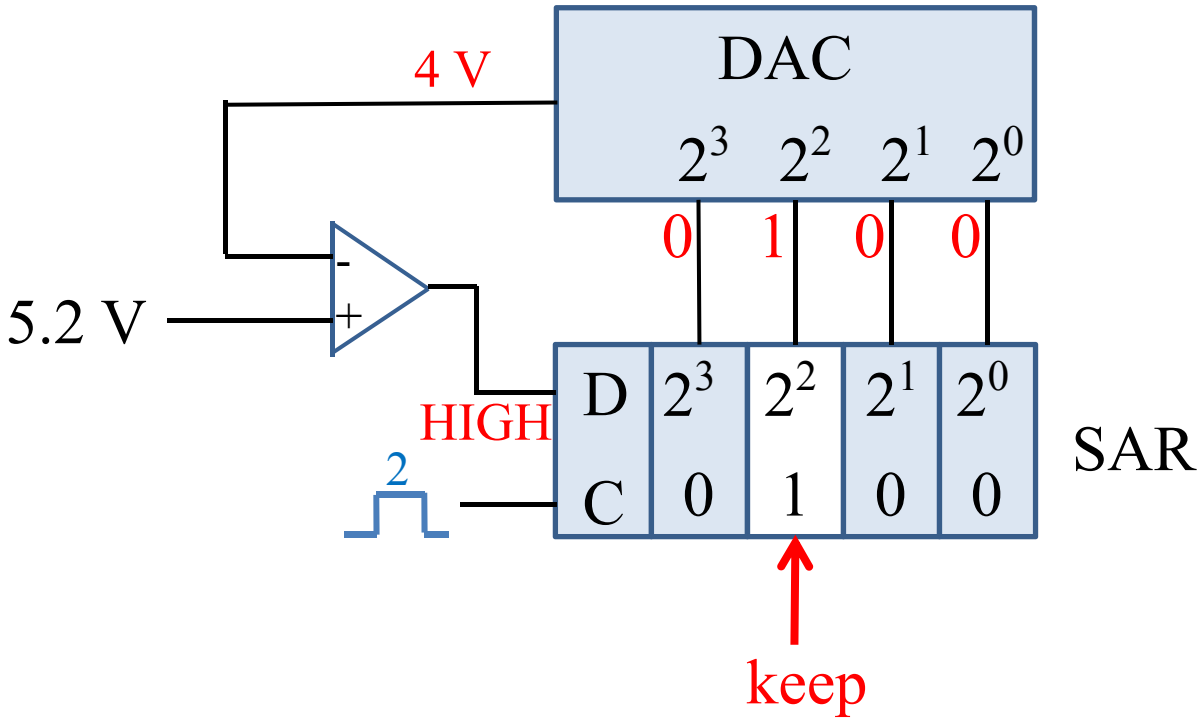
Consider the four bit conversion of a constant input voltage of 5.2V.

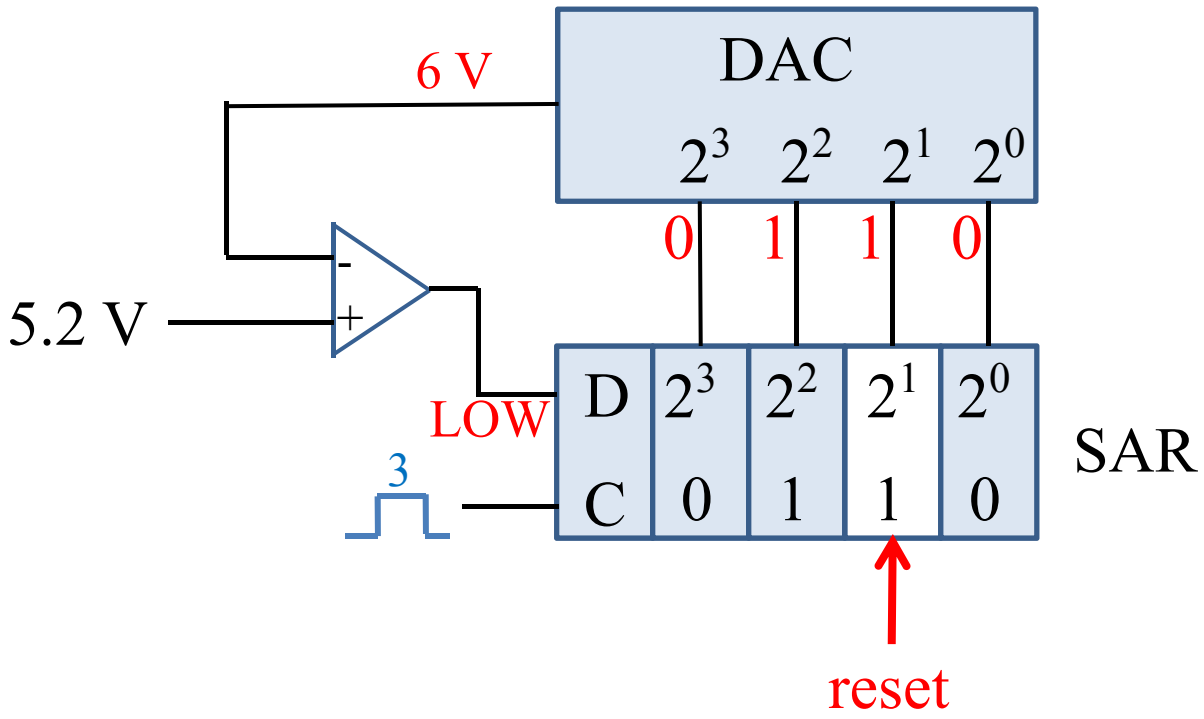
Assume the DAC outputs : 8V for the 2^3 bit (msb)
4V for the 2^2 bit
2V for the 2^1 bit
1V for the 2^0 bit (lsb)

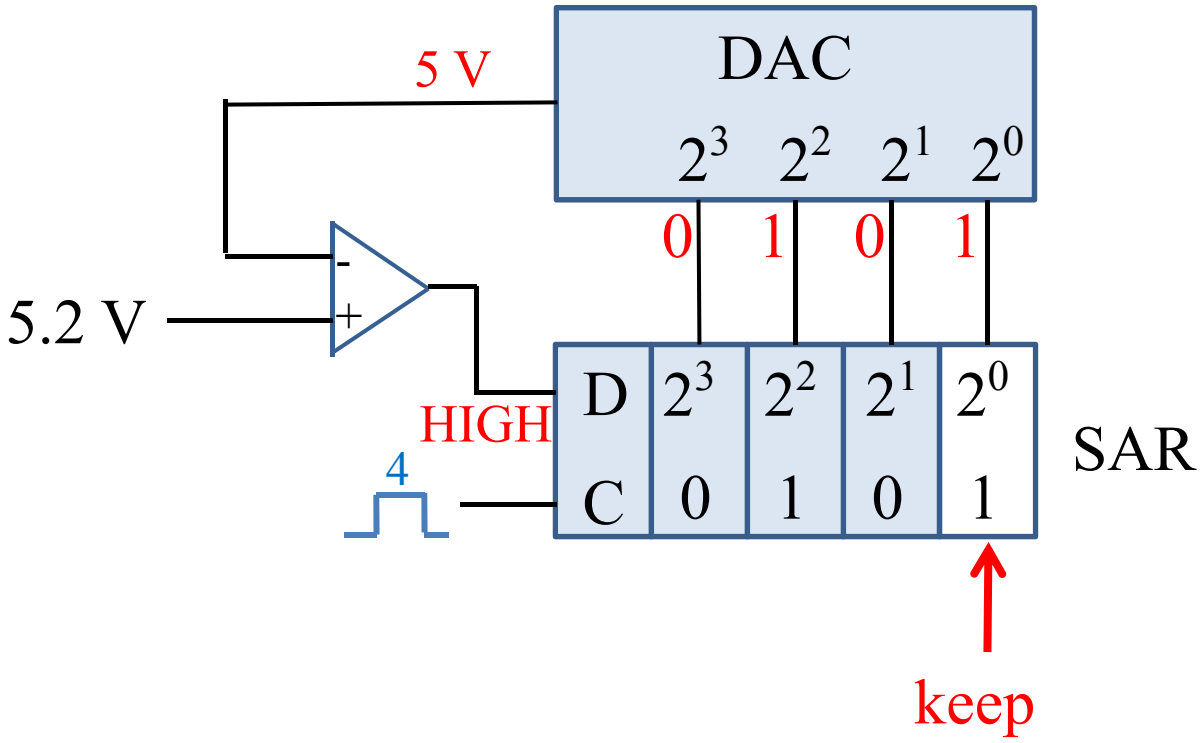


2^3 trial – DAC output 8V which is greater than




4 V
DAC
2^3 2^2 2^1 2^0
0 1 0 0
5.2 V
-
+
HIGH
D 2^3 2^2 2^1 2^0
C 0 1 0 0
SAR
2
keep


6 V
DAC
2^3 2^2 2^1 2^0
0 1 1 0
5.2 V
-
+
LOW
D 2^3 2^2 2^1 2^0
3
C 0 1 1 0
SAR
reset


5 V
DAC
2^3 2^2 2^1 2^0
0 1 0 1
5.2 V
-
+
HIGH
4
D 2^3 2^2 2^1 2^0
C 0 1 0 1
SAR
keep