EEE119 2015 Solutions

1. a. (i)

A B C	F
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	1
1 0 0	0
1 0 1	1
1 1 0	1
1 1 1	1

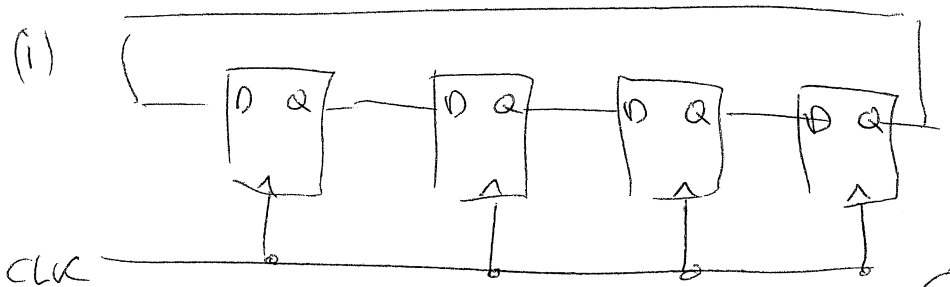
(2)

(ii)

$F = (A+B+C)(A+\bar{B}+C)(\bar{A}+B+C)$

(2)

b. (i)

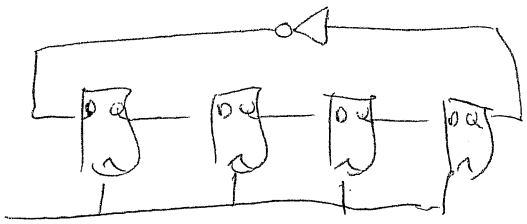


(4)

one bit must be set high initially

1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1
1 0 0 0 repeat

(ii)



(4)

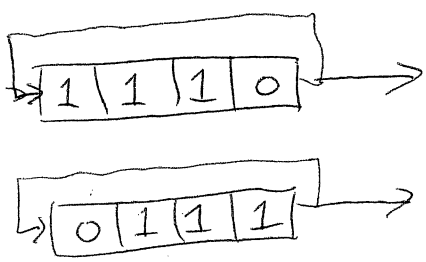
0 0 0 0
1 0 0 0
1 1 0 0
1 1 1 0
1 1 1 1
0 1 1 1
0 0 1 1
0 0 0 1
0 0 0 0 repeat

(iii) ring counter $\frac{1}{25ns} = 40MHz$

twisted ring $\frac{1}{40ns} = 25MHz$

(3)

c.



(5)

Both registers clocked with same 10 MHz clock. reg1 initialised to 1110
reg2 initialised to 0111

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(12)

2.a(i) Moore → output is state or decoded from state

~~(ii)~~ Mealy → input can be used to directly form the output. (2)

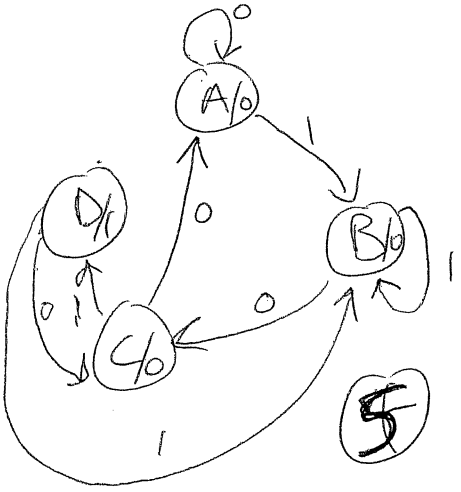
(ii) Binary → 2^n states where n is the number of flip flops

One-hot → one flip flop per state (2)

(iii) non-resetting can use bits from a previous match in a new match. Resetting starts looking at the next bit after a match (2)

b.

A - reset state
B - 1 found
C - 10 found
D - 101 found

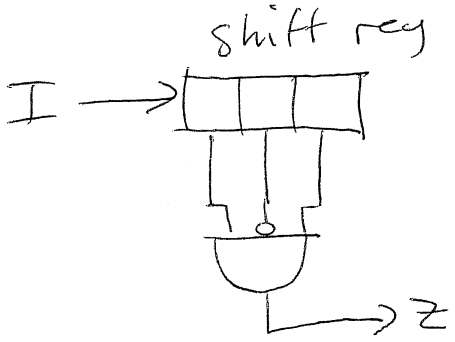


(5)

Present State	I/p	Next State	O/p
A	0	A	0
	1	B	
B	0	C	0
	1	B	
C	0	A	0
	1	D	
D	0	C	1
	1	B	

(5)

c.



This would not work for resetting behaviour as it decodes every occurence of 101.

(4)

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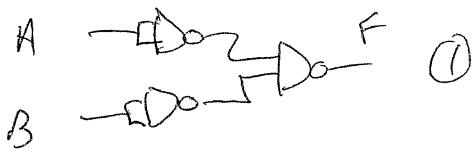
P3

3. a

AB	F
00	0
01	1
10	1
11	1

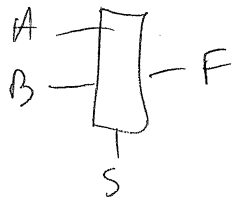
(1)

$F = A+B = \overline{\overline{A+B}} = \overline{\bar{A}.\bar{B}}$ (2)



(1)

b(i)



Mux selects data from two inputs under control of S

S	F
0	A
1	B

(4)

(ii)

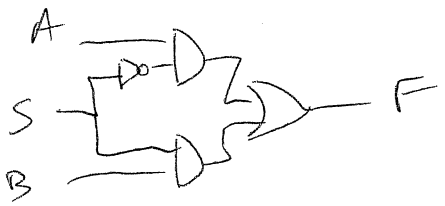
SAB	F
000	0
001	0
010	1
011	1
100	0
101	1
110	0
111	1

$F = \bar{S}A\bar{B} + \bar{S}AB + S\bar{A}B + SAB$

$= \bar{S}A(B+\bar{B}) + SB(A+\bar{A})$

$= \bar{S}A + SB$

(4)



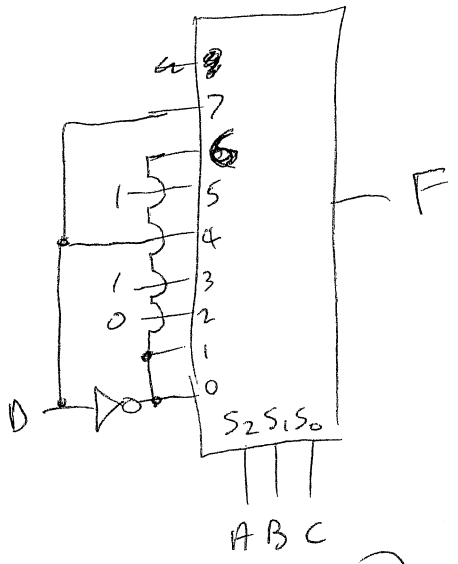
Possibility of glitch on F due to race condition on the select line S

(2)

C.

ABCD	F
0000	1
0001	0
0010	1
0011	0
0100	0
0101	0
0110	1
0111	1
1000	0
1001	1
1010	1
1011	1
1100	1
1101	0
1110	0
1111	1

(2)



(4)

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(P4)

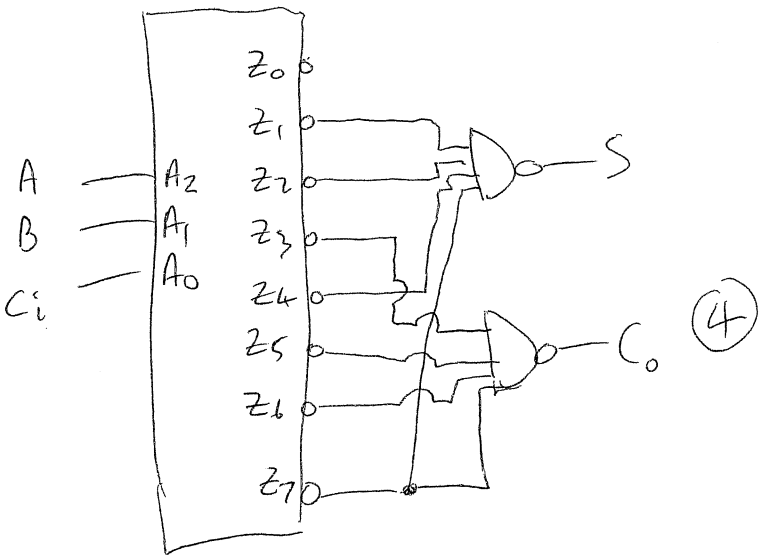
4. (a)

A B C_i	S	C_o
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

(2)

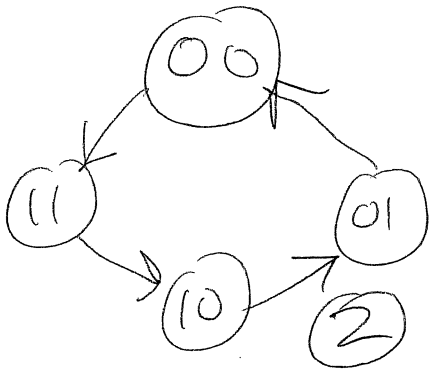
$S = A \oplus B \oplus C_i$

$C_o = AB + (A \oplus B)C_i$ (4)



(4)

(b)



(2)

$Q_1 Q_0$ Present State	$Q_1 Q_0$ Next State
00	11
01	00
10	01
11	10

(2)

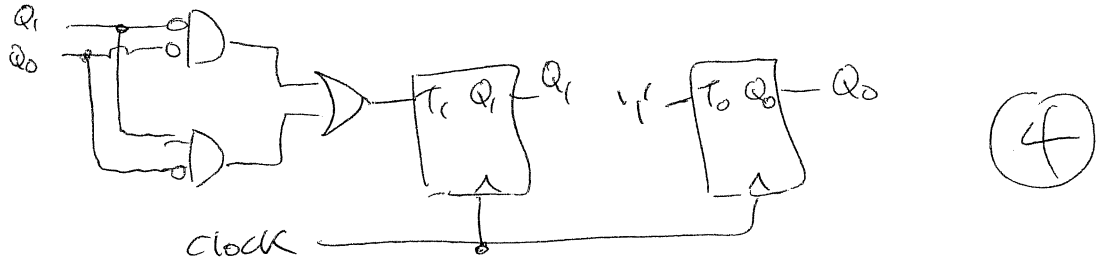
T-type toggles when T input is '1'

T	Q
0	Q
1	$\bar{Q}$

(2)

Q_0 toggles every clock

Q_1 toggles when $Q_1Q_0 = 00$ or $Q_1Q_0 = 10$



(4)