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1 (a) The outer electronic configurations are: Ga s^2p and As s^2p^3. The atoms bond together in the GaAs crystal lattice by forming tetrahedrally-oriented sp^3 hybrid orbitals and then sharing one pair of electrons in each. Because the initial atoms have unequal numbers of electrons in their outer shells, they make unequal contributions to the shared pairs and the bonds exhibit some polarity. The binding energy of the two atoms follows the characteristic of a Morse curve (diagram required) with a combination of attractive and repulsive potentials.

(b) Plane spacing $d_{hkl} = a_0 /\sqrt{(h^2 + k^2 + l^2)}$

For (110) $d_{220} = 0.3567/\sqrt{(1 + 1 +0)}$nm
$= 0.2522$nm

For (211) $d_{310} = 0.3567/\sqrt{(4 + 1 + 1)}$
$= 0.1456$nm

For (310) $d_{311} = 0.3567/\sqrt{(9 + 1 + 0)}$
$= 0.1128$nm

For (422) $d_{422} = 0.3567/\sqrt{(16 + 4 + 4)}$
$= 0.07281$nm

(c) Angle between planes $(h_1k_1l_1)$ and $(h_2k_2l_2)$ is given by
$\cos^{-1}[(h_1h_2 + k_1k_2 + l_1l_2)/\sqrt{((h_1^2 + k_1^2 + l_1^2)(h_2^2 + k_2^2 + l_2^2))}]$

$(100) \wedge (110) = \cos^{-1} [1/\sqrt{2}] = 45^o$
$(111) \wedge (311) = \cos^{-1} [5/\sqrt{33}] = 29.50^o$

(d) $[0\bar{1}1]\cdot[31\bar{1}] = -2$ then $(0\bar{1}1)$ is not perpendicular to $(31\bar{1})$

$[\bar{1}00]\cdot[\,0\bar{1}4] = 0$ then $(\bar{1}00)$ is perpendicular to $(0\bar{1}4)$

$[\bar{1}10]\cdot[\,224] = 0$ then $(\bar{1}10)$ is perpendicular to (224)

(e) If the close-packed planes are designated A, B and C, the following are the required stacking sequences:

intrinsic fault: ABCABCACABCABC

extrinsic fault: ABCABCACBCABCABC

twin: ABCABCBACBABCABC

(f) In Zinc Blende crystals, the group III and Group V atoms alternate throughout the lattice. This results in the most strongly bonded terminating atoms on the {111} type faces being either the Group III or the Group V species and the faces are different on opposite sides of the crystal. These differently terminated surfaces then exhibit different electron densities, the Group III face having a lower electron density than the Group V face. The different faces have different physical properties (under eg etching or crystal growth conditions) and this is the 'polarity' referred to. For comparison, the Si lattice contains only one type of atom (Si) so that the {111} type faces all have the same structure and exhibit no 'polarity' phenomenon.

2(a) **Photolithography**

The present state-of-the-art

- Si ICs with millions of transistor cells and line widths down to 0.1μm are now in standard production and devices with line widths of 0.045μm are in more limited production
- ***photolithography*** using light-optical radiation can meet all these wafer patterning requirements
  - ° I-line radiation at 365nm from a high pressure Hg arc lamp is used for masks with only □relatively coarse□ features
  - ° ***deep-UV*** radiation at 248nm wavelength from ***KrF excimer lasers*** is used for finer features
  - ° further resolution gains are being achieved by changing to 193nm radiation from ***ArF excimer lasers***
  - ° fluorine lasers may be used to reduce radiation wavelength to 157nm

Photoresists provide the medium on the wafer surface for the pattern transfer process

- they contain four components
  - ° a ***resin polymer*** giving body to the resist
  - ° a ***light-sensitive compound***
  - ° a ***solvent***, the amount of which determines the resist viscosity
  - ° ***additives*** such as dyes and surface levelling agents
- the resist solubility is altered by exposure to light so that part of an exposed layer can be removed leaving a pattern
  - ° if less soluble after irradiation - ***negative resist***
  - ° if more soluble after irradiation - ***positive resist***

    positive resists generally offer the highest resolution and are used for most applications

Oxide patterning

- Si wafer with a layer of oxide is first baked to dehydrate its surface and give good resist adhesion
  - ° the surface may also be treated with a chemical adhesion promoter

- the wafer is next spin-coated with a layer of photoresist
  - ° in general, the thickness of the photoresist cannot be greater than 3.5 times the size of features to be defined
    - the viscosity of the resist is important for control of the layer thickness
  - ° the layer will usually receive a short bake to consolidate it by driving off the solvent
- resist is exposed to UV light which passes through the clear areas of a mask
  - ° mask is a glass plate with a precise circuit pattern of clear and opaque areas defined in a ***chromium layer*** on one surface (see below)
    - the mask is first ***accurately registered*** with respect to previous patterns on the wafer: fiducial marks used, with advanced image recognition technology and laser interferometer positioning
  - ° the lithography apparatus is called a ***stepper*** because one IC cell is exposed at a time and the whole wafer is covered in a ***step-and-repeat process***
    - for very high levels of resolution, the pattern for each IC may be transferred by mechanical scanning across a rectangular beam of DUV light: averages system aberrations
- in case of ***positive resist***, the opaque mask areas are located where the oxide is to remain on the surface
  - ° light destroys a dissolution inhibitor by photochemical rearrangement
  - ° matrix of exposed resist is removed by dissolution (***development***) in aqueous base solution
- after ***hardening*** in a further baking step, the patterned resist is resistant to eg HF solution or dry etch plasma
  - ° first resist pattern is checked for errors
    - can be reworked if necessary
  - ° then oxide removed in areas not covered by resist
- final step is to remove the photoresist (by specially tailored plasma etching)
  - ° the geometric pattern has then been transferred to the oxide layer

2(b) ***Definition of metal tracks***

- often carried out by a ***lift-off process***
  - ° circuit covered by a resist (negative resist in this example) which is exposed through a patterned mask, developed and dissolved so that openings are made where metal is to remain (**Figure**)
  - ° metal is then deposited: when the remaining resist is removed it takes with it overlying metal, leaving patterned metal on the circuit

2(c) **Electron and X-ray Lithography**

In ***electron lithography***, patterns can be formed in two ways

- ***scanned beam lithography*** uses a finely focused electron spot to sequentially scan and expose the required pattern in a specially formulated ***electron resist***
  - ° can be used for direct write on wafer, but is slow due to serial nature
    may be used, in eg III-V technology, to define especially fine structures such as very narrow FET gates
  - ° often used to generate the ***patterns on masks***
    each mask is used to pattern many wafers by photolithography
- ***projection electron lithography*** uses a flood-beam to expose a resist
  - ° scattering but low absorption mask and aperture system employed in SCALPEL technique (Lucent Technologies)
  - ° still under development with feature sizes below 0.1μm
    may be employed when photolithography becomes unsatisfactory

In ***X-ray lithography***, high resolution patterns are formed by X-ray exposure of a resist

- requires a ***synchrotron*** X-ray beam to obtain sufficient intensity
  - ° very high cost and still under development

3(a) **Chemical Vapour Deposition (CVD) of Epitaxial Si**

Several types of reaction involving Si-containing gases flowing over a heated substrate are possible

most important is the hydrogen reduction of silicon tetrachloride, which takes place on the heated surface

$$SiCl_4 + 2H_2 = Si + 4HCl$$

deposited Si atoms run around on the substrate and join steps at the edges of growing crystal planes extending across the surface

the deposition temperature is generally in the range 800-1200 C in order to give high quality, single crystal Si layers, with good thickness uniformity, at deposition rates in the range 0.01-5μm/min

prior to deposition, substrates would typically be given a vapour etch with flowing HCl or a bake in H_2 gas to clean their surfaces

A typical CVD apparatus has appropriate reagent and other gas lines feeding into a mixing manifold leading to the reaction chamber (diagram required)

the chamber generally has one of three generic designs, horizontal reactor, pancake (vertical) reactor and barrel reactor (diagrams required)

susceptor has wafers mounted upon it and is heated by RF coupling or by radiant heating from quartz halogen lamps

susceptor is often graphite coated with SiC since this will not react with any gases or introduce contaminants

gas flow in chamber must be very uniform to give layer thickness uniformity on each of the substrate wafers

Doping of grown layers is achieved by mixing a suitable hydride with the flowing hydrogen and $SiCl_4$ gases

arsine (AsH_3) or phosphine (PH_3) for n-type doping and diborane (B_2H_6) for p-type doping

must be careful to avoid so-called autodoping

diffusion of impurity from substrate must be outpaced by layer growth: can be checked by calculating the characteristic impurity diffusion length

The quality of epitaxial Si films must be high if they are to be employed for IC fabrication

if residual contamination is present on the substrate surface before epitaxy, stacking faults or even small pyramidal hillocks may be produced

nonuniform heating of the wafers can lead to slip and dislocation formation

3(b) Diffusion coefficient (D) = $D_0 \exp -[E_A/kT]$

At 1150°C (1423K) $D = 0.76 \times \exp -[3.46/(8.62 \times 10^{-5} \times 1423)]\ cm^2/s$

$= 0.76 \times \exp -[3.46/0.1227]\ cm^2/s$

$= 0.76 \times 5.62 \times 10^{-13}\ cm^2/s$

$= 4.27 \times 10^{-13}\ cm^2/s$

For 60s $2\sqrt{(DT)} = 2\sqrt{(4.27 \times 10^{-13} \times 60)}\ cm$

$= 1.01 \times 10^{-6}\ cm$

$= 0.1\mu m$

This diffusion length is of the same order as the thickness of the Si layer grown per minute, therefore, autodoping of the layer is likely to be a serious problem

3(c) **Internal Gettering**

This requires Si wafers containing ***oxygen*** at between about $7x10^{17}$ and $10^{18}/cm^3$ which are given carefully-controlled ***heat treatments***

Xfirst, high temperature (~1100EC) annealing to cause out-diffusion of oxygen at wafer surfaces to give micron-scale ***denuded zones***

Xsecond, low temperature (~700EC) annealing to cause initial precipitation of (supersaturated) oxygen to give SiO_2 nuclei

Xthird, high temperature (~1100EC) annealing to cause growth of nuclei giving larger SiO_2 precipitates which ***punch out dislocation loops*** in the Si lattice

<Heat treatments give a distribution of SiO_2 precipitates ***only*** in the ***central regions*** of the wafer away from device regions

Xthe dislocations punched out getter unwanted impurities as precipitates

4(a) **Metallization of Si**

Three main areas of application

<IC ***chip bonding*** to package support using Au-containing alloys (or sometimes other solders - see below)

XAu-containing alloys exploit ***eutectic*** exhibited by the Au/Si system

Ballows bond with support to be made by heating to only slightly >370EC

support must have good thermal expansion match to Si and is typically Fe-Ni alloy (alloy 42) or alumina ceramic

<***Formation of contacts*** to Si devices using Al (alternatives are silicides or W)

XAl metal film is deposited onto heavily-doped Si regions to be contacted (eg MOSFET source and drain exposed within oxide layer) and suitably patterned between them

Binitial deposited contacts exhibit unwanted Schottky behaviour

Xfilm is ***sintered*** at −400EC to obtain ***ohmic behaviour***

BSi is slightly soluble (−0.5%) in Al at sintering temperature, leading to formation of pits filled with Al in contact regions

junction spiking can occur

Bdissolution of Si can be controlled by using ***deposited Al containing a few % of Si*** to limit dissolution from the device and by accurately optimising the sintering conditions using short time ***RTP anneals***

such problems can be eliminated by use of silicide or W contacts

<***Formation of interconnects*** between devices using Al lines (polySi tracks may be used eg for local gate connections)

XAl has a suitably ***high electrical conductivity*** for interconnect fabrication

Binterconnects are produced by lithography (eg lift-off technique)

Bmany current ICs have multiple interconnect layers separated by deposited oxide insulator and connected layer-to-layer by vias

Xmodern small devices have especially narrow interconnects with very high current densities (perhaps $-10^6 A/cm^2$) and can fail by ***electromigration***

Bgradual transport of material along an interconnect, primarily involving grain boundaries, leaves voids at one end with hillocks forming at the other

the ***interconnect will fail*** by eg an open circuit occurring in the void-containing region

replacing the metallization with Cu

higher current carrying capacity, but must not be allowed to diffuse into underlying devices

4(b) **Silicides**

<Transition metal silicides are refractory materials, often with ***high electrical conductivities***

Xsilicides can be used both to improve the Si contact interface and to provide relatively stable, high temperature interconnect lines

<Early applications used $MoSi_2$, $TaSi_2$ and WSi_2 as ***interconnect materials***

Xoffered a possible reduction in electromigration rates and also the possibility of forming a protective coating of SiO_2 under heat treatment in an oxidising ambient

Xrequired relatively high temperature processing of deposited mixed metal/Si films to form required silicides

<More recent applications, with greatly reduced device dimensions, require even lower interconnect and contact resistances, together with ***lower processing temperatures***

Xencouraged the use of ***$TiSi_2$ and $CoSi_2$*** which can readily be formed at low temperature by ***direct reaction*** of, in each case, the metal and Si

Bat such temperatures, the metal does not react with surrounding oxide so that contact ***silicide formation is self-aligned*** - so-called ***salicide process***

<In the future, ***epitaxial silicides*** may become important because they offer potentially ideal interfaces with Si and higher temperature stability

Xcould be used as stable contacts to shallow junctions

4(c) <Bonding of the contact pads on the die (typically Al) to those on the package (typically Au, Ag or Cu) can be performed by

X***wire ball-wedge bonding***, often with ultrasonic assistance (Fig required)

Ba ***ball bond*** of Au (or Al) wire to a die bond pad allows the wire to bend in a range of directions to reach a package bond pad.

Bthe final ***wedge bond*** narrows the wire after the bond and allows it to break on retraction of the bonding head

Bafter formation of another ball end (by sparking or transient heating) the complete process can be repeated

at least 6-10 wire connections can be made per second in automatic bonding machines

X***flip chip bonding*** (Fig required)

Bsolder balls are placed on the die contact pads

Bthe chip is placed face down on the metal leads of the package and heat treatment produces soldered joints

interconnect density can be high and low inductance joints favour high frequency applications

5(a) **Molecular Beam Epitaxy (MBE)**

<Typically used to grow epitaxial layers of elemental and compound semiconductors

Xhomoepitaxy and heteroepitaxy

Xlayer growth takes place inside an ***ultrahigh vacuum*** (UHV) stainless steel chamber

X***in situ diagnostics*** allow layer growth to be closely monitored

typically reflection high energy electron diffraction is used to monitor surface structure

<A UHV environment is employed in order to minimise impurity incorporation into a growing layer

Xunwanted impurities generally have sticking coefficients upon the substrate of <<1

Ba base pressure of 10^{-10}-10^{-11}torr can give a background doping level of $-10^{14}cm^{-3}$

X***clean, oil-free pumps*** are used: sorption pumps at low vacuum, ion pumps and Ti sublimation pumps at high vacuum

Binternal panels cooled by liquid nitrogen condense background species

<A typical deposition chamber layout includes a substrate, deposition sources and a reflection high energy electron diffraction (RHEED) assembly

<The substrate mount provides ***heating and rotation*** capabilities for the substrate

Xsubstrate wafers are transferred into and out of the growth chamber through ***load-lock chambers*** with intermediate levels of vacuum

Xthe best epitaxy is often obtained at temperatures in the range 400-800EC, depending upon deposited material type

Xsubstrate rotation compensates for differences in source positions and ensures that deposited layers are ***uniform in thickness and composition***

<Beams of materials to be deposited are usually generated in sources based on Knudsen ***effusion ovens***

Xthe semiconductor to be evaporated is contained in a small crucible fabricated from an unreactive material (usually BN)

Xthe crucible is heated by power dissipation in a coil (usually Ta) carrying a current

Ba thermocouple provides feedback of temperature to a proportional controller

Xthe semiconductor effuses through a small orifice as a molecular beam

Bthe mean free path of the effusant is less than the diameter of the orifice

Xthe source has extensive radiative heat shielding to give good thermal efficiency and to avoid heating adjacent components in the apparatus

Bexcellent operational stability results in typically less than 1% drift over an 8 hour day

<For some materials to be deposited which are eg very reactive, have a high melting temperature and are needed in large quantities, ***electron beam evaporation sources*** are used

5(b) **Scanning Tunnelling Microscopy**

Electrons ***tunnelling*** between a sharp tip and a surface give a signal which allows ***3D images*** of the surface to be produced

- ***spectroscopy*** provides information about the ***electronic structure*** of the sample by probing the density of states as a function of energy

Basic instrument consists of a scanner and a sample-tip approach mechanism

- ***scanners*** are made of piezoelectric elements which expand upon application of an electric field
    - ° typical configurations are orthogonal bars or a cylindrical arrangement
    - ° computer-controlled voltage drive with feed-back stabilisation
- ***tip-approach*** controlled by differential springs or levers which have a movement step resolution of better than 3nm
    - ° piezo-elements also again used
- tips often formed from W wire by mechanical grinding or electrochemical etching
    - ° finest tips prepared by ion beam machining
    - ° less stiff, but oxide-free tips can be made from Au or Pt
- STMs can operate in air, but vacuum gives better characterised oxide-free surfaces
    - ° in UHV, semiconductors can be heated to >1000°C for *in situ* epitaxial growth studies

The mechanism of operation relies upon ***tip-surface electron tunnelling***, and this depends upon the electronic structure of the tip, that of the sample and the tunnelling barrier (related to the work-function of the sample) - two ***imaging modes***:

- '***constant current***' imaging where the tip is scanned with a constant separation from the surface atoms
    - ° maps constant charge-density contours
- '***constant height***' imaging where the changing current gives a surface image
- ***resolution***: approximately atomic in all directions

Tunnelling spectroscopy can be performed in two modes:

- '***point spectroscopy***' where tip is moved to a feature of interest and tunnelling current is recorded as a function of tip bias
    - ° magnitude of current at a specific voltage directly related to density of states in the sample at that energy
- '***current imaging spectroscopy***' where images of an area are collected for a number of tip biases
    - ° identifies the spatial position of energy states with respect to the lattice

6(a) **Stereographic Projection**

<Enables crystal planes and, for cubic system, directions to be plotted and conveniently related to one another in a ***projection plane***

<Projection is carried out by first constructing a sphere and inserting the ***projection plane*** as the horizontal diametrical plane

<Next, the crystal (cubic) is placed at the centre of the sphere and normals to its lattice planes are constructed from the centre outwards to intersect the sphere at particular points

<The latter points in the upper half of the sphere are then connected to the South Pole and where the resulting lines pass through the projection plane are the projected representations (***poles***) of the original crystal planes

<points on the lower half of the sphere can be similarly projected upwards to the North Pole

6(b) <***Overall symmetry of crystal***

Xon (001) projection, equivalent planes are separated by 90E rotations

Bfour-fold symmetry as expected for cube face

<***Arrangement of groups of planes***

Xon (001) projection, eg (102), (101) and (201) lie between (001) and (100): also eg (112), (111) and (221) lie between (001) and (110)

Beach such set of faces constitutes a ***zone***: definition - a set of planes whose mutual intersections are all parallel

Bthe common direction of the intersections in a particular zone is the ***zone axis***

<***Measurement of angles between planes***

Xuse a ***Wulff net*** calibrated in angle placed over the projection

Bshows small circles and great circles graduated in degrees

Xplace net so that the two poles of the planes lie on the same ***great circle***

Bmeasure the angle between the poles

6(c) **X-Ray Sources**

<In the laboratory, X-rays conveniently obtained by bombarding a metal target (anode) with electrons

Xevacuated tube with water-cooled metal anode

Brotating anode arrangement for very high intensity X-ray generation

XCu typically target material, giving CuK$\forall$ doublet with CuK$\forall_1$ wavelength approx 0.154nm

<the intense X-ray emission from an electron synchrotron may also be employed

Xto reduce beam divergence beam passed through lead collimator and then diffracted off accurately planar and highly polished single crystal surfaces

X-Ray Diffraction

<When X-rays (wavelength 8) scatter from crystals, they diffract from crystal planes as determined by ***Bragg's law***

Xfor planes {hkl} of spacing d_{hkl}

$$n8 = 2d_{hkl}\sin 2_B$$

Bthe Bragg angle (2_B) will typically be at least tens of degrees (cf electrons)

XX-rays detected typically using a proportional counter or scintillator/PMT, either situated behind a slit/collimator arrangement

(2 of the following four uses)

<***X-ray powder diffraction*** is used to identify the crystalline phase(s) in a powder sample

XX-ray powder diffraction plots obtained: intensity vs 22_B

Brelated to d_{hkl} values and then phase(s) identified using tables

examples for Si, ZnS (zinc blend) and ZnS (wurtzite)

<The ***crystallographic orientation*** of a single crystal surface can be determined

<***Lattice parameter determination*** can be carried out

<***Heteroepitaxial layer measurements*** can give the state of strain of a layer mismatched upon a substrate

X-Ray Topography

<The ***internal structure*** of semiconductors can be imaged using diffracted beams

X***Berg-Barrett topography*** (diagram required)

Buses a static surface Bragg reflection

Bsample mounted on goniometer and oriented to obtain suitable Bragg reflection from surface: photographic plate exposed using diffracted X-rays

X***Lang transmission topography*** (diagram required)

Bcamera synchronously scans the crystal and the photographic plate past a tall narrow beam of X-rays

X***Defect analysis***

Bdefects in a crystal can be imaged and analysed using topography

eg compare dislocations in LEC and Bridgman GaAs crystals

7(a) Preparation of Si starting material

- elemental Si is made from sand (silica or SiO_2) which is very abundant

°SiO_2 is first reduced to (impure) Si by heating with carbon

$$SiO_2 + C = Si + CO_2\uparrow$$

°the impure Si is then treated with hot HCl gas to covert it to trichlorosilane

$$Si + 3HCl = SiHCl_3 + H_2$$

°trichlorosilane is a liquid boiling at 32°C and is ***fractionally distilled*** to purify it: this continues until impurities are at the level of ppb

°the highly pure trichlorosilane is finally 'cracked' back to Si at high temperature with hydrogen

$$SiHCl_3 + H_2 = Si(\text{electronic grade}) + 3HCl$$

- the Si produced is ***highly pure*** but is a mass of tiny crystals

°must be converted to ***single crystal*** before can be used for all usual devices and ICs

The ***Czochralski*** (CZ) crystal 'pulling' technique

- small broken pieces of polycrystalline Si are first placed in a silica crucible
- the filled crucible then inserted into a vertical furnace, typically resistance-heated, inside an enclosure flushed with inert gas (argon) at low pressure (Fig required)
- the polycrystalline Si is melted and a small seed crystal with the desired orientation (usually (001)) is dipped into the centre of the melt

°as the temperature is slowly reduced and the seed withdrawn, ***a single crystal ingot solidifies onto the seed***

- in order to grow a uniformly shaped, defect-free ingot great expertise is needed

°critical parameters are seed and crucible rotation rates, temperature gradients, melt convective flow

°automatic diameter control is by monitoring position of meniscus around crystal

°this '***zero dislocation***' growth technology has been developed over many years

- ingots up to 300mm (1ft) diameter and of metres length now produced from >100kg melts
- principal contaminant in the Si ingot is ***oxygen*** which is produced during the growth as the melt attacks the silica crucible

°this oxygen (up to 100ppm) can introduce donors into the Si under certain heat treatments

must be allowed for in device processing

°but, the oxygen can be used later in gettering to remove other unwanted impurities

7(b) **Production of III-V Ingots (Gallium Arsenide, etc)**

<The ***Liquid Encapsulated Czochralski*** (LEC) technique

Xingots of these compound materials are produced by a modified Czochralski method

Bbut, standard method cannot be used due to high vapour pressure of Group V component

about 1 atmosphere of arsenic for gallium arsenide and about 35 atmospheres of phosphorus for gallium phosphide

Xit would be possible to balance the loss of the Group V component by applying these pressures of eg arsenic and phosphorus over the melt in a pressure vessel

Bhowever, quite dangerous to do this

Xin practice, a layer of ***molten boric oxide*** (B_2O_3) is floated across the top of the melt in the crucible (typically BN)

Bthis ***seals the melt*** against loss of Group V material

Xit is still necessary to carry out the procedure in a ***pressure vessel*** in order to apply a high pressure of gas to balance the Group V vapour pressure under the boric oxide

Bbut, this can now be an ***inert gas*** such as argon (**Fig**)

much safer!

Xdiameter control can be achieved by eg *in situ* radiography or by measurement of crucible weight change during ingot growth

Xthe technique can be used to grow crystals of a number of III-V compounds

Bcrystals of eg GaAs grown by this method contain ***significant dislocation densities*** due to stresses caused by the cool-down temperature gradients

GaAs crystals of max diameter 150mm (6in) currently grown