Exam Solutions Jan 2001

with examiners comments in italics

1. *Almost everyone had a go at this question. The answers were generally quite satisfactory*

a)Bookwork. *I got many good answers although some were inappropriately long. In one case I found I had given a student all the marks available with still 2 more pages of their answer left to read. Look at the number of marks available to judge how long I expect you to need to spend on a question. Time spent learning to produce short punchy answers that actually answer the question asked will not be wasted*
I expect students to produce a plot of cost per chip vs market volume showing how PLD,GA, Std Cell and full custom is each in turn cheapest as the market volume increases.
They will need to discuss the relative design costs (noting that FC is much more expensive), mask costs (noting the partial saving for GA and large saving for PLDs) and area costs (noting the area cost per chip increasing as FC, std cell, GA and PLD and explaining why)

(b) *This was generally done well. Lots of answers got 3 or 4 out of 4 for each section. Note there were only 4 marks for each section so essays 3 or 4 pages long for each were inappropriate. Those who did this got no extra marks but left themselves in time trouble elsewhere. I include a few extra comments based on misconceptions in some student answers*
This section seeks to find whether they understood the bookwork in section (a). The answers are not fixed and I will accept other solutions if they are well argued, but I expect:
(i) Integrating the logic onto a single chip will make it more difficult to copy, so this is a good idea. *The type of implementation makes little or no difference to the security level. Compared to a PCB any chip is almost impossible to copy.* Clearly the required performance is low (since it can be done by discreets) *Not many students spotted this* so any implementation could do the job. So the decision will simply depend on the size of the market. The number of commercial airliners produced per year cannot be large *(although apparently some students believe aircraft constitute a high volume market. They must be living on a different planet to me)* so we are probably looking at either PLDs or gate arrays. It is not possible to decide which without more detailed costings.

(ii) We have a monopoly for a short time so it is vital to release the product very quickly. *That way we make lots of profit whilst we have no competitors since we can charge what we like.* Small cost differences are unlikely to be important in this initial phase, since we are not competing with others on price. The low time to market might suggest PLD or (to a lesser extent) gate arrays. We do not have to wait several weeks for a full std cell process to be prototyped and checked unless absolutely necessary. PLDs look unlikely to be suitable since the project specifies both large amounts of circuitry and fairly high

speed, but we should check the numbers. Gate arrays will probably meet the logic volume and speed specification, but again this needs checking. *Note I did not say very high speed in the question. There is a reasonable chance that Gate arrays can do it. Although slower than Std Cell they are still pretty good* If not we will be forced to std cell. The most likely solution is gate array.
In the longer term, once we no longer have a monopoly, we may need to worry in more detail about cost. Then (since the market volume is "huge") it will probably be worthwhile moving to std cell (or if the market is big enough even full custom, but this is extremely unlikely).

(iii) The design is ready, the only requirement is to get it implemented quickly to get the factory working fast. Compared with the cost of factory down time, the chip cost is unlikely to be important, but the market volume is very low (essentially 1 chip) so std cell is not preferred. PLDs look unsuitable since we cannot afford "marginal" performance in a safety critical situation. Gate array is clearly the best option, it is the cheapest at acceptable performance and can be produced quickly.
Alternatively, we could try for a solution involving PLDs perhaps incorporating many in parallel to help the speed. If such a solution is possible, this is preferable to GAs even if the chip cost is higher, since factory down time is likely to be the governing financial factor

2. *Again almost every student did this question and the average was high*
(a) (i) *given that they had apparently prepared for it the answers were disappointing.*
Bookwork We assume each line is either fault free, stuck at logical 0 or stuck at logical 1 . It is necessary to make an assumption in order to carry out an analysis of the effect of various test cycles. *Most students did not tell me why it was necessary even though I specifically asked why*

(ii*) I thought this was a gift. Almost nobody got it right*
This is to illustrate that students understand the problems with just making the assumption above. This is the simplest circuit for which this is a meaningful question

with three lines there are 27 different possible fault states

ff=fault free 0=stuck at logical zero 1=stuck at logical 1

line A	line B	line z
ff	ff	ff
ff	ff	0
ff	ff	1
ff	0	ff
ff	0	0
ff	0	1
ff	1	ff
ff	1	0

ff	1	1
0	ff	ff
0	ff	0
0	ff	1
0	0	ff
		0
		1
0	1	ff
		0
		1
1	ff	ff
		0
		1
1	0	ff
		0
		1
1	1	ff
		0
		1

note that this includes the state where the circuit works correctly.

(iii) *This was a lot better*
This is a lot of states to analyse so in practice we reduce the number to be considered by assuming that the circuit can only have zero or one fault. There is the possibility that the circuit will have more than one fault, but we assume a set of test vectors that will find a single fault would also find a combination. In principle this is not necessarily true since a group of faults might "cancel" for a particular set of tests but effect normal operation. However, this is a low risk and one we are forced to accept.

line A	line B	line Z
ff	ff	ff
ff	ff	0
ff	ff	1
ff	0	ff
ff	1	ff
0	ff	ff
1	ff	ff

(iv) If we do not make the single fault assumption there are 3^N fault states. If we do there are 2N+1.

(b)
The restricted fault matrix looks like this calculating the output at F and G in turn

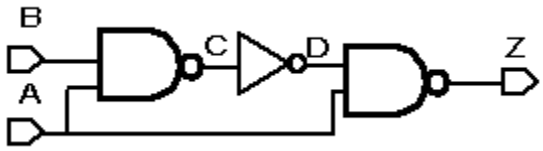
	ff	A0	A1	B0	B1	C0	C1	D0	D1	E0	E1	F0	F1	G0	G1

000	01	01	01	01	01	01	01	01	01	01	01	01	11	00	01
111	10	00	10	01	10	11	10	10	00	10	00	00			11
		Y	N	Y	N	Y	N	N	Y	N	Y	Y	Y	Y	Y

So we fail to detect,
A stuck at 1
B 1
C 1
D 0
E 0

A lot of 10/10 answers but I was surprised how many had no idea. Quite a few did all the working then didn't actually bother to tell me the answer. I asked which faults we fail to detect. I need to know that you understand the matrix well enough to extract that information. If you don't show me, how will I know?

3. *An unpopular question Clearly those who did it found it hard*
(a) This should be fairly easy for students who have understood the physical layout of a chips. The circuit actually looks like:



Apparently it wasn't "fairly easy" because only a few got this right. The rest were in real trouble for the rest of the question.
(b) To answer this question students need 2 things. They need to realise that only energy is dissipated when a capacitance charges or discharges, so they need to work out which of the capacitances are relevant. They then need to realise that they can calculate values for these capacitances simply by looking at the structure in figure 3.
This is fairly straightforward, but in lectures we have only dealt with calculating the power dissipation for a fixed switching frequency rather than specifically looking at which lines switch. So I only expect students with a reasonable understanding of the physics to progress with this question.
Many had a rough idea on this , but no one took it through to the right answer
So first, let's work out the values on all the lines and how they change as a result of the switching events:

event	A	B	C	D	Z
00 (start)	0	0	1	0	1
01	0	1	1	0	1
10	1	0	1	0	1

The question has been designed so that most of the capacitances are now seen to be irrelevant since they do no switch. So the only capacitances that matter are those associated with the input lines A and B.

Each switching events dissipates power ½ CV^2. So we just need to work out the capacitances for lines A and B. The areas of these lines can just be measured directly from the figure and then used with table 3 to get capacitance.
The area of A is 73μm^2 and that of B 32μm^2 in both cases just of polySi. However, I will not punish students for inaccurate measurement provided it is clear that they measured the right things.
A undergoes 1 switching event so the associated energy is ½ CA V2 = ½ 73 5E-16 5 5 = 4.6e-13J
B undergoes 2 switching events so the energy is 2 ½ CB V2 = 32 5E-16 5 5 =4e-13

therefore total energy is 8.6e-13J

(c) This has not directly been covered in the course but for the best students, should be a logical extension of what has been covered. Since dynamic power dissipation is controlled by the number of times each line switches, any extra switching due to glitches causes an increase in the power consumption. *About half realised this. Some thought the glitch would turn on both the p and n groups. I couldn't see their logic that led to this*

4.
This is a deviation from a fairly standard derivation in the course.
Both devices are in saturation so Idsn=-Idsp. Noting that Vgs for the n-type is Vinv and for the p type Vinv-Vdd, we can quickly write.

$$\frac{\beta_n}{\beta_p} = \left(\frac{V_{gs} - V_{tn}}{V_{gs} - V_{tp}}\right)^2 = \left(\frac{V_{inv} - 4}{V_{inv} - 1}\right)^2 = 3$$

simple rearrangement leads to

$V_{inv} = \frac{4 - \sqrt{3}}{1 - \sqrt{3}}$ the value for root 3 that gives physically meaningful results is-1.73 (hence the hint in the question). Thus Vinv=2.1V
Many student drove the answer this far
(b) Consider first the n-type transistor. Vin <Vinv, so Vout >Vinv
Thus Vgs-Vt=1V, Vout=Vds >2.1 i.e. Vds>Vgs-Vt so this must be in the saturation region.
For the p-type Vgs-Vt =Vin-Vdd-Vt=2-5+1=-2, Vds=Vout-Vdd<Vinv-5 . But we only know Vds is somewhere between -2.9 and 0 so the answer is not clear. However, we know that Vgs for the n-type device is less than Vinv so the current must be less than that at inversion. For the p-type device |Vgs|>|Vinv| so if it is still in the saturation region its current must be greater. But the magnitude of these currents is the same. The only way the current through the p can reduce if |Vgs| increases is if it goes into the linear region. So p must be in the linear region

Most students found the above argument beyond them. However, a fair number just asserted the answer so they didn't get many marks but were at least able to proceed to the next section

(c) This is entirely new to the students so I expect them to find it hard. However, it is actually quite straightforward, just a deviation from part (a). The numbers have been chosen so that the quadratic drops out easily at the end.

Quite a few students started this correctly but only one drove the arithmetic through to the right answer.

We know Idsn=Idsp and from part (b) we know the n is in saturation and the p in the linear region.
So

$$\frac{\beta_n}{2}\left(V_{gs}-V_{tn}\right)^2=\beta_p\left[\left(V_{gs}-V_{tp}\right)V_{ds}-\frac{V_{ds}^2}{2}\right]$$

$$\frac{\beta_n}{\beta_p}=3=2\left[\left(2-5+1\right)\left(V_{out}-5\right)-\frac{\left(V_{out}-5\right)^2}{2}\right]/(2-1)^2$$

$$3=-4V_{out}+20-V_{out}^2+10V_{out}-25$$

$$0=6V_{out}-8-V_{out}^2$$

Thus Vout =2 or 4 V. Since Vout must be > Vinv Vout=4V