Data Provided: None

EEE310

The University of Sheffield

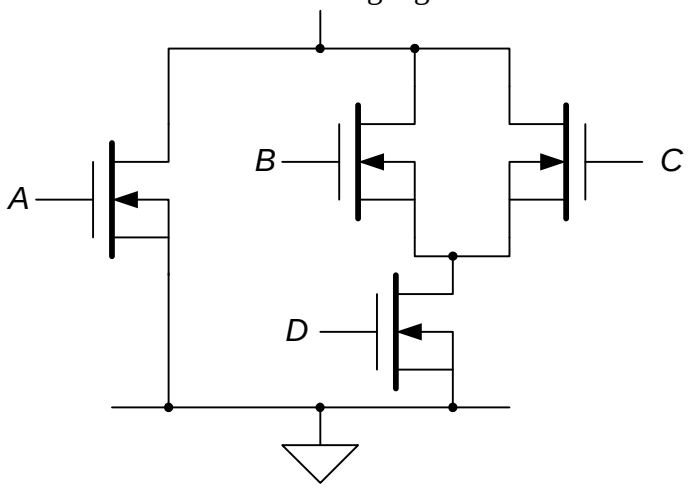
DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2002-2003 (2 hours)

Introduction to VLSI

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. The pull-down network for a CMOS logic gate is:



i) Draw the corresponding pull-up network. **(4)**
ii) Determine the logical function of the logic gate. **(4)**
iii) Size the transistors for a minimum-sized gate. **(4)**

The output of this gate must drive a load capacitance of 140fF. Show how this would be done to minimise the overall delay. **(8)**

(m_E=0.08m^2/Vs, m_H=0.04m^2/Vs, t_{OX}=10nm, W_{min}=1mm, L_{min}=0.25mm, e=3.45x10^{-11}F/m, V_{DD}=3.3V, V_{TN}=-V_{TP}=0.6V)

2. You have to make a decision about how to implement a system with a digital part and an analogue part Your market studies indicate that you might expect to sell 200,000 of these systems.

You have two options:

a) separate digital and analogue ICs. You will need to design the digital part yourself but you find that there is a standard analogue part that will meet your specification at a cost of $4 in large volume quantities.
b) A mixed-signal ASIC containing an analogue sub-system.

Identify the arguments and issues that might affect the decision. **(8)**

You estimate that the basic cost of each packaged digital part in option a), in the quantity that you require, will be $3 and the overall yield will be 70%. You estimate that the basic cost of the mixed signal device in option b) will be $5 but the overall yield will be 65%. The design of the digital part will consume about 6 person months and the mixed-signal device about 9 person months. On the basis of this limited information, which option would you choose. Give reasons to support your answer. **(12)**

3. Derive expressions for the small-signal impedance of a (switched on) pass transistor for the cases where the input voltage equals 0V and V_{DD}. **(6)**

What are the problems associated with using such a pass transistor as a switch and how they are overcome in a transmission gate. **(2)**

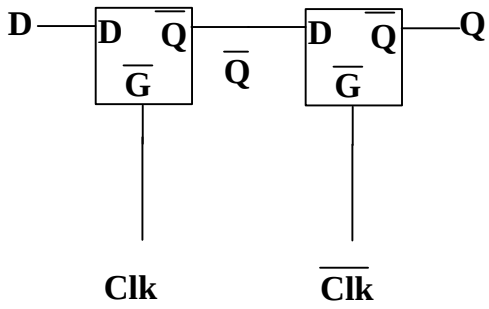
Draw the transistor-level schematic of a multiplexer, based on transmission gates, to form a 4-input, 1-output multiplexer. **(4)**

Using 2-input, 1-output multiplexers and inverters as basic building blocks, construct the following logic gates:

i) A ANDB
ii) A XOR B
iii) A OR B
iv) NOT A (using only a multiplexer) **(8)**

4. Draw a circuit to generate two complementary clock signals that overlap in the high state but are never low at the same time. Show how this circuit can be made to drive a large capacitive load. **(6)**

With reference to the following master-slave flip flop



Show how this sort of circuit behaves as an edge-triggered flip-flop and why clocks that overlap in the low state might cause a problem. **(6)**

More generally, describe how the *synchronous design methodology* for designing digital circuits operates, the requirements that it places on the generation of clocks and the organisation of circuits (e.g. what is allowed and what is not allowed). **(6)**

What is the role of *design for testability* in this methodology. **(2)**