

Bookwork + Understanding

Q1. a) i) 20% of the devices failed at electric fields below 10 MV/cm . Most dielectrics (for example SiO_2 and Si_3N_4) have breakdown fields $\sim 10 \text{ MV/cm}$. Therefore these devices break down prematurely indicating that these are infant failures due to defects, (or poor design, poor manufacturing control, inadequate quality control, incorrect fabrication procedures). A further evidence is the value of $\beta = 0.5$ in the Weibull model which represents infant failures.

ii) Bookwork

- (Any 2) - Use of novel materials such as multilayer dielectrics to reduce pin hole defects.
- Minimise antenna effects during fabrication process such as during dry etching and ion implantation.
 - Control oxidation process to reduce generation of traps. Minimise thermal stress to reduce trap density.
 - Careful addition of atoms to passivate the interfaces.

b) i) Understanding + Calculation

The gradient, β can be estimated from the graph.

$$F(t) = 1 - \exp\left(-\left(\frac{t}{\alpha}\right)^\beta\right)$$

Rearranging gives $\ln[-\ln(1-F(t))] = \beta \ln(t) - \beta \ln(\alpha)$.

$$\beta = \frac{\ln[-\ln(1-F(t_2))] - \ln[-\ln(1-F(t_1))]}{\ln(t_2) - \ln(t_1)}$$

$$\begin{aligned} \textcircled{2} & \sim \frac{0.5 - (-1)}{8.0 - 5.0} \\ & \sim 0.5 \end{aligned}$$

21. b) ii) $F(t) = 0.6$, $\ln(-\ln(1-0.6)) = -0.09$

From the graph $\ln(t) = 6.75$
 $t \sim 854$ hours. (2)

iii) Failure rate $= \lambda(t) = \frac{\beta t^{\beta-1}}{\alpha^\beta}$

let $F(t) = 0.63$

$\ln(-\ln(1-0.63)) = \ln(-\ln(0.37)) \sim -5.8 \times 10^{-3}$
 $\sim 0.$

therefore $\ln(t) = 6.8$ (when $F(t) = 0.63$) (2)
 $\alpha = t = 898$ hours. goes to part b(i).

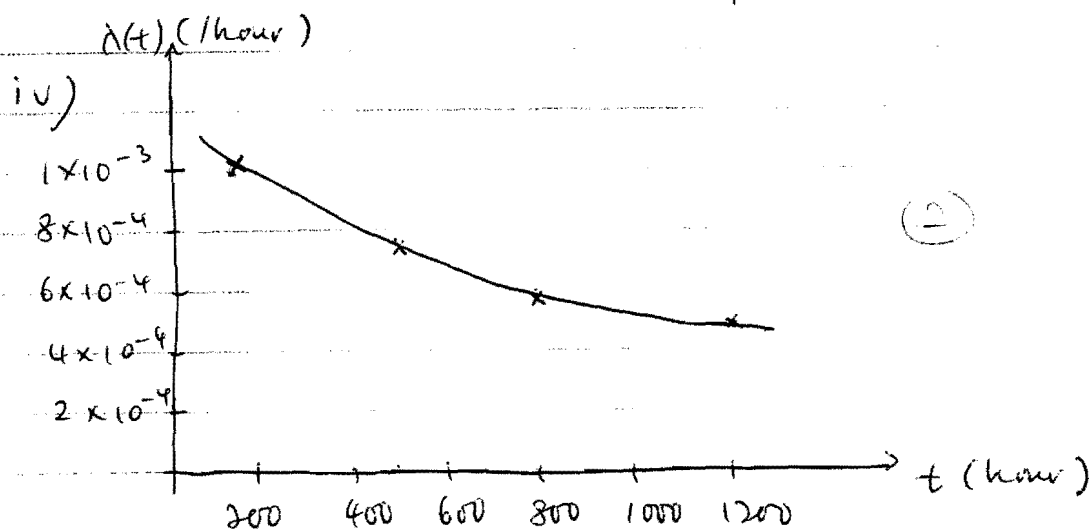
$\lambda(t) = \frac{0.5t^{-0.5}}{898^{0.5}} \sim \frac{0.5t^{-0.5}}{30} \sim \frac{1}{60\sqrt{t}}$

$t = 150$ $\lambda(150) = 1.036 \times 10^{-3}$ /hour

$t = 500$ $\lambda(500) = 7.45 \times 10^{-4}$ /hour (4)

$t = 800$ $\lambda(800) = 5.89 \times 10^{-4}$ /hour

$t = 1200$ $\lambda(1200) = 4.81 \times 10^{-4}$ /hour



Infant failure could be due to insufficient oxide thickness. Other suggestions related to failure in MOSFETs during infant stage are also acceptable.

Q2. a) Bookwork

At high temperature, Si atoms diffuse along the grain boundaries of Al film to create voids. Al atoms counter-diffuse into Si, filling the Si depleted regions. However due to low solubility of Al in Si, Al precipitates in the form of conducting filaments that can either produce a short circuit at the junction or leads to very high electric fields at the tip of the filaments that cause premature breakdown.

b) i) 1.7 wt% of Si is added to minimise the Al-Si interdiffusion while 4wt% of Cu is added to increase the activation energy of the metal to reduce electromigration.

Understanding

ii) See attached lognormal graph.

iii) From the graph, 80% of Al interconnects fail by ~110 hours
" " " " Al-Cu-Si " " " ~8500 hours

iv) Addition of 4wt% Cu will increase the interconnect resistance. Galvanic corrosion can also occur in the presence of moisture since Cu and Al have different potentials in the electrochemical series.

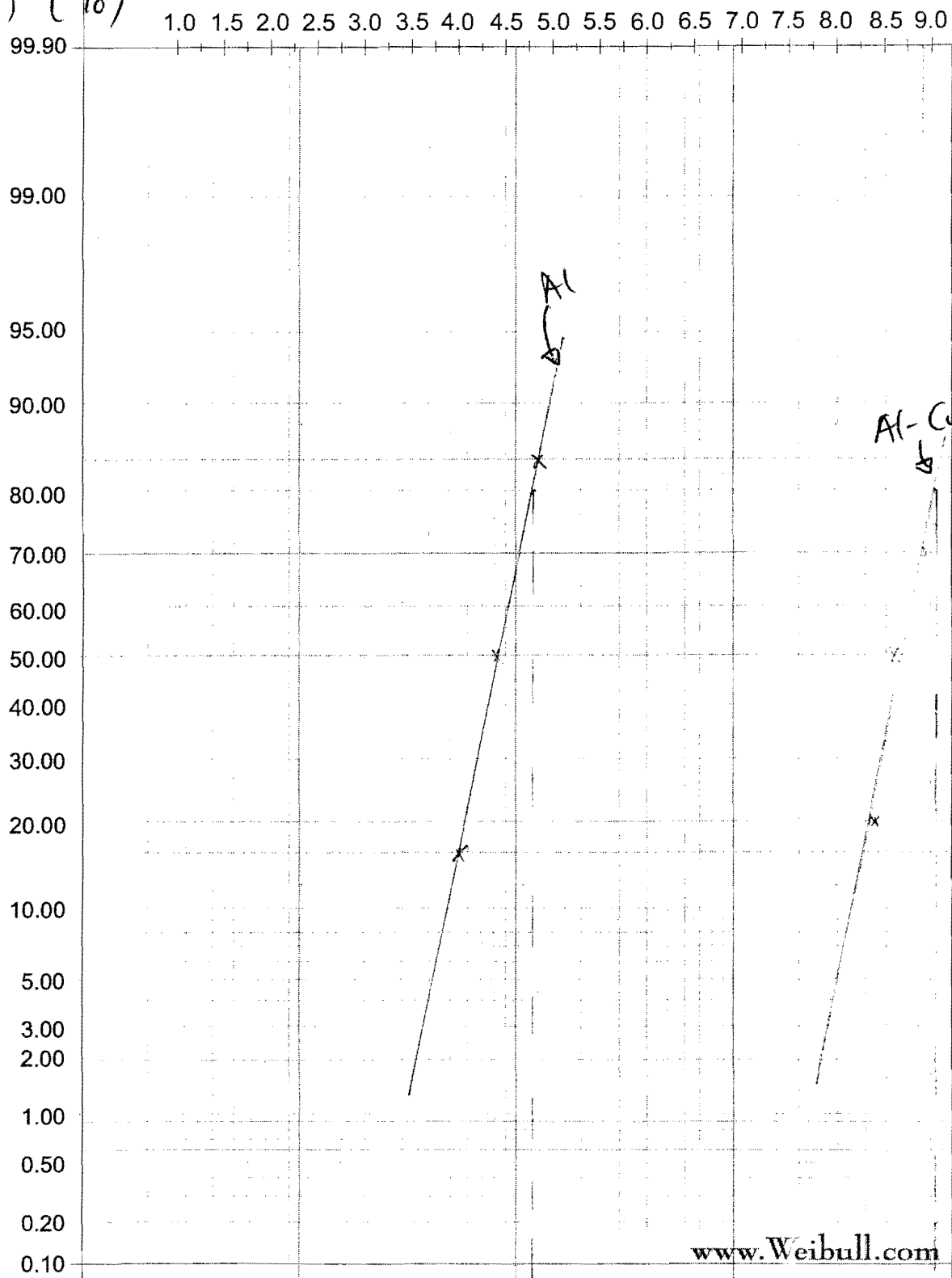
c) Bookwork (Any 4)

- Use short conductors so that the back-flow of atoms counters the electron-wind due to high current density.
- Use single crystal metal with no grain boundaries to reduce atom migration.
- Use conductive with ~~perpendicular~~ grain boundaries normal to the current flow, known as bamboo structure.

Q2 c) - Use multilayer metals with refractory metals such as Ti, W, TiN etc.

- Limit the current density on the conductor
- Addition of Cu and Si to increase the activation energy.

$F(t) (\%)$



www.Weibull.com

4 Cycle Lognormal Probability Plotting Paper Created Using ReliaSoft's Weibull++ www.ReliaSoft.com 1-888-896-0410 ©1999 ReliaSoft Corporation

$t(\text{hour})$

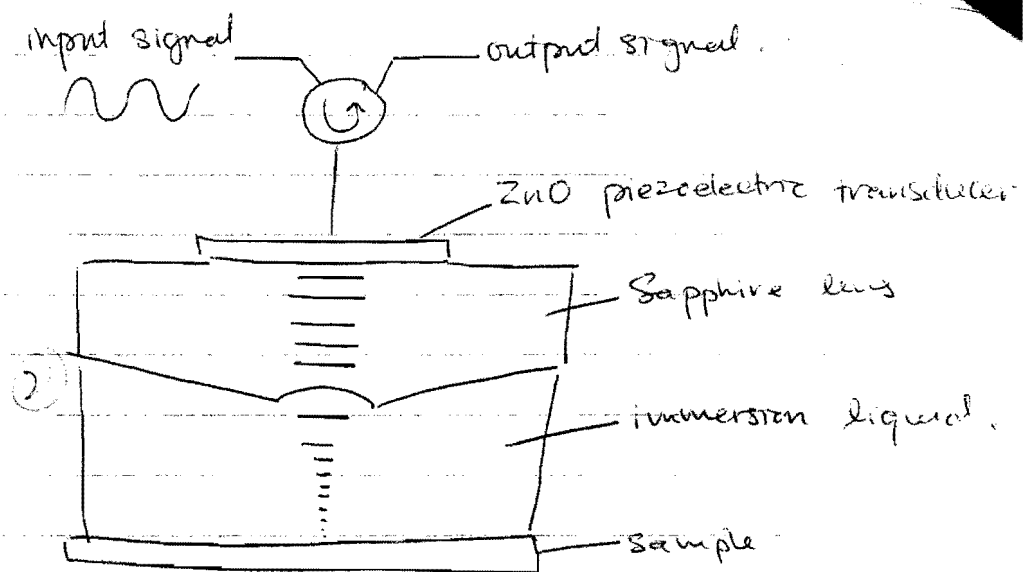
Q3 c) i) Scanning electron microscope operated in the energy dispersive (EDX) mode can be used to study these contaminants. The beam position ~~is~~ is ^{swept} ~~changed~~ from the emitter to the collector and the intensity of signal from Cu is recorded.

In the EDX mode the electron beam produced secondary electrons that are promoted to high energy levels. As they transfer from high to low energy levels x-ray unique to the atom will be emitted. The x-rays are captured by Si(Li) diode and converted into pulse height spectrum.

ii) Resolution is limited to $\sim 1\mu\text{m}$ and analysis is more suitable for atoms with Z number > 11 (mostly metals).

ii) Cu can lead to increased generation-recombination ~~center~~ sites, leading to increased leakage current. Other reliability issues include formation of precipitates due to low solubility in Si, formation of nuclei leading to generation of dislocation.

Q3 a) Bookwork



At the input, an electrical oscillation is transformed into acoustic wave by the ZnO piezoelectric transducer. The acoustic wave is coupled into a rod lens (usually sapphire) and focused onto the sample. Focusing is achieved by the spherical interface between the sapphire and the immersion liquid. The acoustic wave reflected from the surface of the sample will be converted back to electrical signal by the ZnO transducer. By performing a raster scan, an image of the sample can be constructed.

b) i) In general low frequency acoustic waves provide greater penetration depth but poor lateral resolution:
For example at 50 MHz, the penetration depth is $\sim 5 \text{ mm}$ but the spatial resolution is $\sim 25 - 100 \text{ } \mu\text{m}$. At higher frequencies, the penetration depth is reduced but improved resolution is achieved. At 2 GHz the resolution is $\sim 1 \text{ } \mu\text{m}$ and the penetration depth is a few microns.

ii) The low frequency waves are used to image coarse defects such as cracks in encapsulated IC and die delamination.
High frequencies are used to analyse IC dimensions, cracks in Si wafers and voids in dielectrics.

Q4 a) Background.

High energy particles can cause degradation to MOSFETs by inducing lattice damage. The particles cause physical displacement of atoms from their original sites, leading to generation of interstitial defects and vacancies. The high energy particles can also generate electron-hole pairs in the gate oxide and in Si. The former leads to charge trapping in the oxide that changes the threshold voltage and transconductance while the latter causes an increase in the leakage current.

In GaAs MESFETs there is no gate oxide. Therefore charge trapping is not an issue. However the high energy particles will cause lattice damage and increased leakage currents. Trap levels could also be introduced and mobility is reduced. Degradation of transconductance is therefore observed.

- b) i) SEU refers to errors in digital electronics that are not caused by permanent damage to the circuits and can be removed during reinitialization.
- ii) The smaller MTTE is due to significantly higher level of radiation from cosmic ray at the higher altitude at White Mountain.
- iii) When the device dimensions are reduced, the electric field in the pn junction increases. Upon interaction with the high energy particles such as alpha particles, a large number of electron-hole pairs can be generated. The alpha particles can also cause electric field modifications that resulted in more electrons being injected into the depletion region. ~~These additional charges can cause~~ These additional charges can cause SEU events. The critical charge Q_c was found to be

$Q_c \propto l^2$ where l is the feature dimension.

c) Nuclear particles from radioactive atoms such as U^{238} and Th^{232} can generate alpha particles. These atoms can be found in metals used in devices and alumina and lead frame used in dummy packaging.

② Nuclear particles from cosmic rays can also ~~produce~~ produce significant high energy particles, particularly at high altitudes and in space applications.

d) Examples of method to reduce soft errors are

- Use radiation hardened gate oxides and silicon-on-insulator
- use higher channel doping and flat doping profile
- use dielectrics with higher dielectric constants ~~ability~~ to increase Q_c
- modify the fields to delay arrival of excess charges to the circuit nodes.