**Self Assessment Questions (SAQs) 2**

- Briefly can you describe what the main stages in fabrication of semiconductor devices?

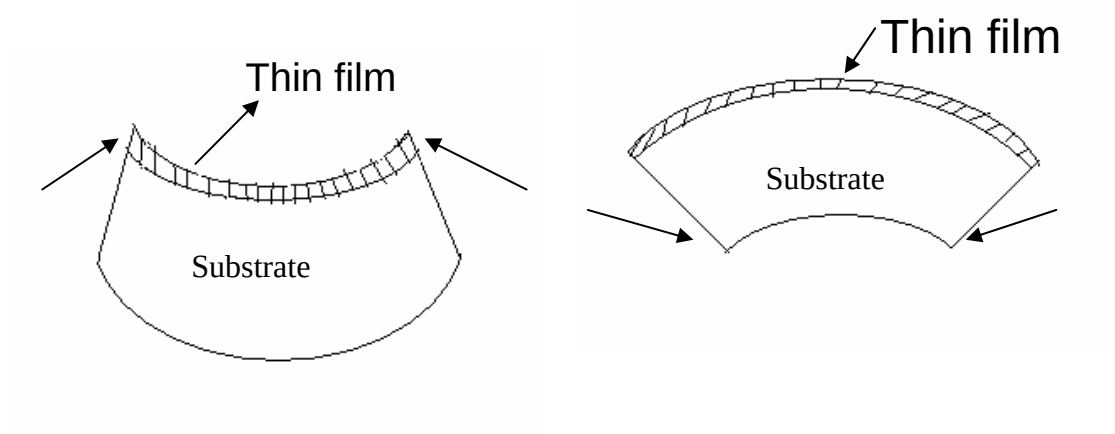
Typical planar Si pn junction fabrication stages are

1) Wafer cleaning
2) Photolithography, steps include baking, photoresist spinning, UV exposure and development to strip off photoresist.
3) Doping process using either thermal diffusion or ion implantation.
4) Metal evaporation to form contact using filament evaporator, e-beam evaporator or sputterer.
5) Second photolithography is used to etch off unwanted metal.
6) Annealing to improve contact.

- Can you think of disadvantages associated with different metal film deposition techniques?

Here are some of the disadvantages.
Filament evaporation: Poor step coverage, poorer thickness uniformity control. Contaminants from filament and chamber can be incorporated into metals.
Electron beam evaporation: X-ray radiation generated by the electron beam can cause radiation damage to Si wafers.
Sputerring system: Ar+ ions can be incorporated into the metal film deposited. Ar+ bombardment can also induce surface damage in some materials. Heat removal from substrate is necessary as the energetic target atoms transfer energy to the substrate in the form of heat.

- Explain the origin of tensile and compressive stress in film/substrate structure.




Film under residual tensile stress  Film under residual compressive stress

ii) If $\alpha_f > \alpha_s$

$\alpha_f$ = Coefficient of thermal expansion of film

$\alpha_s$ = Coefficient of thermal expansion of substrate

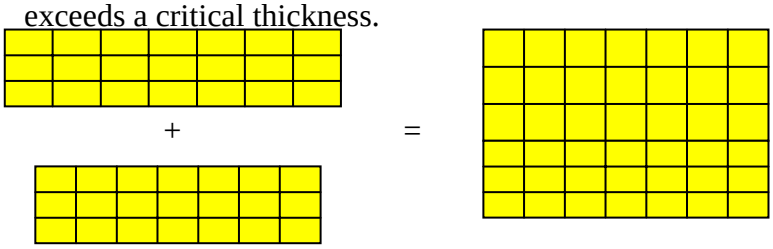
Assume that film is stress free when deposited at a temperature T. When film cools to room temperature $T_o$, it contracts more than the substrate. In order to achieve mechanical equilibrium, the film stretches while the substrate contracts by equal amount to keep the overall length same in each. The

film/substrate pair also needs to bend the substrate concave upward due to the tensile stress.

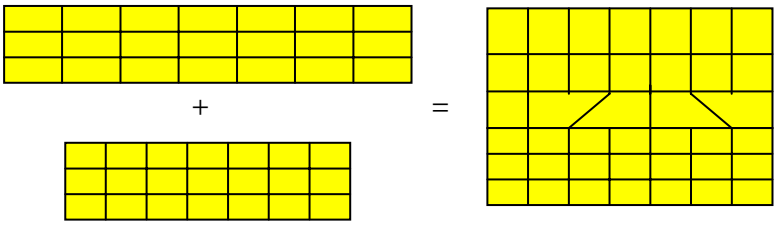
In analogous fashion compressive stress causes the substrate to bow (convex downward)

- Describe how dislocation and stacking faults are generated in heteroepitaxy.

Dislocation and stacking faults is mainly generated by stress originating from lattice mismatch between the different materials having different lattice constants in the heteroepitaxy. The bond strain energy increases with the film thickness and will relax by generating dislocations and stacking faults when the film thickness exceeds a critical thickness.




Defect free when mismatch is small



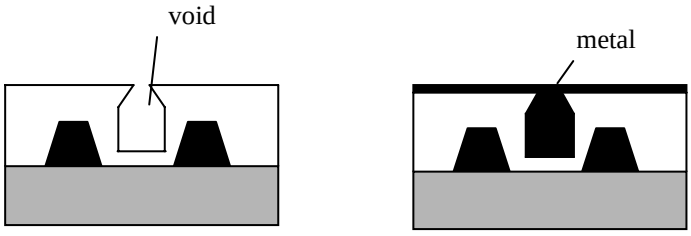

Strain is relaxed by generating dislocation or stacking faults at interface when mismatch is large

- What are the potential reliability and failure issues generated by hillocks and whiskers?

Short circuit between conductors is the main failure mechanism generated by hillocks and whiskers. In particular the length of whisker can increase with time increasing the potential of shorting conductors. They can also initiate cracks in dielectric and increase the risk of corrosion related failures.

- Explain the reasons for poor metal coverage and dielectric coverage in IC fabrication. What are the consequences of these limitations?

ICs usually consist of various trenches, mesas and stripes. It is difficult to achieve uniform metal and dielectric thickness particularly at the vertical sidewalls. Consequently the metal is usually thinner at the sidewalls causing increase in resistance and increased current density (this can promote electromigration if it is sufficiently high). Open circuit can occur if the trenches are deep. Poor dielectric coverage can lead to formation of void that is subsequently filled with metal as illustrated below. This can cause potential dielectric breakdown and short between conductors.



- Provide examples of defects or contaminants that can be introduced in each of the following stages in fabrication: 1) Photolithography 2) Chemical vapour deposition 3) Plasma processing and 4) Ion implantation.

  Lithography
  - Defective mask, e.g., scratches, cracks.
  - Leftover chemicals or photoresists.
  - Clean room residues.
  - Dust, water marks on mask.
  - Contamination from photoresists/ etchants (if wet etching used).

  Chemical Vapour Deposition
  - Thin film deposits deposited onto wafer.
  - Oxidation and flaking of heaters.
  - Impurities from precursor gases
  - Particulars from gas-phase environment
  - Poor adhesion dielectrics
  - Roughened film topologies

  Plasma processing
  - Build up of charge produced by plasma that leads to large current flowing through the dielectric causing wearout damage.
  - Build up of charge leads to charge trapping.
  - Film adhesion damage due to photon and chemical attacks.
  - Damage to surface of semiconductor.

  Ion Implantation
  - Contamination due to ion species, Fe, Ni, Cr and Mo.
  - Ion-beam-sputtered atoms from photoresists, vacuum hardware,
  - Wrong ion may be implanted. Selection of ion species is based on m/q variations.
  - Variation in the depth implantations leading to junction depth variations.