The University Of Sheffield.

Electronic & Electrical Engineering.

EEE336 DIGITAL DESIGN

Credits: 10

Course Description including Aims

The aim of this module is to provide students with a fundamental understanding of synchronous digital systems. This is done in conjunction with the Verilog Hardware Description Language (HDL) and particular emphasis is placed on the architecture and organisation of a basic microprocessor.

1. To introduce the Verilog HDL and gain a working knowledge of its application to the modeling, simulation and synthesis of digital systems.
2. To develop a solid understanding of synchronous digital systems with an awareness of performance limitations and implementation issues.
3. To obtain detailed knowledge of the architecture and organisation of a basic microprocessor and its peripheral interfaces.

Outline Syllabus

Verilog HDL: syntax, simulation, synthesis, digital building blocks, finite state machines. **Microprocessors:** Instruction Set Architecture (ISA), functional behaviour, internal organisation. **Peripherals:** memory hierarchy, memory cycles, Direct Memory Access (DMA). **Operations:** arithmetic, floating point representation, addressing modes, stacks, interrupts. **Processor Architecture:** ALU, registers, data path design, RISC, CISC. **Processor Control:** Hardwired, microprogrammed. **Microcontrollers & DSP:** Architecture, practical examples.

Time Allocation

24 lectures, 12 problem classes, 64 hours guided independent study.

Recommended Previous Courses

EEE119, EEE225.

Assessment

2 hour examination, answer 3 questions out of 4

Recommended Books

Mano & Kime	Logic and Computer Design Fundamentals, 4/E	Prentice-Hall
Gajski, D D	Principles of Digital Design	Prentice-Hall
Ciletti, M D	Advanced Digital Design with the Verilog HDL 2/E	Prentice-Hall
Floyd, T L	Digital Fundamentals	Prentice-Hall

Objectives

On completion of this module successful students will be able to

1. Analyse a synchronous digital system described schematically or in Verilog.
2. Design a small synchronous digital system.
3. Be aware of implementation issues and factors that limit performance.
4. Understand and explain the basic structure and operation of a digital computer.
5. Identify and describe the functional requirements of a (micro) processor and peripherals.
6. Understand and explain the internal organisation of different types of processors.

Detailed Syllabus

lecture	topic
1	**Verilog:** Concepts, hierarchy, structure, behavior
2	**Verilog:** Types, syntax, synthesisable subset
3	**Verilog:** Event driven simulation, test benches
4	**Verilog:** Fundamental digital building blocks
5	**Verilog:** Register Transfer Level (RTL)design, Finite State Machines (FSM)
6	**Implementation**: ASIC, FPGA architectures, design methodology
7	**Computer Arithmetic:** Data representation, addition, subtraction
8	**Computer Arithmetic:** Serial & Parallel multiplication, Booth's algorithm
9	**Computer Arithmetic:** Restoring and non-restoring division algorithms
10	**Computer Arithmetic:** Floating point unit
11	**Memory:** Classification and organisation, SRAM, DRAM, performance
12	**Microprocessor:** Instruction Set Architecture (ISA)
13	**Microprocessor:** Datapath elements
14	**Microprocessor:** Control, microcoding
15	**Microprocessor:** Pipelining and performance
16	**Microprocessor:** Stack architectures
17	**Microprocessor:** Interrupts
18	**Microprocessor:** Direct Memory Access (DMA)
19	**Microprocessor:** Architectural alternatives, RISC, CISC
20	**Microcontroller:** Architectures, peripherals
21	**Digital Signal Processor:** Architecture, practical example using convolution
22	**Direct Digital Synthesis (DDS):** Look up tables
23	**Review Lecture 1**
24	**Review Lecture 2**

EEE336 UK-SPEC/IET Learning Outcomes

Outcome Code	Supporting Statement
SM2m/SM2p	Data representation is covered including number systems and codes. Integer and floating point numbers are examined. Algorithms for computer arithmetic and digital signal processing are developed. Boolean algebra is used throughout to analyse and design digital components
SM5m	Algorithms for multiplication and division are examined. Hardware solutions are developed and trade-offs considered. Floating point arithmetic is examined and limitations considered. Verilog models of digital functional blocks are developed. The relationship between the constructs used in the Verilog model and the synthesised circuit are examined. Implementation of mathematical functions using look up tables is examined.
EA1m/EA1p	Design flow and methodology for digital systems, using a hardware description language, is examined. Principles for the correct use of Verilog for synthesis are established. Synchronous design techniques are encouraged throughout. Simulation using Verilog models is examined in detail.
EA2m/EA2p	Circuit performance is examined (speed/area/power). Algorithms for computer arithmetic are developed and analysed to investigate performance. Alternative microprocessor architectures are considered and compared for performance.
EA4m/EA4p	A top down approach is applied to the examination of computer architectures. Lower level components are developed and integrated to form a microprocessor.
D4p/D4m	Advances in computer architectures and arithmetic have involved creativity to overcome problems. This is highlighted throughout the course.
EP2p/EP2m	Electronic Design Automation (EDA) tools: Verilog modelling, simulation and synthesis are examined in detail. FPGAs are considered for implementation.
EP4p/EP4m	Use of data sheets for memory and microprocessors. Review of instruction set for microprocessor.