The University Of Sheffield.

Electronic & Electrical Engineering.

EEE335 INTEGRATED ELECTRONICS

Credits: 10

Course Description including Aims

This course aims to describe the generic circuit elements, analogue and digital and their associated properties which are typically used within IC circuits. Additionally, this course aims to bring the student to level of understanding of VLSI design, such that they can:

1. Understand the alternatives available to and constraints that act upon a VLSI designer.
2. Understand the underlying technologies, trends, and critical issues that affect and will affect VLSI design.
3. Design and analyse analogue and digital circuits (and understand the limitations)

Outline Syllabus

Introduction: Technology development: historical perspective, trends, and future problems and issues. **Economics and Design Styles:** Economics of chip production. Economics of chip design. **Implementation options**: Full custom; cell based, Gate Arrays, FPGAs and Programmable Logic Devices. **Synchronous Design**: Methodology. Clocks and clocking. **Logic design**: CMOS technology and characteristics. Noise margins. Gate design/sizing. Switching speed. **Analogue circuit structures**: Circuit operating characteristics of BJTs and MOSFETs; single transistor circuit elements; two transistor circuit elements; differential amplifiers; current mirrors and output stages. **Analogue VLSI design**: CMOS operational amplifier.

Time Allocation

24 lectures plus 12 hours of additional support material.

Recommended Previous Courses

Some previous knowledge of MOSFET operation is assumed, EEE118 Electronic Devices and Circuits would be appropriate. A familiarity with digital circuit design is essential, EEE117 Digital System Engineering provides a suitable background.

Assessment

3-out-of 4 question, 2 Hour Examination

Recommended Books

Weste N & Eshragian K	*Principles of CMOS VLSI Design A Systems Perspective*	Addison Wesley
	Technology Roadmap for Semiconductors 2001	http://public.itrs.net
Uyemura J P	*Introduction to VLSI Circuits and Systems*	Wiley
Rabaey J	*Digital Integrated Circuits - A Design Perspective*	Prentice Hall
Geiger R L, Allen P E & Strader N R	*VLSI Design Techniques for Analog and Digital Circuits.*	McGraw Hill

Gray P R, Hurst P J, Lewis S H, Meyer R J	*Analysis and Design of Analogue Integrated Circuits*	Wiley
Sedra, A and Smith, K	*Microelectronic circuits*	OUP

Objectives

By the end of this unit successful students will be able to:

1. Demonstrate an understanding of the costs, options, technological difficulties, behaviour of, and benefits of VLSI for particular applications;
2. Calculate the costs (to a first order) of a VLSI design;
3. Use the appropriate terminology associated with VLSI;
4. Outline the VLSI design process and the methodologies used in system implementation;
5. Design simple logic gates based on an understanding of the required logic and the behaviour of the technology. Students should also be able to estimate the performance of these gates (power, speed, area).
6. Design simple analogue IC structures to achieve particular goals.
7. Identify those parts of a circuit that play a major role in limiting the frequency response and write down and use the high frequency equivalent circuit of a circuit to calculate high frequency behaviour.
7. Understand design issues relate to VLSI operational amplifiers and analyze analogue circuits for CMOS operational amplifiers.

Detailed Syllabus

1. Introduction and historical background to VLSI.
2. Trends in VLSI and future problems/issues - the SIA Roadmap.
3. Design routes - Gate Array, Standard Cell, Full Custom, FPGA and PLD.

4-5. Economic constraints and costs

6. Outline of design process and the role of simulation.
7. Introduction to CMOS technology.

8-9. Performance of simple gates - CMOS inverter, Transmission Gate. A simple RC model.

10. Gate design and sizing.
11. Switching speed of more complex gates.
12. Synchronous design. Clocks and clocking. Metastability.
13. Review of the operating characteristics and small signal models of BJTs and MOSFETs. The Miller transformation.
14. Single transistor circuits including common source, common gate and source follower and their input/output impedance, applications and frequency behaviour. Source degeneration and the Miller Effect.
15. Cascode configurations and their useful characteristics.
16. Differential pairs, mode of operation, linear behaviour, CMRR, derivation of common mode and differential mode ½ circuits.
17. Current mirrors, mode of operation, issues due to early effect, use as an active load and a current source.
18. The 2-stage differential amplifier: design, analysis and VLSI issues.
19. CMOS operational amplifier : a review and VLSI design issues.
20. CMOS operational amplifier : a review and VLSI design issues, continued.

UK-SPEC - IET Learning Outcomes

Outcome Code	Supporting Statement
SM1p/SM1m	Elements of circuit theory and semiconductor device behaviour are considered. This is assessed by examination.
SM2p/SM2m	Various algebraic manipulations and differential calculus employed along with aspects of Boolean algebra. This will be assessed, where appropriate, within relevant questions.
SM3p/SM3m	The course considers VLSI across a range of levels from system down to device and naturally draws from semiconductors, circuit theory and (to a smaller extent) system design (e.g. feedback). Aspects of this knowledge and understanding will be assessed in the examination.
EA1p	Part of the course looks at the analysis of digital and analogue building blocks, allowing the students to undertake (some times simplified) analyses of behaviour and performance (e.g. small signal modelling, frequency response, Bode plots). The ability to understand and apply these principles are assessed in the examination.
EA1m	Students will be expected to understand and apply the circuit analysis of both analogue and digital circuits (intended for VLSI circuits). Students should be able to deploy these skills either in the analysis of existing circuits or the design of new circuits. This aspect will be assessed by relevant examination questions.
EA2p	Simple mathematical modelling is used to describe the behaviour of logic circuits e.g. speed, area, cost. Analogue circuit analysis – frequency response. This ability to characterise performance is assessed in the examination.
EA2m	Students will be expected to understand and apply the circuit analysis of both analogue and digital circuits (intended for VLSI circuits). Students should be able to deploy these skills either in the analysis of existing circuits or the design of new circuits. This aspect will be assessed by relevant examination questions.
EA5m	Although an introductory course, students are provided with sufficient grounding to allow application of the principles covered to new and unfamiliar cases – this will particularly be the case in the analysis of analogue circuits.
D1p/D1m	The course considers approaches to designing systems based on cost, complexity, volume, performance, and domain to identify the critical choices that must be made. Students are expected to be able identify critical issues and make reasoned arguments for a choice of technology in relevant questions in the examination.
D5p, **D5m**	Trends and process limitations/issues/challenges are considered as part of the underlying economic issues associated with VLSI design. Test and the economics of test/design for test are also considered. Students might be expected to address these issues and make reasoned arguments in answering examination questions.
D7m	Design methodologies, design flows, and processes and how these impact on design. Students are expected to be able to describe the need for and applicability of methodologies in answering relevant examination questions.
ET2p / **ET2m**	The economics of VLSI design and time to market are considered. Students are expected to understand the critical role that time to market plays and how such things as reuse/SoC, etc. can be used to mitigate cost escalation. Students will be expected to address the costing of design in relevant examination questions.
EP2p / **EP2m**	Students will understand the basics of IC fabrication and associated costs, issues, trends, and limitations. Students will also be expected to make use of circuit simulation tools such as Spice and to be aware of the limitations of circuit analysis in such cases.
EP4p/EP4m	Students will be made aware of relevant papers and the SIA roadmap

EP5p/EP5m	Students will know the critical role of design reuse and IP blocks and their impact on SoC design and design costs.
EP9m	Students are made aware of the pivotal role of the roadmap in predicting future capability, Additionally, students will know what the future challenges and likely limits of VLSI are.