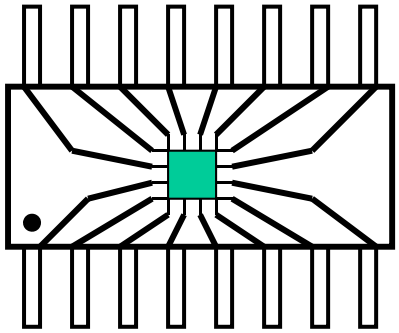
Digital Integrated Circuits

- Complexity Classifications
- Memory Devices
- Memory Expansion

Integrated Circuits (ICs)

An Integrated Circuit (IC) is a circuit constructed entirely on a single chip of silicon.



The silicon chip is mounted in a package. The inputs and outputs on the chip are connected to the package pins to allow connections to the outside world.

IC Packages

Packages generally fall into two types according to the way they are mounted on a printed circuit board (PCB). Through-hole packages have pins that are inserted through holes in the PCB and are soldered on the opposite side.

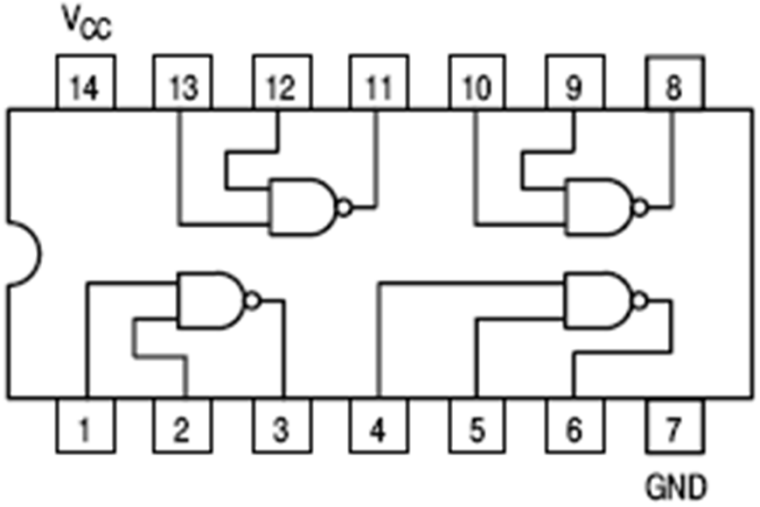
Surface mount packages have pins which are soldered directly onto one side of the board, saving space.

Complexity Classifications

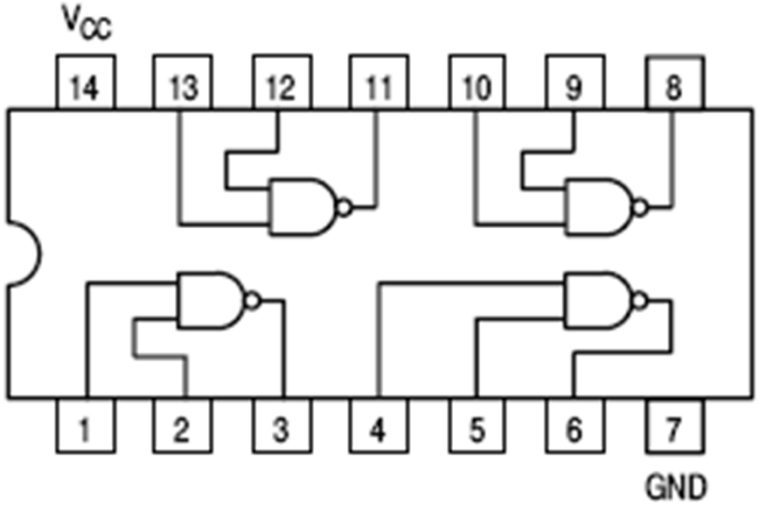
- Small-scale integration (SSI) - up to 10 gates
- Medium-Scale integration (MSI) - 10 to 100 gates
- Very large-scale integration (VLSI) - tens of thousands of gates
- System-on-a-chip (SOC) - several major components on a single integrated circuit.

Small-scale integration (SSI) - includes basic gates and flip-flops.

Example: Quad 2-Input NAND Gate

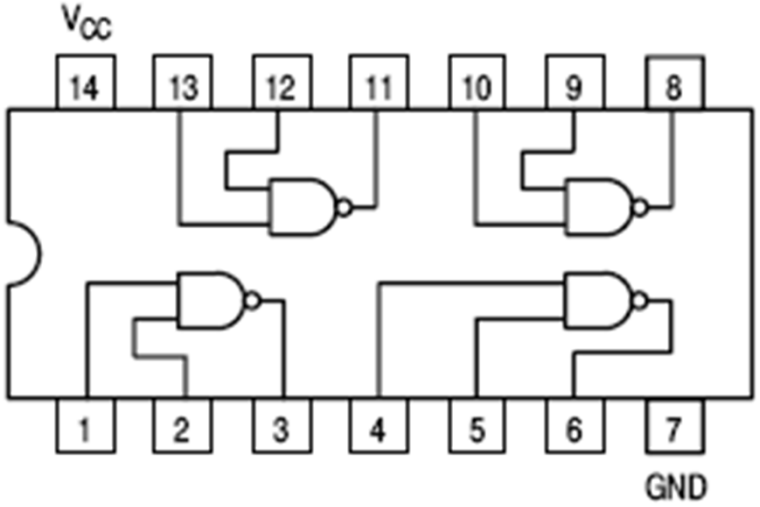


Implement F = A.B.C using 2-input NAND gates



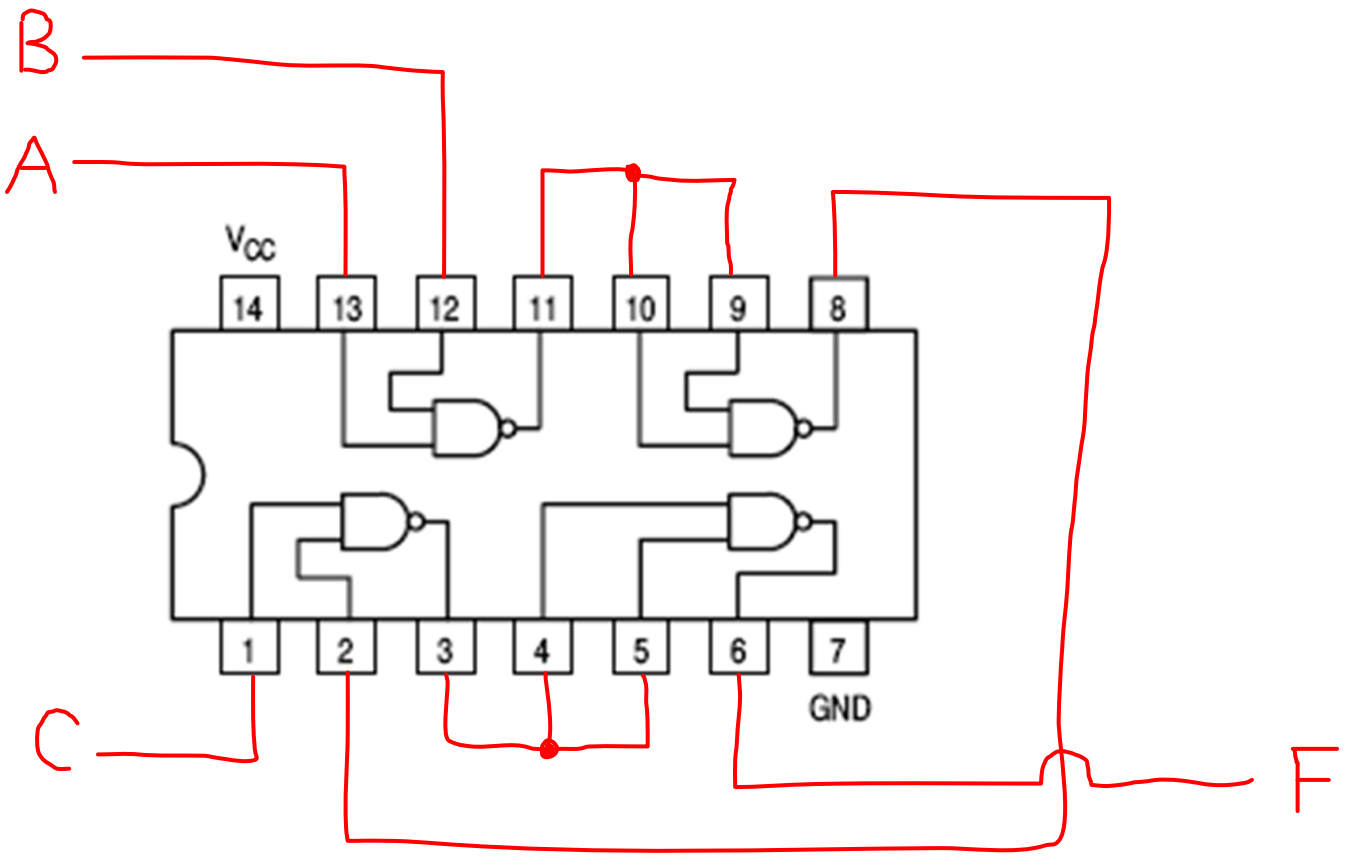
Implement F = A.B.C using 2-input NAND gates

$$F = \overline{\overline{A.B.C}}$$



Implement F = A.B.C using 2-input NAND gates

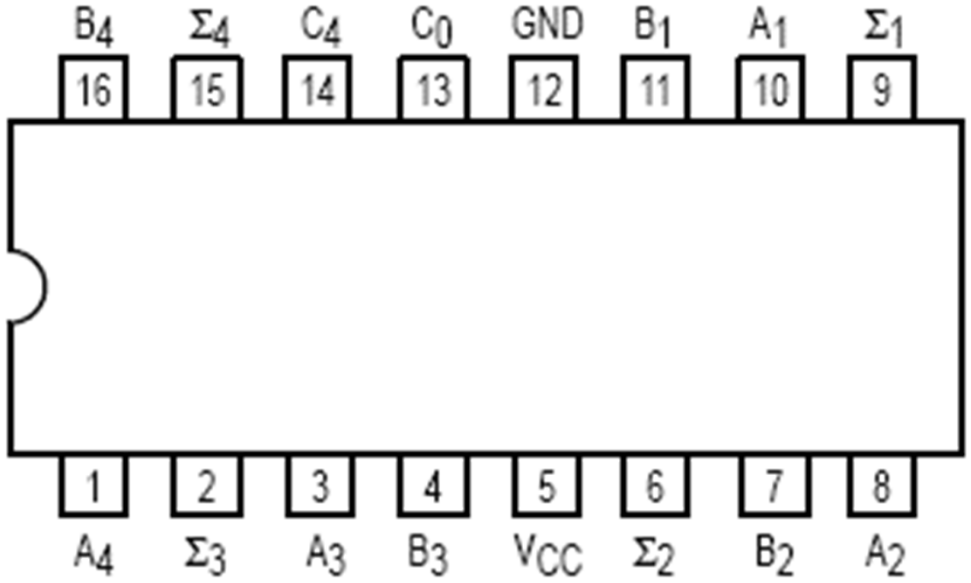
$$F = \overline{\overline{A.B.C}}$$



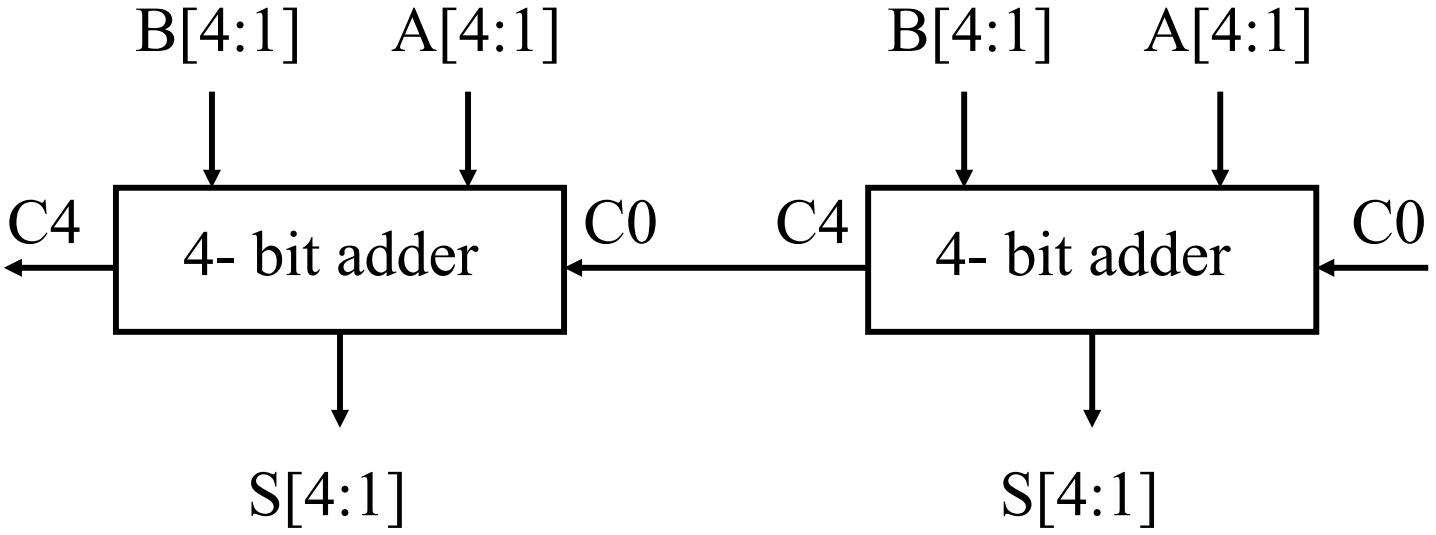
Medium-Scale integration (MSI) - includes logic functions such as decoders, arithmetic units, also small memories, registers, counters.

Example: 4-Bit Adder

$$
\begin{array}{rl}
 & C_0 \\
 & A_4A_3A_2A_1 \\
+ & B_4B_3B_2B_1 \\
\hline
 & S_4\,S_3\,S_2S_1 \\
 & C_4
\end{array}
$$



MSI - Cascading Adders



Very large-scale integration (VLSI) - tens of thousands of gates, includes microprocessors, memories

System-on-a-chip (SOC) - several major components (microprocessor, memory, RF stage) on a single integrated circuit.

DALLAS SEMICONDUCTOR MAXIM

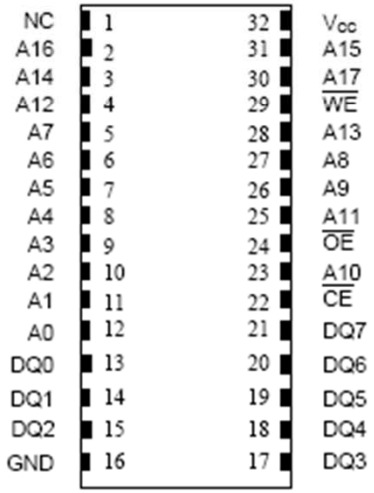
DS1249W
3.3V 2048kb Nonvolatile SRAM

www.maxim-ic.com

FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Unlimited write cycles
- Low-power CMOS operation
- Read and write access times as fast as 100ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional industrial (IND) temperature range of -40°C to +85°C
- JEDEC standard 32-pin DIP package

PIN ASSIGNMENT

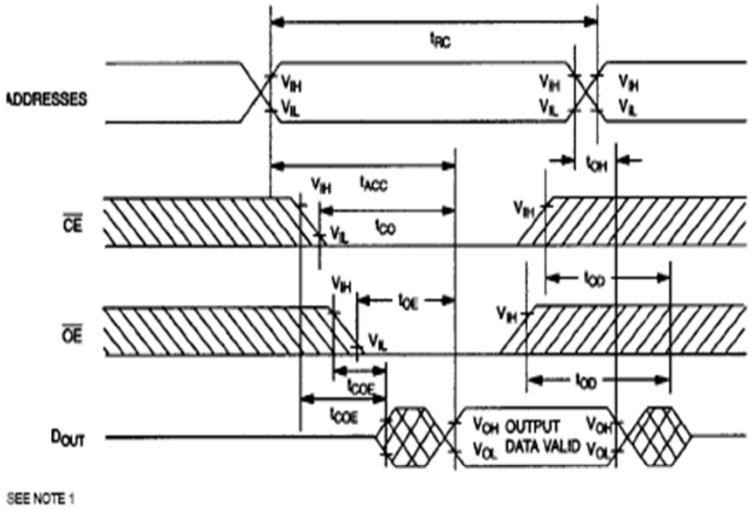


32-Pin Encapsulated Package
740mil Extended

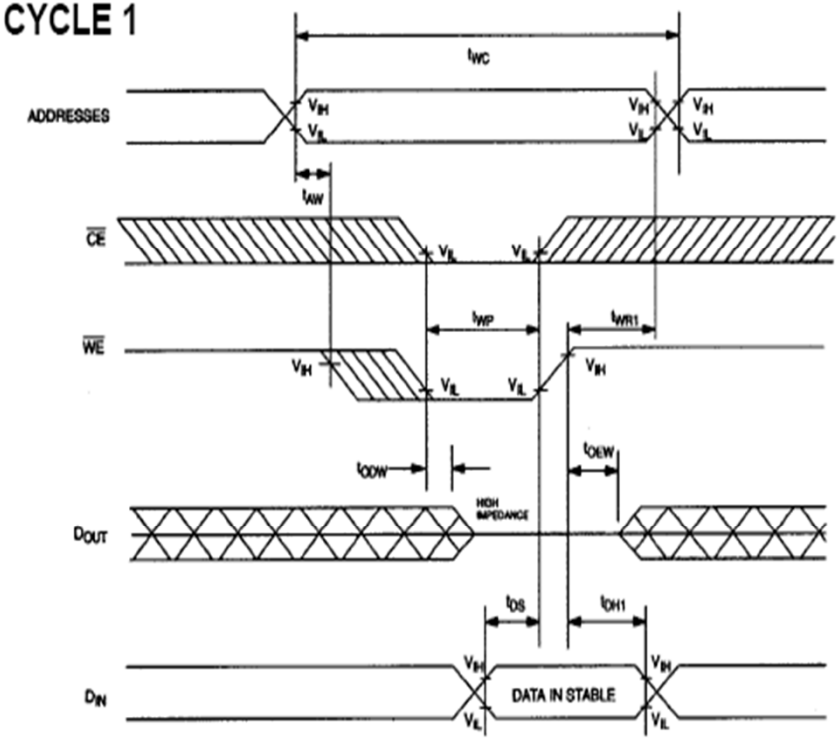
PIN DESCRIPTION

A0–A17	- Address Inputs
DQ0–DQ7	- Data In/Data Out
$\overline{CE}$	- Chip Enable
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
V_{CC}	- Power (+3.3V)
GND	- Ground
NC	- No Connect

READ CYCLE

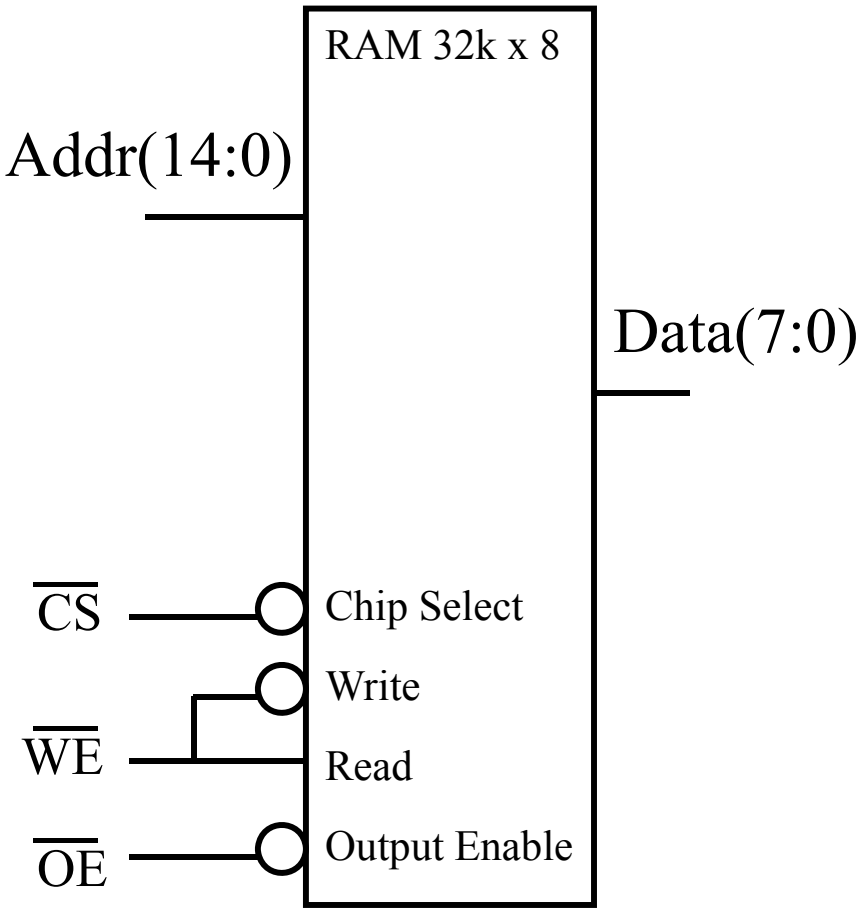


WRITE CYCLE 1



Memory Devices

Memory chips can be arranged in single bits, nibbles, bytes or multiple bytes. The diagram shows a typical 32k x 8 SRAM.

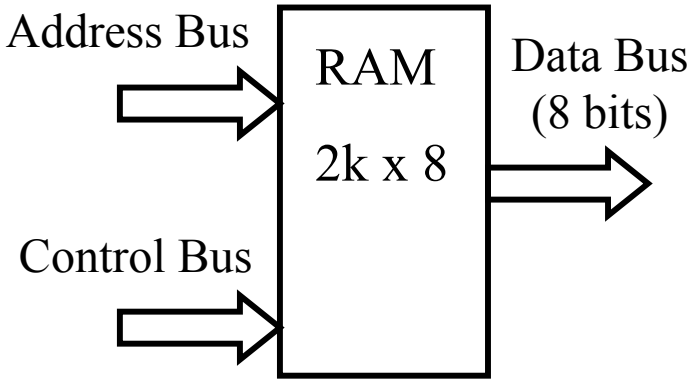


The chip select line must be low for the memory to operate.

In read mode, the write enable line is high and the output enable line is low. Data in the location specified by the address will be available on the data bus.

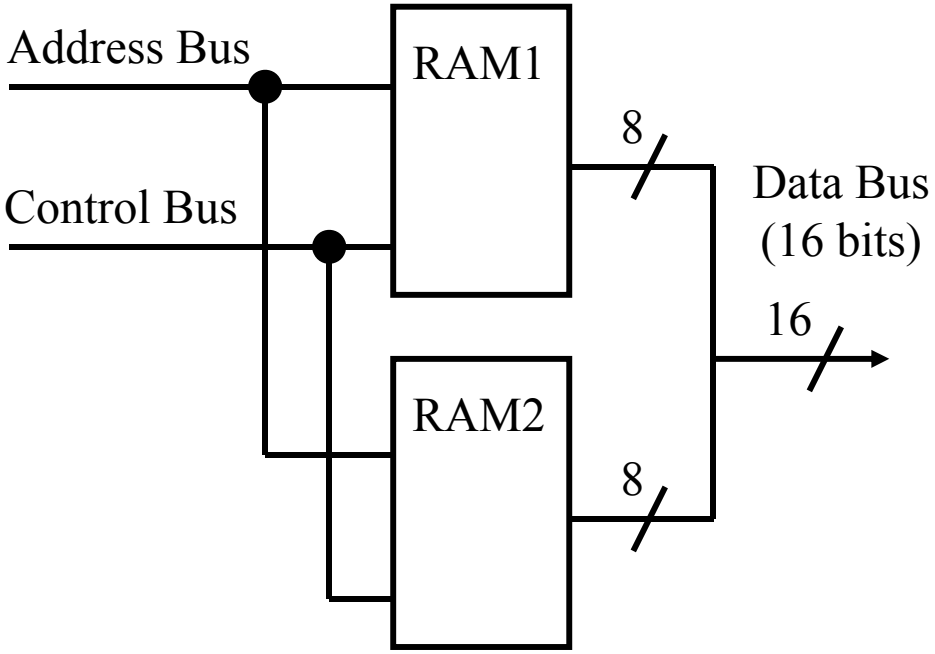
In write mode, the write enable line is low and the output enable line is high. Data on the data bus will be written to the specified address.

Word Length Expansion



The word length of a memory can be increased by combining the data buses of two similar memories.

The memories share the same control signals and address bus. The outputs in this case are 8 bits wide. They are combined to form a 16 bit wide data bus.



0 0 0 0 0
0 0 0 0 1
0 0 0 1 0
0 0 0 1 1
0 0 1 0 0
0 0 1 0 1
0 0 1 1 0
0 0 1 1 1
0 1 0 0 0
0 1 0 0 1
0 1 0 1 0
0 1 0 1 1
0 1 1 0 0
0 1 1 0 1
0 1 1 1 0
0 1 1 1 1
1 0 0 0 0
1 0 0 0 1
1 0 0 1 0

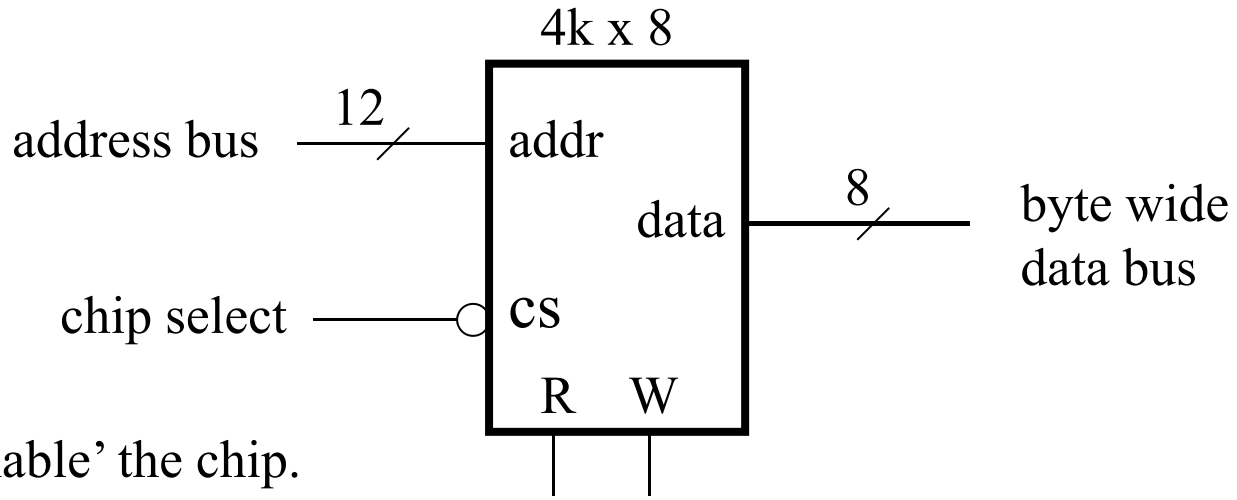
Capacity Expansion

Example: How can a 16K memory can be implemented using 4K memory chips.

This will require 4 chips. (4 x 4K = 16K)

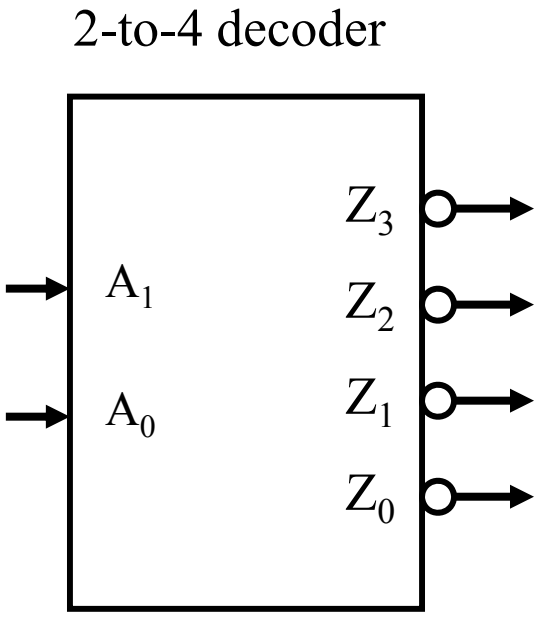
16K = 16 x 1024 = 2^{14} so a total of 14 address lines are required.

Each individual chip has 4 x 1024 = 2^{12} locations, requiring 12 address lines.



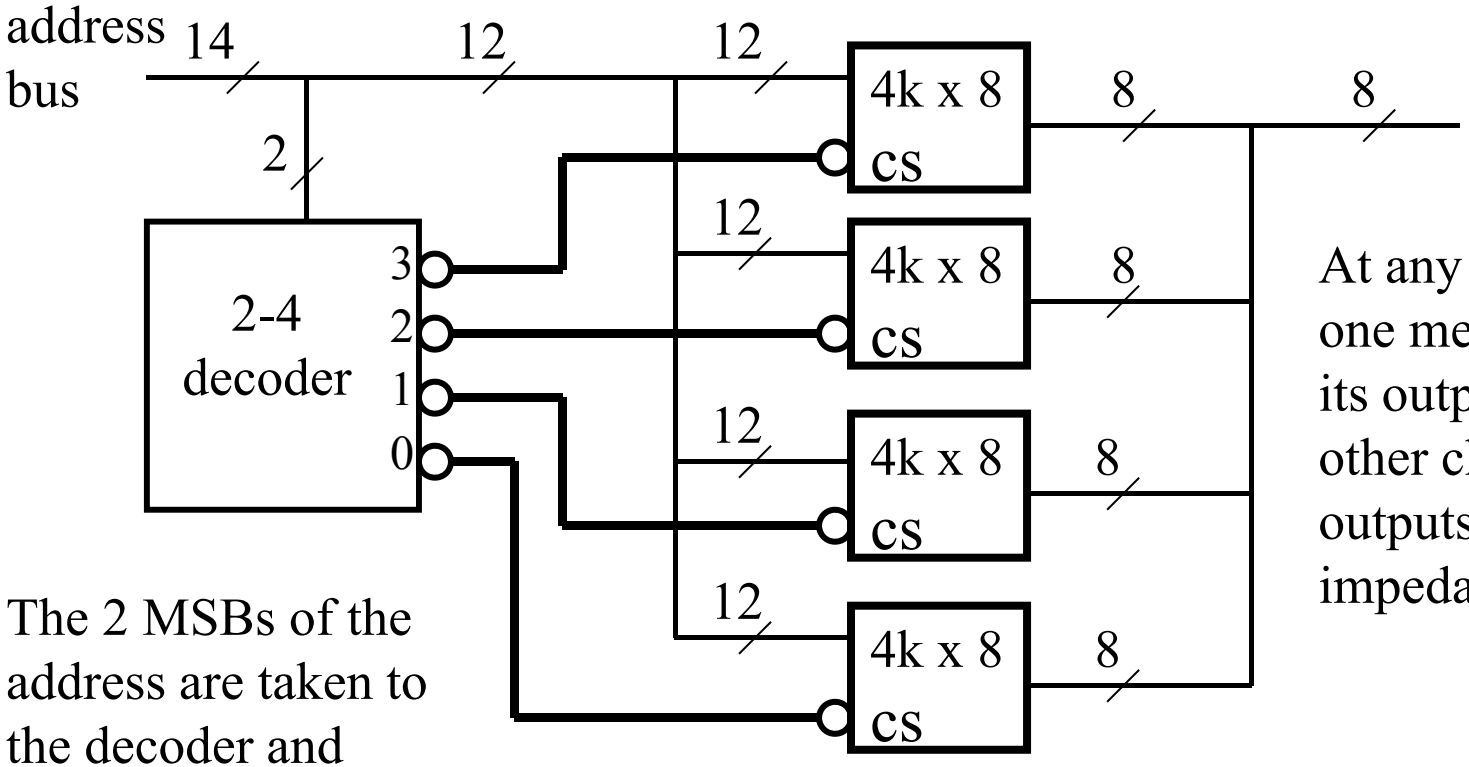
Chip select is used to 'enable' the chip.
A '0' enables the chip and a '1' puts the output into a high impedance state.

2-to-4 line decoder with active low outputs



A_1	A_0	Z_3	Z_2	Z_1	Z_0
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

16K memory with 4K chips



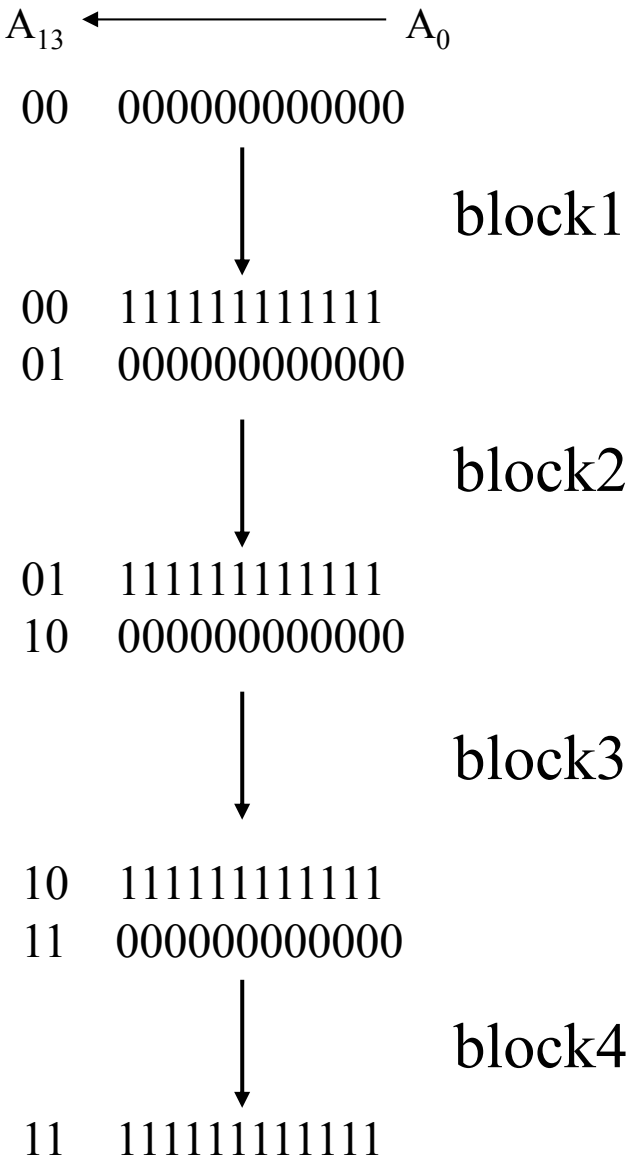
The 2 MSBs of the address are taken to the decoder and used to select one of the memory chips.

At any one time, only one memory chip has its output enabled. The other chips have their outputs in a high impedance or Z state.

Read and write lines have been omitted for clarity, but would be connected so as to give a single write line and a single read line.

Address Space

The 14 bit address A[13:0] is used as shown. The two most significant bits are used to select an individual memory block. Each of these blocks uses the remaining 12 address bits to access each of its locations.



Summary

- Integrated circuits have been classified by their complexity
- Memory word length and address capacity can be expanded by using multiple memory chips.