The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2005-2006 (2 hours)

Answers to Introduction to VLSI Design 3/VLSI Design 6

1. a. *A simplified layout for a standard cell library component is shown in Figure 1.*

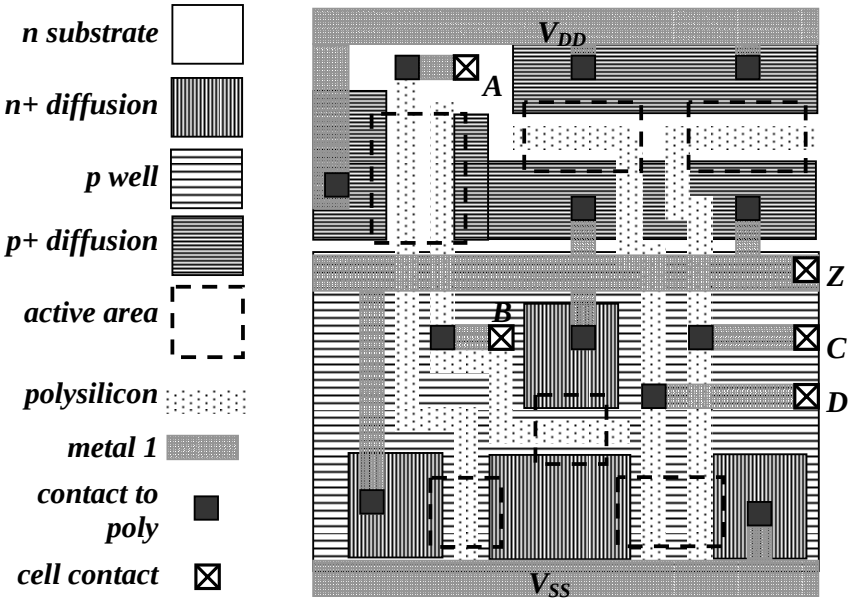
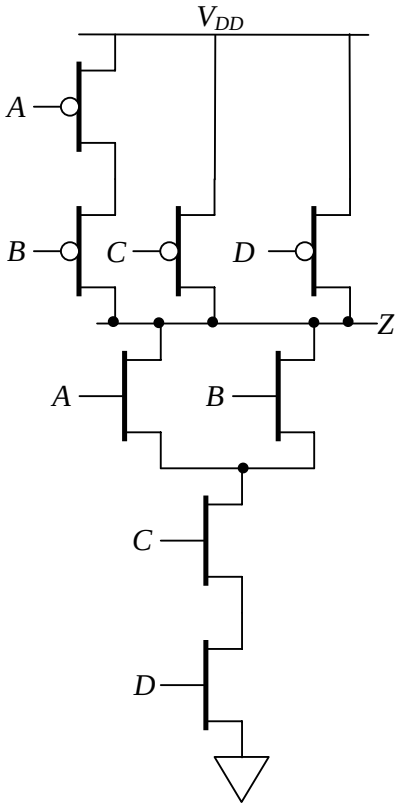


Figure 1: Cell Layout

From the layout:

i. *Draw the corresponding transistor circuit;*



(10)

ii. *Determine the logical function, Z, of the component.*

$$Z = \overline{(A+B).C.D} = \overline{(A+B)} + \overline{C} + \overline{D} = \overline{A}.\overline{B} + \overline{C} + \overline{D}$$

(4)

b. *What is the significance of the active area, defined in Figure 1, and how is it formed.*

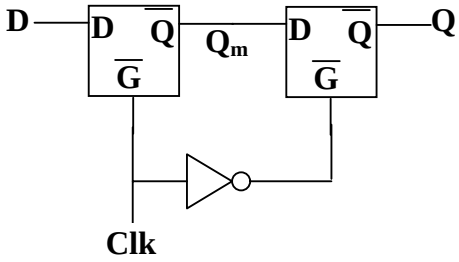
The active area is where the channel of the FET exists. To make this happen, there is a thin, controlled layer of oxide over the silicon, over which the polysilicon gate is placed (usually self aligned). During fabrication, the active area is protected (nitride over the area) whilst a thick layer of oxide (field oxide) is thermally grown over the remainder of the substrate. Once the nitride is removed, a thin layer of oxide, forming the gate insulation, is then grown in the active areas. **(3)**

c. *In the cell layout in Figure 1, V_{SS} is shown running along the bottom of the cell, and V_{DD} is shown running along the top of the cell. Why is this the case and what does it allow?*

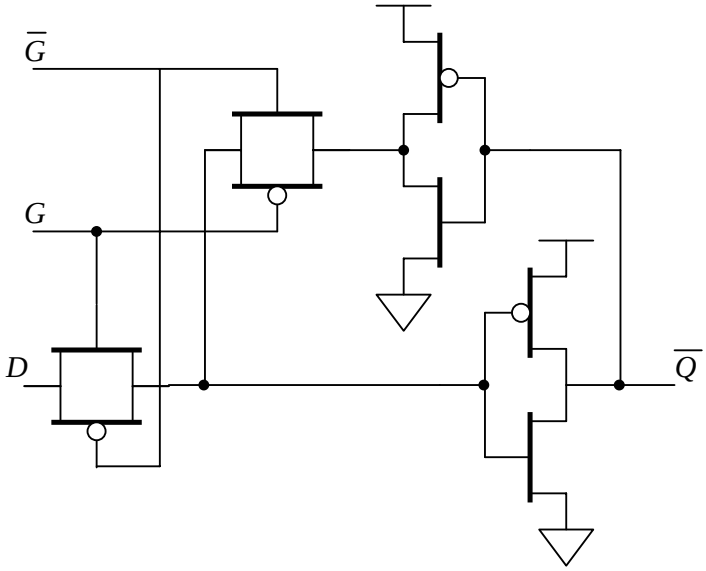
Having, well bussed power supplies is extremely important – to counter the effects of IR drops due to the peak currents in gates around clock edges. Cells from a cell library are designed to be a) compatible with each other in terms of cell height, for example, and to allow cells to be butt-jointed when being laid out, allowing the formation of a regular grid of power supply lines (acting like a power plane). **(3)**

2. a. *Show how an CMOS, edge-triggered, master-slave flip flop might be constructed from transistors (your answer should include a schematic diagram). Ensure that you identify any important requirements for the clock*

A master slave FF can be formed from two latches as follows:



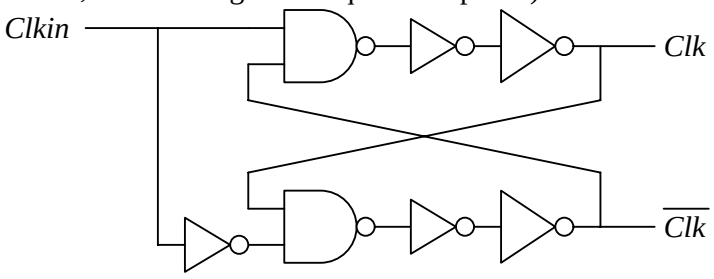
Each latch may be constructed as:



A major issue with respect to the clocking is that, in the circuit, the clock is shown to be inverted to form clockbar. However, it is important that the clock and its inverse do not overlap – that is they should never be low at the same time. If this were to happen then both latches would be transparent and, depending on circumstances, the input around the falling edge of clock could propagate to the output. **(4)**

b. i. *How might a two-phase clock generator – with non-overlapping phases – be designed?*

A two phase clock, such as might be required in part a) could be constructed as follows:



(4)

ii. *How can the amount of underlap be controlled?*

The amount of underlap, the time between *Clk* going high and *Clkbar* going low, is controlled by the delay through the NAND gate and the inverter chain at the output of the RS flip-flop. When *Clk* goes high, the input to the lower NAND gate will be 11 and the output will go to zero – after the signal propagates along the inverter chain, *Clkbar* will then go low. By adding pairs of inverters in each (or one or other) chain, the length of underlap can be altered. **(2)**

iii. *Outline how can the clock generator be designed to drive a large capacitive load (you do not have to do a detailed analysis in this part of the question).*

As is shown, to some extent, in the diagram, by adding a tapered set of inverters – growing exponentially in width, a large capacitive load – such as a clock tree or external load could be driven. Clearly, in this case, it would not be possible to control the underlap and load driving capability independently. **(3)**

c. **i.** *State the expression for upsets/second as a consequence of metastability where a data signal with an effective frequency of f_{data} is sampled in flip-flop being clocked at a frequency of f_{clk}. If you introduce any terms, please ensure that you explain what they are and how they arise.*

$$upsets = T_0 e^{-\frac{t_r}{t_c}} f_{clk} f_{data}$$

T_o is a circuit related figure that relates to design and layout of the sampler and the underlying technology used to implement the sampler. t_c is related to 1/GBW for the inverters/amplifiers in the sampler. t_r is the observation time – that is, the amount of time after the input is sampled before the input is *observed* (typically, by being sampled in the next sampler. If the input is in an intermediatestate when the sampler samples, the positive feedback inherent in the bistable at the heart of a sampler, will cause the output to relax from the intermediate state to the *nearest* stable state (the rate at which it does this is related to the GBW product and the circuit design/layout) – the nearer to the balance point the longer this will take. The longer this process continues before the output is observed, the smaller the probability that the output will be in an intermediate state when it is observed. Clearly, this probability when multiplied by the number of samples per second and conditioned by the rate at which the input is changing will give the number of intermediate states observed per second. **(3)**

ii. *It is calculated that each flip-flop, within an 8-bit register, sampling data from a data bus input, where f_{data}=25kHz and f_{clk} = 100kHz, will experience one upset every 10 minutes. Provide an analysis to find how often the 8-bit value read from the data bus be upset and calculate this value (if you have to introduce an approximation to calculate the result then ensure that you identify what you have done).*

We know that number of upsets = $p_u.f_{clk}.f_{data}$ where p_u is the probability of an upset per data event, per clock edge, per second. If there are n bits in the word being sampled, the probability of an upset in the word per data event, per clock edge, per second will be $1-(1-p_u)^n$. That is, assuming that the upsets are independent, the probability of a bit being correct is $1-p_u$ and raising this to the power of n yields the probability of the word being correct. Consequently, the number of upset words per second will be $(1-(1-p_u)^n).f_{clk}.f_{data}$. However, looking at the values – one upset every 10 minutes is $1.66\text{x}10^{-3}$ upsets per second and $p_u=6.66\text{x}10^{-13}$. Unfortunately, $(1-p_u)^n$ will probably evaluate to 1 on a desktop calculator. However, to a first order, $(1-p_u)^n = 1-n.p_u$. and so an approximation of

$n.p_u.f_{clk}.f_{data}$ can be used. In this case, this is one upset every 1.25 minutes. **(4)**

3. a. *Identify the two conditions that must be met in the pull-up and pull-down networks in a standard CMOS logic circuit, for all combinations of inputs.*

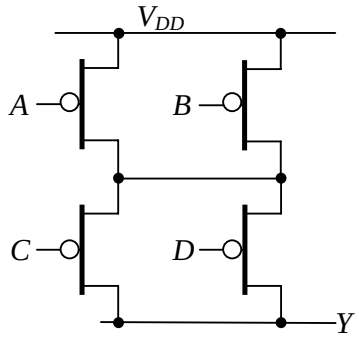
The pull-up and pull-down networks must complementary in the sense that:

There must be a low-impedance path to only one of the power supply voltages for any and all combination of input states – this means that either the pull-up or pull-down network is low-impedance – not both (which would create a low-impedance path between the power supplies)

The must be a low impedance path to a power supply for all input states – this means that the output will be well-defined for all input states. **(4)**

b. *For the pull-down network in **Figure 3** find:*

i. *The corresponding pull-up network.*



ii. *The function, Y.*

$Y = \overline{A.B + C.D}$

iii. *How would the function change if the points labelled p and q are connected?* **(4)**

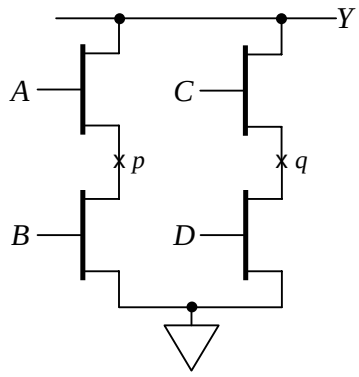


Figure 3: Pull-Down Network

(4)

The function would become:

$Y = \overline{(B + D).(A + C)}$

(4)

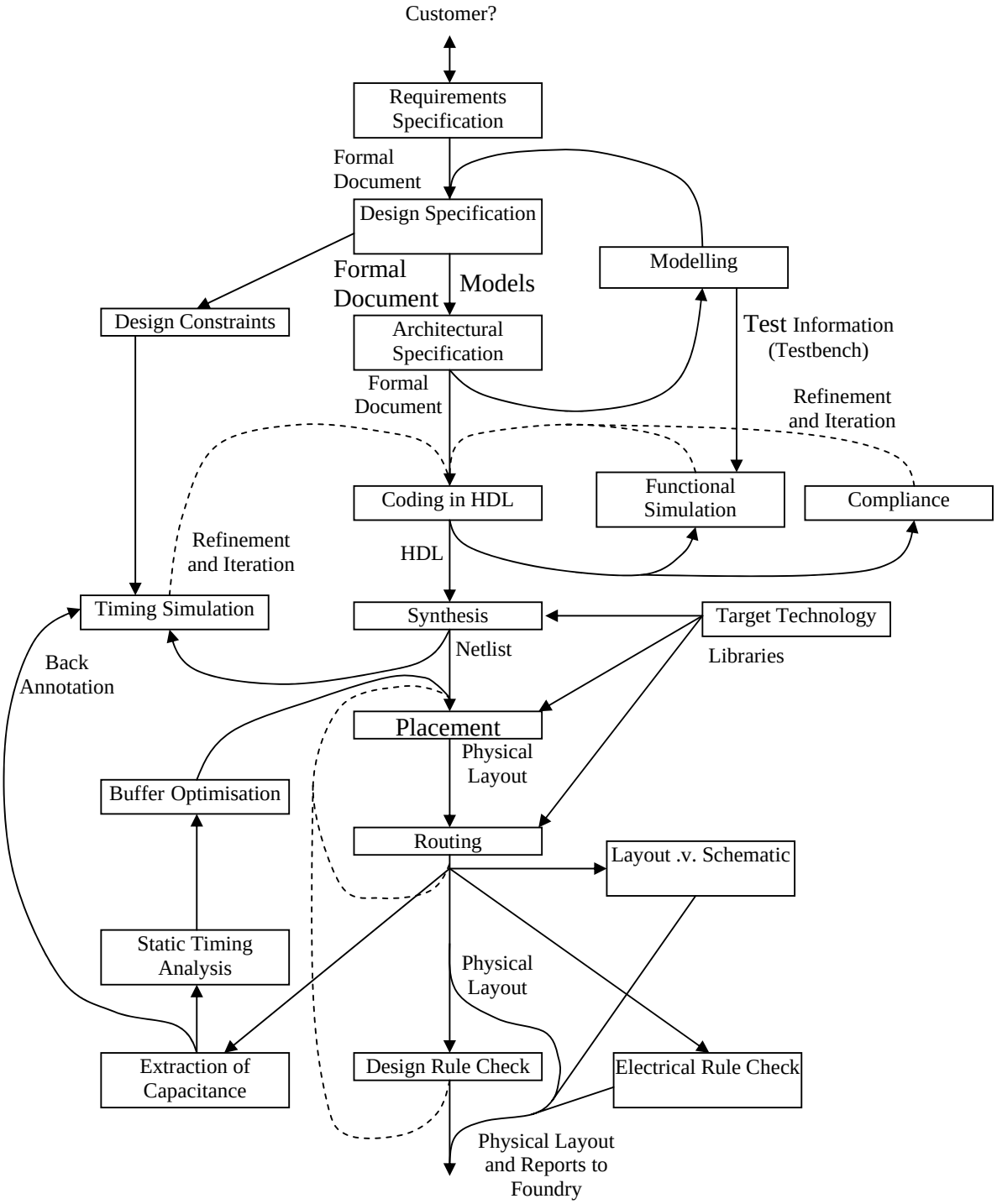
c. *What is the body effect and what limitation does it introduce for CMOS circuits?*

The threshold voltage for an FET depends on the voltage at which the substate material is held. So for an *n*-type FET:

$$V_{TN} = V_{T0N} + \gamma \cdot \left(\sqrt{2|\phi| - V_{BB}} - \sqrt{2|\phi|} \right)$$

Where V_{T0N} is the basic threshold voltage, V_{BB} is the threshold voltage (relative to the source of the FET), γ is the *bulk-threshold parameter*, and ϕ is called the *strong-inversion surface potential*. Normally all of the transistors in the pull-down network for a logic gate will share the same value of V_{BB} and if these transistors are stacked on top of each other this can cause a problem. Consider a stack of *n* *n*FETs in a pull-down network with the bottom one switched off and the upper *n*-1 switched on. The source of the top transistor will be at V_{DD}-V_{TN} but the value of $V_{BB} \approx -V_{DD}+V_{TN}$. In this case, V_{TN} is larger than V_{T0N} and the available current drive (once the bottom transistor switches on, which is related to $1/(V_{DD}-V_{TN})$ will be reduced, as a consequence, and the pull-down network will switch more slowly than might be expected given normal circumstances – this may constitute a problem. **(4)**

4. a. *Identify the various steps or stages in an ASIC design-flow, showing how the various steps might be connected*



A diagram such as this would be helpful – but I would accept something substantially less complex – showing the major steps from requirements through architectural and design specification, coding, verification, synthesis, P+R, interface to the foundry. Answers should identify the iterations and a good answer would say that timing closure will possibly require iteration through P+R back to design **(6)**

b. *An IC design house sees a gap in the market for product that requires a digital ASIC to be designed. Initial analysis suggests that the IC will be approximately 500,000 gate equivalents and will need to run at a clock frequency of 50MHz. Market analysis suggests that the product can be sold for £600 once the market is developed and that, from this, the budget for the IC is £30-40. At this early stage, it is not possible to be sure how big the market will be but it could be 100,000 units per year. Furthermore, it is known that a competitor has also, possibly, seen this opportunity.*

How might the development of the ASIC be undertaken? Ensure that you identify which type of implementation(s) might be chosen: when and why.

The key elements to answering this question are that:

- The ASIC is relatively modest in terms of performance and it would be possible to source a mid range FPGA that might be up to the task; **(2)**
- There is a relatively big budget for the IC – if the selling price is £600, then the manufacturing cost for the whole system is circa £200 and the ASIC is relatively major part of this cost. **(2)**
- The size of the market is unknown – but could be large.
- Time to market is constrained by your competitor possibly pursuing the same opportunity.

All of these things point to a rapid implementation using an FPGA (mid-sized). This would be initially expensive, particularly on a per unit basis. For example, based on a 6 month project at 150kT/year/person estimate for productivity, this might take a 7 person team. **(2)** Assuming £150k pa cost per designer – including O/Hs and CAD/support, this development may cost £500k. **(2)** If you assume a per unit FPGA cost of £20 (this is reasonable) then if you assume 1000 units initially then the cost is quite high per system of £520. At 10,000 units, this falls to £70. So there is some risk. **(2)** However, once the product is in the market – within 6 months. There is a window of opportunity to migrate the design as a derivative design to an MGA. **(2)** This would probably add another £100k for foundry costs and another £100K re-engineering costs with unit costs of say £4 in quantity. With an additional 100,000 units sold in the 2nd year, this gives a total cost of £500K +10000*20+£200K+100000*4 and this would work out to be £11.80 per unit over the 2 years. **(2)**

NLS / MB