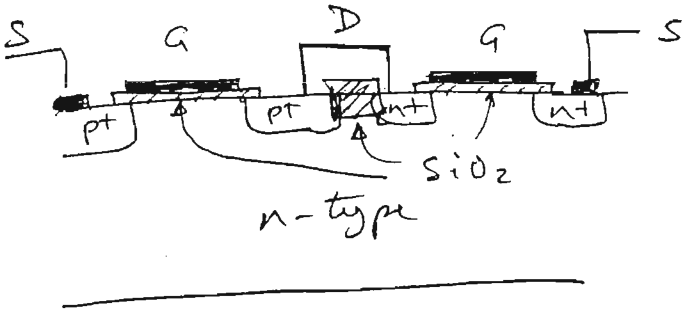
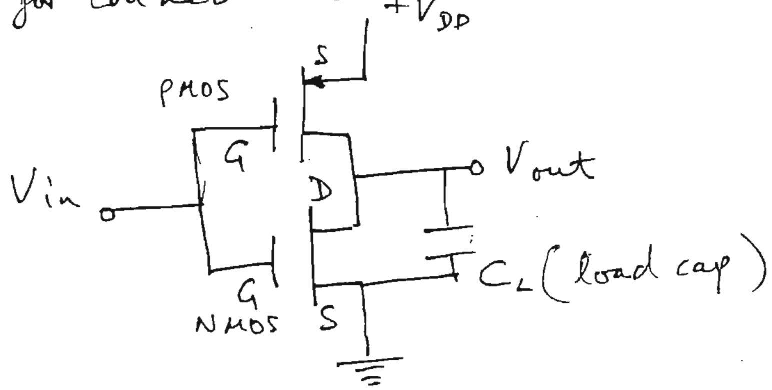
Q1 (a)



6

2 marks for each of p-channel + n-channel device

2 marks for connections



2

<u>$V_{in} = 0$</u> NMOS OFF (zero gate bias)

PMOS ON ((−)ve gate-source bias) 1

until $V_{out} = V_{DD}$.

<u>$V_{in} = +V_{DD}$</u> NMOS ON until Vout discharges 1

to ground ($V_{out} = 0$)

PMOS OF

(b) gate capacitance $C_{ox}^* \propto \frac{1}{d_{ox}} \cdot L_G \cdot Z$

gate capacitance/unit area $C_{ox} \propto \frac{1}{d_{ox}}$ L_G, Z – length and width of gate

Each dimension is reduced by K

$\therefore C_{ox} \rightarrow \frac{K}{d_{ox}}$ $\therefore$ <u>C_{ox} increases by K</u> 1

Q1 (b) cont.

Under velocity saturation conditions.

$$I_D \propto \frac{Z}{L_G} \cdot Q \, v_{sat}$$

Z = gate width
L_G = gate length
Q = charge / unit area in channel
v_{sat} = saturation velocity.

v_{sat} unaffected by scaling

$$\therefore I_D \rightarrow \frac{Z}{K} \cdot \frac{\cancel{K}}{L_G} \cdot \frac{C_{ox} V . \cancel{K}}{\cancel{K}}$$

$\therefore$ I_D independent of scale factor K. 2

Hence switch delay $\propto L \propto \frac{1}{K}$ 1

Power consumption $\propto I_D V \propto \frac{1}{K}$ 1

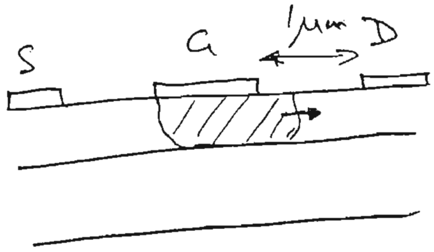
Power-delay product $\propto \frac{1}{K^2}$ 1

$$\text{Power density} \propto \frac{I_D V}{L_G Z} \propto \frac{1}{\cancel{K}} \cdot K^{\cancel{2}} \propto K$$

i.e. power density increases under velocity saturation conditions leading to cooling problems as scaling down is applied. 2

If V is not scaled then power density will increase further, causing more problems. 2

Q3.



Depletion region moves towards the drain and breakdown determined by G–D spacing. 1

Assume field between G–D uniform (zero doping)

i.e. $\int_0^d \alpha\, dx = \alpha d = 1$ at breakdown 1

$\therefore \alpha = \frac{1}{d} = 10^6 \ m^{-1} = 1\times10^{-30} E^5$

$\therefore E^5 = 10^{36}$

$\therefore$ Breakdown field $E = 10^{36/5} = 10^{7.2} = 1.58\times10^7$ V/m

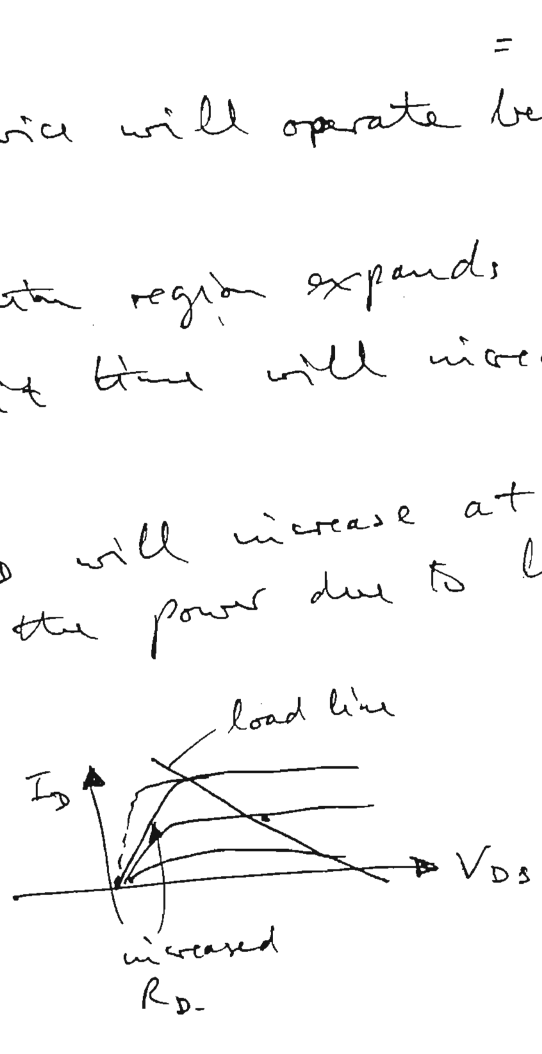
$\therefore$ Breakdown voltage $V_B = 1.58\times10^7 \times 1\times10^{-6}$

$= \underline{15.8\ V}$ 2

$\therefore$ Device will operate below breakdown voltage.

As depletion region expands towards the gate ~~the~~ transit time will increase and hence f_T reduce. 2

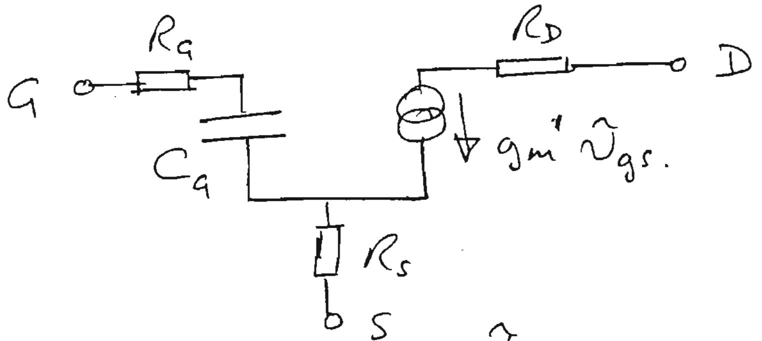
Also R_D will increase at low voltages hence limiting the power due to limited voltage swing.



2

Q2 (cont)

(b) Equivalent circuit reduces to



2

input (gate) current $\hat{i}_G = \dfrac{\hat{v}_{GS}}{\underbrace{\cancel{R_G}}_{\text{small}} + R_S + \frac{1}{\omega C_G}}$ 1

output (drain) current $\hat{i}_D = g_m' \hat{v}_{GS}$ g_m' = extrinsic g_m

current gain $\dfrac{\hat{i}_D}{\hat{i}_G} = \dfrac{g_m' \hat{v}_{GS}}{\hat{v}_{GS}} \left(R_S + \dfrac{1}{\omega C_G} \right)$

$= 1$ when $f = f_T = \dfrac{\omega_T}{2\pi}$ 2

$$\Rightarrow f_T = \frac{1}{2\pi C_G \left(\frac{1}{g_m'} - R_S \right)}$$

$$= \frac{1}{2\pi C_G \left(\frac{1 + g_m R_S}{g_m} - R_S \right)} \qquad g_m' = \frac{g_m}{1 + g_m R_S}$$

2

$$= \frac{g_m}{2\pi C_G}$$ $\boxed{\text{i.e. } R_S \text{ has no effect on } f_T}$

(c) $f_T = \dfrac{g_m}{2\pi C_G} = \dfrac{v_{sat}}{2\pi L_G} = \dfrac{1 \times 10^5}{2\pi \cdot 0.5 \times 10^{-6}}$

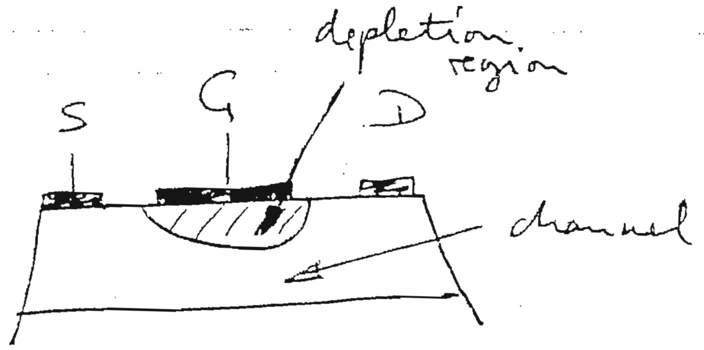
2

$= \underline{31.8 \text{ GHz}}$

Q3

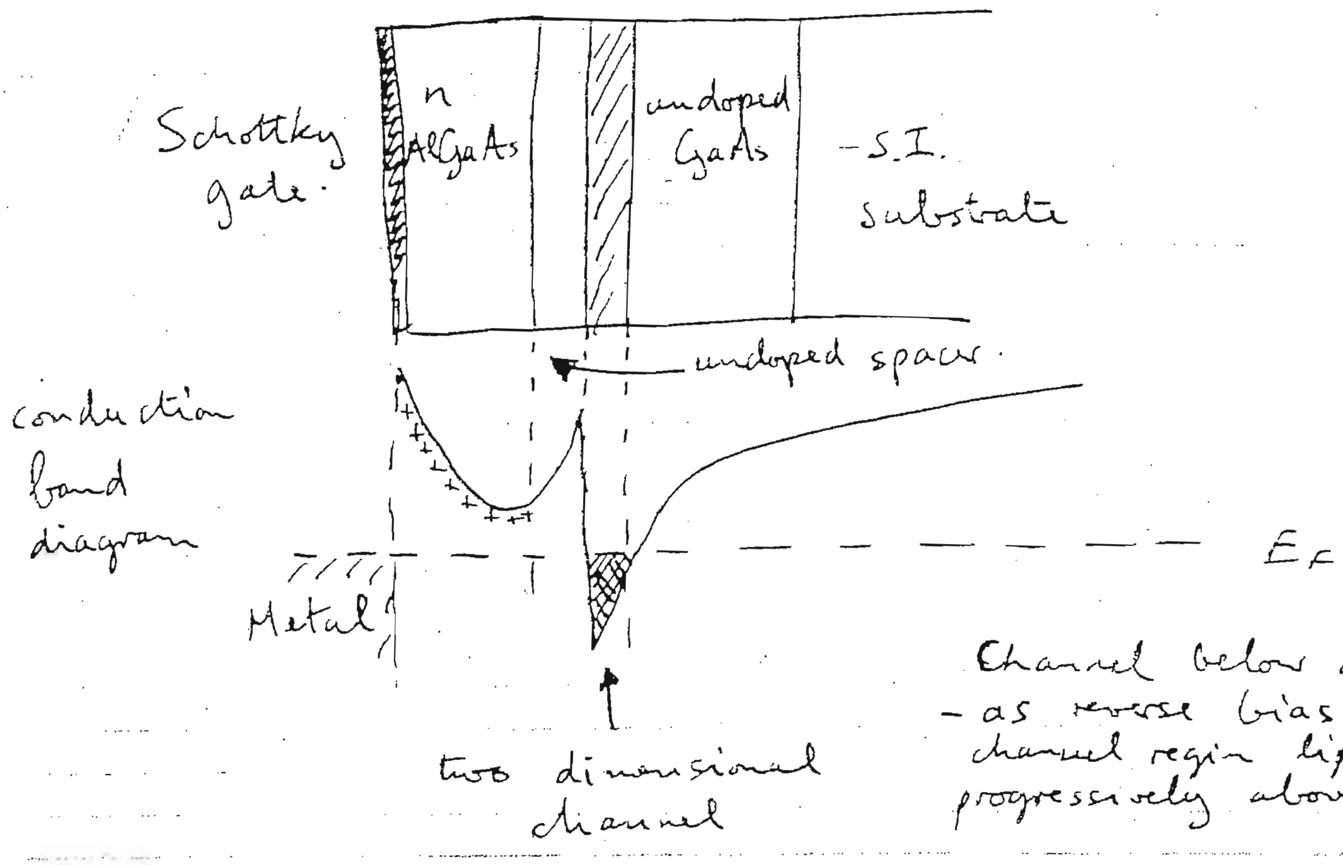
(a)

MESFET.



As gate voltage is increased negatively, the channel is constricted and current from source to drain is controlled. Magnitude of drain currents depends on doping concentration in the channel and mobility. 3

HEMT. As for MESFET but detail of gate region as follows.



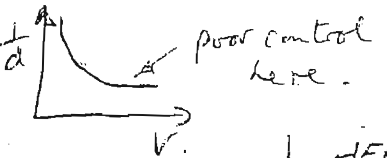
4

Channel below E_F fills – as reverse bias applied channel region lifted progressively above E_F

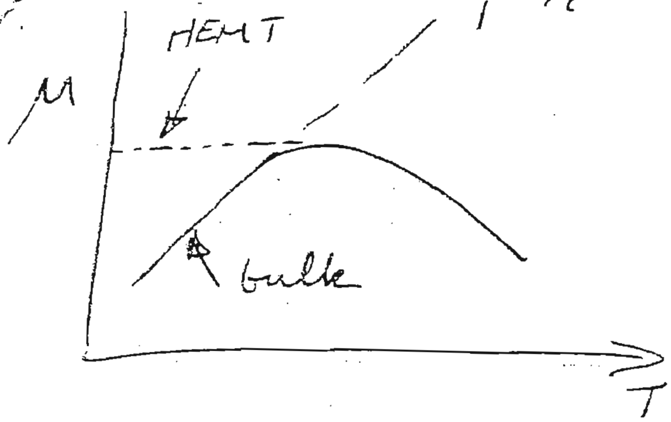
Q3(cont.)

Main HEMT advantage – because free electrons are separated from donor atoms, ionized impurity scattering is minimised hence g_m and transit time improved.

As the channel thickness increases it becomes more and more difficult to control the channel with gate voltage ie. 3



(b)



$T = 77K \quad \mu = 0.3\ m^2V^{-1}s^{-1}$

$\therefore \mu = CT^{3/2}$

$\therefore C = \dfrac{0.3}{77^{3/2}}$

$= 4.4 \times 10^{-4}$

$\mu(10) = 4.4\times10^{-4} \times 10^{3/2} = 0.014 \quad$ i.e. $\dfrac{\mu(10)}{\mu(77)} = \underline{\underline{\dfrac{1}{21.4}}}$

ie. factor of ~21 improvement in g_m for same sheet concentration. 4

(c) $E = \dfrac{V}{L}$, $\quad v = \mu E = \dfrac{\mu V}{L}$, $\quad \tau = \dfrac{L}{v} = \dfrac{L^2}{\mu V}$, 2

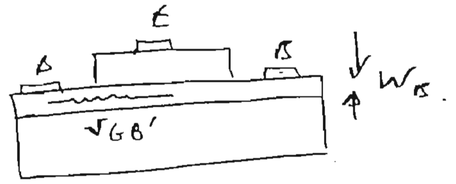
10K

HEMT $f_T = \dfrac{\mu V}{2\pi L^2} = \dfrac{0.3\times1}{2\pi\times0.25\times10^{-12}} = \underline{\underline{191\ GHz}}$ 2

MESFET $f_T = \dfrac{190}{21.4} = \underline{\underline{8.9\ GHz}}$ 2

$E = \dfrac{V}{L} = \dfrac{1}{0.5\times10^{-6}} = 2\times10^6\ V/m$ ie. electrons will reach velocity saturation at these fields ie. $v_{sat} \ll \mu E$.

Q4 (a) $r_{bb'}$ is the base access resistance and can be greatly reduced by increasing the base doping level. This is possible in the HBT since the heterojunction BE ensures good injection efficiency regardless of relative doping levels in the base and emitter. Hence can get good gain and high ~~req~~ frequency (thin base + high doping) 2



$C_{b'e}$ represents the diffusion and depletion capacitance of the BE junction. Reduce depletion capacitance by reducing emitter doping and reduce diffusion capacitance by reducing width of base, W_B (less charge in base). Former would compromise injection efficiency in Si bipolar, latter would increase $r_{bb'}$ to unacceptable levels. Reduced $C_{b'e}$ improves operating frequency. 2

r_o (output resistance) is increased due to reduced Early effect due to increased base doping in HBT. 2

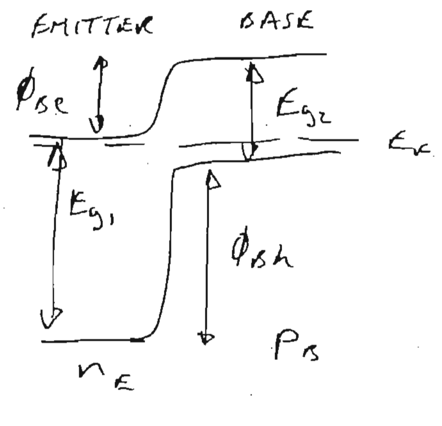
(b) electron current $I_e \propto \sim n_E \exp \frac{\phi_{Be}}{kT}$ 2

hole current $I_h \propto \sim p_B \exp \frac{\phi_{Bh}}{kT}$

ϕ_{Be}, ϕ_{Bh} barrier for electrons, holes.

$$\therefore \frac{I_e}{I_h} \simeq \frac{n_E \exp \frac{-\phi_{Be}}{kT}}{p_B \exp \frac{-\phi_{Bh}}{kT}} \quad 2$$

$$= \frac{n_E}{p_B} \exp \frac{\phi_{Bh} - \phi_{Be}}{kT}$$



Q4 cont.

$$\frac{I_e}{I_h} \approx \frac{n_E}{p_B} \exp \frac{E_{g1} - E_{g2}}{kT}$$

from digram
$\phi_{Be} \approx E_{g2}$
$\phi_{Bh} \approx E_{g1}$

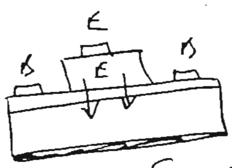
$$= \frac{n_E}{p_B} \exp \frac{0.47}{0.026}$$

$$= \underline{\frac{n_E}{p_B}\, 7.1 \times 10^7}.$$ 2

ie. Injection ratio increase by 7.1×10^7 when an HBT structure (GaAs/AlGaAs) is used.
Since injection efficiency for an HBT ≈ 1 and since the electron lifetime in the base is small ($\propto \frac{1}{p_B}$), base recombination is likely to limit the gain. 2

(c) Since current travels perpendicular to the contacts in bipolars as opposed to parallel to the surface in FETs, larger area is available to the former and hence power handling for a given device size is likely to be better for bipolars.

ie. bipolar



vertical current flow.

FET

lateral current flow 3

Frequency of FET determined by gate length L, which is defined by lithography – difficult.
Bipolar is determined by base and collector thickness which is defined during crystal growth – much easier.
Hence on this argument bipolars are easier to make.

3