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Lecture 16

- CMOS
- Digital electronics and integrated circuits
- Scaling of CMOS

Complimentary MOS (CMOS)

- CMOS is made up of n-channel and p-channel MOS devices.
- The NMOS and PMOS devices operate complementary to each other.
- When one is off the other is on.

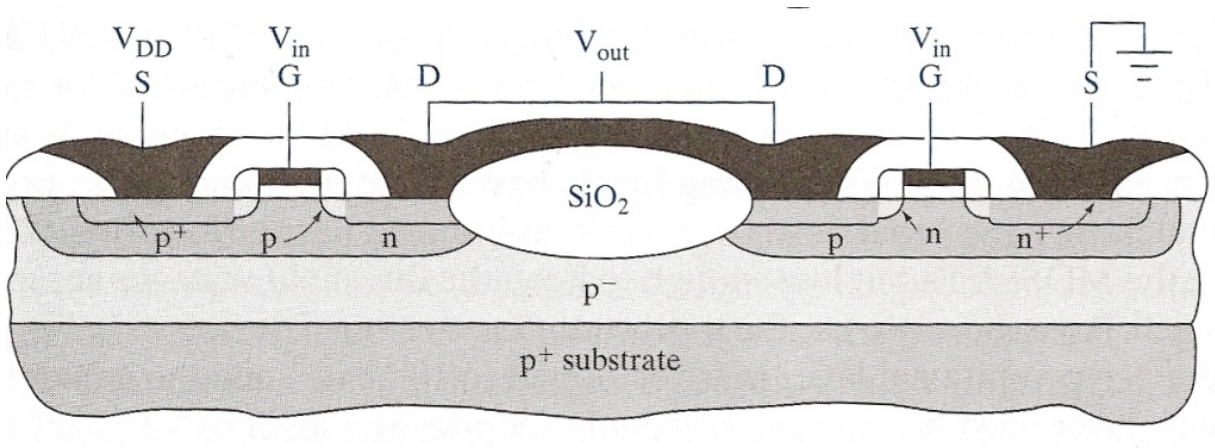

Figure 9–4 Complementary MOS structure: (a) CMOS inverter; (b) formation of p-channel and n-channel devices together.

From Streetman 6th Ed.

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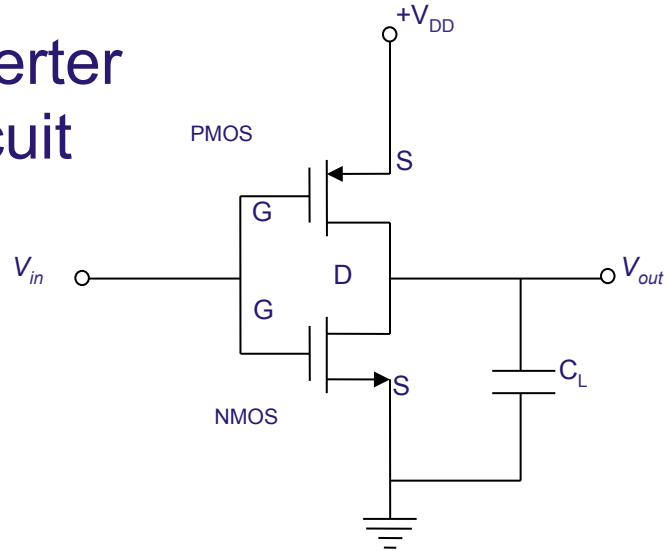
Complimentary MOS (CMOS)

- Because of complementary action, current only flows during the switching cycle (from low to high).
- This means that CMOS uses very little power and virtually none during stand-by
- Hence very useful for low power circuits and very large scale integrated circuits where power dissipation causes severe problems (such as in microprocessors)

Inverter circuit



$V_{in} = 0$
NMOS device off (zero gate bias)

PMOS conducts (effective negative gate/source bias) until $V_{out} = V_{DD}$

$V_{in} = +V_{DD}$
NMOS device on (positive gate bias) and conducts until V_{out} discharges to ground ($V_{out} = 0$)

PMOS off (positive gate bias)

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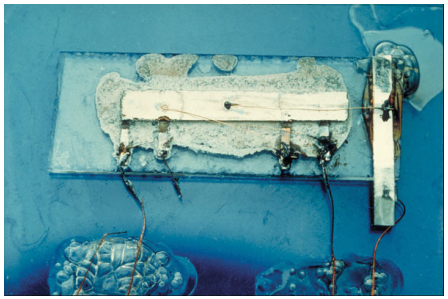
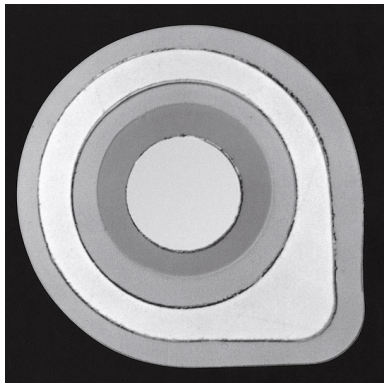
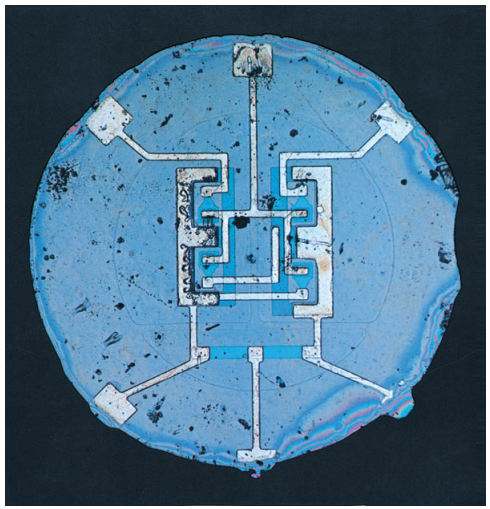
Evolution of the Integrated Circuit



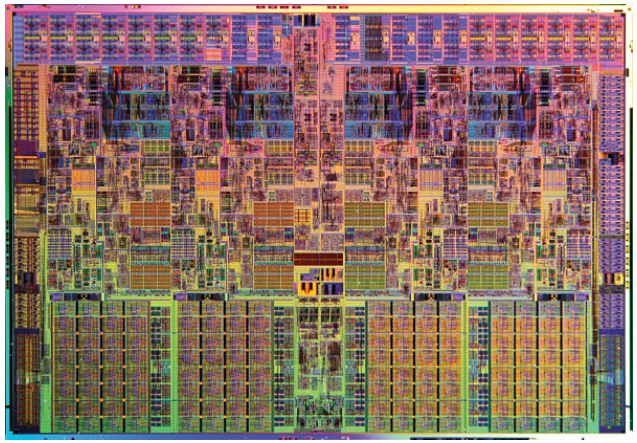
Jack Kilby - 1958 -first integrated circuit



Jean Hoerni – 1959 - first planar (flat) transistor



Robert Noyce -1961 - resistor-transistor logic chip with four transistors



VLSI – Very Large Scale Integration

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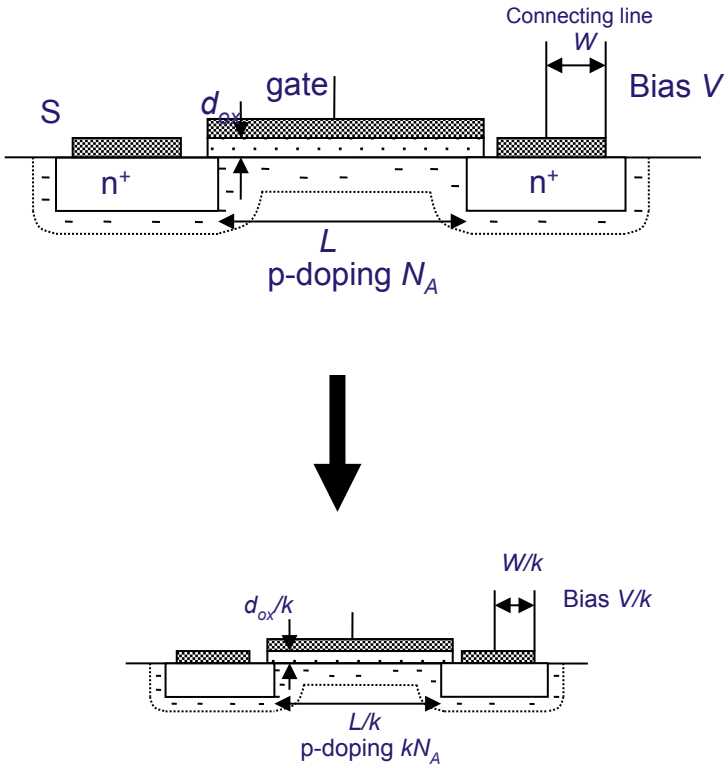
Miniaturisation (scaling)



- Increased density
- Faster switch
- Reduced voltage
- Reduced power per switch
- Reduced cost per function

Scaling (reducing transistor size) has been the basis for progression of integrated circuit technology described by Moore's Law for over 30 years.

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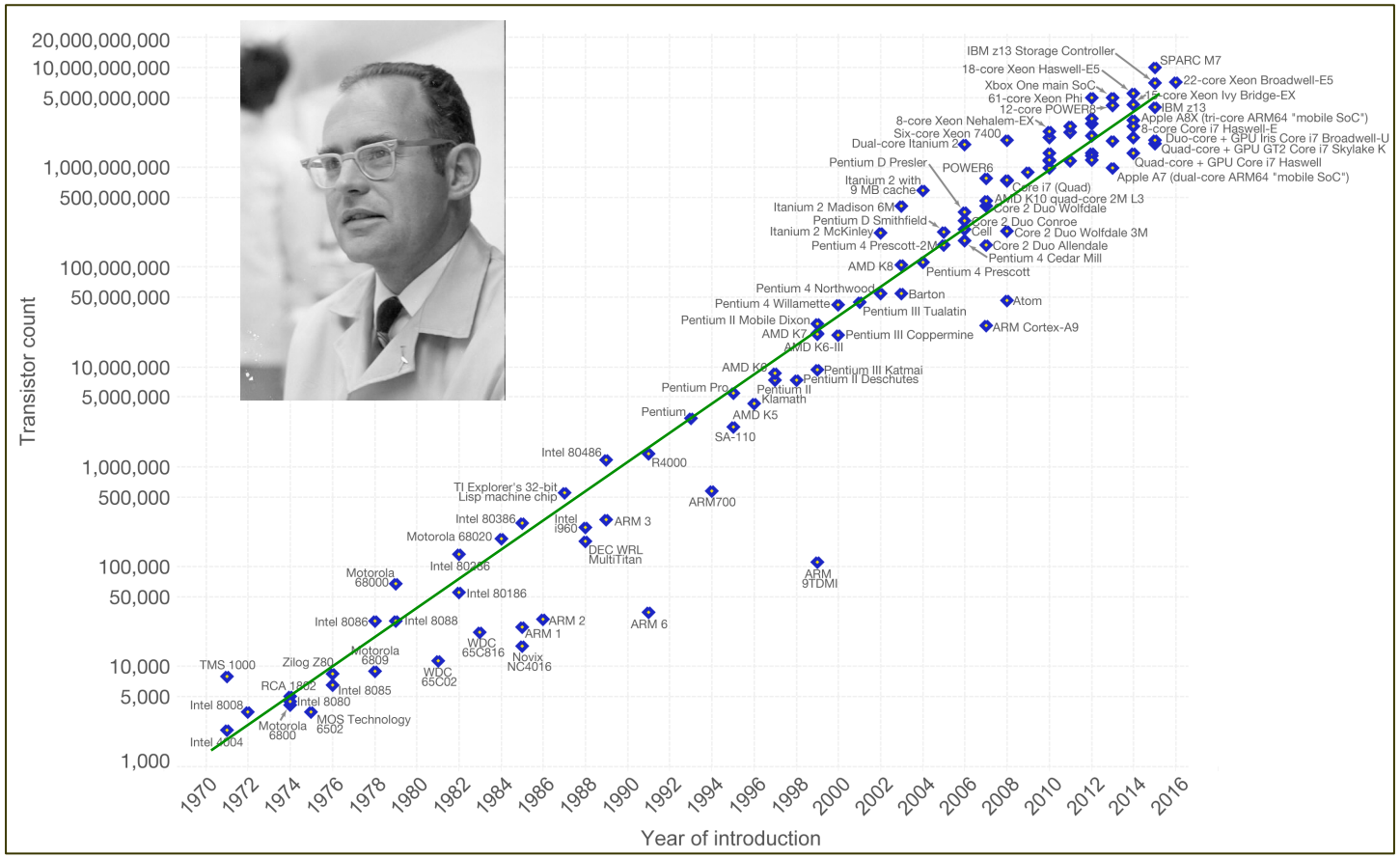
Moore's Law – transistor count/chip
approx doubles every 2 years



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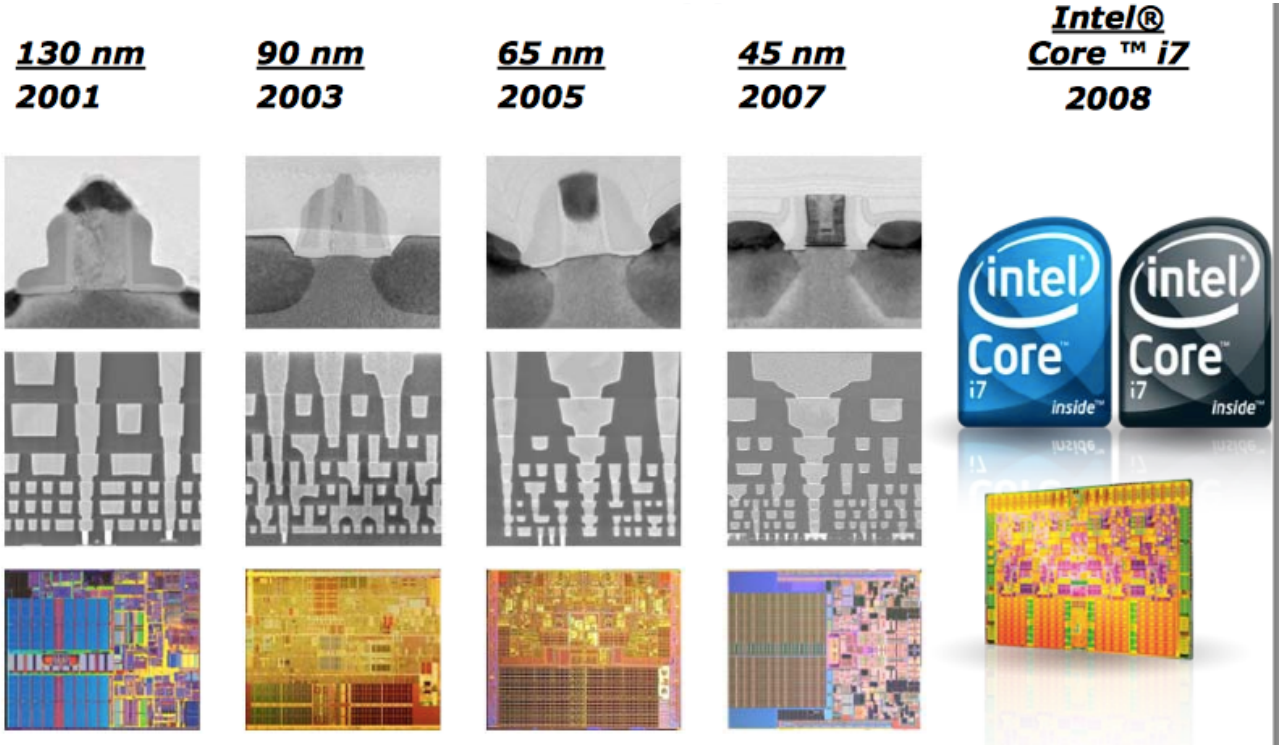
Evolution of the Integrated Circuit



- Latest technology is 45nm gates
- Next is 32nm gates

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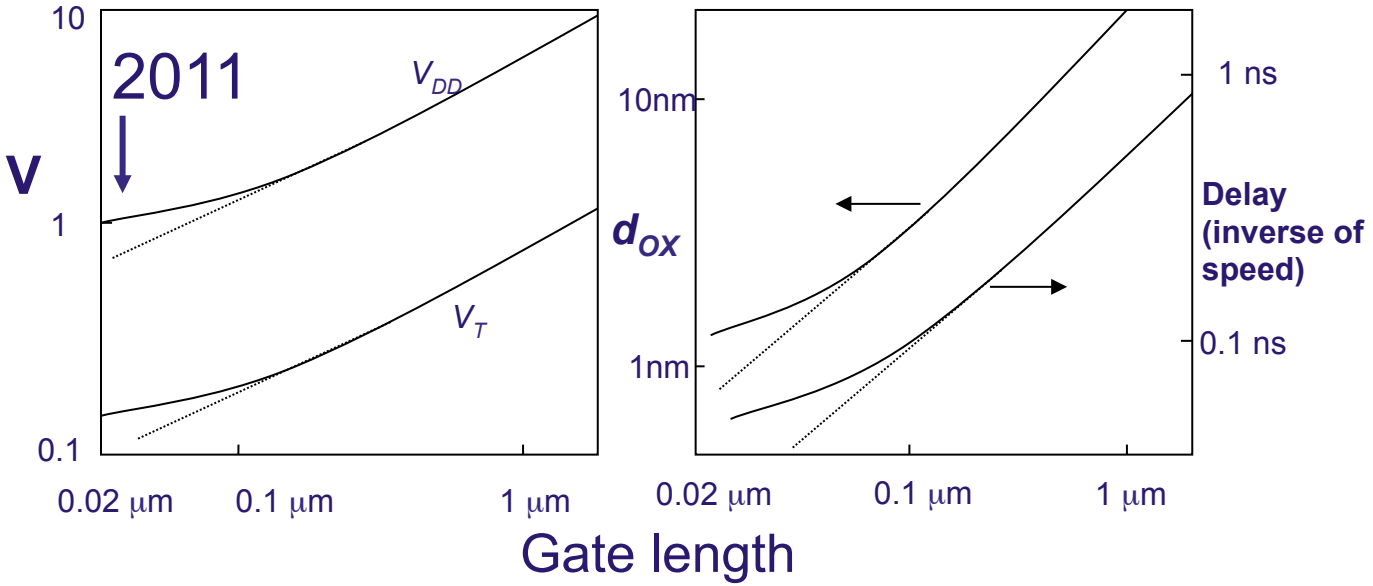
Problems in Maintaining Scaling



- Need some voltage to operate
- Thin oxide allows electrons to 'tunnel' through the gate – high gate leakage current
- Cannot reduce beyond atomic scale!

Summary

- CMOS allows a low power and high speed technology that can be scaled in Very Large Scale Integration (VLSI) processes on Silicon wafers

- Scaling has allowed doubling of transistor count every 2 years for 50 years

- Limits of Moore's law being reached as gate length is reduced to only a few nanometers

- Finding solutions to this problem is the major challenge in electronics

- The next phase of electronics may be in your hands!