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EEE331 Analogue Electronics

2nd lecture:

- Miller transformation
- single transistor circuit elements:
  - common emitter
  - common base
  - emitter follower

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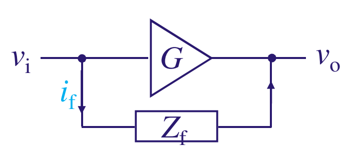
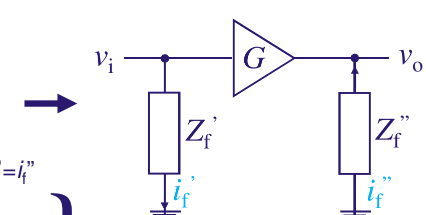
Miller transformation: definition

- problem: amplifier circuits with feedback elements are quite difficult to solve
- solution: **convert feedback circuit into separate input and output circuits** that are easier to solve & give better understanding of high-frequency behaviour
- example: amplifier with **gain $G=v_o/v_i$** and **feedback impedance $Z_f=(v_i-v_o)/i_f$:**





must have same currents: $i_f = i_f' = i_f''$
with $i_f = (v_i - v_o)/Z_f = v_i(1-G)/Z_f$
and $i_f' = v_i/Z_f'$
and $i_f'' = v_o/Z_f''$

$$\boxed{Z_f' = Z_f/(1-G)},\ \boxed{Z_f'' = Z_f\, G/(1-G)}$$

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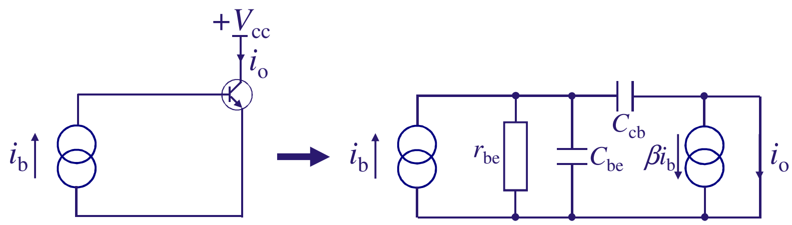
Miller transformation: example

- problem: small signal frequency response of BJT



- use hybrid π model (sometimes also called Giacolleto model)
- driven by an ideal current source, hence r_{bb}=0 has no effect
- load impedance on collector is zero, hence r_{cb} and r_{ce} can be omitted
- without load, any voltage change at input will cause no change in output voltage, hence ***G*=0 without load**

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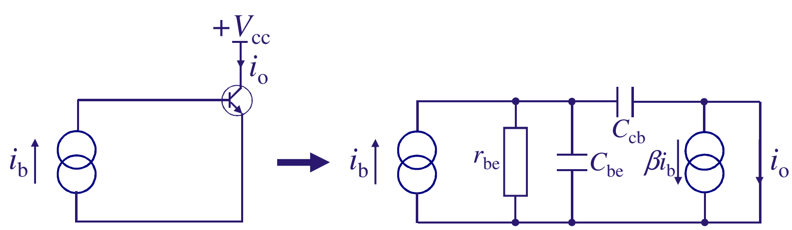
Miller transformation: example

- problem: small signal frequency response of BJT



- identify feedback elements between input and output: C_{cb}
- remember: we derived **Miller transformation for impedance *Z***, hence for a capacitor this means we have to use $1/(j\omega C)$, which e.g. on the input side becomes $1/[j\omega C(1-G)]$.
- so, for input side: $C_{cb}' = C_{cb}(1-G)$
- and for output side: $C_{cb}'' = C_{cb}(G-1)/G$

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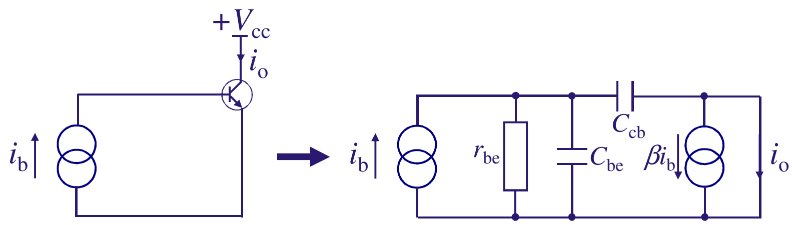
Miller transformation: example

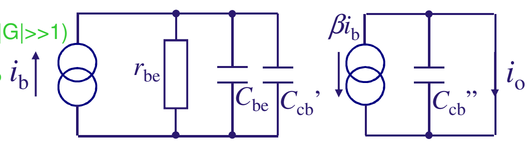
- problem: small signal frequency response of BJT



distinguish between 2 cases:

without load (G=0) or with load (|G|>>1)

- at input: $C_{cb}' = C_{cb}$ $C_{cb}' \approx -GC_{cb}$
- at output: $C_{cb}'' = \infty$ $C_{cb}'' \approx C_{cb}$



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Miller transformation: explains small-signal frequency response of BJT

- for low frequencies $f \approx 0$, the base current flows as i_{br} (i_{bx}=0), hence we have $\boxed{\beta_0 = \beta(f=0) = -i_o(0)/i_b(0) = -i_o/i_{br}}$
- for high frequencies:

  consider voltage across parallel combination of resistor and capacitors:

  $i_{br} r_{be} = v_{be} = i_{bx} Z_{cap} = i_{bx} / [j\omega(C_{be}+C_{cb})]$

  use Kirchhoff's Law for currents:

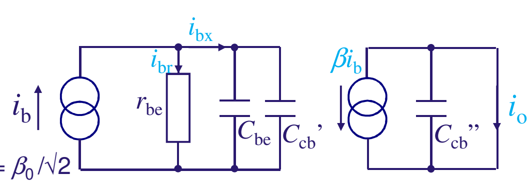
  $i_b = i_{br} + i_{bx} = i_{br}\,[1 + r_{be}\, j\omega(C_{be}+C_{cb})]$, thus

  get frequency-dependent gain

  $$\beta(f) = -i_o(f)/i_b(f) = \frac{\overbrace{-i_o/i_{br}}^{\beta_0}}{[1+j\omega \underbrace{r_{be}\,(C_{be}+C_{cb})}_{\omega_{cut\text{-}off}^{-1}}]}$$

  with **transition frequency**

  $\boxed{f_t = \frac{|\beta_0|\omega_{cut\text{-}off}}{2\pi}}$ so that $\beta(f_t) = \beta_0/\sqrt{2}$



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Miller transformation: explains small-signal frequency response of BJT

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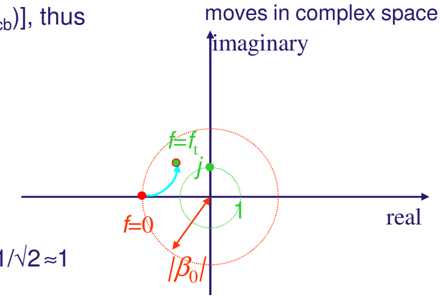
get frequency-dependent gain

$$\boxed{\beta(f) = -i_o(f)/i_b(f)} = \boxed{\frac{\overbrace{-i_o/i_{br}}^{\beta_0}}{[1+j\omega\underbrace{r_{be}\,(C_{be}+C_{cb})}_{\omega_{cut\text{-}off}^{-1}}]}}$$

with **transition frequency**

$\boxed{f_t = \frac{|\beta_0|\,\omega_{cut\text{-}off}}{2\pi}}$ so that $|\beta(f_t)| = 1/\sqrt{2} \approx 1$

$\beta(\omega) = -|\beta_0| / (1 + j\omega/\omega_{cut\text{-}off})$ moves in complex space



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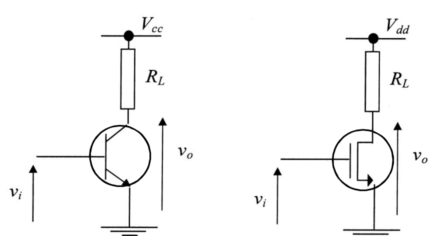
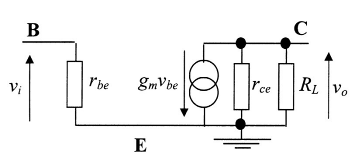
Single transistor circuits: common emitter, common base, emitter follower

1. common emitter (BJT) [common source (MOSFET)]



Common emitter Common source



general method to determine input (output) impedance r_i (r_o):

- draw small signal circuit for $r_{bb}\to 0$, $r_{cb}\to\infty$
- shorten other side to ground
- apply voltage or current to input (output)
- calculate resulting current or voltage

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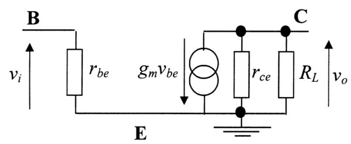
1. **common emitter (BJT)**



basic impedances here:

$r_i = r_{be}$

$r_o = [1/r_{ce} + 1/R_L]^{-1} = r_{ce}R_L/(r_{ce}+R_L)$ (in parallel)

$\approx R_L$ for small load resistor R_L

(**not** for current source!)

calculation of voltage gain:

consider output voltage: $v_o = -g_m v_{be}\, r_{ce}R_L/(r_{ce}+R_L)$, thus

voltage gain: $v_o/v_i = v_o/v_{be} = -g_m\, r_{ce}R_L/(r_{ce}+R_L) \approx -g_m R_L$ for small loads R_L, i.e. the voltage gain is high and controlled by the load R_L. This is relevant for voltage gain stages in OpAmps.

common source (MOSFET) *$r_i \to \infty$ (gate capacitance is open circuit at dc) High input resistance makes MOSFET particularly attractive as input stages of OpAmps!*

$r_o = r_{ds}R_L/(r_{ds}+R_L) \approx R_L$ (as above)

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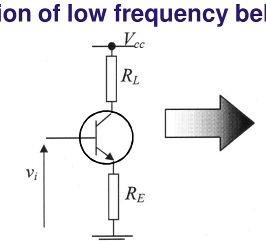
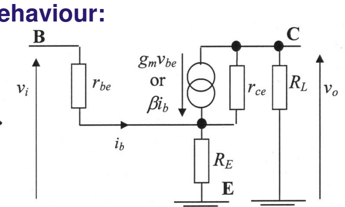
1. **common emitter (BJT)**

emitter degeneration: additional impedance between emitter and ground

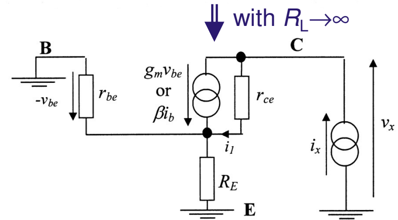
calculation of low frequency behaviour:





dc s.s. equivalent circuit

with $R_L \to \infty$



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1. **common emitter (BJT)**

emitter degeneration: additional impedance between emitter and ground

calculation of low frequency impedance:

consider current: $i_1 = i_x - g_m v_{be}$ with voltage $-v_{be} = i_x\, r_{be} R_E/(r_{be}+R_E)$

$= i_x + g_m\, i_x\, r_{be} R_E/(r_{be}+R_E)$

output voltage: $v_x = -v_{be} + i_1\, r_{ce}$

$= i_x\, r_{be} R_E/(r_{be}+R_E) + [i_x + g_m\, i_x\, r_{be} R_E/(r_{be}+R_E)]\, r_{ce}$

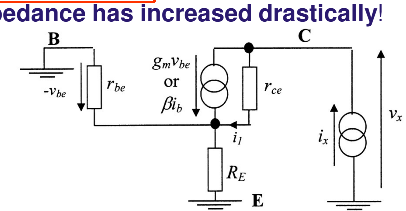
$= i_x\, \{r_{be} R_E/(r_{be}+R_E) + r_{ce}\, [1+g_m\, r_{be} R_E/(r_{be}+R_E)]\}$

impedance: $\boxed{v_x/i_x = r_{be} R_E/(r_{be}+R_E) + r_{ce}\, [1+g_m\, r_{be} R_E/(r_{be}+R_E)]}$

$\boxed{\approx r_{ce}\, [1+g_m\, r_{be} R_E/(r_{be}+R_E)]}$ (for large g_m)

output impedance has increased drastically!

note:
voltage across R_E limits v_{be}, hence also i_b and i_c: emitter degenerated circuits are important for design of high impedance loads!



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1. **common emitter (BJT)**

emitter degeneration: additional impedance between emitter and ground

calculation of low frequency transconductance:

input voltage: $v_i = i_b r_{be} + (i_b + \beta i_b) R_E$ with $r_{be} = v_{be}/i_b = g_m v_{be}/g_m i_b = \beta/g_m$

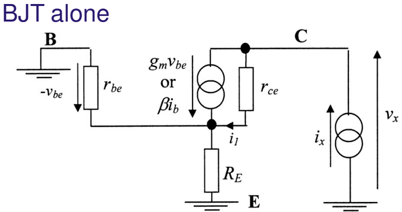
$= i_c\, [1/g_m + R_E(1+1/\beta)]$

transconductance:

$\boxed{i_c/v_i = 1/\, [1/g_m + R_E/(1+1/\beta)]}$

$\boxed{\approx g_m/(1+g_m R_E)]}$ (since $\beta \gg 1$)

transconductance $dI_c/dV_{be}\,|\,V_{ce=\mathrm{const.}}$ **is reduced by a factor** $(1+g_m R_E)$, i.e. for the CE circuit with R_E it is lower than for the BJT alone



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note for common source (MOSFET):

source degeneration is less common than emitter generation because

- *g_m is low anyway, and further reduction is undesirable*
- *rising input impedance would be pointless as $R_i \rightarrow \infty$ anyway*
- *rising output impedance generally is beneficial for creating high impedance load but adverse if we are trying to build an output stage (which would require a low output impedance).*

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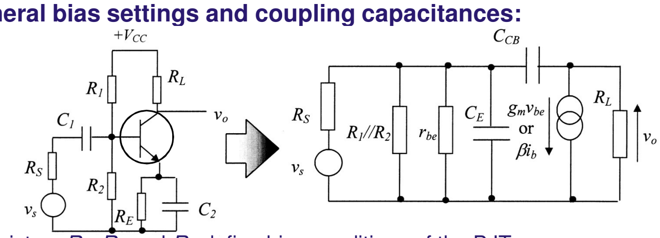
1. common emitter (BJT)

general bias settings and coupling capacitances:



- resistors R_1, R_2 and R_E define bias conditions of the BJT
- R_1 and R_2 are connected to a constant voltage and so, from a small signal point of view, appear to be in parallel
- $r_{bb} << R_S$ (in series) and $r_{ce} >> R_L$ (in parallel) can both be ignored
- capacitor C_1 is a bypass capacitor that transmits the time-varying v_s to the base of the BJT without disturbing the dc bias conditions
- capacitor C_2 is another bypass capacitor; it effectively compensates the negative feedback provided by R_E, thereby increasing gain
- at high frequencies, C_{CB} and C_E cannot be ignored.
- with voltage gain $G=v_o/v_{be}$, **C_{CB} becomes the target for the Miller transformation**

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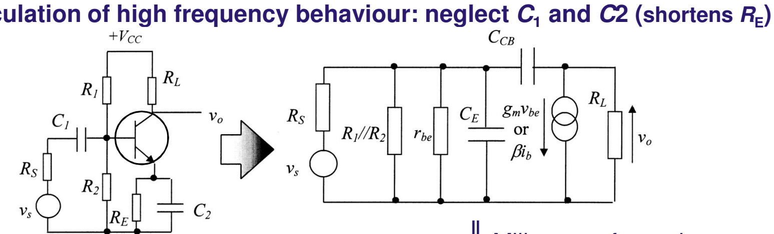
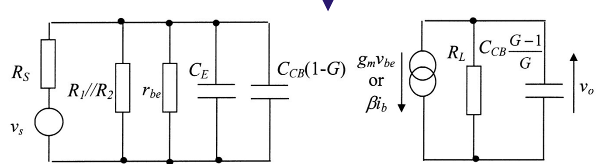
1. common emitter (BJT)

calculation of high frequency behaviour: neglect C_1 and $C2$ (shortens R_E)



Miller transformation



problem: circuit is 2nd order, with poles both on input and on output side: which limits the high frequency behaviour?

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1. common emitter (BJT)

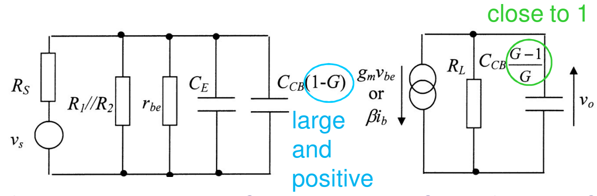
calculation of high frequency behaviour:

assumption: input circuit is frequency limiting, i.e. $f_i \ll f_o$ assumed
then: $C_{CB}\,(G-1)/G$ negligible
output voltage: $v_o \approx -g_m v_{be}\,R_L$
high-f voltage gain: $\boxed{G_{hf} = v_o/v_{be} = -g_m R_L}$ is large and negative
corner frequencies:

$$\boxed{\begin{aligned} f_i &= [2\pi\,(R_S\,//\,R_1\,//R_2\,//r_{be})(C_E + C_{CB}(1-G))]^{-1} \\ f_o &= [2\pi\,R_L\,C_{CB}\,((G-1)/G)]^{-1}\end{aligned}}$$

where // means parallel connection and $\omega = 1/R_{eff}C_{eff}$

close to 1



large and positive

NBs: impedance of capacitor is $Z_c = 1/(j\omega C)$, hence $\omega = 1/RC$ and $f = 1/(2\pi RC)$
Always check assumption that $f_i \ll f_o$ after calculation!

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1. **common emitter (BJT)**

calculation of mid frequency behaviour:

assumption: C_1 and C_2 are still short circuits, but C_{CB} and C_E open
then: C_{CB} $(G-1)/G$ negligible
output voltage: $v_o \approx -g_m v_{be} R_L$
mid-f voltage gain: $\boxed{G_{mf} = v_o/v_i = -g_m R_L (R_1 // R_2 // r_{be})/(R_S + R_1 // R_2 // r_{be})}$

NBs: Miller effect describes the apparent increase of C_{CB} by factor $(1-G)$, which reduces the corner frequency. **Dominant pole compensation** means that in practice extra capacitance is often added between base and collector of BJTs of multi-transistor amplifier stages such as OpAmps to separate the pole frequencies due to the different stages, thereby avoiding instabilities and ensuring stable operation.

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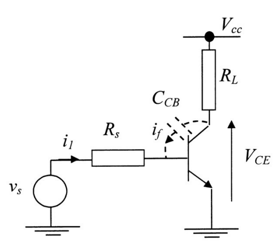
1. **common emitter (BJT) / [common source (MOSFET)]**

slew rate limiting:

For **large** input signals, the rate of change of V_{CE} is dominated by the availability of the base drive current. Consider I=dQ/dt=d(CV)/dt =C dV/dt *[in analogy, for a power MOSFET the rate of change of drain voltage is governed by the availability of gate drive current].*



consider BJT drive on process:
v_s= 0 for t<0, V_1 for $t \geq 0$
current to base for $t \geq 0$: $I_1 = (V_1 - V_{BE})/R_S$
current to collector for $t \geq 0$: $I_f = C_{CB}\, dV_{CE}/dt$
Rate of change at output is maximum when all the base current available is utilised by capacitor, i.e. $I_f + I_B = 0$, thus

$$\boxed{dV_{CE}/dt\,|_{max\text{-}on} = I_f/C_{CB} = -I_B/C_{CB} = -(V_1 - V_{BE})/(R_S C_{CB})}$$ lags behind

and correspondingly

$$\boxed{dV_{CE}/dt\,|_{max\text{-}off} = V_{BE}/(R_S C_{CB})}$$ leads

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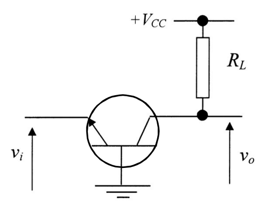
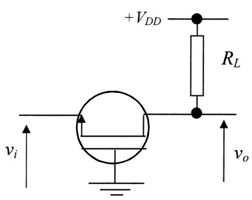
2. common base (BJT) / [common gate (MOSFET)]



Common base



Common gate

voltage gain: $G = g_m R_L$

current gain: $i_o/i_i = 1/(1+1/G)$ (i.e. <1: **no current gain**, as $I_C \leq I_E$)

advantages: 1. C_{CB} does not cause high frequency feedback: ideal for **fast switches** (no Miller effect as $I_C \approx I_E$)

2. for large R_L, output impedance is higher than in CE mode, i.e. use as current source

derivation: cf section 3.3.3 in Gray's textbook

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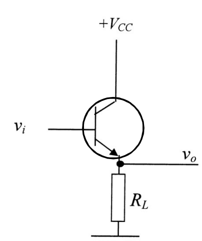
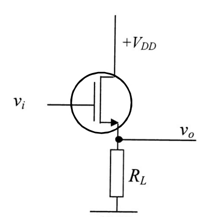
3. common collector = emitter follower (BJT) / [common drain (MOSFET)]



Common collector



Common drain

use Kirchoff's law at output node: $(v_i - v_o)/r_{be} + \beta(v_i - v_o)/r_{be} - v_o/R_L = 0$, thus

voltage gain: $\boxed{G = v_o/v_i = R_L(1+\beta)/[r_{be} + R_L(1+\beta)] = 1/[1 + r_{be}/(\beta+1)R_L] \approx g_m R_L/(1+g_m R_L) \cong 1}$

Note: The gain is usually just less than unity, so the emitter follows the input voltage (hence the name emitter follower). These circuits have high input impedance and low output impedance and are useful for **buffers**.