Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (3.0 hours)

EEE119 Digital System Engineering 1

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. i) Explain with the aid of a truth table and state diagram, the function of a D-type flip-flop. **(3)**

ii) Explain the term 'self-starting' when applied to counters. **(2)**

b. i) Derive the state transition diagram and state table for a synchronous binary counter with the following properties. When its input $X = 0$, the counter will count in the sequence 0, 1, 3 and repeat. When $X = 1$, the counter will count in the sequence 1, 2, 3 and repeat. Ensure that the counter is self-starting and clearly indicate how you have achieved this. **(6)**

ii) Derive the simplest equations that you can for the counter in part **(i)** as a sum-of-products and show how the circuit could be implemented using two D-type flip-flops and some logic gates. **(5)**

iii) What is the theoretical maximum frequency of operation for the counter that you have designed? You may assume the following properties. Propagation delay of any logic gate is 7ns, propagation delay of an inverter is 0ns, propagation delay of a flip-flop is 5ns and the data set-up time for a flip-flop is 1ns. **(2)**

iv) In practice, you exceed the frequency obtained in part **(iii)** and the circuit fails. Briefly describe some of the possible causes of the failure. **(2)**

2. **a.** Explain, with the aid of a truth table, the function of:

i) 2-to-1 logic multiplexer. **(3)**

ii) 2-to-4 line decoder with active low outputs. **(3)**

b. Show how you could construct an 8-to-1 logic multiplexer using only 2-to-1 logic multiplexers. Explain briefly how your circuit operates. **(4)**

c. Show how the Boolean function F, described by the maxterm list

$F(A,B,C,D) = \Pi\ (0,2,5,6,7,8,9,10)$ can be implemented using:

i) 8-to-1 multiplexer and logic inverters. **(5)**

ii) 4-to-16 line decoder with active low outputs and an additional logic gate. **(5)**

3. **a.** Simplify the following Boolean expressions as much as you can.

(A' represents NOT A)

i) (X + Y).(X + Z)

ii) A.B.C + A'.B + A.B.C' **(4)**

b. Briefly explain the difference between:

i) Mealy and Moore finite state machines.

ii) Binary and 'one-hot' encoding.

iii) Resetting and Non-Resetting behaviour. **(6)**

c. A Moore type state machine is required that can recognize certain sequences on its serial input line. It has a single bit output **Z** and a single bit input **I** which receives the serial input sequence. The circuit will recognize all of the input sequences that have three or more consecutive 1s, or three or more consecutive 0s and respond by setting **Z** = 1. It should not reset after finding a valid sequence.

Draw a state diagram for this system and a state transition table, clearly labelling the states. A circuit implementation and next state equations are **not** required. **(10)**

4. **a.** Write down De Morgan's theorems for two variables and prove them by truth table. **(6)**

b. Using two simple switches marked A and B (each having two positions labelled as logic 0 or 1) together with a lamp and a battery only, draw a circuit which performs a 2-input NAND function (i.e. the circuit lights the lamp only when A NAND B is true). **(4)**

c. Show how an SR latch can be formed from two cross-coupled NOR gates. With the aid of a characteristic table, describe the function of this circuit and any requirements for correct operation. **(5)**

d. A new type of latch is required that has the following properties. There are two inputs A and B, there are two outputs Q and its inverse Q'. If A = B = 0, the latch should be reset (Q = 0). If A = B = 1, the latch should be set (Q=1). The output of the new latch should remain unchanged if A and B differ. Show how the latch could be implemented using the SR latch in part (c) and some additional logic gates. **(5)**

NJP / MPF