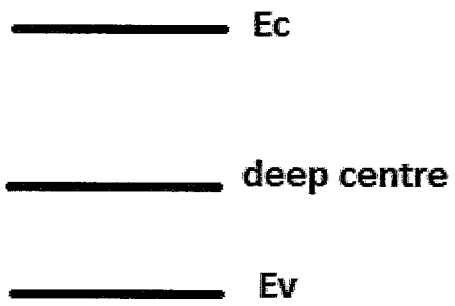
Solutions to EEE6042 2013-14.

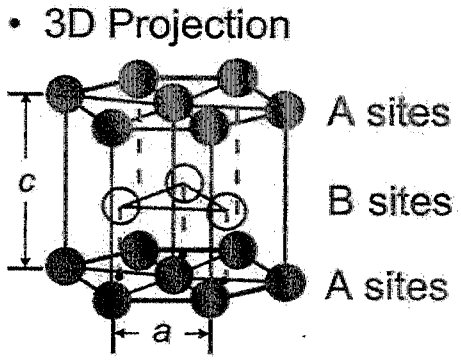
1a: Ionisation energy is the energy required for an atom to donate a free electron or hole to the crystal.



A deep state as opposed to a shallow state is closer to the centre of the bandgap

1b

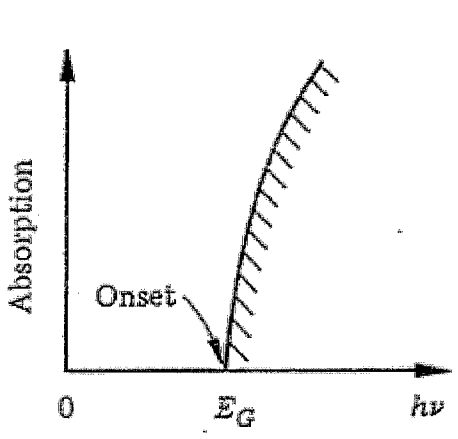
Wurtzite structure shown in diagram below

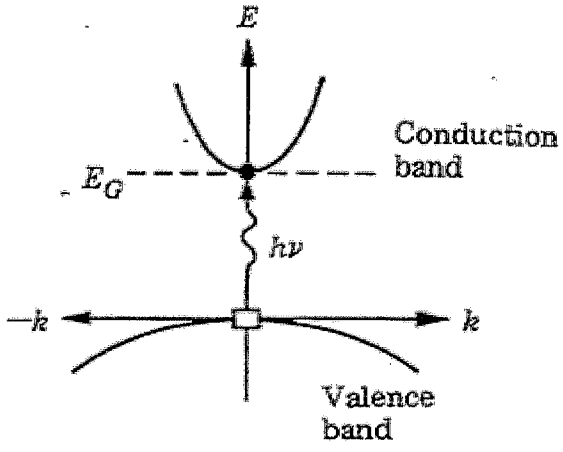


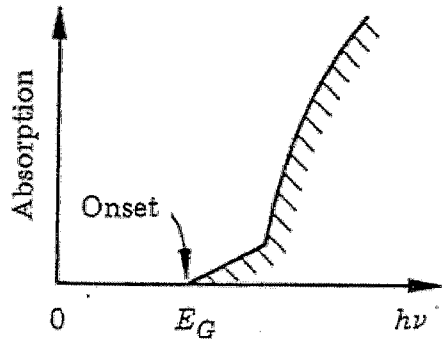
Two semiconductors which are wurtsite GaN, CdS.

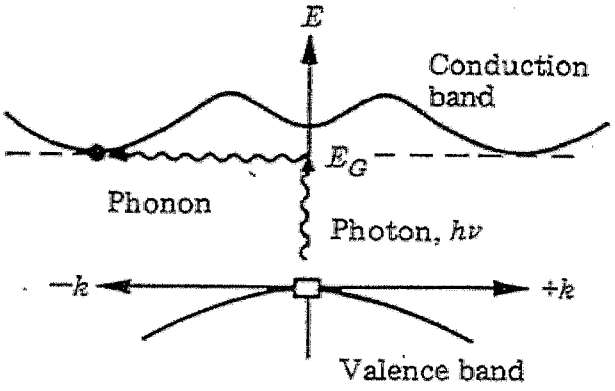
Polar: Yes, stacking ABAB as shown in the figure above.

1c. Energy versus momentum of carriers which shows the bandstructure of the material.

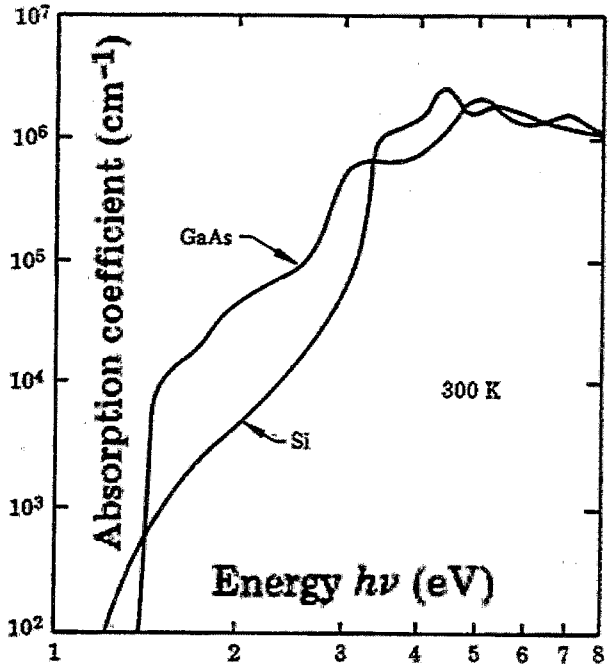








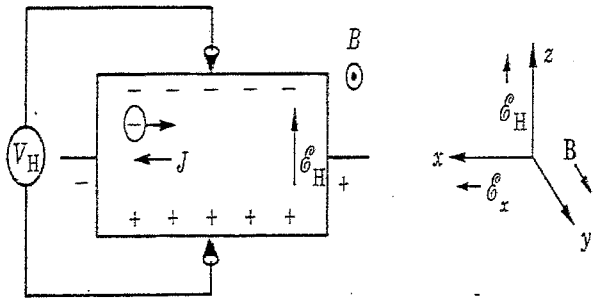
Direct and indirect bandgap materials identified by a response of the absorption spectra as shown in the diagrams.



1d. Resistivity of a metal decreases with temperature, for a semiconductor it increases with temperature.

Two methods: Four point probe and van der paw.

1e Hall effect

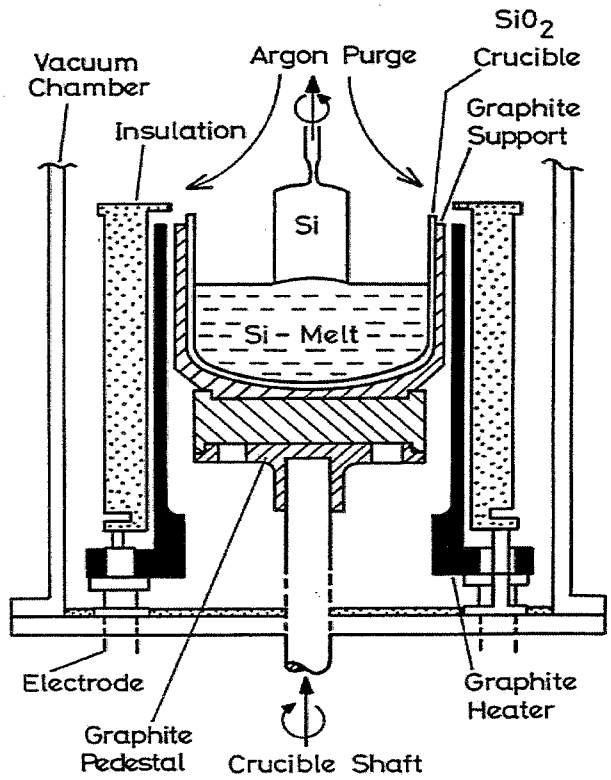


A semiconductor bar carrying a current (voltage V_x along length L_x) perpendicular to a magnetic field (B_y) develops a voltage (the *Hall voltage* V_H) at right angles to both across the width of the bar (L_z) . The Hall effect allows for an *independent measure of mobility,* since it can be shown that:

The Sign of V_H distinguishes the type of charge carrier, i.e. electrons or holes

If. Concentration of the impurity increases along the crystal due to increase in concentration of dopants remaining in the melt (Scheils equation). $C_S = k_0 C_0 (1-x)^{k_0 - 1}$

Q2.a: Differences between Cz and Fz (**any 3 of the points highlighted below in colour code 3 marks each + 3 marks diagram**).



CZ technique

1.**Method.** Small, polycrystalline Si particles are placed in a silica crucible, crucible put in resistance-heated, vertical furnace, furnace flushed with low pressure inert argon gas. The Polysi melt is seeded

with a crystal which is dipped in the centre of the melt and temperature slowly reduced, withdrawing the seed. The seed nucleates as a solid single crystal ingot.

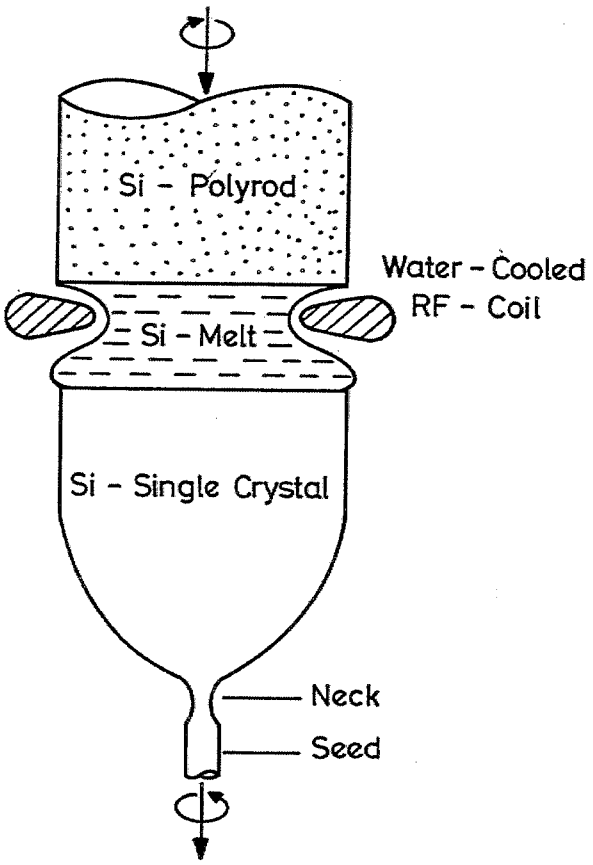
2. **Size** of a CZ crystal is large typically 100kgx1mlong x 0.3m diameter.

3. Principle **contaminant** is Oxygen <100ppm as melt attacks the crucible.

4. Control of growth in this zero dislocation technique is via control of seed and crucible rotation rates, temperature gradients and melt convective flow.

5. **The cost** is lower than FZ.

FZ technique.



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1. Method consists of moving a polycrystalline Si rod through short RF heater to melt the zone inside the RF coil (needle eye), resulting in single crystal solidification onto a seed.
2. Crucible free technique gives very low oxygen concentration.
3. control of molten zone difficult: Floating Zone crystals smaller than CZ crystals
4. Floating Zone Si is less important than CZ Si and is more expensive

Q2b.

The CVD technique is used to deposit many electronic materials: especially important is the deposition of elemental Si (Key features highlighted below).

Several reaction types are possible, involving Si-containing gases flowing over a heated substrate

Importantly, heated silicon tetrachloride surface is reduced by hydrogen to silicon

$SiCl_4 + 2H_2 \rightarrow Si + 4HCl$ (Reaction 1 mark)

Deposited Si atoms migrate over substrate, to join steps at the edges of growing crystal planes, extending across the surface, deposition temperatuure range from ~800 -1200 Cs, with deposition rates ~0.01 - 5μm/min, forms highly uniform single crystal Si layers

Doping of grown layers is achieved by mixing a suitable hydride with the flowing hydrogen and $SiCl_4$ gases (Arsine or phosphine for n and diborane for ptype)

- must be careful to avoid so-called autodoping
- Residual contamination leads to stacking faults, non-uniform heating to slip and dislocation.

MOCVD

This is typically used to grow epitaxial layer structures of III-V (and II-VI) compounds

Hydrogen high purity carrier gas passes through the reactor, transporting the reagent gases (organic) which it contains over the substrate, all regulated with MFCs in a gas switching matrix. Reagent materials pyrolyse on heated substrate. The precursors should have high volatility, low tendency to decompose homogeneously and should be available in high purity (no carbon). Oxygen (present in alcholhols ethers) is usually a problem.

layer growth takes place at either atmospheric pressure or low pressure (perhaps ~ 150torr).

Key reaction for GaAs (1 mark)

$$Ga(CH_3)_3 + AsH_3 \sim GaAs + 3CH_4$$

Key differences: CVD primarily used to grow Si by reduction of silicon containing compound at temperatures 800-1200C, MOCVD used to grow III-V and II-VI compounds using organic precursors which have high volatility (hence lower temperature) and pyrolyse over the substrate.

6 marks for description, 3 for each technique + 1 mark each for equations.

Q2c: 30*Co=0.3C0(1-x)^0.3-1; k0=0.3

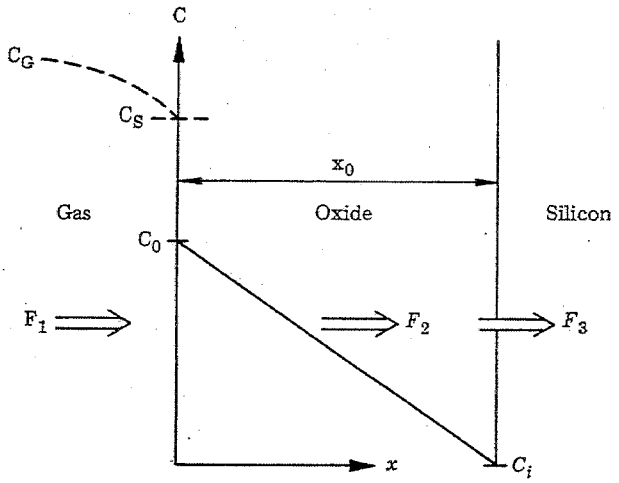
Gives -2/0.7=log(1-x)

Gives x=1-0.00141=0.99859. **6 marks**

Q3a: Wet and dry oxidation

Dry oxidation is thermal oxidation with dry oxygen gas, $\mathbf{Si + O_2 = Si0_2}$

Oxidation with steam ***(wet oxidation)*** - a faster proces $\mathbf{Si + 2H_2O = Si0_2 + 2H_2}$ **1 mark**



1 mark diagram

The reaction kinetics involves ***three steps*** in the oxidation process; the oxidising species is ***transported*** from the bulk of the gas to the oxide/ gas interface

flux = $h_G (C_G - C_S)$ [h_G is mass- -transfer coefficient]

The oxidising species diffuses across the oxide layer already present

flux = $D (C_o - C_i)/Xo$ [D is the diffusivity in oxide]

The oxidising species reacts with the **Si** at the oxide/**Si** interface

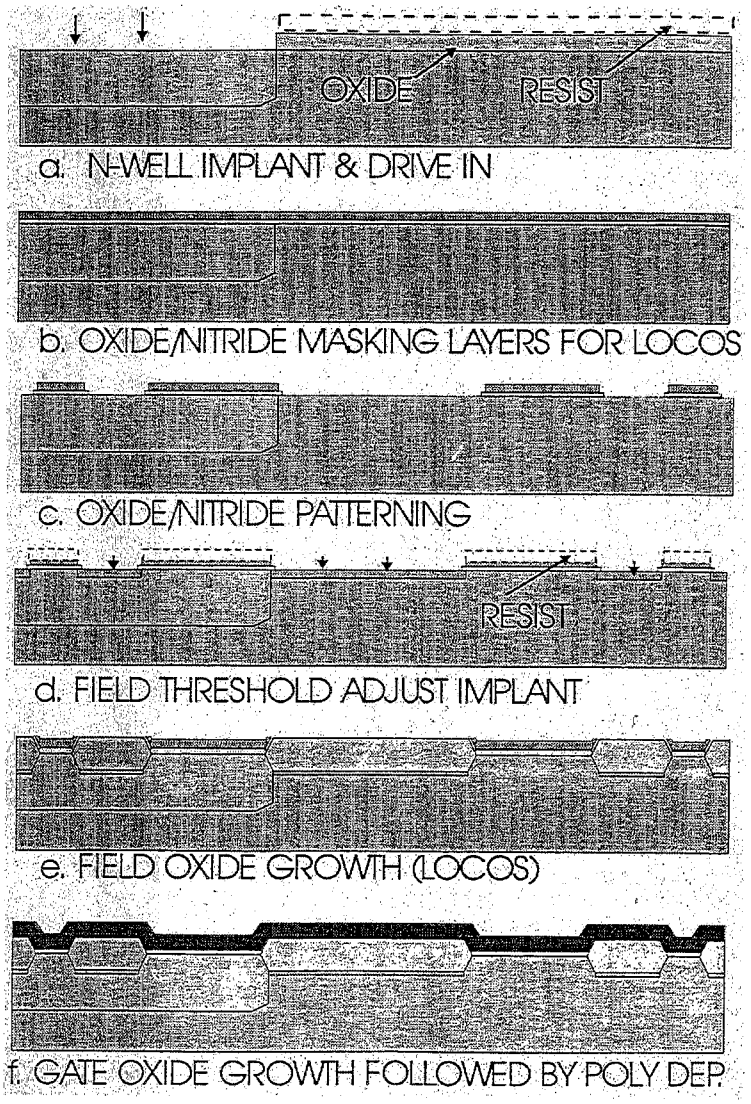
flux = $k_S C_j$ [k_S is reaction rate constant] **2 marks**

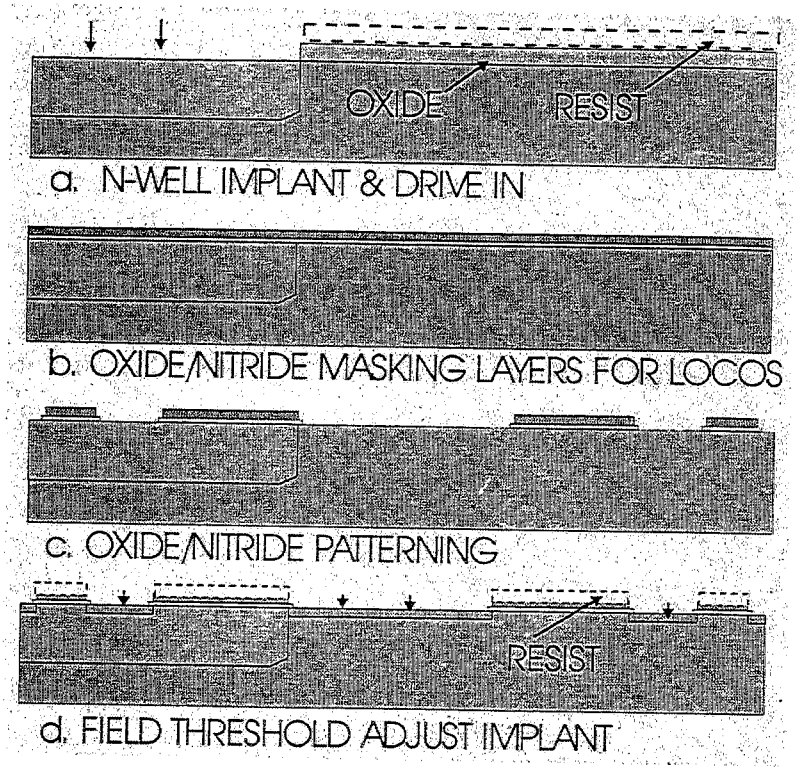
High concentrations of **B** or **P** in the **Si** cause both the linear and parabolic reaction rates to *increase,* probably by different mechanisms

Presence of **HCl** (giving $\mathbf{Cl_2}$ by reaction $\mathbf{2HCl + 1/2O_2 = H_2O + C1_2}$) also *increases* the reaction rates

1 mark

Q3b.CMOS steps (with diagrams).


OXIDE
RESIST
a. N-WELL IMPLANT & DRIVE IN
b. OXIDE/NITRIDE MASKING LAYERS FOR LOCOS
c. OXIDE/NITRIDE PATTERNING
RESIST
d. FIELD THRESHOLD ADJUST IMPLANT
e. FIELD OXIDE GROWTH (LOCOS)
f. GATE OXIDE GROWTH FOLLOWED BY POLY DEP.


OXIDE
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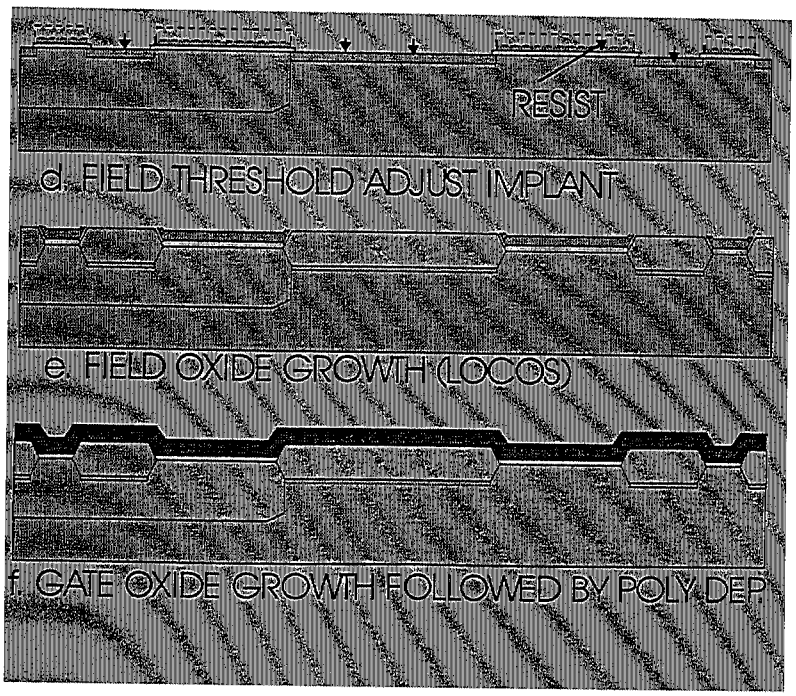
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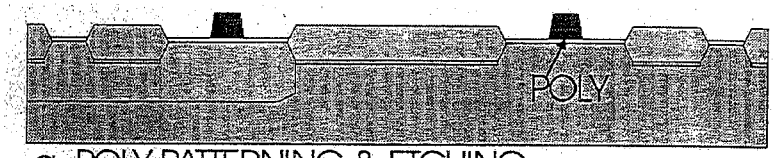
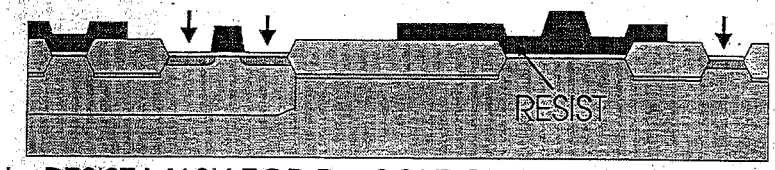
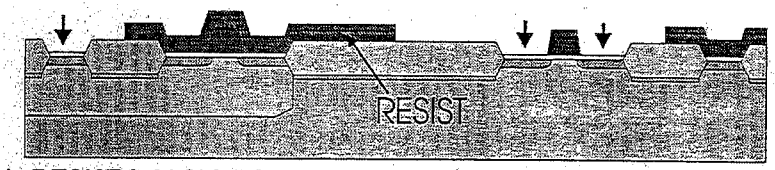


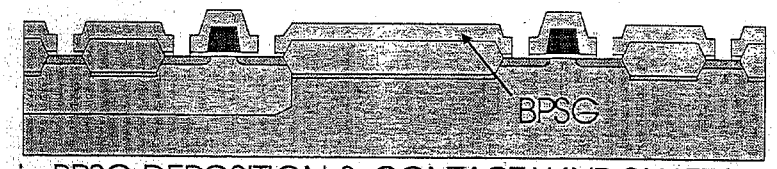
g. POLY PATTERNING & ETCHING



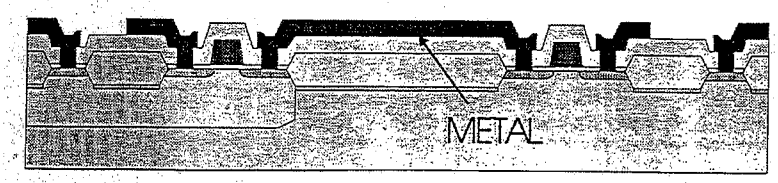
h. RESIST MASK FOR P+ SOURCE & DRAIN IMPLANT



i. RESIST MASK FOR N+ SOURCE & DRAIN IMPLANT



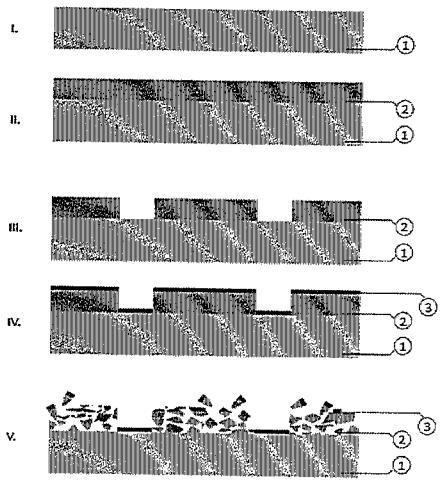
j. .BPSG DEPOSITION & CONTACT WINDOW ETCH



k. METAL DEPOSITION AND ETCH

N Well implant and drive in; Oxide/nitride masking layers for LOCOS; oxide nitride patterning, ield threshold adjust implant, field oxide growth (locos);gate oxide growth and poly deposition;poly patterning and etching;resist mask and p+ source and drain implants (B),resist mask and n+ source and drain implants (As);BPSG deposition and contact window mask and etch, metal deposition and etch. (10)- ***of which 3 marks for getting the sequence correct, 3 marks for diagrams and 4 for content.***

Q3c.



3marks

The lift off technique consists of depositing a PhotoResist (2) on a substrate (1), the PR is developed to show regions where the metal (3) is required. Metal is deposited on the entire wafer, and the PR is etched off, taking metal on the top along with it. This only leaves the metal in the desired locations.
2 marks

Q4a

Diffusion coefficient (D) = D_0 exp –[E_A/kT]
At 1250°C (1523K) D = 0.76 x exp –[3.46/(8.61 x 10^{-5} x 1523)] cm^2/s
= 0.76 x exp –[26.3859] cm2/s
=2.63975x$10^{-12}$$cm^2/s$
For 60seconds 2√(Dt) = 2√(2.63975x10-^{12} x 60) cm
= 2.517x10^{-5} cm.

=0.25 microns

Then autodoping is not a problem for a growth rate of 0.5micron/min

Q4b.

External gettering is achieved by applying treatment to the back of a silicon wafer by a range of techniques:

1. application of carefully-controlled ***abrasion damage*** (wafers often supplied pretreated)
    - impurities are trapped at general defects by precipitation
2. deposition of a layer of ***polySi***
    1. impurities are trapped at grain boundary defects by precipitation
3. ***implantation*** of a high dose of *inert gas ions* and recrystallization of the layer to give ***polySi*** and inert gas bubbles
    1. impurities are trapped at grain boundary defects and internal bubble surfaces by precipitation
4. diffusion into the **Si** of a ***high concentration of phosphorus*** dopant

1. impurities are trapped at accompanying misfit dislocations by precipitation and, also, within the **Si** lattice by solubility enhancement due to the presence of the phosphorous

Q4c:

The five requirements are

i)silicon substrate, ii)good interface with oxide, iii)good bandoffset of dielectric with carriers, iv)higher mobility than silicon,v) low temperature processing.