**Data Provided: None**

The University Of Sheffield.

**DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING**

**Spring Semester 2013-14 (3.0 hours)**

**EEE118 Electronic Devices & Circuits 1**

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

**You may require the following:**

Electronic charge, e =1.6x10$^{-19}$C

Permittivity of free space, $\varepsilon_0$ = 8.85x10$^{-12}$ Fm$^{-1}$

Boltzmann's constant, k =1.38x10$^{-23}$ JK$^{-1}$

Planck's constant, h = 6.6x10$^{-34}$ Js

Energy of a photon =hc/$\lambda$

Poisson's Equation $\frac{d^2V}{dx^2} = -\frac{ne}{\varepsilon}$

$$E = -\frac{dV}{dx}$$

$$W = \left[\frac{2\varepsilon V_o}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

$$J = eD\frac{dn}{dx}$$

$$J_0 = \frac{eL_e n_p}{\tau_e} + \frac{eL_h p_n}{\tau_h} \quad and \quad J = J_0\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

$n_p p_p = n_n p_n = n_i^2$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \gamma B$$

$$\partial p = \partial p_0 \exp\left(\frac{-x}{L_h}\right)$$

$$L = \sqrt{D\tau}$$

$$\sigma = ne\mu_e + pe\mu_h \qquad \rho = \frac{1}{\sigma}$$

$$C = \frac{\varepsilon A}{d}$$

$$D = \frac{kT}{e}\mu$$

$v = \mu E$

Resistance $R = \rho L/A$

For silicon: relative permittivity $\varepsilon_r$ = 12 built-in voltage = 0.7 V

electron mobility = 0.07 m$^2$/Vs hole mobility = 0.045 m$^2$/Vs

band gap = 1.12 eV

**1.** This question is about diodes and some common circuits that contain diodes.

**a.** The diode in figure 1a has a forward voltage drop of 0.7V but is otherwise ideal.

For the circuit of figure 1a,

**i)** Show that the diode is conducting. (*Hint: Assume it is not conducting, then use circuit analysis to show your assumption is incorrect*). **(4)**

**ii)** Find the forward conduction current through the diode. **(3)**

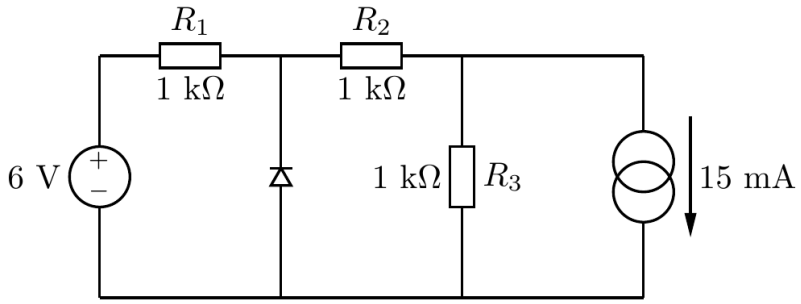


**Figure 1a**

**b.** The circuit in figure 1b is a rectifier circuit which will be used to produce a linear power supply.

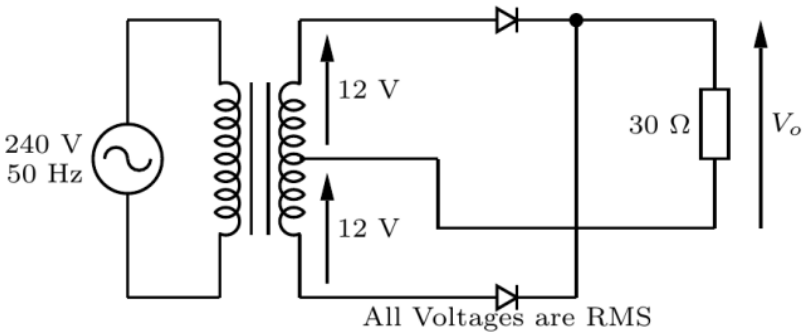


**Figure 1b**

**i)** State what kind of rectifier circuit figure 1b shows. **(1)**

**ii)** Sketch on labelled axes, the load voltage, $V_L$ **(2)**

**iii)** State the peak magnitude and frequency of the current flowing through the load. **(2)**

**iv)** A capacitor is added in parallel with the load to smooth the output voltage. Calculate a suitable value for this capacitor if the output voltage ripple must be less than 2 V peak to peak. Assume the ripple voltage waveform is triangular. **(4)**

**c** The power supply in part 1b is now required to power some measurement circuitry and the output voltage ripple should be reduced using a Zener diode shunt regulator.

The Zener diode has a reverse breakdown voltage of 9 V and requires 4 mA to maintain proper operation. The measurement circuitry requires a minimum of 20 mA in standby mode and a maximum of 500 mA when fully operational.

**i)** Sketch a suitable Zener diode shunt regulator circuit **(2)**

**ii)** Find the largest resistor value which will allow proper regulation. **(3)**

**iii)** Suggest (with calculations) a suitable power rating for the resistor **(2)**

**iv)** Calculate the power dissipated in the diode when the circuit is on standby and when it is fully operational. **(2)**

**2.** **a.** Carefully sketch the I/V characteristic of a p-n junction diode showing both the forward and reverse bias and paying attention to the region around zero bias. Identify the reverse leakage current and the forward dynamic resistance in terms of the I/V slope at any particular bias. **(4)**

How does this resistance vary with forward bias? **(2)**

**b.** A silicon p-n diode forms the emitter-base junction of a p-n-p bipolar transistor and is doped as follows:

$p = 7x10^{25}\ m^{-3}, \quad n = 7x10^{23}\ m^{-3}$

Calculate the emitter injection efficiency. Assume that the current due to each carrier is proportional to the conductivity of the semiconductor from where it originates. **(4)**

Calculate the current gain if the base transport factor, $B = 1$. **(2)**

**c.** Describe the main contributing mechanism which results in the small reverse leakage current in a p-n junction? **(3)**

Would you expect the reverse biased leakage current to increase or decrease:

i. when using a semiconductor with an increased bandgap or bond strength? **(2)**

ii. at a lower diode temperature? **(2)**

**d.** The reverse leakage current in a p-n junction at room temperature is $1 \times 10^{-6}$ A. What applied forward junction voltage will give a current of $1 \times 10^{-2}$ A? In your calculation assume that the exponential term in the diode equation is >> 1. **(4)**

The actual measured voltage across the diode terminals required to give this current is 25 mV higher than the value calculated above. Explain why this happens? **(2)**

**3.** This question is about transistors both as switches and amplifiers.

**a.** Using the information provided in figure 3a find,

**i)** the load current when the transistor has been on for a long time. **(1)**

**ii)** the energy stored in the inductor assuming the transistor has been switched on for a long time. **(1)**

**iii)** the power dissipated in the load. **(1)**

**iv)** the power dissipated in the switch. **(1)**

**v)** the base resistance, $R_B$. **(1)**

**vi)** the NPN bipolar transistor in figure 3a is replaced with an N-channel MOSFET. What value of $r_{ds(on)}$ would the MOSFET need to have in order to yield the same on-state power dissipation as the bipolar transistor. **(4)**

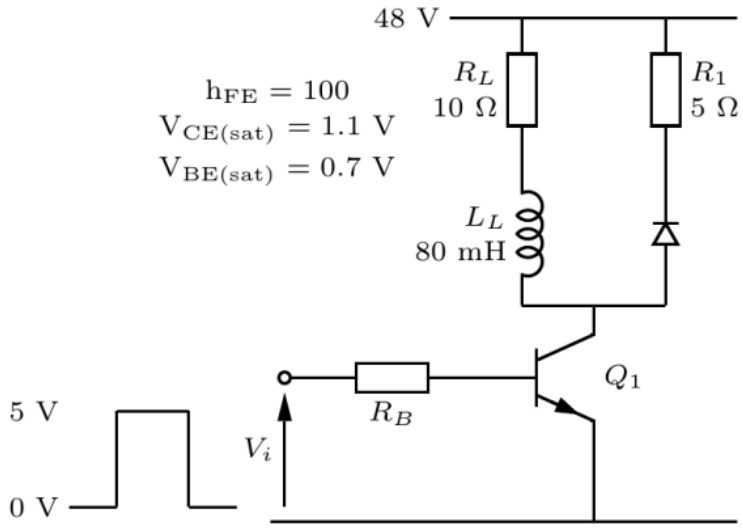


**Figure 3a**

**b.** For the amplifier in figure 3b calculate the DC conditions. (*Collector current, load voltage, collector voltage, emitter voltage, base current, emitter current and the current in the base biasing network ($I_1$)*). Assume that the transistor $V_{BE}$ is 0.7 V in the forward active region and β = 150. State all other assumptions clearly. **(9)**

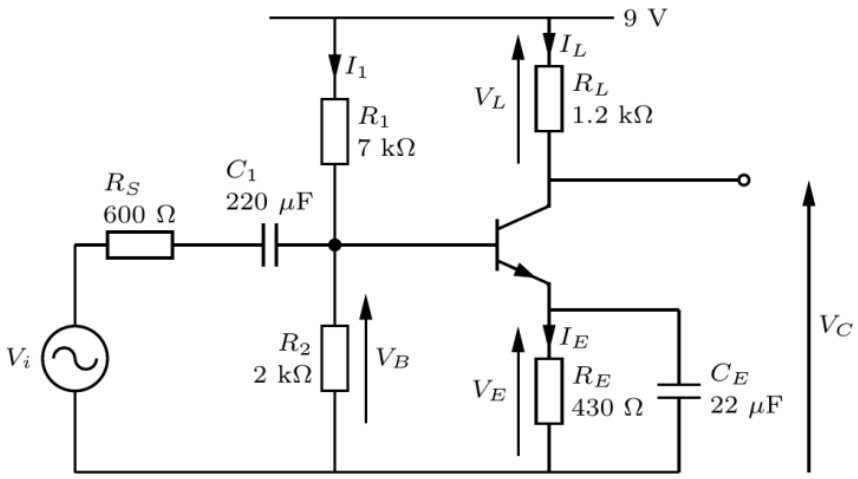


**Figure 3b**

**c.** Using a small signal equivalent circuit, find,

**i)** an expression for the small signal voltage gain for the amplifier in figure 3b. It is acceptable to use // to represent components which appear in parallel. **(5)**

**ii)** a numerical value for the gain, stating any assumptions. **(2)**

**4.** **a.** i. Using sketches briefly describe the operation of the n-channel JFET and n-channel MOSFET planar devices. You should highlight the main differences between the two, including how the gate bias controls the drain current in each case. **(14)**

ii. Identify the 'on' and 'off' gate bias conditions for each when operated as a switch. **(4)**

**b.** i. Using data and equations from page 1 calculate the time it takes for an electron to travel underneath a 1 μm long gate in an n-channel Si MOSFET. You should assume a lateral electric field of $5 \times 10^6$ $Vm^{-1}$ under the gate region. **(4)**

ii. Why is this delay time important when designing high frequency or fast switching MOSFETs? **(3)**

**5.** **a.** Boron (group 3) is used to dope a piece of silicon semiconductor to a concentration of $1 \times 10^{24}$ $m^{-3}$. Explain on an atomic scale why this results in p-type material with a hole produced for every boron atom introduced into the lattice. **(6)**

**b.** Will the hole concentration change significantly as the temperature is increased by 50 $^{o}$C above room temperature? Under the same temperature increase will the fractional change in charge carriers be higher for intrinsic (undoped) material? Justify your answers. **(4)**

**c.** Calculate the concentration of minority electrons in this material ($n_i = 1 \times 10^{16}$ $m^{-3}$ for silicon at room temperature). **(3)**

**d.** What is the conductivity resulting from this doping? **(3)**

**e.** Compare this with the conductivity component due to the minority electrons **(3)**

**f.** Calculate the resistance between opposite faces of a cube of 1 mm edge dimension made from this doped silicon. **(3)**

**g.** What is the resistance between the end faces of a cube where the edge dimension is doubled? **(3)**

**6. a.** **i)** Draw a diagram of an inverting opamp circuit **(2)**

**ii)** Draw an arrow on your diagram pointing to the "virtual earth" **(1)**

**iii)** State briefly how the "virtual earth" is created and maintained. **(3)**

**iv)** State the input resistance of the inverting opamp circuit. **(1)**

**v)** Derive an expression for the gain of the circuit assuming $\boldsymbol{A_v \to \infty}$. **(3)**

**vi)** Show that $\frac{v_o}{v_i} = \frac{-R_f}{R_i + \frac{1}{A_v}[R_i + R_f]}$ assuming $A_v$ is finite. **(5)**

**b.** Consider the multiple input opamp circuit in figure 6b.

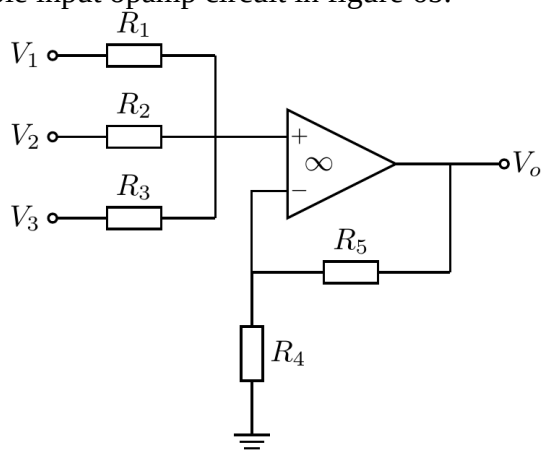


**Figure 6b**

**i)** Find the output voltage as a function of the input voltages. **(3)**

**ii)** Based on your answer to 6. b. i. deduce and state briefly the function of the circuit. **(1)**

**c.** The opamp circuit in figure 6c is a "subtracting circuit" and is also called a "difference amplifier".

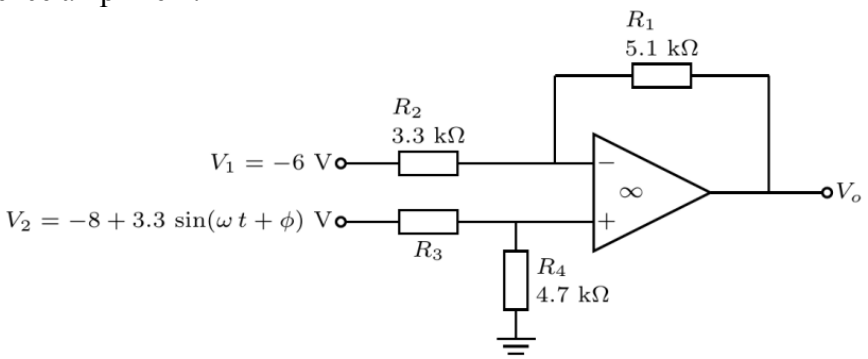


**Figure 6c**

**i)** Find, algebraically, the DC output voltage as a function of the input voltages. **(4)**

**ii)** Hence or otherwise calculate the value of $R_3$ needed to yield $V_o = 0$ V for the inputs in figure 6. c. **(2)**

**PAH / JEG/JPRD**