EEE105 - Electronic Devices
Lecture 16

Junction Field Effect Transistor as a Variable Resistor

(CAL: Jfet(c))

It is quite difficult to model out the exact form of the drain characteristic in the general sense. It is complex as we need to solve for the channel resistance at each point along the channel and integrate to get a sensible result. This is because of the effect of the drain bias meaning that the depletion region thickness varies as one moves along the channel. The details of this can be found in Streetman & Banerjee, if you are interested.

However, if we assume the drain bias, V_d, to be small the we can also make the assumption that the depletion region thickness, d_j, is nearly uniform along the channel and hence make an analysis of the effect of the gate bias. It is important to note here that this region of operation is where the current is rising with drain bias, ***not*** the region where we can use the JFET as an amplifier.

Now in this case we can calculate the resistance from geometry and use Ohm's law to get the drain current, I_d, as a function of V_d.

In this case the halfwidth of the channel that the electrons can move in is given by:

$$b = a - \left[\frac{2\varepsilon(V_0 + V_g)}{qN_d}\right]^{1/2}$$

Note that for a planar device (shown as the practical device in Lecture 15) the value of *b* will be the full channel width as we will be pinching the channel off from one side, not both.

The above equation simply comes from the depletion width equations we calculated in Lecture 14.

Note that as the gate bias increases then the channel width will decrease, as expected.

Let us first use this equation to estimate the pinch-off voltage, V_p.

We can find V_p when the value of the channel width, *b* is equal to

Hence at this point: $a^2 = \frac{2\varepsilon(V_0 + V_p)}{qN_d}$ where V_p will be the gate bias required to pinch the device off.

We can rewrite this as $\boxed{V_p = \frac{qN_d a^2}{2\varepsilon} - V_0}$

Prove this for Homework!

Substituting into our equation for *b* above will give: $b = a\left[1 - \left(\frac{V_0 + V_g}{V_0 + V_p}\right)^{1/2}\right]$

Now to obtain the drain current let: $I_d = GV_d$

Question: What is *G* in this equation?

Now, $G = qN_d\mu_e\frac{2bw}{l}$

where w is the width of the gate and l its length.

Substituting for *b* in the above we can get the relationship:

$$I_d = \frac{qN_d\mu_e 2wa}{l}\left[1 - \left(\frac{V_0 + V_g}{V_0 + V_p}\right)^{1/2}\right]V_d$$

Which can be rewritten as $I_d = G_0\left[1-\left(\frac{V_0+V_g}{V_0+V_p}\right)^{1/2}\right]V_d$ where G_0 is the channel conductance at $V_g = 0$.

Note that if the operating conditions allow us to make the assumption that both the gate and pinch-off voltages are much greater than the built-in voltage (i.e. $V_g, V_p >> V_0$) then we can simplify the above equation to:

$$I_d = G_0\left[1-\left(\frac{V_g}{V_p}\right)^{1/2}\right]V_d$$

Note that this means we can design the desired characteristics of a JFETs but considering its material's parameters, and the device geometry.

Note also that the relationship is only true if, as well as the drain bias, V_d, being small, we have the situation that the gate voltage, V_g is less than the pinch-off voltage, V_p.

What we have derived here a method to use the JFET as a controlled variable resistor in the circumstance where the voltage across the resistor is small.

Junction Field Effect Transistor as an Amplifier

(CAL: Jfet(d))

Let us consider what an amplifier is before looking at using a transitor to act as an amplifier.

In an amplifier we wish to take some ***small*** input signal and obtain a large output that is identical to the input.

For example we wish to take the small analogue signal from a music reading system as the input to the amplifier and increase it to get a large current that can be used to drive a speaker system.

Considering a music signal there are a number of points to be made:

1. A music signal is an a.c. signal. (Any musical signal can actually be viewed as the sum of many sine waves) We need to be able to amplify both the negative and positive parts of the wave.
2. The output waveform should have the same shape as the input waveform. If there are deviations in the shape then we can say that the wave is distorted, and the music will not sound as it should, even if the speaker producing the sound was perfect.

In order to operate the JFET as an amplifier we need to operate the device with a drain voltage that is larger than the pinch-off voltage $(V_d > V_p)$.

Let us look again at the output characteristic. For an ***ideal*** JFET there are two factors we will look at.

1. When the drain voltage is greater than the pinch off voltage then the output current, I_d, ***only*** depends on the value of the gate voltage, V_g. The output (drain) current does not depend on the value of the drain voltage V_d.
2. The value of the current I_d rises and falls linearly with the gate voltage V_g.

From these two points, an ideal JFET should be able to take a small input signal voltage change and give an output current change that is directly in proportion to the change in the input. This means that the ideal JFET should amplify without distortion.

(This is of course for an ***ideal*** JFET. A ***real*** JFET will not perfectly meet either of the two ideals listed above. Real amplifiers use a combination of many transistors in order to minimise the distortion of the output.)

To use a single JFET as an amplifier, let us consider the following simple "common-source" circuit. (It is called "common-source" as the source terminal is shared by both the input (signal) circuit of the amplifier, and the output circuit, carrying the amplified signal.

The input circuit is the circuit supplying the voltage to the gate. It consists, in this very simple design, of a biasing battery giving some voltage on the gate, V_{g0}, and the input signal source giving a voltage v_{in}.

NOTE: We use small letters for signal voltages and currents, and capital letters for d.c. voltages and currents used to bias the circuit to some ideal starting point.

The output circuit consists of a d.c. power supply, in this case a battery with source voltage, V_{dd}, a load resistor, R_L, and the current in the output circuit flows through the source and drain of the transistor. Note that the current in the output circuit all flows through the transistor so the current in the output circuit will be equal to the drain current, I_d.

In order to understand the circuit it is also very important to note that the sum of the voltage drop across the load resistor ($= I_d R_L$) and the source-drain voltage drop (V_d) must equal the voltage of the power supply, V_{dd}. This means that if the voltage drop across the resistor increases, then the voltage drop across the transistor must decrease.

Hence we can write:

We can use this equation to create a ***LOAD LINE*** determining the voltage across the transistor, V_d, for any particular current through the transistor, I_d. (Remember also that in the transistor the output current, I_d, ***only*** depends the voltage on the gate.). The load line can be drawn on the output characteristic as shown:

Note that when there is no current flowing through the transistor, then the voltage drop across the load resistor will be zero and the voltage drop across the JFET will be equal to the power supply voltage.

Similarly if the transistor were perfectly conducting then the voltage drop across the load resistor will equal the power supply voltage and the drain current will be limited to a maximum value of $I_{d0} = V_{dd} / R_L$.

Now note that the region where the transitor operates is only for values of the drain voltage between zero and the power supply voltage. We cannot amplify both positive and negative inputs with this circuit. However we know that our a.c. music input signal will have both positive and negative parts in its waveform. In order to overcome this we must set up the amplifier such that when there is no input signal (the so-called ***quiet point,*** or ***quiescent point***) the amplifier is in the middle of the load line.

This is achieved by the gate d.c. battery giving some quiescent point bias condition, given by V_{g0}, which of course is negative in this circuit.

Now let us consider what happens when we add our a.c. input signal, v_{in}, into the input circuit.

If the a.c. input signal is negative then is will add additional reverse bias to the gate

Therefore the drain current will

This means that the voltage drop across the load resistor will

Hence the voltage drop across the transistor must

This means we will move down the load line in the output characteristic shown above.

By a similar process we can also see that we must move up the load line if the a.c. input signal is in a positive part of the waveform as then the total applied gate voltage will reduce, reducing the reverse bias on the JFET p-n junction and hence allowing the drain current to rise.

This means that we now have the situation where small changes in input voltage cause proportionate changes in output current and by using the a.c. part of the output current we can drive a speaker to reproduce our musical input signal.

NOTE that in this transistor we do not wish the input signal to become so large that the theoretical point on the load line indicates a negative drain current, which in not possible, or so large in the other direction that the theoretical point on the load line means that voltage drop across the transistor is less than the pinch-off voltage. In both these cases the effect will be massive distortion of the signal by the amplifier, which, in the case of music would make it sound terrible, or in the case of amplifying a signal from a sensor could lead to a misleading or non-results.

The amplifier must always be designed so that the largest expected input signal still gives an output signal that is linearly dependent on the input.

Key Points to Remember:

1. By considering the situation of a JFET with small drain bias, we can obtain a value for the pinch off voltage in terms of the material parameters and JFET design.
2. We can characterise easily the behaviour of a JFET as an electrically controlled resistor when the value of the drain voltage is small.
3. A JFET can be used to make a simple amplifier.
4. For an amplifier we must use the region of the drain characteristic above the pinch-off voltage, where the output, drain current depends only on the reverse bias of the gate.
5. We need to bias the gate to the middle of the drain characteristic so that we can amplifiy both the positive and negative parts of an a.c. input signal.
6. We use small letters, rather than capitals to represent signal voltages and currents.
7. In a simple amplifier the current and voltage of the output circuit will move along a load line governed by the amplifier's power supply voltage and the value of the load resistor.