Examination Feedback for EEE6208 – Advanced Integrated Electronics
Spring Semester 2015-16

Feedback for EEE6208 Session: 2015-2016

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

DIGITAL (NJP) – There is more to passing an exam than just practicing tutorial questions and past papers. You must learn and understand all of the material in the notes. If you do not understand it, you will not be able to explain it in an exam question. The techniques that you learn should be applied to many examples of circuits that you can make up yourself or find in books. Answers can be verified using LTspice. Students often complain that there is not a practical element related to MSc modules. In this instance, LTspice is freely available and you should be using it on a regular basis to consolidate your understanding of the notes. You won't receive everything on the end of a spoon!

Question 1:

Part a: straightforward calculation based on the formula sheet and most students got full marks
Part b: most students realised that Vbias was calculated as 5-VGS, and were able to draw the small signal model accurately. However, it was important, to gain full marks in section iii, that some derivation was shown (e.g. a nodal equation) and that the formula for gain not simply stated from memory. The descriptive part (section iv) of the question posed difficulties for some students – marks were awarded for talking about feedback, temperature dependence of transistor performance, room on the IC substrate and voltage headroom.

Question 2:

Part a: in section ii, the minimum voltage across M2 was equal to Vov for M1 (already calculated in section i), because M1 and M2 were matched. In section iii, the easiest way to proceed was to write di=dv/ro.
Part b: Most students could accurately draw the small-signal model, and although some got bogged down rearranging the nodal equations in section ii, I was impressed that the nodal equations themselves were correct in nearly every case. Strangely, the section concerning conditions on the approximation of Rout was poorly managed by quite a few students: expand brackets and see which terms need to be small!

Question 3:

Part a. (i) A poor attempt with many students just reflecting the question back ie 'the silicon is strained which increases performance' A much better explanation is required for the award of any marks. (ii) A reasonable attempt.
Part b. Most students could produce a truth table and confirm that this is a NAND function. Also many realised that the input to the inverter would be Vdd - Vtn but could not describe why this might result in unwanted power dissipation. Good attempts at putting in a level restoring pmos but not how to determine its size. The question did not ask you to calculate transistor sizes, just to describe what you would need to consider when determining the size.

Question 4:

Part a. Surprisingly a very poor attempt at what should have been easy marks. Obviously this must not have been understood. Ask in the lectures or use the recommended texts if there are things that do not make sense.
Part b. (i) A good attempt by most. (ii) A poor attempt, this is straight from your notes!
Part c. Generally a poor attempt. The method is described in your notes, you need to be able to apply this to different logic gates.