EEE 331 – Tutorial Answers 1

Bookwork questions

1) a) See diagram on page 1 of 'Review of BJT operating characteristics'.

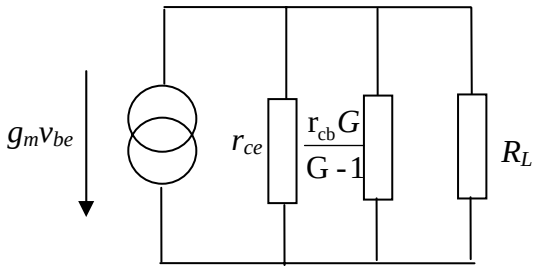
b) See list on pages 1 & 2 of 'Review of BJT operating characteristics'.

c) Typically, when the load impedance is small we can ignore the resistances r_{ce} and r_{cb}.

The reason for this is as follows. Let's draw the small signal equivalent circuit of the output of a common emitter amplifier, we can apply the Miller transformation to r_{cb} ($G = v_o/v_{be}$) to yield the following. The output voltage of this circuit is given by,

$$v_o = g_m v_{be}\left(R_L \,//\, r_{ce} \,//\, \frac{r_{cb}G}{G-1}\right) \approx g_m v_{be} R_L ,$$

when the load impedance is small.



2) See diagram on page 5 of 'Review of BJT operating characteristics'.

3) a) $I_C = I_S \exp\left(\frac{V_{be}}{V_T}\right)$, or $I_C = I_S \exp\left(\frac{V_{be}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}\right)$ if including taking into account the early effect.

b) $I_D = K(V_{GS} - V_T)^2$, or $I_D = K(V_{GS} - V_T)^2(1+\lambda V_{DS})$ if including the effects of finite output impedance.

4) See analysis on page 4 of 'Review of BJT operating characteristics'.

5) a) gain = $-g_m R_L$
   b) gain = $g_m R_L$
   c) gain ~ 1

6) Emitter degeneration makes the output impedance of a common emitter circuit go up from r_{ce} to $r_{ce}(1+g_m R_E)$, where R_E is the value of the emitter degenerating resistor.

7) Common emitter circuits offer a large voltage gain, especially when loaded with an active load, and as such are commonly used as voltage gain stages in op-amps or power amplifiers.

Application questions

8) First thing to note is that this is a common emitter circuit with a degenerated emitter. Hence the gain of the circuit is $-g_m R_L$, from the notes.

The trick to this circuit is calculating what g_m is. From the notes you should remember that,

$$g_m = \frac{dI_C}{dV_{be}}.$$

In the question we're given that $I_C = 4\times10^{-31}\exp(100\times V_{be})$. Hence the transconductance of the BJT is given by,

$$g_m = 4\times10^{-29}\exp(100\times V_{be}).$$

And so now we must calculate what V_{be} is.

From the circuit we can see that $V_b = 80V \times \frac{1k\Omega}{20k\Omega + 1k\Omega} = 4V$, since i_b << i_1. We are also given that the current flowing through R_E is 1A, making $V_e = 1A\times 3.3\Omega = 3.3V$. Hence, $V_{be} = V_b - V_e = 0.7V$ and the transconductance of the BJT is $g_m = 4\times10^{-29}\exp(100\times V_{be}) = 100$.

The next part will test whether you've got your brain switched on… Remember that the transconductance of an *emitter degenerated circuit* is lower than the transconductance of the *BJT in the circuit*. The circuit transconductance, g_{mc} is related to the BJT transconductance, g_m by the following relation (in the notes),

$$g_{mc} = \frac{g_m}{1 + g_m R_E} = 0.302\,.$$

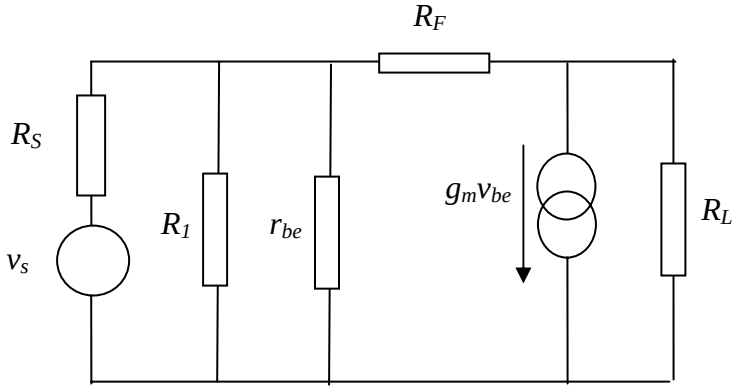
Quite small! Therefore the gain of the circuit is,

$$\frac{v_o}{v_i} = -g_{mc} R_L = -22.7.$$

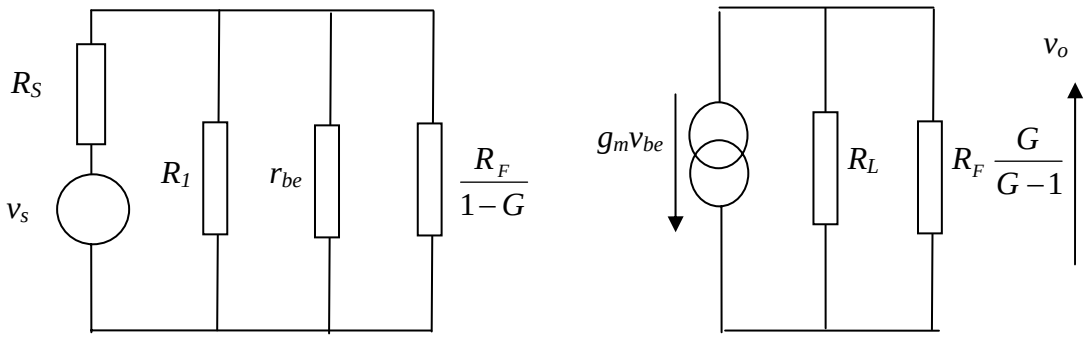
If you forgot to modify the transconductance to account for the effects of the emitter degenerating resistor, you will lose some marks for this question, but will get most.

And now for the difficult question…. What should occur to you is that there is a large quiescent power being developed in the BJT (1A×1V=1W) and therefore this circuit is relatively inefficient. This occurs because the transistor is biased on in order to provide voltage gain. A two stage amplifier, where the voltage gain was provided by a low current stage (low power loss) and the current gain is provided by a push-pull stage (low power loss) would be much more efficient and still develop the same power gain (arguably more since we would be able to operate the circuit at higher load power without worrying about the devices melting).

9) The given circuit, when assuming we are operating in the mid-frequency range, can be reduced to the following small signal circuit.



If we define G = v_o/v_{be} we can simplify the above to the following.



The first task is to calculate the value of G. The most likely way of us calculating this looks like the output circuit, since v_{be} appears courtesy of the current generator, and v_o appears across the resistances.

The only problem with this is that we have an unknown value of resistance, $R_F G/(G\text{-}1)$. However, this is an amplifier circuit, and as such G is likely to be large and $R_F G/(G\text{-}1) \rightarrow R_F$, we will assume this for the time being and then check later.

$$\begin{aligned} v_o &= -g_m v_{be} R_L // R_F \\ \therefore G &= -g_m R_L // R_F \end{aligned}.$$

Both R_L and g_m are likely to be large then $|G| >> 1$ and our assumption appears to be valid.

Now all we need to do is relate v_i to v_{be}, which we can do by looking at the input side of the circuit.

$$v_{be} = \frac{v_i \left(R_1 // r_{be} // \frac{R_F}{1-G} \right)}{\left(R_1 // r_{be} // \frac{R_F}{1-G} \right) + R_S}.$$

And hence the gain of the circuit,

$$A = \frac{v_o}{v_i} = G \frac{\left(R_1 // r_{be} // \frac{R_F}{1-G} \right)}{\left(R_1 // r_{be} // \frac{R_F}{1-G} \right) + R_S}.$$

The output impedance of the circuit is $R_L // R_F$, by inspection.

10) You should notice from the question that we are not dealing with a small signal case here, as the input voltage is 3V, the gain of the circuit is 100, whilst the maximum output voltage is limited to 15V. Hence the rate of change of voltage at the output is not only determined by the signal, but also the availability of drive current to move the output voltage from its on state to its off state.

From the notes,

$$\left.\frac{dV_o}{dt}\right|_{\max\_ON} = \frac{I_F}{C_{CB}} = -\frac{I_B}{C_{CB}} = -\frac{(V_i - V_{BE})}{R_S C_{CB}} = -2.3\times10^9 Vs^{-1}$$

Similarly for turn on off…

$$\left.\frac{dV_o}{dt}\right|_{\max\_OFF} = \frac{V_{BE}}{R_S C_{CB}} = 7\times10^8 Vs^{-1}.$$

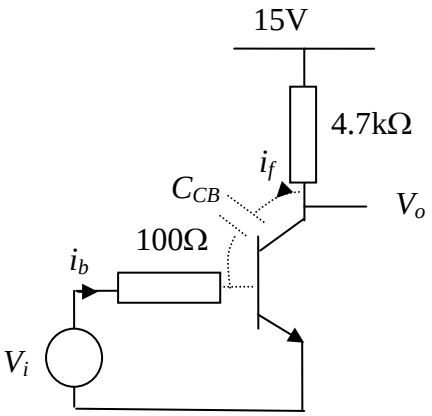


Figure 5a

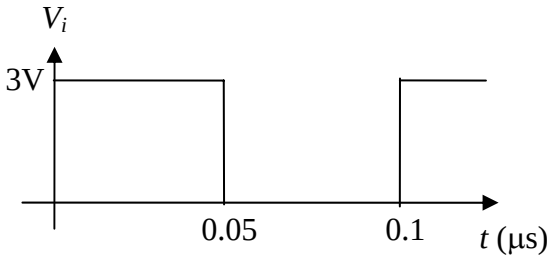


Figure 5b

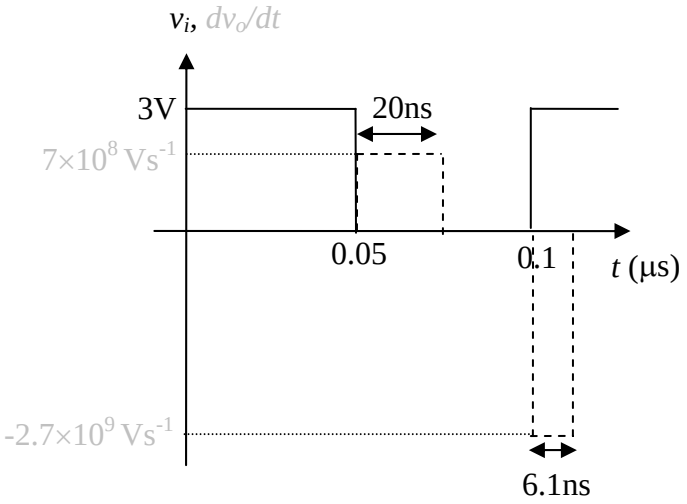
Having determined the rates of change when the transistor is turning on and off we must now tackle the problem of plotting the graph, $(dv_o/dt, t)$. For this we must calculate the time it takes for the output voltage to swing from off to on, t_{on} and vice versa, t_{off}.

$$t_{on} = \frac{v_{o\_on} - v_{o\_off}}{\left.\frac{dv_o}{dt}\right|_{\max\_ON}} = \frac{(1-15)}{-2.3\times10^9} = 6.08ns,$$

and similarly,

$$t_{off} = \frac{(15-1)}{7\times10^8} = 20ns.$$

Therefore the graph asked for in the question looks like this,



One could increase the slew rate by increasing the current available to C_{CB}, either by increasing the input voltage or by reducing the source impedance (although of course this runs the risk of blowing the transistor up! Particularly in MOSFET circuits, source resistors are used to prevent damage to the gate via high currents)

Difficult questions

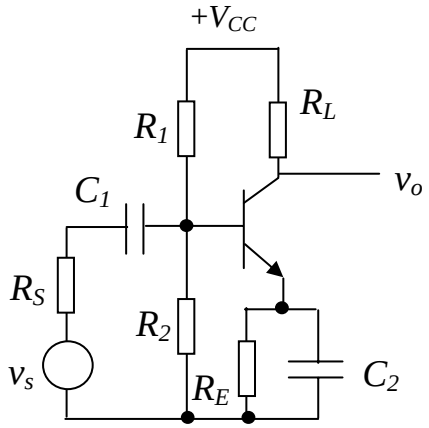
11) The voltage gain of the simple circuits that we have examined here varies like $g_m R_L$ (the voltage gain for a common source circuit is ~1 and so we would not use this topology for a voltage gain stage). The gain therefore depends upon the transistor used via g_m, which itself is the slope on the output current, control voltage graph.

In a BJT $I_C = I_S \exp\left(\frac{V_{be}}{V_T}\right)$, whereas $I_D = K\left(V_{GS} - V_T\right)^2$ in a MOSFET.

Because of these relationships, a MOSFET will always have a lower transconductance than a BJT, as its output current varies like the square of the input voltage, rather than exponentially. Therefore the gain of a circuit using a MOSFET will typically be smaller than that of a circuit using a BJT.

12) The emitter degenerating resistor provides negative feedback and thus the gain is reduced. This can be explained as follows.

- The input voltage appears at the base of BJT. Hence when the input rises, so does the drive to the transistor, which in turn leads to an increase in collector current.
- Since the current gain of the transistor is high, most of this increased collector current flows through out of the emitter.
- The increased emitter current results in an increased voltage across the emitter degenerating resistor.
- The increase in emitter voltage reduces the drive to the transistor (remember the transistor is controlled by $v_{be} = v_b - v_e$), thus limiting further increases in the collector current and hence the gain.



The capacitor C2 is chosen such that at the frequencies of interest, it appears as a short circuit to ground to our small signal, thus bypassing R_E and the negative feedback it provides.

13) The Miller effect is a small signal effect, whereas slew rate limiting is a large signal effect. Put another way, the Miller effect is independent on signal amplitude and slew rate limiting is dependent upon the signal amplitude.

14) Capacitors are typically included between the base and collector of a BJT in the gain stage of a power amplifier to avoid gain peaking (and hence instability) caused by two poles in close proximity (one due to the gain stage, and one due to the feedback).