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Metal Semiconductor Junctions

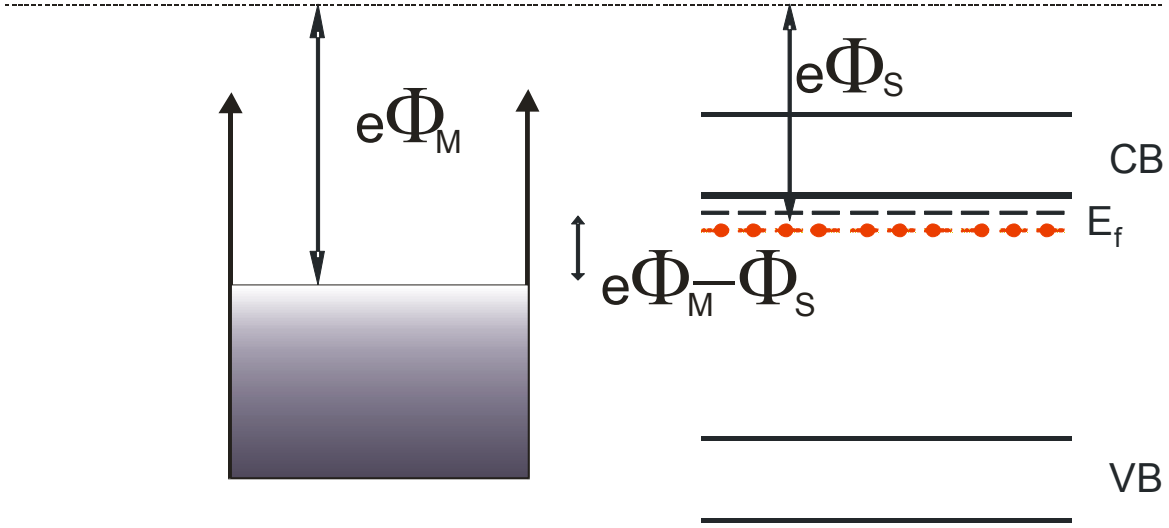
Metal / Semiconductor Junctions

Two types : Ohmic & Rectifying

Depends on relative work functions (Ø) of metal and semiconductor

eg metal on n-type semiconductor

Case 1: $Ø_m > Ø_s$ n-type



On contact, electrons spill over from the semiconductor to empty level in the metal , leaving a positive depletion layer in the semiconductor and a negative region in the metal.

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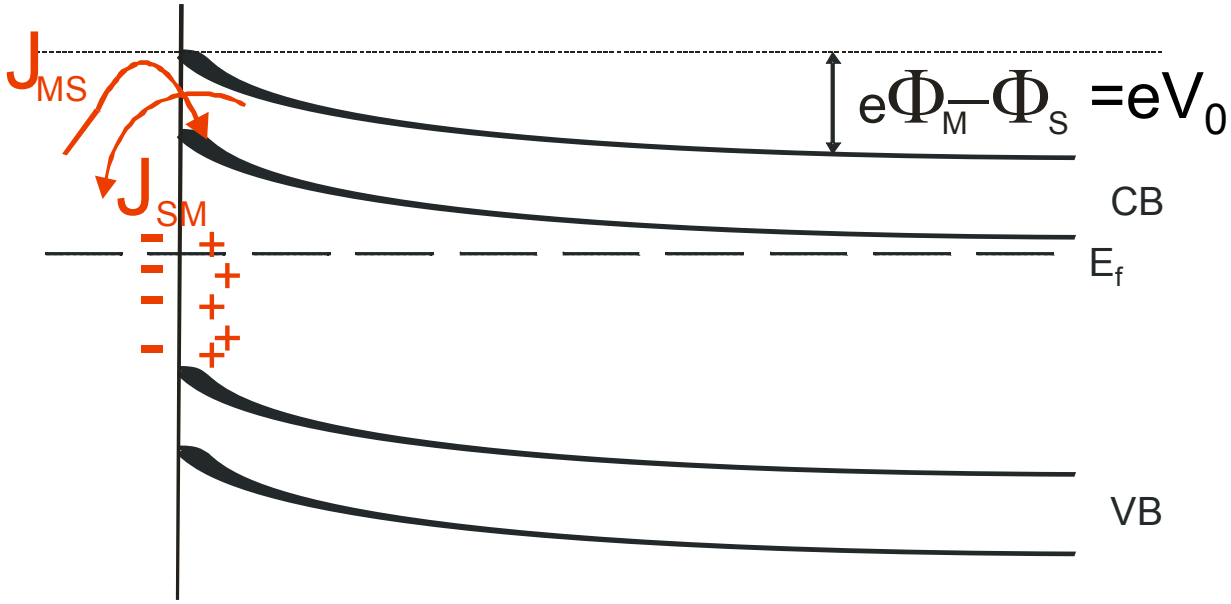
Metal Semiconductor Junctions

In equilibrium, electron currents each way are equal ($J_{sm} = J_{ms}$). Band edges bend-up in semiconductor depletion layer to form a potential energy barrier and $eV_o = e(\varnothing_m - \varnothing_s)$



Reverse bias

All levels in n-type are lowered as +ive potential is applied.

Barrier height increases for electrons in the semiconductor. Barrier height for electrons in the metal remains the same.

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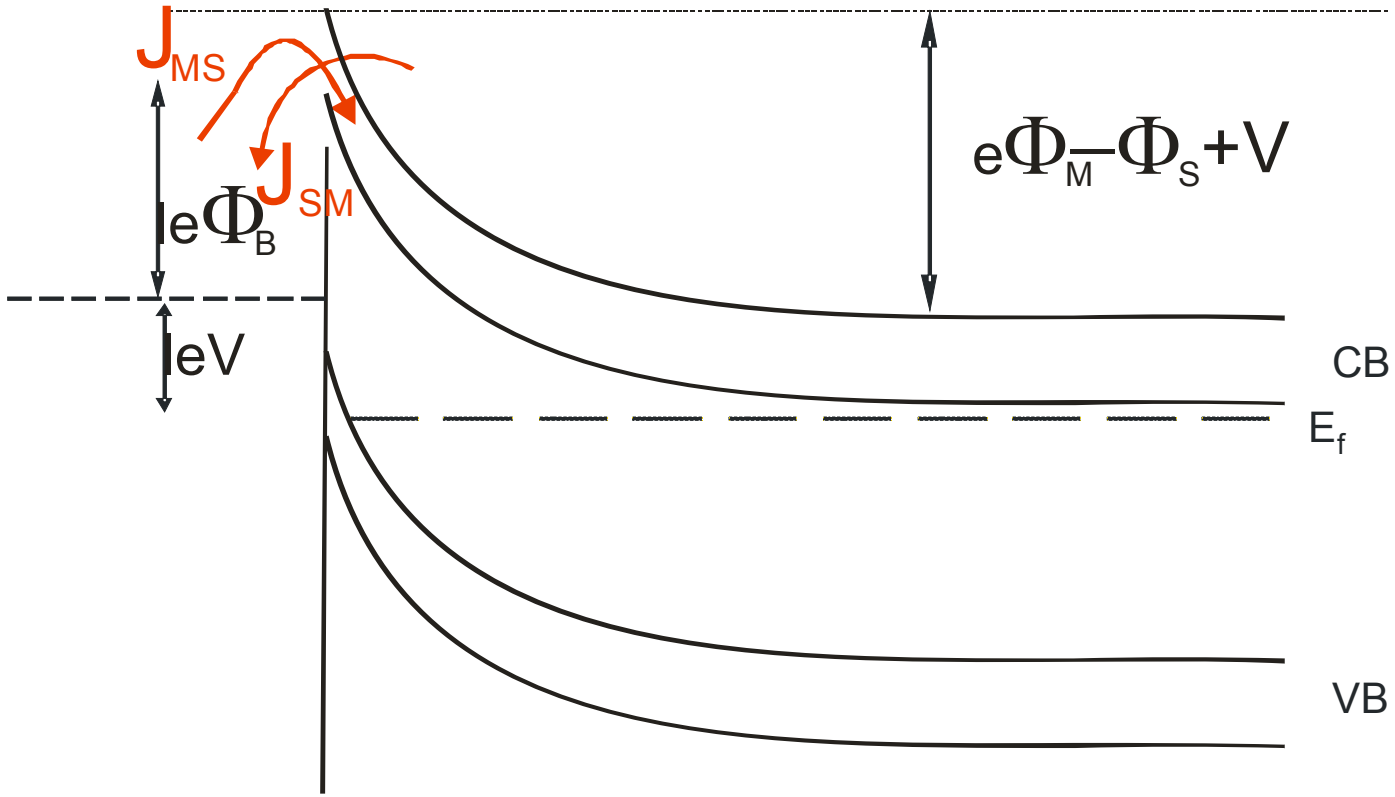
Metal Semiconductor Junctions



J_{sm} reduced. J_{ms} remains same.
V increase the barrier height and cuts off any electron flow from semiconductor to the metal. There remains a small saturation current independent of V due to thermal emissions across the barrier seen by electrons in the metal.

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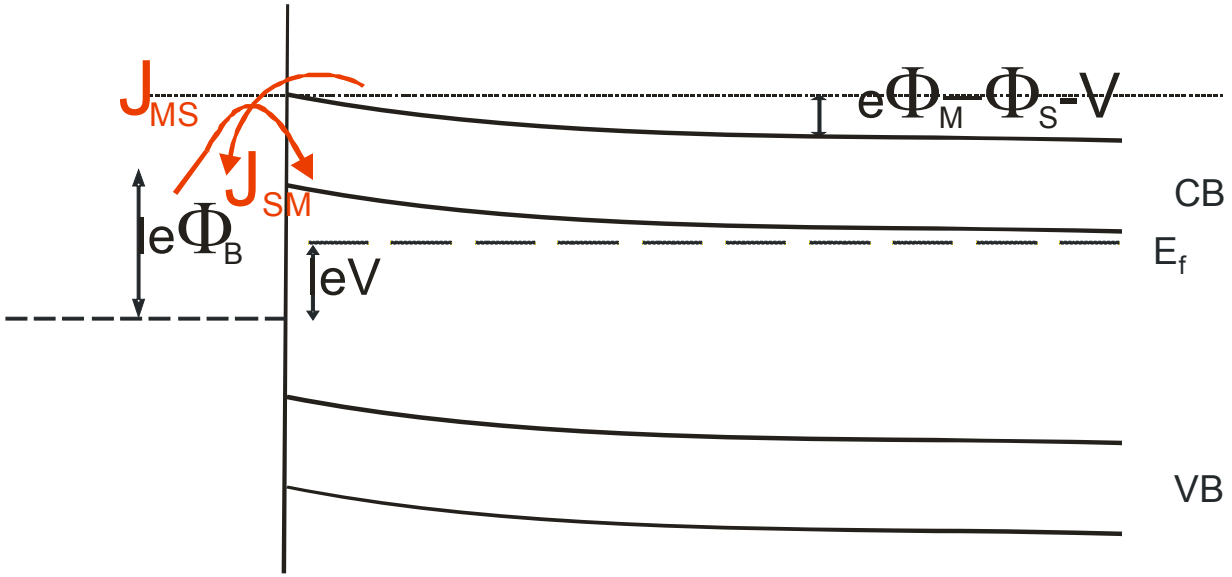
Metal Semiconductor Junctions

Forward bias

All levels in n-type are raised as –ve potential applied.

Barrier height decreases for electrons in the semiconductor. Barrier height for electrons in the metal remains the same.



i.e. J_{sm} increased while J_{ms} remains the same.

∴ i.e. Junction rectifies if $\emptyset_m > \emptyset_s$ for an n-type semiconductor.

I-V Characteristics

Electrons from metal → semiconductor need energy $e\emptyset_B$ to surmount barrier and move into semiconductor, so:

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Metal Semiconductor Junctions

Barrier height to electron from semiconductor side is $e(V_o \pm V)$ where + is for reverse bias and –is for forward bias. Barrier for electrons in metal stays the same.

$$J_{ms} \propto P(e\Phi_B) \propto \frac{1}{1 + \exp\left(\frac{e\Phi_B - E_F}{kT}\right)} \propto \exp -(e\Phi_B)$$

$$J_{sm} \propto \exp -\left(\frac{e(V_o \pm V) + e\Phi_n - E_F}{kT}\right) \propto \exp -(e\Phi_B \pm V)$$

n.b.: no hole conduction ALL ELECTRONS

$\rightarrow J_{ms}$

$\leftarrow J_{sm}$

$\rightarrow$ conventional current flow, $J = J_{sm} - J_{ms}$

$$J \propto \exp\left[\frac{-(e\Phi_B)}{kT}\right].\left[\exp\left(\frac{eV}{kT}\right) - 1\right] = J_o\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

This is the usual **rectifier** equation – same form as p-n junction but J_o is different.

Call this behavior a Schottky diode

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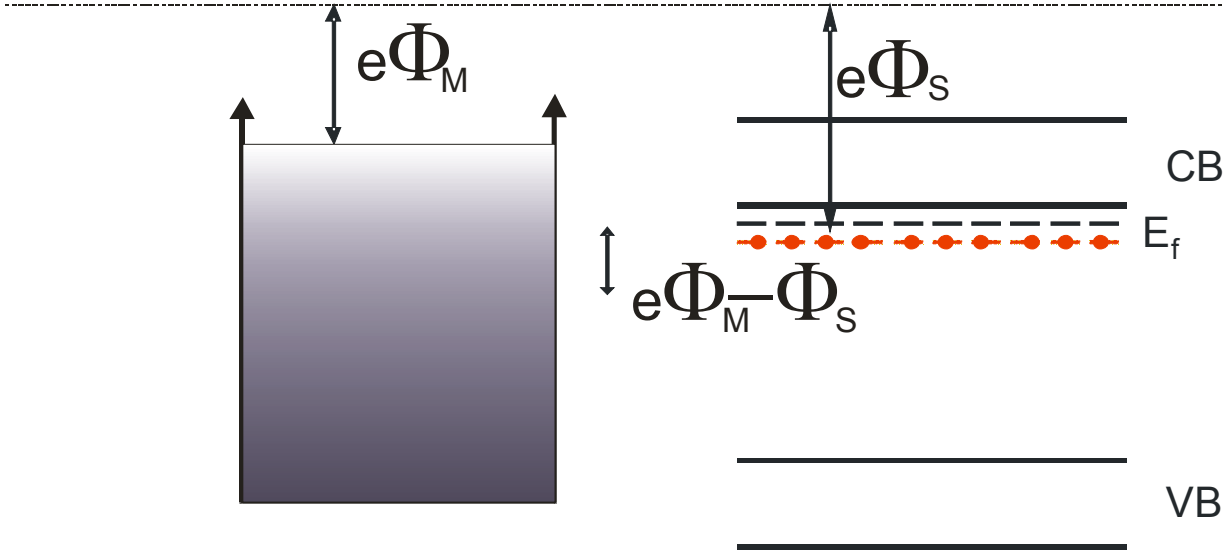
Metal Semiconductor Junctions

Case 2: $Ø_s > Ø_m$ n-type



Before contact Øs > Øm and $E_{FM} > E_{FS}$

On contact electrons flow from metal to semiconductor.

In equilibrium there is virtually no barrier to impede the flow of electrons in either direction.

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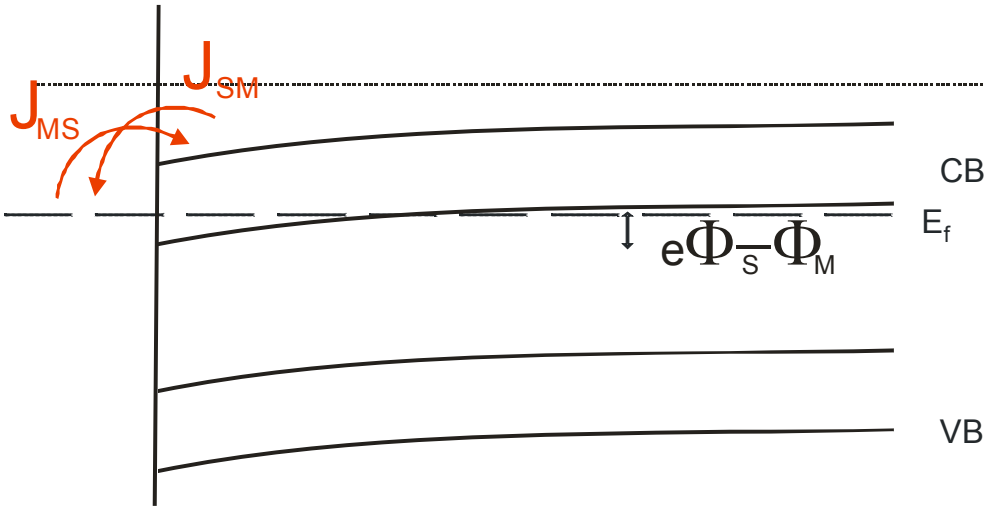
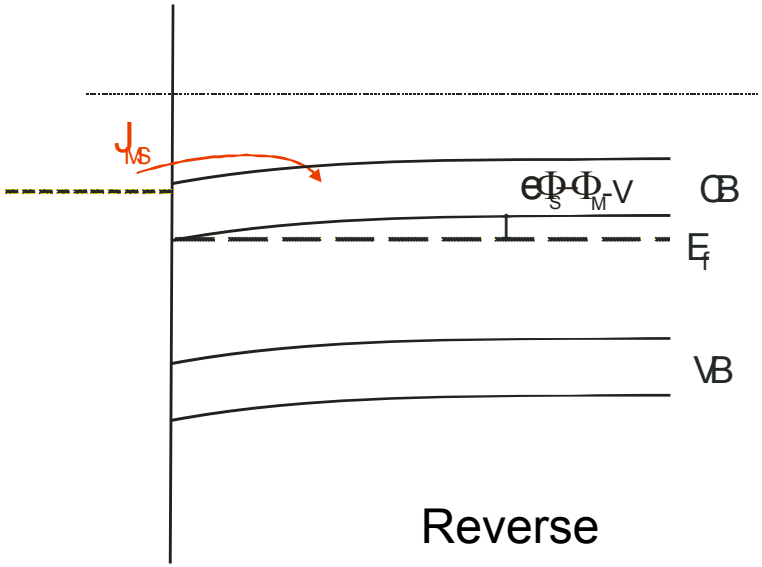
Metal Semiconductor Junctions

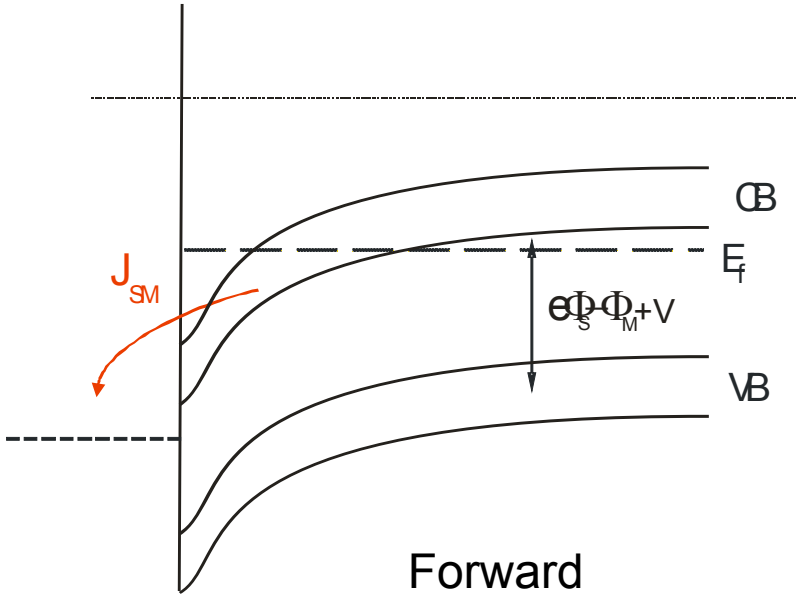


Passes current in both directions

Ohmic contact



Reverse



Forward

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Metal Semiconductor Junctions

Similar arguments hold for metal/P-type semiconductor – just opposite.
Easy to find metals with different workfunctions
Metal-semiconductor junctions can be dominated by surface effects, surface must be clean

Advantages of a Schottky diode
Smaller Vo than a pn junction- low voltage operation
Faster than a pn junction because there is only one carrier type

Schottky diode is a Unipolar device (only electrons or holes, but not both)

Bipolar Junction Transistor

Consider symmertically doped n-p-n transisitor.
No Bias: Barrier eV_o established to prevent diffusion of majority carriers in equilibrium

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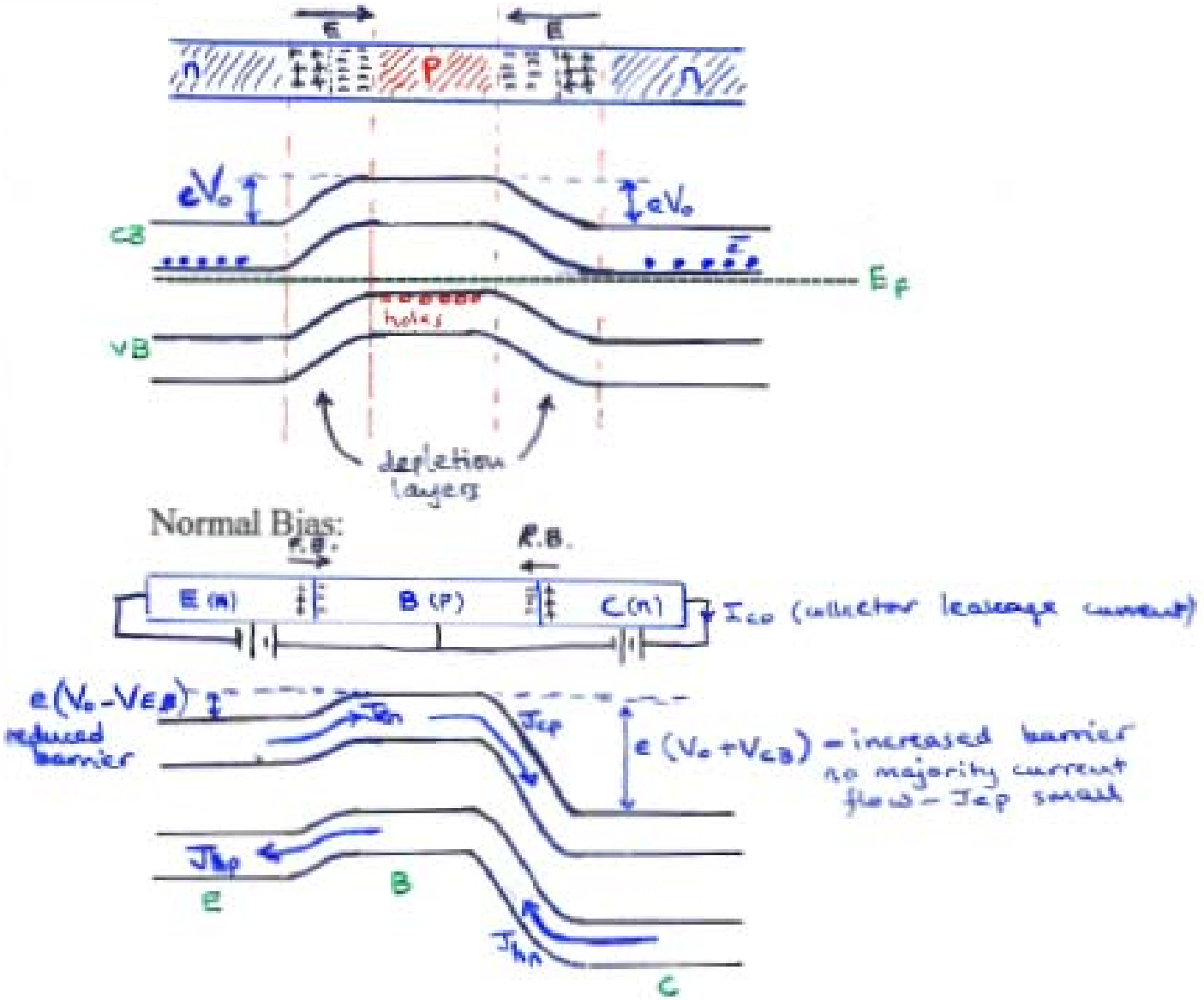
Bipolar Junction Transistor



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Bipolar Junction Transistor

Majority currents J_{en} and J_{np} flow at the EB junction.

Arrange for $J_{en} >> J_{hp}$ by doping the base to be less than that in the emitter .

i.e. N_d (E) >> N_a (B) $\sigma E >> \sigma B$ high injection efficiency, so most of the junction current carried by electrons.

If the base is thin compared to the electron diffusion length, little recombination in the base, most electrons from the emitter will make it across to the collector. A small change in base current results in a large change in emitter (i.e. collector) current– hence gain and amplification of power.

E-B junction forward biased – low impedance

C-B junction reverse biased – high impedance

Transfer of power from low Z to high Z circuit – Transfer Resistor – TRANSISTOR

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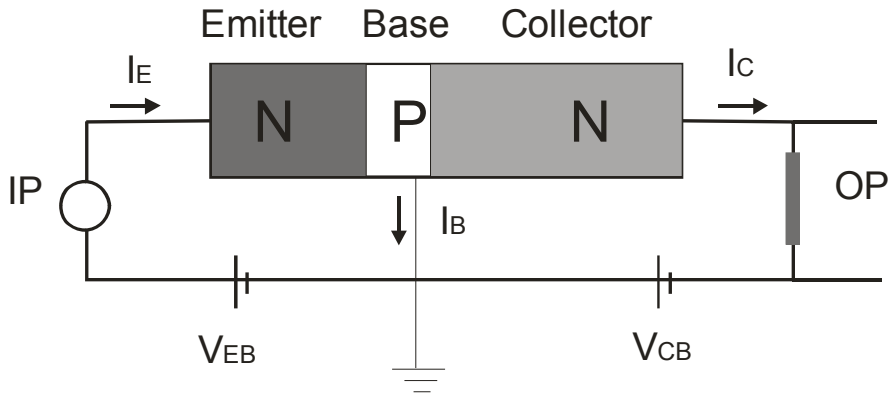
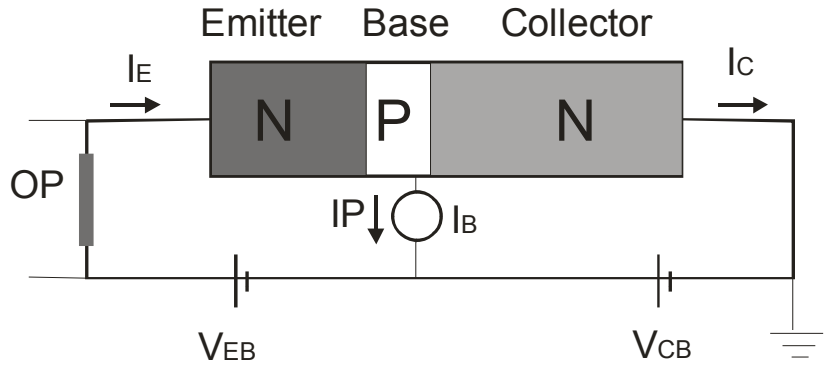
Bipolar Junction Transistor

NPN transistor in common base configuration



NPN transistor in common emitter configuration



Need to find the current gain for both configurations

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Bipolar Junction Transistor

Common Base Gain $(\alpha_B) = \frac{\partial I_C}{\partial I_B}$ Common Emitter Gain $(\alpha_E) = \frac{\partial I_C}{\partial I_E}$

Kirchoffs Law $I_B = I_E - I_C$ therefore $\alpha_E = \frac{\alpha_B}{1-\alpha_B}, \alpha_B = \frac{\alpha_E}{1-\alpha_E}$

$$\text{Injection efficiency } (\gamma) = \frac{\text{change in electron current from emitter}}{\text{change in total emitter - base current}} = \frac{\partial J_{nE}}{\partial J_{nE} + \partial J_{pE}} = 1 - \frac{\partial J_{nE}}{\partial J_{pE}}$$

$$\partial j_{nE} = \frac{eD_e n}{l_B}, \quad \partial j_{nE} = \frac{eD_p p}{l_E} \ldots\ldots \frac{\partial J_{nE}}{\partial J_{pE}} = \frac{D_e n}{D_p p}\frac{l_E}{l_B}$$

$\gamma = 1 - \frac{D_e n}{D_p p}\frac{l_E}{l_B}$ normally use a thin base $l_B << l_E$ so $\gamma \to 1$

$$\text{Base transport factor } (\beta) = \frac{\text{change in electron current reaching collector}}{\text{change in electron current from emitter}} = \frac{\partial J_{nC}}{\partial J_{nE}}$$

if we make the base thin, all electrons transmitted across base $\partial J_{nC} = \partial J_{nE}$ $\beta \to 1$

$\alpha_B = \gamma\beta \to 1$ $\alpha_E = \frac{\alpha_B}{1-\alpha_B} \to \frac{1}{\approx 0} \to$ high number

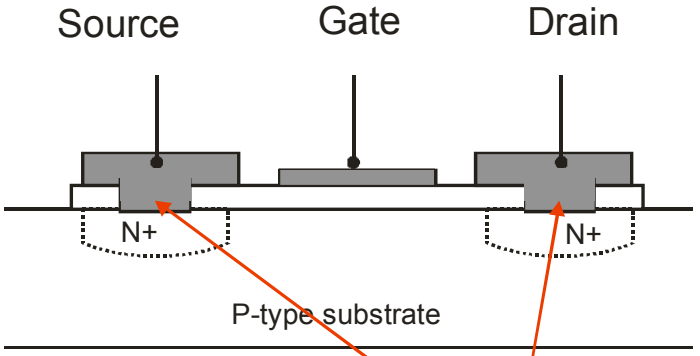
Metal oxide Semiconductor Transistor

Metal Oxide Semiconductor Transistor (MOST)

(CMOS – complementary MOS transistor)

used in most modern digital applications.

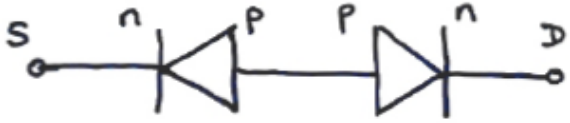
low power, easy to manufacture



Ohmic S-D contacts formed by diffusing donors into substrate

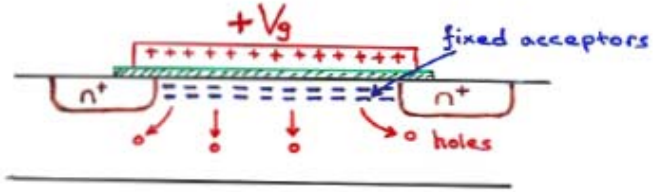
If Vgs = 0, Id = 0 since we get two back to back diodes between the source and drain.

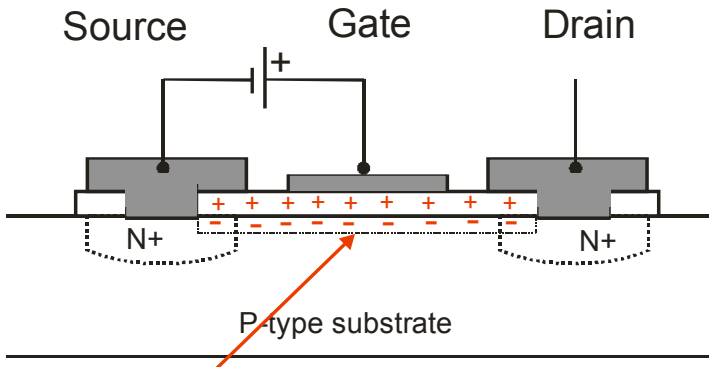
Oxide prevents any gate current.



Small Vgs > 0

- Small V_{gs} > 0 results in negative charge being induced under the gate (capacitor). -these come from ionised acceptors (-ve). I_d = 0 since these charges are fixed in the crystal lattice.





A negative conducting channel is formed under the gate

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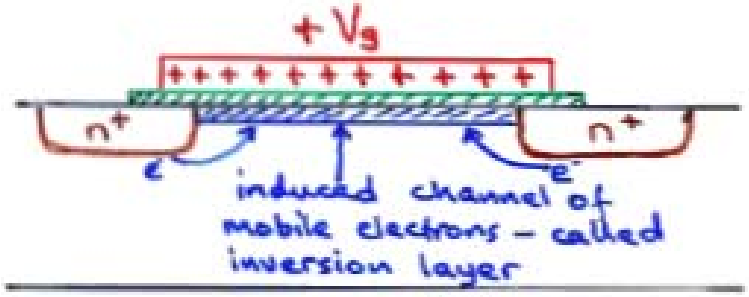
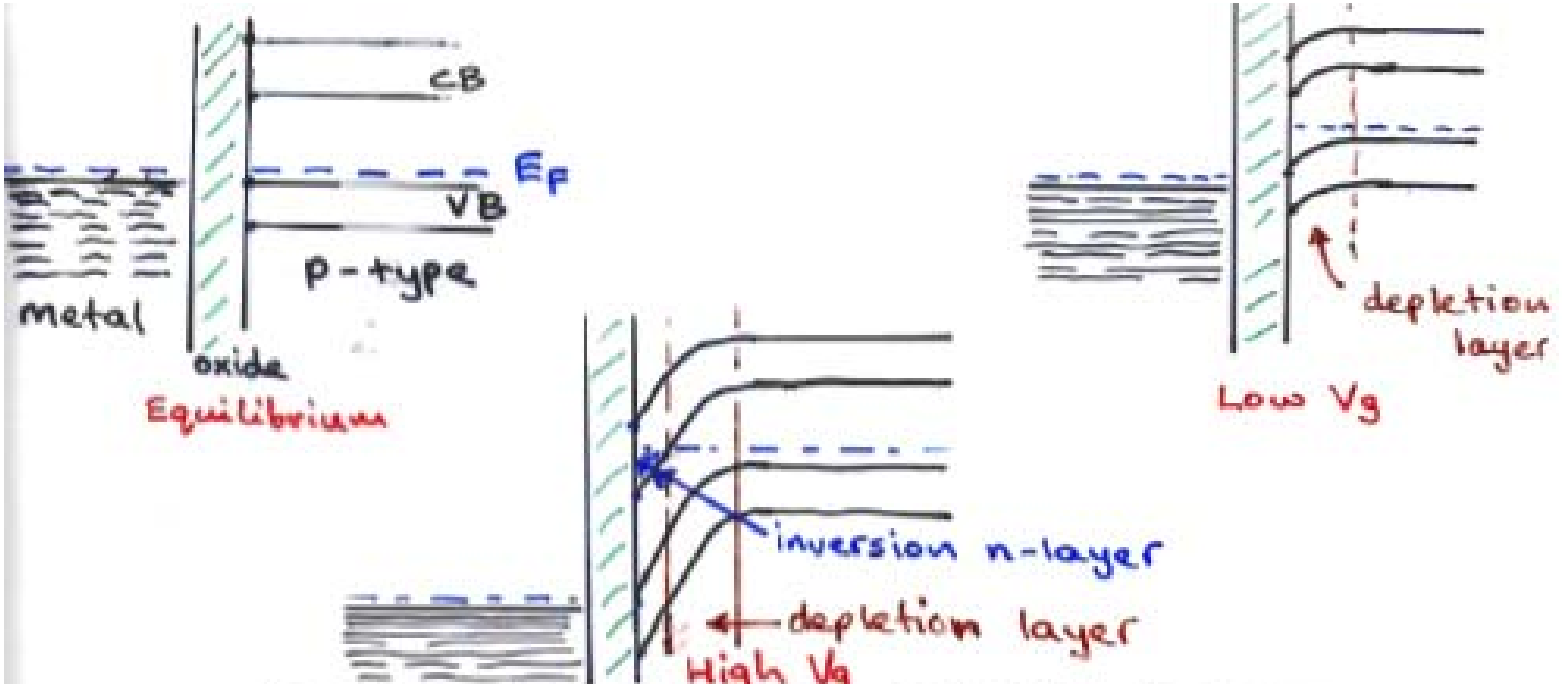
Metal oxide Semiconductor Transistor

Large Vgs > 0

For large Vgs all the charge cannot be provided from the depletion layer. The additional negative charge is drawn from the n+ source and drain regions in order to balance out the increasing positive charge on the gate.





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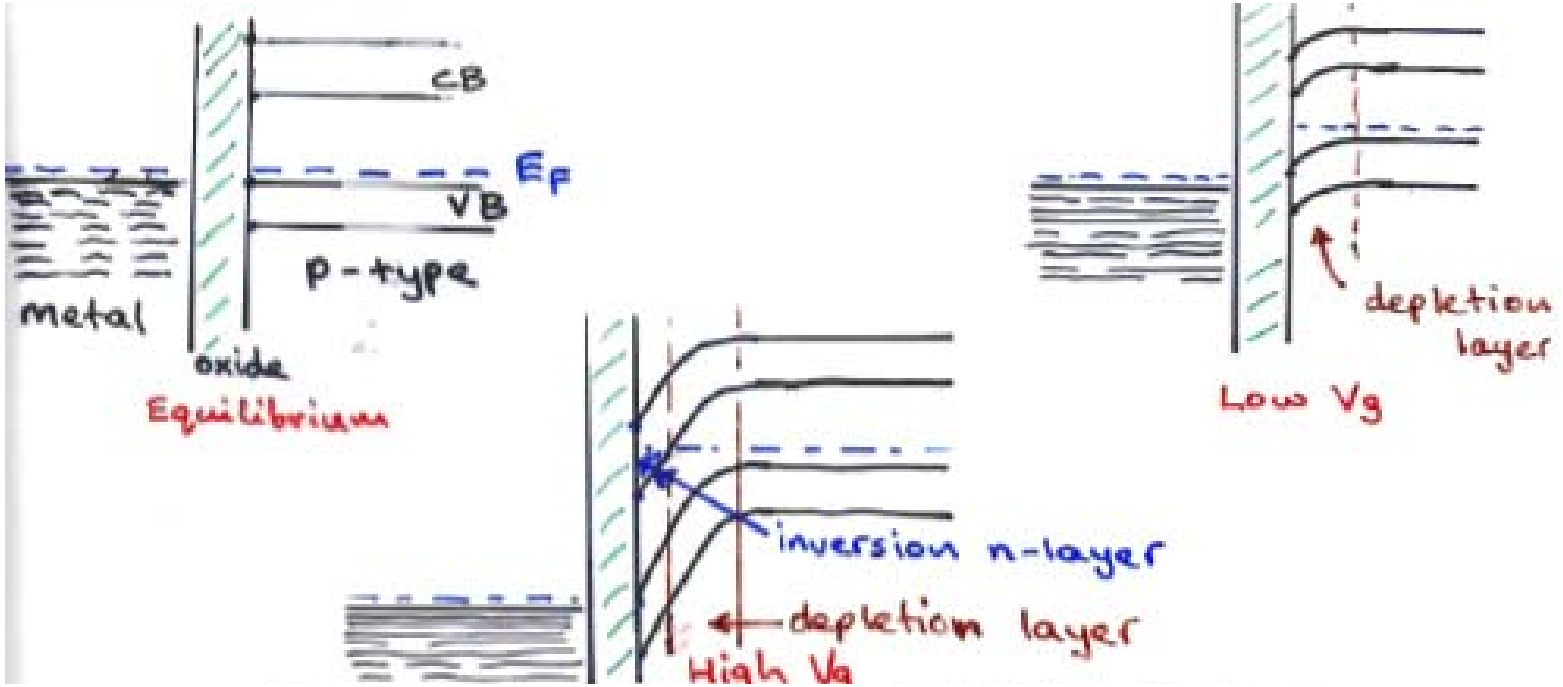
Metal oxide Semiconductor Transistor



As soon as a channel is formed, current can flow between the Source and Drain. If a drain voltage Vd is appied, a current Id will flow. For a fixed drain voltage Vd, if the gate voltage V_g increases

- The width of the channel increases
- The conductivity of the channel increases
- I_d increases
- This is called ENHANCEMENT MODE