The University Of Sheffield.

Data Provided: List of formula and useful constants at end of paper

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE348 Electronics and Devices

Answer **FIVE QUESTIONS** comprising **AT LEAST TWO** each from **part A** and **part B. No marks will be awarded for solutions to a sixth question, or if you answer more than three questions from parts A or B.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Part A

A1 **Figure 1** shows the schematic for a digital circuit.

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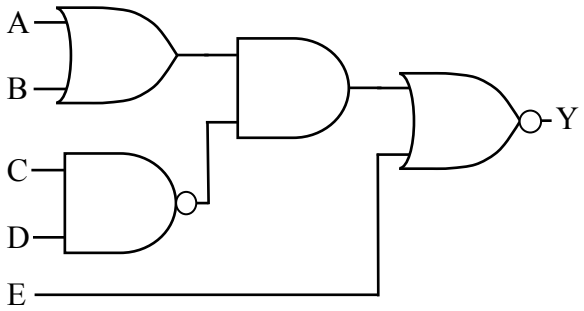

Figure A1: Digital Circuit

a. Derive the logic function of the circuit in **Figure A1**. **(2)**

b. Draw the *transistor-level* schematic diagram for a CMOS circuit that would implement the function in **Figure A1**. There may be more than one way to implement this function: justify the way in which you have implemented the circuit. **(6)**

c. Size the transistors in the circuit that you have drawn, assuming that the gate is *minimum-sized* (using the normal definition for this). **(4)**

d. Assuming that the gate capacitance associated with a minimum-sized *n*-type FET is 0.5fF, estimate the capacitance associated with each of the connections (wires connecting inputs and output, and any intermediate wires between separate sub-circuits) in your *transistor-level* circuit. **(2)**

e. Rather than implement the circuit in Figure A1 as a specific circuit, you decide to implement each of the individual logic gates separately as CMOS circuits. What would be the important differences between the implementation of the circuit as a whole and as separate, individual parts. **(6)**

A2 **a.** A pass transistor is incorporated in a circuit as shown in **Figure A2**.

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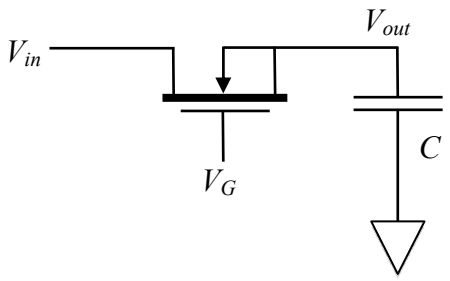

Figure A2: Pass Transistor Circuit

Initially (and for some time), V_{in}=0V, V_G=V_{DD} (a voltage which is above the threshold voltage, V_T, of the transistor). You may assume that the gain of the transistor is K_N.

i). At time, t=0, the input V_{in} is changed to V_{DD}. Verify that the response of V_{out} as a function of t in the period $t \geq 0$ is:

$$V_{out}(t) = (V_{DD} - V_T) - \frac{(V_{DD} - V_T)}{1 + \frac{K_N(V_{DD} - V_T)t}{2C}}$$ **(4)**

ii). Identify the value of voltage to which V_{out} becomes asymptotic. Explain why this is the case. **(2)**

b. With the capacitor, C, disconnected, what is the small signal impedance of the point labelled V_{out} to ground when:

i). V_{in}=0 **(3)**

ii). V_{in}=V_{DD} **(3)**

Comment on the use of the transistor as an electronic switch in this circuit. **(2)**

c. If you were to make a *good* electronic switch for use in a digital circuit, identify how this might be done. You do not need to do a detailed analysis of the switch's performance but you do need to relate the behaviour of the electronic switch to the behaviour of a perfect switch. **(6)**

A3. **a.** **i.** An n-channel MOSFET has W/L = 2µm/0.4µm, V_{TO}=0.6V and a process transconductance parameter K_n=150µA/V^2. Ignoring channel modulation and assuming the transistor is operating in saturation, calculate the values of V_{OV} and V_{GS} required for this transistor to be biased at a drain current of 100µA. What is the minimum value of V_{DS} required to ensure the transistor is saturated? **(2)**

ii. For the transistor in part **i**, and assuming operation in the saturation region, what will happen to the drain current when the following device dimensions and voltages are changed:

- The channel length is doubled,
- V_{OV} is doubled.

Which of these changes could lead to the transistor falling into the triode region of operation and why? **(3)**

b. **Figure A3** shows a SPICE model of a source-follower, or common drain, amplifier. The transistor M1 operates at a drain current of 150µA, and you can assume that its parasitic capacitances can be neglected at the frequencies under consideration. The transistor has the following parameters:

Kn = 200µA/V^2, W/L = 6µm/0.6µm, λ=0.05V^{-1} and V_{TO} = 0.5V.

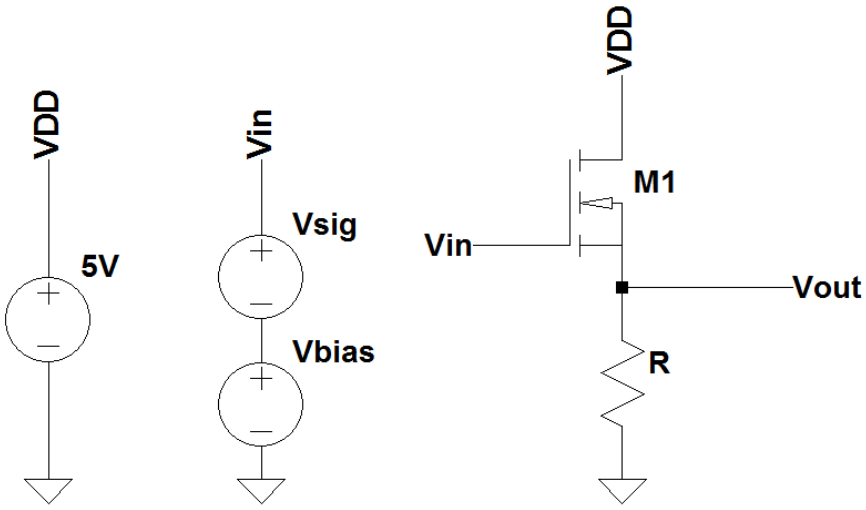

Figure A3: a SPICE model of a source follower

i. Draw the small signal model of the circuit in **Figure A3**, using the T-model for the transistor M1 and including the transistor output impedance r_o. Calculate the values of r_o, and g_m. **(5)**

ii. For R=10kΩ, calculate a suitable value for Vbias. **(3)**

iii. Use your small signal model to derive an expression for the gain of the source follower (show your working). Calculate the value of the gain for R=10kΩ. **(4)**

iv. Sketch a graph of the output voltage, Vout, of the circuit in **Figure A3** over time. Assume R=10kΩ and Vsig is a 0.2V pk-pk sine wave at 1kHz. Include numbered axes on your graph to show the maximum, minimum and average (DC) output voltages, as well as suitable values along the time axis respectively. **(3)**

A4 **a.** Give a short description of the following terms:

i. Current steering,
ii. The transconductance parameter, g_m,
iii. Channel length modulation. **(5)**

b. Consider an NMOS transistor having the following parameters:

V_{TO}=0.4V, K_n=175μA/V^2, λ=0.1V^{-1}, W=3μm, L=1μm, Cgs=Cgd=2fF.

i. Draw the small signal π model of the MOSFET described by the parameters above with the source terminal at ground. Include the dominant parasitic capacitances and the output resistance r_o. **(3)**

ii. Calculate the values of r_o and g_m, assuming V_{GS}=1V. **(2)**

iii. The FET is attached to a circuit such that the voltage at its drain is -25x that at its gate: compute the Miller equivalent capacitances and redraw your small signal model to show them. **(4)**

c. **Figure A4** shows a basic PMOS current mirror driven by a **5V** power supply and with the reference current set by a resistor **R**. M1 and M2 are matched transistors having V_{TO}=-0.5V, K_p=200μA/V^2, λ=0.04V^{-1}and W/L = 2μm/0.5μm.

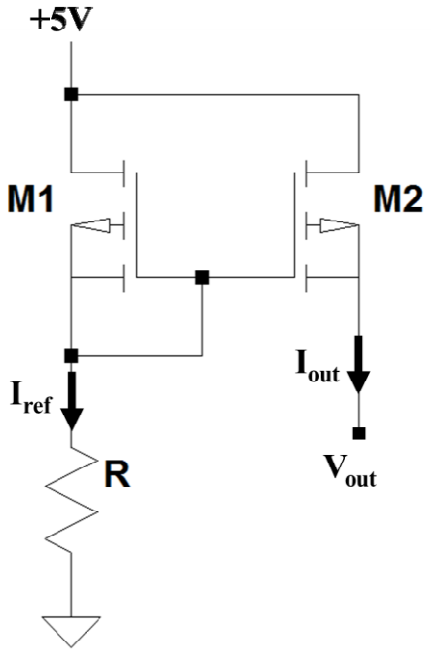

Figure A4: a PMOS current mirror

i. Determine an appropriate value for the resistor **R** in order to set $\mathbf{I_{ref}}$, the reference current through M1, at 150μA. **(3)**

ii. V_{DS} for M1 and M2 in **Figure A4** are initially identical. A change in the circuit to which the current mirror is attached causes $\mathbf{V_{out}}$ to increase by 0.5V. What will the resultant current error be (i.e. the difference between $\mathbf{I_{ref}}$ and $\mathbf{I_{out}}$)? What feature of more advanced current mirrors minimises the current error resulting from changes such as those described? **(3)**

Part B

B1. a. Consider a Si pn junction with the following parameters.

Diode area, $A = 0.1\text{ cm} \times 0.1\text{ cm}$
p-side doping, $N_a = 1\times10^{16}\text{ cm}^{-3}$
n-side doping, $N_d = 1\times10^{17}\text{ cm}^{-3}$
Electron diffusion coefficients, $D_e = 20\text{ cm}^2/\text{s}$
Hole diffusion coefficients, $D_h = 12\text{ cm}^2/\text{s}$
Electron minority carrier lifetime, $\tau_e = 100\text{ ns}$
Hole minority carrier lifetime, $\tau_h = 10\text{ ns}$
Intrinsic carrier concentration, $n_i = 1.5\times10^{10}\text{ cm}^{-3}$

i) Explain why it is important to have long minority carrier diffusion length in solar cell. Verify that the electron and hole minority carrier diffusion lengths are 14.1 and 3.46 μm, respectively. **(2)**

ii) In addition to long minority carrier diffusion length, it is also important to have a large depletion width. Verify that the depletion width is 0.33 μm at 0 V. **(4)**

b. i) When the solar cell in part (a) is exposed to direct sunlight the electron-hole pair generation rate is assumed to be constant and is given by $10^{22}\text{ cm}^{-3}\text{s}^{-1}$. Using parameters from part (a), verify that the photocurrent produced is 29 mA. **(2)**

ii) Calculate the open circuit voltage for this Si diode if the saturation leakage current is 10 fA. **(2)**

c. Consider a solar cell that produces a short circuit current $I_{SC} = 30$ mA and an open circuit voltage, $V_{OC} = 0.6$ V. Assuming that $V_m = 0.9V_{OC}$ and $I_m = 0.9I_{SC}$, describe how a cluster of solar cells can be connected to produce a total power of 10 W at an output voltage of 10 V. [V_m and I_m are the voltage and current that produces the maximum output power] **(4)**

d. Figure B1 shows an optimised solar cell known as Passivated Emitter & Rear Locally-diffused (PERL) cell. **(6)**

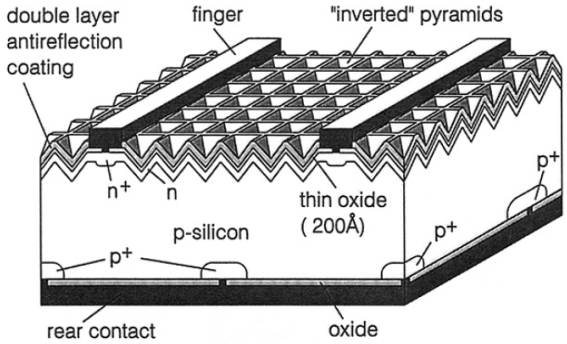

Figure B1: Schematic of a PERL cell (Zhao et. al., Solar Energy Materials and Solar Cells 41/42(1996) 87-89)

Explain the design features that enable PERL cell to achieve a high conversion efficiency.

B2. **a.** Consider an InGaAs pin photodiode designed to absorb signal at 1550 nm. This InGaAs pin diode has a depletion width of 1 μm and InP p and n layers. The dielectric constant is 13.9 and the saturation velocity is 10^5 cm/s.

i) Discuss the main advantages of using the wide bandgap InP for the p and n layers. **(3)**

ii) The absorption coefficient of InGaAs is 8000 cm^{-1} at the wavelength 1550 nm. Calculate the quantum efficiency of this photodiode assuming no surface reflection. **(2)**

iii) Determine the size of the photodiodes that should be fabricated in order to achieve an RC-limited bandwidth of 20 GHz. [Assume that the device series resistance is negligible and the metal transmission line is 50 Ω]. **(3)**

b. Current high speed optical networks operate up to 100 Gb/s with higher bit rate networks being evaluated. Recommend a photodiode design that will achieve a bandwidth of 75 GHz. Provide supporting statements for features included in your design (specify the choice of material, layer thicknesses and dimension of diode). **(6)**

c. Consider a Si avalanche photodiode (APD) with a breakdown voltage V_b = 200 V, a quantum efficiency of 0.9, series resistance of 1 Ω and n_m = 1.6. When biased at 90% of its breakdown voltage the dark current is 1 nA due to surface leakage.

i) The APD is used to detect a signal at 633 nm with an optical power of 1 nW. Verify whether this APD will be able to detect the signal when when operated at 10 V. **(3)**

ii) Suggest a suitable operating voltage range for this APD to generate gain that will raise the signal above the dark current. **(5)**

B3. a. The parameters of a GaAs pn homojunction LED are given below

Electron diffusion coefficient, $D_e = 30$ cm^2/V-s
Hole diffusion coefficient, $D_h = 15$ cm^2/V-s
p-doping, $N_a = 5\times10^{16}$ cm^{-3}
n-doping, $N_d = 5\times10^{17}$ cm^{-3}
Electron minority carrier lifetime, $\tau_e = 10^{-7}$ s
Hole minority carrier lifetime, $\tau_h = 10^{-8}$ s
Intrinsic carrier concentration, $n_i = 2\times10^{6}$ cm^{-3}

i) Calculate the injection efficiency, $\gamma_{inj} = \dfrac{J_e}{J_e + J_h}$, assuming no recombination due to traps in this GaAs LED.

ii) The electrons are injected into the top p-layer, so that photons generated by radiative recombination can be emitted vertically. Calculate the injection current at a forward bias of 1 V. Assume the diode has an area of 1 mm^2 **(10)** **(4)**

b. Sketch and label the structure to produce high brightness GaN LED. Explain the features that improves the efficiency of the LED in your answer. **(6)**

B4. a.

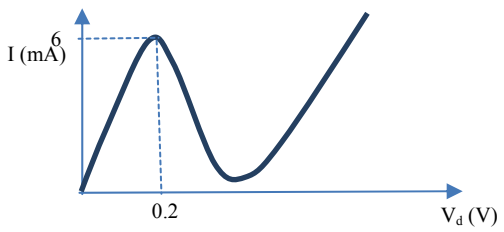

Figure B4

A typical current-voltage characteristics of a GaAs tunnel diode is shown in Figure B4. Using band diagrams, explain how the current changes with bias voltage. **(6)**

b. The impedance of a tunnel diode is given by

$$Z_{in} = \left[R_s + \frac{-R}{1+(\omega R C_j)^2} \right] + j\left[\omega L_s + \frac{-\omega C_j R^2}{1+(\omega R C_j)^2} \right].$$

Z_{in} changes with frequency, making it a very important component for high speed circuit applications. Consider a GaAs tunnel diode with the following parameters; a lead inductance of 0.1 nH, a series resistance of 4 Ω, a junction capacitance of 70 fF and a negative resistance of 20 Ω. Calculate the frequency when the real part of the impedance becomes zero. **(7)**

c. With the aid of band diagrams, explain how a resonant tunnel diode works. **(4)**

d. Discuss the key advantages of resonant tunnelling diodes over conventional tunnel diodes based on a pn junction. **(3)**

NLS/AM/CHT/ TWANG

ADDITIONAL INFORMATION

List of formulae

$$f^e(E) = \frac{1}{\exp\left(\frac{E - E_{Fn}}{kT}\right) + 1}$$

$$f^h(E) = \frac{1}{\exp\left(\frac{E_{Fp} - E}{kT}\right) + 1}$$

$$I_d = I_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$I_s = qAN_cN_v\left[\frac{1}{N_A}\sqrt{\frac{D_e}{\tau_e}} + \frac{1}{N_D}\sqrt{\frac{D_h}{\tau_h}}\right]\exp\left(-\frac{E_g}{kT}\right)$$

$$J_e = \frac{qD_en_p}{L_e}\exp\left(\frac{qV}{kT}\right)$$

$$J_h = \frac{qD_hp_n}{L_h}\exp\left(\frac{qV}{kT}\right)$$

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_aN_d}{n_i^2}\right)$$

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_a + N_d}{N_aN_d}\right)V_{bi}}$$

$$L_{e(h)} = \sqrt{D_{e(h)}\tau_{e(h)}}$$

$$D_{e(h)} = \frac{kT}{q}\mu_{e(h)}$$

$$V_{OC} = \frac{kT}{q}\ln\left(1 + \frac{I_{ph}}{I_s}\right)$$

$$I_{tot} = I_s\left[1 - \exp\left(\frac{q(V - I_{tot}R_s)}{kT}\right)\right] + I_{ph}$$

$$I_{ph} = qAG(L_e + W + L_h)$$

$$\eta = \left(\frac{I_{ph}}{q}\right)\left(\frac{P_{opt}}{h\nu}\right)^{-1}$$

$$\eta = (1 - R)[1 - \exp(-\alpha W)]$$

$$R_{res} = \frac{\eta q\lambda}{hc}$$

$$I_{ph} = \frac{\eta\lambda P_{opt}}{1.24}$$

$$t_{diff} = \frac{4x^2}{\pi^2 D_p}$$

$$f_{3dB\_tr} = \frac{0.4}{t_r} = \frac{0.4v_s}{W}$$

$$f_{IMP} = \frac{v_{sat}}{2(w - x_a)}$$

$$f_{RC} = \frac{1}{2\pi RC}$$

$$M = \frac{1}{1 - \left(\frac{V - IR}{V_b}\right)^{n_m}}$$

$$V_B = E_mx_a + \left(E_m - \frac{qQ_c}{\varepsilon_s}\right)(w - x_a)$$

$$SNR = \frac{I_{ph}^{\ 2}}{< i_s^{\ 2} > + < i_{th}^{\ 2} >} = \frac{(q\eta P_{opt}/h\nu)^2}{2qI_TB + 4kTB/R_{eq}}$$

$$g(h\nu) = G_{las}[f^e(E^e) + f^h(E^h) - 1] \quad cm^{-1} \text{ where } G_{las} = 5.6\times10^4\,\frac{(h\nu - E_g)^{1/2}}{h\nu} \text{ for GaAs}$$

$$J_{th} = \frac{qd_{las}n_{th}}{\tau_r(J_{th})}$$

PHYSICAL CONSTANTS

Quantity	Symbol	Value
Boltzmann constant	k	1.38066×10^{-23} J/K
Electron rest mass	m_o	9.1095×10^{-31} kg
Electronic charge	q	1.60218×10^{-19} C
Permeability in vacuum	μ_0	1.25663×10^{-8} H/cm
Permittivity in vacuum	ε_0	8.85418×10^{-14} F/cm
Planck constant	h	6.62617×10^{-34} Js
Speed of light in vacuum	c	2.99792×10^{10} cm/s
Thermal voltage at 300 K	kT/q	0.0259 V

Dielectric constant = 11.9 (Si), 12.4 (GaAs), 13.9 (InGaAs)