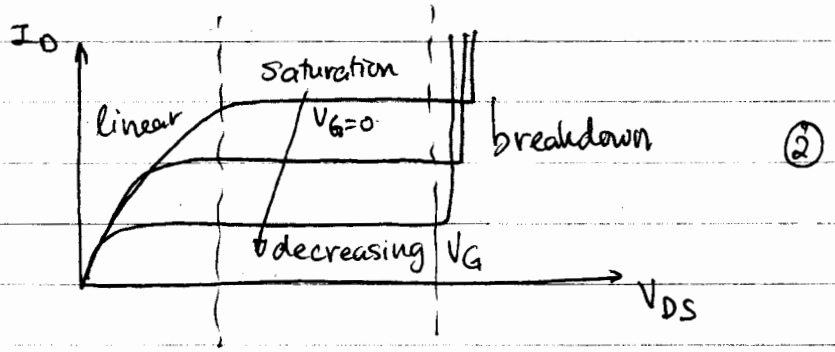
(Bookwork)

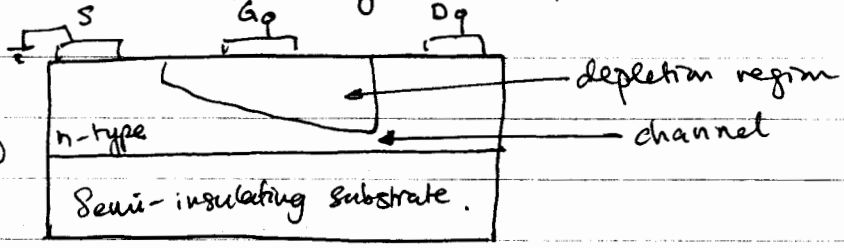
Q1. a) The typical current-voltage characteristics of a MESFET at different gate voltages are shown below



(2)

In the linear region, the width of the depletion region beneath the gate is controlled by the gate bias. Increasing the reverse bias increases the depletion width and reduces the channel width, leading to a reduced current flowing from the source to the drain.

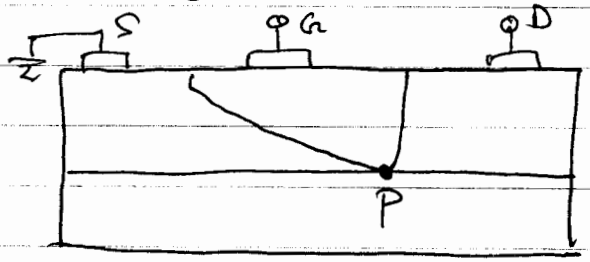
(2)



(1)

In the saturation region, the current from the source to the drain is saturated since the gate bias V_G is sufficiently large to increase the depletion width that shuts the channel. Further increase in V_{DS} does not increase the current flow because the potential at point P remains constant.

(2)



In the breakdown region, the voltage V_{DS} is sufficiently large such that high electric field in the depletion region causes avalanche breakdown.

(1)

[8].

(Bookwork + Calculation)

b) i) Pinch off voltage is the applied V_{DS} that closes the channel.

Pinch off voltage $V_p = \frac{qa^2 N_D}{2\varepsilon} = \frac{1.6\times10^{-19}\times(0.5\times10^{-6})^2\times 2\times10^{21}}{2\times 8.85\times10^{-12}\times 12.9}$ ③

$= 0.35$ #

ii) The cut off frequency $f_T = \frac{V_{sat}}{2\pi L} = \frac{1.0\times10^5}{2\times\pi\times 1\times10^{-6}} = 15.9\ GHz$ # ①

iii) The threshold voltage $V_T = \phi_{BN} - V_n - V_p$

$V_n = \frac{kT}{q}\ln\left(\frac{N_c}{N_D}\right) = 0.026\ln\left(\frac{4.7\times10^{17}}{2\times10^{15}}\right) = 0.14$ ④

$V_T = 0.8 - 0.14 - 0.35 = 0.31\ V$ #.

[8]

Any of the followings (Understanding)

c) i) To increase the f_T to above 100GHz, it is necessary to use very short channel so that $L < 0.16\ \mu m$ which is easily achievable.

2) Fabricate the MESFET using materials with higher mobility such as InGaAs, InAs and InSb.

3) Introduce a 2-DEG by using doped AlGaAs or use a strained-InGaAs channel via pseudomorphic growth.

[4]

(Bookwork) $f_T = \frac{1}{2\pi\tau_{EC}}$, $\tau_{EC} = \tau_{BE} + \tau_{BC} + \tau_B + \tau_C$

Q2.

a) To increase the f_T in a Si BJT, we can

i) Increase the drive current I_C to reduce the dynamic resistance $\frac{kT}{qI_C}$ which will reduce τ_{BE} and τ_{BC}.

ii) Reduce device area to reduce C_{BE} and C_{BC} which leads to smaller τ_{BE} and τ_{BC}

iii) Reduce the thickness of the base layer to reduce diffusion time τ_B

(4)

iv) Reduce the resistance r_E and r_C which will reduce τ_{BC}.

[4]

(Understanding) and (some bookwork)

b) The approaches above are limited by

i) Kirk effect: When the current density $J_C = q n_c v_{sat}$ such that n_c is comparable to the doping in the collector, base pushout occurs. This increase the diffusion across the base.

(4)

ii) The reduction in the area is ultimately limited by lithography. However a more important effect is the increased current density in small area and hence is also subjected to Kirk Effect.

iii) If the base layer is too thin, base punchthrough occurs, shorting the emitter-base and collector-base depletion regions. This leads to uncontrollable current.

iv) Increasing the doping in emitter leading to bandgap reduction that reduces gain and increased C_{BE} that increases τ_{BE}.

[4]

(Understanding)

c) SiGe has narrower bandgap than Si. Hence in the Si/SiGe HBT

② the gain is higher due to $\beta \propto \exp\left(-\frac{\Delta E_g}{kT}\right)$

① The mobility of SiGe is higher, so that diffusion time across the base is reduced leading to higher f_T.

Doping in the base layer can be increased without compromising

② the gain. The increased doping allows lower base access resistance and thinner base layer to be used.

[5]

(Calculation)

d) $\tau_{BE} = \frac{kT}{qI_C} C_{BE} = \frac{0.026}{1\times10^{-3}} \times 14\times10^{-15} = 3.64\times10^{-13}$

$\tau_{BC} = \left(\frac{kT}{qI_C} + r_E + r_C\right) C_{BC} = (26+26+45)\times 4\times10^{-15} = 8.28\times10^{-13}$

$\tau_B = \frac{W_B^2}{2D_e} = \frac{W_B^2}{2\left(\mu\frac{kT}{q}\right)} = \frac{(75\times10^{-9})^2}{2\times0.15\times26\times10^{-3}} = 7.2\times10^{-13}$

$\tau_C = \frac{W_C}{2V_{sat}} = \frac{200\times10^{-9}}{2\times1\times10^5} = 1\times10^{-12}$

$\tau_{EC} = \tau_{BE} + \tau_{BC} + \tau_B + \tau_C$

$= 1.86$ ps.

$f_T = \frac{1}{2\pi\tau_{EC}} = 85$ GHz #.

[7]

(Bookwork + Understanding)

Q3. a)i) As the dimensions of CMOS reduces, the thickness of the oxide layer reduces to maintain the oxide capacitance. Likewise the depletion region width should also be reduced by increasing the doping concentration N_A. (2)

$\frac{N_A^{1/2}}{C_{ox}}$ is therefore the strongest parameter that controls V_T.

(1) $V_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$ is only weakly dependent on N_A.

$V_{FB} = \frac{Q_0}{C_0}\frac{x_0}{d}$ depends on the change in oxide layer. in practical case.

(2) However can be assumed to be V_{FB} = difference in work function between oxide and semiconductor

∴ V_B and V_{FB} are weaker factors.

(Understanding)

ii) V_T needs to be reduced in order to minimise the power dissipated during switching.

As $\frac{N_A^{1/2}}{C_{ox}}$ continue to be reduced, V_{FB} and V_B (3) become more dominant and eventually will make V_T reduction difficult, especially when changes in oxide layer is significant.

[8]

(Understanding + Bookwork)

Q3 b) i) The oxide thickness needs to be thin in order to maintain high oxide capacitance required to achieve low V_T. Having thin oxide also allows large oxide capacitance required to maintain high drain current

(4) $$I_D = \frac{Z}{L} \mu_n C_o \left(V_G - V_T - \frac{V_D}{2} \right).$$

Similarly $g_m = \frac{Z \mu_n \varepsilon_{ox}}{dL} (V_G - V_T)$ also require thin oxide layer.

[note the equations are not compulsory part of the answer but students should be able to argue why thin oxide is required]

ii) Gate length. Short gate length is required to
(1) maintain high g_m and I_D as well as high f_T.

iii) Junction Depth. Shallow depletion is required to maintain
(1) the overall capacitance of the MOSFET. This is ~~achieved~~ achieved using higher doping concentration in the semiconductor.

[6]

(Understanding + Bookwork)

c) i) The lower limit of the oxide thickness will be imposed by onset of tunnelling through the oxide. To overcome this high k-dielectric is required so that oxide thickness < 2nm can be fabricated. HfO used but need to develop new oxide layer.

ii) Limited by lithography. EUV technology ~ 45nm. To go to lower limit electron or x-ray beam will be required. These are expensive and not suitable for high volume manufacturing.

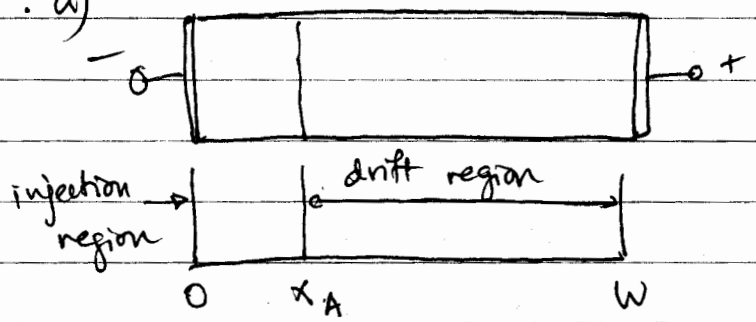
Q3 c) ii) Ultimately gate length is limited by tunnelling from source to drain at dimension of a few nm.

iii) Junction depth is controlled by doping of semiconductor. It is difficult to achieve very shallow junction due to diffusion of dopant.

[6]

(Bookwork)

Q4. a)



A schematic of an idealized IMPATT is shown above. Charge carriers are generated by impact ionization in the injection region which has high electric field. Those charges subsequently drift in the drift region which has low electric field to ensure no impact ionization. The time delay due to impact ionization and the drift time introduces a phase lag between the output current and the input voltage, producing the negative resistance. [4]

(Calculation)

b) $f = \frac{V_{sat}}{2(W - x_A)} = \frac{1 \times 10^5}{2(500 \times 10^{-9})} = 100\ GHz.$

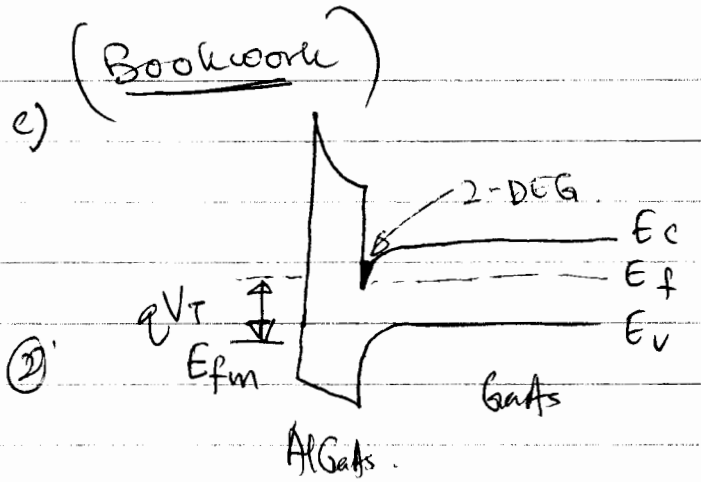
The total applied voltage = $(6 \times 10^7 \times 100 \times 10^{-9}) + (1 \times 10^7 \times 500 \times 10^{-9})$

$= 11\ V_{\#}.$

[3]

(Bookwork)

Q4 c)



(2)

i) At the threshold voltage, the bottom of the conduction band in GaAs surface coincides with E_f. Since GaAs is undoped and AlGaAs is heavily doped, electrons from AlGaAs diffuse to GaAs to form a 2-DEG channel. These electrons have high mobility due to absence of impurity scattering. Therefore a high f_T can be achieved.

[4]

(Bookwork)

ii) Pseudomorphic – growth of a strained channel using a thin layer of lattice mismatched semiconductor. The thickness has to be below the critical thickness.
(eg: InGaAs on GaAs/AlGaAs HEMTs).

(2)

Metamorphic – growth of relatively thick buffer layer that relaxes towards a new lattice constant to accommodate growth of alloy composition beyond the pseudomorphic case.

[2]

(Understanding)

iii) Pseudomorphic allows growth of InGaAs with higher mobility on (2) GaAs, however this is limited to low In composition only. Metamorphic allows use of InAs on GaAs. InAs has much (2) higher mobility than GaAs. This however still has dislocations that leads to poorer reliability.

[4]

(Calculation)

Q4. d) $g_m = \dfrac{a\,2qN_D\mu}{L}$ $\quad aN_D = 2DEG = 3\times10^{16}$

$$= \frac{3\times10^{16}\times1.6\times10^{-19}\times1.6}{100\times10^{-9}}$$

② $$= 7.68\times10^{4}.$$

① $$f_T = \frac{1}{2\pi\tau} = \frac{V_{sat}}{2\pi L} = \frac{1\times10^{5}}{2\pi\times100\times10^{-9}} = 159\ GHz.$$

[3]