Examination Feedback for EEE310 – Introduction to VLSI
Spring Semester 2006-07

Feedback for EEE310 Session:2006-2007

General Comments:

Less well attempted than I would have hoped. In some cases, answers betrayed a lack of understanding of even basic electrical effects and units, which I find disturbing.

Question_1:

This question was relatively well attempted. Most people made a reasonable job of producing an XOR gate (although some people were clearly working from an imperfect memory). The TG version was less well done. In some cases, people wired completely different signal to the true and inverted control inputs of the TG – this does not make sense. Furthermore, for section b.ii I did not give marks for merely adding an inverter because I asked for the *optimal* solution – this was rearranging the inverters at the inputs (one or other).

Question_2:

This question was not well attempted. Many people replaced the FFs with scan FFs but then did not wire up the scan chain properly (or at all) – it should be in a serial order (as shown in the notes). However, the part that people really seemed to have problems with was identifying the tests – 7 nodes, therefore 14 possible tests. These tests for different faults could be delineated and equivalent tests identified (along with tests that could be combined). Few people did this.

Question_3:

Quite a lot of people had difficulty with the capacitance. Each gate has 2 inputs (3fF each), one output (1.5fF) and 35um of wire at 0.2fF/um. Capacitance per gate = 3+3+1.5+35*0.2=14.5fF. There are 15x10^6 gates. Therefore, total capacitance is 217.5nF. Additionally, of prob of changing state=0.15 then alpha will be 0.075. In section d, there were many and various answers. Regardless of what they said was happening, some people just gave qualitative answers without justification – this did not gain marks. Clearly with scale factor, s = 1.4, cap -> 1/s (this is open to dispute because it depends on scaling wires down in height so I was flexible), f -> s, and Vdd -> 1/s. Overall, scaling of power should be s*s/(s*s*s)=1/s based on this analysis. Would have been happy not to scale f to get *equivalent* system.

Question_4:

Least-attempted question but, I thought, quite easy in parts. Most people who attempted it recognized what the pass-transistors were doing although converting this to a logic expression caused some problems. However, a few people completely misinterpreted it. Think of the pass transistors forming a tree with the root at the output. Each branch is controlled by switches, switched on by a signal or its inverse (so one path is always on). When you get back to a *leaf*, the logic state here defines the state of the root point when all the switches leading to it are on. Looking all terms, we have /C.1 + C(B.A+/B.0)=/C+C.B.A
The output is the inverse of this so Y=/(/C+CBA)=C./(ABC)=C(/A +/B +/C)=C/A + C/B