Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2013-14 (2 hours)

EEE6031 Advanced Computer Architectures 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. The pipeline shown in **Figure 1** is intended to process data as follows:

In →*P1*→ *P2*→ *P3*→ *P2*→ *P4*→ *P3*→ *P2*→ *P3*→ *P4*→ *Out*

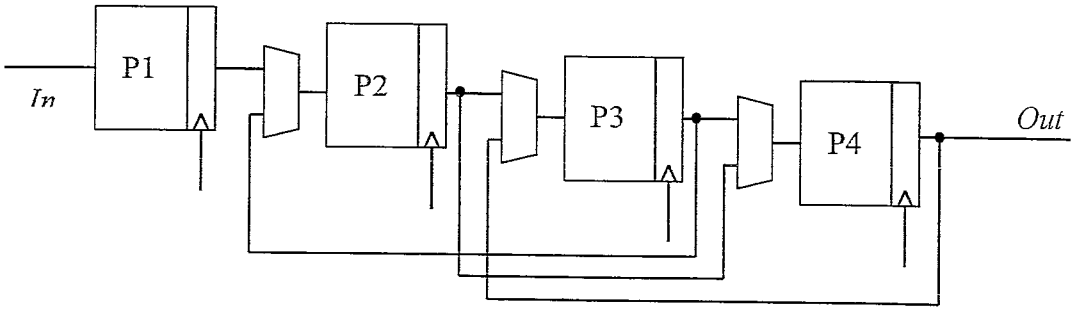

Figure 1: Processing Pipeline

For this processing activity:

i. Write down the reservation table; (8)

ii. Identify the data throughput and the processor utilisation; (2)

b. You notice that adding a single register, acting as a delay, will improve the data throughput of the pipeline in **Figure 1**.

i. Where should you put the delay? (4)

iii. How much will the performance improve? (6)

2. **a.** A pipelined processor will suffer from problems arising from data-flow dependencies. Describe:

i. how these problems arise; **(4)**

ii. two methods (other than reorder buffers) used to overcome these problems (you only have to give brief descriptions of the method – not too much detail). **(4)**

b. In some cases, a reorder buffer is used to solve problems caused by data/control dependencies in such pipelined processors.

i. Describe how such buffers are used and, in particular, identify the difference between instructions completing and committing. **(4)**

ii. For the following code snippet, show how a reorder buffer might be used:

```
        LOAD    @addr,R1    ; R1 ← addr
        MUL     R1,R2,R3    ; R3 ← R1 x R2
        CMP     R3,10       ; is R3 equal to 10
        JEQ     L1
        ADD     R4,R5,R1    ; R1 ← R5 + R4
        JMP     L2
L1      ADD     R4,R6,R1    ; R1 ← R6 + R4
L2      ...
```

(6)

c. What is meant by *precise* interrupts and a *precise* architectural state and what is their relevance to reorder buffers? **(2)**

3. **a.** A network of m processors is as shown in **Figure 3**. Three busses link the processors together allowing three communications in parallel *but* the processors do not support simultaneous internal processing and I/O. However, all internal activity in the processors runs in parallel.

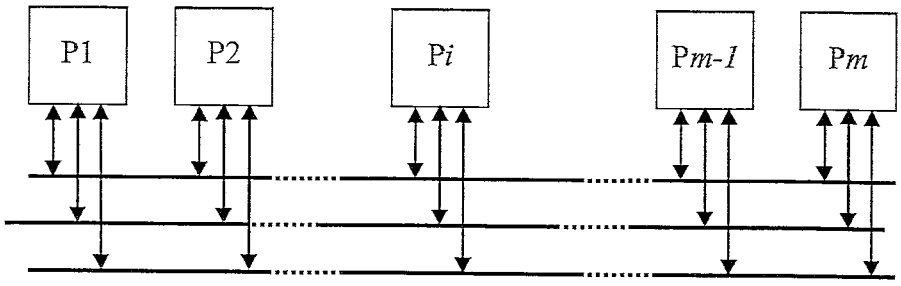

Figure 3: Network of Processors

n tasks are distributed across the m processors. All tasks are the same: the internal execution time of each task is t_{exe} and the total communication time between any two tasks is t_{int} if the two tasks are on the same processor and t_{ext} if the two tasks are on different processors. All tasks communicate equally with all other tasks.

i. Show that the total time spent on internal computation is:

$$\frac{n}{mt_{exe}}$$

ii. Show that the total number of task-task communications that need to be carried by the external busses is: **(3)**

$$\frac{1}{2}n^2\left(1-\frac{1}{m}\right)$$

(5)

iii. Hence, show that the speedup due to the parallelisation is:

$$speedup = \frac{6 \cdot m \cdot t_{exe} + m \cdot 3 \cdot (n-1) \cdot t_{int}}{6 \cdot t_{exe} + n \cdot (m-1) \cdot t_{ext} + 3\frac{(n-m)}{m} \cdot t_{\text{int}}}$$

(8)

iv. From this, show that parallelisation is only worthwhile when:

$$\frac{t_{exe}}{\frac{1}{3}t_{ext} - t_{\text{int}}} > \frac{n}{2} \text{ (approximately)}$$

for the case when $m \gg 1$, and $n \gg m$. (4)

4. a. There are a number of schemes for classifying processor systems. What are the objectives of processor classification? (3)

b. Describe Flynn's Classification. (3)

c. You estimate that an algorithm can be split into three sequential parts making up, respectively, 25%, 60%, and 15% of the algorithm: the first part can be parallelised four ways; the second part three ways; the third part two ways.

What speed-up could you expect to achieve? (6)

Which stage of the algorithm is the major limit to this speed up? (2)

d. You decide to implement the parallelised algorithm by mapping each separate, parallel part of the algorithm onto separate, identical processing units (rather than implementing the whole algorithm on a single such processing unit). What is the cost benefit ratio associated with this parallelisation? (3)

e. You recognise that, because the phases of the algorithm are sequential, the system could be used as a pipeline. What would the improvement in speed-up be in this case? (3)

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