Examination Feedback for EEE119 – Digital System Engineering
Spring Semester 2012-13

Feedback for EEE119 Session: 2012-2013

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

A reasonable attempt at the exam but still a disappointing average. Many students still loose marks on what should be straightforward bookwork. Many marks are also lost for poor diagrams with little or no explanation. When a question asks for an explanation or description a concept, it is not enough to just put a circuit diagram or truth table alone, some words of explanation are also required to obtain full marks.

Question 1:

a. Some explanation required in addition to the truth table and state diagram.
b. Generally well attempted. Maximum frequency is found from the longest combinational delay (critical path) and the delays associated with one flip-flop. Most students added up all of the delays in the entire circuit which is not correct.

Question 2:

a. Generally well attempted.
b. 8-to-1 mux should only have three select lines. Many students put an individual select line for each mux. The question also asks you to briefly explain the circuit. Very few students did this, effectively throwing away half of the marks.
c. Well attempted by those who knew what to do.

Question 3:

a. Well attempted.
b. Many explanations were vague. A clear, explicit explanation was required for full marks.
c. The question asked for a Moore type machine. Many solutions had a Mealy type state diagram with outputs on the directed arrows. A Moore type state machine should indicate the output in the state circle as the current output depends upon the current state, not the current input. Clearly label each of the states and describe what the state represents. Even if you do not get this entirely correct, you may pick up marks if the rest of the circuit is correct based on your own described states.

Question 4:

a. Both of De Morgan's theorems were required. Many students lost half of the marks by only producing one of them.
b. Many circuits contained a switch that produced a short circuit across the supply which would not work.
c. Many solutions had the S and R inputs connected the wrong way around.
d. Few successful attempts here. The question required you to draw a truth table in order to determine the correct combinational logic to drive the SR inputs.