Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (2.0 hours)

EEE119 Digital System Engineering

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. **i)** Find the decimal equivalent of the largest binary number that can be made with 7 bits. **(2)**

ii) Find the binary equivalent of the Binary Coded Decimal **0011 0010**. **(2)**

iii) What decimal number is represented by the 2s complement binary number **1101**? **(2)**

iv) How many bits of memory are available from the hexadecimal addresses **CE6** to **FD2** inclusive, if each location is 4 bits wide? **(3)**

b. Draw the truth table for a three input Exclusive OR function. Show how this could be implemented using only a 3-to-8 line decoder with active low outputs, plus one other logic gate. **(6)**

c. A synchronous sequential circuit is required that checks for even parity on an incoming serial data sequence. The circuit input ***I*,** presents a new data bit on each rising clock edge. The output *Z* must be high whenever the parity of the sequence received up to that point is even. *Z* must be a function of the present state only.

Define the required states and hence draw a state diagram for this circuit.

(a state transition table, state equations and a circuit diagram are not required) **(5)**

2. a. **i)** Explain the terms 'setup time' and 'hold time' for a flip-flop. **(2)**

ii) Explain the term 'critical path' when applied to a sequential logic circuit. **(2)**

iii) Explain what you understand by the term 'metastability' when applied to sequential logic circuits. **(3)**

b. A shift register is constructed with four flip-flops, and the output from the last flip-flop is inverted and then fed to the input of the first flip-flop. The initial state of the register is set to 0110.

i) Draw a circuit diagram for this configuration and describe, using a table of sequential values, what happens when a series of clock pulses is applied to the register. **(5)**

ii) Does the register ever return to its original state? If not, why not? If it does, how many clock pulses are needed? **(2)**

iii) How are your results changed if the initial state is set to 1111 instead? **(2)**

iv) What will happen if any other initial state is chosen? **(1)**

v) What is the maximum theoretical frequency of operation of this shift register if the propagation delay of the inverter is 2ns, the propagation delay of a flip-flop is 5ns and the setup time of a flip-flop is 3ns. Assume that the hold time is negligible. **(3)**

3. a. The Consensus theorem in Boolean Algebra is given by:

X.Y + X'.Z + Y.Z = X.Y + X'.Z (where **X'** represents **NOT X**)

i) Write down the dual of this expression. **(2)**

ii) Prove the Consensus theorem by truth table or otherwise. **(4)**

b. Draw a truth table for the Boolean function **F**, described by the maxterm list

F(A,B,C) = Π (0,2,3,7) **(2)**

Show how this could be implemented using:

i) 8-to-1 multiplexer **(2)**

ii) 4-to-1 multiplexer and a logic inverter **(4)**

c. Show how you could construct a 2K byte wide Read Only Memory (ROM) using two 1K byte wide ROM chips. Clearly show any required control lines and describe how your addressing scheme works. **(6)**

4. **a.** Explain, with the aid of a truth table, the function of:

i) 2-to-1 logic multiplexer. **(4)**

ii) 2-to-4 line decoder with active high outputs **(4)**

b. Draw the truth table for a two input XNOR gate. Show, using Boolean Algebra and a circuit diagram, how this XNOR gate could be implemented using only AND gates and inverters. **(4)**

c. A Moore type state machine is required that can detect a sequence of three consecutive **1**'s on its serial input line. It has a single bit output *Z* and a single bit input *I* which receives the serial input sequence. When a sequence has been detected, the output *Z* should be set high. The machine should then reset and look for a new sequence, with the next input *I*.

Draw a state diagram for this system and a state transition table, clearly labelling the states. A circuit implementation is not required. **(8)**

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