The University Of Sheffield.

Data Provided:

Thermal conductivity aluminium = 150 W/m°C

WORKED SOLUTIONS

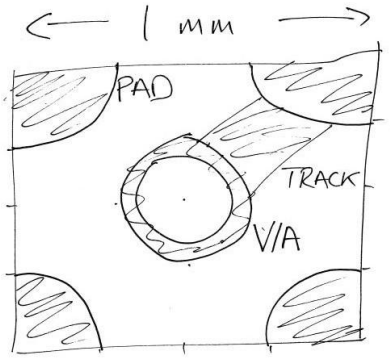
DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

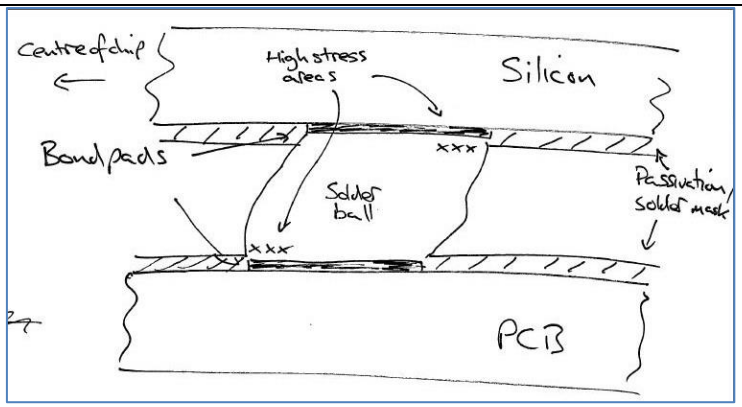
Spring Semester 2015-16 (2.0 hours)

EEE6214 Packaging and Reliability of Microsystems

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1.	**a.**	Standard method for singulation is by use of a wafer saw. High speed (3000rpm), diamond tipped, water cooled. Wafer attached to backing tape to prevent individual chips from flying off. Saw blade width ~ 0.3mm. Limitation: can only cut in straight lines; debris may damage ICs; heat generated may damage ICs; sequential process, hence fairly slow; large amounts of (expensive!) lost.	(4)
	b.	Laser singulation. Plasma singulation. Both allow non-rectangular IC shapes. Thinner cuts. Less thermal damage. Reduction/elimination of debris.	(2)
	c.	Wafer level test, using flying probes or probe card. Done in order to avoid the effort of packaging failed ICs.	(2)
	d.	BGA: 30x30 pins; pitch = 1 mm Worst case scenario: routing to centre of array with a single layer PCB. Need to route14 connections between the two outer pads, hence 29 tracks/gaps in 0.5 mm (assuming equal track and gap), hence track width = 1/58 mm = 17 µm. this is an unfeasibly small value for a PCB. Solution is to use a multilayer PCB… … with one via positioned between each set of 4 pads and a short track connecting it to pad (as per sketch below). PCB needs to be multilayer in order to route tracks. Full marks if a sensible analysis of number of routing layers is attempted (i.e. with sensible PCB line	(4)

		widths > 100 µm).  	
	e.	Temperature control in 3d MCMs is difficult because of high Si packing density. Normally heat sink is put close-by top surface of Si, but in 3d this cannot be done. Possible innovative solutions (they may come up with others!) - water cooling? – either heat pipe or pumped - avoid underfill, thus allowing room for air cooling between layers? - incorporate Peltier coolers into stack? - clever stack design to eliminate hot spots? 3d MCM advantages over a) SIP: smaller; short interconnection lengths b) SOC: heterogeneous integration; shorter design time; less hassle with IP	(4) (3)

2.	**a.**	Wave soldering process: 1 Plated through hole (PTH) on PCB, long pins on package; 2 Insert, cut and bend pins; 3 Immerse in molten solder bath, solder mask prevents shorts; 4 Components usually on top side of board (else immersed in molten solder!) Small passives on bottom surface of PCB if tacked in place with adhesive. Heat and solder applied simultaneously.	(3)
	b.	Wave soldering still used for attaching through hole connectors. It's a much more robust attachment, hence good for components that experience high and repeated forces.	(1)
	c.	 PCB has larger thermal expansion coefficient than silicon, hence, on cooling	(4)

from reflow temperature to room temperature the PCB contracts more than the silicon. The ductile solder ball changes shape to compensate for this change in geometry. Repeated temperature cycling will lead to failure (i.e. cracking) of the ball in the high stress areas.

The stress in the corners of the solder ball can be reduced by using an underfill material to fill the voids between the solder balls. This reduces the effective TCE mismatch between the silicon and the substrate. The underfill material is typically a low-viscosity silica-loaded epoxy resin.

d.

i)

For safety critical Si, T_{max} = 80 °C. Assume room temperature = 20 °C.

Hence ΔT = 80-20 = 60 °C

Assume that all heat is extracted via the metal leads.

$R_{lead} = L/(k_{Cu}*A)$

Where :

L = 5 mm = $5x10^{-3}$ m ; k_{Cu} = 390 W/m °C; A = 20*0.5mm^2 = $10x10^{-6}$ m^2

Hence R_{lead} = 3.3 °C/W

R_{pcb} = 10 °C/W (given)

Hence :

Total thermal resistance through substrate, $R_{sub} = R_{lead} + R_{pcb}$ = 11.28 °C/W (2)

Hence: $Q_{max} = \Delta T/R_{sub}$ = 60/13.3 = 5.3 W

ii)

For consumer grade Si, T_{max} = 125 °C. Assume room temperature = 20 °C.

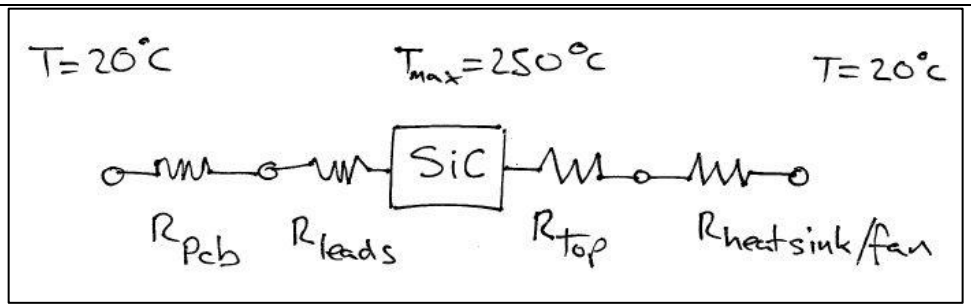
Hence ΔT = 125-20 = 105 °C

Hence, maximum thermal resistance $R_{max} = \Delta T/Q$ = 105/12 = 8.75 °C/W

This required value for R_{max} is *less* than the stated value for the PCB thermal resistance (10 °C/W), so, regardless of the thermal resistance of the leads, the thermal resistance is too high, hence this package is NOT OK for the IC. (2)

e.

i)



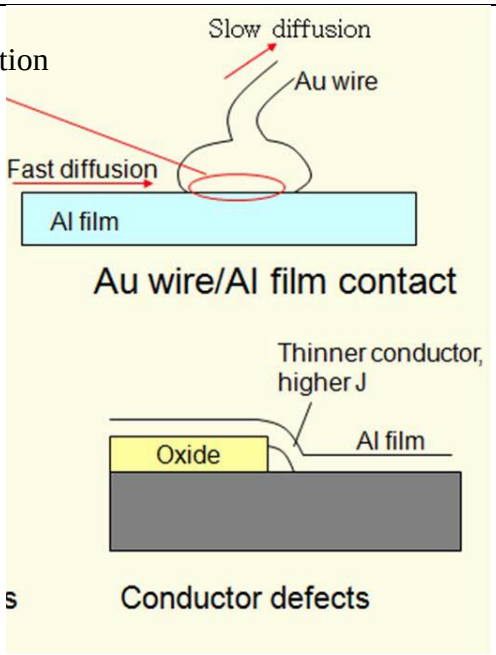
ii) T_{max} = 250 °C, hence ΔT = 250-20 = 230 °C

Q = 30 W (given)

Two pairs of resistors in parallel, hence :

$R_{total} = ((R_{pcb} + R_{lead}) * (R_{top} + R_{heatsink}))/(R_{pcb} + R_{lead} + R_{top} + R_{heatsink})$

		$\Delta T = Q(R_{total})$ hence, rearranging leads to : Max. $R_{heatsink}$ = <u>10.5 °C/W</u> iii) At high altitude the density of air will be less, hence the cooling provided by the fan will be less, hence the chip will be hotter than the safe maximum operating temperature and may fail.	(5)

3	**a.**	i) MOSFET radiation damage: Radiation particles can easily produce e-h+pairs in SiO_2. Ionization energy of SiO_2 = 17eV. 1 rad generates 10^{13}pairs/cm^2. Mobile electrons extracted, holes are trapped at the Si/SiO2interface. Positive charge reduce the threshold voltage by $\Delta Vt = Qox/Cox$ causing MOSFETs to turn on at lower applied voltage and large leakage currents.Vt can be large before irradiation, but thick oxide suffers large ΔV. ii) Radiation creates e-h+ pairs which are trapped in defect sites in the fibre creating new energy levels that absorb light. This ↑ optical loss which can be observed from darkening of fibre. Amount of loss depends on dose, temperature, composition and uniformity of fibre. iii) Photodiodes suffer surface currents from ionization (the bulk detector is insensitive to ionization) and increased dark current from physical formation of defects. Positive charge in passivation - leakage path shorting pn junction. Recombination of photogenerated carriers reduces signal. Localised breakdown could also occur.	**(2)** **(2)** **(2)**
	b.	accumulation  i) E_a of GB diffusion higher in Au than Al and density of GBs lower in bulk Au wire than thin Al, leads to accumulation under joint – distortion/cracking ii) Current density higher through thinner region over step leads to higher temp and enhanced electromigration. May also be a void increasing temperature.	**(2)** **(2)**

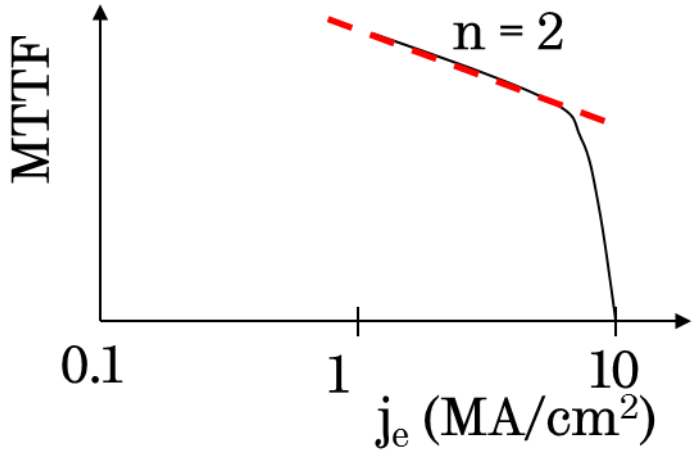
c.

i)

$$MTTF^{-1} = Bj_e{}^{n} \exp\left[-\frac{E_a}{kT}\right]$$

B is a constant, E_a is the activation energy and j_e is the current density. At low current densities n = 2. **(2)**

ii)



(2)

iii) Black's assumption supported at low J (ie. <2x10^{6}Acm^{-2}). **(1)**

iv)

$$AF = \left(\frac{J_{stress}}{J_{use}}\right)^{n} exp\left[-\frac{E_a}{k}\left(\frac{1}{T_{stress}} - \frac{1}{T_{use}}\right)\right]$$

$$AF = \left(\frac{4 \times 10^5}{2 \times 10^5}\right)^{2} exp\left[-\frac{0.5}{8.617 \times 10^{-5}}\left(\frac{1}{373} - \frac{1}{303}\right)\right]$$

AF= 145.5

MTTF(use) = AF × MTTF(stress) = 145.5 × 2000 = 291000 = <u>33 years</u> **(5)**

4. **a.**

a) i) gold wire displacement can be observed with X-radiography prior to opening package. **(3)**

ii) intermetallics best observed using IR-microscopy (SAM only really useful for voids). Prep by removing backside of package. **(3)**

iii) popcorn cracking using SAM (no removal of packaging needed) **(3)**

b.

Possible failure anaylsis process flow:

Examine prior to opening

Microscope (corrosion, whiskers)

X-ray radiation (internal geometry, physical defects, bond wires, solder)

IR microscopy

Package opening/encapsulation removal **(3)**

		Grid/mill lid off (check mechanical damage, corrosion, misalignments) Internal examination initially using optical microscope (eg check facets for COD) then via SEM Remove chip and apply selective layer removal e.g. for ESD, EOS, sub-surface evidence. Layer removal by ion milling once identified defect location. TEM of defect or SIMS analysis	
	c.	Yield = 0.98^2 x 0.99^8 x 0.85 = <u>75 %</u>	**(3)**
	d.	The critical area is the area that will cause a 'hard' failure of the circuit. This can be approximated to a square with a size determined by the inter-track spacing. If we assume equal track and gap, then, for a pitch of 1mm: A_c = 0.5 x 0.5 mm = 0.25 mm^2 Hence: FY = (1 – exp(-2 x 0.25 x0.1)) / (2 x 0.25 x 0.1) = 1 – $e^{-0.05}$ / 0.05 = <u>97.5 %</u>	**(5)**

GLW / KG