Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE6206 Power Semiconductor Devices

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** List the main differences in electrical properties between metals, insulators and semiconductors. **(2)**

b. Briefly discuss the main difference between direct and indirect bandgap semiconductors, providing an example of each type. **(3)**

c. Define the terms Fermi-level and thermal runaway in a semiconductor. **(4)**

d. Briefly describe what is meant by an intrinsic semiconductor **(2)**

e. Taking care to comment on any key issues, determine whether a Silicon ingot with an n type doping of $1\times10^{15}/cm^3$ operating at 250^oC (523K) has reached its maximum operational temperature.

(Hint: You may assume the maximum temperature of operation of a semiconductor occurs when the intrinsic carrier concentration is the same as the background doping). **(5)**

f. Calculate the Fermi-level position from the intrinsic energy level of a Silicon ingot of p type doping of $5\times10^{15}/cm^3$ at 27^OC (300K), assuming complete ionisation of impurities. **(4)**

Question 1 answer sheet

Question 1a)

Metals are good conductors of electricity. Insulators are bad conductors of electricity. Similarly, semiconductors are partial conductors of electricity, which means their conductivity lies between conductors and insulators.

Metals: In case of metals, electrons fill the conduction band partially. The overlapping of both the bands i.e. valence and conduction band also take place. This shows that no forbidden energy gap is present.

Insulators: In case of insulators the forbidden energy gap is extremely high as compared to the conductors. Its valence band is fully filled with the electrons, whereas its conduction band is empty.

Semiconductors: In case of semiconductors the conduction band is empty and the valence band is fully filled with electrons. Unlike insulators, energy gap is not so large in semiconductors. In these materials, the resistances can be modulated by doping with impurities.

(any two features listed above)

Question 1b)

In a **direct band gap semiconductor**, the top of the valence band and the bottom of the conduction band occur at the same value of momentum. (GaAs)

In an **indirect band gap semiconductor**, the maximum energy of the valence band occurs at a different value of momentum to the minimum in the conduction band energy. (Silicon)

Therefore, the movement of carriers from the valance band to the conduction band of an indirect band gap semiconductor requires a change in energy as well as momentum, while it only requires change in energy in direct bandgap semiconductors.

(any three from the above)

Question 1c

The energy level (if it exists) which has a 50% probability of being occupied by an electron at any temperature.

Thermal runaway refers to a situation where an increase in temperature changes the conditions in a way that causes a further increase in temperature, often leading to a destructive result. It is a kind of uncontrolled positive feedback.

(2 mark for Fermi level position, 2 marks for the definition of thermal runaway, decription via illustration is also acceptable: 2 key features of both)

Question 1d

An intrinsic semiconductor, also called an undoped semiconductor or i-type semiconductor is a pure semiconductor without any significant dopant species present. The number of

charge carriers is therefore determined by the properties of the material itself instead of the amount of impurities.
(any two features of the above)

Question 1e

$N_C = 4.83 \times 10^{15} T^{\frac{3}{2}}$ $N_V = 1.71 \times 10^{15} T^{\frac{3}{2}}$ $ni^2 = N_v N_c exp\frac{-qE_G}{kT}$

At 250^{O}C, N_C = 5.77E19/cm^3, N_v = 2.05E19/cm^3 and ni = 1.4E14/cm^3. Material is below its maximum operating temperature for the condition given.

(4 marks for using correct formula, constants and calculations, 1 mark to identify that the material is below its maximum operation temperature (sting))

Question 1f

$$E_i - E_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 0.0259\ln\left(\frac{5\times10^{15}}{1\times10^{10}}\right) = 0.34\text{eV}$$

Fermi level position is 0.34eV below the mid band energy level

(4 marks for using the correct formulae and obtaining the correct result)

2. **a.** Describe two techniques to form junctions in high voltage devices during the device fabrication process, taking care to explain how these techniques are used to form structures at the cathode and anode region of the device. **(3)**

b. Explain why shallow and short n+ source/cathode regions are formed with impurities of a low diffusion coefficient in n-channel MOSFETs or n-channel IGBTs. Comment on why is it important to keep such regions shallow. **(3)**

c. Calculate the built-in potential of the following:

i) Silicon PN junction with an acceptor doping concentration of $1\times10^{18}/cm^3$, donor concentration of $1\times10^{13}/cm^3$, and an intrinsic carrier concentration of $1\times10^{10}/cm^3$ at $27^{O}C$ (300K). **(5)**

ii) Discuss any difference between current voltage characteristics if the semiconductor material was changed from Silicon to Silicon Carbide. **(3)**

d. Calculate the drift region width and concentration for a Silicon Carbide PiN structure for a voltage rating of 3300V. Assume a 20% pass band. **(6)**

Question 2 answer sheet

Question 2a
Ion implantation and anneal
Epitaxial growth;
Deep diffusion from solid sources
Ion implantation is compatible with photo-lithography techniques and is used to form complex structures on the semiconductor surface.
Epitaxial growth is used to form uniform drift regions onto of handle wafers of higher doping concentration.
Deep diffusion from solid sources are used to form very deep junctions (such as Aluminium).

(3 marks for 2 processes and description)

Question 2b
An ion with low diffusion coefficient would result in a shallow junction with high doping concentrations after thermal activation. Shallow and heavily-doped source/cathode junctions result in ohmic contact. The activation of parasitic inherent transistors/thyristors in MOSFETs/IGBTs are proportional to the length of the n+ cathode region and therefore needs to be minimised.

(any 3 from the above)

Question 2c(i)

i) $V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{{n_i}^2}\right) = \left(\frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}}\right) ln\left[\frac{1\times10^{18}\times1\times10^{13}}{(1\times10^{10})^2}\right] = 0.655V$

Question 2c (ii)
Due to the larger band gap a silicon carbide device would exhibit a higher knee voltage (Vbi). Therefore the device would turn on at a higher voltage than that of silicon and display a larger forward voltage drop.

(up to 5 marks for calculation, any three points for 2c(sting))

Question 2d

$Break\ down\ voltage\ (V) = \frac{{E_c}^2\varepsilon_o\varepsilon_S}{2qN_D}$ Depletion width $(W_{max}) = \sqrt{\frac{2\varepsilon_S BV}{qN_D}}$

$N_D = \frac{{E_c}^2\varepsilon_S}{2qV}$ $N_D = \frac{(3\times10^6)^2\times9.8\times8.85\times10^{-14}}{2\times1.6\times10^{-19}\times3960} = 6.2\ \times 10^{15}/cm^3$ (3 marks)

$W_{max} = \sqrt{\frac{2\times9.8\times8.85\times10^{-14}\times3960}{1.6\times10^{-19}\times6.2\times10^{15}}} = 26.3\mu m$ (3 marks)

(up to 4 marks for the calculations required (2 marks sting – using the correct pass band voltage and not voltage rating))

3. **a.** Draw and label the metal semiconductor energy band diagram for a metal contact to an n-type semiconductor for the following conditions

i) Thermal equilibrium, **(2)**

ii) Forward biased, **(2)**

iii) Reverse biased. **(2)**

Provide labels for the Fermi Level, Work Functions, Conduction Band, Valence Band, Vacuum level and ground state.

By reference to these band diagrams describe the on-state and off-state behaviour. **(2)**

b. Describe the on-state conduction mechanism of a Schottky diode. **(1)**

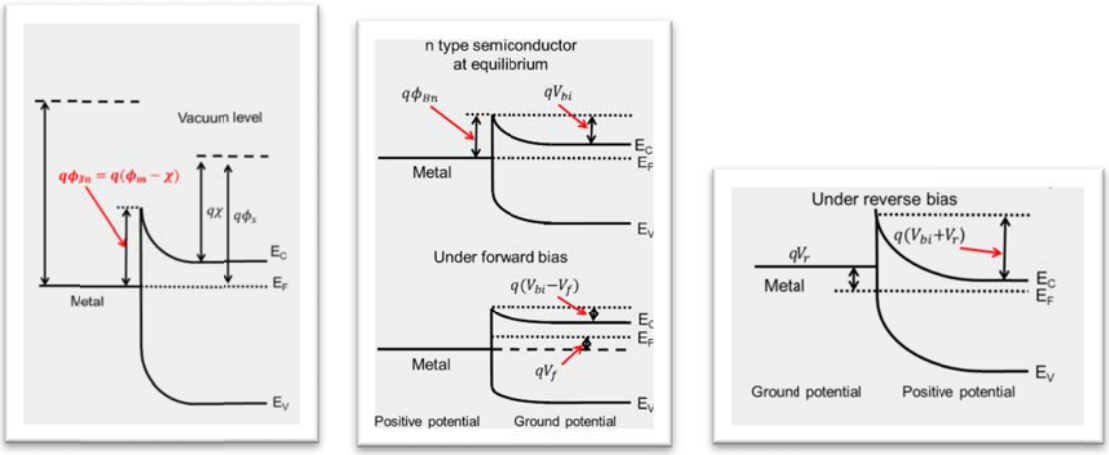
How does it differ from a PiN diode? **(1)**

What differences would you find if you compare on-state and switching characteristics of high voltage PiN and Schottky diodes? **(2)**

c. Calculate the on-state forward voltage drop of a Silicon Carbide Schottky diode operating at a current level of 100A. The drift region thickness is 10μm and a doping concentration of $1\times10^{15}/cm^3$. The cross-section area of the die is 5mm x 5mm and it has a built in potential of 0.9V. **(8)**

Question 3 answer sheet

Question 3a:



(6 marks for band diagrams for all three conditions highlighting the required labels)

At thermal equilibrium, the difference between metal and semiconductor work functions sets up energy barrier, which carriers need to overcome for conduction. Positive potential applied to the metal lowers the barrier (on-state) and the negative potential applied to the metal increases the barrier (off-state)

(2 marks for two from the above)

Question 3b

Schottky diodes are majority carrier or unipolar devices. That is, they only use the majority carrier for conduction therefore they show no tail current during switching. PiN diodes are bipolar, using both carriers for conduction. The bipolar carrier conduction causes conductivity modulation within the drift region, substantially reducing it resistance. These carriers need to be removed during the switching transient causing reverse recovery.

(majority carrier device (1) PiN diode are bipolar (1) any two other key differences)

Question 3c

$$\rho = \frac{1}{q\mu_n N_D} = \frac{1}{1.6 \times 10^{-19} \times 1450 \times 1 \times 10^{15}} = 4.3\Omega - cm$$

$$R = \rho \frac{L}{area}\ 4.3 \times \frac{10 \times 10^{-4}}{0.5 \times 0.5} = 17.2m\Omega$$

$$V_f = (IR) + V_{bi} = (100 \times 17.2 \times 10^{-3}) + 0.9 = 2.62V$$

(5 marks for using equations to obtain resistance, 3 additional marks to calculate the forward drop (equation not given - sting)

4. **a.** i) Draw the forward current voltage characteristics of a high voltage bipolar transistor including open base and open emitter breakdown performance. **(4)**

ii) Explain the breakdown mechanism for open base operation and comment on how this compares to the maximum breakdown voltage. **(3)**

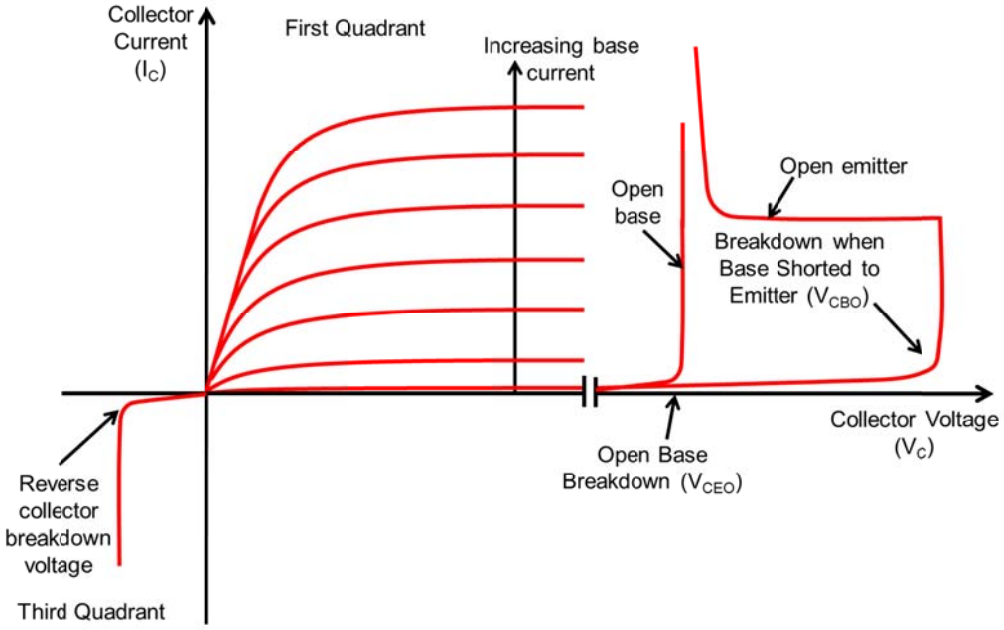
b. Consider a silicon BJT transistor with an N- collector thickness of 100μm. Calculate the breakdown voltage of a punch through BJT operated in a shorted emitter configuration. Consider an N-doping concentration of $1\times10^{14}/cm^3$ and critical electric field strength of $2\times10^5 V/cm$. **(4)**

c. To the nearest 100V, what is the breakdown voltage of the structure in part (b) if the drift region doping concentration is increased to $5\times10^{14}/cm^3$ and the critical electric field remains at $2\times10^5 V/cm$. You may assume that the electric field profile is triangular. Hint; calculate depletion layer thickness and electrical field strength at an applied voltage of 500V. Vary this voltage until maximum breakdown voltage is obtained. **(5)**

d. Draw and label the current voltage characteristic of a thyristor. Label any key features and define the switching current and holding current. **(4)**

Question 4 answer sheet

Question 4a



Open base: In an open base circuit, when positive potential is applied to the collector, the base/emitter junction becomes forward biased and base-collector is reverse biased. Leakage current flowing through the structure into the base-emitter junction and is amplified by the gain of the transistor, reducing breakdown voltage. During open emitter operation the base is connected to ground eliminating this gain and increasing the breakdown performance. Under high collector current levels breakdown voltage reduces to open emitter condition.

(4 marks to reproduce image with at 3 key features, 3 marks for any three of the above)

Question 4b

$$BV_{PT} = 2 \times 10^5 \times 100 \times 10^{-4} - \frac{1.6 \times 10^{-19} \times 1 \times 10^{14} \times (100 \times 10^{-4})^2}{2 \times 11.7 \times 8.85 \times 10^{-14}} = 1228V$$

(up to 4 marks)

Question 4c

Starting the analysis at 500V:

$$W_{max} = \sqrt{\frac{2\varepsilon_r \varepsilon_o BV}{qN_D}} \qquad W_{max} = \sqrt{\frac{2\times11.7\times8.85\times10^{-14}\times500}{1.6\times10^{-19}\times5\times10^{14}}} = 36\mu m$$

$$E_c = \frac{2V}{W} = \frac{2\times500}{50.8\times10^{-4}} = 2.78 \times 10^5 \text{ V/cm}$$

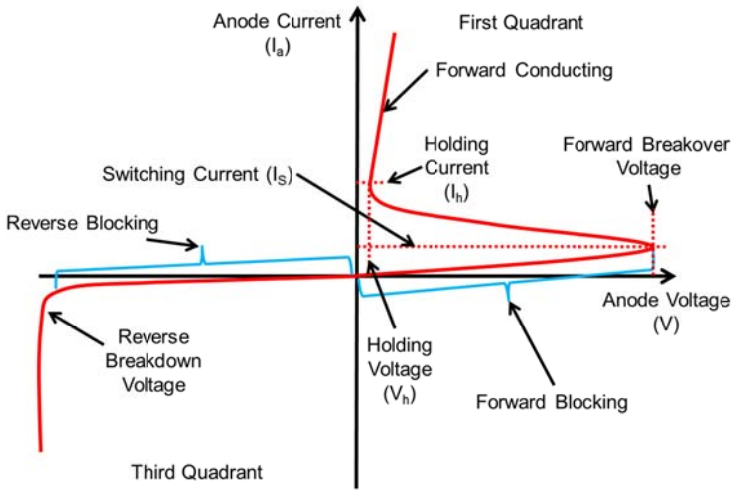
(3 marks)

The hinted start point is above the critical electric field strength. Repeating this equation with respect to voltage (at least one iteration) (1 mark)

Obtaining the correct solution ~200V (1 mark)

V	W (um)	Ec V/cm
500	35.98	277958.8
400	32.18	248613.9
300	27.87	215306
200	22.75	175796.6

Question 4d



Switching current: The minimum anode current that must flow through the SCR in order for it to switch from forward blocking to forward conducting. Voltage at which this occurs is the forward break over voltage.

Holding current or latching current: Minimum value of anode current required to maintain the SCR in the conducting state, holding voltage is the voltage at which this occurs.

(2 marks for the image and two labels, 1 mark for a key feature of holding current, 1 mark for a key feature of latching current)

5. **a.** Draw and label a Metal-Oxide-Semiconductor energy band diagram for a p-type semiconductor for the following conditions:

(i) Flat-band condition, **(3)**

(ii) Accumulation, **(3)**

(iii) Inversion. **(3)**

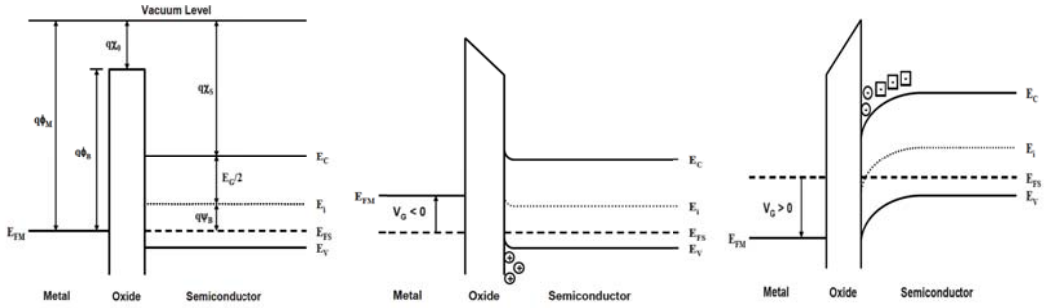
Define Threshold voltage of a MOSFET using these energy band diagrams. **(2)**

b. Calculate the threshold voltage of an n-channel MOSFET with an oxide thickness of 100nm and a p-body doping of $1\times10^{17}/cm^3$ at both room temperature and at 125^oC (398 K). **(4)**

c. Draw a cross-section through a power MOSFET taking care to label any significant features including practical elements. List the parasitic capacitances in this device and how do they influence its switching behaviour? **(5)**

Question 5 answer sheet

Question 5a



Energy band diagram at flat band condition and Energy band diagram under accumulation condition

(3 marks for each figure with correct material labels and at least 2 additional labels)

Energy band diagram under strong inversion condition. The voltage applied at the gate, to enable the strong inversion is called threshold voltage. This condition is reached when the electron density exceeds the majority carrier density in the bulk in an N-channel device.

(Two marks for two points from the above – sting relating inversion with threshold)

Question 5b

$$V_{TH} = V_{FB} + 2\psi_B + \frac{t_{OX}}{\varepsilon_{OX}}\sqrt{2qN_A\epsilon_{si}(2\psi_B)} =$$

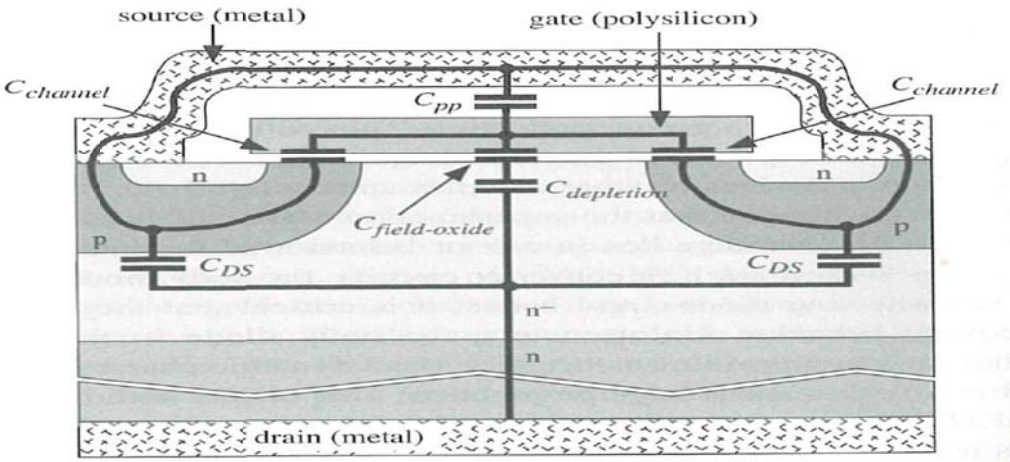
$$1 + 2 * \left(\frac{400 * 1.3810^{-23}}{1.63 * 10^{-19}}\right) * ln\left(\frac{10^{17}}{10^{10}}\right)$$

$$+ \frac{100 * 10^{-9}}{3.9 * 8.85 * 10^{-14}}\sqrt{4 * 8.85 * 10^{-14} * 11.7 * 1.38 * 10^{-23} * 400 * 10^{17} * \ln\left(\frac{10^{17}}{10^{10}}\right)}$$

$$= 2.1473\ V$$

(up to 4 marks for calculation)

Question 5c



The switching transients are mainly determined by the charging and discharging processes of its internal capacitances.

- The Gate-Source Capacitance C_{GS}: $C_{channel}$ and C_{pp}
- The Gate-Drain Capacitance C_{GD}: $C_{field-oxide}$ and $C_{depletion}$
- The Drain-Source Capacitance C_{DS}
- The Input Capacitance: $C_{iss} = C_{GS} + C_{GD}$
  The Output Capacitance: $C_{oss} = C_{DS} + C_{GD}$

(4 marks for image with three capacitors labelled, 1 mark to link the capacitance with switching behaviour)

6. **a.** Briefly describe two main differences between a Power MOSFET and an IGBT **(2)**

b. Describe the main differences between PT, NPT and FS technologies in an IGBT **(3)**

c. Briefly describe the phenomena of latch-up in an IGBT and discuss means of minimising this effect. **(2)**

d. Describe the operating behaviour of a reverse-Conducting IGBT, the means by which it can be realised in practice and its principal benefits. **(5)**

e. Draw cross-sections through typical planar and trench IGBT structures and discuss the differences in their operation. **(5)**

f. List the factors and the effects of gate resistance of an IGBT device performance. **(3)**

Question 6 answer sheet

Question 6a

In an IGBT, the n+ drain is replaced by p+ anode. This results in bipolar mode of conduction, controlled by a MOSFET. The MOSFET begins to conduct at a drain voltage above 0 V, as long as the gate voltage is above its threshold voltage. The IGBT begins to conduct only when the anode voltage exceeds its bipolar on-set voltage. Due to bipolar conduction, the turn-off loss of an IGBT much higher than that of an equivalent MOSFET of similar capacitances. However, with the conductivity modulation, the on-state resistance of an IGBT is much lower than its equivalent MOSFET.

(2 from the above)

Question 6b

Comparison of PT, NPT and FS characteristics

Structure	PT-IGBT	NPT-IGBT	FS-IGBT
Drift layer thickness	Thin	Thick	Thin
Wafer type	Epitaxial	Float Zone	Float Zone
Buffer layer	Thick and highly doped	N/A	Thin and lowly doped
P+ collector	Thick and highly doped	Thin and relatively lowly doped	Thin and relatively lowly doped
Bipolar gain control	Lifetime killing	Injection efficiency	Injection efficiency
On-state losses	Low	Medium	Low
Switching losses	High	Medium	Low
Turn-off tail	Short	Long	Short
Temperature coefficient	Negative	Positive	Positive
SCSOA (short circuit conditions)	Medium	Large	Large
RBSOA (reverse bias conditions)	Narrow	Large	Large
Device in parallel	Hard	Easy	easy

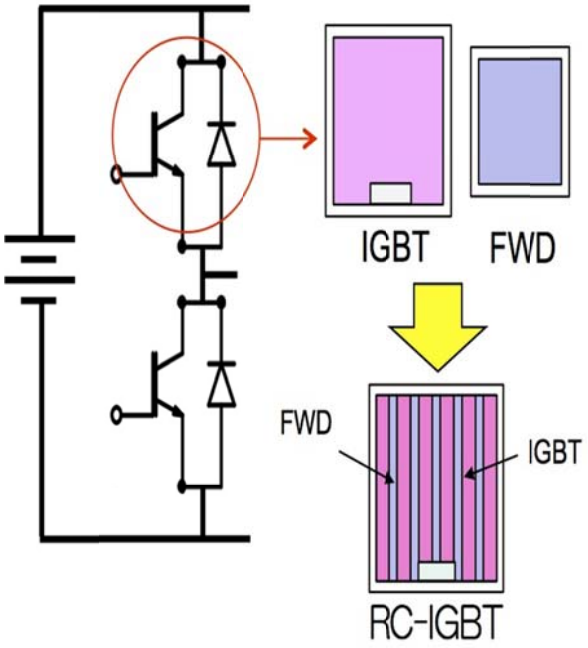
(3 from the above table)

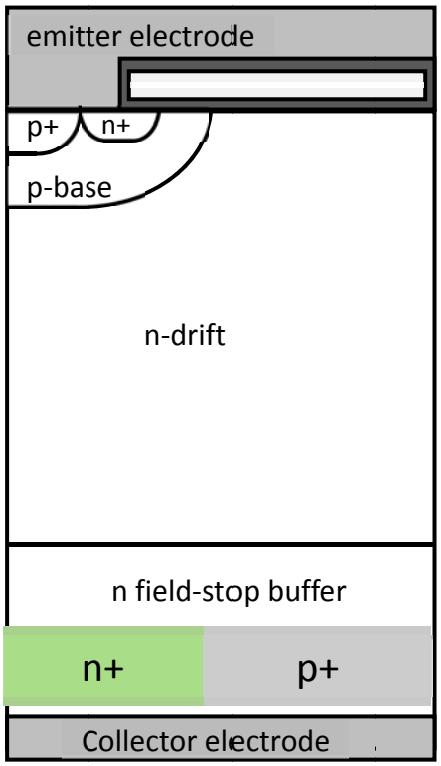
Question 6c

Latch-up occurs when the NPN transistor formed by the n+ emitter/P-base/n- drift region is turned on. To minimise the occurrence of the latch up, the n+ region has to be kept small and the conduction in the P base region needs to be increased.

(2 marks from the above)

Question 6d





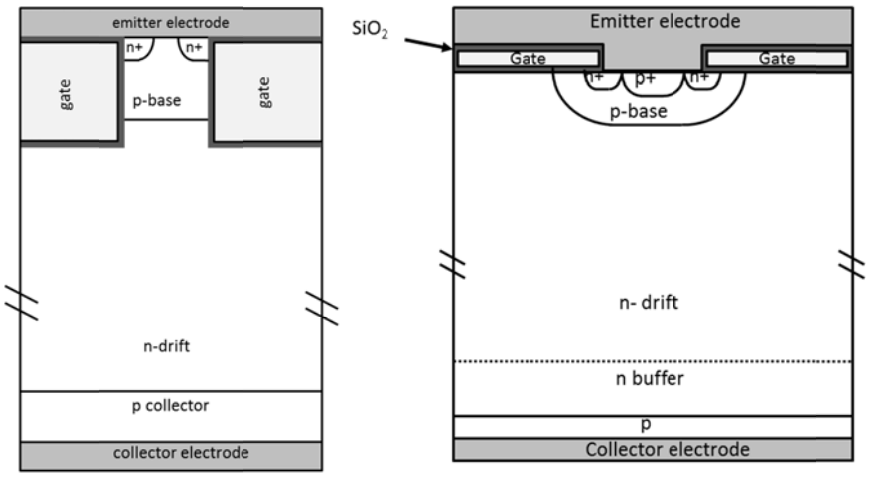
Structure of an RC-IGBT

The benefits of the combination of the IGBT and diode:

- Improved performance for module area
- Reduction of the chip size
- Reduction in temperature ripples per chip
- Improved flexibility for optimal thermal properties in power module

(3 marks for the images, 2 marks for at least 2 benefits)

Question 6e



- The trench gates provide higher channel density for the MOSFET portion

- show improved on-state voltage drop compared to planar gate devices due to the elimination of the JFET component
- higher cell packing density
- vertical current flow during conduction.
- Due to smaller cell size of the Trench IGBT, it has higher saturation current than planar IGBT. Its short circuit capability is limited as increase power dissipation.
- Planar IGBT also has the disadvantage of a high on-state voltage drop.
- By intentionally making a portion of active trench cells disconnected (dummy cells). It reduces the saturation current at the expense of sacrificing $V_{ce(sat)}$

  (figures and any three of the above)

(3 marks for images 2 marks for at least 2 features)

Question 6f

Characteristics	**Rg ↑**	**Rg ↓**
Turn-on time loss, t_{on}	↑	↓
Turn-off time loss, t_{off}	↑	↓
Turn-on energy loss, E_{on}	↑	↓
Turn-off energy loss, E_{off}	↑	↓
Turn-on peak current	↓	↑
Turn-off peak current	↓	↑
dV/dt	↓	↑
di/dt	↓	↑
Voltage spike	↓	↑
EMI noise	↓	↑

Any three from above table