EEE105 - Solutions 2004-5 Paper

1 a. [Bookwork]: diode and satuaration current given in table of formulae. This actually combines two different derivations in the notes so in not as trivial as it might seem.

The diode equation is

$$J = J_0\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

Where

$$J_0 = \frac{qL_e n_p}{\tau_e} + \frac{qL_h p_n}{\tau_h}$$

This equation represents the sum of the electron and hole currents in the material
Thus we can write that the ration of electron and hole currents as:

$$\frac{J_e}{J_h} = \frac{\frac{qL_e n_p}{\tau_e}\left[\exp\left(\frac{qV}{kT}\right)-1\right]}{\frac{qL_h p_n}{\tau_h}\left[\exp\left(\frac{qV}{kT}\right)-1\right]} = \frac{L_e n_p \tau_h}{L_h p_n \tau_e}$$

now using $n_p = \frac{n_i^2}{p}$ and $L = \sqrt{D\tau}$ we can get

$$\frac{J_e}{J_h} = \frac{L_e n_p \tau_h}{L_h p_n \tau_e} = \frac{L_e n_i^2 L_h^2 n D_e}{L_h n_i^2 L_e^2 p D_h} = \frac{L_h n D_e}{L_e p D_h}$$

From the diffusion equation we get $D \propto \mu$ and conductivity, $\sigma_e \propto n\mu_e$ and vice versa for holes.

Thus we get $\frac{J_e}{J_h} = \frac{L_h \sigma_e}{L_e \sigma_h}$ and assuming that $L_e \approx L_h$ we get $\frac{J_e}{J_h} = \frac{\sigma_e}{\sigma_h}$

1 b. [Trivial problem] substituting into the diode equation:

$$I = I_0\left[\exp\left(\frac{qV}{kT}\right)-1\right]$$

given that I=2x10^{-2} A and I_o=1x10^{-24} A, so V= 1.33V

1 c [Easy problem – merely applying resistivity equations to the n and p layers]

$$R_n = \frac{l_n}{nq\mu_e A}, R_p = \frac{l_p}{pq\mu_h A}$$

Substituting in gives R_n=2.89 Ω, R_p=0.00017 Ω, Thus R~ R_n
Applying Ohms law for I=20 mA gives a drop of 0.058 V and adding the voltage drop from (b) gives 1.39 V:

1 d [Hidden]

First as the doping is much heavier on the p-type side we know that the hole current will be much greater than the electron current so we should dope the n-type side in the region near the junction.

The proportion of current will be given by the ratio of the hole current to total current which will, if $J_e << J_h$ equal $1 - \frac{J_e}{J_h}$ (Binomal Theorem).
In part (a) we said that the ratio of conductivities approximated the ratio of electron and hole currents. Thus the ratio of currents $\frac{J_e}{J_h}$ can be calculated to be 0.015. Thus the proportion of current able to interact with the nitrogen doped region will be around 98.5%.

2 a) [Bookwork] – relatively simply, but unusual to use in this course

Figures should be shown to support the following explanation.
A capacitor's capacitance is qiven by C=Q/V. When a dc voltage is applied to a capacitor with free space between the plates then charge is stored on the plates such such that the voltage drop across the capacitor is equal to the voltage applied.
If an insulator is placed between the plates the positively charged nuclei and electrons (or in an ionically bonded material the positive ions and negative ions) can distort in some manner due to the e-field across the material. This in effect sets up a potential across the material opposing the field from the plates.
However the voltage applied across the capacitor is constant. Thus more charges will be supplied to the capacitor plates increase the overall field back to the original value (as E=V/d). As Q increases while the voltage stays the same so the capacitance must also increase.

2 b) [Bookwork]

The dielectric should have a high dielectric constant, be manufacturable, have a high breakdown voltage, have good reliability, be cheap (any three)

2 c) [Bookwork – although requires thought about depletion region)

Picture showing diode with thick n-depletion region and extremely thin p-depletion region. In Junction area. Conducting regions are doped areas that are not depleted and depletion region is insulating. Capacitor is formed with the depletion region being the dielectric. Depletion region is formed due to diffusion of carriers across junction leading to built-in potential which prevents further flow of carriers.

2 d) [Hidden]

Need to recognise that the device will cease to operate as a capacitor if it breaks down, and does not operate as a capacitor in forward bias (too much current flow in both cases). Thus the range of V is from 0 to 100V
Need to recognise the equation

$$d_j = \left(2\varepsilon_0\varepsilon_r V_j / qN_d\right)^{0.5}$$

given in table on exam paper as the equation to use. The value of V_j ranges from 0.7 V(built in voltage) to 100.7 V (~100 V). Thus the limits of d_j are $5.6\text{x}10^{-7}$ m and $6.7\text{x}10^{-6}$ m.

We can now use standard capacitor equation: $C = \frac{\varepsilon A}{d}$ to get max and min capacitance.

Area is 1 mm diameter = $7.9\text{x}10^{-7}$ m^2

Thus the capacitance can vary from a maximum at V=0V of 150 pF to a minimum at V=100V of 12.5 pF.

3 a) [Easy Bookwork]

If the a thermally generated free electron and hole meet they will recombine. The rate at which electrons recombine with a holes will be proportional to the density of holes, p, in the material and vice versa. Thus the overall recombination rate, R will be proportional to the product of the electron and hole densities. We can define a constant of proportionality, B to get $R=Bn_ip_i$.

b) [Bookwork]

For an n-type semiconductor the material is doped with an impurity to create a high density of free electrons, much higher than the intrinsic density. There will still be holes present in the material from thermal generation at a low level, these holes are minority carriers in the material.

In any material the thermal generation rate, and therefore in equilibrium the recombination rate is equal. In an n-doped case the density of electrons will be much higher so we get

$R= R=Bn_ip_i = Bnp_n$.

As $n_i=p_i$ we can rewrite the above to get $p_n=n_i^2/n$.

c) [More difficult bookwork]

Assume a n-type semiconductor. The majority carrier density is high and the minority density many orders of magnitude lower. Light will create e-h pairs which will radically increase the minority carrier density, while making minimal impact on the majority density. The extra holes will be in an environment where there are many electrons to recombine with. The minority carrier lifetime is a measure of how long the hole will survive before recombining.
If the light is absorber near the surface then their will be a hole concentration gradient which will act to allow the holes to diffuse into the material. The diffusion length is a measure of how far they will travel before recombining.

d) [Bookwork]

In a photodiode light is absorbed in or near the p-n junction, creating e-h pairs. The device should either be unbiased or reverse biased. If the minority carriers can diffuse across the junction before recombining they will form a photocurrent.

e) [Hidden – I suspect quite difficult – all the equations used are in the table at the beginning of the examination question]

The key point to this question is to recognise that for a photocurrent to form the minority carrier electrons have to diffuse from the surface where they are photogenerated to the depletion region. This is glossed over in the lectures (I make a brief oral mention of this fact but concentrate on describing a situation where the e-h pairs are photogenerated in the depletion region itself), but the there are hints in the question, especially the assumption and minority carrier lifetime data that should put able students on the right track.

We first need to calculate the electron minority carrier diffusion length in the material. The equations required are: $L_e = \sqrt{D_e \tau_e}$ and $D_e = \frac{kT}{q}\mu_e$.

For Si μ_e is given as 0.07 $m^2V^{-1}s^{-1}$, and we were told that τ_e= 1 μs.
Thus D_e= 1.81x10^{-3} m^2s^{-1}, and hence L_e= 43 μm.

We now need to use the equation for diffusion length: $\delta n(x) = \delta n_0 \exp\left(-\frac{x}{L_e}\right)$, where we want $\frac{\delta n(x)}{\delta n_0}$.

For a thickness, x=1 μm, substituting for x, L_e gives $\frac{\delta n(1\mu m)}{\delta n_0} = 0.977$.

Thus 97.7% of the photogenerated carriers should produce a photocurrent (ie the electrons and holes will reach the contacts of the device. The remainder will recombine in the p-type layer, removing the e-h pair created by the light.

[Note: Q4 is quite similar to Q2 last year – this was the least attempted question and had a low average – parts b,d of the question are different and a is shorter, c is slightly simpler]

4 a) [Bookwork]

Description of MOSFET in p-layer with n^+ regions for source and drain. Silicon Oxide between gate and semiconductor. Should include picture(s) showing structure and describing how a positive gate bias increases the p-depletion region and then pulls carriers in from the n^+ regions to form an n-channel. The threshold voltage is the critical minimum voltage for the channel to form, ie where sufficient bias is applied to the gate for electrons to be pulled from the source, drain n-type regions to form the channel

b) [Bookwork]

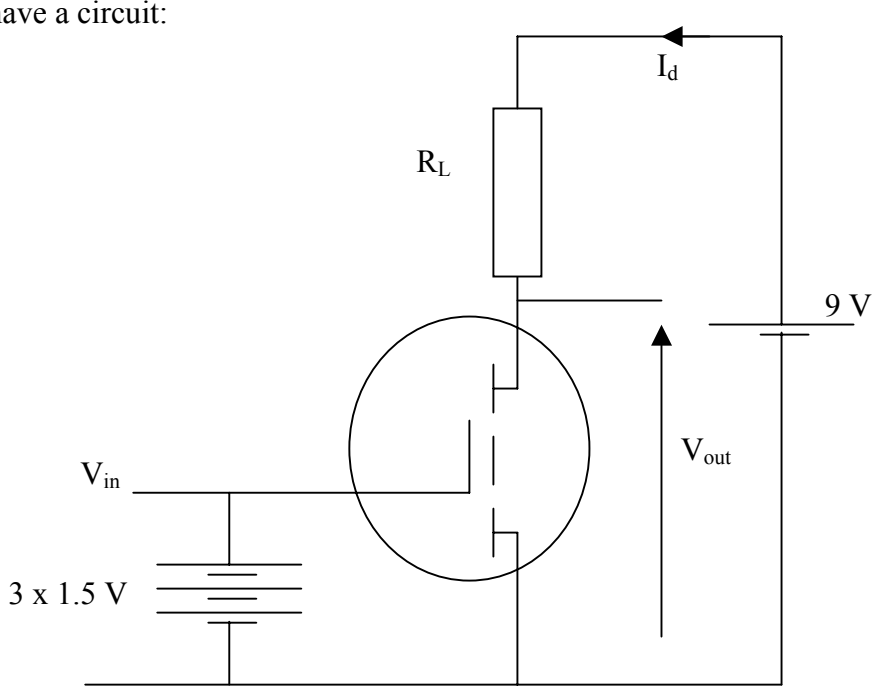
The transconductance is the rate of change of drain current with gate voltage. It is usually measured at some particular value of gate voltage in a device, as it can vary a little (although in theory it does not).

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_g}$$

c) [Hidden – although a similar problem was set for the first time last year]

We need to design a circuit to get a voltage gain of 200, powered by a 9V battery. Let us use three 1.5 V batteries to bias the quiescent point of the gate to 4.5 V, where we know the transconductance.

Thus we have a circuit:



Now for a we need a maximum peak to peak output of V_{gs}= 4 V for a 20 mV input

Using the equation: $i_d = g_m v_{gs}$ we have 2 mS x 20 mV = 40 μA.

Thus we need a load resistor with a voltage drop difference of 4 V for a current difference of 40 μA through it.
Therefore R_L = 100 kΩ

(d) [Hidden/Very obscure bookwork]

Students are not given the equivalent circuit for the MOSFET amplifier, but need to recognise that it is the same as for a JFET, but that the gate – source,drain resistances can be ignored. It should include a current source dept on the transconductance and gate voltage between source and drain with the output resistance between the two terminals also. The output resistance leads to a sloped output characteristic, in the amplifier region. That is the drain current rises slightly with drain voltage, rather than remaining perfectly flat.