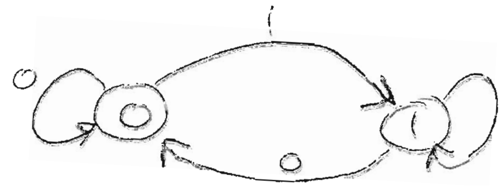
EEE119 12/13

1. a. i)

D	Q'
0	0
1	1

$Q' = D$

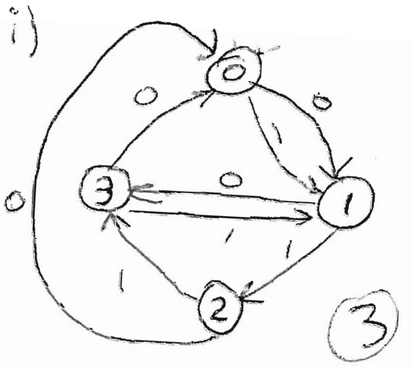


3

ii) Self starting – if counter gets into an unused state, the next state will be part of the valid sequence.

2

b i)



3

	Present state $Q_1 Q_0$	Input X	Next state $Q_1 Q_0$
0	0 0	0	0 1
	0 0	1	0 1
1	0 1	0	1 1
	0 1	1	1 0
2	1 0	0	0 0
	1 0	1	1 1
3	1 1	0	0 0
	1 1	1	0 1

3

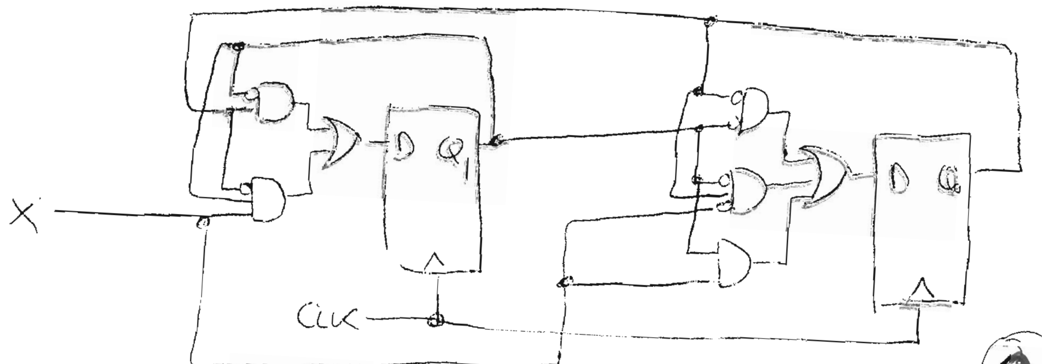
when $x = 0$, state 2 is unused so take it to state 0

when $x = 1$, state 0 is unused so take it to state 1

(ii) $Q_1' = \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 X$, $Q_0' = \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 \bar{X} + Q_1 \bar{Q}_0 X + Q_1 Q_0 X$

$= \bar{Q}_1 \bar{Q}_0 + \bar{Q}_1 Q_0 \bar{X} + Q_1 X$

3



2

other solutions valid

(iii) two gate delay = 7 + 7 = 14 ns

add to flipflop delay 14 + 5 = 19 ns, allow 1 ns setup

19 + 1 = 20 ns, $\frac{1}{20\text{ns}}$ = 50 MHz

2

(iv) Flip-Flops may have entered a metastable condition

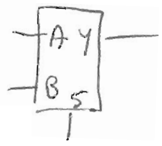
Race conditions in the combinational logic may lead to an incorrect input to the flip flops being clocked in.

2

EEE119 SOLUTIONS 12/13

2. a. (i)

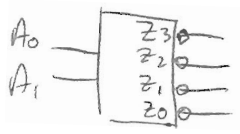
S	Y
0	A
1	B



Switches data from one of the two inputs (A, B) to the output (Y) under the control of select (S)
S=0 pass A, S=1 pass B

3

(ii)

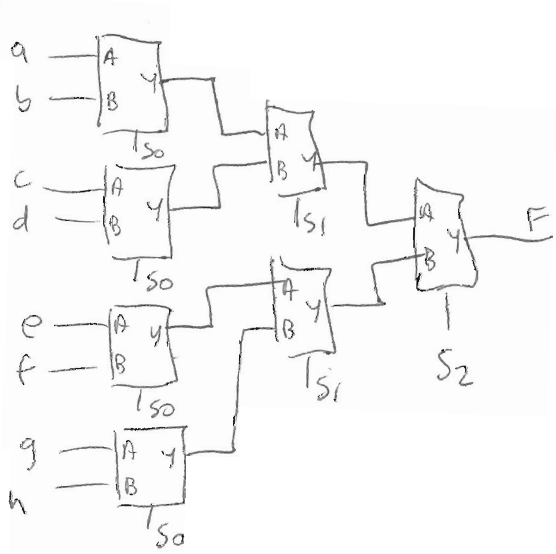


$A_1 A_0$	Z_3	Z_2	Z_1	Z_0
00	1	1	1	0
01	1	1	0	1
10	1	0	1	1
11	0	1	1	1

For each input combination, one output is set low as seen in the truth table. All other outputs are high

3

b.



$S_2 S_1 S_0$	F
000	a
001	b
010	c
011	d
100	e
101	f
110	g
111	h

Each column of 2-to-1 multiplexers has a common select line. Data is selected as shown in the truth table.

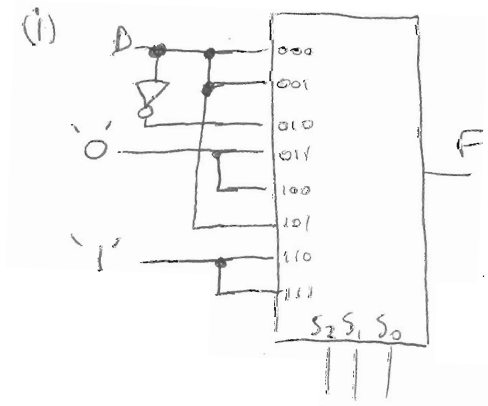
4

c.

	ABCD	F
0	0000	0
1	0001	1
2	0010	0
3	0011	1
4	0100	1
5	0101	0
6	0110	0
7	0111	0
8	1000	0
9	1001	0
10	1010	0
11	1011	1
12	1100	1
13	1101	1
14	1110	1
15	1111	1

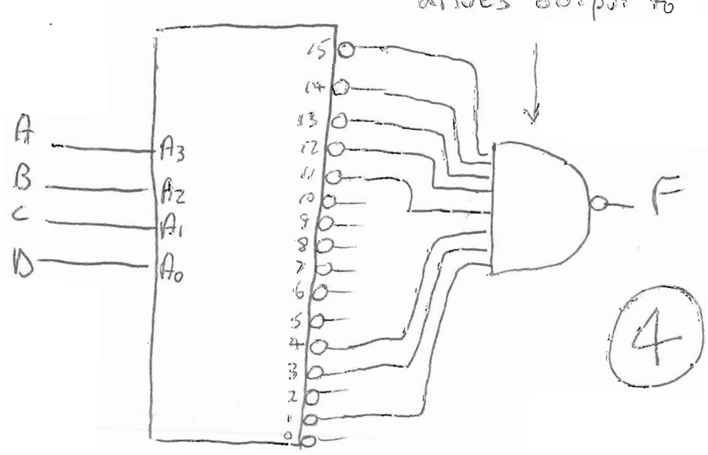
2

(i)



4

8-input NAND. Any '0' drives output to '1'



4

EEE 119 12/13

3 a. (i) $(X+Y)(X+Z) = XX + XZ + YX + YZ = X + XZ + YX + YZ$

$= X(1 + Z + Y) + YZ$

$= X + YZ$

(ii) $ABC + \bar{A}B + AB\bar{C}$

$= AB(C+\bar{C}) + \bar{A}B = AB + \bar{A}B = B(A+\bar{A}) = B$ 4

b. (i) Moore output is formed from the present state

Mealy output is formed from the state and the current input. 2

(ii) Binary coding 2^n states requires n flip flops

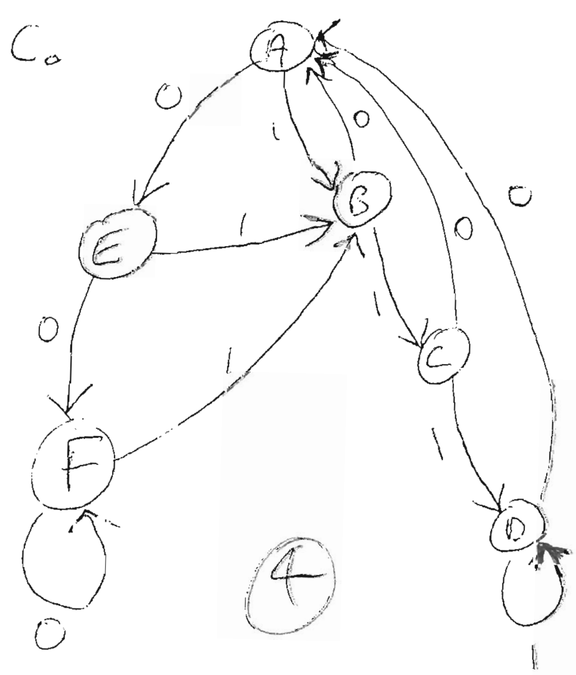
'One Hot' one flip flop per state is required.

The state is indicated by a single flip flop being '1' or 'hot'. 2

(iii) Resetting ⇒ when a sequence is found, look for the next sequence starting again at the next bit. 2

Non Resetting ⇒ bits from a previous sequence can be used in the next valid sequence.

c.



A ⇒ Reset State, single '0'

B ⇒ First '1', C ⇒ Second '1'

D ⇒ three 1's, E ⇒ Second '0'

F ⇒ three 0's 2

Present state	I	Next State	output Z
A	0 1	E B	0
B	0 1	A C	0
C	0 1	A D	0
D	0 1	A D	1
E	0 1	F B	0
F	0 1	F B	1

4

EEE119 12/13

4. a. $\overline{x+y} = \bar{x}\cdot\bar{y}$

$x\ y$	$x+y$	$\overline{x+y}$	$\bar{x}$	$\bar{y}$	$\bar{x}\cdot\bar{y}$
0 0	0	1	1	1	1
0 1	1	0	1	0	0
1 0	1	0	0	1	0
1 1	1	0	0	0	0

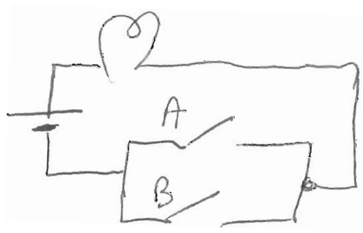
same (3)

$\overline{x\cdot y} = \bar{x} + \bar{y}$

$x\ y$	$x\cdot y$	$\overline{xy}$	$\bar{x}$	$\bar{y}$	$\bar{x}+\bar{y}$
0 0	0	1	1	1	1
0 1	0	1	1	0	1
1 0	0	1	0	1	1
1 1	1	0	0	0	0

same (3)

b.



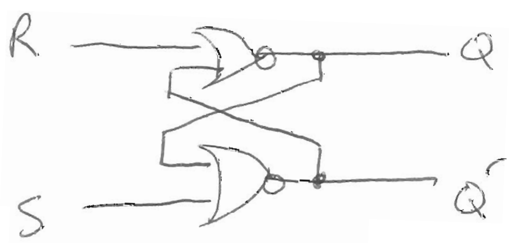
using $\overline{A\cdot B} = \bar{A} + \bar{B}$

switches logic '0' closed

logic '1' open

(4)

c.

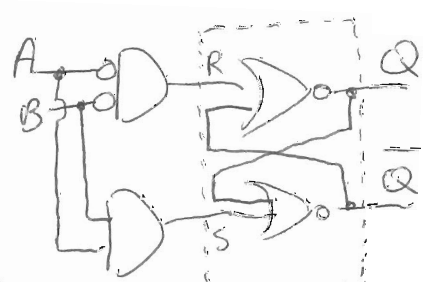


S	R	Q
0	0	unchanged
0	1	0
1	0	1
1	1	not allowed

Active high SR Latch
Remains in stable state for $S=R=0$ (6)
Set with pulse of '1' on S
Reset with pulse of '1' on R
$S=R=1$ unstable race condition

d.

A	B	Q	$\bar{Q}$	R	S
0	0	0	1	1	0
0	1	Q	$\bar{Q}$	0	0
1	0	Q	$\bar{Q}$	0	0
1	1	1	0	0	1



$R = \bar{A}\bar{B}$
$S = AB$

(4)