University of Sheffield

Department of Electronic and Electrical Engineering

EEE207 Semiconductors for Electronics and Devices

Problem Sheet 4

1. A certain germanium p-n junction diode has a conductivity of 10^4S m^{-1} in the bulk n-type region and 10^2S m^{-1} in the p-type region. Find the "built-in" voltage drop across the junction in equilibrium at 300K, assuming electron and hole mobilities of 0.36m^2 V^{-1} s^{-1} and 0.17m^2 V^{-1} s^{-1} respectively and an intrinsic carrier density of 2.5×10^{19}m^{-3}.

2. Assuming the formula $g_m = \mu_e C_g V_{d,s} / l^2$, where the symbols have their usual meaning, calculate the saturation-region transconductance of an induced n-channel MOST having the following properties:

relative permittivity of SiO_2 = 3.7
width of gate = 0.84mm
channel length, l = 5μm
oxide thickness = 150nm
electron mobility, μ_e = 0.02m^2 V^{-1} s^{-1}
drain-source voltage at saturation, $V_{d,s}$ = 10V

3. An induced-channel MOS transistor can be used as a linear resistor in an integrated circuit, where the effective value of resistance between source and drain is controlled by the gate-source voltage, V_g. Assuming the usual formula $I_d = \mu_e C_g (V_g - V_T - \frac{1}{2}V_d)V_d / l^2$, show that, provided the drain voltage is much smaller than the difference between V_g and the turn-on voltage (V_T), a MOS transistor behaves as a linear resistor with resistance given by $R = l^2 / [\mu_e C_g (V_g - V_T)]$, where l is the length of the channel, C_g is the gate capacitance, and μ_e is the mobility of majority carriers in the channel.

A certain MOS transistor is to be used to simulate a 2000Ω resistor, and has a gate capacitance of 1pF, channel length 5μm, turn-on voltage 3V, and the mobility of electrons in the channel is 0.02m^2 V^{-1} s^{-1}. What gate voltage is necessary to achieve the required resistance? Are there any disadvantages in using this arrangement in an integrated circuit?

4. Assuming the usual expression for the drain current of an induced-channel MOS transistor operated in the unsaturated region, $I_d = \mu_e C_g (V_g - V_T - \frac{1}{2}V_d)V_d / l^2$, show that the saturation-region transconductance of a MOS transistor is proportional to the square root of its drain current. A certain n-channel MOS transistor has a transconductance of 2mS at a drain current of 5mA. Estimate the gate capacitance, assuming a channel length of 10μm and an electron mobility of 0.13m^2 V^{-1} s^{-1}.

Numerical Answers

1. 0.358V
2. 7.34×10^{-3}S
3. 3.63V
4. 0.31pF

Charge on electron:	$-1{\cdot}602\times10^{-19}$C
Free electron rest mass:	$m_0 = 9{\cdot}110\times10^{-31}$kg
Speed of light in vacuum:	$c = 2{\cdot}998\times10^{8}$m s^{-1}
Planck's constant:	$h = 6{\cdot}626\times10^{-34}$J s
Boltzmann's constant:	$k = 1{\cdot}381\times10^{-23}$J K^{-1}
Melting point of ice:	0°C = 273·2K
Permittivity of free space:	$\varepsilon_0 = 8{\cdot}854\times10^{-12}$F m^{-1}
Permeability of free space:	$\mu_0 = 4\pi\times10^{-7}$H m^{-1}