Data Provided: Yes

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (3.0 hours)

EEE6205 Power Electronic Converters

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. A Voltage Source Inverter shown in figure 1.1 is modulated by Sinusoidal Pulse Width Modulation SPWM and it supplies a balanced three-phase RL load. The inverter is supplied from a 600V dc source. A peak current value of I_{peak} = 10A is drawn by the load and the load power factor is 0.7. The inverter operates in linear mode. The amplitude and frequency of the fundamental component of the output phase voltage are 240V and 50Hz, respectively. The first sideband harmonics of the output voltage are centred around the 200th harmonic. Switches S1-S6 are assumed to be ideal.

Propose a solution to modulate switches S1-S6.

(4)

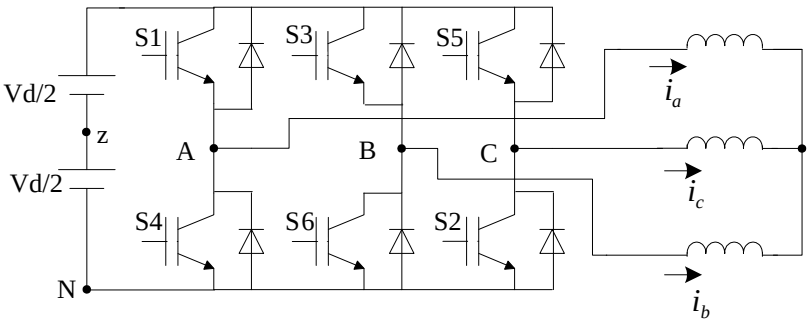


Figure 1.1 Voltage Source Inverter

b. For switches S1-S6 in a) consider their finite turn on time of 0.3μs and turn off time of 0.65μs. Modify the gate-drive signals selected in a) and justify your solution. **(2)**

c. With reference to equivalent circuit diagrams, explain the effect of deadtime on output voltage v_{AN} of the inverter shown in figure 1.1.

(6)

d. For the case in b) calculate the amplitude of the fundamental component of the inverter output phase voltage. The error voltage due to deadtime is given by:

$$v_{error} = v_{Az(real)} - v_{Az(ideal)} \quad (1.1)$$

The fundamental component of the error voltage is given by

$$v_{error,1st} = \frac{4}{\pi} \cdot V_d \cdot \frac{T_d}{T_s} \sin(\omega_o \cdot t - \theta) \quad (1.2)$$

(4)

2. a. One leg of the three-level Flying Capacitor Multilevel Converter is shown in figure 2.1. For the converter shown in figure 2.1 identify available switching states and the corresponding output voltage v_{iN}.

(2)

b. For the case in a) and with reference to suitable circuit diagrams explain which switching states can be affected by the direction of load current i_i.

(6)

c. For the case in a) and with reference to suitable gate drive signals explain how voltage v_{C2i} across capacitor C_{2i} can be kept constant by using Phase-Shifted Carrier Pulse Width Modulation PSCPWM.

(4)

d. For the case in a) and with reference to waveforms of voltage v_{C2i} and current i_{C2i}, calculate the voltage ripple across capacitor C_{2i}. The capacitance of C_{2i} is 1200μF. The dc link voltage is 1kV. The converter is modulated by Phase-Shifted Carrier Pulse Width Modulation PSCPWM and the carrier frequency is 10kHz. For the current switching period, the load current i_i can be considered to be constant and equal to 20A. Within the current switching period, capacitor C_{2i} is charging during a time interval of 30μs.

(4)

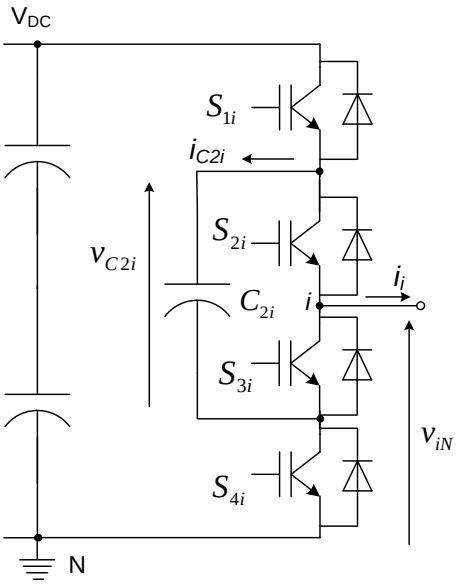


Figure 2.1 One leg of the three-level Flying Capacitor Multilevel Converter

3. a. A resonant dc link inverter can be represented by an equivalent circuit shown in figure 3.1. With reference to figure 3.1 explain the basic operational principles of the resonant dc link inverter.

(4)

b. For the case in a) sketch voltage and current waveforms of v_o, i_L, i_C, i_S and i_D with respect to a gate drive signal for switch S.

(4)

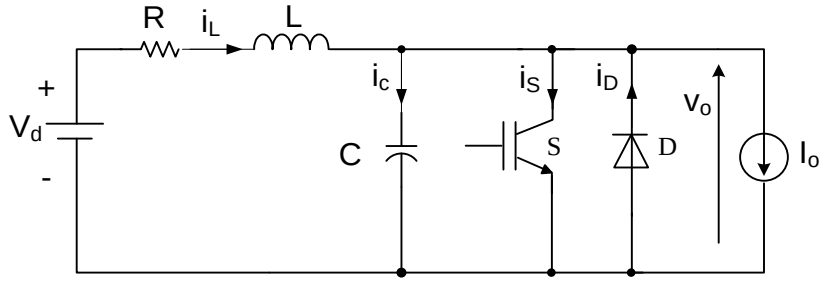


Figure 3.1 Equivalent circuit of resonant dc link inverter

c. A Voltage Source Inverter is shown in figure 3.2. It is controlled by Space Vector Modulation and it operates with a sampling frequency of 5 kHz and a unity power factor. Consider a switching cycle in which the phase angle of the reference output voltage $\vec{V}_{ref}$ is 120° and the amplitude of the reference voltage is at its maximum. With reference to figure 3.2, dwell times for vectors $\vec{V}_1$ and $\vec{V}_2$ are respectively given by (3.1) and (3.2). Represent the reference vector $\vec{V}_{ref}$ in the space vector diagram and calculate the dwell times of the static vectors that are used to synthesis the reference voltage vector $\vec{V}_{ref}$.

$$T_{V_1} = \sqrt{3}\frac{V_{ref}}{V_{dc}} T_s \sin\left(\frac{\pi}{3} - \theta\right) \quad (3.1)$$

$$T_{V_2} = \sqrt{3}\frac{V_{ref}}{V_{dc}} T_s \sin(\theta) \quad (3.2)$$

(4)

d. For the case in c), design a switching sequence to synthesise the reference vector $\vec{V}_{ref}$ and justify your selection.

(4)

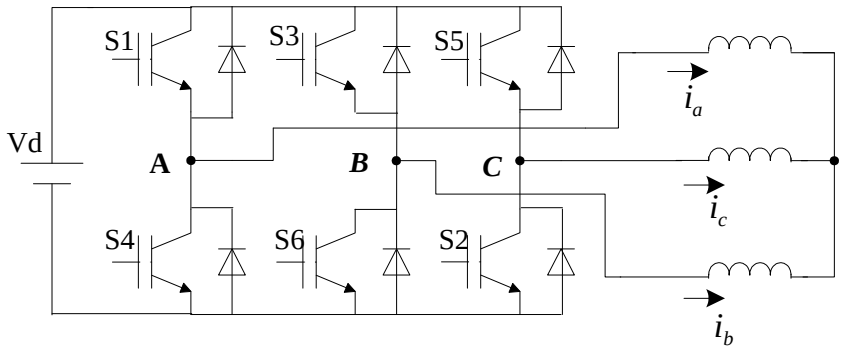


Figure 3.2 Voltage Source Inverter

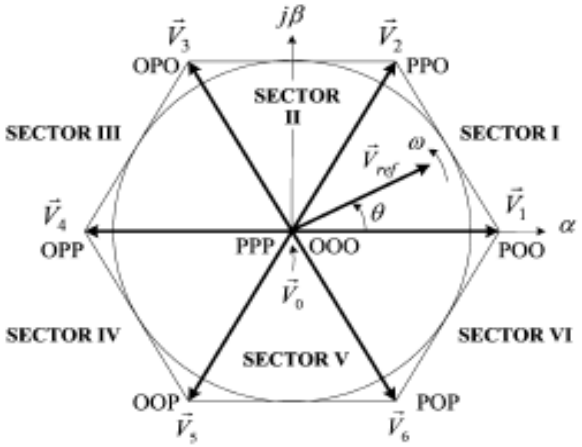


Figure 3.3 Space Vector Diagram

4. a. In the circuit shown in figure 4.1.a), an IGBT is used to switch a diode-clamped inductive load. Figure 4.1.b) shows the equivalent model of the circuit shown in figure 4.1.a) which can be used for transient analysis. The load is represented by a constant current source I_o of 300A and the dc supply voltage is 600V. The free-wheeling diode is considered to be ideal. The complete IGBT circuit module with its own gate drive circuit has the following performance characteristics:
V_{GG+} = 15V, $V_{GG-} = -15V$, $\frac{v_{ds}}{dt} \cong \frac{2500\ \text{V}}{1\ \mu\text{s}}$, $C_{gs} = 17.58$ nF, $C_{gd} = 1.02$ nF, $g_{fs} = 60\ S$, $V_{gs,th} = 6\ V$ (threshold voltage), R_G=2Ω.

a.i. During turn-on, once the IGBT is carrying the full load current but is still in active region, the gate-source voltage becomes temporary clamped. With reference to the gate-source voltage waveform and the transfer curve calculate the gate-source voltage needed to maintain load current I_o through the drain circuit.

(3)

a.ii. For the case in a.i), determine the current in the gate circuit while the gate-source voltage is clamped at the level needed to maintain current I_o through the drain circuit.

(2)

a.iii. With reference to the gate-source voltage and figure 4.1 sketch the voltage and current waveforms of i_d, i_{Df}, v_{ds} and v_{Df} during IGBT turn-on.

(4)

b. The Voltage Source Inverter shown in figure 4.2 works in SIX-STEP mode and supplies an induction motor. The rms value and frequency of the fundamental component of the output line to line voltage are 460V and 50Hz, respectively. The power factor of the load is 0.86.

b.i. With respect to gate drive signals for switches S1-S6, sketch output voltage v_{AB}.

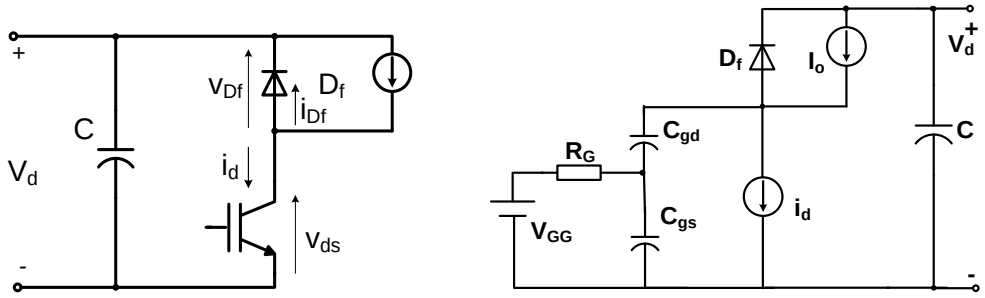
(2)

b.ii. With respect to gate drive signals for switches S1-S6, determine all switching commutations in SIX-STEP mode during one fundamental period of the output voltage.

(2)

b.iii. Select the most appropriate value of the voltage at the dc terminals of the inverter shown in figure 4.2.

(3)



a) Circuit diagram b) Equivalent model

Figure 4.1 Step-down dc to dc converter

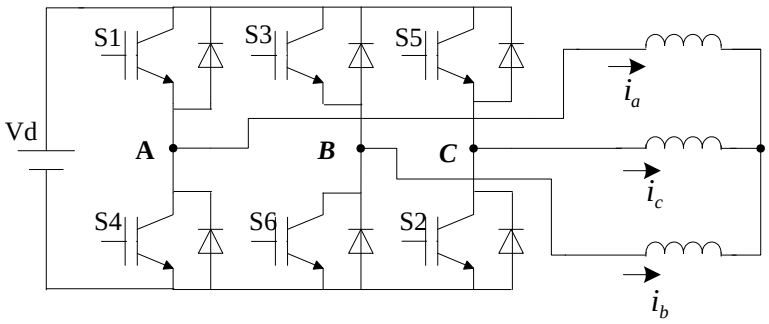


Figure 4.2 Voltage Source Inverter

5. a. The six-pulse phase-controlled rectifier connected to the utility grid is shown in figure 5.1. Switches S1-S6 are realized by Silicon-Controlled Rectifier SCR devices. The rms value of the grid line to line voltage is 2300V ($V_{llrms} = 2300V$). The equivalent inductance L_s is assumed to be zero. The inductance of the dc choke L_d is assumed to be sufficiently high such that the dc current I_d is ripple-free. The dc choke and the load can be replaced by an adjustable dc current source as shown in figure 5.1. The output power is P = 400kW. The losses in the system are neglected. The firing angle of the SCR devices is $\alpha = 30°$.
Sketch the voltage and current waveforms of the rectifier: v_N, v_P, v_d, i_a.

(4)

b. For the case in a), determine the conduction period and switching frequency of switch S4.

(2)

c. For the case in a) show that the output voltage is given by (5.1).

$$V_d = \frac{3}{\pi} \cdot \sqrt{2} \cdot V_{llrms} \cdot cos\alpha \qquad (5.1)$$

(4)

d. **di**. For the case in a), calculate the amplitude of the fundamental component of input current i_a.

(4)

dii. For the case in a), calculate the reactive power in the system.

(2)

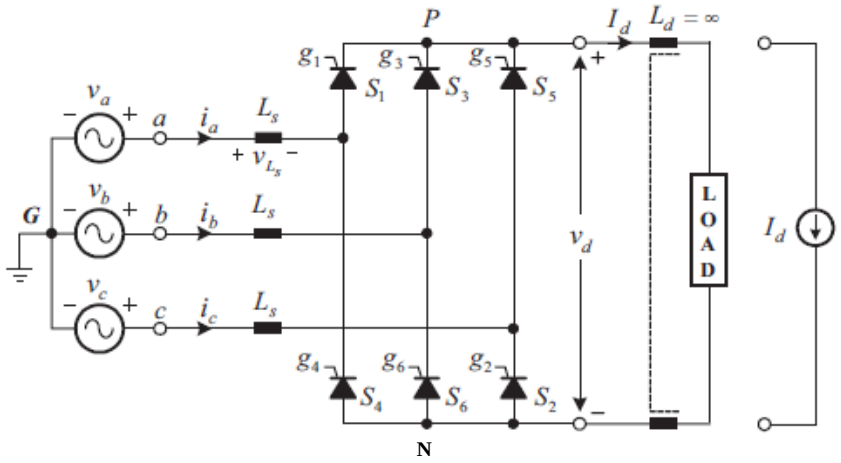


Figure 5.1 Six-pulse phase-controlled rectifier

6. a. The inverter shown in figure 6.1 is modulated by Space Vector Modulation. The reference vector $\vec{V}_{ref}$ of the inverter is in Sector II as shown in figure 6.2. The sampling frequency is 10 kHz. The reference vector is at the position $\theta = 70^{\circ}$. The position of the subsequent reference vector is 73.6°. Calculate the fundamental frequency of the output voltage and explain your solution.

(4)

b. For the case in a) and with respect to suitable circuit diagrams explain the effect of switching states on neutral-point voltage v_{zN}.

(4)

c. For the case in a) and for the switching combination [PON], draw the equivalent circuit diagram and calculate the amplitude and position of the corresponding static space vector based on the general space vector form given by (6.1).

$$\vec{y}(t) = \frac{2}{3} \cdot \left(y_a(t) \cdot e^{j0} + y_b(t) \cdot e^{\frac{j2\pi}{3}} + y_c(t) \cdot e^{\frac{j4\pi}{3}} \right) \qquad (6.1)$$

(4)

d. For the case in a) and with respect to suitable circuit diagrams explain switching states (S1=off, S4=off, S2=on, S3=on) and (S1=on, S4=on, S2=off, S3=off) with respect to voltage v_{AN} and the direction of load current i_A.

(4)

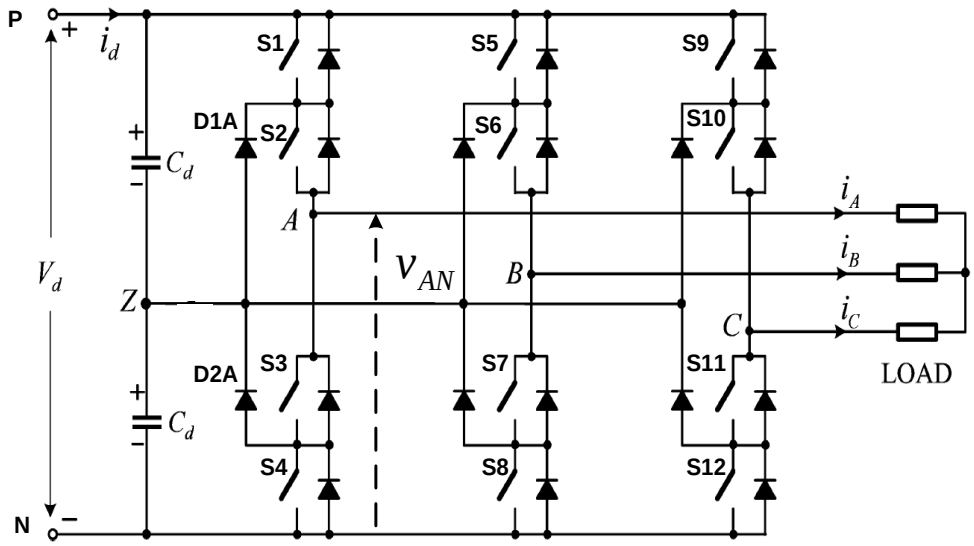


Figure 6.1 Neutral point clamped Voltage Source Inverter

(figure 6.2 overleaf)

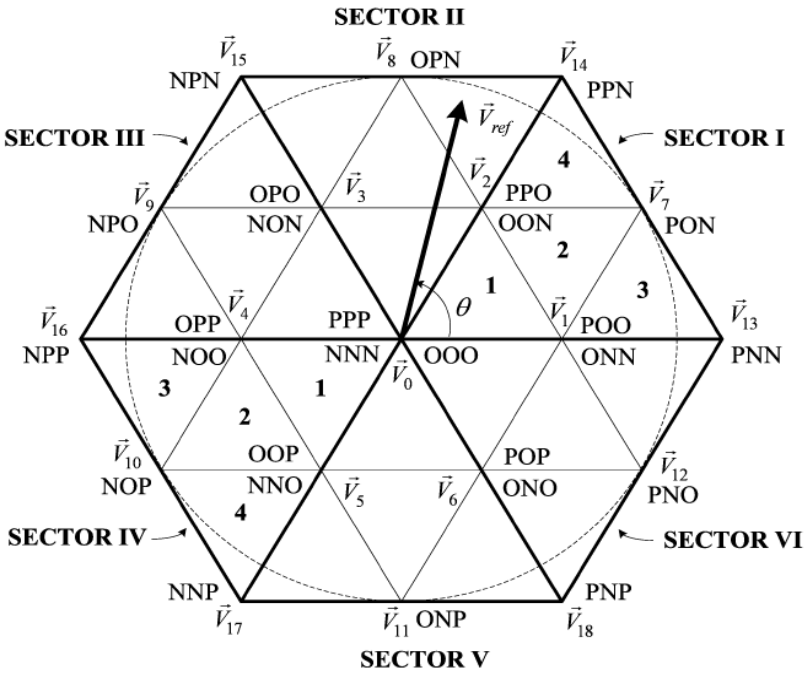


Figure 6.2 Space vector diagram

MO/DG