Exam Feedback: EEE101 January 2010

General Comments: Your attempts at EEE101 were mixed and I think overall I was slightly disappointed. Many of the problems people had were due to lack of practice - particularly in the execution of standard processes like loop analysis and handling the complex number algebra associated with the j notation approach to ac circuits. Quite a few marks were lost because of silly numerical errors that could easily have been checked and quite a few more marks were lost because the answers given were not in line with the questions asked. It is really important that you read the questions properly and make sure you do everything it asks of you. Some of you are very organised; it is easy to follow your working and, where your answer is wrong, identify your error and give you appropriate credit for what you have done. Some of you, on the other hand, presented very messy work that was hard (in some cases impossible) to interpret and in a few cases you confused even yourselves by failing to take an ordered approach to your questions. If you are doing an analysis, you need to draw a circuit diagram – how else can I credit correct formulation of equations describing the circuit? You need to explain briefly (three or four words is usually enough) what you are doing so that I can follow your thinking – if I just see a set of numbers or equations you leave me in a position of having to guess whether or not you are intentionally doing the right thing - not wise if you want marks from me. Try to do quick checks on your answers - in dc circuits these take about 15 seconds and can easily identify errors and answers that don't make physical sense (eg, voltage across a resistor bigger than the voltage of the driving source).

Q1: Question 1 was answered pretty well by the majority of people. Most people could work out the effective resistance in part (i) and hence work out I_S. Some had trouble with (ii), the most common problem here was to put down the voltage across R_1 instead of V_A which was, of course, V_S - V_{R1}. Part (iii) was answered correctly by most and part (iv) produced a variety of interesting approaches, the majority of which were correct. The introduction of the current source in part (v) caused some difficulties for the majority of you although about 25% of you got it right. Most of the problems surrounding part (v) arose because of poor discipline in the execution of a superposition approach. In particular, those who went wrong did not define currents in the same direction for both parts of the superposition exercise and so came to grief in the summing of contributions. Some tried using loop analysis and those who went wrong with this approach went wrong in a loop containing the current source - remember that it is necessary to define the voltage across the current source if you use loops. The easiest approach was a nodal analysis - only Node A was needed.

Q2. The response to this question was disappointing. Part (a) was supposed to be an easy start - I went through this problem as an example in class. There seemed to be great confusion about V_{Th} and R_{Th}. V_{Th} is the voltage difference between nodes **A** and **B** with no external resistance connected between them - ie, a potentially divided version of V_S. R_{Th} is the resistance seen looking into the terminals **A,B** with V_S replaced by its internal resistance - zero Ω. Part (b)(i) was answered generally well but part (b)(ii) caused some problems that were almost all associated with lack of discipline in defining current directions. All that was needed on the transformed circuit was a current sum at the node at the top end of V_A . . . but this relatively straightforward task bamboozled many of you. The last part was a classical transient analysis that was very similar to work done in class.

Q3: This was probably the most disappointing question from my point of view. In part (a)(i) many of you drew a current phasor diagram with I_L and I_R in different directions. This is a series circuit so the same current travels through each component, current should be chosen as the reference direction and a phasor sum of component voltages should be drawn. Well over half of you didn't bother to evaluate the phase of I_S with respect to V_S and of those who did, most gave me the phase of V_S with respect to I_S (same number, opposite sign) which was not what was asked for. In part (ii) many managed the right answer. Those that went astray mostly either lost a mark for incorrectly working out $\omega = 2\pi f$ - in most cases forgetting the π was the problem or they forgot that the modulus of a complex number is the ***square root*** of the sum of real squared + imaginary squared. One or two people did long and complicated calculations that I couldn't make head or tail of. In part (b)(i) the commonest error was a failure to recognise that $V_Z = V_{S1} - V_{S2}$; many of you drew a phasor diagram summing rather than subtracting the two. Part (b)(ii) was generally done well but part (b)(iii) was mixed. Most of the errors were again associated with the VS2 - VS1 bit; some tried direct subtraction of the polar forms (wrong, of course), some added the two voltages, some got them the wrong way round. Most knew what to do with the impedance.

Q4: Attempts at question 4 were reasonable. Most people identified correctly that the circuit impedance was resistive at resonance and then went on successfully to derive the resonant condition for the series circuit of figure 4a. Many of the answers to part (a)(iii) revealed a lack of understanding of modulus - some answers had "*j*"s and some had "-" signs associated with them. Modulus is always a positive real number. About two thirds of you managed part (a)(iv). In part (b)(i) most people managed to derive the required relationship. In part (b)(ii) most knew what to do and of those who went wrong most made errors in getting all *j* terms in the numerator. Some ended up with a frequency given by the square root of a negative number but didn't seem to suspect that their answer might not be sensible.