Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (3.0 hours)

EEE225 Analogue and Digital Electronics 2

Answer a total of **FOUR** questions including at least **ONE** question from each of sections **A**, **B** and **C**. **No marks will be awarded for solutions to a fifth or sixth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

SECTION A

1. a. With reference to the output stage of a digital logic gate, explain briefly, with the aid of a diagram, what you understand by the terms:

i) Open-Drain
ii) Wired-AND
iii) Three-State output **(8)**

b. The following Verilog code describes a certain logic gate at the switch-level.

```
module mygate(Y,A,B,C);
input A,B,C;
output Y;
supply1 POWER;
supply0 GROUND;
wire W1,W2;
pmos t1 (Y, POWER,A);
pmos t2 (Y, POWER,B);
pmos t3 (Y, POWER,C);
nmos t4 (Y, W1, A);
nmos t5 (W1, W2, B);
nmos t6 (W2, GROUND, C);
endmodule
```

Draw a transistor-level circuit diagram for this logic gate. Produce a table indicating the state of each of the transistors for all possible combinations of the inputs **A**, **B**, **C**. Hence, deduce the logic function of the gate. **(8)**

c. In a **74** series logic gate such as **74S00**, what does the designation **S** refer to? Explain how this affects the performance of the gate and the reason for this. **(4)**

2. a. Briefly describe the main differences between a microprocessor and a microcontroller from both a hardware and software point of view. **(6)**

b. A counter is required that will count the number of 1's in an input data word. The data word is supplied from the external environment. On completion, the result of the count will be returned. Draw an Algorithmic State Machine (ASM) chart for this 1's counter. You may assume that a 'Moore' type solution is required. Clearly define the states and variables that you use. **(8)**

c. A certain Field Programmable Gate Array (FPGA) is fed with a 90 MHz clock signal from an external source. The digital system implemented on the device requires a 30 MHz clock.

i) With the aid of a timing diagram explain how this can be achieved.

ii) Are there any precautions that should be taken with the clock signal that you generate and if so why? **(6)**

SECTION B

3. a. **i)** For the current mirror circuit of figure 3, which can be assumed to contain two identical transistors, show that

$$I_M = \frac{I_I h_{FE}}{2 + h_{FE}}$$

where h_{FE} is the dc current gain, I_C/I_B of the transistors. State any assumptions made in arriving at your result. 5

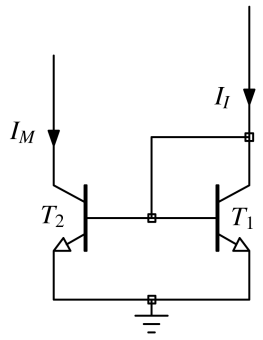

Figure 3

ii) Draw a circuit diagram to show how the circuit of figure 3 could be used as an active load for a differential (or long-tailed) pair. **3**

iii) State two advantages to be gained by using a current mirror as an active load for a differential pair. **2**

b. An operational amplifier with a gain-bandwidth product of 16 MHz is used to make a standard non-inverting amplifier circuit with a gain of 64.

i) What -3dB bandwidth should be expected from the amplifier? **1**

ii) Calculate the gain magnitude and phase at a signal frequency of 400 kHz. **4**

The gain of 64 is to be achieved by putting in series two identical non-inverting amplifier circuits each using the same 16 MHz gain bandwidth product amplifier type as in parts **i)** and **ii)**.

iii) What gain is needed for each amplifier circuit in the series combination? **1**

iv) What is the -3dB frequency of the series combination? **4**

4. a. **i)** Write down the high and low frequency gains of the circuit of figure 4. **2**

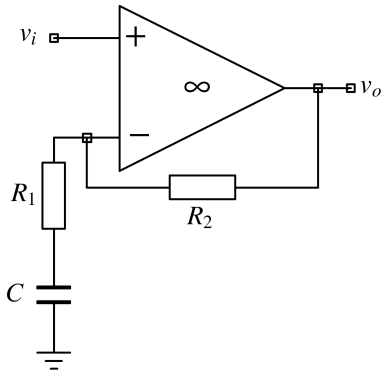

Figure 4

ii) Show that the transfer function of the circuit of figure 4 is **3**

$$\frac{v_o}{v_i} = \frac{1 + j\dfrac{\omega}{\omega_1}}{1 + j\dfrac{\omega}{\omega_0}}$$

where $\omega_1 = \dfrac{1}{C(R_1 + R_2)}$ and

$\omega_0 = \dfrac{1}{CR_1}$.

iii) Assuming that R_1 = 1 kΩ, choose values of R_2 and C that will give a high frequency gain of 21 and a lower frequency -3dB point for that gain of 16 Hz. **3**

iv) Sketch the shape of the gain magnitude (in dB) as a function of log frequency for your design. Label all the key features of your sketch. **3**

b. A particular amplifier with a gain of 200 V/V and a noise bandwidth of 15 kHz has equivalent input noise voltage and current generators of 10 nV $Hz^{-1/2}$ and 1.3 pA $Hz^{-1/2}$. The signal source has a noisy 4.7 kΩ internal resistance. Find

i) The noise factor of the amplifier. **4**

ii) The signal to noise ratio at the amplifier output if the rms input signal level is 20 μV. **5**

The noise associated with a resistor R is $4kTR$ V^2 Hz^{-1} where k = 1.38 x 10^{-23} J K^{-1} and T = 300 K.

SECTION C

You may need to use the following physical constants:

Charge on electron: -1.602×10^{-19} C

Free electron rest mass: $m_0 = 9.110\times10^{-31}$ kg

Speed of light in vacuum $c = 2.998\times10^{8}$ m s^{-1}

Planck's constant: $h = 6.626\times10^{-34}$ J s

Boltzmann's constant: $k = 1.381\times10^{-23}$ J K^{-1}

Melting point of ice: 0^{o}C = 273.2 K

Permittivity of free space: $\varepsilon_0 = 8.854\times10^{-12}$ F m^{-1}

Permeability of free space: $\mu_0 = 4\pi\times10^{-7}$ H m^{-1}

5. **a.** Starting from the charge neutrality condition and assuming that the acceptor and donor doping densities in a semiconductor are known, derive expressions for the majority and minority carrier densities for the following cases:

(i) an n-type extrinsic doped structure, and

(ii) a compensated near-intrinsic doped structure

State clearly all assumptions made. **4**

b. An intrinsic layer of silicon is initially uniformly doped with donors such that the intrinsic resistivity changes by a factor of 10,000. You wish to make a photodiode from this material so need to further dope the top part of this semiconductor layer with acceptors. What is the minimum level of acceptor doping needed to make a p-type layer in the silicon and thus make the photodiode?

The resistivity of intrinsic silicon at room temperature is 5×10^{3} Ω-m, and μ_e = 0.12 m^2 V^{-1} s^{-1}, μ_h = 0.05 m^2 V^{-1} s^{-1} and E_g = 1.1 eV. (Note: all the symbols have their usual meaning.)

Explain qualitatively whether or not this acceptor doping level would have to change if the photodiode was to operate at below room temperature. **8**

c. Draw a band diagram of the photodiode of part **b.** for the conditions of total darkness and no external bias. Identify clearly on your diagram the conduction band, the valence band and the Fermi-level. **4**

d. By drawing the current-voltage characteristics of the photodiode in the dark and under illumination, explain how we may use this photodiode to detect light. **4**

6. **a.** Draw the cross-sectional diagram of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST). Label your drawing to identify all the significant parts of the device and make clear the polarities of the applied voltages necessary for channel conduction. **4**

b. The unsaturated drain characteristic of a MOST is given by:

$$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds}$$

where the symbols have their usual meaning.

Derive the condition in terms of V_{gs}, V_{ds} and V_T for when saturation of the drain current occurs. **5**

c. If the source terminal of a MOST operating in the saturation region is grounded and the drain terminal is connected directly to the gate terminal, find the relationship between I_d and V_{ds}. Comment on the range of values of V_{ds} over which this relationship would be true. **7**

d. A particular MOST connected as in part **c.** of this question has $\mu e C_g/l^2 = 8\times10^{-4}$ A V^{-2}. No I_d is observed to flow until V_{ds} reaches 3V. What is the value of I_d when V_{ds} = 5 V? Describe a possible use for such a device. **4**

NJP / RCT / JPRD