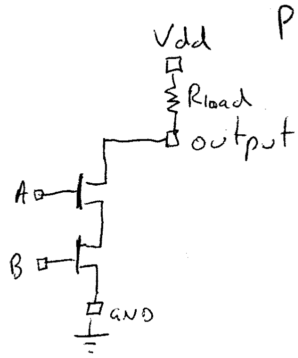
EEE225 – SECTION A – Solutions

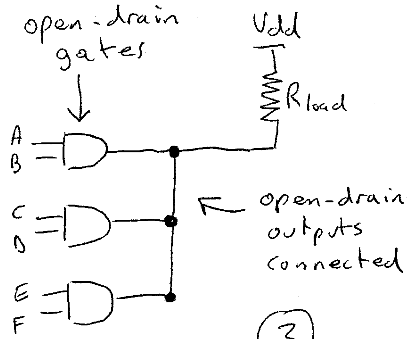
P 1

1 a (i) Open-drain refers to an output structure where the P-channel pull-up transistor is omitted and the drain terminal of the output transistor is left unconnected. It must be connected to Vdd by a load such as a resistor



3

(ii) The outputs of several open-drain gates can be tied together with a single resistor to pull-up to Vdd. This results in a wired-logic function, in this case an AND configuration



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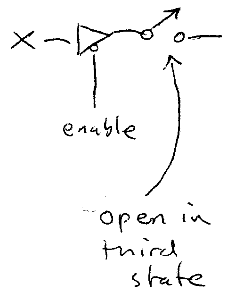
(iii) In addition to output levels of HIGH and LOW, a three state output has a third high-impedance state chosen by an enable input. When in this third state, the output is effectively disconnected.

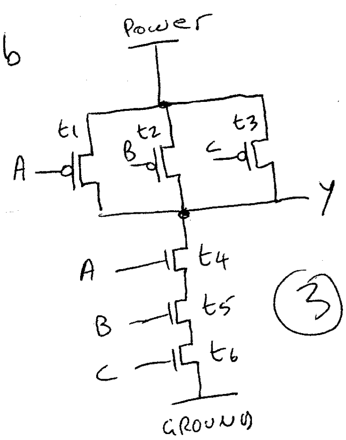


2

NJP

EEE 225 - SECTION A - solutions P2

1b



3

ABC	t_1	t_2	t_3	t_4	t_5	t_6	Y
000	ON	ON	ON	OFF	OFF	OFF	1
001	ON	ON	OFF	OFF	OFF	ON	1
010	ON	OFF	ON	OFF	ON	OFF	1
011	ON	OFF	OFF	OFF	ON	ON	1
100	OFF	ON	ON	ON	OFF	OFF	1
101	OFF	ON	OFF	ON	OFF	ON	1
110	OFF	OFF	ON	ON	ON	OFF	1
111	OFF	OFF	OFF	ON	ON	ON	0

3

THREE INPUT NAND FUNCTION

2

1c The S indicates that Schottky diodes have been used. This gives faster switching times by preventing the transistors from going into saturation. This decreases the time for a transistor to turn on or off.

4

NJP

EEE225 Solutions – Section A

P3

2. a. Microprocessor – generally just the CPU for a PC or laptop. RAM/ROM supplied externally. A microcontroller has RAM/ROM, timers and other peripheral functions built in.

A microprocessor is used in general purpose applications to execute user programs.

A microcontroller is used for a specific purpose and hence needs smaller RAM/ROM resources.

A microcontroller has pins dedicated to serial I/O, analog I/O, waveform generation to allow a minimal solution. A microprocessor would require extra chips for this functionality

(6)

b. DATA → stores the incoming data

COUNT → stores the number of 1's counted.

Start → signal to load the input into DATA

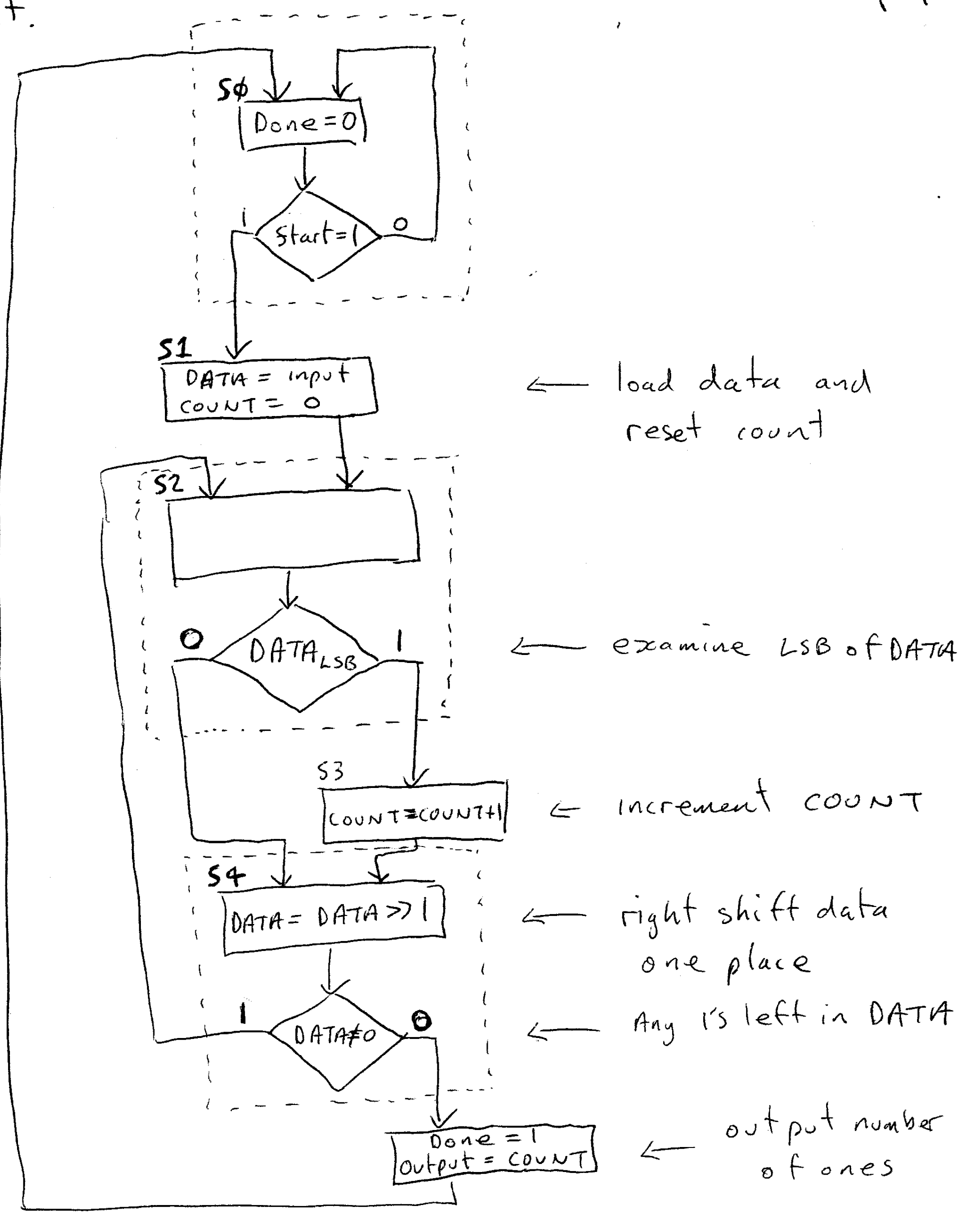
Done → signal to indicate no more 1's to count and output the result

(2)

NJP

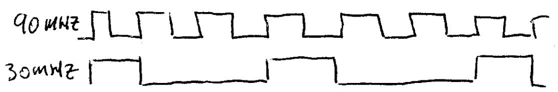
2b. cont.

P4



6

2c (i) A modulo-3 counter could be used to divide the frequency.



2

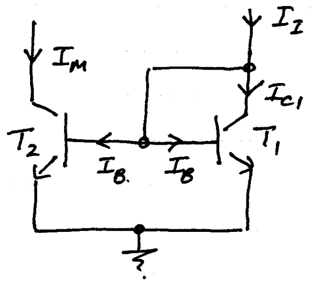
(ii) You must ensure that the divided down clock is connected to the FPGA's dedicated clock distribution network. If it is not, it will use routing resources that may result in large clock skew and hence incorrect operation.

4

NJF

Solution guide to Q3 + Q4

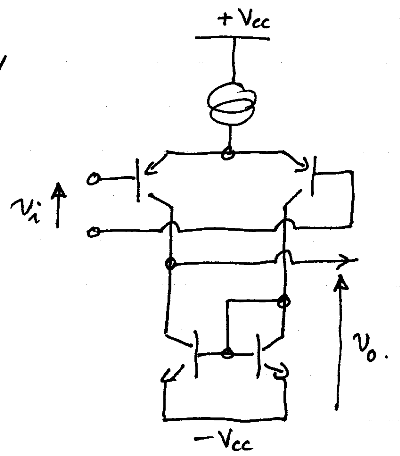
Q3 (a) (i) The first things to do here are
- label the currents in the circuit
- recognise that $I_M = I_{C2} = I_{C1}$ (because the transistors are identical).



Then sum currents at the collector node of T_1 to give: $I_I = I_{C1} + 2I_B$.

I_B can be expressed in terms of I_{C1} (or I_M) using h_{FE} so the problem is then solved by algebraic rearrangement.

(ii) This circuit could equally well be drawn with an n-p-n differential pair and p-n-p current mirror at $+V_{cc}$.



(iii) – Helps to improve the current balance between the two halves of the differential pair

– Makes use of the modulated collector current of the right hand differential pair transistor.

– Increases stage gain because of high impedance at the output node.

– Transistors are space efficient in ICs.

Solution guide to Q3 & Q4

Q3 (b) (i) $BW(Hz) = \frac{GBP(Hz)}{gain}$ [ANS = 250 kHz]

(ii) System is a first order system described by $\frac{v_o}{v_i} = \frac{K}{1 + j\,f/f_o}$

where K = dc gain = 64
f_o = −3dB f = corner f
= 250 kHz.
f = 400 kHz, the frequency of interest.

So problem boils down to finding magnitude and phase of

$$\frac{64}{1 + j\frac{400}{250}}.$$

[ANS = 33.9 and −58°]

(iii) For elements in series, gains multiply
[ANS = 8]

(iv) The −3dB frequency of the cascade is the −1.5dB frequency of each amplifier.

$$\frac{8}{1 + j\,f/2\times10^6} = 8 \times \frac{1}{1 + j\,f/2\times10^6}.$$

[note that −3dB f of each amplifier in cascade is now different because gain is different from b(i).]

Need to find the f at which

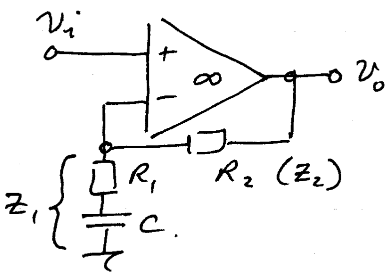
$$\left|\frac{1}{1 + j\,f/2\times10^6}\right| = 10^{-1.5/20}$$

Solution guide to Q3 + Q4

or $\left|\dfrac{1}{1+j\,f/2\times10^6}\right|^2 = \dfrac{1}{1+\left(\frac{f}{2\times10^6}\right)^2} = 10^{-3/20}$.

[ANS = 1.29 MHz].

Q4 (a) (i)



h.f gain, $X_c \to 0$

$\dfrac{v_o}{v_i} = \dfrac{R_2+R_1}{R_1}$

l.f. gain, $X_c \to \infty$

$\dfrac{v_o}{v_i} = 1$

(ii) $\dfrac{v_o}{v_i} = \dfrac{Z_2+Z_1}{Z_1} = \dfrac{R_2+R_1+1/j\omega C}{R_1+1/j\omega C}$.

$= \dfrac{1+j\omega C(R_1+R_2)}{1+j\omega CR_1}$

Then put $\omega_1 = \dfrac{1}{C(R_1+R_2)}$, $\omega_0 = \dfrac{1}{CR_1}$.

etc.

(iii) $R_1 = 1k\Omega$.

It is ω_0 that gives rise to the lower 3dB frequency ...

so C given by $16 = \dfrac{1}{2.\pi.C.1k\Omega}$

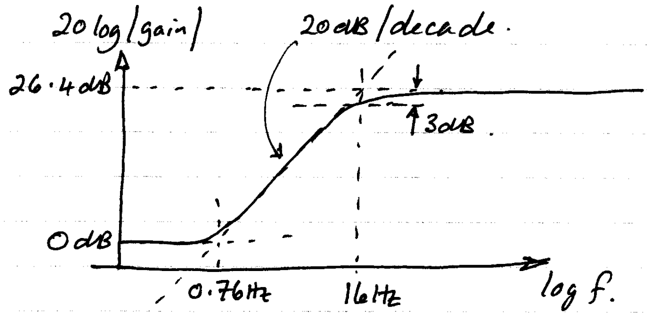
[ANS = 9.95 μF]

hf gain $= 21 = \dfrac{R_1+R_2}{R_1}$

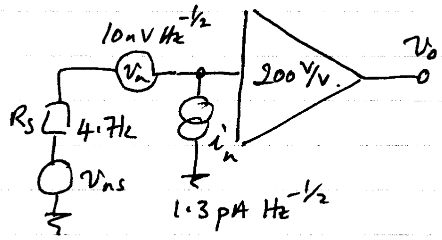
[ANS = 20kΩ].

Solution guide to Q3 + Q4.

(iv)



Q4 (b) (i)



$F = \dfrac{\text{noise output from real amp.}}{\text{noise output from ideal amp.}}$

F is a power ratio so mean squared values must be used.

$$F = \frac{200^2\left[\overline{v_n^2} + \overline{i_n^2}R_s^2 + 4kTR_s\right]}{200^2 \times 4kTR_s}$$

[ANS = 2.77]

(ii) S/N is a power ratio.

mean squared output signal, $\overline{v_{os}^2}$, given by

$$\overline{v_{os}^2} = 200^2(20\mu V)^2$$

mean squared total output noise, $\overline{v_{onT}^2}$, given by

$$\overline{v_{onT}^2} = 200^2\left[\overline{v_n^2} + \overline{i_n^2}R_s^2 + 4kTR_s\right] \times BW.$$

$$S/N = \frac{\overline{v_{os}^2}}{\overline{v_{onT}^2}} =$$ [ANS = 124 = 20.9 dB]

(1)

Q5 EEE 225 2013 Semiconductor Devices

(a) Charge neutrality gives : $n + N_a = p + N_d$

also $np = n_i^2$

so $n + N_a = \frac{n_i^2}{n} + N_d$

$$n^2 + n(N_a - N_d) - n_i^2 = 0$$

so, $n = \left(\frac{N_d - N_a}{2}\right) \pm \frac{\sqrt{(N_d - N_a)^2 + 4n_i^2}}{2}$

$$= \left(\frac{N_d - N_a}{2}\right)\left(1 \pm \sqrt{1 + \left(\frac{2n_i}{N_d - N_a}\right)^2}\right) \quad (2)$$

(i) When doped n-type,

$n \approx N_d \gg n_i$ (1)

$p = \frac{n_i^2}{n}$

(ii) when near intrinsic due to compensation,

$n_i > (N_d - N_a)$, so (1)

$n = n_i = p$

(b) Resistivity of intrinsic Si = $5 \times 10^3\ \Omega m$

$\sigma = \frac{1}{5 \times 10^3} = 1.6 \times 10^{-19}(0.12 + 0.05)n_i$

From this, $n_i = 7.3 \times 10^{15}\ m^{-3}$ (1)

Doping increases conductivity 10^4 times

$\sigma = \frac{10^4}{5 \times 10^3} = 1.6 \times 10^{-19} \times 0.12 \times n$ (ignore holes)

From this $n = 10^{20}\ m^{-3} = N_d$ (2)

(2)

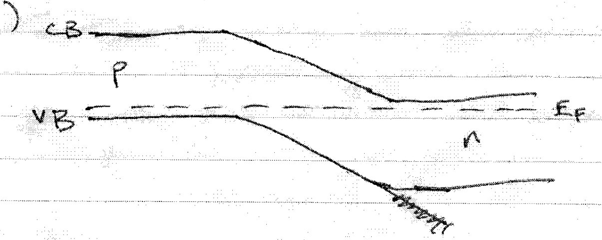
1(b) To make the top part p-type, we need to ensure that $|N_a - N_d| \gg n_i$

so minimum doping required is

$N_a \geq 10^{20} + 7.3 \times 10^{15}\ m^{-3}$ (4)

If the photodiode operated below RT, n_i would decrease, so the Na determined for RT operation would not have to change. (2)

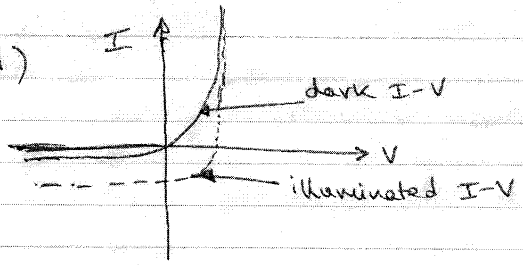
(c)



unbiased and in the dark

(3)

(d)



The device can be operated unbiased. The presence of light would cause a photo-voltaic effect and we would get a voltage that depends on the light intensity

Alternatively, we can reverse bias the device. In the dark, only the minority leakage current would flow. When illuminated, we would see a large photo-current flowing.

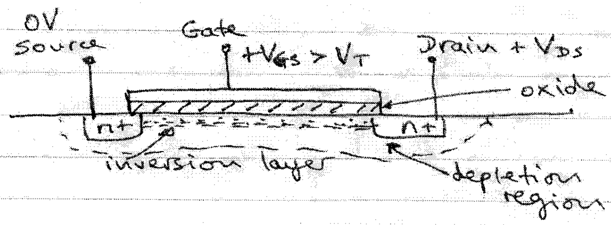
(either one of these explanations will do)

(4)

(3)

Q6

(a)



(4)

(b) In the unsaturated region we have ;

$$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right] V_{ds}$$

Saturation occurs when I_d is a maximum – this occurs when $\partial I_d / \partial V_{ds} = 0$

$$\therefore \frac{\partial I_d}{\partial V_{ds}} = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - V_{ds}\right] = 0$$

(4)

$$\Rightarrow \quad V_{gs} - V_T - V_{ds} = 0$$

so saturation occurs when $V_{gs} - V_T - V_{ds} < 0$

i.e. when $V_{gs} - V_T = V_{ds}$ (1)

(c) When drain and gate are shorted, $V_{gs} = V_{ds}$

At saturation, $I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{gs} - V_T}{2}\right].(V_{gs} - V_T)$

$$= \frac{\mu_e C_g}{2l^2}(V_{gs} - V_T)^2 = \frac{\mu_e C_g}{2l^2}(V_{ds} - V_T)^2$$

This is true for saturated current provided $V_{ds} > V_T$.

(7)

(4)

Q6 cont

(d) For current to flow $V_{ds} \geq 3V \Rightarrow V_T = 3V$

$$I_d = \frac{\mu_e C_g}{2l^2}(V_{ds}-3)^2 = \frac{8\times10^{-4}}{2}(5-3)^2 = 1.6\,mA$$

I_d depends exponentially on V_{ds} ($> 3V$) so can act as a non-linear resistor.

(4)