The University Of Sheffield.

Data Provided:

Boltzmann constant $k_B = 1.38 \times 10^{-23}$ J K^{-1}

Electron charge $e = 1.6 \times 10^{-19}$ C

Thermal conductivity data:

$k_{silicon}$ = 120 W m^{-1} K^{-1} k_{copper} = 390 W m^{-1} K^{-1}

$k_{alumina}$ = 25 W m^{-1} K^{-1} k_{solder} = 60 W m^{-1} K^{-1}

$k_{diamond}$ = 2000 W m^{-1} K^{-1} $k_{aluminium}$ = 200 W m^{-1} K^{-1} k_{gold} = 300 W m^{-1} K^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (2.0 hours)

EEE6393 Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** *Draw a graph of the average failure rate versus time for an electronic component. Explain the reasons for the shape of the curve by identifying and describing its main regions.* **(3)**

b. *Describe the process of 'burn-in' and what advantages this might have for an integrated circuit (IC) manufacturer.* **(4)**

c. *A power IC fabrication process produces 360 dies per wafer. The process gives 250 random defects per wafer that obeys a Poisson distribution. Assuming that a single defect would destroy a die, calculate the function yield of the process*. The Poisson distribution can be described thus: $P(x) = (e^{-\lambda}\lambda^{x})/x!$ **(3)**

d. *Each power IC in **1.c.** consists of a number of separate modules. Suppose that the IC can be redesigned to include a number of spare extra modules that can be configured after fabrication to replace any modules found to be faulty. Assuming one extra module is needed to replace exactly one defective module, how many extra modules are required by each IC to insure a yield greater than 95 %?* **(5)**

e. *A power diode product for an automotive application needs to achieve a 15 year lifetime at an operating temperature of 90 °C. From prior experience it is known that the primary failure mechanism is a thermally activated process with an activation energy of 0.75 eV. A total of 1000 hours are available to perform an accelerated lifetime test on the product. What is the minimum temperature at which the test should be performed?*

(5)

(a)

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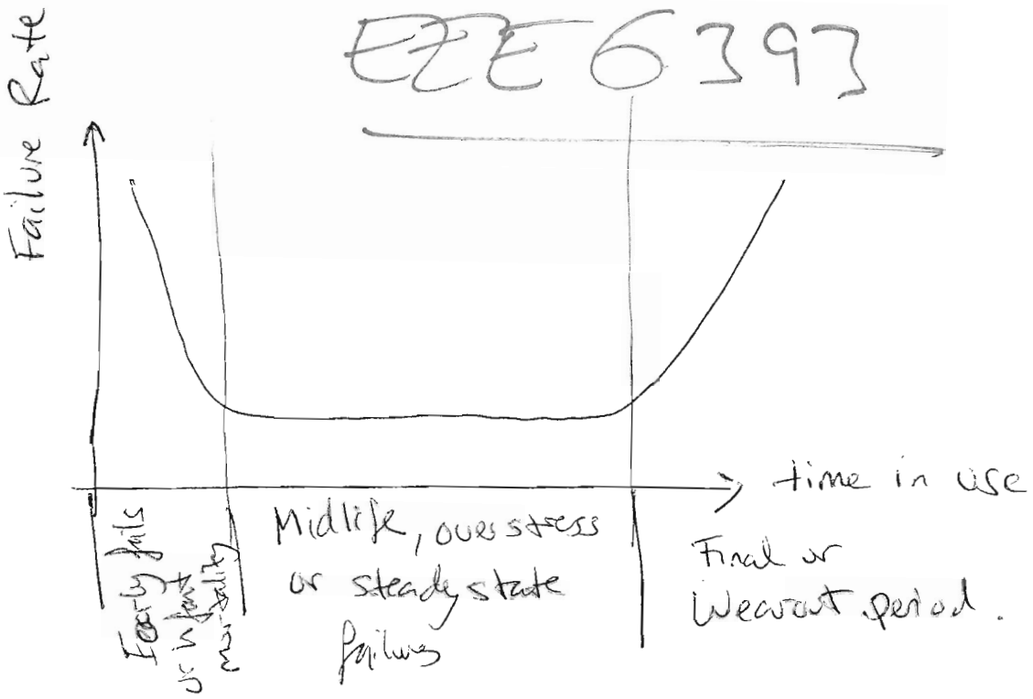

(b)

Burn in screens devices for infant mortality. Infant mortality failures are generally due to manufacturing defects such as pinholes, photo-resist residue, etching defects which generate short circuits over time. Packaging failures can be attributed to scratches, cracks, weak die mounts, voiding or poor wire bonding. To screen for these failures a burn in process is adopted. devices are operated under extream conditions for a few mins/hours. studies show that infant mortality failures have an activation energy of 0.35 - 0.5eV. This is a time consuming process, reduces down-stream costs of system failure and repairs.

C. 150mm Power IC Component.

360 dies / wafer

250 random defects exhibiting a Poissim's distributio

fractional yield:

$$P = \sum_{x=0}^{x=0} \frac{e^{-\lambda} \lambda^{x}}{x!} \qquad \lambda = \frac{\text{defects}}{\text{dies}}$$

$$x = 0 \qquad P = \frac{e^{-\frac{250}{360}} \left(\frac{250}{360}\right)^{0}}{0!}$$

$$= e^{-\frac{250}{360}} = 0.4996$$

$$\text{yield} = \boxed{49.96\%}$$

(D.) target yield ≥ 95%.

$Y = P_0 + nP_1 + nP_2 + \ldots$

Assuming that each redundant circuit would fix the fault i.e $n = 1$.

$$P_x = \frac{e^{-\lambda} \lambda^x}{x!} \qquad x = 0 \text{ to } x = 0.694$$

$$\lambda = \frac{250}{360} = 0.694$$

$$P_0 = e^{-0.694} = 0.4996$$

$$P_1 = \frac{e^{-0.694} \times 0.694^1}{1} = 0.347$$

$$P_2 = \frac{e^{-0.694} \times 0.694^2}{2!} = 0.12$$

$$P_3 = \frac{e^{-0.694} \times 0.694^3}{3!} = 0.026.$$

e. 15 year lifetime. $= 15 \times 365 \times 24 = 131400\,h$

$T_j = 90^\circ C = 363\,K$

$Ea = 0.75$

Test time = 1000

$$\frac{Rate_2}{Rate_1} = \exp\left[\frac{Ea}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right].$$

$$\ln\left|\frac{Rate_2}{Rate_1}\right| = \frac{k}{Ea} + \frac{1}{T_1} = \frac{1}{T_2}$$

$$\ln\left|\frac{1000}{131.4k}\right| \frac{1.38e^{-23}}{0.75 \times 1.609e^{-19}} + \frac{1}{363} = \frac{1}{T_2}$$

$$-4.878 \times 114.332e^{-6} + \frac{1}{363} = \frac{1}{T_2}$$

$$T_2 = 455.1\,K$$

$$= \boxed{182.104^\circ C}.$$

2. a. *A digital watch contains a single integrated circuit (IC). The IC is glued directly to a printed circuit board (PCB); wire bonds are then made to pads on the PCB and then the IC and bond wires are encapsulated with 'glob top' epoxy resin. Discuss the advantages and disadvantages of this 'chip-on-board' assembly method in comparison to packaging the IC within a surface mount package.*

COB: cheap; non-hermetic, hence moisture ingress, hence low reliability; shorter interconnection length, hence better for fast signals; testing and rework not possible; faulty chip condemns entire PCB.

SMT: modular, hence easy for mass production (pick and place machine); easy to test and replace if defective.

(5)

b. *A microprocessor with 1 million gates is flip-chip bonded onto a substrate with two routing layers. The flip chip connections are made using 100 µm diameter solder balls on a square pitch of 0.8 mm. All of the inputs and outputs need to be routed to the edge of the substrate. What is the maximum allowable pitch of the routing on the substrate in line with the edge of the chip? You may assume a Rent exponent $\alpha = 0.45$ and a Rent coefficient $\beta = 0.8$.*

Number of I/Os = $0.8 \times 1000000^{0.45} = 400.9 \sim 400$ (Rent' rule)

Assume n x n = 20 x 20 array of I/Os

Available routing length (bottom) = 4 x pitch x (n-1)

Available routing length (top) = 4 x pitch x (n-1) *

*note – no need to disallow the area of pads on top surface, since these can accommodate the outer row of I/Os, which can route directly outwards.

Total routing length = top + bottom = 8 x pitch x (n-1)

= 8 x 0.8 x 19 = 121.6 mm

Number of connections = 400

Hence 400 tracks + 400 gaps = 800

Assume track=gap

Hence max track width = total routing length / 800

= 121.6/800 = <u>152 um</u>

(5)

c. *For a ball grid array connection, explain the sequence of materials that exist between the aluminium IC bond pad and the copper PCB trace.*

Sequence of materials = under-bump metallisation UBM:

- IC (silicon)
- Bond pad (Al, Cu, Au)
- Passivation (SiO_2) beside bond pads
- Compliant stress relief layer beside bond pads (polymer)
- Adhesion layer (~ 150 nm Cr, Ti, Ni, W or TiW) –adhesion of Cu to Al
- Diffusion barrier layer (~ 150 nm Cr/Cu) – prevent diffusion of solder into bond pad. Needed to prevent formation of brittle intermetallics.
- Solder wetting layer (~ 1 um Cu)

(5)

- Oxidation barrier (~ 20 nm Au) – temporary layer to prevent tarnishing of Cu prior to solder reflow
- Solder ball

d. *The eutectic tin-silver-copper alloy contains 3.7 mass% silver and 0.8 mass% copper. In comparison, a commonly-used solder ('SAC305') contains 3.0 mass% silver and 0.5 mass% copper. Compare and contrast the use of these two alloys within a surface mount assembly process.*

Eutectic: lowest melting point, hence reduced energy costs; abrupt melting point, no 'slushy' phase, hence good for process stability.

Non-eutectic: higher melting point than eutectic; difficult process control due to 'slushy' phase; better for preventing tombstoning of small SMT passives. **(5)**

3. **a.** *The integrated circuits (ICs) on a 10×10 cm printed circuit board (PCB) dissipate a total of 6 W. The PCB has sufficient copper routing and thermal vias to assume that in operation the entire PCB becomes isothermal. What is the temperature of the PCB when the PCB is horizontal? Make use of the data below and state any assumptions that you have made.*

Natural convection heat transfer coefficients for 10×10 cm horizontal plane:
Top surface: $h_{top} = 6\ W\ m^{-2}\ K^{-1}$ *Bottom surface:* $h_{bottom} = 3\ W\ m^{-2}\ K^{-1}$

$R_{top} = 1/h_{top}A = 16.67$ K/W

$R_{bot} = 1/h_{bot}A = 33.3$ K/W

Resistors in parallel, hence: $R_{total} = (R_{top} \times R_{bot}) / (R_{top} + R_{bot}) = 11.14$ K/W

Assume $T_{ambient} = 20$ °C

Hence: $T = R_{tot}Q + T_{ambient} = 11.14 \times 6 + 20 = \underline{86.8\ °C}$

(5)

b. *Suggest ways in which the temperature of the PCB described in **3.a.** could be reduced without reducing the power.*

Fan; orientate PCB vertically; better heat sinking to chasis. **(4)**

c. *Starting from an FR4 laminate, explain the fabrication of a two layer PCB. Include a description of the steps involved in making electrical vias.*

How could the generation of waste copper solution be minimised?

Bookwork. Photolithography to define thin seed layer, then electroplating to build up to desired thickness. Vias formed as follows: photolith to define pads top and bottom; passivate entire board; drill holes; desmear; activate holes (Pd catalyst); electroless then electroplating of copper; strip passivation. **(4)**

d. *The connections between the bond pads of a high speed IC and the legs of its quad flat pack (QFP) package have the following electrical characteristics:*
L = 4 nH; C = 0.6 pF; R = 5 mΩ.

Suggest suitable dimensions for the microstrip lines on the PCB to which it is **(5)**

soldered. You may assume the following relationship for a microstrip line:

$$Z_0 = \frac{87}{1.41+\sqrt{\varepsilon_{eff}}} \ln\left(\frac{5.98h}{0.8w+t}\right)$$

- where h, w and t are the height, width and thickness of the track and the other symbols have their usual meanings.

Why is a QFP package preferable to a dual in-line (DIP) package for this IC?

$Z(IC) = (L/C)^{½} \sim 80\ \Omega$ - for the IC package

For matching we want Z(PCB) = Z(IC)

Substitution into equation, assuming t = 35 um; ε ~ 3; w = 200 um

Gives h = 290 um.

DIP package will have longer connections and, more importantly, different length connections to the pins. This will result in unequal signal propagation delays.

e. *Explain the positioning and purpose of the decoupling capacitors that often surround a high speed IC.*

Provide current during rapid switching of transistors. Situated close to chip to avoid extra parasitics. **(2)**

4. **a.** *The 'efficiency' of an integrated circuit (IC) packaging technology is a complex function of many parameters including the following: electrical performance; thermal performance; reliability; cost; size. For a complex, high-speed IC design, place the following five packaging technologies in order of increasing efficiency: through-hole package; system-in-package; flip-chip; surface-mount package and system-on-chip.*

THP; SMT; flip-chip; SiP; SoC **(2)**

b. *The current design for a CMOS image sensor IC in a mobile phone consists of a rectangular array of elements – 'pixels'. Each pixel comprises a photodiode plus associated circuitry to generate a digital signal. The digital signals leave the image sensor IC via four levels of metallisation. Explain, with the aid of sketches, how through silicon vias (TSVs) could be used to improve the light gathering capability of the sensor. Include a discussion of the necessary TSV fabrication steps in your answer.*

In normal image sensor the routing is on top of the CMOS, hence blocking light to photodiodes. By using TSVs, metallisation can be on bottom of chip, thus increasing optical sensitivity.

TSV fab (likely before CMOS, though could be after): pattern photoresist; drill blind holes by Bosch process (DRIE) or laser; insulate holes; metallise holes (Cu electroplating); bond to carrier wafer; thin wafer by grinding; metallise bumps; add routing layers; add ball grid array; bond to substrate; underfill; remove carrier wafer. **(8)**

c. *The continued miniaturisation of microsystems is leading to the development of 'interposers', which act as very high pitch circuit boards. Most interposers are made from silicon, but there is also interest in manufacturing them from silicate glass. Compare and contrast the use of these two materials for this application.* **(2)**

Main difference is in thermal expansion coef. Mismatch if glass interposer is used with Si IC. Glass will be cheaper and less fragile (?) than Si.

d. *A 10×10×1 mm insulated gate bipolar transistor (IGBT) module dissipates 200 W and is packaged on a direct-bond copper (DBC) substrate, as shown schematically in Figure 4 (below). The bottom copper surface is in contact with a water cooling channel, which is maintained at room temperature. What is the temperature of the top surface of the silicon IGBT? Please show your working and indicate what assumptions you have made. Thermal conductivity data is provided at the front of the exam paper.*

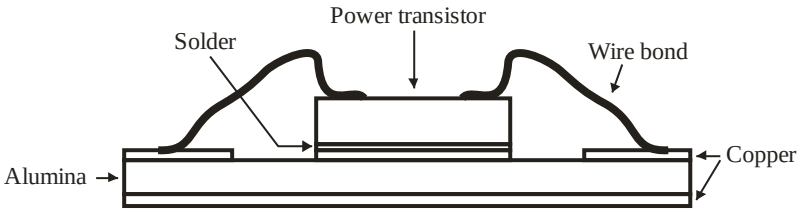

Figure 4

Assume that heat flow through wire bonds can be ignored.

Assume no heat spreading in alumina layer.

Thermal resistances for layers = R = L/kA

Where L = layer thickness, k = thermal conductivity and A = area = 10^{-4} m

R_{Si} = 0.08 K/W (assume L = 1 mm)

R_{solder} = 0.016 (assume L = 100 µm)

R_{copper} = 0.005 (assume L = 200 µm)

$R_{alumina}$ = 0.24 (assume L = 600 µm)

Hence R_{total} = 0.346 K/W

Assume $T_{ambient}$ = 20 °C

Fourier's law of heat flow: $\Delta T = RQ$ hence:

T-20 = 0.346 x 200 hence <u>T = 89 °C</u>

(6)

e. *If the junction to case thermal resistance of the package in **4.d.** is reduced to R_{jc} = 0.1 °C/W by replacing the alumina with diamond, would it be possible to use air-cooling instead of water-cooling? Assume a heatsink / fan combination with a case to ambient thermal resistance R_{ca} = 1 °C/W is available. Explain your answer.*

$R_{total} = R_{jc} + R_{ca}$ = 1.1 °C/W hence $T_{junction}$ = 1.1 x 200 + 20 = <u>240 °C</u>

<u>This is much too hot for silicon</u> **(2)**

GLW / MRS