Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2012-13 (2 hours)

EEE6031 Advanced Computer Architectures 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

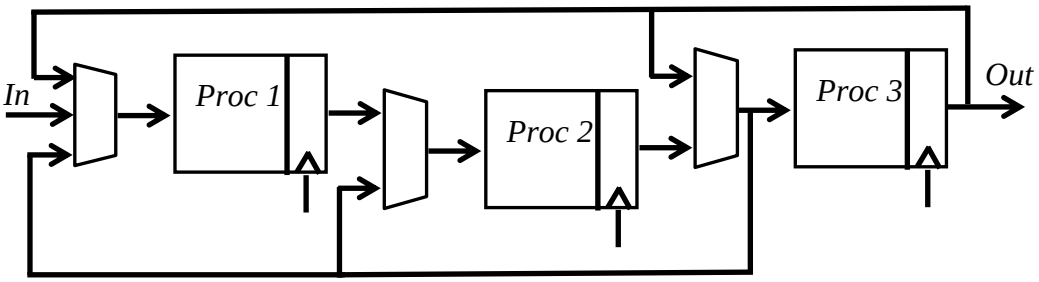
1. a. Describe a hypercube connection for a loosely-coupled multiprocessor. **(4)**

b. What is the difference between packet- and circuit-switching for transmitting data in a network. What are the advantages and disadvantages of both schemes? **(4)**

c. Draw the block diagram for a 2:3:2 (*s*:*f*:*l*) Banyan network where the terms have their usual meaning. **(6)**

d. Derive an expression for the complexity of an *s*:*f*:*l* Banyan network. **(6)**

2. a. A pipelined system appears as in **Figure 2**.



The sequence of processing activities is:

In→Proc1→Proc2→Proc2→Proc3→Proc3→Proc1→Proc2→Proc3→Out

For this sequence:

i. Draw the reservation table **(4)**

ii. Calculate the collision vector **(2)**

iii. Find the throughput of the pipeline **(4)**

iv. Find the utilisation of each processing block **(2)**

b. You notice that the throughput can be improved by some *minor* changes to the pipeline. Show how, with some minor changes, the peformance can be improved and calculate a new throughput to show that performance has improved. **(8)**

3. a. **i.** State Amdahl's Rule and identify its significance in understanding the benefits of parallelising any activity. **(4)**

ii. Show how the basic Amdahl's rule can be extended to cope with a more generalised case of an activity where separate parts can be parallelised differently. **(4)**

b. A task running on a system consists of a bidirectional communication interface (running on a separate control processor) that is receiving a sequence of messages and farming each of the messages out to a number of separate data processors for processing. The results from each processor are transferred back to the communication interface and transmitted as a sequence of messages.

Each received, input message takes 10μs to receive, decode, and farm out. Each transmitted, result message takes 1.5μs to collect, encode, and transmit. Each message can be processed in 170μs.

i. Identify and justify your choice for the number of separate data processors (for processing the messages) that you would use in this system. **(4)**

ii. What is the throughput of message for your chosen number of data processors? **(2)**

iii. What is the latency associated with each message? **(2)**

iv. A decision is made to alter the communication interface from bidirectional to unidirectional. How does this affect the design and performance of the system? **(4)**

4. a. What characteristics make a memory technology amenable to use within a memory hierarchy where block data transfers are used to/from the memory? **(4)**

b. Describe, particularly, how SDRAM (the dominant memory used for main memory in a system) is designed to be amenable for use within a memory hierarchy. **(3)**

c. Why is it important to use *Read-Around-Write* in the buffer systems that sit between the caches and main memory? **(3)**

d. A memory sub-system has the following characteristics:
Initial access time 5ns
Any subsequent access 5ns
Word width 32 bits

It is required that the memory sub-system, where it is used in the hierarchy, must be capable of supplying blocks of contiguous data at an average rate of at least 3 Gbytes/sec and that interleaving will be used to achieve this.

i. Describe how interleaving works and how it helps. **(4)**

ii. Show that the memory be four-way interleaved to meet the data rate objective. **(2)**

iii. Does the interleaving place any limitations on the block/line size at this point in the hierarchy? **(2)**

iv. The memory technology is changed so that the initial access time is 5ns but subsequent, contiguous access times are now 0.5ns. What is the minimum size of block transferred now to meet the data rate requirement – without using interleaving. **(2)**

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