Exam Answers 1999/2000

1. *Students have been taught about types of chip implementation and the financial arguments behind which type you would use in different circumstances. However, I have not covered this specific situation. Nevertheless, this should be a fairly straightforward question provided students have understood the various types of implementation and can put together a coherent argument. The following is the line I would expect students to take and a rough marking scheme is indicated, but I would award marks for intelligent and relevant reasoning outside the parameters set here.*

We must consider any extra NREs caused by the change in implementation style. These will be dominated by mask costs which impose a unit cost per chip of
number of masks x cost per mask / number of chips.
in this case 1600 x 15 /60000 = 0.4 Euros per chip
Some students may compare this with the costs of the mask for the gate array, but of course, in this example those costs do not represent new NREs since the masks already exist.
[5 marks for mask costs]
We need to estimate the change in the silicon area costs. The costs for the current chip is given by
cost per chip= cost per wafer/ number of good chips per wafer
= cost per wafer/(number of chips per wafer x yield)
=cost per wafer x area per chip / area of wafer x yield = 290* 64/1.8e4*0.8=1.3Euros
Note that here we have used a value of 80% for the yield although this information is not supplied in the question. This is the first of the bits of information that the students need to realise is missing. I would accept any value that the students choose between 50% and 95%. The main point is that they realise that yield is important.
To estimate the change in area cost we need to estimate the change in chip area. This is not known, but we can expect a minimum of 25% reduction since this is the number of unused cells in the gate array. However, this can be taken as an absolute minimum since area for the cell based design can be laid out in a form appropriate to the particular design. For the purposes of this illustration I will assume an area reduction of 30% , but I would accept any value between 26% and 50% from the students. For full marks they need to note the wasted gate array area and to argue that the cell-based allows further optimisation.
So cost reduction = 0.3*1.3=0.4Euros per chip.
[8 marks for area costs]
Students should mention that such costs exist, but are likely to be small since the design already exists as a gate array so simulation to confirm function will be small. [3 marks for design costs]
Thus in this example the wafer cost exactly balances the area cost so there is no advantage in changing the implementation.. This becomes particularly true once we consider the design costs associated with the change.. [2 marks for overall conclusion]
The final conclusion will depend on the assumption the students have made, but I will award marks for any conclusion consistent with sensible assumptions.
[2 marks will be reserved for an overall logical argument]

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2. The first part of this question asks the students to evaluate Vt and beta by plotting appropriate graphs from the characteristics.
The appropriate graphs are in the saturation region where

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

So students should plot root Ids vs Vgs. The data provided includes a sub-threshold current and some scatter in Vgs so that students who do not plot and make appropriate use of the graphs will get the

wrong values. (We find students are often guilty of using only a single point in data to make such a measurement. This will test which use correct engineering practice)
For students who have grasped the characteristics of MOSFETs this should be very straightforward.
The correct values are; for the n-channel transistor Vt=1.2V, beta=5e-4A/V^2
for the p-channel transistor Vt=-1.2V, beta=1.25e-4A/V^2

Proving both devices are in saturation. This is set as an exercise for students during the year, so diligent students should again find this reasonably straightforward.
The argument is:

Saturation occurs for the n-type if

$$V_{ds} \geq V_{gs} - V_t$$

And for p-type if

$$-V_{ds} \geq -(V_{gs} - V_t)$$

If an inverter has input voltage Vin=Vinv such that if Vin=Vinv, Vout=Vinv the for the n-channel Vgs=Vinv, Vds=Vinv and since Vt is positive Vds>Vgs-Vt thus saturation
For p-channel
Vgs=Vinv-5 Vds=Vinv-5 Thus we have saturation if 5-Vinv>5-Vinv+Vt since Vt is negative, this is true. QED

The final part has two possible solutions. One is very quick and elegant, but requires students to make a conceptual leap that I doubt that many will do. The other is a brute force modification of a derivation supplied in the course.
Both solutions rely on recognising that Idsn=-Idsp and that the devices are in saturation.
The elegant approach is just to plot

And look for the intercept voltage.

The approach I expect most students to take is to say

$$I_{dsn} = -I_{dsp}$$

$$\Rightarrow \beta_n \left(V_{gsn} - V_{tn}\right)^2 = \beta_p \left(V_{gsp} - V_{tp}\right)^2$$

$$\sqrt{\frac{\beta_n}{\beta_p}} = \frac{V_{inv} - 1.2}{V_{inv} - 5 + 1.2} = \frac{V_{inv} - 1.2}{V_{inv} - 3.8} = \pm 2$$

$$\Rightarrow V_{inv} = 6.6$$

$$or$$

$$V_{inv} = 2.9$$

Where 2.9 is the physically realistic value.

3. Standard bookwork: I expect an answer on the lines: When testing a VLSI circuit we want tests that will detect the maximum number of possible faults. Fault cover describes the proportion of possible faults that a particular set of tests will detect.

Exhaustive test : This makes no assumptions so we need to apply all possible combinations of inputs. In this case there are 3 inputs so 8 tests are required.

The fault matrix looks like:

TEST abc	fault free	A0	A1	B0	B1	C0	C1	X0	X1	Y0	Y1
000	10	10	00	10	00	10	11	00	10	10	11
111	00	00	00	00	00	00	00	00	11	00	00
001	11	00	11	11	00	10	11	00	11	10	11
011	00	00	00	11	01	00	01	00	11	00	01
010	00	00	00	10	00	00	00	00	00	00	00

This set of tests gives a set of outputs different to the fault free case for each of the possible faults. However, it is clear that the tests 010 and 111 are redundant since the other tests between them detect all the possible faults.

4 (a) Students are shown this circuit during the course and asked to work out how it works as an exercise. Diligent students should therefore all be able to get the answer to this.
Essentially they just need to say:
If enable is low then the output of the NAND gate is high, whilst that of the NOR gate is low irrespective of the data value. Since these outputs turn on neither of the output transistors, in this state the circuit does not drive the output line. However, if enable is high, the outputs of the NAND and NOR are low if data is high, so the output is driven high. But if data is low then the NAND and NOR provide high levels so the output is low.

This is better than a gate based on pass transistors since the pass transistors act as a resistance in the output line where the maximum drive is needed to overcome the large load capacitance.

(b) The rise time is governed by the p-channel transistor

$t_r = 3CR$

$\therefore R = 3*10e-8/2e-9 = 150$

but

$R = -1/\beta\left(V_{gs} - V_t\right) = 1/4\beta$

$\therefore \beta = 1/4R = 1/600$

now

$\beta = C_{ox}\mu W / L$

$C_{ox} = \varepsilon / d = 2e-11/1e-8 = 2e-3$

$\Rightarrow W = L / C_{ox}\mu 600 = 0.5e-6/600*2e-3*.04 = 10.4\mu m$

(c) This question is to see to see if students can translate the abstract ideas into a physical description. If they can do so then the answer is easy. It looks like: