Data Provided:

Equations and physical constants at end of paper

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (3.0 hours)

EEE348 Electronics and Devices

Answer **FIVE QUESTIONS** comprising **AT LEAST TWO** each from **part A** and **part B. No marks will be awarded for solutions to a sixth question, or if you answer more than three questions from parts A or B.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Part A

A1 The *pull-down* network for a digital CMOS gate is as shown in **Figure A1**:

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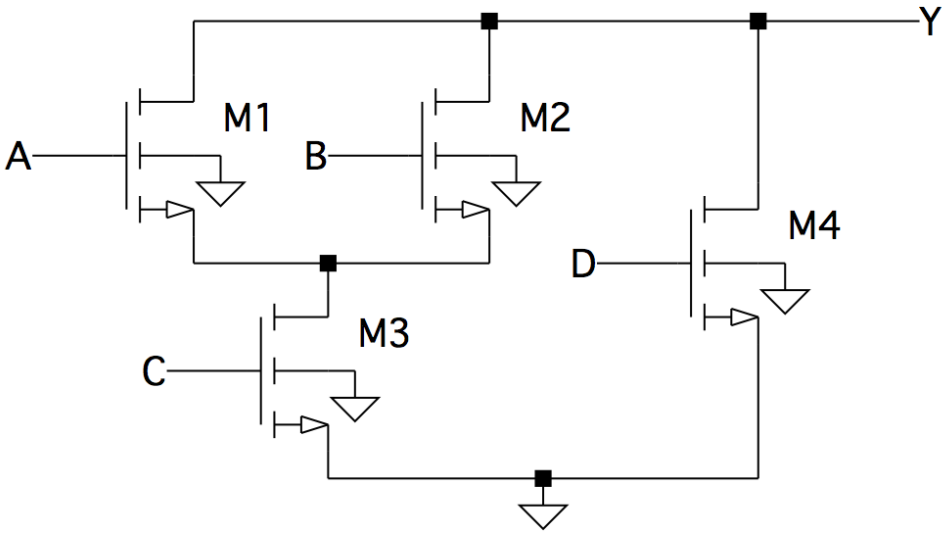

Figure A1: Pull-Down Network

a. Draw the corresponding *pull-up* network for the gate in **Figure A1**. **(4)**

b. Derive an expression for **Y** in terms of **A**, **B**, **C**, and **D**. **(4)**

c. Size the transistors **M1**…**M4**, assuming that the gate is *minimum-sized*. State any assumptions made. **(4)**

d. What is the justification for connecting all of the substrate connections for **M1**…**M4** to the negative supply rail? What problem can this, potentially, cause? **(4)**

e. If circuit in **Figure A1** were used in an environment where the output of the **(4)**

circuit, **Y**, could sometimes *under-shoot* (that is, a voltage at the output could be below the negative supply rail), the consequence could be that one or more of the transistors in the circuit could be damaged. Describe how this could happen and what might be done to prevent this problem.

A2. **a.** How is a *master-slave* D-type flip-flop organised. Draw a transistor-level schematic, identifying the function of each part. **(4)**

b. What is the constraint on the clock used for a *master-slave* D-type flip-flop? Draw a schematic for a non-overlapping clock generator. **(4)**

c. One of the problems that can occur with a flip-flop is *metastability*. What is *metastability* and what is the solution to minimise its occurrence. **(2)**

d. A system consists of two separate clock domains (D1, and D2). Data from D1 is being transferred to D2, as shown in Figure A2.

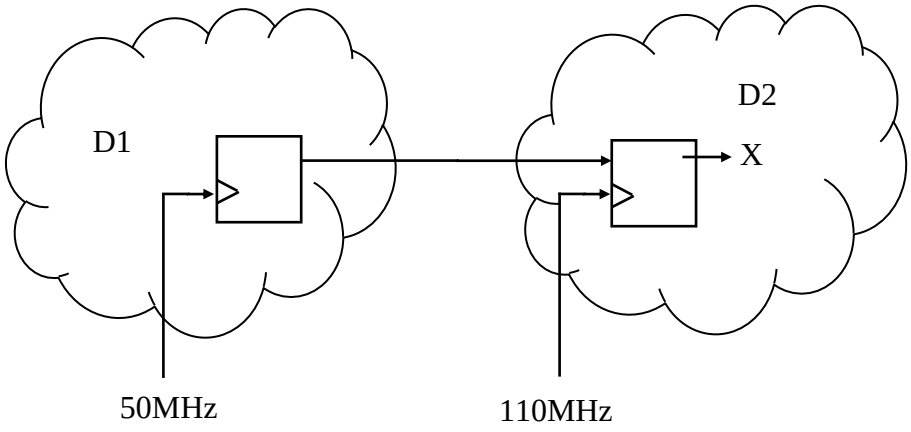

Figure A2: Transfer of Signal Between Clock Domains

i) You know that, for the fabrication process in which the components are implemented, $T_0=t_c=0.5$ns. Show that you would expect to see approximately 0.0175 *upsets/second* at point X. Please ensure that you justify your choice of t_r. **(4)**

ii) Is 0.0175 *upsets/second* at point X a reasonable result? If not then why? **(2)**

iii) You decide that you need the number of *upsets/second* at point X to be fewer than $2.5\text{x}10^{-10}$. How would you design the receiving circuit in D2 to meet this requirement? **(4)**

A3 **a.** Give a brief description of the following terms:

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i) Overdrive voltage,
ii) Transconductance,
iii) Channel length modulation. **(3)**

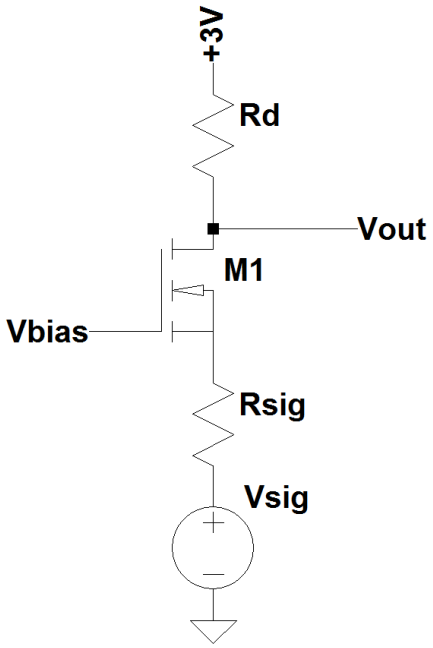

Figure A3: A SPICE model of a common gate amplifier.

b. **Figure A3** shows a SPICE model for a common gate amplifier. The MOSFET in the circuit, labelled M1, has the following parameters:

V_{TO}=0.6V, K_n=100μA/V^2, W/L = 8μm/1μm, λ=0.05V^{-1}.

The amplifier is to be biased at a drain current I_{D0}=150μA.

i) Calculate the overdrive voltage, V_{OV}, the transconductance, g_m, and the output resistance, r_o, of transistor M1. **(3)**
ii) Draw the small signal model of this circuit. Use the 'T' model for transistor M1 and include the effects of channel length modulation – you may ignore parasitic capacitances. **(5)**
iii) By ignoring the effects of channel length modulation, derive an expression for the gain of the amplifier, showing your working. Calculate this gain if the signal source V_{sig} has an output resistance, R_{sig} of 5kΩ and the drain resistor, R_d, is 50kΩ. **(3)**

c. For implementation on an IC, the drain resistor in **Figure A3** can be replaced by a PMOS current mirror active load.

i) Redraw **Figure A3** to show how you would implement this current mirror, showing where an external resistor would be connected to realise the reference current for the mirror. **(4)**
ii) If the PMOS transistors used in your mirror have a channel length modulation parameter λ=0.025V^{-1}, determine the gain of your redesigned amplifier (you may again ignore channel modulation effects for transistor M1 in this calculation). The bias current remains the same at 150μA. **(2)**

A4
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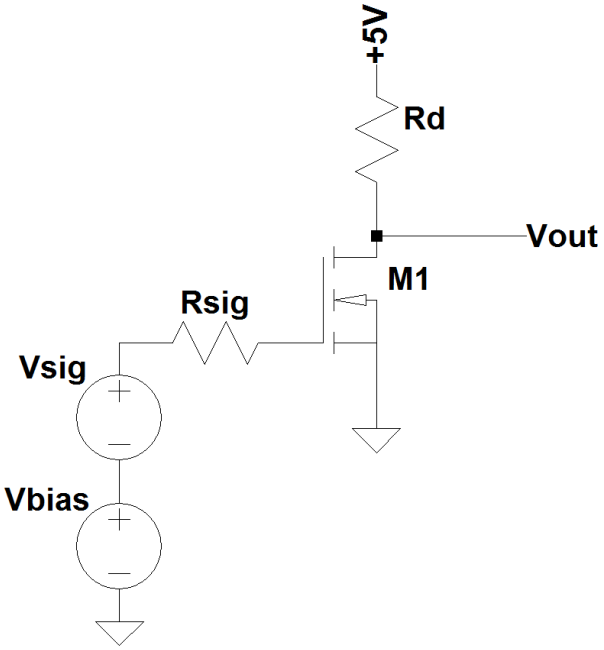

Figure A4: A SPICE model of a common source amplifier.

Figure A4 shows a common source amplifier. The amplifier operates with a transconductance of g_m=1.5mS. The parasitic gate-source and gate-drain capacitances are: C_{gs}=C_{ds}=10fF.

a. The bias voltage, V_{bias}, in **Figure A4** could be realised using a potential divider. Explain why this is not the ideal solution and give an example of a situation where it may cause a problem. Suggest an alternative method that could be used to bias the amplifier. **(5)**

b.

i) Draw the small signal model of the amplifier in **Figure A4**. Use the 'π' model for transistor M1 and include the dominant parasitic capacitances in your drawing. **(5)**

ii) The amplifier has a drain resistance R_d=5kΩ. Use this value and your small signal model to calculate the midband gain of the amplifier. Explain any assumptions you make in this calculation. **(3)**

iii) Calculate the two Miller capacitances for this amplifier and describe where they would appear in your small signal model (e.g. 'between the drain and source of M1', 'between the source of M1 and ground' or similar). **(3)**

iv) Calculate an approximate upper cutoff frequency for the amplifier when a source is connected whose output resistance, R_{sig}, is 100kΩ. State any assumptions made. **(4)**

Part B

B1. **a.** Sketch and label the current-voltage characteristics of a p-n junction solar cell in the dark and when illuminated with a strong light. **(2)**

b. The so-called Passivated Emitter & Rear Locally-diffused (PERL) solar cell produces a very high conversion efficiency.

i. Describe how the Silicon PERL cell achieve high absorption efficiency.
ii. Explain the design features that maximise the photocurrent generated in the PERL cell. **(7)**

c. Discuss one major advantage as well as a disadvantage of using a narrow bandgap semiconductor, such as InGaAs, for constructing a solar cell. **(4)**

d.
i. Describe manufacturing modifications required to reduce the cost of Si solar cell so that large area solar panels can be manufactured.
ii. Explain major drawbacks of the modifications you proposed in (i).
iii. Propose and describe a method to overcome the drawbacks discussed in (ii). **(7)**

B2. **a.** List the two essential conditions to achieve lasing in a GaAs pn diode. **(2)**

b. With the aid of diagrams, describe the key features of a GaAs-AlGaAs Fabry Perot laser. In your answer you should discuss how the features help to improve the laser performance. **(10)**

c. In fiber optic communication, wavelength division multiplexing (WDM) is a technique that combines a number of signals at different wavelengths into a single fiber to increase the data transmission.

i) Explain why a simple stripe laser is not suitable for WDM.
ii) Describe a laser structure that can be used in WDM.
iii) Discuss the advantages and disadvantages of the laser structure in (ii) over a Fabry Perot laser. **(8)**

B3. **a.** Using a band diagram discuss the origin of the broad spectrum of light emitted by a simple LED. **(4)**

b. An LED is not suitable for high modulation rate, required for optical communication. Explain why? **(2)**

c. The bandgap of $Al_xGa_{1-x}As$ is given by 14242 +1.247x. Describe in detail a design for an LED which can achieve bright emission of near infrared light with a wavelength of 800 nm. A band diagram should be included in your answer. **(7)**

d. The injection efficiency of an LED is given by $\gamma_{inj} = \frac{J_e}{J_e + J_{GR} + J_h}$, where J_e is due to electron injection, J_h is due to hole injection and J_{GR} is due to generation-recombination process. Clearly the injection efficiency improves as J_h and J_{GR} are suppressed. For an LED p-i-n structure, discuss

i) two approaches to reduce J_h
ii) how the doping concentration in the i-layer will influence the injection efficiency
iii) how temperature will affect the injection efficiency **(7)**

B4. **a.** Describe why is a negative differential resistance of interest to electronic engineers? **(2)**

b. Discuss how the Gunn effect leads to a negative differential resistance in semiconductors. **(6)**

c. i) Propose a suitable diode structure to achieve Gunn effect.

ii) With the aid of velocity vs. electric field diagrams, explain how high frequency oscillation is produced in this Gunn diode. **(8)**

d. Conventional Gunn diodes provide useful microwave power up to around 150 GHz. Describe an alternative microwave deviceAll that are used for applications at higher frequencies. **(4)**

CHT/NLS/AM/TWANG

You may require the following for Part A:

The Shichman-Hodges model:

In the *triode* region:

$$I_D = K_n \frac{W}{L}\left(V_{OV} - \frac{V_{DS}}{2}\right)V_{DS}$$

In the *saturation* region:

$$I_{D0} = K_n \frac{W}{L}\frac{{V_{OV}}^2}{2}$$

In the *ohmic* region:

$$I_D \approx K_n \frac{W}{L} V_{OV} V_{DS}$$

Regardless of the region:

$$I_S = I_D$$

$I_G = 0$

Channel length modulation:

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

The overdrive voltage:

For an NMOS device: $V_{GS} = V_{TO} + V_{OV}$

For a PMOS device: $V_{GS} = -(|V_{TO}| + |V_{OV}|)$

MOSFET output resistance:

$$r_o = \frac{1}{\lambda I_{D0}}$$

MOSFET transconductance:

$$g_m = K_{n,p}\frac{W}{L}V_{OV}$$

Metastability:

$p_u = T_0 e^{-\frac{t_r}{t_c}}$ upsets/clock/data

You may require the following for Part B

$$f^e(E) = \frac{1}{\exp\left(\frac{E - E_{Fn}}{kT}\right) + 1}$$

$$f^h(E) = \frac{1}{\exp\left(\frac{E_{Fp} - E}{kT}\right) + 1}$$

$$I_d = I_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$

$$I_s = qAN_cN_v\left[\frac{1}{N_A}\sqrt{\frac{D_e}{\tau_e}} + \frac{1}{N_D}\sqrt{\frac{D_h}{\tau_h}}\right]\exp\left(-\frac{E_g}{kT}\right)$$

$$J_e = \frac{qD_e n_p}{L_e}\exp\left(\frac{qV}{kT}\right)$$

$$J_h = \frac{qD_h p_n}{L_h}\exp\left(\frac{qV}{kT}\right)$$

$$J_{GR} = \frac{qn_i W}{2\tau}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right]$$

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_a N_d}{{n_i}^2}\right)$$

$$V_{OC} = \frac{kT}{q}\ln\left(1 + \frac{I_{ph}}{I_s}\right)$$

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)V_{bi}}$$

$$L_{e(h)} = \sqrt{D_{e(h)}\tau_{e(h)}}$$

$$D_{e(h)} = \frac{kT}{q}\mu_{e(h)}$$

$$I_{tot} = I_s\left[1-\exp\left(\frac{q(V-I_{tot}R_s)}{kT}\right)\right]+I_{ph}$$

$$I_{ph} = qAG(L_e+W+L_h)$$

$$\eta = \left(\frac{I_{ph}}{q}\right)\left(\frac{P_{opt}}{h\nu}\right)^{-1}$$

$$\eta = (1-R)[1-\exp(-\alpha W)]$$

$$R_{res} = \frac{\eta q\lambda}{hc}$$

$$I_{ph} = \frac{\eta\lambda P_{opt}}{1.24}$$

$$t_{diff} = \frac{4x^2}{\pi^2 D_p}$$

$$f_{RC} = \frac{1}{2\pi RC}$$

$$f_{3dB\_tr} = \frac{0.4}{t_r} = \frac{0.4v_s}{W}$$

$$f_{IMP} = \frac{v_{sat}}{2(w-x_a)}$$

$$M = \frac{1}{1-\left(\frac{V-IR}{V_b}\right)^{n_m}}$$

$$V_B = E_m x_a + \left(E_m - \frac{qQ_c}{\varepsilon_s}\right)(w-x_a)$$

$$SNR = \frac{I_{ph}^{\ 2}}{<i_s^{\ 2}>+<i_{th}^{\ 2}>} = \frac{(q\eta P_{opt}/h\nu)^2}{2qI_T B + 4kTB/R_{eq}}$$

$g(h\nu) = G_{las}[f^e(E^e)+f^h(E^h)-1]$ cm^{-1} where $G_{las} = 5.6\times10^4\,\frac{(h\nu-E_g)^{1/2}}{h\nu}$ for GaAs

$$J_{th} = \frac{qd_{las}n_{th}}{\tau_r(J_{th})}$$

PHYSICAL CONSTANTS

Quantity	Symbol	Value
Boltzmann constant	k	1.38066×10^{-23} J/K
Electron rest mass	m_o	9.1095×10^{-31} kg
Electronic charge	q	1.60218×10^{-19} C
Permeability in vacuum	μ_0	1.25663×10^{-8} H/cm
Permittivity in vacuum	ε_0	8.85418×10^{-14} F/cm
Planck constant	h	6.62617×10^{-34} Js
Speed of light in vacuum	c	2.99792×10^{10} cm/s
Thermal voltage at 300 K	kT/q	0.0259 V

Dielectric constant = 11.9 (Si), 12.4 (GaAs), 13.9 (InGaAs)