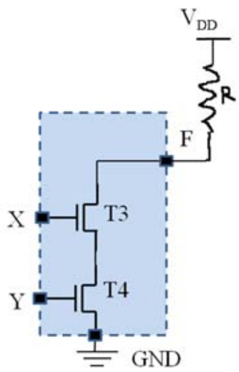
EEE225 Solutions 2015-2016

1. (i)

Open-Drain refers to a device where the drain terminal of the output transistor is unconnected. It must be externally connected to V_{DD} by an external pull-up resistor.



(2)

When x = 0 y = 0 > T3 & T4 both off

x = 0 y = 1 > T3 is off

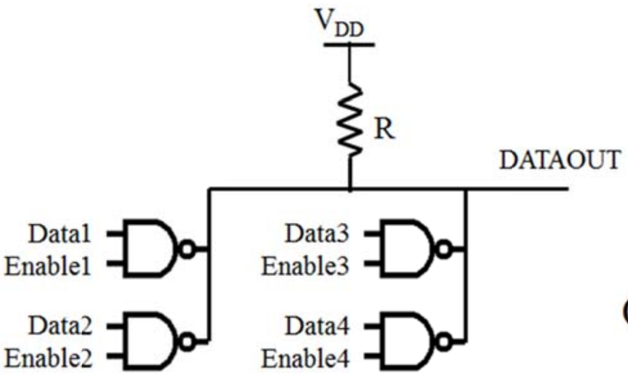
x = 1 y = 0 > T4 is off

Output F will be pulled HIGH in each case.

When x = 1 y = 1 > T3 & T4 are both on.

Output F will be connected to ground and LOW. **(2)**

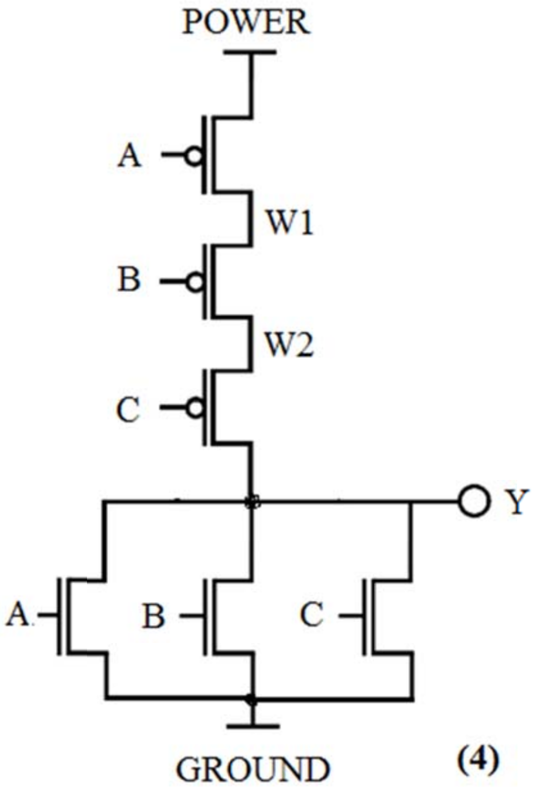
1. (ii)



(2)

This configuration allows several devices to put data onto a common bus. Only one device at a time can drive this bus, all other devices must be in the 'open' state and will be pulled HIGH.
The driving device will take its enable line HIGH (all other enables must be LOW). If its data input is LOW the output is pulled HIGH. If its data input is HIGH, the output is driven LOW. **(2)**

2.



(4)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

(3)

3-input NOR function (1)

3.

Static Power Consumption**:** Power consumed when the output is not switching. **(1)** This is leakage currents and very small. **(1)**

Dynamic Power Consumption: Consists of transient power consumption which is the power due to the partial short-circuiting of the transistors during switching **(2)**and capacitive-load power consumption which is power consumed in charging external load capacitances. **(1)**

Not all gates will be switching every clock cycle so the dynamic power is often multiplied by α which is a switching activity factor **(2)** and lies between 0 and 1. **(1)**

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4a. If $R_1 = 10k\Omega$, $R_2 = 20k\Omega$, $R_3 = 2.5k\Omega$
AND $C = 10nF$.

THE LOW FREQUENCY GAIN:

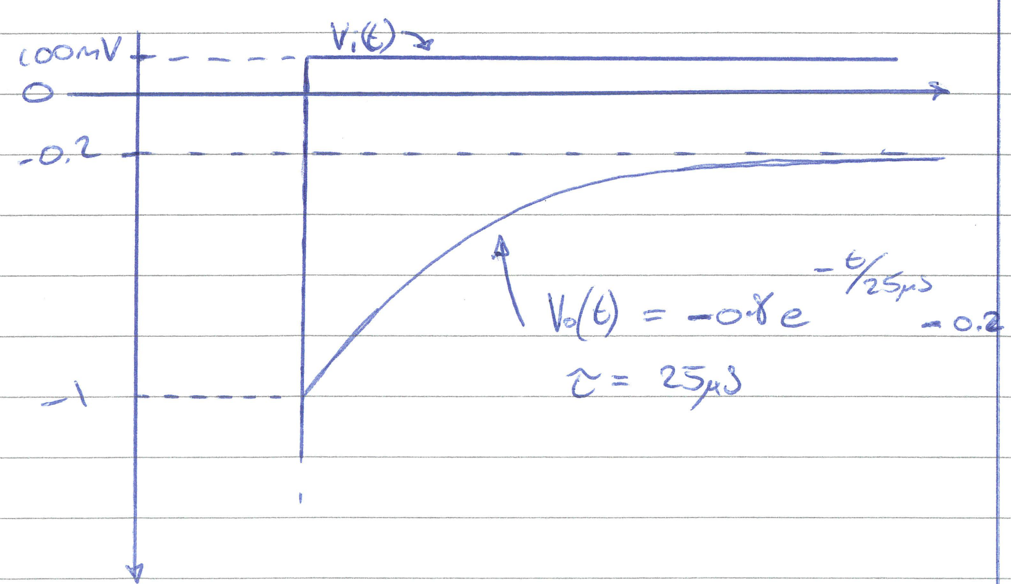
$$\text{LF GAIN} = -\frac{R_2}{R_1} \quad \because x_c \to 0 \text{ AS } f \to \infty$$ 1 (LF)

THE HIGH FREQUENCY GAIN: 1 (JUSTIFY)

$$\text{HF GAIN} = -\frac{R_2}{R_1 // R_3} \quad \because x_c \to 0 \text{ AS } f \to \infty$$ 1 (HF)

$$\text{LF GAIN} = -\frac{20}{10} = 2$$

$$\text{HF GAIN} = \frac{-20}{(10//2.5)} = \frac{-20}{\left(\frac{10 \times 2.5}{10 + 2.5}\right)} = -10$$



1 (SHAPE $V_i(t)$)
1 (Y-AXIS VALUES)
1 (SHAPE V_o)
1 (τ)
1 (EXPONENTIAL EQ=)

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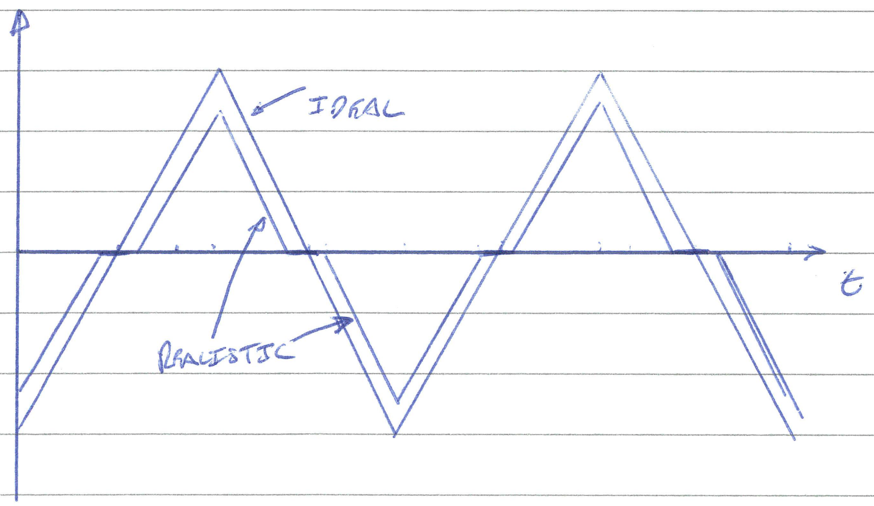
5 CROSSOVER DISTORTION ARISES WHEN CONDUCTION IS TRANSFERRED FROM ONE TRANSISTOR TO THE OTHER IN THE OUTPUT STAGE OF A PUSH PULL CLASS B AMPLIFIER, THE PROBLEM IS CAUSED BY THE DEPENDENCE OF TRANSCONDUCTANCE ON COLLECTOR (OR DRAIN) CURRENT AND HENCE OUTPUT VOLTAGE.

EVEN IF g_m WAS INDEPENDENT OF I_C (I_D) THERE WOULD STILL BE A PROBLEM BECAUSE THERE WOULD BE A CHANGE IN THE PUSH PULL OUTPUT RESISTANCE WHEN CONDUCTION WAS TRANSFERRED UNLESS DEVICE BIASING WAS PERFECT i.e. OUTPUT DEVICES NEVER ON OR OFF TOGETHER. 180° CONDUCTION FOR BOTH.

THE EFFECT ON THE WAVEFORM IS:



IN A REAL CIRCUIT THE PROBLEM CAN BE REDUCED TO A POINT WHERE IT IS NO LONGER SIGNIFICANT BY ARRANGING FOR SOME OVERLAP OF CONDUCTION ANGLE OF THE OUTPUT DEVICES.

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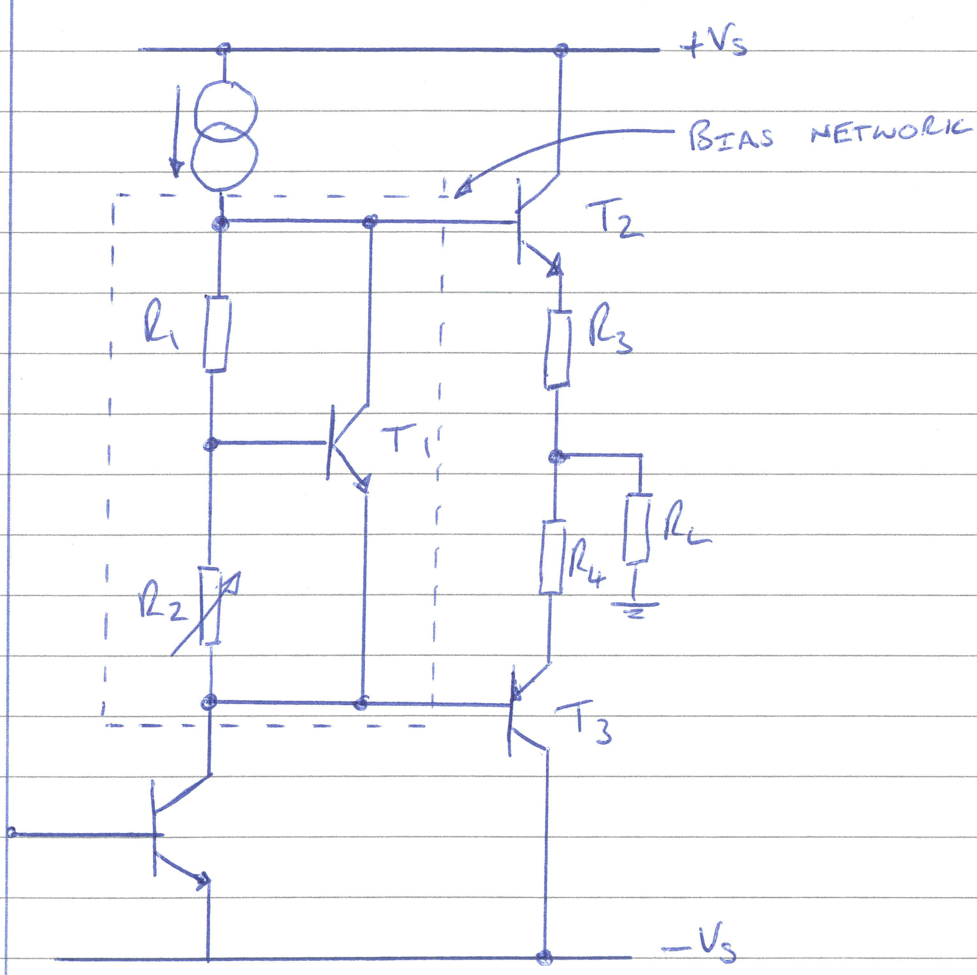
A CIRCUIT THAT CAN ACHIEVE THIS IS SHOWN BELOW. R_1, R_2 & T_1 ACT AS A FLOATING VOLTAGE SOURCE WHICH, IN CONJUNCTION WITH R_3 & R_4 CONTROLS THE QUIESCENT CONDITIONS. 1



3

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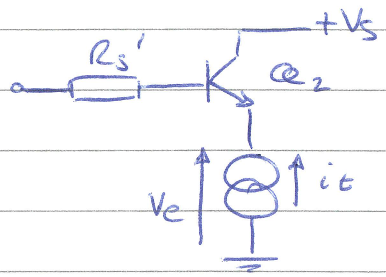
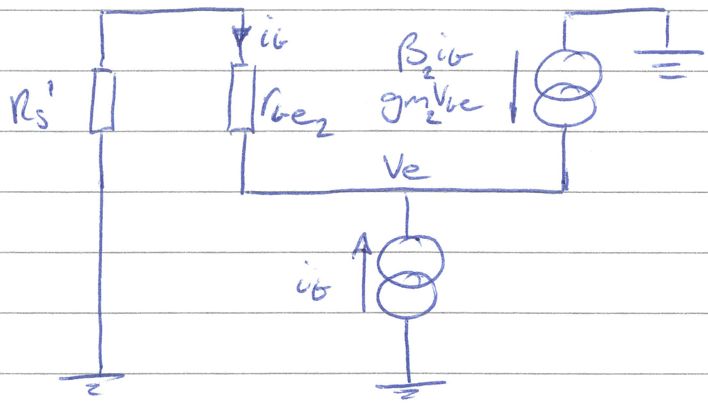
6

THE "TRICK" HERE IS TO REALISE THAT Q_2 & Q_1 ARE CONNECTED IN THE SAME WAY AND SO HAVE THE SAME SMALL SIGNAL MODEL. Q_2 SEES A RESISTANCE LOOKING OUT OF ITS BASE WHICH IS EQUAL TO THE RESISTANCE LOOKING INTO Q_1'S EMITTER. WE CAN USE A SIMPLER SMALL SIGNAL MODEL FOR:





SUMMING CURRENTS AT THE EMITTER:

$$i_E + \beta_2 i_b + i_b = 0 \qquad (1)$$ 1

$$V_e = -i_b\left(r_{be_2} + R_S'\right) \qquad (2)$$ 1

FROM (1) $i_E + i_b(\beta_2 + 1) = 0 \qquad (3)$

BUT IF $\beta \gg 1 \quad (\beta_2 + 1) \approx \beta_2$

$$\therefore \quad i_E + \beta_2 i_b = 0 \qquad (4)$$ 1 (ASSUMPTION)

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SOLVE (2) FOR i_b,

$$i_b = \frac{-v_e}{r_{be_2} + R_s'} \qquad (5)$$

(5) → (4)

$$i_t + \frac{-v_e \beta_2}{r_{be_2} + R_s'} = 0 \qquad (6) \qquad 1$$

SOLVE FOR $r_o = v_e / i_t$

$$r_o = \frac{r_{be_2} + R_s'}{\beta_2} \qquad (7) \qquad 1$$

BUT $\frac{r_{be_2}}{\beta_2} = \frac{1}{g_{m2}}$ $\left(\because r_{be} = \beta / g_m \right)$

$$\therefore r_o = \frac{1}{g_{m2}} + \frac{R_s'}{\beta_2} \qquad (8) \qquad 1$$

R_s' IS THE TOTAL RESISTANCE LOOKING FROM Q_2'S BASE INTO Q_1'S EMITTER AND R_s IS THE TOTAL RESISTANCE LOOKING FROM Q_1'S BASE BACK TOWARDS THE VAS. THEREFORE:

$$r_o = \frac{1}{g_{m2}} + \frac{\frac{1}{g_{m1}} + \frac{R_s}{\beta_1}}{\beta_2} \qquad (9) \qquad 1$$

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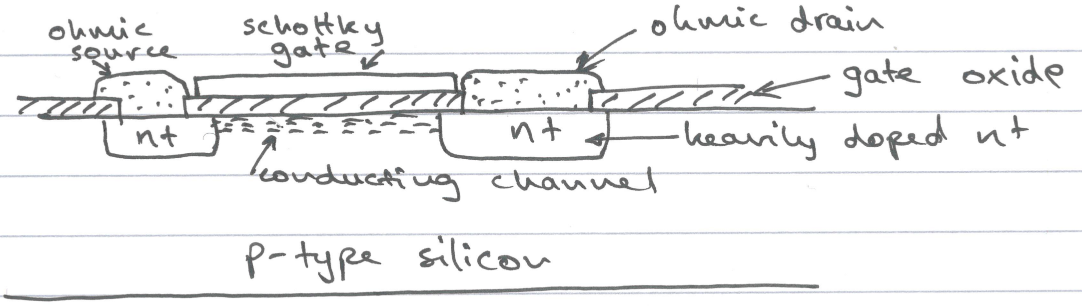
Q1 Q7



3

Initially, at low $+V_g$, holes are repelled under gate and a depletion forms. At higher $+V_g$, electrons from the n^+ regions are attracted to the region under the gate oxide and a conducting channel forms. 3

As the V_g changes, so does the charge under the gate oxide, and so I_{ds} will change. A small change in V_g can therefore cause a large change in I_{ds} when it is in the saturation region. 2

Q2 Q8 Given $\dfrac{dI_d}{dV_d} = \dfrac{\mu_e C_g}{l^2}\left[V_g - V_T - V_d\right]$,

to get I_d we integrate the above, getting

(i) $$I_d = \frac{\mu_e C_g}{l^2}\left[V_g - V_T - \frac{V_d}{2}\right]V_d$$ 3

(ii) Saturation occurs when $\dfrac{dI_d}{dV_d} = 0$, $\therefore$ $V_g - V_T - V_d = 0$

so V_d for saturation $= V_g - V_T$

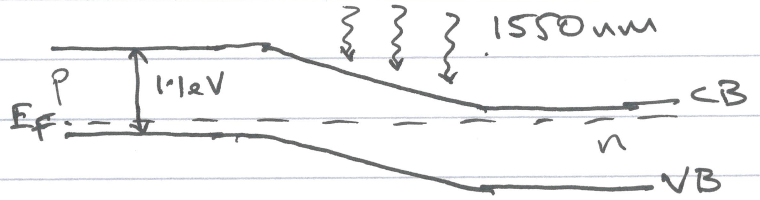
To get the saturation current I_{ds}, substitute above into expression for I_d, so:

$$I_{ds} = \frac{\mu_e C_g}{l^2}\left[V_d - \frac{V_d}{2}\right]V_d = \frac{\mu_e C_g}{l^2}\frac{V_d^2}{2}$$ 3

~~Q 2 (iii)~~ Q8 (ii) Transconductance, $g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d}$ in saturation region

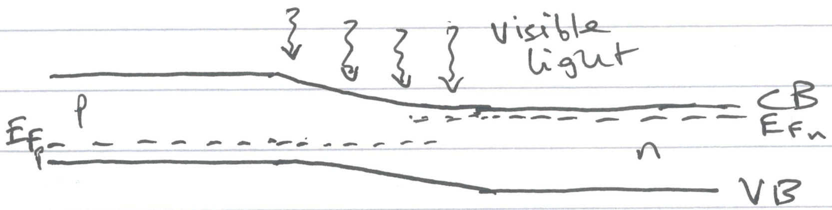
$\therefore\ g_m = \frac{\mu_e C_g V_d}{\ell^2}$ 2

~~Q 3~~ Q9



3

1550 nm light ≡ 0.8eV, so will not create e-h pairs in silicon. The p-n junction is therefore not perturbed from its equilibrium state

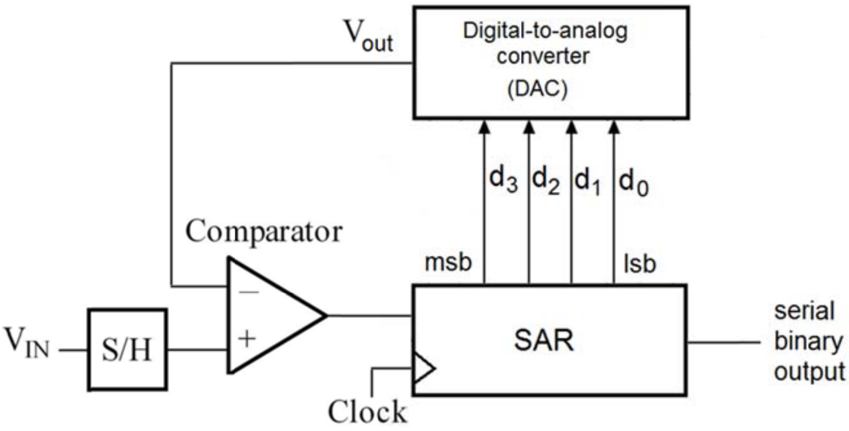


3

Visible light is > 1·1eV so will create e-h pairs in silicon. Minority electrons move to the n-type and minority holes move to the p-type, causing the bands to move and to reduce the built-in voltage.

Voltage with 1550 nm light = 0
Voltage with visible light ≈ 0·4 - 0·6 V_{bi} 2

10.a.



(3)

Starting with the msb, each input to the DAC is set to a '1' one at a time in decreasing order of significance. For each setting, the DAC produces an output V_{out} which is compared with the input voltage $V_{in.}$ If $V_{out} > V_{in}$ the comparator will give a high output and the set bit in the register is retained. When all bits have been tried, the conversion is complete. **(3)**

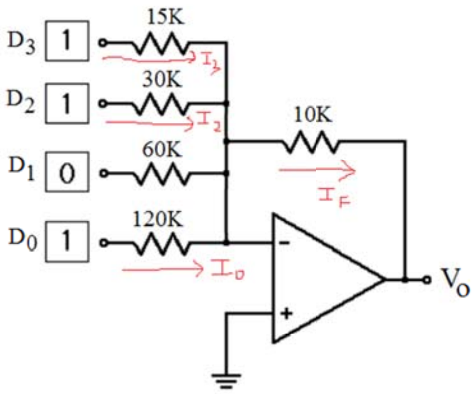
Step1, set SAR to 1000 11.7 is less than 16 so reset bit
Step2, set SAR to 0100 11.7 is greater than 8 so keep bit
Step3, set SAR to 0110 11.7 is less than 12 so reset bit
Step4, set SAR to 0101 11.7 is greater than 10 so keep bit

Hence 0101 = 10V is the approximation of 25.9V **(4)**

10.b.

(i) The resistor network has values that are inversely proportional to the binary weightings of the inputs. There is practically no current flowing into the inverting input of the op-amp which is a virtual ground (0V). Thus, the sum of the input currents will flow through the op-amp feedback resistor and hence the output voltage will be proportional to the sum of the binary weights. **(3)**

(ii)



Virtual earth at inverting input, hence

$I_0 + I_2 + I_3 = I_F$ **(1)**

$3.0\,(1/120K + 1/30K + 1/15K) = -V_0 / 10K$

$3.0\,(10/120 + 10/30 + 10/15) = -V_0$ **(1)**

$V_0 = -3.25V$ **(1)**

(iii)

The disadvantage of this method is the number of different resistor values required. For say, a 12 bit converter, 12 resistors in the range R to 2048R would be required. Tolerance required would be 1 part in 4095 (0.0244%). **(3)** It is difficult to mass produce these resistors within the required tolerance. **(1)**

Q11.a.

i. THE OUTPUT VOLTAGE HAS CONTRIBUTIONS FROM FOUR SOURCES. THE MEAN SQUARED CONTRIBUTIONS ARE:

$$\overline{V_{o(v_n)}^2} = \overline{V_n^2}\left(\frac{R_2}{R_1+R_2}\right)^2 = 25\times10^{-18}\times\left(\frac{3}{4.5}\right)^2$$ 1 (EQN)

$$= \frac{25\times4}{9}\times10^{-18}\ V^2 Hz^{-1}$$ 1

$$\overline{V_{o(i_n)}^2} = \overline{i_n^2}\left(R_1 // R_2\right)^2 = 9\times10^{-24}\times\left(10^3\right)^2$$ 1 (EQN)

$$= 9\times10^{-18}\ V^2 Hz^{-1}$$ 1

$$\overline{V_{o(R_1)}^2} = 4kTR_1\left(\frac{R_2}{R_1+R_2}\right)^2 = 2.484\times10^{-17}$$ 1 (EQN)

$$\times\frac{4}{9} = 11.04\times10^{-18}\ V^2 Hz^{-1}$$ 1

$$\overline{V_{o(R_2)}^2} = 4kTR\left(\frac{R_1}{R_1+R_2}\right)^2 = 49.68\times10^{-18}$$ 1 (EQN)

$$\times\frac{1}{9} = 5.52\times10^{-18}\ V^2 Hz^{-1}$$ 1

THE TOTAL OUTPUT NOISE POWER,

$$= \left(11.11 + 9 + 11.04 + 5.52\right)\times10^{-18}\ V^2 Hz^{-1}$$

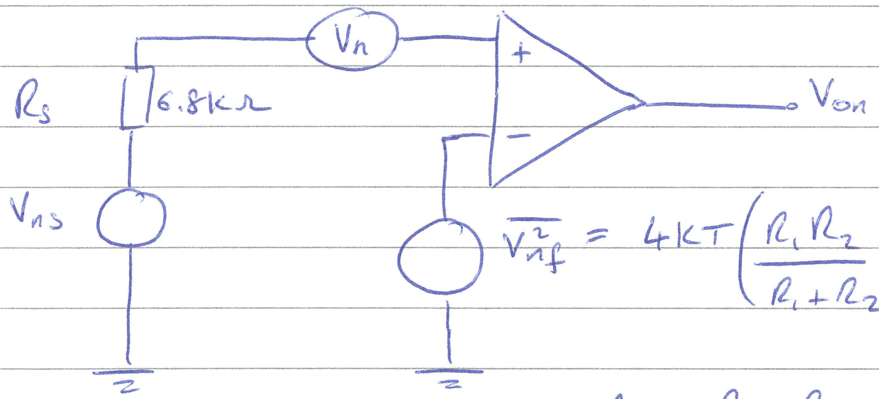
$= 36.67 \times 10^{-18}\ V^2 Hz^{-1}$

OR $V_{on} = V_{nTH} = \sqrt{36.67}\ nV/\sqrt{Hz}$

$= 6.06\ nV/\sqrt{Hz}$ 1

$R_{TH} = R_1 // R_2 = 1k\Omega$ BY INSPECTION 1

Q11b. THE NOISE EQUIVALENT CIRCUIT IS



$\overline{V_{nf}^2} = 4KT\left(\frac{R_1 R_2}{R_1 + R_2}\right)$

$A = \frac{R_1 + R_2}{R_1}$

11b ii $\overline{V_{on}^2} = A^2 \overline{V_n^2} + A^2 \overline{V_{ns}^2} + A^2 \overline{V_{nf}^2}$ 1

IF $\overline{V_{nf}^2}$ MUST BE LESS THAN OR EQUAL TO 10% OF $\overline{V_n^2}$ THEN $4KT\left(\frac{R_1 R_2}{R_1 + R_2}\right) = 0.1\ \overline{V_n^2}$ 2

THIS PROVIDES THE UPPER LIMIT TO $R_1 // R_2$

i.e. $R_1 // R_2 = \frac{0.1 \times (15 \times 10^{-9})^2}{4KT} = \underline{1.36\ k\Omega}$ 1

IF $\frac{R_1 R_2}{R_1 + R_2} = 1.36\,k\Omega$ AND $\frac{R_1}{R_1 + R_2} = 1/20$

$R_2 = 20 \times 1.36\,k\Omega = \underline{\underline{27.2\,k\Omega}}$ 1

$R_1 = \frac{R_2}{19} = \underline{\underline{1.43\,k\Omega}}$ 1

11 b iii $\overline{V_{on}^2} = A^2 \left[\overline{V_n^2} + \overline{V_{ns}^2} + \overline{V_{nt}^2} \right]$ 1

$= A^2 \left[\overline{V_{ns}^2} + 1.1\,\overline{V_n^2} \right]$ 1

$= 400 \left[4kT\ 6.8\,k\Omega + 247.5 \times 10^{-18} \right]$

$= 400 \left[112.6 \times 10^{-18} + 247.5 \times 10^{-18} \right]$

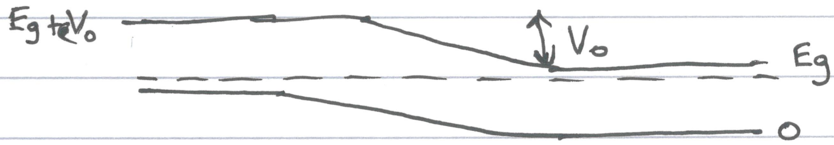
$= 144 \times 10^{-15}\ V^2 Hz^{-1}$ 1

TOTAL RMS OUTPUT NOISE VOLTAGE OVER 1 ~~0~~ KHz ;

$V_{o(RMS)} = \sqrt{\overline{V_{on}^2} \times BW}^{\,1} = \sqrt{144 \times 10^{-11}}$

$= \underline{\underline{37.9\,\mu V_{RMS}}}$ 1

Q4 : i) Let n_n = electrons in CB of n-type
Q12
n_p = electrons in CB of p-type



No. of electrons in CB of n-type, $n_n \propto P(E_g)$

$$n_n \propto \frac{1}{1+\exp\left[\frac{E_g-E_F}{kT}\right]} \propto \exp -\left(\frac{E_g-E_F}{kT}\right)$$

Similarly, no. of electrons in CB of p-type, $n_p \propto P(E_g+eV_o)$

$$n_p \propto \frac{1}{1+\exp\left(\frac{E_g+eV_o-E_F}{kT}\right)} \propto \exp - \left(\frac{E_g+eV_o-E_F}{kT}\right)$$

$$\frac{n_n}{n_p} = \exp\left(\frac{eV_o}{kT}\right)$$

$$\therefore \quad V_o = \frac{kT}{e} \ln\left(\frac{n_n}{n_p}\right).$$ 5

ii) Since $np = n_i^2$ and $n_n \simeq N_d$ and $p_p \simeq N_a$, we can write the above as:

$$V_o = \frac{kT}{e} \ln\left(\frac{N_d N_a}{n_i^2}\right)$$

$p = N_a = 2\times10^{16}\ cm^{-3}$, $n_i = 10^{10}\ cm^{-3}$
$n = n_i^2/p = 10^{20}/(2\times10^{16}) = 5\times10^{3}\ cm^{-3}$

n-doped region $= N_d - N_a = 10^{17} - 2\times10^{16} = 8\times10^{16}\ cm^{-3}$
You can use either expression to calculate V_o:
(Note: As $|N_d-N_a| \gg n_i$, no compensation doping to worry about)

Q4:
Q12

$$V_0 = \frac{KT}{e} \ln\left(\frac{8\times10^{16}}{5\times10^{3}}\right) = 0.0259 \ln(1.6\times10^{13}) = 0.787V$$

6

iii) When Temp increases to 450K, Na and Nd will not change, but n_i will increase rapidly. Consequently the V_0 value will decrease, significantly. 3

iv) 1mW of 633nm.

Energy of single photon of 633nm $= \frac{hc}{\lambda} = \frac{1.24}{0.633}$

$= 1.95eV$ or 3.1×10^{-19} J

$1mW = 10^{-3}$ J/sec, no. of photons is

$$\frac{10^{-3}}{3.1\times10^{-19}} = 3.2\times10^{15} \text{ photons/sec.}$$

As energy of 633nm photon $= 1.95eV$ is $> E_g$ of silicon, each photon creates e-h pairs.

The current that flows will therefore be equal to 3.2×10^{15} electrons/sec $= 3.2\times10^{15}\times1.6\times10^{-19} = 0.51mA$

6