Examination Feedback for EEE6042– Integrated Circuit Technology
Autumn Semester 2011-12

Feedback for EEE6042 Session: 2011-2012

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

A much better performance this year- good grasp of resistivity, growth techniques, general awareness of semiconductors and CMOS process!

Question 1:

Need to emphasize more the first two lectures particularly crystal structure and representation.

Question 2:

Marks were lost in calculations, good grasp of CVD, some student confused CVD with MOCVD.

Question 3:

This question included basic CMOS process flow, contact technology and lift off. Two candidates did not do this question so well, but by and large, there were good answers from the majority who did

Question 4:

Most did not do well in terms of listing failure mechanisms, the question about the metal tracks, although simple was not completed by students at the calculation phase and most did well on the MBE/MOCVD.