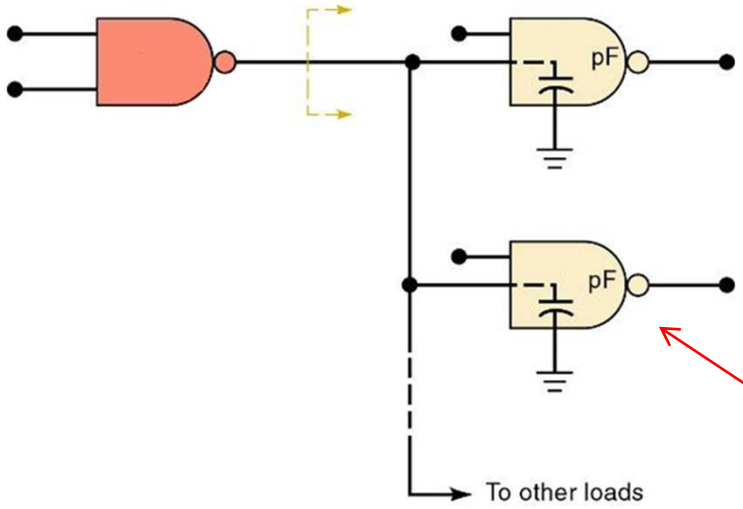
CMOS Characteristics (II)

- Fan-out
- Resistive Loads
- Driving LEDs
- TTL CMOS Interfacing

Fan-Out

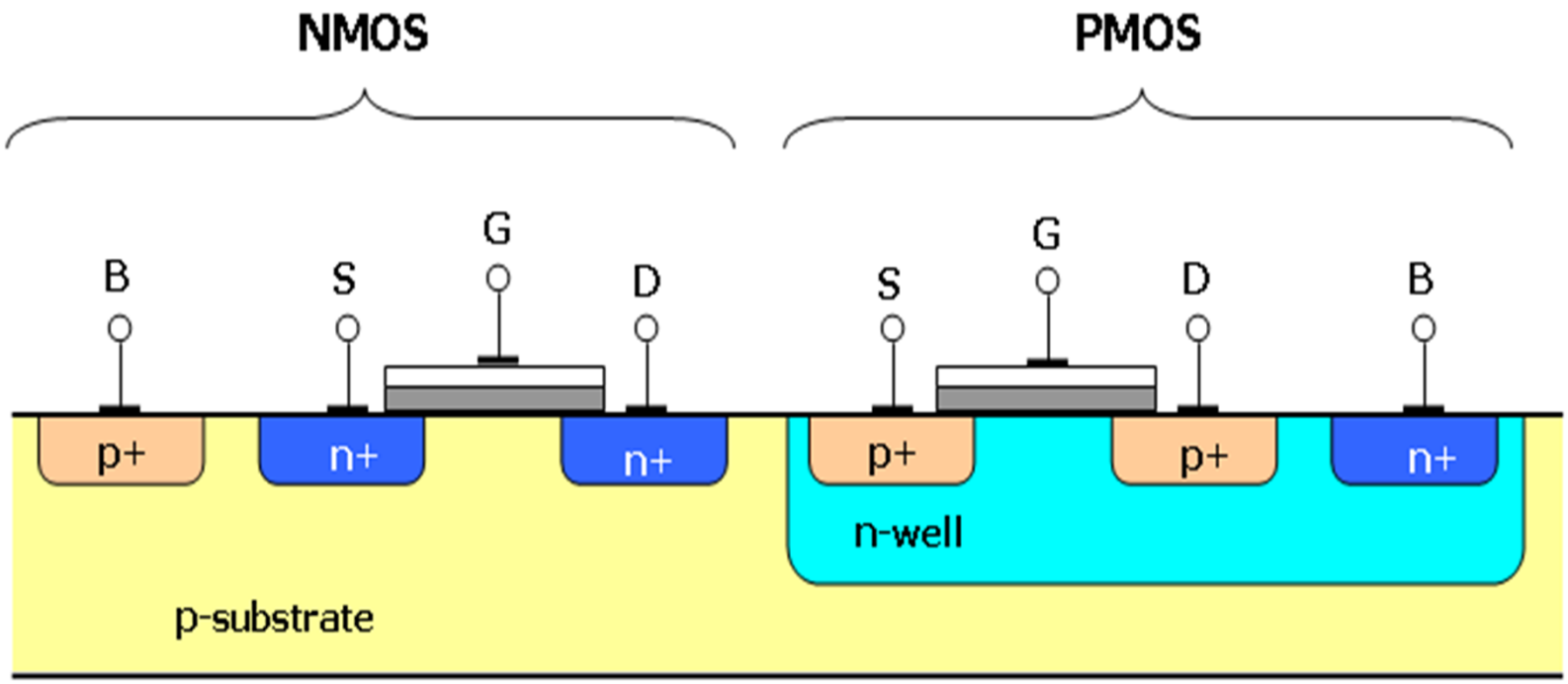
Fan-out specifies the number of standard loads that can be connected to the output of a logic gate without degrading its normal operation.
(standard load = input to a gate of same family)



A CMOS gate has very high input impedance due to the gate insulating material. They consume a very small amount of current.

Typical 5V CMOS values

I_{IL} - maximum current that flows into the input in the LOW state ( )
I_{IH} - maximum current that flows into the input in the HIGH state ( )


NMOS
PMOS
B
S
G
D
S
G
D
B
p+
n+
n+
p+
p+
n+
n-well
p-substrate

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:

Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

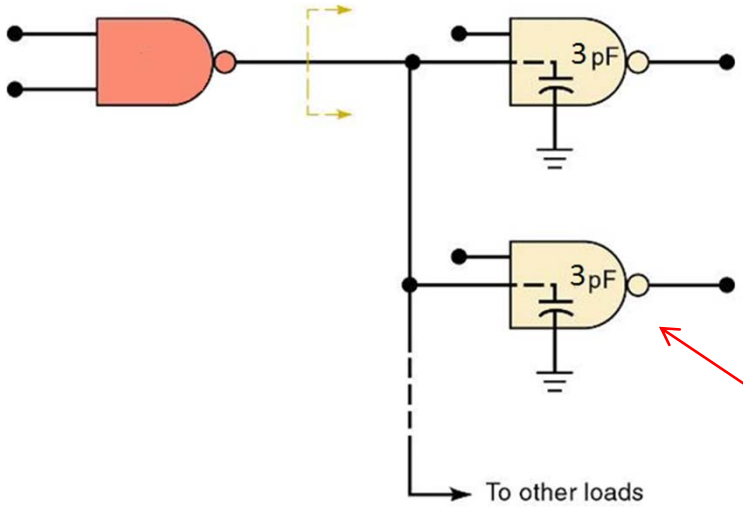
Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	–1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	–0.7	–1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ µA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	$I_{OL} = 20$ µA	—	.001	0.1	V
			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	µA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

Fan-Out

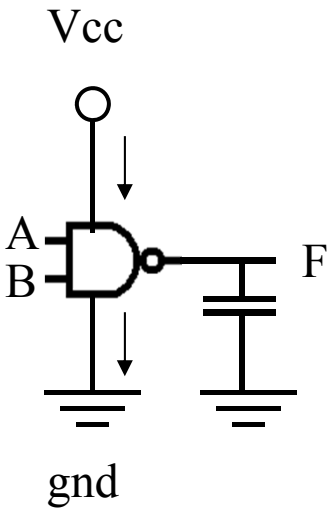
Fan-out specifies the number of standard loads that can be connected to the output of a logic gate without degrading its normal operation.
(standard load = input to a gate of same family)

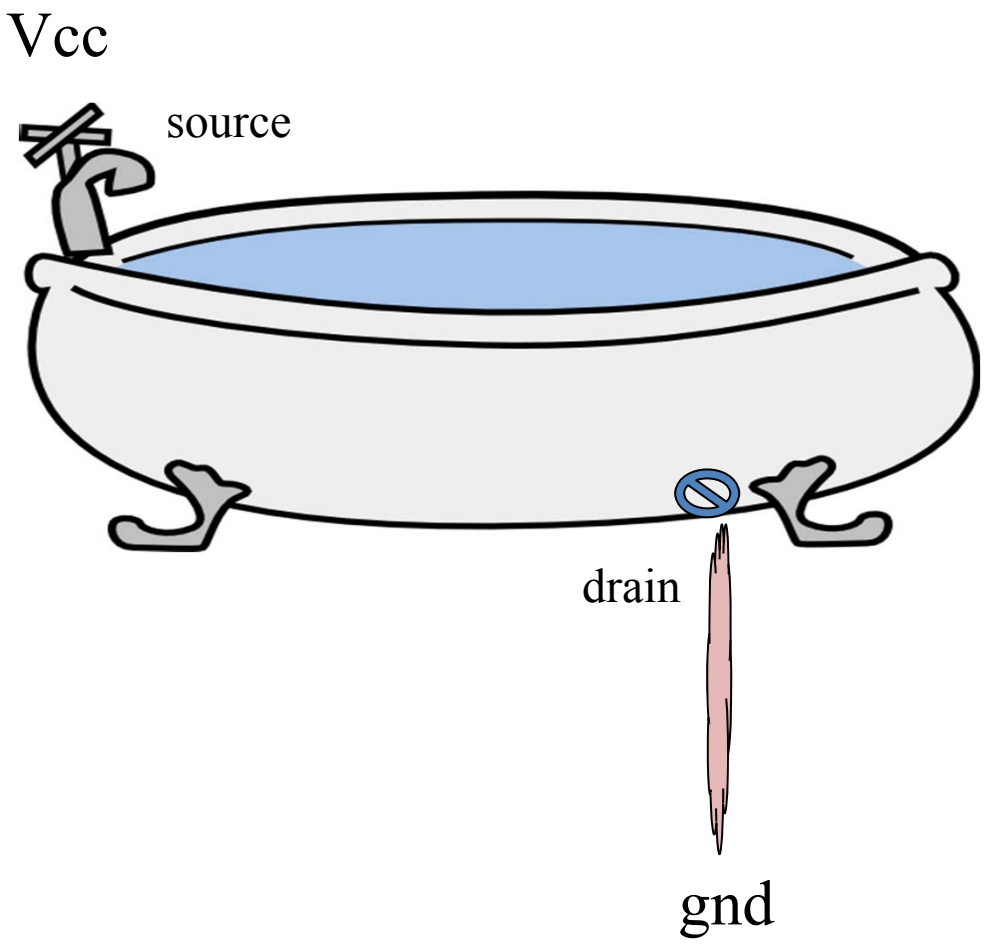


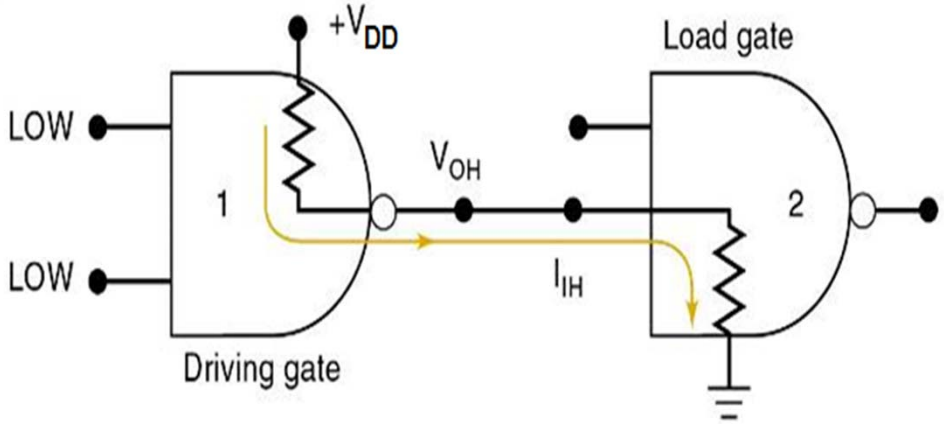
A CMOS gate has very high input impedance due to the gate insulating material. They consume a very small amount of current.

Typical 5V CMOS values

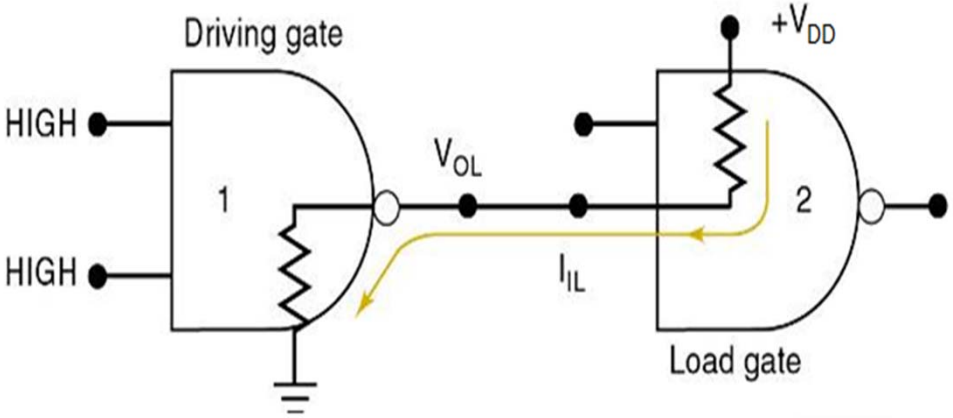
I_{IL} - maximum current that flows into the input in the LOW state -1μA
I_{IH} - maximum current that flows into the input in the HIGH state 1μA


Vcc
A
B
F
gnd


Vcc
source
drain
gnd



When the driving gate output is HIGH, it acts as a source of current to the load gate. The driving gate must be able to source current I_{IH}.



When the driving gate output is LOW, it sinks current from the load gate. The driving gate must be able to sink current I_{IL}.

TI data sheets specify currents flowing out of a device as negative.

- When calculating the fan-out, both the ‘sourcing’ and ‘sinking’ cases must be considered.
- The fan-out is the minimum of these two cases.

$$\text{Fan-out} = \min \left(I_{OHmax} / I_{IH} , I_{OLmax} / I_{IL} \right)$$

Typical fan-out for 5V CMOS :

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V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	µA
I_{IL}	Input LOW current	V_{CC} = Max., $V_I = 0$ V		—	—	–1	µA
V_{IK}	Clamp diode voltage	V_{CC} = Min., $I_N = -18$ mA		—	–0.7	–1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	$I_{OH} = -20$ µA	4.4	4.499	—	V
			$I_{OH} = -4$ mA	3.84	4.3	—	V
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			$I_{OL} = 4$ mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, $I_O = 0$		—	2	10	µA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

- When calculating the fan-out, both the ‘sourcing’ and ‘sinking’ cases must be considered.
- The fan-out is the minimum of these two cases.

$$\text{Fan-out} = \min\left(I_{OHmax} / I_{IH} , I_{OLmax} / I_{IL} \right)$$

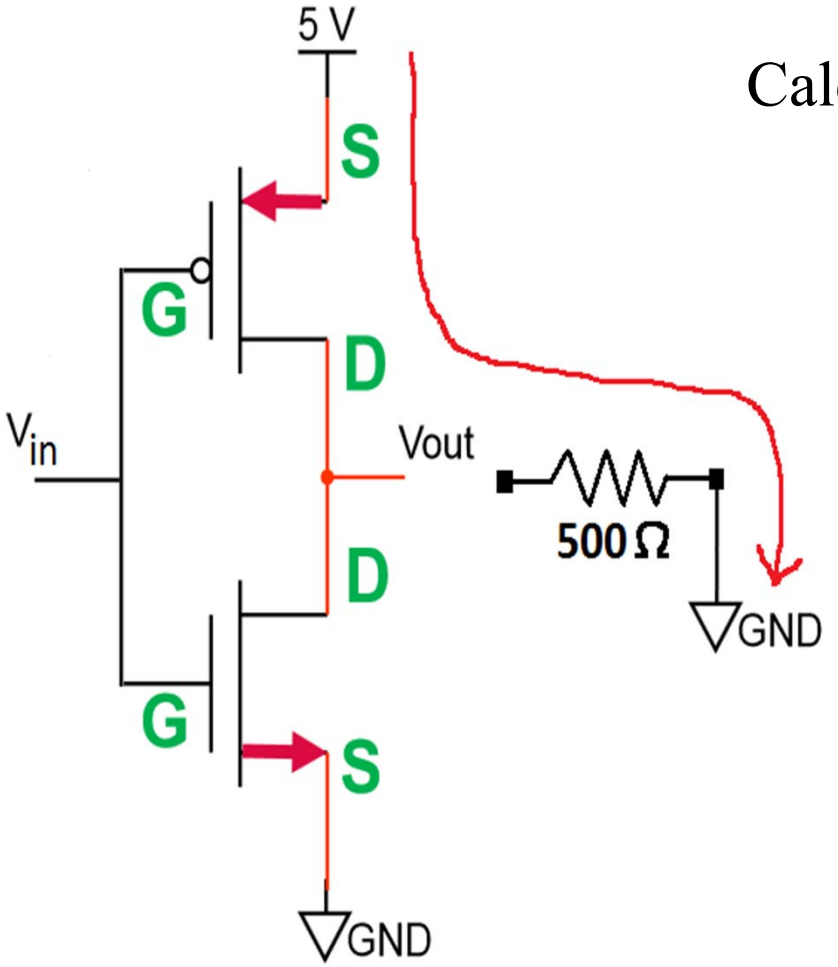
Typical fan-out for 5V CMOS : $20\mu A / 1\mu A = 20$

However, capacitive loading may be more of a problem as it limits the frequency of operation.

Resistive Loads

- CMOS loads require very little current for a HIGH or LOW on their inputs (typically microamps).
- Resistive or ‘DC’ loads require significantly more current (typically milliamps).
- Manufacturers usually supply two sets of loading specifications for the two conditions.

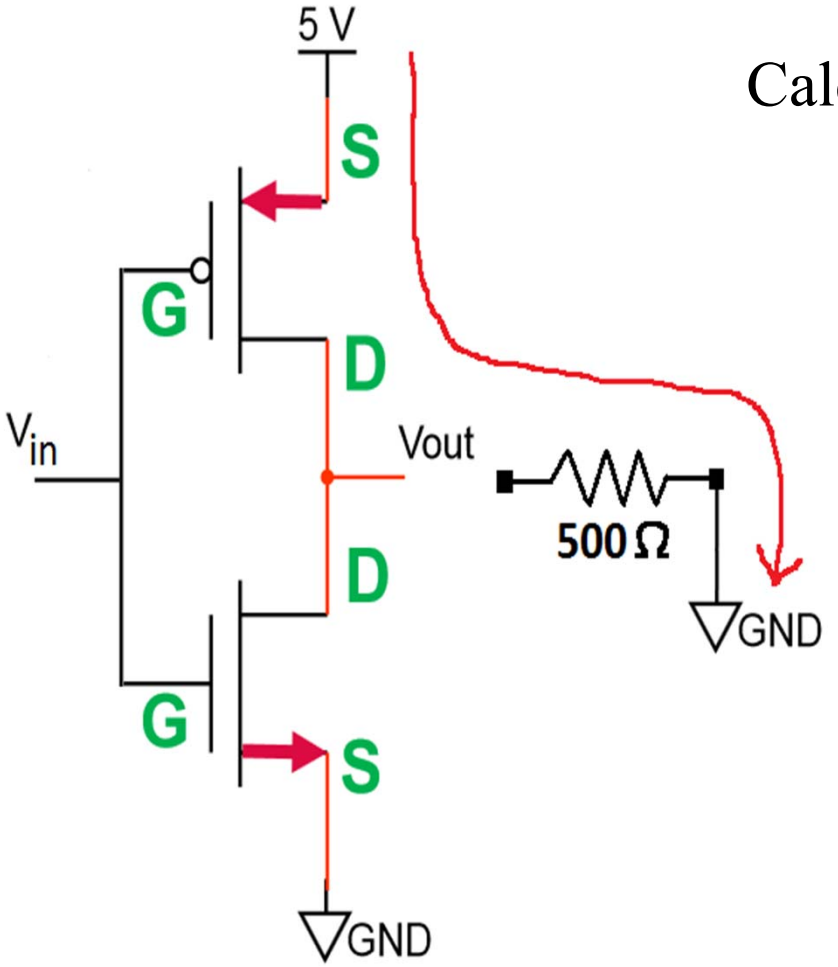
Inverter - Current Sourcing



Calculate V_{OH} and I_{OH} for a LOW input.

PMOS 'on' R_{DS} = 75 Ω , 'off' R_{DS} = 500,000 Ω
NMOS 'on' R_{DS} = 25 Ω , 'off' R_{DS} = 500,000 Ω

Inverter - Current Sourcing



Calculate V_{OH} and I_{OH} for a LOW input.

Load impedance is 500,000 Ω
in parallel with 500 Ω ≈ 500 Ω

$V_{OH} \approx 5 \times (500 / 575)$
$\approx 4.35V$

$I_{OH} \approx 5 / (75 + 500)$
$\approx 8.7mA$

PMOS 'on' R_{DS} = 75 Ω , 'off' R_{DS} = 500,000 Ω
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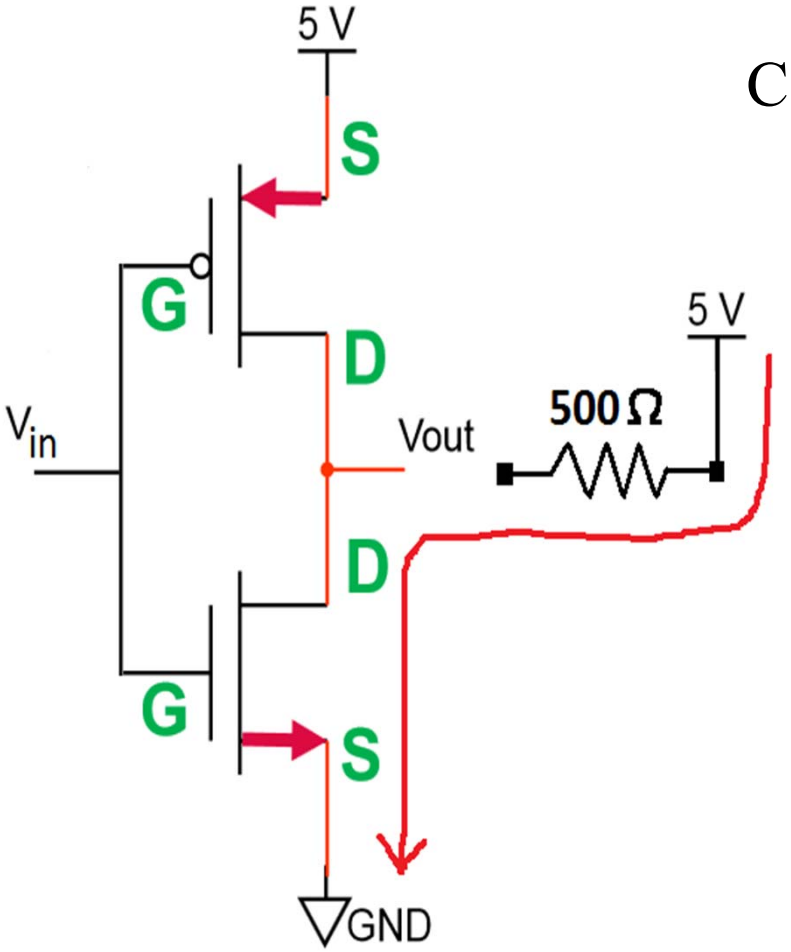
Inverter - Current Sinking



Calculate V_{OL} and I_{OL} for a HIGH input.

PMOS 'on' R_{DS} = 75 Ω , 'off' R_{DS} = 500,000 Ω
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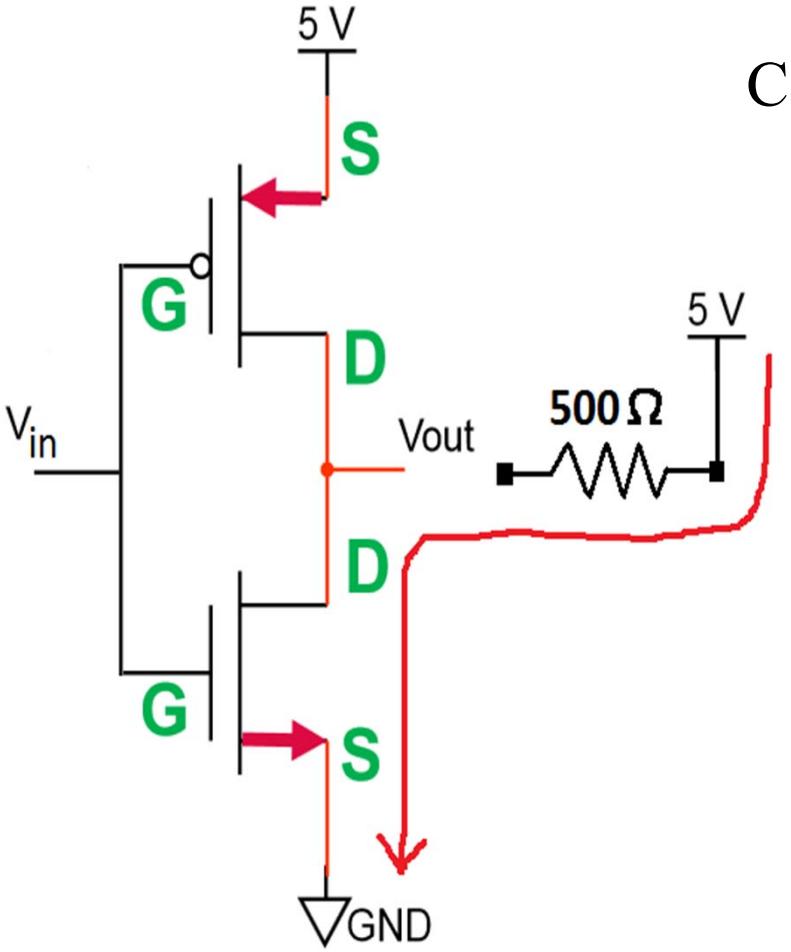
Inverter - Current Sinking



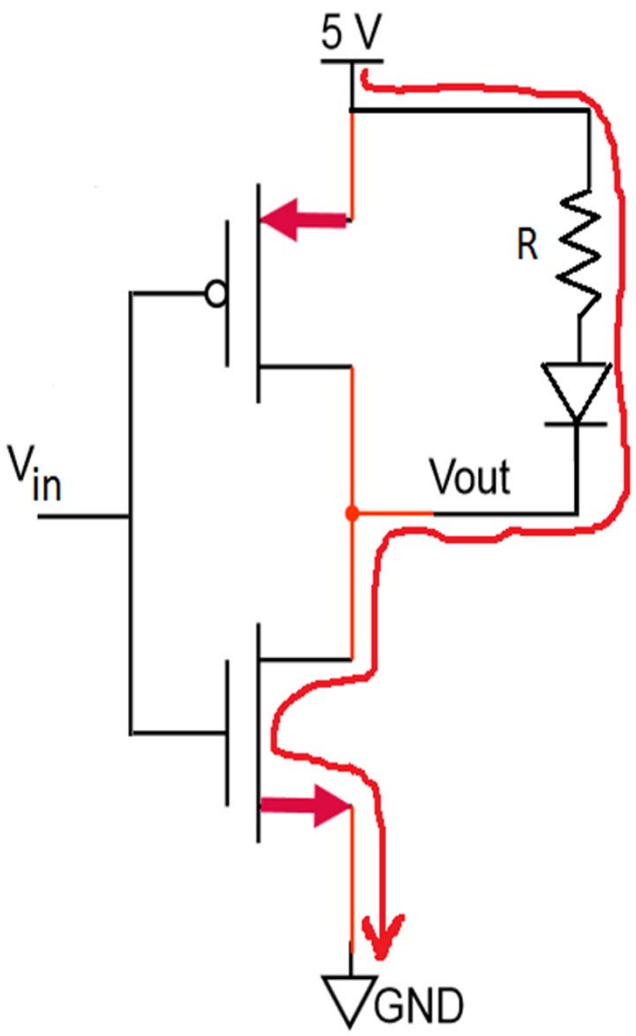
Calculate V_{OH} and I_{OH} for a HIGH input.

$V_{OL} \approx 5 \times (25 / 525)$
$\approx 0.24V$

$I_{OL} \approx 5 / (25 + 500)$
$\approx 9.5mA$

PMOS 'on' $R_{DS} = 75\ \Omega$, 'off' $R_{DS} = 500{,}000\ \Omega$
NMOS 'on' $R_{DS} = 25\ \Omega$, 'off' $R_{DS} = 500{,}000\ \Omega$

Driving LEDs – Current Sinking



Calculate the value of the LED current limiting resistor for the worst case current sinking configuration.

Calculate the power dissipated by the current limiting resistor.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

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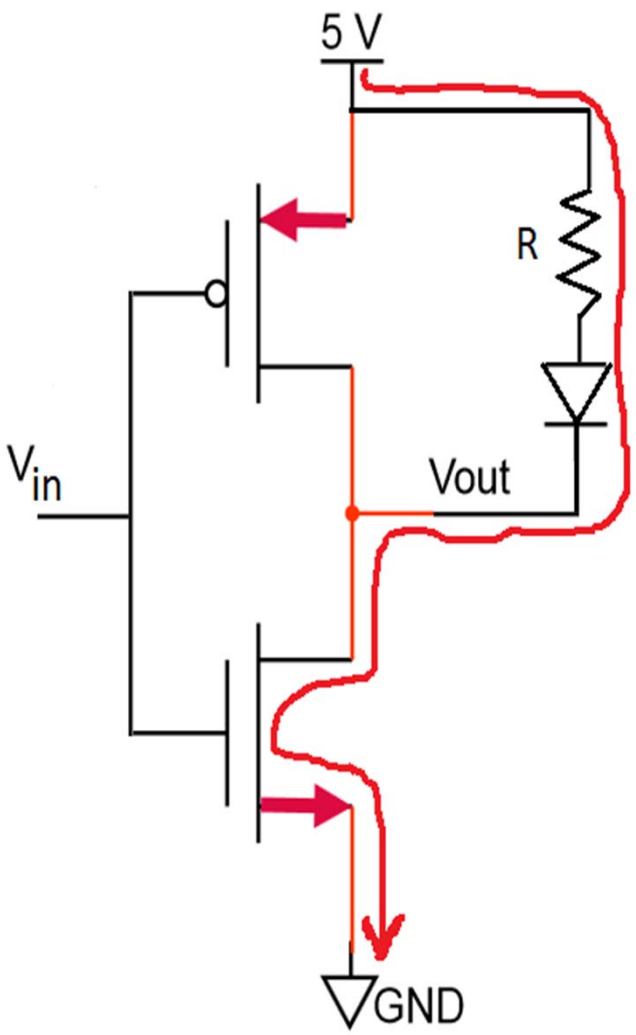
SWITCHING CHARACTERISTICS OVER OPERATING RANGE, $C_L = 50$ pF

Sym.	Parameter[4]	Test Conditions	Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y	—	9	19	ns
C_I	Input capacitance	$V_{IN} = 0$ V	—	3	10	pF
C_{pd}	Power dissipation capacitance per gate	No load	—	22	—	pF

Driving LEDs – Current Sinking



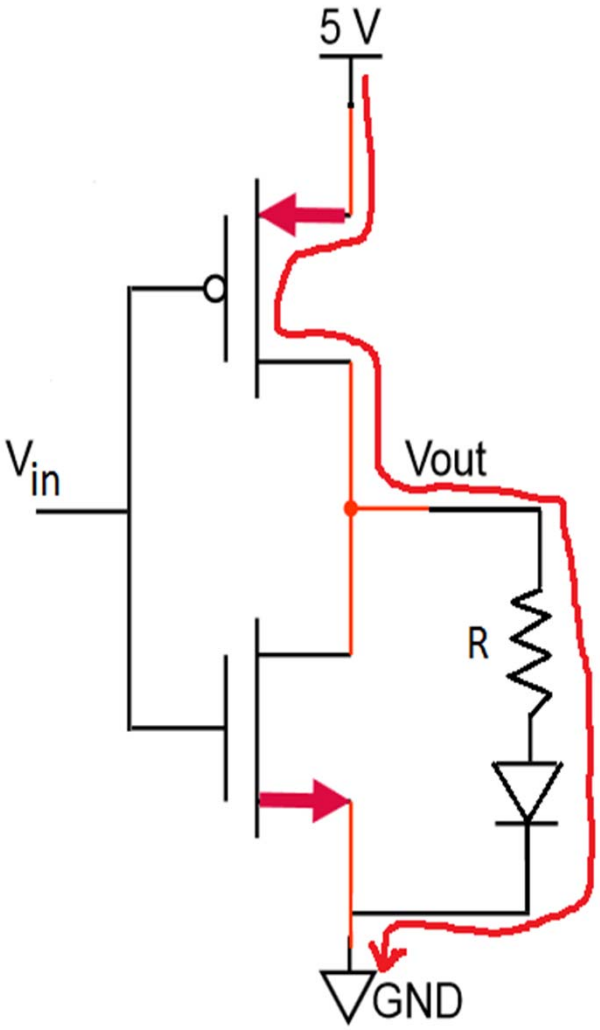
Calculate the value of the LED current limiting resistor for the worst case current sinking configuration.

$$V_R = 5.0 - V_{LED} - V_{OL}$$
$$= 5.0 - 1.9 - 0.33$$
$$= 2.77V$$

$$R = V_R / I_{OL}$$
$$= 2.77 / 0.004 = 693\ \Omega$$

$$P_R = R \times I_{OL}^2$$
$$= 693 \times (0.004)^2 = 11.1mW$$

Driving LEDs – Current Sourcing



Calculate the value of the LED current limiting resistor for the worst case current sourcing configuration.

Calculate the power dissipated by the current limiting resistor.

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I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	–35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = –20 µA	4.4	4.499	—	V
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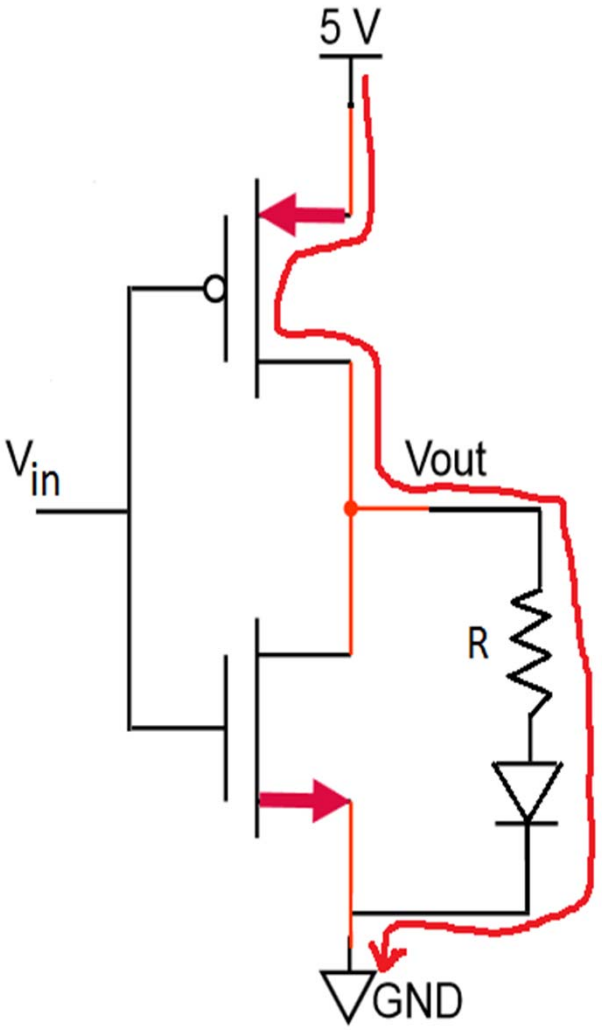
SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions	Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y	—	9	19	ns
C_I	Input capacitance	V_{IN} = 0 V	—	3	10	pF
C_{pd}	Power dissipation capacitance per gate	No load	—	22	—	pF

Driving LEDs – Current Sourcing



Calculate the value of the LED current limiting resistor for the worst case current sourcing configuration.

$$V_R = V_{OH} - V_{LED}$$
$$= 3.84 - 1.9$$
$$= 1.94V$$

$$R = V_R / I_{OH}$$
$$= 1.94 / 0.004 = 485\ \Omega$$

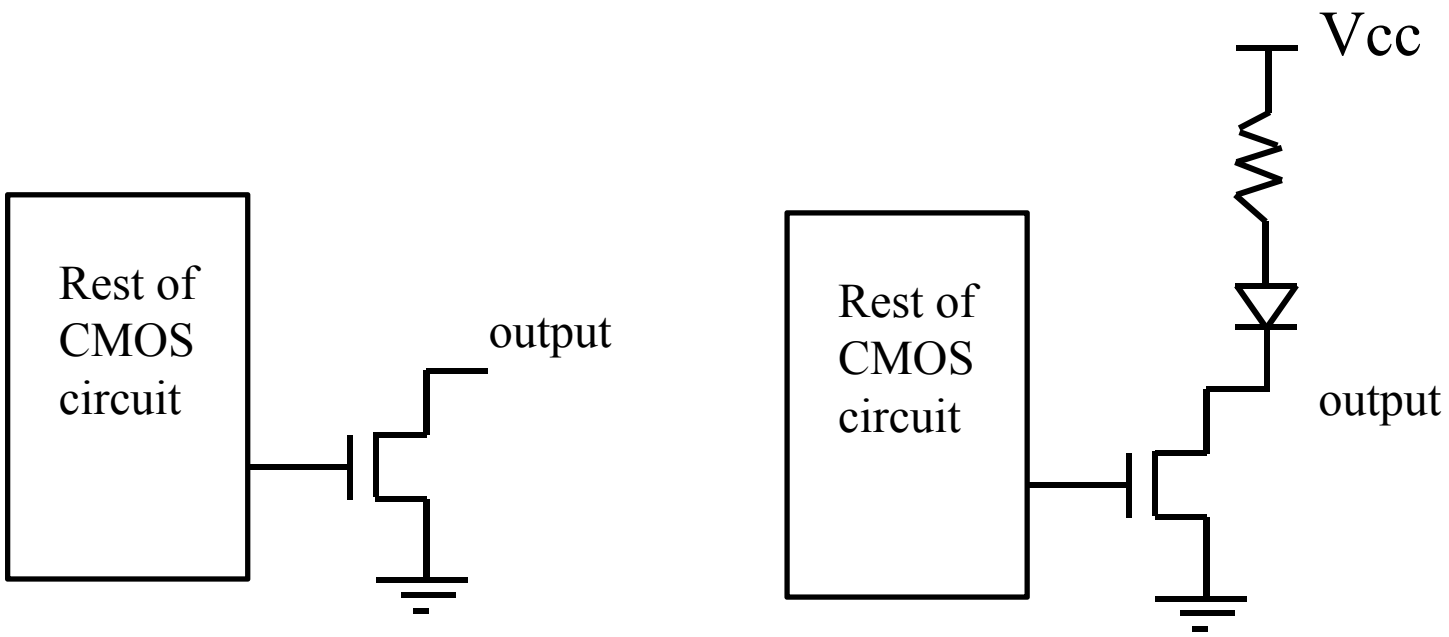
$$P_R = R \times I_{OH}^2$$
$$= 485 \times (0.004)^2 = 7.8mW$$

Effects of Excessive Loading

- Output voltage levels may be violated
- Rise and fall times may increase
- Temperature of the device may increase

Driving LEDs – Open Drain

A typical LED may require current in the range 10mA to 50mA which may be beyond the capability of a standard CMOS device.



If the driving gate does not have sufficient drive capability, it may be necessary to use an open drain device (see later).

CMOS TTL Interfacing

There are some practical considerations when mixing technologies.

1. Are the logic levels compatible?
2. Can the output stage provide sufficient current to drive?

This information must be checked from the data sheets.

CMOS outputs can generally drive TTL devices.

TTL outputs cannot generally drive CMOS devices directly as voltage levels are violated. It is necessary to use CMOS devices with TTL compatible inputs designated by T (HCT, ACT etc). Alternatively, it may be possible to adjust the logic levels using a pull-up resistor at the input to the CMOS device.