Data Provided:

List of constants, materials data and useful equations at end of paper

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (2.0 hours)

EEE6040 High Speed Electronic Devices

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Sketch cross-sections through a typical MESFET device under the following bias conditions. Indicate the different semiconductor types and metal contacts used and the position of the depletion region in all cases.

(i) $V_G=V_D=0$
(ii) $V_G+V_D=V_P$

where V_G is the gate-source voltage, V_D is the drain source voltage and V_P is the pinch off voltage

As V_G+V_D increases further above V_P the drain current drops to a stable low, but finite value. What is happening to the channel in this case?

A further large increase in V_G+V_D results in a large and unstable increase in the drain current. Describe the mechanism that is responsible for this behaviour.

(5)

b. Describe the main differences between the MOSFET and the MESFET in terms of the:

(i) Device structure
(ii) Operating principles and mode
(iii) Mobility of carriers in the conducting channel
(iv) Manufacturing issues

Why is the MOSFET dominant in digital applications?

Why might the MESFET device be favourable compared to the MOSFET in certain high-performance applications?

(6)

c. An n-channel enhancement mode silicon MOSFET exhibits a drain current of 50μA at a gate voltage (V_G) of 1.0V and a drain voltage (V_D) of 0.4V. Predict the **(5)**

drain current for the same drain voltage at (i) V_G=2.0V and (ii) V_G=4.0V.

You may assume the MOSFET has a gate length 500nm, a gate width of 200μm and gate capacitance per unit area of $2x10^{-6}F.m^{-2}$

d. Draw energy band diagrams to describe the following bias conditions an n-channel enhancement mode MOSFET.

(i) $V_G = V_D = 0$
(ii) $V_G > V_T > > V_D$

where V_G is the gate voltage, V_D the drain voltage and V_T the threshold voltage.

Indicate the position of the conduction and valence bands, the intrinsic and Fermi levels and the position of any conducting channel **(4)**

2. a. Discuss how the following technological developments have contributed to, or may contribute to, the extension of Moore's law in CMOS devices

(i) Advances in Lithography
(ii) High-k dielectrics
(iii) Strained channels
(iv) Use of III-V semiconductor channels

Developments along these lines are seen as 'more Moore'. What is meant by the alternative phrase 'more than Moore' when applied to future developments? List two possible approaches which would come under this heading.

(10)

b. Draw typical output and transfer characteristics for both n-channel enhancement and depletion mode MOSFETs. Your output characteristics should have several curves to indicate the variation with V_G. Mark on the transfer characteristics the threshold voltage V_T.

Why is the enhancement mode device is generally preferred for digital applications?

(5)

c. The transconductance of a MOSFET is given by $g_m = \frac{Z\mu C_{ox}}{L}\ [V_G - V_T]$

By equating the input and output current, derive an expression for the cut-off frequency of the MOSFET. Discuss which parameters are critical for high speed operation

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(5)

3 a. Transport through an *npn* bipolar transistor is characterised by an emitter-collector transit time $\tau_{EC.}$ List the components of τ_{EC} which relate to the transit through various regions of the device and describe their origin.

Give the expressions for these individual time components which relate to the collector current and the individual capacitances, resistances and region widths in the transistor.

Which of these components are capacitance related and which are resistance related? Describe how we could reduce these components through changes to the structure.

Use your expression to calculate the individual components and total $\tau_{EC.}$ Use this value to calculate the f_T value for the transistor

The transistor has the following measured parameters, where all symbols have their usual meaning:

C_{BE}=20pF, C_{BC}=15pF, r_e=0.3Ω, r_c=0.3Ω, w_b= 0.25μm, w_c= 0.6μm.

The following may be of assistance:

Capacitance charging time = $C\frac{dV}{dI}$ Depletion region transit time = $\frac{w^2}{2D_e}$

Transit time at high field $\frac{w}{2.v_{sat}}$

From Kirchoff's law $\Delta V_{BC} = \Delta V_{BE} + \Delta I_{C.}(R_e + R_c)$

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(12)

b. A CMOS foundry currently uses 1.2nm thickness of SiO_2 as the gate dielectric. The devices have a sub-threshold leakage current of 120nA at V_G=0.3V. The foundry wishes to change to HfO_2 to reduce gate leakage whilst keeping all of the other electrical characteristics constant. It is able to change the dielectric thickness, but no other device dimension.

What thickness of HfO_2 is required to achieve this?

The primary leakage mechanism is field-assisted electron tunnelling through the silicon/oxide barrier. The tunnelling current, I_{tn} , is known to follow the relationship

$$I_{tn} \propto \frac{\sqrt{m_{eff,ox}}}{\epsilon_{r,ox}\,\phi_b}.exp\left(-\mathrm{K}\phi_b^{3/2}/E\right)$$

where $m_{eff,ox}$ is the oxide electron effective mass, Φ_b is the silicon/oxide barrier height in eV (determined by the electron affinity), $\epsilon_{r,ox}$ is the relative permittivity of the oxide a E is the magnitude of the electric field across the oxide and K is a constant ≈ $1x10^8$.

Estimate the new value of the leakage current at V_G= 0.3V

(8)

4 **a.** Figure 1 shows the small signal equivalent circuit for a bipolar transistor

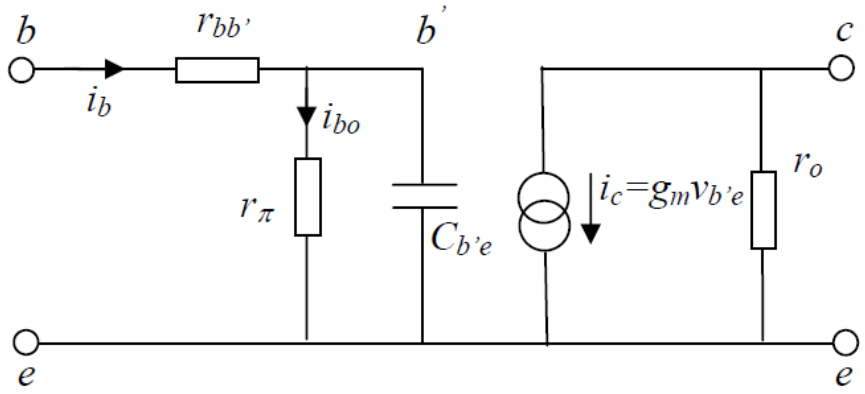

Figure 1: Small signal circuit diagram of a bipolar transistor

Describe the origin of each of the various resistance and capacitance components using diagrams and equations where necessary. How could we reduce the value of these components through design or through operational changes?

(6)

b. Which of the components in figure 1 is related to the 'Early' effect? Sketch typical output characteristics which show this effect and indicate on your diagram the Early voltage.

A bipolar transistor has a base doping of 10^{17} cm^{-3} and a base width of 0.2μm. Calculate the Early voltage give that the base-collector capacitance is 1 pF and the collector area is 10^{-4} cm^{-2}.

(4)

c. By consideration on the input and output currents and using figure 1, derive an expression for the small-signal circuit current gain, h_{fe}, as a function of the frequency. Simplify this to give expressions for the h_{fe} at (i) low frequency ($\omega \rightarrow 0$) and (ii) high frequency ($\omega \rightarrow \infty$).

At high frequency the gain reduces until it reaches a value of unity. Use this information to derive an expression for the cut-off frequency f_T. By consideration of this expression, state which parameters need to be improved to give high f_T values. How might we accomplish this?

(5)

d. Draw a simple (1D) schematic of the structure of a typical $Si/Si_{.5}Ge_{.5}$ HBT. Show the materials used and the doping type and doping concentration. Mark any interfaces which should be graded in composition.

Sketch an energy level diagram for the HBT under typical forward bias conditions. Show the conduction and valance bands, the Fermi level and the applied voltages.

Describe how this device represents an improvement over the basic BJT. How will the f_{max} and the transconductance be improved by these changes?

(5)

MH/ IR

USEFUL INFORMATION

Fundamental constants

Electronic charge, $q = 1.6\times10^{-19}$ C

Permittivity of free space, $\varepsilon_o = 8.85\times10^{-12}$ Fm^{-1}

Planck constant, $h = 6.63\times10^{34}$ Js

Boltzmann Constant, $k = 1.38x10^{-23} m^2 \cdot kg.s^{-2}K^{-1}$

Mass of electron $=9.1x10^{-31}$Kg

Materials Data

Saturation velocity, $v_{sat} = 1\times10^5$ ms^{-1} (Si), 2×10^5 ms^{-1} (GaAs)

Conduction band density of states, $N_c = 2.86\times10^{19}$ cm^{-3} (Si), 4.71×10^{17} cm^{-3} (GaAs)

Electron mobility at room temperature, $\mu_e = 0.15$ $m^2V^{-1}s^{-1}$ (Si)

Electron diffusion coefficient = $3.9x10^{-3}$ m^2.s (Si)

	Si	GaAs	Ge	$Si0_2$	$Hf0_2$
Band Gap (eV)	1.12	1.42	0.66	9.0	6.8
Relative Permittivity, ϵ_r	11.9	12.9	16.2	3.9	25
Electron Affinity, Φ (eV)	4.1	4.07	4.0	0.95	2.0
Effective mass, m* (m_o)	0.26	0.068	0.12	0.55	0.11

Useful Formulae (all symbols have their usual meaning)

NB: Not all the equations needed are presented here. You WILL have to remember or derive some basic formulae.

$$I_D = \frac{Z}{L}\mu_n C_o \left(V_G - V_T - \frac{V_D}{2}\right)$$

$$V_T = -|V_{FB}| + 2|V_B| + \frac{(2q\varepsilon_s N_A|2V_B|)^{1/2}}{C_{ox}}$$

$$|V_A| = \frac{qA_C N_B w_b}{C_{BC}}$$

$$V_n = \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right)$$

$$I_{Dsat} = \frac{Z\mu\varepsilon_s}{2aL}(V_G - V_T)^2$$

$$D_e = \frac{\mu_e kT}{q}$$

$$g_m = \frac{qa\mu N_D}{2L}$$