Combinational Logic Circuits (III)

- Decoders
- XOR Networks
- Parity Generators & Checkers

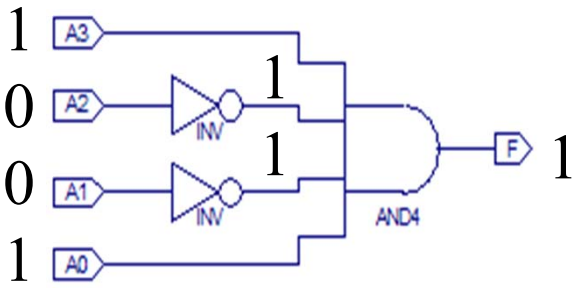
Decoders

A decoder is a device that can detect a specific combination of bits on its input. It indicates this on its output using a specified logic level.

Active high decoders put a **1** on the output.

Active low decoders put a **0** on the output.

Example: A circuit is required that will give an output of **1** when the binary pattern **1001** is present on its inputs.
An AND gate can be used as the decoding element because it gives out a 1 when its inputs are high. As all of the inputs must be high when 1001 is present, the middle two bits must be inverted.

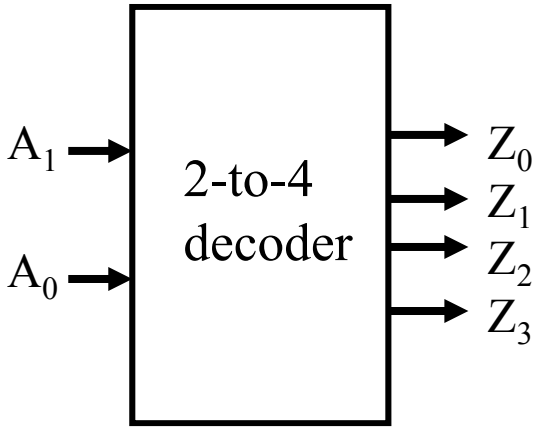


$$F = A_3\overline{A}_2\overline{A}_1A_0$$

Using a NAND gate in place of the AND gate will give an active low output.

Line/Address Decoders

The select bits are decoded to provide a desired output. Only one output signal is asserted at any time. In this case, it is active ‘high’.



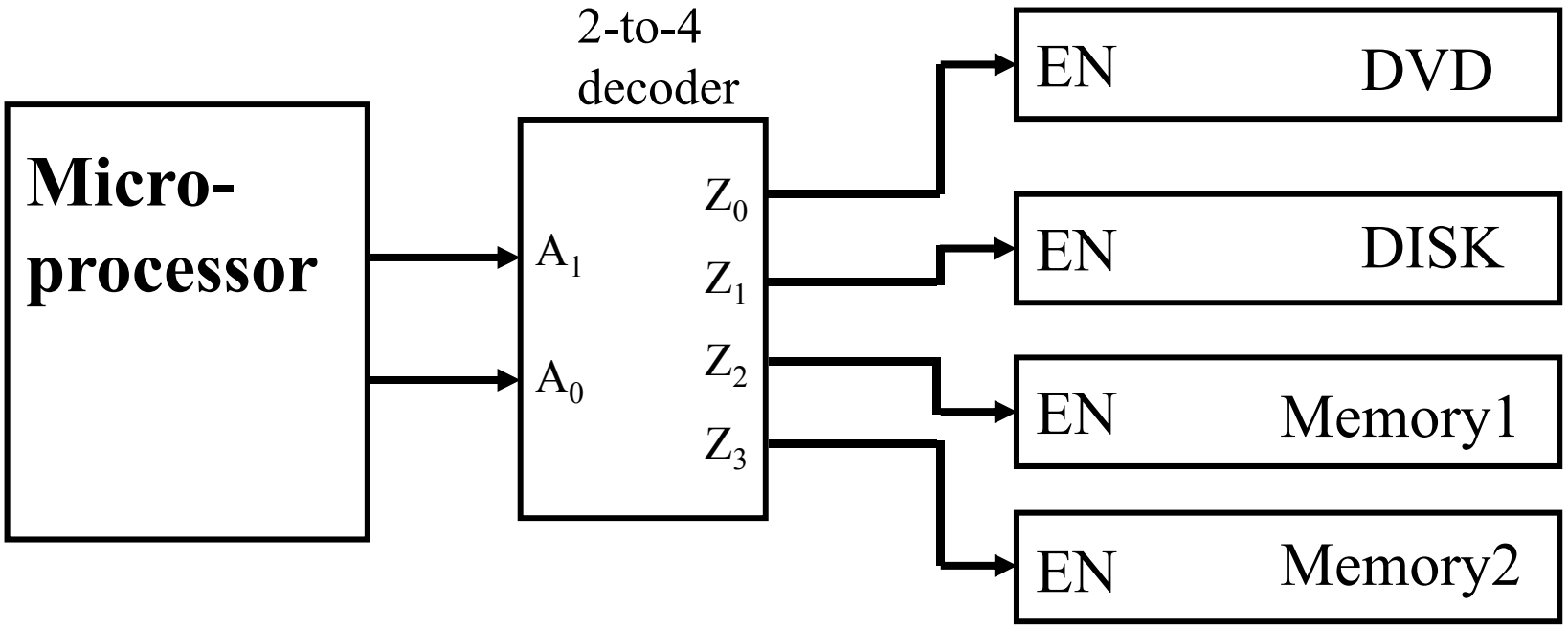
A_1	A_0	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

An AND gate is used to decode each of the possible combinations of the inputs. An n-input decoder has 2^n output lines.

Address Decoder Application

An address decoder can be used when a computer must select between several peripheral devices. The single active output can be used as an enable signal for the peripheral required.

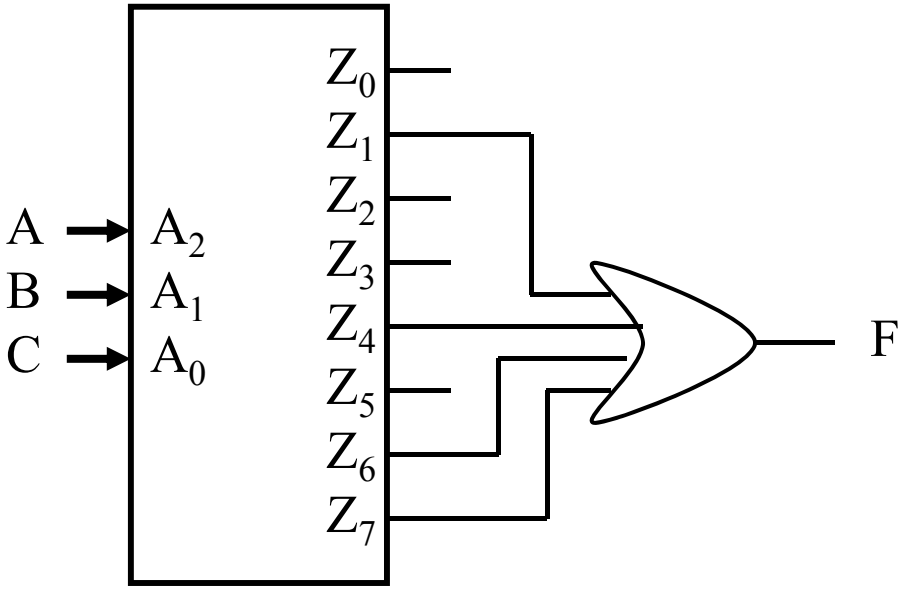
A_1	A_0	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



Implementing Logic Expressions

A decoder can also be used as a function generator. A canonical sum of products expression can be implemented by simply picking of the required minterms and OR'ing them together.

Example: Implement $F(A,B,C) = \Sigma\,(1,4,6,7)$ using a 3-to-8 address decoder with active high outputs and a single logic gate.

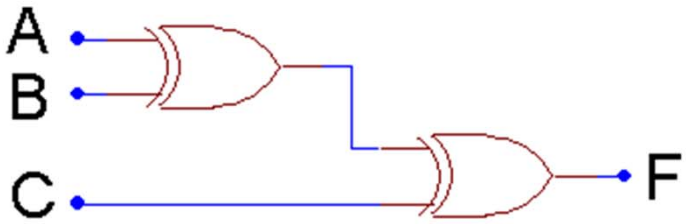


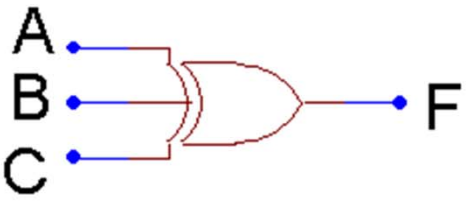
Using multiplexers and decoders to implement logic functions does not exploit minimisation but is useful in accommodating a regular fixed structure in a hardware device. (see later lectures)

Multiple Input Exclusive-OR Gates

Exclusive-OR is an “odd” function, it is equal to 1 if the input variables have an odd number of 1’s.

A B C	F
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1





XOR is commutative and associative.

$$(A \oplus B) \oplus C = A \oplus (B \oplus C) = A \oplus B \oplus C$$

Parity Method for Error Detection

When binary data is transferred between systems, errors can occur. This means that a transmitted ‘1’ may be received as a ‘0’, or a transmitted ‘0’ may be received as a ‘1’. A single bit in a group may be in error or multiple bits may be in error.

A simple way to check for a single bit in error is to add a parity bit. This is an extra bit in the message to make the number of 1s either even or odd.

Even number of 1s - **EVEN PARITY** scheme.

Odd number of 1s - **ODD PARITY** scheme.

This scheme can only tell us if a single bit is in error.

Parity Examples

Add a parity bit to give **EVEN** parity

_ 1010

_ 110011001

_ 0000000

_ 11001100101

Add a parity bit to give **ODD** parity

_ 1010

_ 110011001

_ 0000000

_ 11001100101

Parity Examples

Add a parity bit to give **EVEN** parity

0 1010

1 1110011001

0 00000000

0 11001100101

Add a parity bit to give **ODD** parity

1 1010

0 1110011001

1 00000000

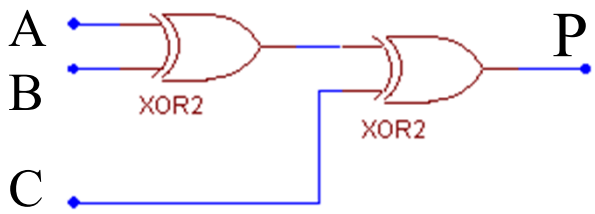
1 11001100101

Parity Generation and Checking

A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Consider a three bit message (A,B,C) to be transmitted with even parity. An extra bit P must be added to make the number of 1s even.

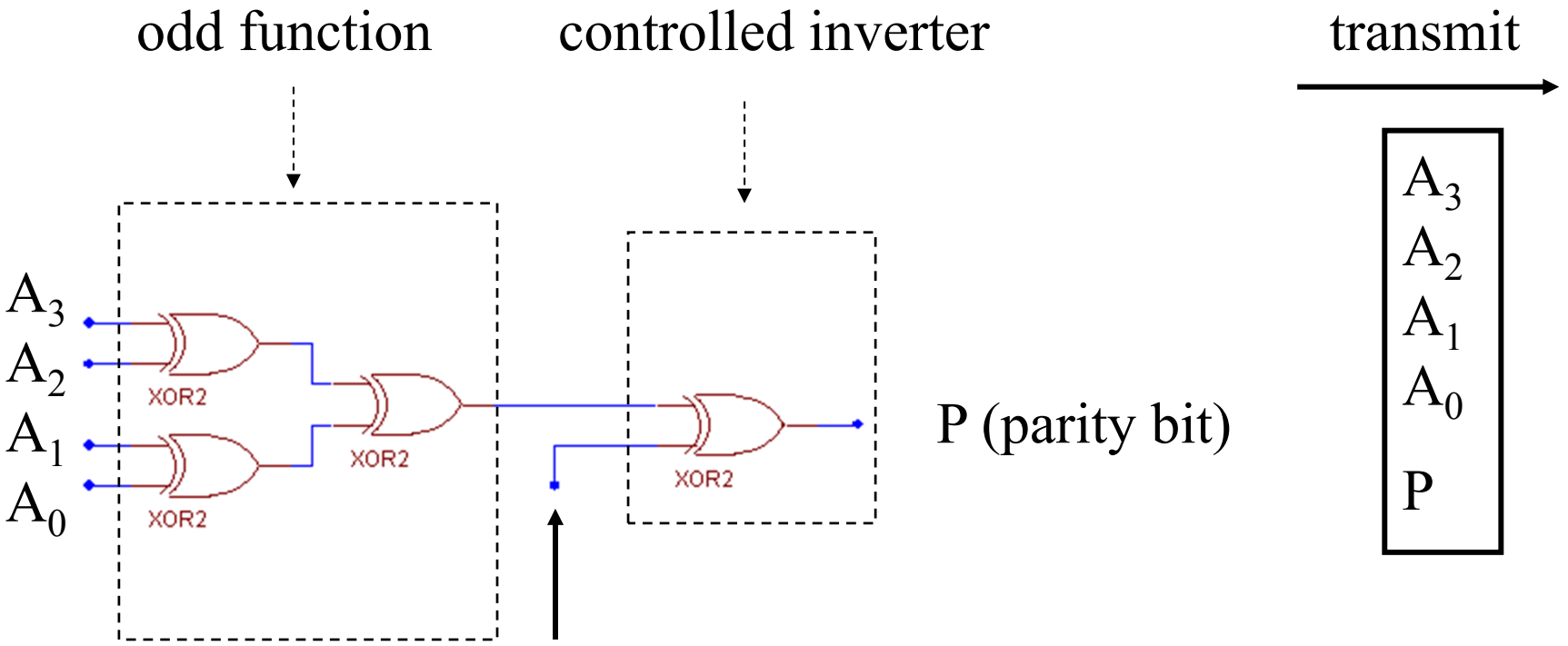
P is only a 1 when there is an odd number of 1s. This can be realised with a three variable exclusive-OR function.



If we require odd parity, P must be inverted. Using an additional XOR gate as a controlled inverter will enable selection between odd and even parity.

Parity Generator

Consider a four bit data word, $A_3A_2A_1A_0$.



0 passes data (for even parity scheme)
1 inverts data (for odd parity scheme)

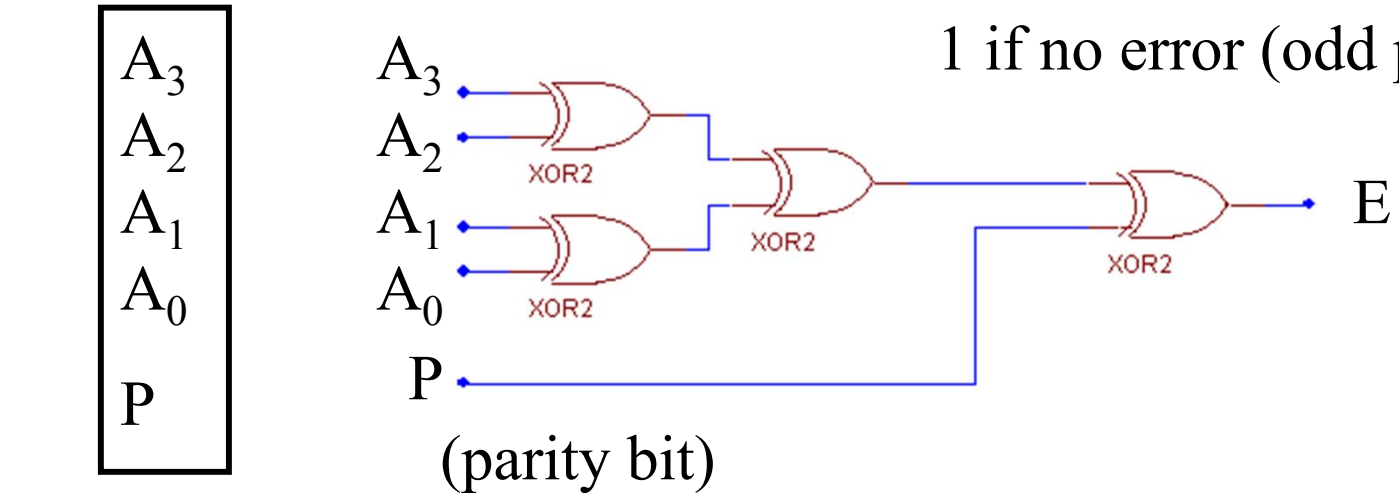
Parity checker

Error signal E

0 if no error (even parity scheme)

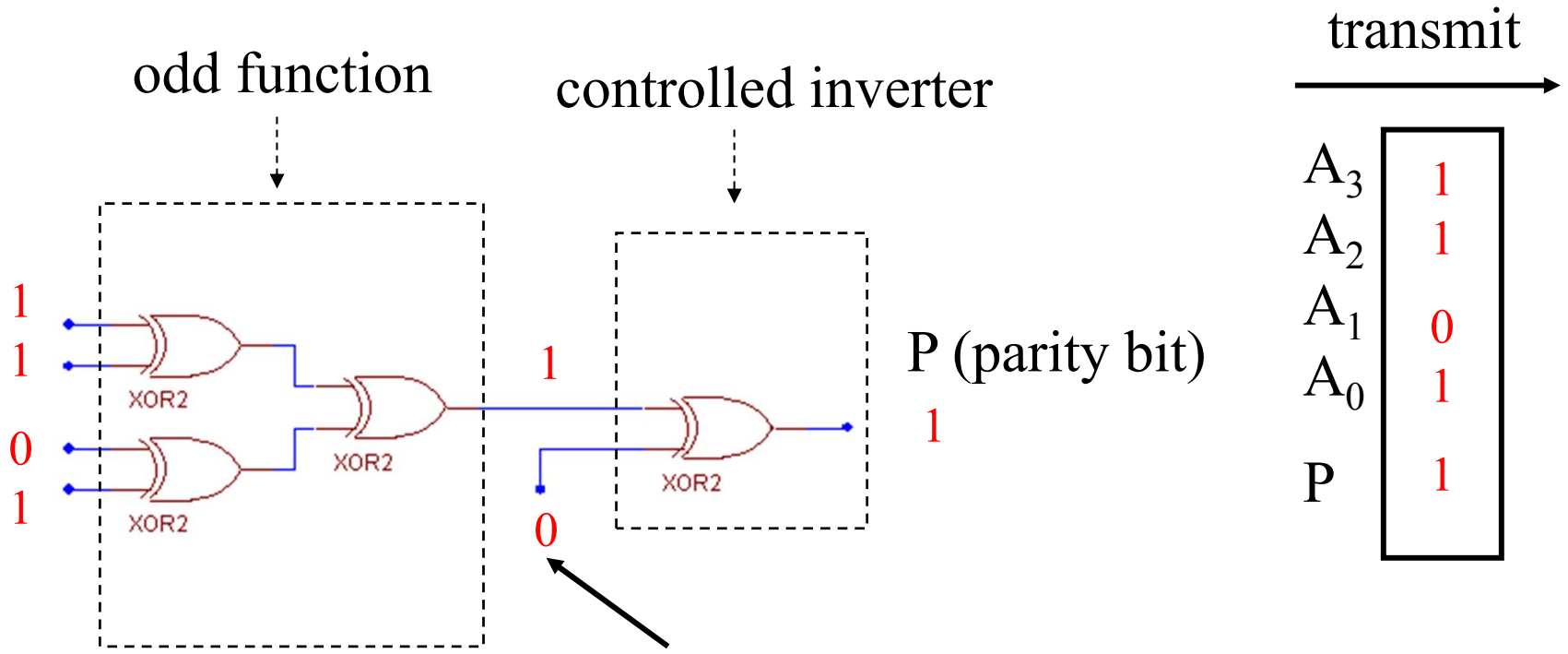
1 if no error (odd parity scheme)

receive



EVEN PARITY – transmit 1101

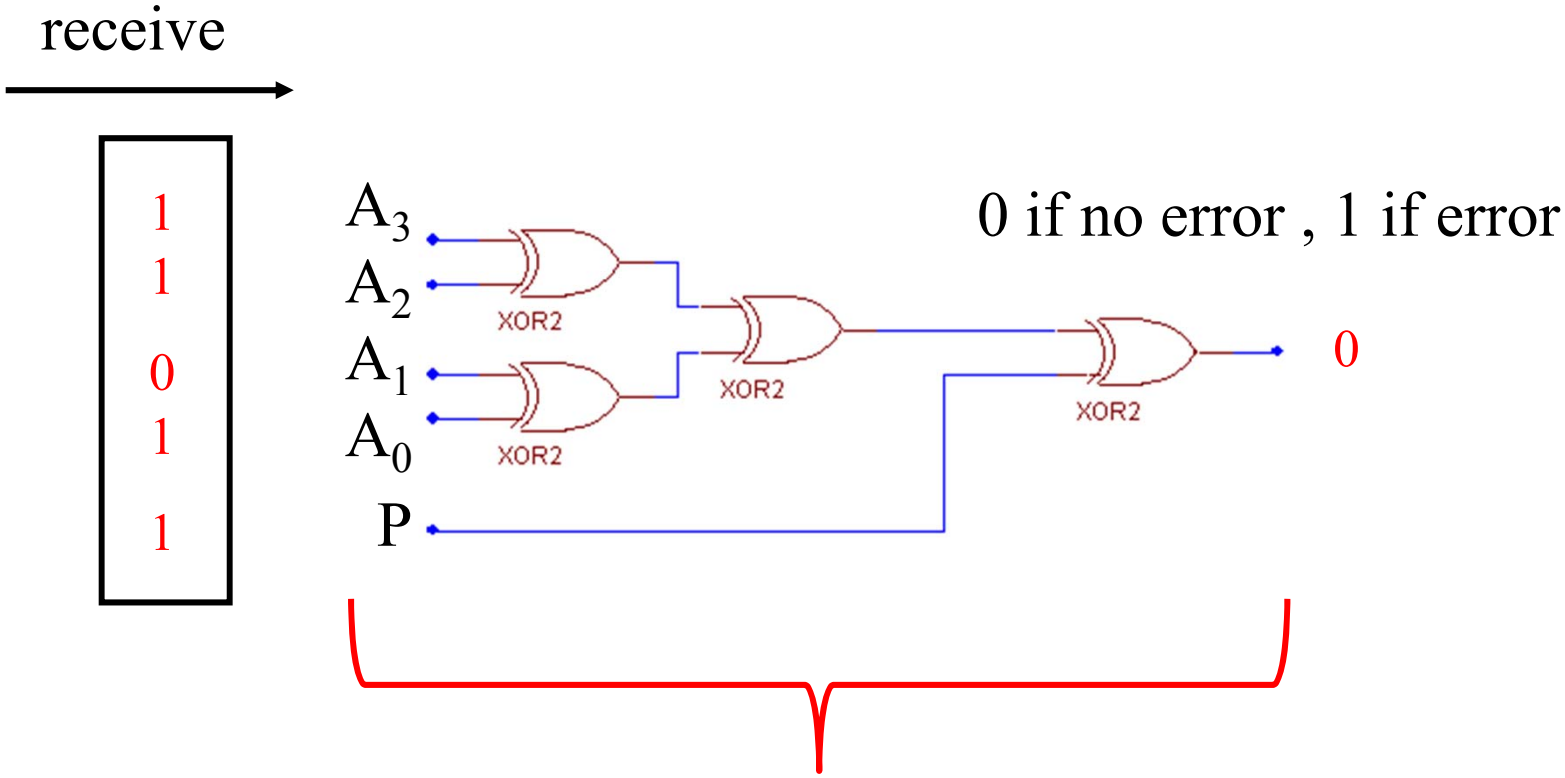
Consider transmitting $A_3A_2A_1A_0 = 1101$



Pass data straight through for even parity scheme. For an odd parity scheme this would be set to 1 to invert the data.

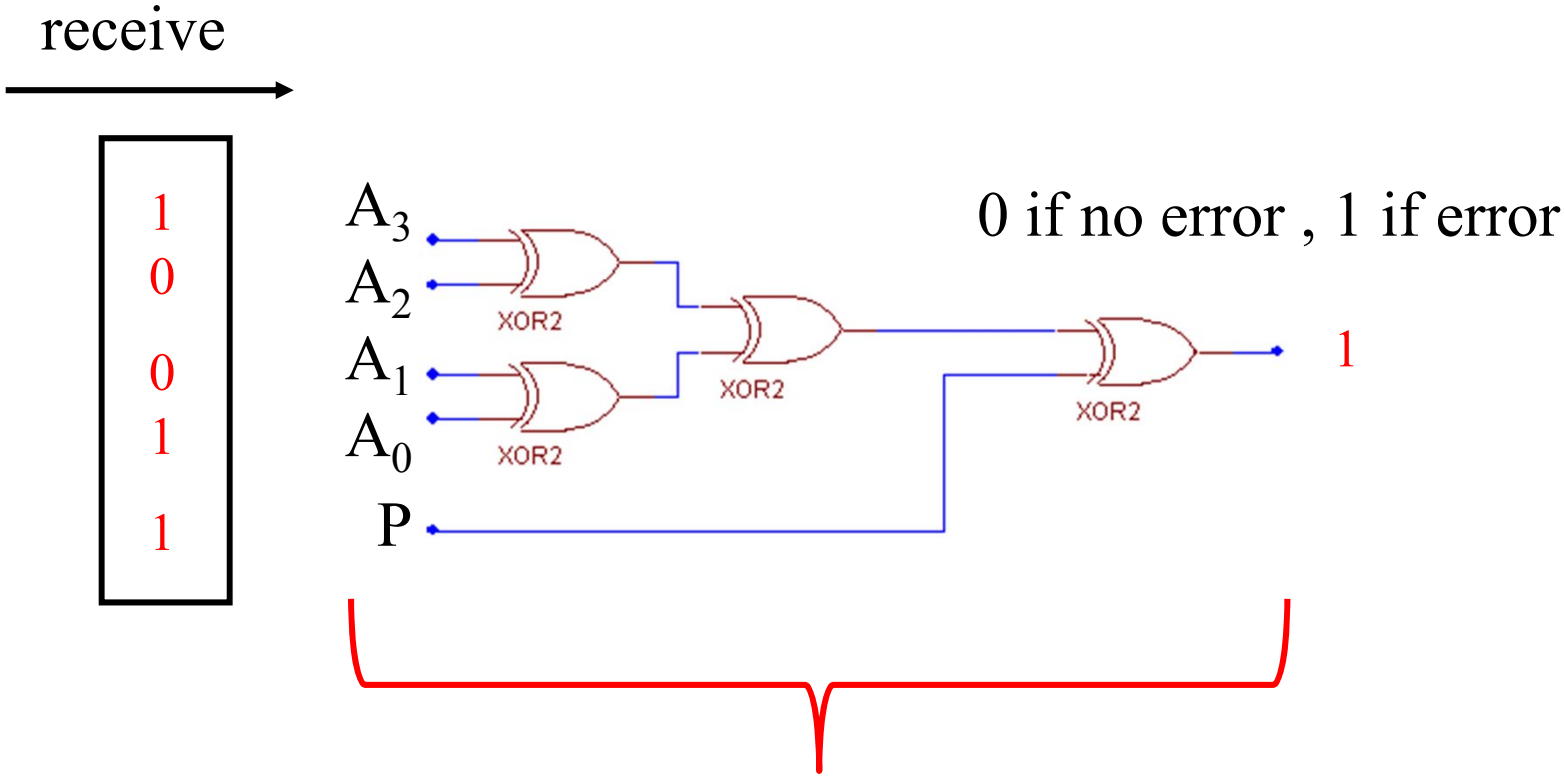
EVEN PARITY – transmit 1101

Case1 - Correct data received



EVEN PARITY – transmit 1101

Case2 - Incorrect data received



Summary

- Decoders have been examined.
- A parity bit can be added to data for error checking.
- Exclusive OR gates can be utilised for parity generation and checking.