Examination Feedback for EEE6213 – Principles of Semiconductor Device Technology
Spring Semester 2014-15

Feedback for EEE6213 Session: 2014-2015

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

The students have done well, despite a large change in the exam paper for the revised syllabus of the increased credit module. This included a large percentage of new subject matter in comparison to the older version of this course.
The assignment component needs more work next year- part of the problem seems to be the tools on the nanohub were not as easy to handle and work begun rather late but had to be kept in line with the subject matter taught in class. By and large all students got a chance to develop some modelling skills- all have shown some level of skills by showing figures achieved from running device simulators.

Question 1:

15 students answered this question. It is quite pleasing to note that several students were able to calculate the areal density in various planes in silicon. All sub-questions were proven to be attainable.

Question 2:

22 students answered this question (which is almost the whole class). New components here included the band diagrams in a MOSFET which a few students got correct, and so also the calculations of the scattering time.
Next year, I would like to focus more so that 100% of the students are able to achieve the understanding of the band diagrams.

Question 3:

19 students attempted question 3. Not many were familiar with the range and projected range in the ion implantation technique. The question on ion implantation appeared for the first time, not many were able to attempt this. Other subquestions were very well answered and in particular to higher standards than what I have seen before.

Question 4:

Q 4 a was not well answered by most of the students, however many were able to draw and understand the band diagrams for the working of a tunnelfet- which is very pleasing. The CMOS process flow was also answered to high standards.