Feedback for EEE348 Session: 2014-2015

General Comments:

Students' attempts at this paper were hampered because very few people did Q2 – despite it being straightforward.

Question 1:

This question was relatively well answered. Many people correctly derived the circuit (in various forms). However, in some cases, people made silly mistakes in the algebraic manipulations needed. $\overline{CD} \neq \overline{C}.\overline{D}$. I tried to mark each section based on the correctness of what a student had done relative to what they believed they were doing. So, for example, if they had made a mistake in the logic function but then implemented the logic function correctly then they would get marks.

Question 2:

So few people did this question that it is difficult to make sense of what they had done. However, in the main, in part ai), people got the mode of the transistor wrong (it's saturated) and/or the equation for I_D and then did not recognize that all they had to do was equate it with CdV_{out}/dt and then integrate to find V_{out}.

Question 3:

Part ai) was book work and most students did well with it. aii) could be worked out by formula (many students did this) but also just from physical intuition – the triode region is defined as a $V_{DS\ less}$ than $V_{OV,}$ which could evidently become the case if V_{OV} is doubled.
bi) produced all sorts of strange small signal models. It was clear which students had attempted the tutorial sheets as there are plenty of examples of deriving the small signal model in there… bii) and biii) were generally tackled well. biv) had the classic mistake: label-less or incorrectly labelled axes!

Question 4:

Part a) was book work but students do always seem to struggle on these descriptive questions - it's as important to understand the terms involved in a subject as to be able to apply some of the relevant equations. Part b) was perhaps a little trickier but I was pleased with how well students did here. Part c) was less well attempted, with a lot of students confused by the PMOS transistors, which are 'upside down' compared to the NMOS devices.

Question 5:

Most students did well. However for part 1(c) a number of students did not describe how the solar cells should be connected. In part 1(d), some of the students provided descriptions for PERL cell but the answer are too short and lacking details.

Question 6:

It is a surprised that students appear to not have read the question carefully as it was stated that the InP is the p and n layer of a pin diode. Therefore a number of students failed to describe the advantages of using InP. InP is transparent at 1550nm, and hence loss of carriers through recombination is reduced. Lower diffusion current, and hence lower dark current can also be obtained using the wider bandgap InP.
For 2(a) iii, some students calculated transit time limited bandwidth instead of RC limited bandwidth.
In 2(b) most students provided brief answers lacking in details, such as how the thickness of the depletion should be smaller than 0.53 μm and provide comments on the size and capacitance of the required diode.
In 2(c) i) gain should be calculated at 10V not at $0.9V_b$. It can be easily shown that the signal is below the dark current. In 2(c) ii, noise calculation is not required, as we simply need to work out the gain required so that multiplied photocurrent is larger than dark current.

Question 7:

Most did well in 3(a) however in 3(b) a number of students provided description of double heterostructure LED, which is not a suitable structure for high brightness GaN LEDs. Instead the answer should focus on features in the MQW InGan/GaN with flip-chip, substrate removal, roughened surface, bottom contact and use of high thermal conductivity substrate.

Question 8:

Some of you provided very poor (or wrong) sketch of the band diagram in 4(a). In part (c) and (d) a number of students failed to describe resonant tunneling diode. Instead they discuss tunnel diodes.