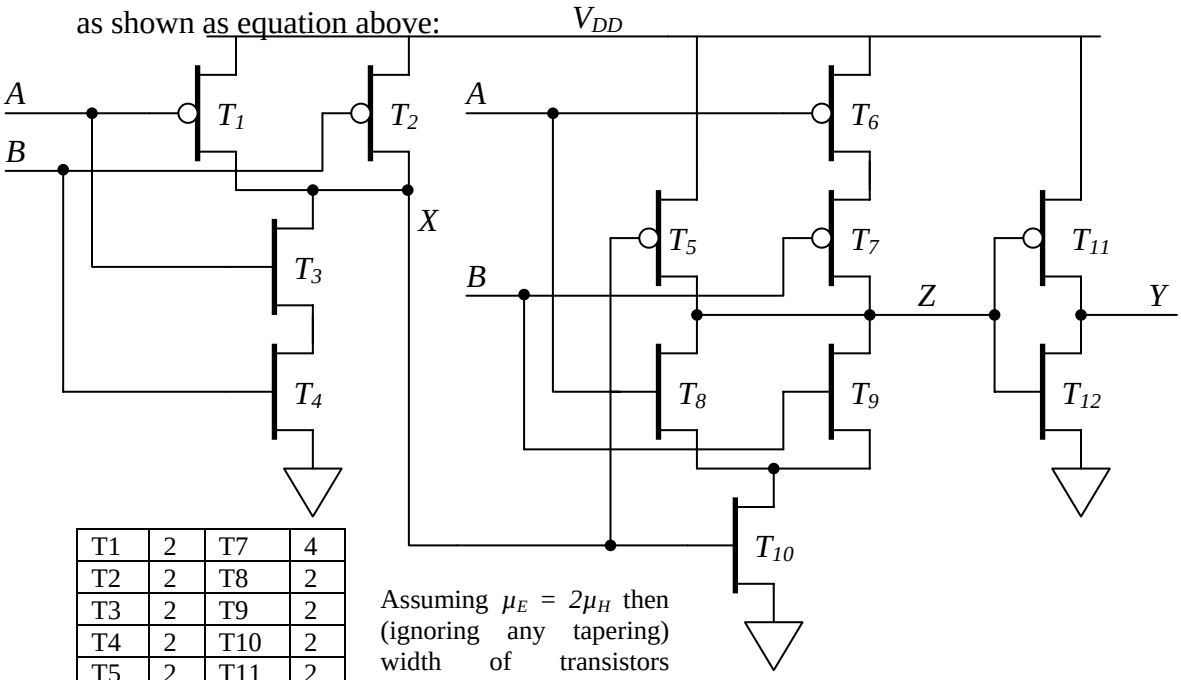
DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2006-2007 (2 hours)

Answers Introduction to VLSI Design (EEE310)/VLSI Design (EEE6036)

1. a. i. *Design a standard-CMOS, transistor-level circuit for an XOR function of two inputs, A and B (hint: $Y = A \oplus B = A.\overline{B} + \overline{A}.B$) and size the transistors for a minimum sized gate.*

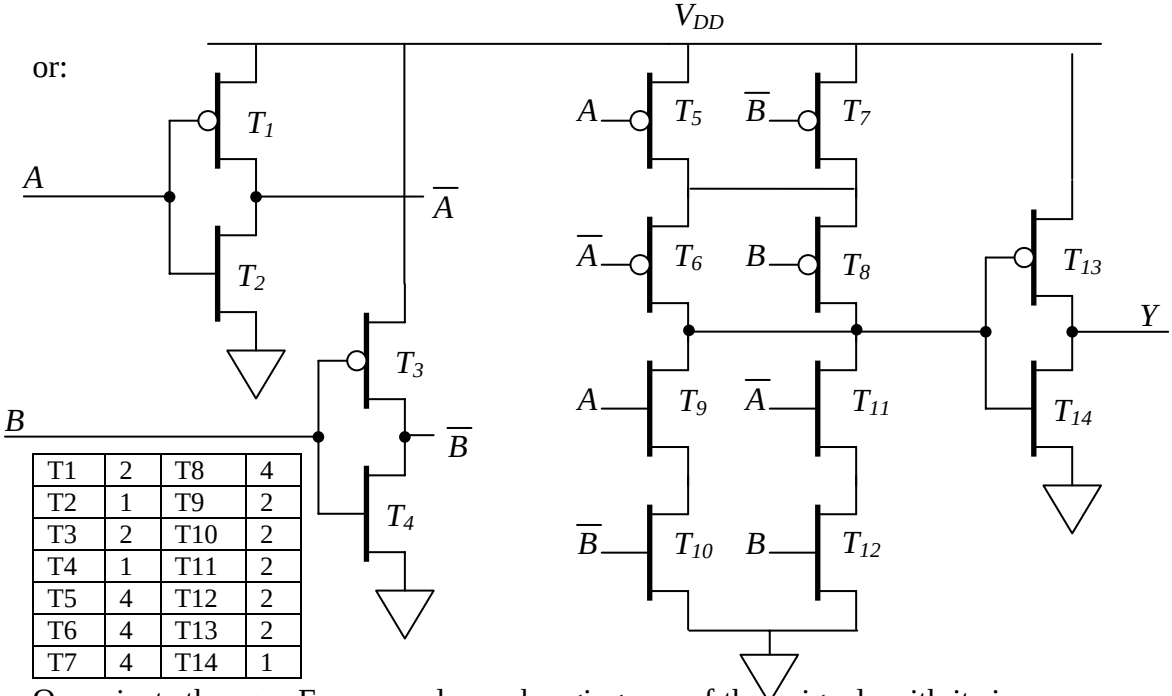
Number of approaches that might be taken e.g. decomposing it as $\overline{AB}.(A+B)$ or as shown as equation above:



T1	2	T7	4
T2	2	T8	2
T3	2	T9	2
T4	2	T10	2
T5	2	T11	2
T6	4	T12	1

Assuming $\mu_E = 2\mu_H$ then (ignoring any tapering) width of transistors compared to a minimum sized *n*-FET

or:



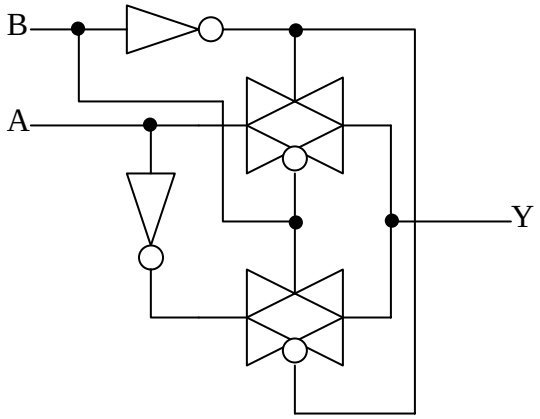
T1	2	T8	4
T2	1	T9	2
T3	2	T10	2
T4	1	T11	2
T5	4	T12	2
T6	4	T13	2
T7	4	T14	1

Or variants thereon. For example, exchanging one of the signals with its inverse in the central part of the circuit will allow the final inverter to be dispensed with. **(8)**

ii. *How would you change the circuit in part **1.a.i** to produce an XNOR function.*

Remove inverter from either circuit, or in the case of the latter, swap over the transistors controlled by one of the inputs and its inverse (independent of whether the circuit has an inverter on the end). **(2)**

b. **i.** *Draw a circuit to show how a two input XOR function could be implemented using two transmission gates (TG) and a few inverters.*



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ii. *How, optimally, would the circuit in part **1.b.i** be changed to produce an XNOR function?*

By swapping the TG inputs driven by A or its inverse, or by swapping the TG control inputs driven by B and its inverse. **(1)**

iii. *Does the TG approach to implementation have any advantages or disadvantages over the standard-CMOS approach? If so, what are they?*

The CMOS implementations have circa 12-14 transistors and areas between 30-40x a minimum sized *n*-FET. The TG approach requires 8 transistors (area circa 12). However, the output is driven via TGs (which introduces a larger output impedance than for a CMOS circuit) and, indeed when A is 1 and B is 0, the output will be driven from the previous stage. This will increase susceptibility to noise. **(3)**

2. *The circuit in **Figure 2** (which is somewhere inside an IC and part of a bigger circuit) must be altered to allow it to be tested.*

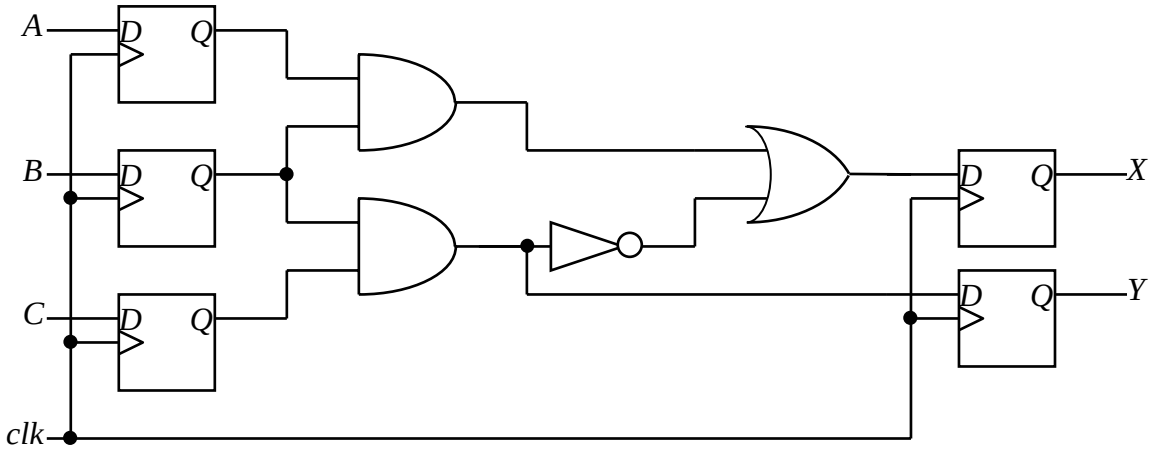
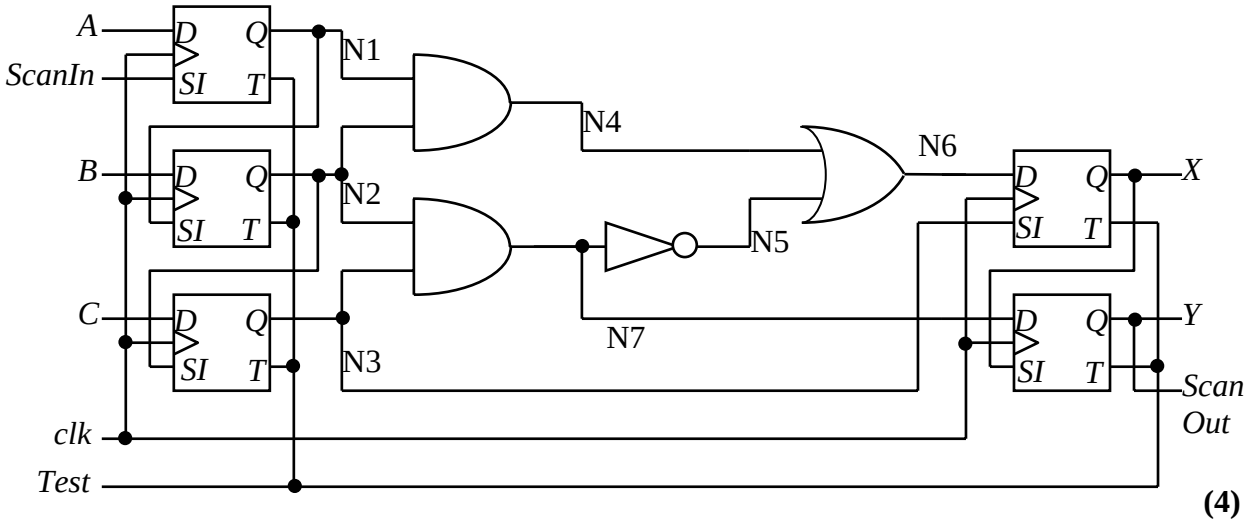


Figure 2

a. **i.** *What changes must be made to the circuit to allow it to be tested (draw a diagram to show what must be done)?*

The FFs must be changed to scan FFs, which can be connected to form a Shift Register to load/unload test vectors. The *T* input is used to change between normal operation and shifting in via the *SI* input during test. The Scan FFs are connected from *Q* to *SI* to form a chain. *ScanIn* and *ScanOut* allow the chain to be connected to rest of the circuit's test structures.



(4)

ii. *Assuming a simple stuck-at fault model, identify how many individual tests must be applied and the associated test vectors.*

There are 7 internal nodes between the FFs (note: extra mark if you recognise that the upper AND gate and the OR gate have one extra internal node e.g. NAND followed by INV and NOR followed by INV). Consequently, this should result in 14 tests (stuck-at 0 and 1 for each node). However, some faults are equivalent and so you cannot isolate all of the possible faults and some of the tests can be used to find more than one fault

Node	**SA**	**N1**	**N2**	**N3**	**N4**	**N5**	**N6**	**N7**	**X**		**Y**	
		A	B	C					✓	×	✓	×
N1	0/1	1/0	1	1	1/0	0	1/0	1	1/0	0/1	1/1	1/1
N2	0/1	1	1/0	1	1/0	0/1	1/0	1/0	1/1	1/1	1/0	0/1
N3	0/1	X	1	1/0	X	0/1	X	1/0	X	X	1/0	0/1
N4	0/1	1/0	1	1	1/0	0	1/0	1	1/0	0/1	1/1	1/1
N5	0/1	0	1	1/0	0	0/1	0/1	1/0	0/1	1/0	1/0	1/0
N6	0/1	0	1	0/1	0	1/0	1/0	0/1	1/0	0/1	0/1	0/1
N7	0/1	X	1	1/0	X	0/1	X	1/0	X	X	1/0	0/1

For the best marks: the candidate should identify that:

Tests for N1 and N4 are equivalent.

Tests for N5 and N7 can be combined (with N1 being set to 0), recognising that the discrepancies between X and Y will identify that one is in error (or the other). Additionally, the tests for N3 and N6 are equivalent to these tests. Having said this, the test for N1/N4 will also test N6. Consequently, the results from all of these tests will give a much better idea of faulty nodes.

From this there are six independent tests (N1, N2, N5 SA1/0 above). **(8)**

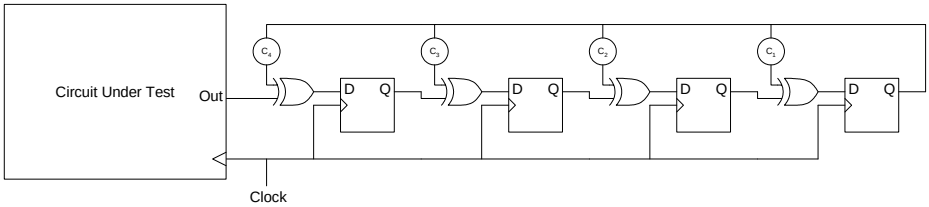
iii. *Are there any problems with testing this particular part of the circuit?*

It is not possible, simply, to test for all the possible nodes independently and, in some cases, differences cannot be resolved without additional test logic. This additional logic would force certain nodes to defines states to stop them interfering with other tests. **(2)**

b. *What is BIST and how is it used? What is the significance of the signature?*

BIST is based upon a linear-feedback shift register that is set to generate pseudo-random sequences of bits or numbers - hence the name Pseudo-Random Binary Sequence (PRBS) generator.

In BIST, the LFSR is augmented as follows:



An output from the circuit being tested is combined with one of the feedback paths in the LFSR (the inputs to the circuit being tested are provided by other LFSRs). During BIST, the circuit and the LFSRs are initialised to defined states and a defined number of clocks are applied. As the circuit and LFSRs are clocked, the state of the inputs and, hence, output changes in a way determined by the function of the circuit and the state of the LFSR connected to the output changes *influenced by the output from the circuit being tested*. At the end of the test, the state of this LFSR, the signature, should be well-defined but seemingly random value – the *signature*. If the sequence of outputs were different - even in a single value - the signature in this LFSR would be completely different. Comparing the value in the LFSR at the end of the test gives confidence that the circuit is performing properly. The LFSRs can be very long to ensure that the probability of the same value occurring for correct and incorrect operation is very low. Other PRBS generators are used to generate the inputs to the circuit under test. **(4)**

How is communication normally made between the outside of an IC and the test structures inside the IC?

JTAG defines a serial interface between ICs for boundary scan purposes (i.e. loading and reading the pins of the IC). However, it can equally well be used as an access mechanism to a test controller within the IC either for scan testing or BIST. **(2)**

3. *A 0.13µm digital IC can be modelled as being equivalent to $15x10^6$ simple, 2-input gates where each gate has, on average, the equivalent of 35µm of wire connected to its output. Each gate has an input capacitance of 3fF on each input and an effective output capacitance of 1.5fF. The wiring, on average, has a capacitance equivalent to 0.2fF/µm.*

The IC is clocked at 2GHz with a power supply voltage of 1.8V and, on average, the probability of any wire changing state on the rising edge of the clock is 0.15

a. *Derive an expression for the power dissipation in a digital CMOS circuit due to switched capacitance.*

Substantially, the inputs to a gate and the interconnect between gates appears to be capacitive. As a wire connected to an input cycles from $0V \rightarrow V_{DD} \rightarrow 0V$, the

capacitance is charged and discharged. The charge comes from V_{DD} and is discharged to 0V. This is a current.

Consider charging a capacitor, C to V_{DD}. The charge on the capacitor will be CV_{DD}. As the capacitor is discharged to 0V, this charge will flow down to earth. The net charge moved through V_{DD} is, therefore, CV_{DD}. If this operation is being done f times a second then the charge moved per second is fCV_{DD}. and this is current, axiomatically. This current flows across V_{DD} and so the power dissipated by this switching activity, P_{sw}, is fCV_{DD}^2. To put this in terms of a circuit, $C=C_{in}+C_{wire}$ (the sum of the gate's input capacitance and the capacitance of the wire driving the gate input), and f is the frequency at which the input is being driven. If we are to extend this expression from a single gate to an entire circuit we must perform a summation across all of the gates and interconnect in the circuit. So if we assume that there are n wires in the design and the total capacitance associated with wire$_i$ and the load that it is driving is C_i then the total switching power dissipated by the circuit should be: **(1)**

$$P_{sw} = \sum_{i=1}^{n} f_i C_i V_{DD}^2$$ **(1)**

This expression assumes that each wire is switching at its own frequency, f_i. However, in practice, the switching of all the wires will be controlled by a single frequency f_{clk} and each wire will change state on *either* clock edge with a defined probability α_i. In this case, the expression becomes:

$$P_{sw} = f_{clk} V_{DD}^2 \sum_{i=1}^{n} \alpha_i C_i$$

In many cases, it is possible to simplify the expression further by assuming a value for α that is representative for the whole circuit rather than an individual wire.

$$P_{sw} = \alpha f_{clk} V_{DD}^2 \sum_{i=1}^{n} C_i$$ **(2)**

b. **i.** *What is the total capacitance that is being switched in the IC?*

Each gate has an output capacitance of 1.5fF and 35µm x 0.2fF/µm = 7fF of wiring capacitance. Thus, this total = 8.5fF. Each gate also has two inputs at 3fF each – hence, the total switched capacitance associated with each gate is 14.5fF. There are $15x10^6$ gates and so the total switched capacitance is 217.5nF.

ii. *What is the power dissipation of the IC, due to switched capacitance, under the stated conditions?* **(2)**

$$P_{sw} = \alpha f_{clk} V_{DD}^2 \sum_{i=1}^{n} C_i$$

and V_{DD}=1.8V, $f_{clk}=2x10^9$, $C_i=2.175x10^{-7}$. If the probability of the signal changing state on the *rising* clock edge is 0.15 then α, as defined above is 0.075. That is, αf_{clk} is the effective, average clock frequency on the wires. From this,

$P_{sw} = 0.075 * 2x10^9 * 1.8^2 * 2.175x10^{-7} = 105W$

(4)

c. **i.** *What is other major contributor to the overall dynamic power dissipation apart from switched capacitance?*

The other major contributor is the crowbar current, which flows when the pull-up and pull-down networks are momentarily on together when the output is transiting. **(2)**

ii. *What factors give rise to static power dissipation – what is happening to static power dissipation as the technology is shrunk?*

Sub-threshold leakage, when the gate voltage is below V_T is becoming a major problem. As technology shrinks, it is desirable to reduce V_T with V_{DD} to keep current drive up. However, as V_T falls conduction when V_{GS} is 0V increases exponentially. Consequently, there is a trade-off as technology shrinks.

Gate Leakage, where, in an effort to keep charge generated in the channel at a reasonable value, the gate is thinned as the supply voltage is dropped (constand field scaling). However, as the gate thickness reaches 1nm, the current that tunnels through the gate reaches tolerable limts ($100/cm^2$). **(4)**

d. *The technology that is used to fabricate the IC is shrunk to 90nm (so that linear dimensions reduce by a factor of 1.4). Estimate, simply, what might happen to the power dissipation due to switched capacitance, stating any assumptions that you make.*

We might assume that input and output capacitance reduce by 1.4 – because the area will halve but the thickness of the oxide might reduce by the same amount. With respect to the interconnect, again we are implementing the same system so even the longer wires will reduce in length and area but the dielectric layers will, again reduce. Consequently, the interconnect capacitance might reduce by 1.4. However, it is entirely possible that the height/spacing of the wires might not reduced to offset the increased coupling effects and reduce the resistance of the wires so it is not really possible to give anything more than a 1st order answer to the amount by which the capacitance is reduced. The supply voltage would probably also be reduced to circa 1.2V and this would have the most significant effect. Consequently, the power consumption might fall to:

$P_{sw} = 0.075 * 2x10^9 * 1.2^2 * 1.554x10^{-7} = 34W$

However, it might also be possible to increase the operating frequency but this is not accounted for in the answer. However, f_{CLK} might increase anywhere up to 3GHz. **(4)**

4. *The circuit in **Figure 4** implements a logic function but is not standard CMOS*

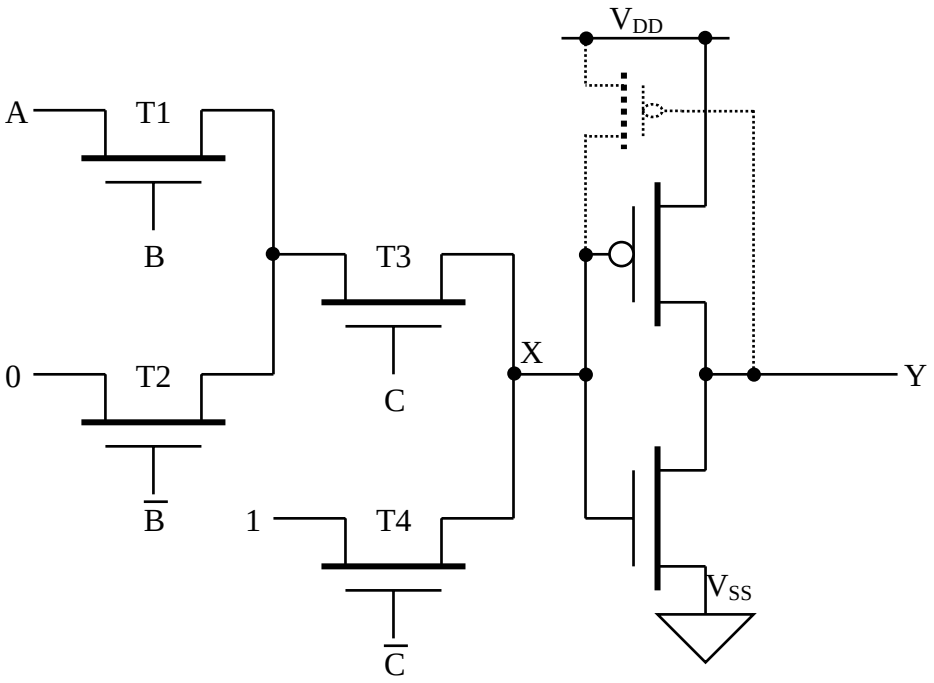


Figure 4

a. *What is the logical function of the circuit (Hint: you can ignore the dotted transistor when determining the function)?*

The output stage is an inverter and so *Y* is the logical inverse of the node at the inverter's input. The pass-transistor network at the input to the inverter controls the state of this point. Looking at a truth table, and ignoring the fact that the *n*-pass transistors will not define 1s very well:

A	*B*	*C*	*X*	*Y*	*Notes*
0	0	0	1	0	T4 on
0	0	1	0	1	T2, T3 on
0	1	0	1	0	T4 on
0	1	1	0	1	T1, T3 on
1	0	0	1	0	T4 on
1	0	1	0	1	T2, T3 on
1	1	0	1	0	T4 on
1	1	1	1	0	T1, T3 on

From this:

$$Y = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C$$
$$= \overline{A}\overline{B}C + \overline{A}BC + \overline{A}\overline{B}C + A\overline{B}C$$
$$= \overline{A}(\overline{B} + B)C + (\overline{A} + A)\overline{B}C = \overline{A}C + \overline{B}C$$

(8)

b. *Why do you think that the dotted transistor (shown smaller here to denote that it is a weak transistor – reduced current drive) is included in the circuit – make sure you describe its purpose?*

When there is a 1 at the input to the inverter then this will be poorly defined. Assuming that the drain and gate of one of the *n*- pass transistors is at V_{DD} then the source (defining the voltage) will be at V_{DD}-V_T. This may be sufficiently low to begin switching on the *p*-FET of the inverter – resulting in increased power consumption and potentially defining the output voltage less well. To avoid this there is a *weak p*-FET pulling up this point. When the point rises to V_{DD}-V_T this will be sufficient, at least, to cause the output to fall far enough to switch on the dotted transistor, which will pull the poorly defined point to V_{DD}. **(4)**

Why is a weak transistor needed as opposed to a transistor of normal drive strength?

The problem is that when the output transits to 1, the input to the inverter must be pulled to 0 through a string of a few pass transistors. Consequently, the weak dotted transistor, whilst good enough to raise the voltage in the absence of being driven, must be poor so that the point can be pulled down to zero quickly and without too much power being dissipated before the dotted transistor switches off. **(4)**

How would you make a weak transistor?

Make it longer.

(2)

c. *In the circuit in Figure 4 there are more n-type than p-type transistors. Does this make any difference to circuit layout?*

Yes, it makes it more compact. Assume that it is an *n*-well process, there will be smaller (and probably fewer) *n*-wells for the *p*-FETs – being mainly composed of *n*-FETs and the area lost at the boundaries of the wells will be reduced. **(2)**

End of Answers