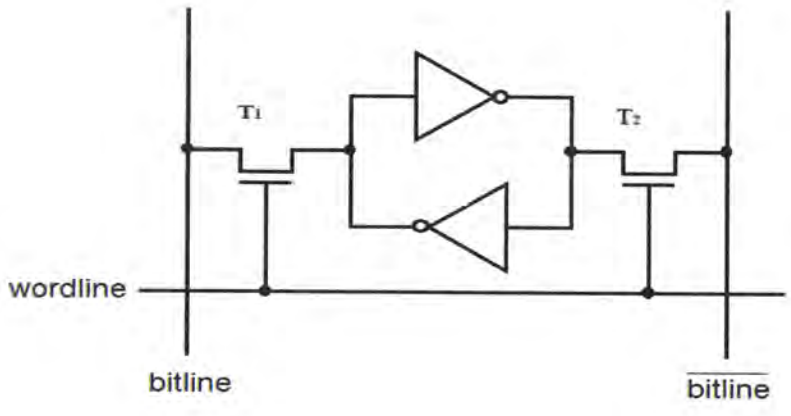
EEE225 Solutions (NJP) Digital Part

1.

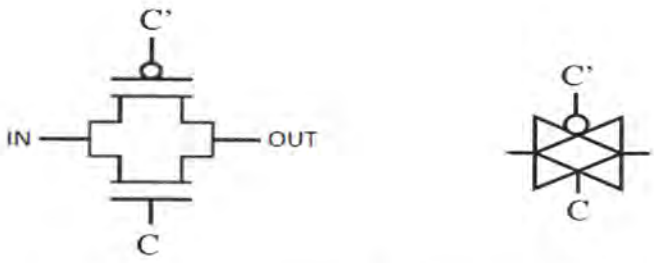


(3)

To write to the cell, *bitline* is set to the required data value and $\overline{bitline}$ is set to the complement. The controller then sets wordline = 1 which turns on transistors T1 and T2. The data values then appear in the inverter loop overwriting any previous value. **(2)**

To read from the cell, *bitline* and $\overline{bitline}$ are both precharged to 1. Wordline is then set to 1. One of the enabled transistors will have a 0 at one end which will cause the corresponding precharged 1 to drop to a slightly lower voltage than a normal 1. Both of the bitlines are connected to a sense amplifier which can detect this variation and hence the data value. **(3)**

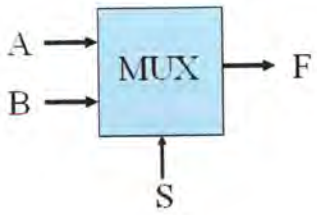
2.

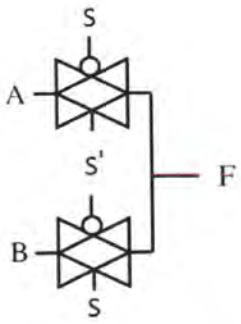


(2)

Both transistors are ON or OFF simultaneously. The nmos switch passes a good zero but a poor 1. The pmos switch passes a good one but a poor 0. A bilateral switch is formed which passes a good 0 and good 1 in both directions. **(3)**

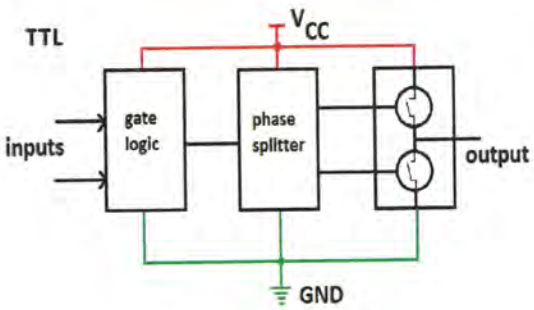
S	F
0	A
1	B

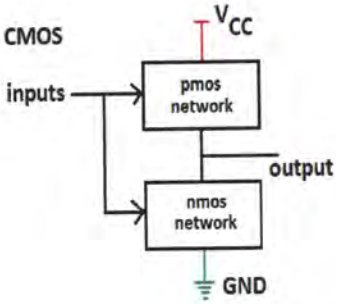




(3)

3.





(3)

TTL – the first structural block implements the required logic. The second block is a phase splitter which is required to drive the final block which is a totem-pole output stage. In contrast, a CMOS logic gate consists of a pmos pull-up network to the positive supply rail and an nmos pull down network to ground. **(2)**

In the case of TTL the gate logic consists of a multi-emitter transistor and the number of emitter connections would be increased. In the case of CMOS, an additional transistor in both the pull-up and pull-down network would be required for each extra input. **(3)**

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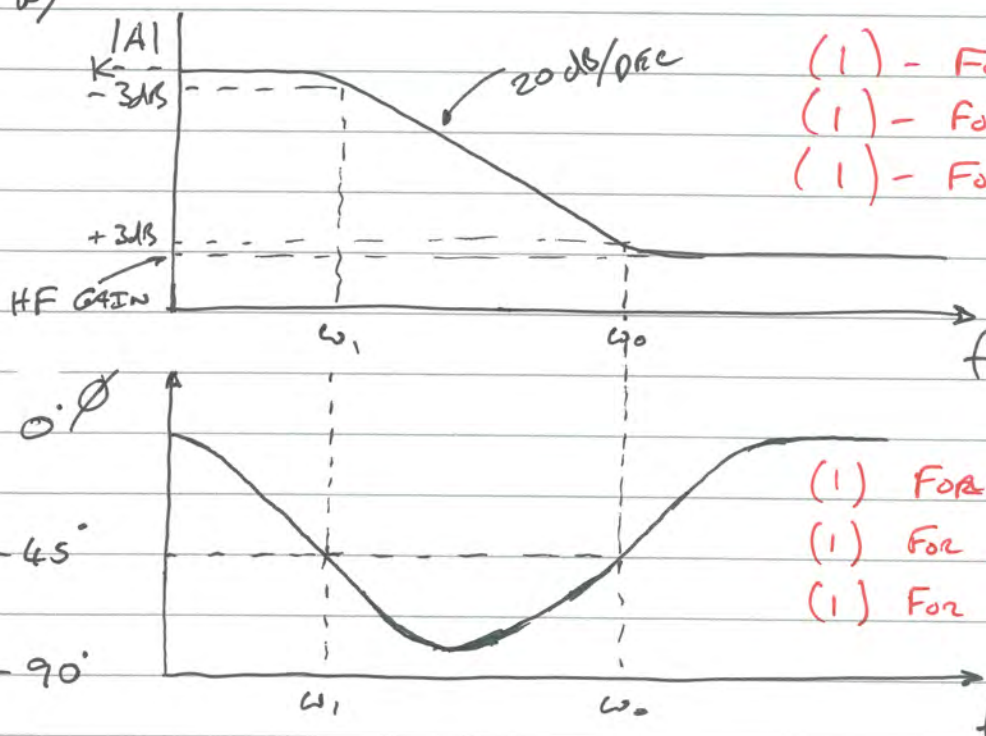
Q4

a) LF GAIN $= -K = \dfrac{-R_3}{R_1}$ (1)

HF GAIN $= \dfrac{-\left(\dfrac{R_3 \cdot R_2}{R_3 + R_2}\right)}{R_1}$ (1)

b)



(1) - FOR SHAPE
(1) - FOR ω_1 & ω_o [x AXIS]
(1) - FOR K +/- 3dB [y AXIS]

(1) FOR SHAPE
(1) FOR ALIGNMENT OF ω_o & ω_1
(1) FOR 45° LAG AT +/- 3dB.

THESE DIAGRAMS ARE GIVEN IN THE LECTURE NOTES SO COULD BE "LEARNED" BUT BEING ABLE TO "THINK" THEM OUT IS BETTER.

(8 IN TOTAL)

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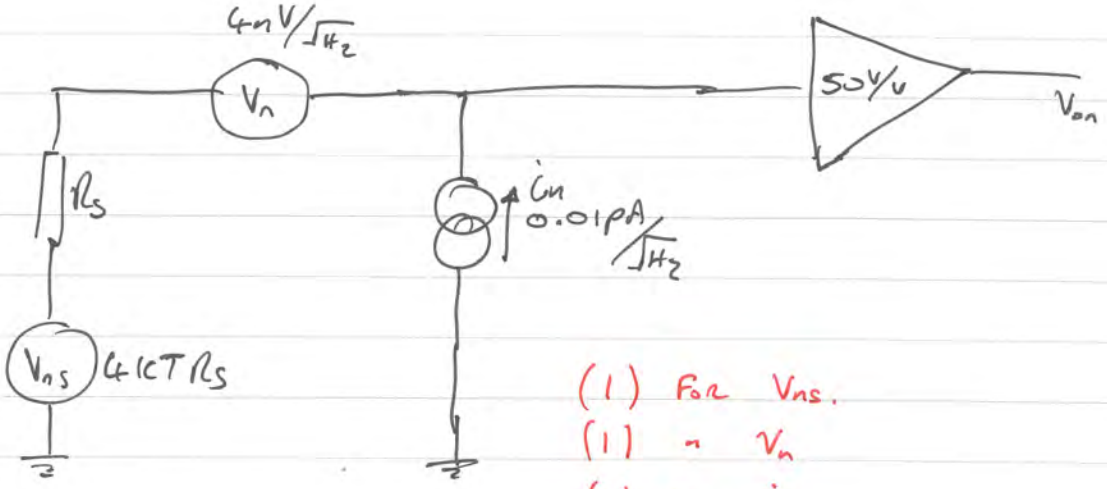
Q5

a)



(1) For V_{ns}.
(1) " V_n
(1) " i_n
(1) " THE AMPLIFIER

b) $$\overline{V_{on}^2} = K^2\left(\overline{V_{ns}^2} + \overline{V_n^2} + \overline{i_n^2}R_s^2\right) \quad (1)$$

$$= 50^2\left(4KTR_s + 1.6\times10^{-17} + 1\times10^{-28}\cdot 360\times10^3\right) \quad (1)$$

$$= 2500\left(9.875\times10^{-18} + 1.6\times10^{-17} + 3.6\times10^{-23}\right) \quad (1)$$

$$= 6.4688\times10^{-14}\ V^2/Hz.$$

OR $254\,nV/\sqrt{Hz}$. (1)

- IT'S OK TO IGNORE THE $\overline{i_n^2}R_s^2$ TERM.
FULL MARKS STILL AVAILABLE.

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Q6

a) FIRST ORDER AMPLIFIER HAS SMALL SIGNAL BANDWIDTH = GBP ÷ GAIN ← (CLOSED LOOP GAIN.)

AND RISE TIME:

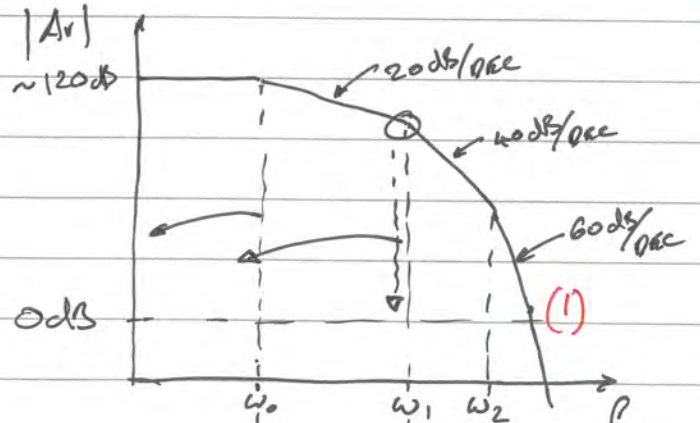
$$t_R = 2.2\tau$$

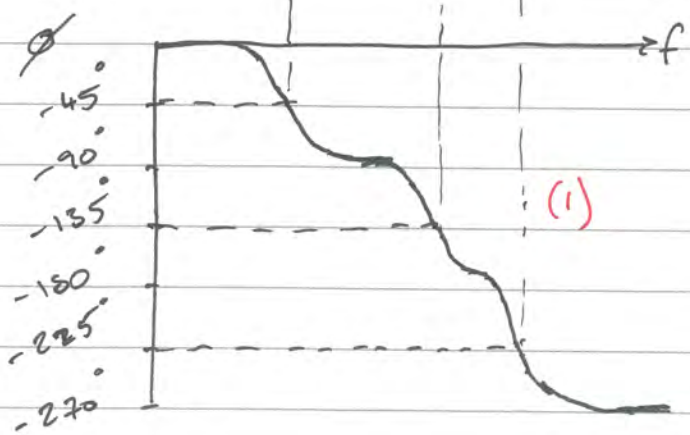
WHERE $\tau = \frac{1}{\omega_0}$: ω_0 IS THE SMALL SIGNAL BANDWIDTH.

(1) FOR FREQUENCY DOMAIN.

(1) " TIME "

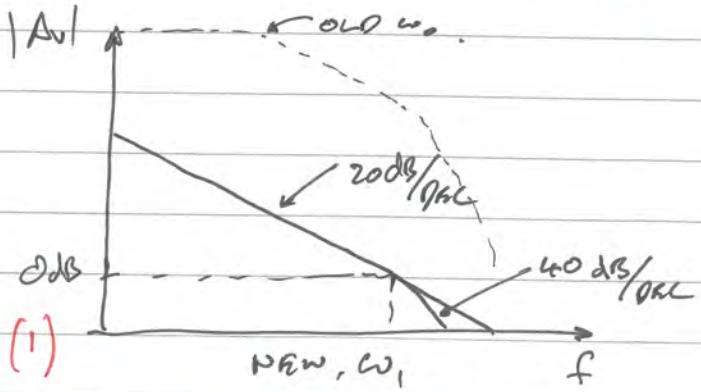
b) • A STANDARD OPAMP HAS 3 STAGES AND EACH STAGE PROVIDES 1 POLE. (1)





• BY MOVING THE LOWEST OR "DOMINANT" POLE, ω_0, DOWN IN FREQUENCY UNTIL $A_V = 1$ @ ω_1, THE CLOSED LOOP RESPONSE CAN BE MADE FIRST ORDER. (1)

• THIS IS CALLED "UNITY GAIN COMPENSATION". IT YIELDS THE RESPONSE CHARACTERISTICS IN CLOSED LOOP GIVEN IN 6a. (1)



(6 IN TOTAL)

THIS IS A STANDARD ANSWER THAT CAN BE MEMORISED.

EEE 225 May 2015

~~No~~ 7

Q(1)a Charge neutrality condition

$$n + N_a = p + N_d$$

also $$np = n_i^2 = p_i^2$$

$$n + N_a = \frac{n_i^2}{n} + N_d$$

$$n^2 - (N_d - N_a)n - n_i^2 = 0$$

$$n = \frac{N_d - N_a}{2} + \frac{N_d - N_a}{2}\left[1 + \left\{\frac{2n_i}{(N_d - N_a)}\right\}^2\right]^{1/2} \quad (3)$$

i) For n-type extrinsic, $N_d - N_a \gg n_i$

$$\therefore \quad n = N_d - N_a \simeq N_d$$

$$p = \frac{n_i^2}{N_d} \quad (2)$$

ii) For compensated near intrinsic

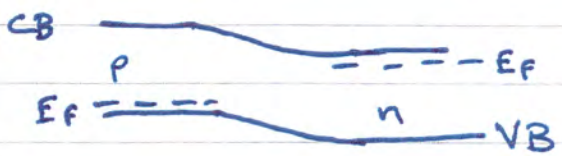
$$n_i \gg |N_d - N_a|$$

so

$$n = \frac{N_d - N_a}{2} + \frac{N_d - N_a}{2}\left[\frac{2n_i}{N_d - N_a}\right] \simeq n_i$$

$$p = \frac{n_i^2}{n} \simeq p_i \simeq n_i \quad (3)$$

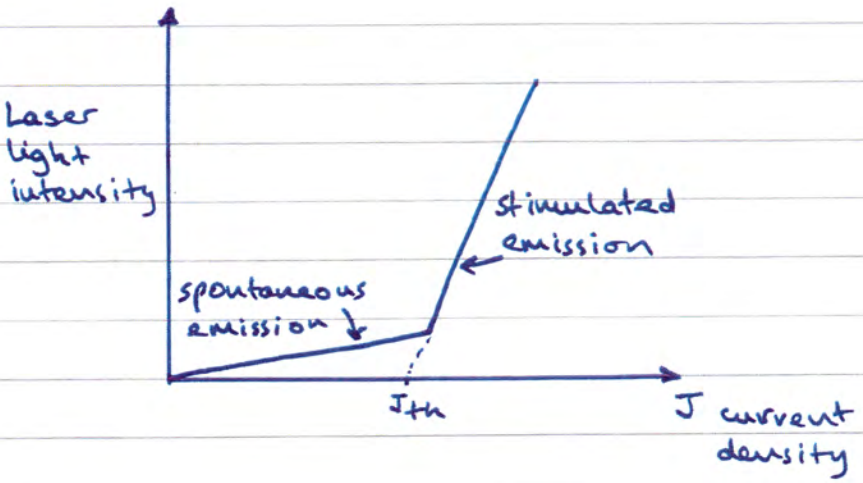
Q b Under lasing condition, the p-n junction is forward biased, so



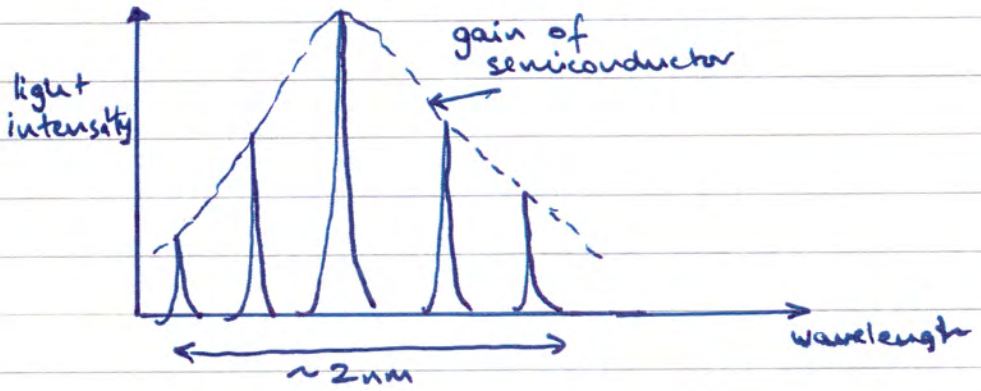
(2)

cont.

Q1



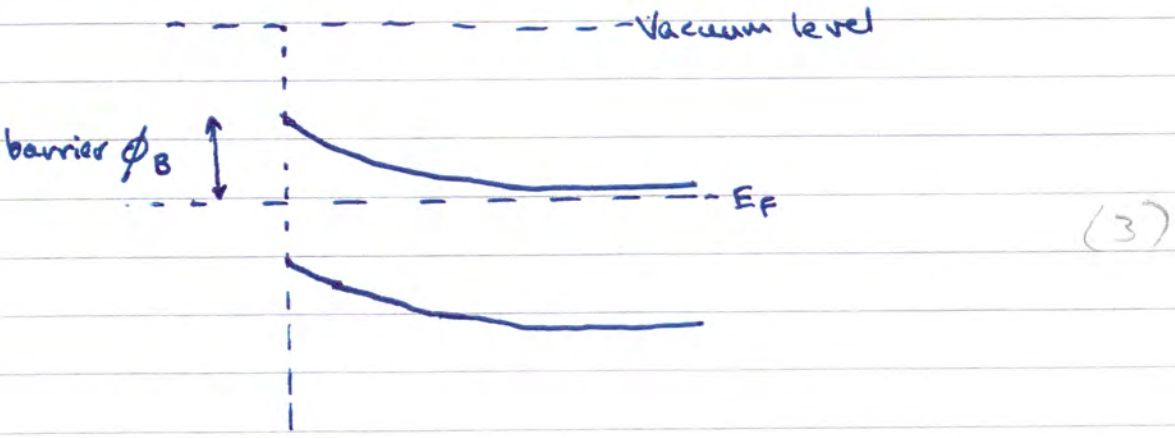
(3)



(3)

Q2

(i) Rectifying junction $\phi_M > \phi_S$ n-type



(3)

cont

Q2(ii) ohmic

(3)

$\phi_s > \phi_m$ n-type semiconductor

For rectifying junction, under forward bias, majority electrons flow from semiconductor to metal. Under reverse bias, minority electrons from metal can thermionically get across the barrier ϕ_B into the semiconductor

(2)

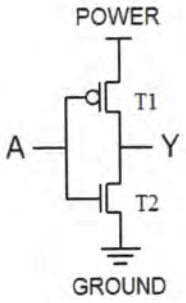
10.

Apply $V_{out} = -\frac{V_S}{2^{n-i}}$ to all inputs that are HIGH, then sum the results.

$V_{out}(D_0) = -\frac{3.3\text{V}}{2^{4-0}} = -0.206\ \text{V}$ $\quad V_{out}(D_1) = -\frac{3.3\text{V}}{2^{4-1}} = -0.413\ \text{V}$

$V_{out}(D_3) = -\frac{3.3\text{V}}{2^{4-3}} = -1.65\ \text{V}$ Applying superposition, $V_{out} = -2.269\ \text{V}$

(8)

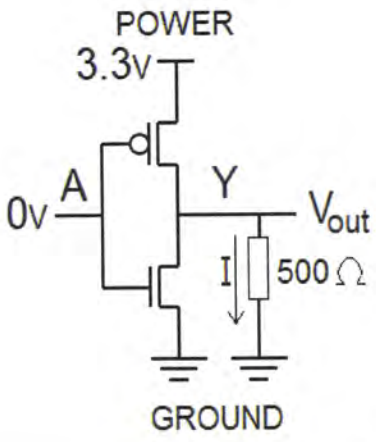


Inverter

A	T1	T2	Y
L	on	off	H
H	off	on	L

Inverter truth table

(4)



(4)

pmos is on with a resistance of 75 Ω

nmos is off with a resistance of 500,000 Ω

Load impedance is 500,000 Ω in parallel with 500 Ω ≈ 500 Ω

$V_{out} \approx 3.3 \times (500 / 575)$

$\approx 2.87\text{V}$

$I \approx 3.3 / (75 + 500)$

$\approx 5.7\text{mA}$

(4)

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Q11 a

i) T_1 & T_2 - ARE A DIFFERENTIAL AMPLIFIER. (1)

OR ANYTHING ELSE - THEY SUBTRACT V^+ & V^- TO GIVE AN ERROR

THAT IS TRUE AND PERTINENT. CURRENT THAT FLOWS IN THE COLLECTOR OF T_1 & T_2 (1)

T_3 & T_4 - AREA CURRENT MIRROR (1)

- T_4 REFLECTS THE ERROR CURRENT IN T_2'S COLLECTOR TO T_3'S COLLECTOR AND IS IN ANTI PHASE WITH THE ERROR CURRENT IN T_1'S COLLECTOR EFFECTIVELY DOUBLING THE DIFFERENTIAL AMPLIFIER GAIN.
- T_4 & T_3 REDUCE THE LOAD OF T_5 ON T_1'S COLLECTOR EFFECTIVELY BALANCING THE DIFFERENTIAL AMPLIFIER AND REDUCING OUTPUT OFFSET.

(1) FOR EITHER OR ANYTHING ELSE THAT IS TRUE AND PERTINENT.

T_5 & T_6 - DARLINGTON. (1)

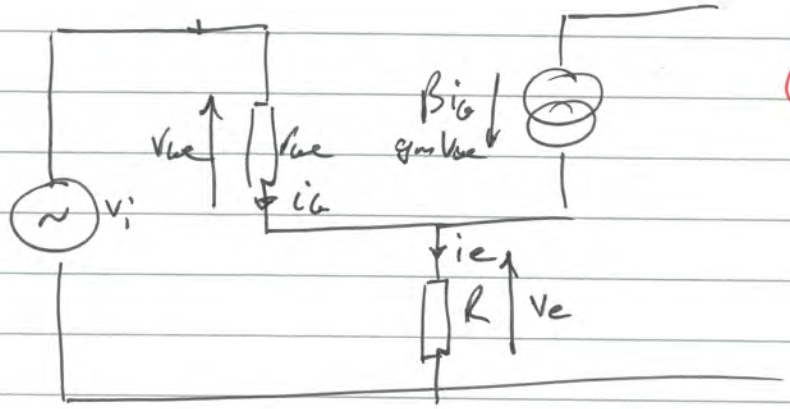
- T_5 REDUCES THE BASE CURRENT SUPPLIED BY T_1'S COLLECTOR MINIMISING ~~EMBAL~~ LOAD ON THE DIFFERENTIAL AMPLIFIER.
- T_5 & T_6 ARE THE "VOLTAGE AMPLIFIER" STAGE.
- T_5 & T_6 PROVIDE A VERY LARGE VOLTAGE GAIN WHICH PROVIDES MOST OF A_V
- T_5, T_6 & C SET ω_0 AND AFFECT THE COMPENSATION OF THE AMPLIFIER.

(1) FOR ANY OF THESE OR ANYTHING ELSE PERTINENT.

(6 IN TOTAL)

Q4 a

ii)



(1) - FOR A REASONABLE S.S. DIAGRAM THAT WOULD BE USEFUL IN A WELL CONSTRUCTED SOLUTION.

- ASSUME THE INPUT RESISTANCE OF T_G IS R IN THE DIAGRAM ABOVE.
- SUM I AT THE EMITTER:

$$i_e = i_G + \beta i_G$$

$$\frac{V_e}{R} = \frac{V_{be}}{r_{be}} + g_m V_{be}$$

(1) FOR SUM I AT E.

- SUM V ROUND THE INPUT LOOP.

(1) FOR SUM V ROUND I/P LOOP.

$$V_G = V_{be} + V_E$$

$$\frac{V_{be}}{r_{be}} + g_m V_{be} = \frac{V_{in} - V_{be}}{R}$$

$$V_{be} + \left(\frac{1}{r_{be}} + g_m + \frac{1}{R} \right) = \frac{V_{in}}{R}$$

$$i_G r_{be} \left(\frac{1}{r_{be}} + g_m + \frac{1}{R} \right) = \frac{V_{in}}{R}$$

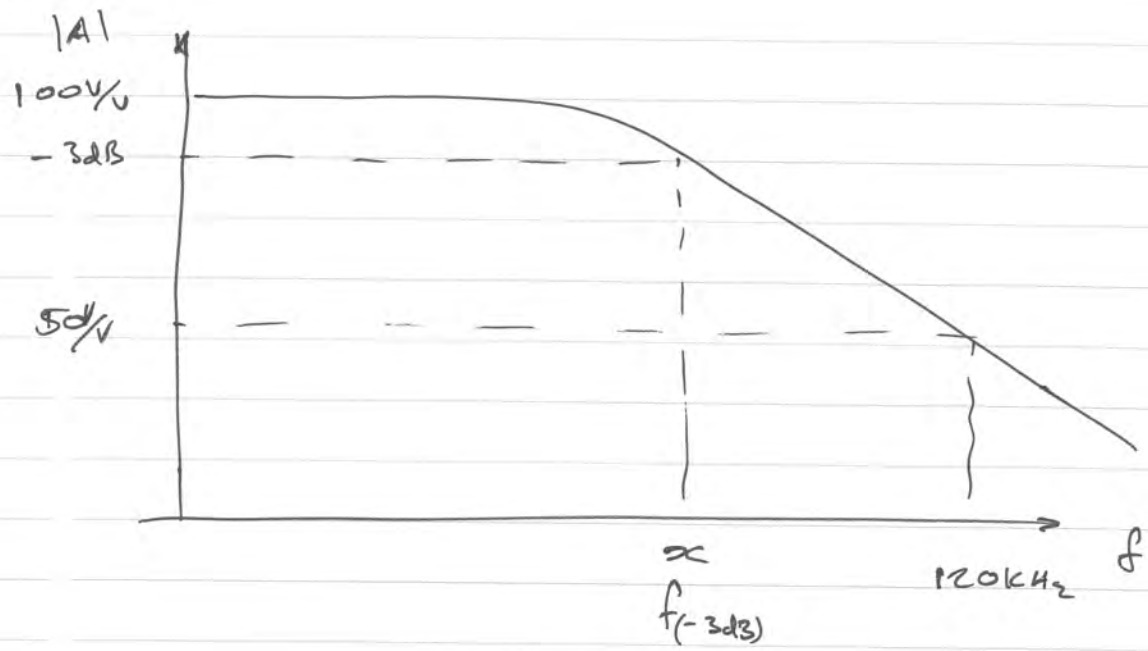
$$r_i = \frac{V_{in}}{i_G} = \left(1 + g_m r_{be} + \frac{r_{be}}{R} \right) R$$

$$= R + g_m r_{be} R + r_{be}$$

(1) FOR GETTING TO THIS RESULT

FHE 225

Q11 G.i



GAIN BANDWIDTH PRODUCT = CONSTANT (1)

$GBP = 120 \times 10^3 \times 50 = 6MHz$ (1)

$-3dB$ BELOW $100 V/V = 100 \cdot 10^{(-3/20)}$

$= 70.7946 V/V.$ (1)

$f_{-3dB} = \frac{GBP}{A_{(-3dB)}} = \frac{6 \times 10^6}{70.7946} = 84.75KHz$ (1)

SOLUTIONS ALONG THE LINES OF $100 V/V \times 120KHz$ CAN SCORE A MAXIMUM OF (2) MARKS.

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Q4 B

GBP = 100KHz.

$$V_o/V_i = K \cdot \frac{1}{1 + j\omega/\omega_0} = 100 \cdot \frac{1}{1 + j\left(\frac{f}{\left(\frac{100\text{KHz}}{100}\right)}\right)}$$

GBP; K

$$\text{At } 75\text{KHz}, \ |\text{gain}| = \left(V_o/V_i\right) = \frac{100}{\left(1 + \left(\frac{75}{1}\right)^2\right)^{1/2}}$$

$$= 1.3332 \text{ V/V}$$

$$\text{OR } \underline{2.498 \text{ dBV}}$$

$$\text{PHASE SHIFT} = \angle\left[V_o/V_i\right] = -\tan^{-1}\left(\frac{f}{f_o}\right) \quad (1)$$

$$= -\tan^{-1}\left(\frac{75}{1}\right) = -89.236^\circ \quad (1)$$

$$\text{OR } -1.557^c$$

iii) $3V_{RMS} = 3\sqrt{2}\, V_{pk} = 4.2426 \text{ V}$ (1)

MAX RATE OF CHANGE OF SINUSOID $V(t) = V_p \sin(\omega t)$

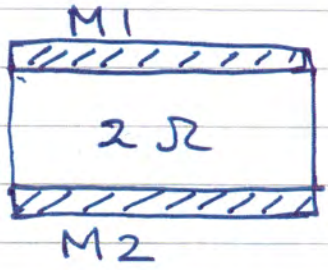
$\frac{dV(t)}{dt} = V_p \omega \cos(\omega t)$. THIS IS MAX WHEN

$\cos(\omega t) = 1 \quad \therefore \text{ MAX } \frac{dV}{dt} = V_p \omega$ (1)

EQUATE MAX $\frac{dv}{dt}$ WITH SLEW RATE...

$$f_{MAX} = \frac{S.R}{2\pi V_p} = \frac{0.05 \times 10^6}{2\pi\, 4.2426} = \underline{1.876 \text{ KHz}} \quad (1)$$

Q2



$\phi_{M1} = 4\,eV$

$\phi_{M2} = 1\,eV$

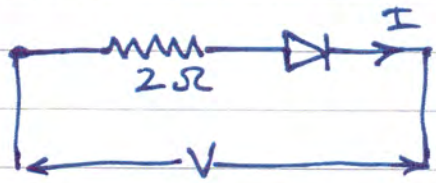
n-type semiconductor $\phi_s = 3\,eV$

M1/semiconductor = schottky contact (2)

M2/semiconductor = ohmic contact

When a large current of 500mA flows, the M1/s.c. junction is forward biased.

Equivalent circuit:



(2)

$$I = I_0 \left\{ \exp\left[\frac{e(1.5 - 0.5 \times 2)}{kT} \right] - 1 \right\}$$

$$0.5\,A = I_0 \times 2.25 \times 10^{8} \quad (4)$$

$$I_0 = 2.22 \times 10^{-9}\,A$$

When bias voltage is reversed, the M1/s.c. junction is reverse biased and only the small leakage current I_0 flows. (2)

Q26

$$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right] V_{ds} \quad \text{in unsaturated region}$$

When $V_{gs} - V_{ds} - V_T < 0$, or
$V_{ds} > V_{gs} - V_T$, saturation of Id occurs, I_{ds} (2)

$$I_{ds} = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{(V_{gs} - V_T)}{2}\right](V_{gs} - V_T)$$

$$= \frac{\mu_e C_g}{2l^2}(V_{gs} - V_T)^2 \qquad (4)$$

Gate and Drain connected together, so
$V_{gs} = V_{ds}$, $\frac{\mu_e C_g}{l^2} = 4\times10^{-4}\,A\,V^{-2}$, $V_T = 2V$

$I_d = 0$ when $V_{ds} = 1V$ as V_{ds} (or V_{gs}) $\leq V_T$
and no channel can form (2)

When $V_{ds} = 3V$, $V_{gs} = 3V$

$$I_d = \frac{4\times10^{-4}}{2}(V_{gs} - 2)^2 = 2\times10^{-4}\,A \qquad (2)$$

When $V_{ds} = 4V$, $V_{gs} = 4V$

$$I_d = \frac{4\times10^{-4}}{2}(4 - 2)^2 = 8\times10^{-4}\,A \qquad (2)$$