EPCEM Microsystem Packaging Examination Model Answers 2007

1a.
Power distribution: supply power current to the chip. **Signal distribution:** connecting electrical and optical signals from chip to chip or to external devices. **Heat dissipation**: remove heat from the devices/chips, to have optimum performance, make system reliable. **Protection**: protect devices or chips from environmental or mechanical damage

1b.
Wire Bonding
Advantages
- Simple process
- Relatively inexpensive lead frame and tooling
- Easy to inspect and test (wire pull)
- Good for low volume, one-off production

Disadvantages
- Large Packages
- Mechanical and Thermal damage
- Oxidized bond pads
- Extrusion of metal from bond pads
- Stresses. Long term reliability

TAB
Advantages
- Smaller bond pad compared to wire bonding technology ~ 100 μm
- Increase in production rate, lower labour costs
- Less variations in bond geometry
- Stronger and more uniform inner lead bonding strength
- Better electrical performance (noise and frequency, higher I/O counts (up to 850 pins) and lighter weight.
- Greater densities are achievable and the chip can be attached in a face-up or face-down configuration

Disadvantages
- IC specific. Each die must have its own tape patterned for its bonding configuration
- Time and cost of designing and fabricating the tape and the capital expense of the TAB bonding equipment.

Wire bonding has low (zero) cost tooling and is therefore perfect for prototyping.

1c.
i. I/O's = a gates^b and the a and b coefficients are 0.2 and 0.6 respectively.
Simple calculation: 2091 I/Os.

ii. Circumference of chip = 80 mm, hence average spacing = 80/2091 = 38 μm.

iii. Bond pad sizes below 50um are difficult in production.

1d.
Flip Chip solder bump

Advantages
The chip is directly bonded to the PCB and then encapsulated: short interconnection lengths, low resistance and impedance. Good mechanical stability
High density interconnects, 2D array of interconnects.
Technique is compatible with high frequency operation
Less expensive than wire bonding for high connections counts
Very small "package" leads to high density
Interconnection is made by heating and reflow

2a.
Electrical Power : Optoelectronic devices are generally quite inefficient, need high current drives. **Signal In/Out** Semiconductor Emitter generates light, which needs to get out. **Temperature Control** Inefficiency of lasers lead to high power dissipation. Output power and wavelength change with temperature. Heat sinking is critical. **Protection** Complex and accurate alignment needs to be preserved. Moisture can damage device, lead to absorption of light

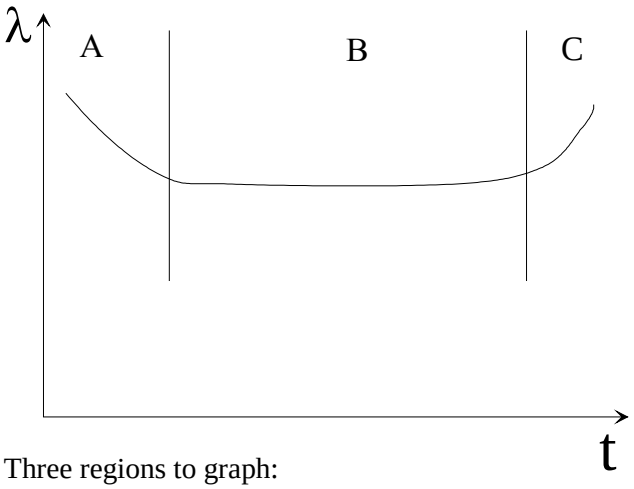
VCSEL- on chip geometry makes testing and packaging simple. No complex pick & place. Fiber alignment greatly simplified.

2b.
$R_{th} = L/k.A$ (°C/W) and $\Delta T = Q \, . \, R_{th}$

Area of chip = 1 x 5 mm = $5x10^{-6}$ m^2
200 µm indium R = 0.5 °C/W
3 mm SiN. R = 9.2 °C/W
10 mm aluminium. R = 9.3 °C/W

Q = 5W
Delta T= 5(0.5 + 9.2 + 9.3 + 0.5) = 97.5 °C
Therefore device temperature = 25 +97.5 = 122.5 °C

2c.



Three regions to graph:

A. High "early failures" or "Infant Mortality" due to manufacturing defects

B. “Midlife” or “Steady state” period of low and generally constant failure rate

C. “Final” or “wear out” period

Use burn in, short accelerated testing, to deal with infant mortality. Less returns for the company to deal with.

2d.

i. It is impossible to test the required reliability under normal operating conditions and therefore this necessitates means to accelerate the mechanisms that cause devices to fail.

Stresses: temperature, voltage, current, temperature cycling to accelerate mechanical failure of chips and assembly package, Humidity, Mechanical stresses, vibration.

ii. Highly Accelerated Steam and Temperature (HAST). Determines the moisture resistance capability and can detect similar failure mechanisms found in Life Test. In addition, it can detect electrolytic and chemical corrosion. HAST tests useful for immediate feedback and corrective action. Test Conditions: 120°C, 85% RH, biased,100 hrs.

iii. $R = R_0 \exp(-E_a / k_B T)$

time (t)= 1/rate

$$\frac{t_1}{t_2} = \frac{R_2}{R_1} = \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$$\ln(\frac{t_1}{t_2}) = \frac{E_a}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

t1 must be 5000 hours or less

ln (1E5/5E3)=2.99

E_a/k_B= 5797

$$\ln(\frac{t_1}{t_2}) / \frac{E_a}{k_B} = 0.00052$$

T_1=25^{o}C = 298K $1/T_1$= 3.355E-3

T2= 1/(0.00335-0.00052)- 353K=80^{o}C

3a.

QFP construction:

Glue die to die paddle. Wire bond pads to lead frame. Encapsulate in epoxy. Trim tie bar. Shape leads. Test.
Attachment to PCB:
Screen-print solder paste onto PCB bond pads. Place chip onto pads. Reflow solder process: preheat, soak, reflow cool.

3b.
Switch to lead free solder implies:
More expensive raw materials (silver, copper, etc rather than lead)
Often non-eutectic composition, therefore different crystal structure of solder – possibly brittle.
Generally higher melting point, therefore higher energy requirements and more stresses on components. Old reflow ovens may need replacing
Lots of different compositions – may be incompatible.

3c.
$T_{ambient}$ = 20 °C, T_{max} (Si) = 125 °C therefore ΔT = 125-20 = 105 °C
$R_{ja} = \Delta T/Q$ = 105/5 = 21 °C/W
$R_{ja} = R_{jc} + R_{ca}$ therefore $R_{ca} = R_{ja} – R_{jc}$ = 21 – 19 = 2 °C/W
From graph, required velocity = 3000 m/h
Assume fan diameter = 4cm (same as chip) therefore:
Volume flow rate = π x $(0.02)^2$ x 3000 = 3.8 m^3/h

3d.
Fan fails - therefore natural convective cooling. From fan curve R (v=0) = 8°C/W.
Therefore R_{ja} = = $R_{jc} + R_{ca}$ = 19 + 8 = 27 °C/W
Therefore $Q = \Delta T/R_{ja}$ = 105/27 = 3.9 W
Alternative cooling strategies: Peltier cooler. Heat pipe.

4a.
Partition design across PCBs
Choose IC packages and connectors
Simulate logic and interconnects
Complete schematics
Layout PCB
Verify design rules
Fabricate and test prototype
Fabricate final PCB

4b.
SMT packages smaller than PTH, therefore PCB smaller
Possible to mount SMT components on both sides of PCB.
6 layer PCB allows for power and ground planes and directional routing on different layers.
Blind, buried and through vias possible rather than just through vias, therefore space saving.

4c.

$$Z = \frac{87}{1.41 + \sqrt{\varepsilon_r}} \ln\left(\frac{6h}{0.8w + t}\right)$$

Therefore w = 1.25 (6h/E – t) where $E = e^{Z/87(1.41+\varepsilon_r^{0.5})}$
Assuming h = 100 µm, t = 1 µm gives w = 100 µm.

4d.

Inductive crosstalk: current change on aggressor causes current change on victim
Capacitive crosstalk: 2 tracks act as parallel plate capacitor. Voltage change on aggressor causes voltage change on victim.
Reduce effects by maximising spacing between conductors and using high ε_r dielectric.