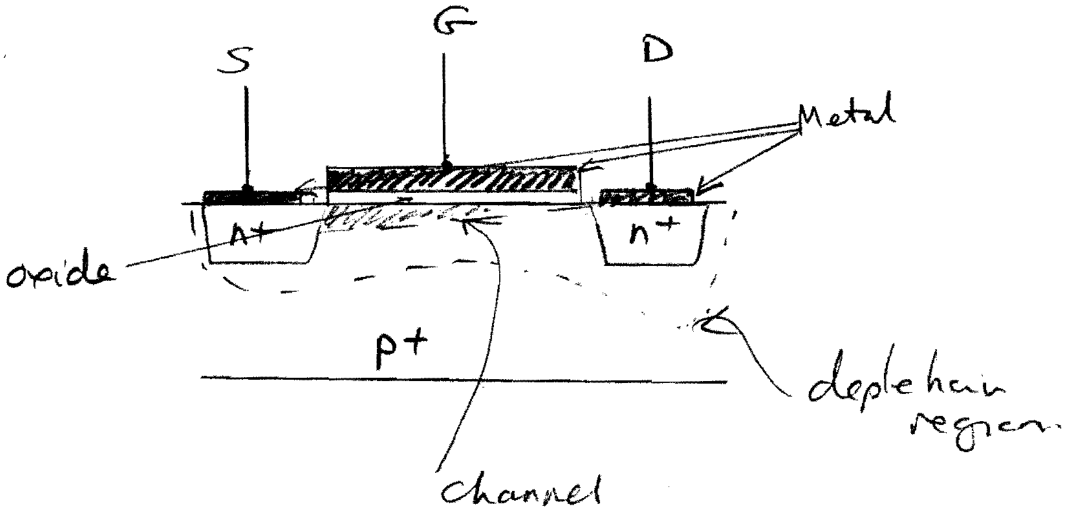
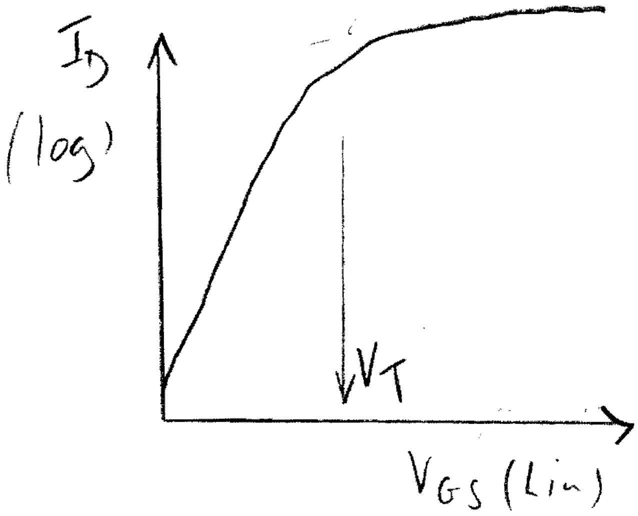
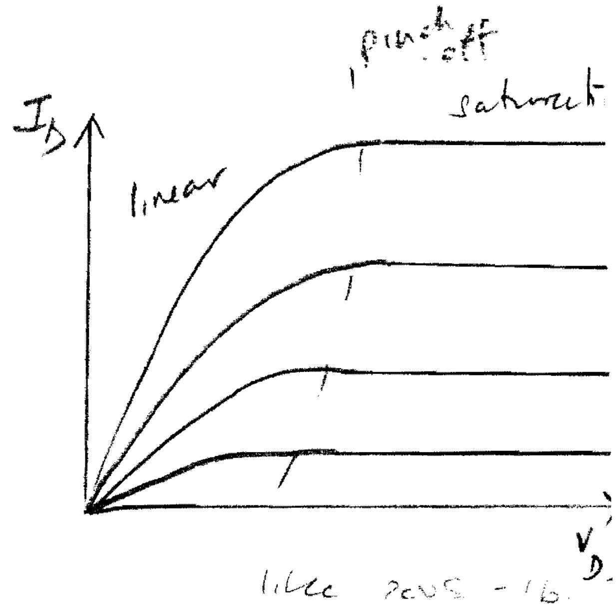
1a.



1b





1c. Capacitance $= \dfrac{\varepsilon_s \varepsilon_0 A}{d}$ C_{ox} is per unit length

so $C_{ox} = \dfrac{\varepsilon_s \varepsilon_0}{d} = \dfrac{3.9\times 8.85\times10^{-12}}{20\times10^{-9}}$.

$= 1.726\times10^{-3}$.

$$V_T = -0.32 + 2\times0.35 + \frac{\sqrt{2\times1.6\times10^{-19}\times12\times8.85\times10^{-12}\times10 \times 2\times0.35}}{1.726\times10^{-3}}$$

$$= -0.32 + 0.7 + 0.283 = \underline{0.663}$$

1d 2008 q2

$I_d(2.5) - I_d(1.5) = 80\mu A$

$= \frac{Z\mu C_{ox}}{L} V_{DS}\left[V_{GS_2} - \cancel{V_T} - \frac{\cancel{V_{DS}}}{\cancel{2}}\right] - \left[V_{GS_1} - \cancel{V_T} - \frac{\cancel{V_{DS}}}{\cancel{2}}\right]$

V_T is cancelled.

$= \frac{Z\mu C_{ox}}{L} V_{DS}\left[V_{GS_2} - V_{GS_1}\right]$

$[= 1.0]$

So $80\mu A = \frac{Z\mu C_{ox}}{L} 0.1 [1]$

$800\times10^{-6} = \frac{Z\mu C_{ox}}{L}$ $\mu = \frac{800\times10^{-6} \times L}{Z C_{ox}}$.

$\frac{800\times\cancel{10^{-6}} \times 0.1\times10^{-6}}{1\times10^{-3} \times 1\times\cancel{10^{-6}}}$ $\frac{80\times10^{-6}}{1\times10^{-3}} = 0.08$ $m^2V^{-1}s^{-1}$

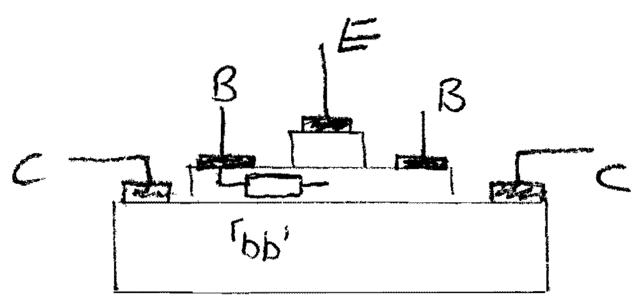
Electron bulk mobility $= 0.15\ m^2 V^{-1} s^{-1}$

value is about half this value.

Mobility reduced due to channels proximity to surface and interface with the oxide - scattering losses from interface charges.

2.

a)



$r_{bb'}$ - Base access resistance - lateral resistance present between the base contact and the centre of the emitter

r_π is the input dynamic resistance $= \left(\dfrac{dI_E}{dV_{BC}}\right)^{-1}$

$= \dfrac{qI_e}{KT}$.

r_o is the output ~~cond~~ resistance $\left(\dfrac{dI_C}{dV_{CE}}\right)^{-1}$

This occurs as a result of the Early effect

Physical origin comes from an increase in the collector-base depletion width, effectively shortening the base width. Gives an increase in I_C for an increase in V_{CE}, whereas at saturation we would expect no such increase.

2b. Input $i_p = i_{bo} + jwC_{B'e}V_{B'e}$

o/p $i_c = g_m V_{B'e}$

$$\text{gain} = \frac{o/p}{i/p} = \frac{\cancel{g_m V_{B'e}}\ i_c}{i_{Bo} + jwC_{b'e}V_{B'e}} = h_{fe}$$

$$h_{fe} = \frac{i_c}{i_{Bo} + jwC_{b'e}V_{B'e}} = \frac{1}{\frac{i_{bo}}{i_c} + \frac{jwC_{B'e}V_{B'e}}{i_c}}$$

$\beta = i_c / i_{bo}$ dc current gain $i_c = g_m V_{B'e}$ from above.

$$h_{fe} = \frac{1}{1/\beta + \frac{jwC_{b'e}}{g_m}}$$

At low frequency $w \to 0$ $1/\beta \gg$ 2nd term

$h_{fe} \simeq \beta$.

High freq. $1/\beta \ll$ 2nd term

$$h_{fe} = \frac{g_m}{wC_{B'e}}.$$

2D cont.

using high freq expression

$$h_{fe} = \frac{g_m}{\omega C_{b'e}} = 1$$ (when $f \to f_T$

or
we can say
when
$\omega \to \omega_T = 2\pi f_T$.

So $\frac{g_m}{\omega C_{b'e}} = 1 = \frac{g_m}{2\pi f_T C_{b'e}}$

$$f_T = \frac{g_m}{2\pi C_{b'e}}.$$

For a high f_T require high g_m value
high mobility
and/or a small value of $C_{b'e}$.

2bc Differences HBT versus BJT.

HBT has a wide gap emitter, chosen to have a reduced barrier height for electrons compared to that for holes at the EB junction

As a consequence the base doping can be increased reducing the base access resistance.

We may also make use of a narrow gap base with higher electron mobility.

$r_{bb'}$ will be reduced considerably by the higher base doping allowed in the HBT

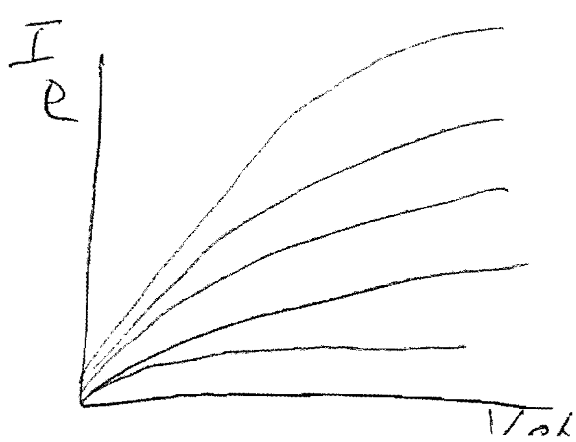
r_o will be increased since the depletion of the base is reduced due to the higher doping

r_π is unaffected.

Characteristics

f_{max} will be increased due to the reduction in $r_{bb'}$

output characteristics will take on a greater linear component



2d (contd)

GaAs $E_g = 1.43$

AlAs $E_g = 2.16$

$Al_{.5}Ga_{.5}As = 1.795$

$\Delta E_g = 1.795 - 1.43 = 0.365\text{eV}$

$\Delta E_c = 0.3 \times 0.365\text{eV} = 0.1095\text{eV}$

$\Delta E_v = 0.7 \times 0.365\text{eV} = 0.255\text{eV}$

Barrier for holes > Barrier for electrons.

Effective at suppressing hole current from base

Relatively small barrier for electrons from e → b.

3a Moore's Law - doubling of the density of transistors on an IC every 18 months (2 years in Moore's original statement).

Design philosophy has been scaling device dimensions reduction in device size giving improvement in speed and packing densities

(i) Voltage - Low operating voltage needed to reduce power dissipation. Limited by V_T of MOSFET, which itself is dependent on interface charge + channel doping. Over the years V_T has reduced from 3.5V to around 300mV today.

(ii) Oxide Need to maintain C_g when scaling down device size otherwise I_D and g_m would be reduced.

$I_D + g_m \propto \frac{1}{d_{ox}}$. However cannot be reduced indefinitely due to Quantum mechanical tunnelling through the oxide. SiO_2 reached its lower thickness limit several years ago. Now the trend is to use High K refractory metal oxides eg: HfO_2 to allow a somewhat thicker oxide.

(iii) Gate length

Reducing gate length increases g_m, I_D and improves the high frequency response. Over the years the

3a (cont)

gate length has been reduced from several 10's of μm to around 20nm in the latest processors.

Limits

Voltage - Logic swing needs to be a few KT to be above thermal noise limits. This sets a fundametal minimum of about 100mV. Practical limit is somewhat higher and is due to V_T variations which are caused by random positioning of dopant atoms or impurities/defects. As a result V_T varies from device to device. Clearly $V_S \gg V_T$ for all devices on an IC.

Oxide

Quantum mechanical tunnelling sets a limit to the oxide thickness ~1nm, otherwise the gate leakage becomes too high. High k has been very successfully employed and even higher k materials are available and are being investigated. Limit may be when we exhaust the list of new materials

Gate lengths

Fundamental limits - as we approach the 10nm range transport becomes ballistic and our conventional picture of the MOSFET breaks down. In the few nm range QM tunneling directly between source and drain will become very significant.

We are now very close to the limits of optical lithography even using the current EUV sources. Alternative methods such as X-ray and e-beam will have to be sought. Although e-beam has a capability down to 1nm it has not been the technology of preference for the IC industry due to its relatively slow write speed.

CMOS Alternatives a number discussed in lectures, like SET, Carbon (nanotubes, graphene), All optical etc.

3b) $C = \frac{\varepsilon_r \varepsilon_0 A}{d} = \frac{3.9 \times 8.85 \times 10^{-12} \times 45 \times 100 \times 10^{-18}}{2 \times 10^{-9}}$

$= 7.76 \times 10^{-17}$ F

$P = \frac{1}{2} \, 0.5 \times 3 \times 10^{9} \times 7.76 \times 10^{-17} \times (1.1)^2$

$= \cancel{1.408 \times 10^{-7}}$ $\quad 7.04 \times 10^{-8}$

$\times 1 \times 10^{9}$ Transistors $= 70$W

Static power dissipation is due to gate leakage. The magnitude for an individual MOSFET is low, typically < 1nA yet integrated over a large number of devices this becomes significant. V_g is not zero, but less than V_T to allow rapid switching. Power is therefore non zero.

3c Transit time $f_T = \frac{1}{2\pi\tau}$

$\tau = V/L$

At pinch-off $V_{DS} = V_{GS} - V_T = 3.5 - 2V$
$= 1.5V$

0.1µm gate $E = \frac{1.5}{0.1\times10^{-6}} = 1.5\times10^{7}\ V\,m^{-1}$
$1.5\times10^{4}\ kV\,m^{-1}$
$= 150\ kV.cm^{-1}$

10µm gate $\frac{1.5}{10\times10^{-6}} = 1.5\ kV\ cm^{-1}$

For 0.1µm $v \to 1\times10^{5}\ m.sec$ (V_{sat})

10µm $v \to 1.76\times10^{4}\ m\,sec.$

$\tau_{0.1} = \frac{1\times10^{5}}{0.1\times10^{6}} = 1ps$

$\tau_{10} = \frac{1.76\times10^{4}}{10\times10^{6}} = 1.76ns$

4a) $f_T = \frac{1}{2\pi\tau_{EC}}$ $\tau_{EC} = \underbrace{\tau_{BE} + \tau_{BC}}_{\text{capacitance Related}} + \tau_B + \tau_C$

τ_{BE} = Time required to charge the base-emitter junction Relates to C_{BE}

τ_{BC} : Time required to charge the base-collector junction - Relates to C_{BC}

$\tau_B + \tau_C$ = resistance related

Reduce τ_{BE} - Increase I_E or reduce C_{BE} by reducing the emitter doping

Reduce τ_{BC} - increase I_C or reduce C_{BC} again by reduced doping

Reduce τ_B, τ_C - reduce length or increase doping (somewhat in conflict with above)

b) $\tau_{EC} = \tau_B + \tau_C$ - told others are not significant

$\tau_B = \frac{W_B^2}{2D_e}$ given $\tau = \frac{W_C}{2V_{st}}$ student need to remember or work out.

so $\tau_{EC} = \frac{(0.2\times10^{-6})^2}{2\times0.026} + \frac{0.5\times10^{-6}}{2\times1\times10^5}$

$7.69\times10^{-13} + 2.5\times10^{-12} = 3.27\,ps$

$f_T = \frac{1}{2\pi\tau_{EC}} = 48\,GHz$

4c Avalanche condition

$$\int_0^L \alpha(E)\,dx = 1. \qquad \text{ok if } \alpha = \beta.$$

$$\frac{dE}{dx} = \frac{eN_D}{\varepsilon} \qquad dx = \frac{\varepsilon}{eN_D}\,dE$$

$$\frac{\varepsilon \times 10^{-24}}{e\,1\times10^{21}} \int E^4\,dE = 1.$$

$$\frac{\varepsilon \times 10^{-24}}{e\,1\times10^{21}} \frac{E^5}{5} = 1.$$

$$\frac{12.9 \times 8.854\times10^{-12} \times 10^{-24}}{1.6\times10^{-19} \times 1\times10^{21}} \frac{E^5}{5} = 1$$

$$1.425\times10^{-37}\,E^5 = 1.$$

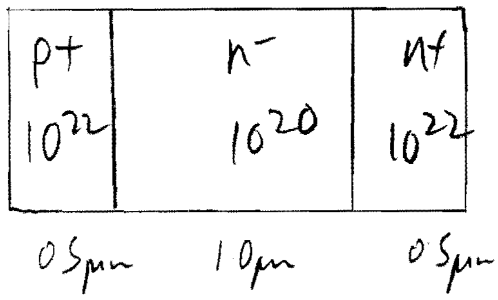
$$E = \sqrt[5]{7.015\times10^{36}}$$

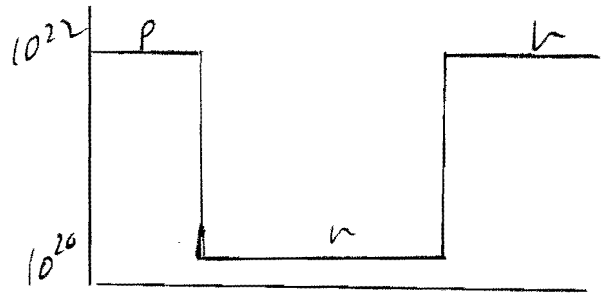
$$E = 2.34\times10^{7}\ \mathrm{V\,m^{-1}}$$

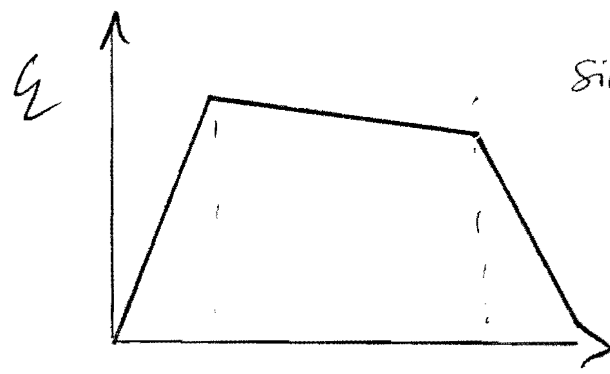
$$L = 1\,\mu m \qquad \underline{V = 23.4\,V}$$

4(d)

ImPATT







Since $\frac{\partial E}{\partial x} = \frac{\rho}{\varepsilon_r \varepsilon_0}$.

Transit time.

This is a high field device so $V \to V_{sat}$

$$\tau = \frac{2L}{V_{sat}} = \frac{2 \times 1 \times 10^{-6}}{1.1 \times 10^{5}} = 18.1\,\text{psec}$$

$$f = \frac{1}{2\pi\tau} = 8.8\ \text{GHz}$$

Voltage need to put $\mathcal{E}$ above breakdown field

$\mathcal{E} = 3 \times 10^{7}\ \text{V.m}^{-1}$

$d = 1\mu m$ $\quad 3 \times 10^{7} \times 1 \times 10^{-6} = 30V$