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# EEE331 Analogue Electronics

## 3rd lecture:

- common emitter with feedback resistance
- 2 transistor circuit elements:
  - Darlington pair
  - Cascode pair
  - differential pair (introduction)



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**summary of last lecture: single BJTs and their voltage gains**

- common emitter: $G = -g_m(r_{CE}||R_L) \approx -g_m R_L$
  used as inverting amplifier
- common base: $G = g_m R_L$
  used as fast switch
- emitter follower: $G = \dfrac{(\beta+1)R_L}{(r_{BE}+\beta+1)R_L}$
  $\approx g_m R_L/(1+g_m R_L) \approx 1$
  used as buffer

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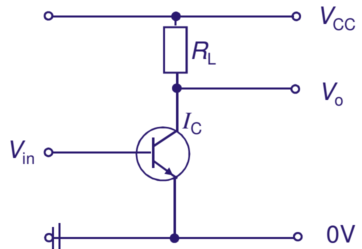
**common emitter (CE) BJT: situation without bias**




$r_{CB}$ varies from device to device

$g_m$ depends on bias & temperature

transconductance: $g_m = \Delta I_C / \Delta V_{in}$

consider input voltage: $V_{in} = V_{BE\ bias} \pm \Delta V_{BE}/2$

gives collector current: $I_C = I_{CB} \pm g_m \Delta V_{BE}/2$

changes collector voltage: $V_o = V_{CC} - I_C R_L$

$= V_{CC} - I_{CB} R_L \mp g_m R_L \Delta V_{BE}/2$

$V_{o,bias}$=const. $\Delta V_o$ varying

hence voltage gain: $\boxed{\Delta V_o / \Delta V_{in} = -g_m R_L}$

note: $g_m$<0 inverts signal and **is a function of $V_{BE\ bias}$**



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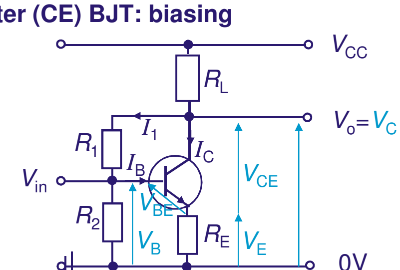
**common emitter (CE) BJT: biasing**




aim: use resistors to establish **constant bias conditions** & control $I_C$

principle: large $R_E$ -> large $V_E$ -> $V_B = V_E + V_{BE} \approx V_E = R_E I_E$=const.

and **negative feedback** by $R_1$, $R_2$:

increase of $I_C$ -> smaller $V_C = V_{CC} - (I_1 + I_C) R_L$

-> smaller $V_B = V_{CC} - (I_1 + I_C) R_L - I_1 R_1$

-> reduces $I_C$ by $\Delta I_C = g_m \Delta V_B$

-> **stabilises $I_C$**

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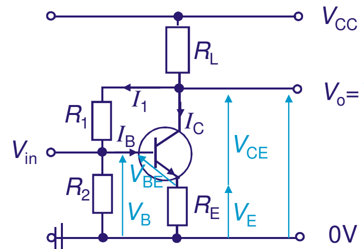
**common emitter (CE) BJT: biasing**




note for max. symmetrical swing of output voltage:
$V_C=V_B\,(R_1=0)\ldots\ V_{CC}\,(R_L=0)$
$=\frac{1}{2}\,(V_{CC}+V_E+0.7V)$

aim: calculation of output $I_C$

assume: $I_B$ negligibly small, $V_{BE}\approx 0.7V$, $h_{FE}>>1$ (i.e. $I_C\approx I_E$)

Kirchhoff's Voltage Law: $V_{CC}=I_1R_2+I_1R_1+(I_1+I_C)R_L$

$= I_CR_L + I_1(R_1+R_2+R_L)$ (i)

and also: $I_1R_2=V_B=V_E+V_{BE}=I_CR_E+0.7V$ (ii)

insert (ii) into (i) gives: $V_{CC}=I_CR_L+[I_CR_E+0.7V]/R_2\,(R_1+R_2+R_L)$

and solve for $I_C$: $\boxed{I_C=\dfrac{V_{CC}R_2-0.7V(R_1+R_2+R_L)}{R_2R_L+R_E(R_1+R_2+R_L)}}$ $\approx$ constant



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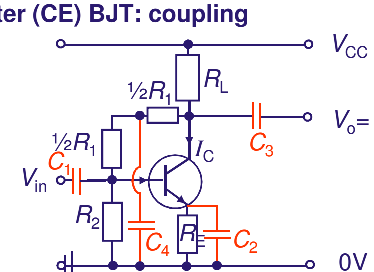
**common emitter (CE) BJT: coupling**




note on $C_2$ and $C_4$: shorten small a.c. signals to ground and so remove negative feedback by $R_1$ and $R_E$ on circuit gain

aim: getting mid-frequency signals in and out

use: capacitors for **coupling** (signal transfer) and **decoupling** (removal)

roles: $C_1$ couples signal from source to BJT base without allowing source to affect bias (or vice versa)

$C_2$ decouples emitter BJTnode (shortens emitter node to ground as far as small signals re concerned, prevents RE has same stabilisation effect on the signal as on DC bias conditions)

$C_3$ couples signal from output at collector node to the load

$C_4$ decouples mid-point of $R_1$

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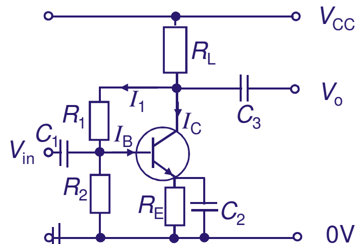
**common emitter (CE) BJT: voltage gain with bias**




aim: draw small signal circuit by replacing
- all d.c. voltage sources by short circuits (0Ω)
- all d.c. current source by open circuits (∞ resistance)
- all capacitors by short circuits
- $V_{CC}$ by direct connection to ground from signal's point of view



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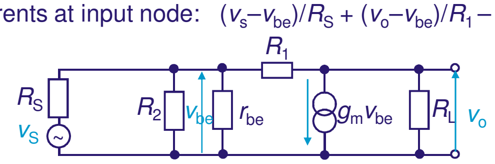
**common emitter (CE) BJT: voltage gain with bias**

sum currents at output node: $v_o/R_L + (v_o - v_{be})/R_1 + g_m v_{be} = 0$ (i)

sum currents at input node: $(v_s - v_{be})/R_S + (v_o - v_{be})/R_1 - v_{be}/R_2 - v_{be}/r_{be} = 0$ (ii)




aim: draw small signal circuit by replacing
- all d.c. voltage sources by short circuits (0Ω)
- all d.c. current source by open circuits (∞ resistance)
- all capacitors by short circuits ($C_4$ ignored here)
- $V_{CC}$ by direct connection to ground from signal's point of view

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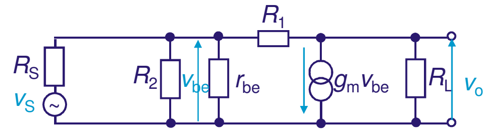
**common emitter (CE) BJT: voltage gain with bias**

sum currents at output node: $v_o/R_L + (v_o - v_{be})/R_1 + g_m v_{be} = 0$ (i)

sum currents at input node: $(v_s - v_{be})/R_S + (v_o - v_{be})/R_1 - v_{be}/R_2 - v_{be}/r_{be} = 0$ (ii)




solve (i) and (ii) for $v_{be}$, then equate to eliminate $v_{be}$:

$-v_o/[g_m(R_1||R_L)] \approx -v_o(R_1+R_L)/(g_m R_1 R_L - R_L) = v_{be}$

$= (v_s/R_s + v_o/R_1)(R_1||R_2||R_S||r_{be})$

$= v_s(R_1||R_2||R_s||r_{be})/R_s + v_o(R_1||R_2||R_s||r_{be})/R_1$

gives voltage gain

$\boxed{G = v_o/v_s = -R_1/R_s\{1 + R_1/[(g_m R_1||R_L)(R_1||R_2||R_s||r_{be})]\}^{-1} \approx -R_1/R_s\ 1/(1+g_m R_1) \text{ mostly independent from BJT for } R_1 << R_2, R_S, r_{be}}$

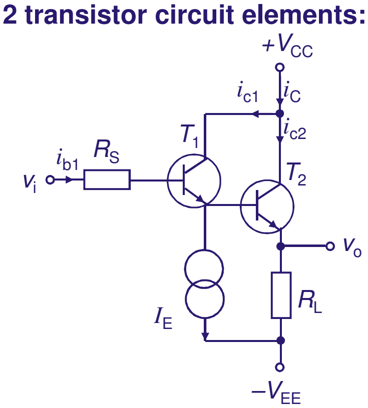
lim $R_1 \to \infty$: $G = -R_1/R_s\{1 + R_1/[(g_m R_L)(R_2||R_s||r_{be})]\}^{-1}$

$\approx -g_m R_L(R_2||r_{be})/(R_s + R_2||r_{be})$ independent of $R_1$ (no feedback)



# EEE331 Analogue Electronics

**2 transistor circuit elements: The Darlington pair**




- definition: two transistors $T_1$ and $T_2$ in CC mode with **collectors connected**
- current source (or resistor) establishes DC bias current $I_E$ for $T_1$ to ensure $\beta_1$ is large enough (not needed for s.s. circuit)
- for the composite transistor element:

$i_C = i_{c1} + i_{c2}$

$i_{c1} = \beta_1 i_{b1}$

$i_{c2} = \beta_2 i_{b2}$

$i_{b2} = i_{b1} + i_{c1} = (\beta_1+1) i_{b1}$

-> $i_{c2} = \beta_2(\beta_1+1)\, i_{b1}$

symmetrical in $i$=1,2

-> current gain: $\boxed{\beta_{tot} = i_C/i_{b1} = \beta_2(\beta_1+1) + \beta_1 \approx \beta_1\beta_2}$

voltage gain:

$$\boxed{v_o/v_i = \frac{R_L}{R_L + r_{be2} + [r_{be1} + R_S/(\beta_1+1)]/(\beta_2+1)}}$$

is ≈1 for large $R_L$ and $\beta_1, \beta_2 >> 1$

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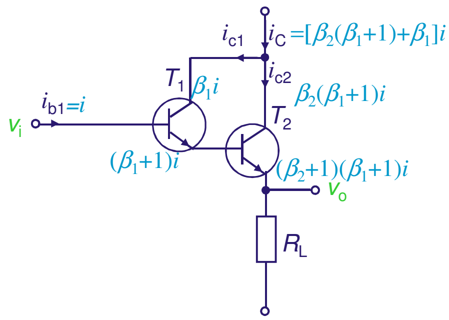
## 2 transistor circuit elements: The Darlington pair




- work out small signal currents and voltages to determine the input resistance
- at output:
  $v_o= R_L\,(\beta_2+1)(\beta_1+1)i$
  and also:
  $v_o=v_i-(\beta_1+1)i\,r_{be1}$
  $-(\beta_2+1)(\beta_1+1)i\,r_{be2}$
- equate and get
  $r_i=v_i/i$ ...



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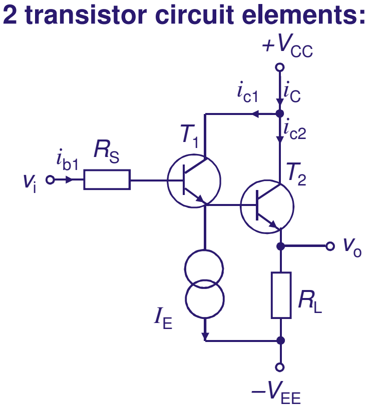
## 2 transistor circuit elements: The Darlington pair




- definition: two transistors $T_1$ and $T_2$ in CC mode with **collectors connected**
- input resistance:
  $$\boxed{\begin{aligned} r_i &=(\beta_1+1)[r_{be1}+(\beta_2+1)(r_{be2}+R_L)] \\ &\approx(\beta_1+1)(\beta_2+1)(r_{be2}+R_L) \text{ is large}\end{aligned}}$$
- output resistance:
  $r_o=R_L \,||\, \{r_{be2}+[r_{be1}+R_S/(\beta_1+1)]/(\beta_2+1)\}$
  $\approx r_{be2}$ is small
- **Both, input resistance and current gain are improved (enlarged)** compared to single transistor, which is very useful for BJTs (but not for MOSFETs for which both quantities are infinite anyway.)

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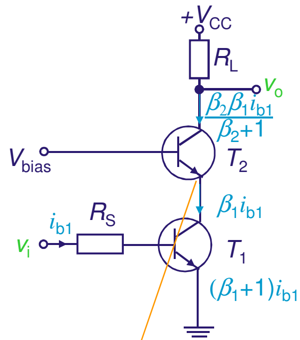
## 2 transistor circuit elements: The Cascode pair




- definition: two transistors with $T_1$ in CE mode driving $T_2$ in CB mode so that **emitter** of $T_2$ connected to **collector** of $T_1$
- consider output current:
  $i_o=i_{C2}=\beta_2\beta_1 i_{b1}/(\beta_2+1)\approx\beta_1 i_{b1}$, hence current gain:
  $\boxed{i_o/i_{b1}=\beta_2\beta_1/(\beta_2+1)\approx\beta_1}$ is rather small
- consider output voltage:
  $v_o=-i_o R_L=-\beta_2\beta_1 i_{b1} R_L/(\beta_2+1)$
  consider input voltage:
  $v_i=[R_S+(\beta_1+1)r_{be1}]i_{b1}$, hence voltage gain:
  $$\boxed{v_o/v_i=-\beta_2\beta_1 R_L/\{[R_S+(\beta_1+1)r_{be1}][\beta_2+1]\} \approx-\beta_1 R_L/(R_S+\beta_1 r_{be1})}$$ can be high
- **CE stage of $T_1$ sees only load of $r_{be2}$<<$R_L$**, hence gain ($=g_m R_L$) and associated Miller effect are much smaller for cascode compared to normal CE circuit: good high-f amplification!
- use also as level shifter in MOSFETs



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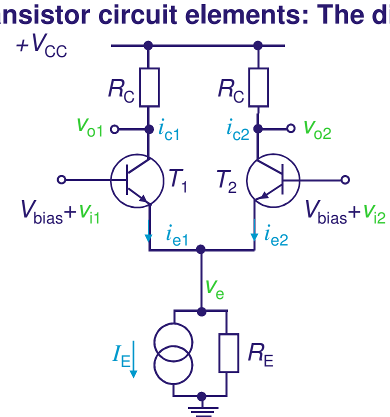
# EEE331 Analogue Electronics

## 2 transistor circuit elements: The differential pair (emitter coupled pair)




- definition: **two transistors with joined emitters** and biased by constant current source
- operation principle:
  consider $v_{i1}=v_{i2}+\Delta v$,
  this increases $i_{e1}$ by some $\Delta i$,
  hence, as $i_{e1}+i_{e2}=I_E$=const.:
  $i_{e2}$ must decrease by same $\Delta i$,
  thus output for $i_c\approx i_e$:
  $\boxed{v_o^{diff}=v_{o1}-v_{o2}}$
  $=[V_{CC}-(i_c+\Delta i)R_C]-[V_{CC}-(i_c-\Delta i)R_C]$
  $\boxed{=-2\Delta i R_C}$
  is proportional to **current difference** through $T_1$ and $T_2$
- problem: for BJTs this is usually not proportional to **voltage difference**

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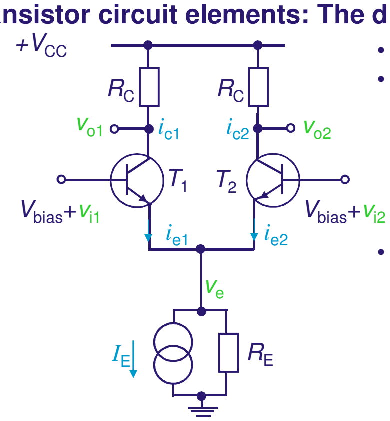
## 2 transistor circuit elements: The differential pair (emitter coupled pair)




- assume $R_E$, $r_{ce}\rightarrow\infty$, $r_b=0$
- use Ebers-Moll equations for $i_c(v_{be})$:
  $i_c=i_s \exp(v_{be}/V_{to})$
  with turn-on voltage of $V_{to}\approx0.7$eV for a Si BJT and some characteristic current $i_s$, hence
  $i_{c1}/i_{c2}=\exp(v_{i1}-v_{i2})/V_{to}=\exp(v_i^{diff}/V_{to})$
- also $v_{i1}-v_{be1}+v_{be2}-v_{i2}=0$
  and $i_{e1}+i_{e2}=I_E=(i_{c1}+i_{c2})/\alpha$
  where $\alpha=i_c/i_e=\beta/(\beta+1)$, hence:
  $i_{c1}/I_E=\alpha\, i_{c1}/(i_{c1}+i_{c2})$
  $=\alpha/(1+i_{c2}/i_{c1})$
  $=\alpha/[1+\exp(-v_i^{diff}/V_{to})]$
  and
  $i_{c2}/I_E=\alpha/[1+\exp(+v_i^{diff}/V_{to})]$





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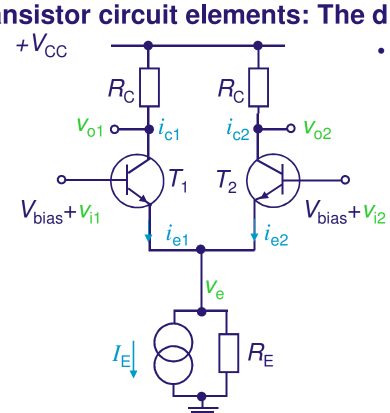
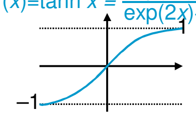
## 2 transistor circuit elements: The differential pair (emitter coupled pair)

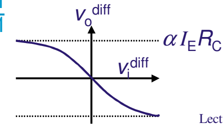



- $\boxed{v_o^{diff}=v_{o1}-v_{o2}}$
  $=-2\,{}^{1\!}/_{2}(i_{c1}-i_{c2})R_C$
  $=(i_{c2}-i_{c1})R_C$
  $=\alpha I_E R_C\{1/[1+\exp(+v_i^{diff}/V_{to})]$
  $-1/[1+\exp(-v_i^{diff}/V_{to})]\}$
  $\boxed{=\alpha I_E R_C \tanh(-v_i^{diff}/2V_{to})}$

where tanh $x$ is a function that is symmetrical about the origin and converges to unity for $x\rightarrow\infty$, i.e. we have a **linear relationship between output voltage difference and input voltage difference for small signals**!

$$f(x)=\tanh x=\frac{\exp(2x)-1}{\exp(2x)+1}$$



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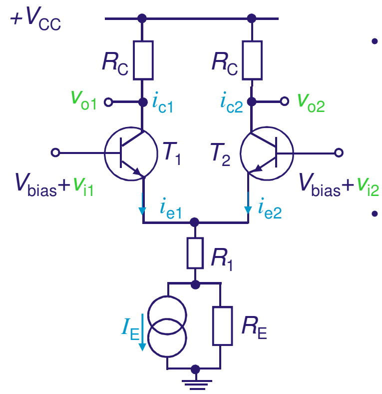
## 2 transistor circuit elements: The differential pair (emitter coupled pair)




- **note on emitter degeneration**: add $R_1$ to the joint emitters provides negative feedback: if $i_c$ rises, $i_e$ increases, thus also the voltage drop across $R_1$, which reduces the bias and thus drives $i_b$ and $i_c$ back.
- in detail: look at Ebers-Moll equation: $v_{be}=V_{to} \ln (i_c/i_s)$
  If one must provide higher base voltages to $T_1$ and $T_2$ to get the same $i_c$ with $R_1$ present, then this also means the non-linear $i_c(v_{be})$ regime begins only at higher voltage; i.e. ***R*₁ effectively extends the linear region**!



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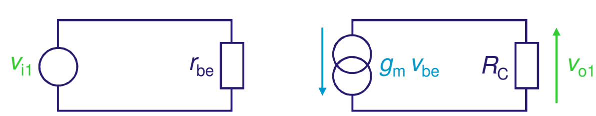
## 2 transistor circuit elements: The differential pair (emitter coupled pair)


**calculation of differential mode gain $A_{dm}$:**

- consider
  $v_{o1}\rightarrow v_{o1}+\Delta v$, $i_{c1}\rightarrow i_{c1}+\Delta i$, hence also
  $v_{o2}\rightarrow v_{o2}-\Delta v$, $i_{c2}\rightarrow i_{c2}-\Delta i$
- As total current $I_E$ into current source and resistor $R_E$ stays constant, no changes occur below the emitters of $T_1$ and $T_2$ and we can replace this part with a short circuit and only need to consider $T_1$ (no need to worry about $T_2$ since $T_1$'s emitter is tied to ground from small signal point of view). Thus get the differential mode half-circuit:




$v_{o1}=-g_m v_{be} R_C=-g_m v_{i1} R_C$
with $v_{i1}=-v_{i2}=v_i^{diff}/2$ and $v_{o1}=-v_{o2}=v_o^{diff}/2$,
hence $\boxed{A_{dm}=v_o^{diff}/v_i^{diff}=2v_{o1}/2v_{i1}=-g_m R_C}$

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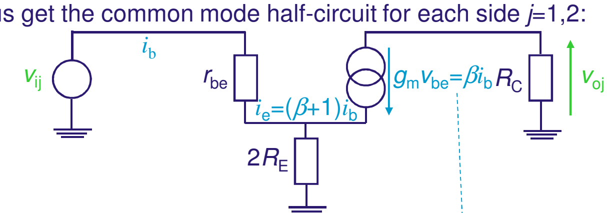
## 2 transistor circuit elements: The differential pair (emitter coupled pair)

**calculation of common mode gain $A_{cm}$:**

- replace single $R_E$ with two parallel branches, each with resistance $2R_E$
- As left and right halves of circuit are completely identical and the drives signals to both sides also, no large signal current will flow between emitters between $T_1$ and $T_2$. As there is no interaction between both halves, we can split circuit down the middle and consider just one half. Thus get the common mode half-circuit for each side $j$=1,2:




Kirchhoff's Law: $v_{ij} - i_b r_{be} - i_b(\beta+1)2R_E=0$, thus $i_b=v_{ij}/[r_{be}+2R_E(\beta+1)]$

Also: $v_{oj}= -\beta i_b R_C$

Put together: $\boxed{A_{cm}}=v_{oj}/v_{ij}= -\beta R_C/[r_{be}+2R_E(\beta+1)]= \boxed{\dfrac{-g_m R_C}{1+2g_m R_E(1+1/\beta)}}$



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## 2 transistor circuit elements: The differential pair (emitter coupled pair)

**common mode rejection ratio (CMRR)**:

- aim: for differential amplifier, maximise gain $A_{dm}$ in differential mode (= gain for opposite voltage signals) and simultaneously, minimise gain $A_{cm}$ for identical input voltages applied to both inputs
- use as a quality factor the common mode rejection ratio (CMRR) defined as the dimensionless ratio
  $\boxed{\text{CMRR}=|A_{dm}/A_{cm}|=1+2g_m R_E(\beta+1)/\beta}$
- CMRR increases with $g_m$, and as $g_m v_{be}=\beta i_b$ it is best to use BJTs with large $\beta$ and operate them at high current.
- **at high frequencies: $Z$=1/($j\omega C_{cb}$)** || **$R_C$** decreases $R_C^{eff}$ for small signals, which thus **reduces $A_{dm}$ (not $A_{cm}$ !) and thereby CMRR**.
- notes on differential amplifiers using FETs:
  - ~ **JFETS are better than MOSFETs** for this as they have lower noise.
  - – **Differential gain of FETs is lower** than for differential amps based on BJTs, due to smaller $g_m$.
  - \+ **FETs give much wider linear operation** than BJTs as current varies only like the square rather than exponentially with voltage.