Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2007-2008 (2 hours)

High Speed Electronic Devices 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Under saturation conditions ($V_D > V_P$) the expression for the transconductance, g_m, for a MESFET transistor can be written as:-

$$g_m = -\frac{aZqN_D\mu}{L}\left[1-\left(\frac{V_G}{V_P}\right)^{\frac{1}{2}}\right]$$

where the symbols have their usual meaning.

Define g_m in words only. Sketch a plan view of a typical FET, showing the shape of the source, drain and gate contacts with dimensions Z and L and explain physically why these particular shapes maximise g_m. **(8)**

b. To achieve a high cut-off frequency (f_T) in FETs it is necessary to have a large g_m. Explain why this is so by deriving f_T in terms of g_m and the gate capacitance. Explain what the resultant expression means physically. **(6)**

c. Calculate g_m and the cut-off frequency for a GaAs MESFET device with a channel thickness of 0.25 μm, a gate width and length of 500 μm and 0.75 μm respectively, a channel doping of 5×10^{16}cm^{-3}, a channel electron mobility of 0.4 m^{2}V^{-1}s^{-1} and a pinchoff and gate voltage of 2.14 V and 1.5 V respectively. **(6)**

2. a. Sketch the cross-section of an n-channel enhancement mode MOSFET showing clearly the bias arrangements, the gate, source and drain contacts, the depletion regions and the conducting channel for each of the following bias conditions:

(i) Gate-source and drain-source voltage = 0

(ii) Gate-source voltage greater than the threshold voltage and much greater than the drain-source voltage

(iii) Bias as in (ii) above except that the drain-source voltage is equal to the gate-source voltage minus the threshold voltage (channel pinch-off condition)

(9)

b. Carefully sketch the band diagrams which describe the bias conditions in (i) and (ii) above, showing the conduction and valence bands in relation to the Fermi level in the gate and semiconductor channel. **(6)**

c. A drain current of 100 µA and 160 µA flows in an n-channel MOSFET at gate-source voltages of 1.5 V and 2.5 V, respectively, and a drain-source voltage of 0.1 V (less than threshold). If the gate length and width is 0.2 µm and 2 mm respectively with a gate oxide capacitance of 1 x 10^{-6} Fm^{-2}, calculate the corresponding channel mobility. You may require the expression for the drain current in the linear region of a MOSFET given by:

$$I_D = \frac{Z\mu C_{ox}}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

Where the symbols have their usual meaning **(5)**

3. a. Figure 3a shows a simplified small signal equivalent circuit for a bipolar transistor. Explain the physical origin of the circuit components, using a sectional sketch of the bipolar transistor where necessary. **(8)**

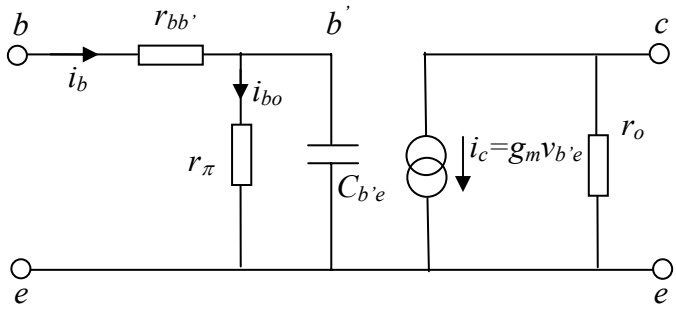

Figure 3a

b. Using figure 3a, derive an expression for the small circuit current gain, h_{fe}, as a function of frequency. Identify the low frequency and high frequency gain and, by setting the latter to unity derive an expression for the unity gain cut-off frequency, f_T, in terms of the parameters in the figure and from this interpret the total electron transit time through the device, τ_{ec}. **(8)**

c. What effect, if any, does $r_{bb'}$ have on f_T? Explain. **(4)**

4. **a.** The progress in technology which has resulted in an increase in complexity of CMOS ICs according to Moore's Law and the corresponding increase in operating speed, have up to now been largely due to scaling of device dimensions and voltages. For each of the following parameters, briefly comment on the consequence of reducing their size or value, in terms of how they contribute to this progress, what the ultimate limits are on scaling of each and how these limits may be overcome.

i. Voltage

ii. Oxide thickness

iii. Gate length

iv. Junction depth

v. Interconnects **(15)**

b. The power developed during a switching cycle in a MOSFET can be expressed as:

$$P_D = \frac{1}{2}\alpha C V^2 f$$

Where α is the switching probability, C is the total device capacitance, V is the supply voltage and f is the clock frequency. Calculate the average power density developed in an IC with a clock frequency of 3 GHz, supply voltage of 1 V and switching probability of 0.5. The gate dimensions are 0.09 μm x 5 μm, the oxide thickness is 10 nm and each device is spaced 10 μm apart as measured between the centre of the gates. Would this power density be suitable for portable application such as lap tops? ($\varepsilon(SiO_2) = 3.45 \times 10^{-11}$ Fm^{-1}) **(5)**

PAH / RAH