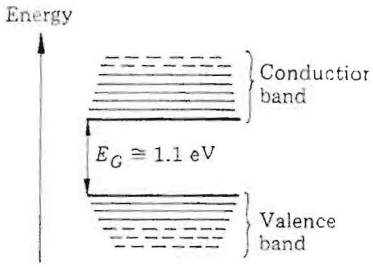
Solutions to EEE402/6042 YEAR 2010-2011:

Solution 1a.



For a metal E_g=0 and for insulator E_g is large > 5 eV. 1
If you heat a semiconductor the resistance increases. If you heat a metal it decreases. 1
In a semimetal, the valence and conduction bands join at some k points (ie graphene). 1

Solution 1b.

Four point probe or Van der Paaw (with diagrams). 2

$R_s = K_p(V/I)$ where K_p is a constant depending on configuration of probes and sample or for Van der Paaw

$$\exp(-\pi L\, R_A/R_S) + \exp(-\pi L\, R_B/R_S) = 1$$ 1

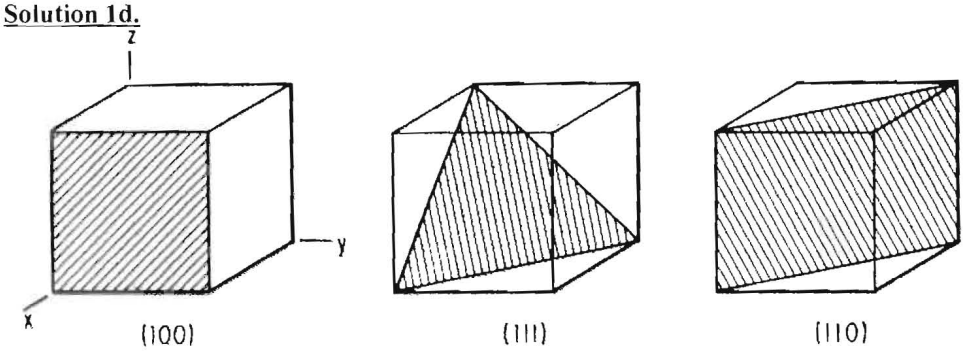
Solution 1c.

Silicon has a Diamond Cubic lattice (diagram). 1
Diagonal of a face is sqrt (2)*a.
Diagonal of cube is sqrt(3)* a=8*r.
No of atoms/unit cell=8.
vol of cube=x^3

packing density= $$8 * \frac{4}{3}\pi r^3 \Big/ (\frac{8}{\sqrt{3}} r)^3$$

=34% 5

Solution 1d.

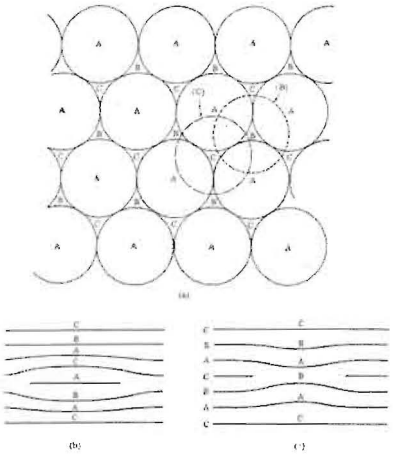


1
{} represent a family of planes. 1

Solution1e.

Any one of screw, edge, glissile or lomer dislocations. 2
a/2 [110] is commonly a burgers vector in diamond cubic. 1

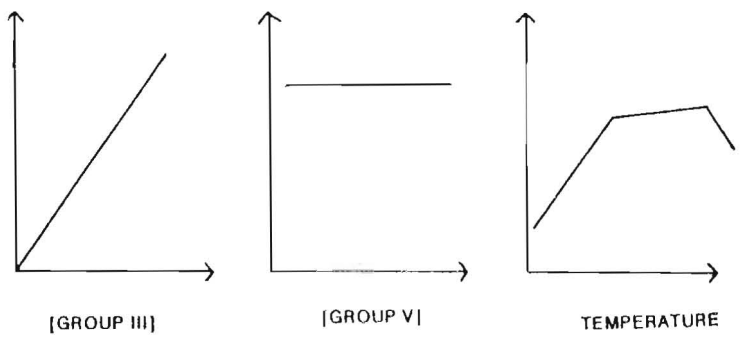
Solution 1f.



two types of fault
intrinsic: **missing** close-packed **plane** stacking ABCACABCABC.....
extrinsic: **extra** close-packed **plane** stacking ABCACBCABCABC.....
This is effectively a bilayer intrinsic fault. 3

Solution 2a:

(i)MBE layers can be grown at *lower temperatures* than for MOCVD
(ii) MBE is not limited by precursor decomposition kinetics
(iii) MOCVD employs a *simpler technology* than MBE
(iv) MOCVD does not require advanced DRV technology
(v) but, MOCVD does need substantial toxic gas handling facilities 2.5



MOCVD growth characteristics (Fig)

(i) Growth rate is controlled by the group **III** precursor concentration
(ii) Growth rate is little affected by the group **V** precursor concentration
(iii) Growth rate depends upon the temperature in ***three regimes***
(iv) Increase at low temperatures due to speeding up of reaction kinetics
(v) Intermediate regime limited by diffusion across boundary layer
(vi) Decrease at high temperatures due to desorption of group **V** element 2.5

Solution 2b.

The *Liquid Encapsulated Czochralski* (LEC) technique

(i) Ingots of these compounds produced by modified CZ method
(ii) But standard method cannot be used due to 'high vapour pressure' of Group **V** component:
(iii) ~ 100 kPa (1 at) for As in gallium arsenide
(iv) ~ 3,500 kPa (35 at) for **P** in gallium phosphide
(v) It would be possible to balance the loss of the Gr V component by applying these pressures of eg As and P over the melt in a pressure vessel.
(vi)However, quite dangerous to do this.
(vii)In practice, a layer of molten boric oxide (B_2O_3) is floated across the top of the melt in the crucible (typically BN).
(viii)This seals the melt against loss of Group V material.
(ix)It is still necessary to carry out the procedure in a pressure vessel in order to apply a high pressure of gas to balance the Group V vapour pressure under the boric oxide.

(x)But this can now be done in an **inert gas** such as argon (much safer)!

(xi) Could be possible to balance the loss of the Group V component by applying these pressures of As and P over the melt in a pressure vessel.

(xii)**Control of ingot dia. is by:**

a. ***in-situ*** radiography, **or** measuring change in ingot mass 4

Solution 2c. Autodoping is when impurity diffuses out into a growing epitaxial layer during growth.

Diffusion of impurity from substrate must be outpaced by layer growth: can be checked by calculating the characteristic impurity diffusion length. 2

Solution 2d.

Velocity = $v0[\exp(-EA/kT)]$

$= 3.68\times10^{8}\ [\exp(-2.76/8.617\times10^{-5}\times1073)]$

$=1.758\times10^{-8}$ cm/s.

Time required to regrow 2×10^{-5} cm:

$= 3\times10^{-5}/1.758\times10^{-8}$ s

$=1.7\times10^{3}$ s. 6

Solution 2e.

(i)The MBE growth process relies on the good mobility of deposited atoms on the heated substrate surface

(ii)Once again, for **III - V** growth, a substantial ***excess* of the group V** element is employed

(iii)Growth rate is controlled by the group III element concentration

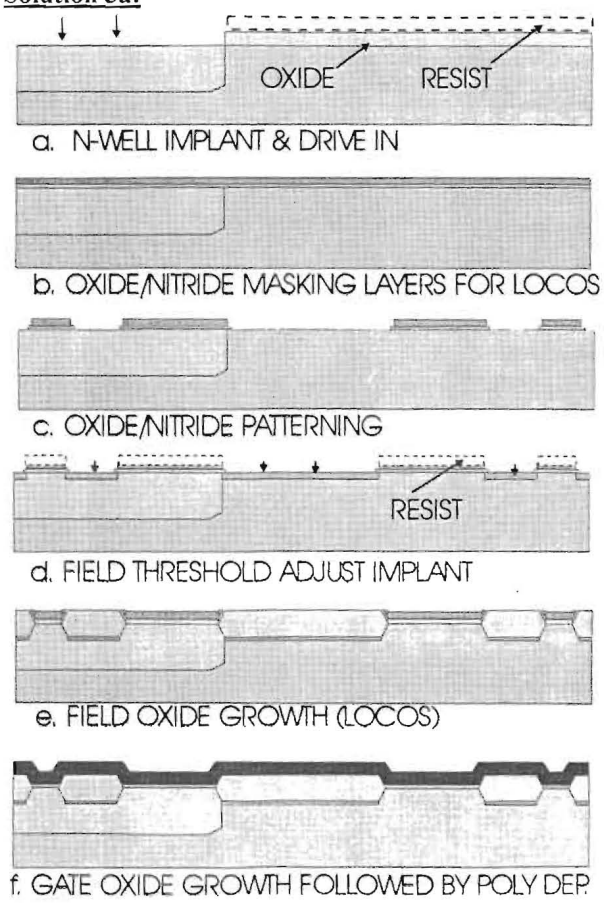
(iv)Extremely high group V excess can increase deep level incorporation

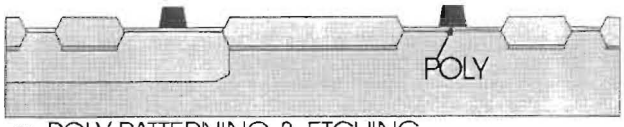
(v)atomic structure of the growth surface depends upon the type of substrate surface reconstruction

(vi)Varies with group **V** flux and temperature

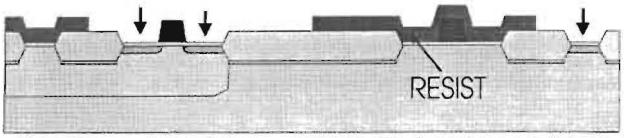
(vii)the migrating atoms may incorporate into existing surface step edges *step flow* growth mode. 3

Solution 3a:

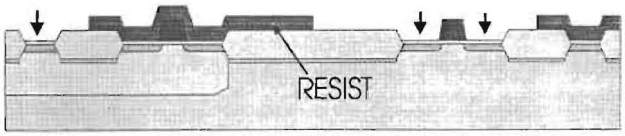




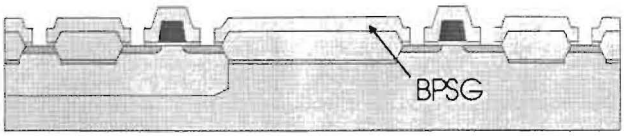
g. POLY PATTERNING & ETCHING



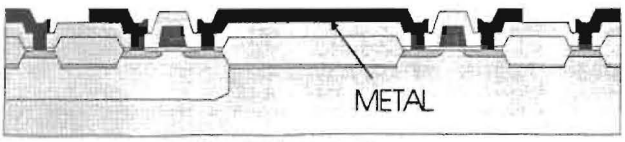
h. RESIST MASK FOR P+ SOURCE & DRAIN IMPLANT



i. RESIST MASK FOR N+ SOURCE & DRAIN IMPLANT



j. .BPSG DEPOSITION & CONTACT WINDOW ETCH



k. METAL DEPOSITION AND ETCH

10

Solution 3b.

Generally achieved by applying treatments to the ***back of a Si wafer***

(i) application of carefully-controlled ***abrasion damage*** (wafers often supplied pretreated)
impurities are trapped at general defects by precipitation

(ii)deposition of a layer of ***polySi***

Impurities are trapped at grain boundary defects by precipitation

(ii) ***implantation*** of a high dose of *inert gas ions* and recrystallization of the layer to give ***polySi*** and inert gas bubbles
impurities are trapped at grain boundary defects and internal bubble surfaces by precipitation

(iv)diffusion into the **Si** of a ***high concentration of phosphorus*** dopant
impurities are trapped at accompanying misfit dislocations by precipitation and, also, within the **Si** Lattice by solubility enhancement due to the presence of the phosphorous 3

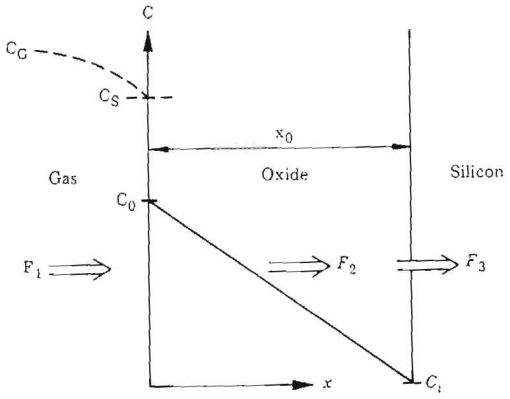
Solution 3c.

Key methods of implementation of a silicon oxide:

1. Thermal oxide, carried out in a furnace 900-1200 C.

   Dry oxidation: Si+ O2 -> SiO2

   Wet oxidation: Si + 2 H2O=SiO2 + H2. 2



Reaction kinetics (Fig)

three steps in the oxidation process

- the oxidising species is ***transported*** from the bulk of the gas to the oxide/ gas interface

flux = $h_G (C_G - C_S)$ [h_G is mass- -transfer coefficient]

- the oxidising species diffuses across the oxide layer already present

flux = $D (C_o - C_i)/Xo$ [D is the diffus- -ivity in oxide]

- the oxidising species reacts with the **Si** at the oxide/**Si** interface

flux = $k_S C_j$ [k_S is reaction rate constant]

- the rate determining step depends upon the oxide thickness (x_o)
  - for ***small*** x_o, there is a large oxidising species flux across the oxide layer and the reaction at the oxide/**Si** surface is rate-limiting
  - for ***large*** x_o, the flux across the oxide is small and this diffusion step is ratelimiting

Combining the above equations and determining the rate of change of x_o, it is found that

- for ***small*** x_o, rate of oxidation is ***linear***

for ***large*** x_o, oxidation rate is ***parabolic*** *3*

Solution 3e:

Two methods to boost channel mobility: Introduce Germanium in source/drain regions of pMOS to introduce compressive stress, or a thick nitride layer on NMOS to introduce tensile stress. 2

Solution 4a.

Wet and dry chemical etching.

Wet chemical etching

SiO_2 layers are readily etched in hydrofluoric acid

$SiO_2 - 6HF = H_2SiF_6 + 2H_2O$

Such etching is typically carried out either directly with HF solution ***(low pH)*** or using **HF** solution with added **NH_4F** as a buffering agent ***(high pH)***

Si_3N_4 layers can also be etched with added HF and buffered HF solutions

Selective **Si_3N_4** etching in the presence of oxide can be achieved using ***phosphoric acid***

Dry etching

Ions, atoms and radicals are formed in a plasma by ionisation and fragmentation

etching is produced by ***physical sputtering*** and/or catalysed ***chemical reactions***

reactive ion beam etching (**RIBE**) relies on chemical reactions to produce volatile compounds

typical dissociative reaction in a CF_4 plasma:

$$CF_4 + e^- = CF_3 + F^- + e^-$$

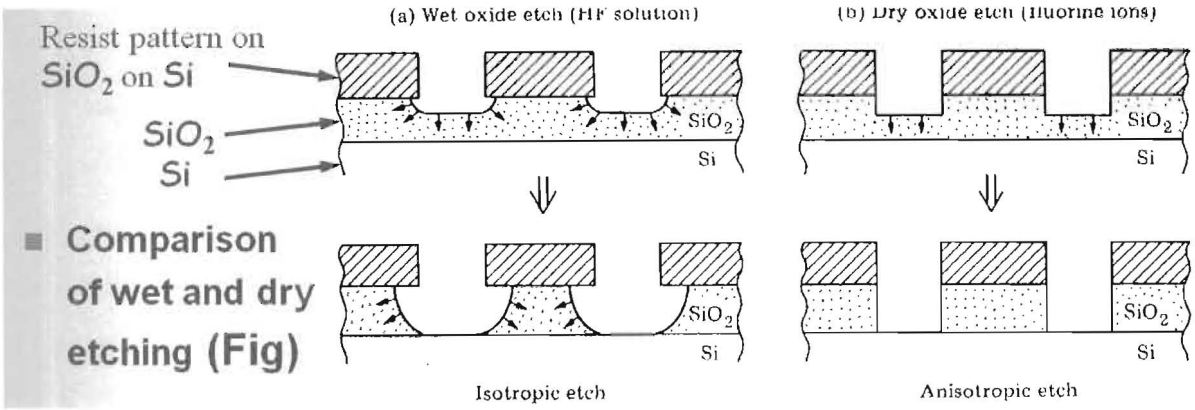
Gas composition determines etching rate and selectivity

halogen-containing gases are used to etch **Si, SiO_2, Si_3N_4** and **Al**

oxygen-containing gases are used to etch phototresist and organic layers 4

Etch Characteristics

- ***Dry etching*** characterised by high selectivity and pronounced directional etching ability
  - Favoured for **ULSI** technology due to etch ***dimensional accuracy***



- Comparison of wet and dry etching (Fig)

- SiO_2 on **Si** is covered with resist, which is then photographically exposed and patterned
- ***wet chemical etch*** dissolves the exposed oxide in an ***isotropic*** manner and progressively undercuts the resist Large structures.
- ***RIBE is highly anisotropic*** and produces parallel-walled etched regions with dimensions closely similar to those of the original resist pattern
- ideal for the very small structures characteristic of **ULSI** circuits 2

<u>Solution 4b</u>.

Pseudomorphic layers: Two different types of lattices grown one on top of another where epi layer grows to the same in-plane lattice vectors. 1

If the growing layer is stretched in-plane, the lattice constant normal to the plane decreases slightly

- If the lattice mismatch is relatively large (>1.5%), the sign of the lattice distortion determines the outcome
  - If the grown layer is under tension. Pre-existing threading dislocations are forced to bend over into the interface, whereupon they extend across the layer. The edge componenets of the Burgers vectors in the interface relax the strain- Matthews and Blakeslee mechanism. If there are any inhomogeneities in the layer (precipitates, etc), local strain can produce dislocation loops which expand into the interface
  - If the grown layer is under compression, it will become morphologically distorted

- As layer growth proceeds, after a small number of uniform monolayers, there is often a transition to the growth of isolated, small islands (a Stranski-Krastanow transition)
- Islands can be exploited as quantum dots in eg laser cavities
- Further growth leads to island overlap and the formation of undulating, wavy continuous layers
- Islands and undulations are produced because lateral dilatation of the lattice in the growth crests (which are unconstrained) lowers the strain energy of the system.

Ultimately, for sufficiently thick grown layers, array of misfit-relieving dislocations will be introduced. 2

Solution 4c.
Diffusion coefficient (D) = D0 exp –[EA/kT]
At 1250°C (1523K) D = 12 x exp –[4.05/(8.61 x 10^{-5} x 1423)] cm^2/s
= 12 x exp –[33.055] cm2/s
=5.29x10^{-14} cm^2/s
For 30min $2\sqrt{(Dt)} = 2\sqrt{(5.29 \times 10\text{-}14 \times 1800)}$ cm
= 1.95x10^{-5} cm.

Solution 4d.
Bipolar consumes more power. 1

Factors which may lead to device yield reduction are:
processing effects
lithographic mask misalignment, deposited or grown layer nonuniformities,
ion implantation nonuniformities, etc
circuit sensitivities
failure of the circuit design to take into account unavoidable device parameter variations across a wafer
local defects
dust or other particulate contamination, spikes on epitaxial layers, pin-holes in dielectric layers, crystallographic defects, etc 3