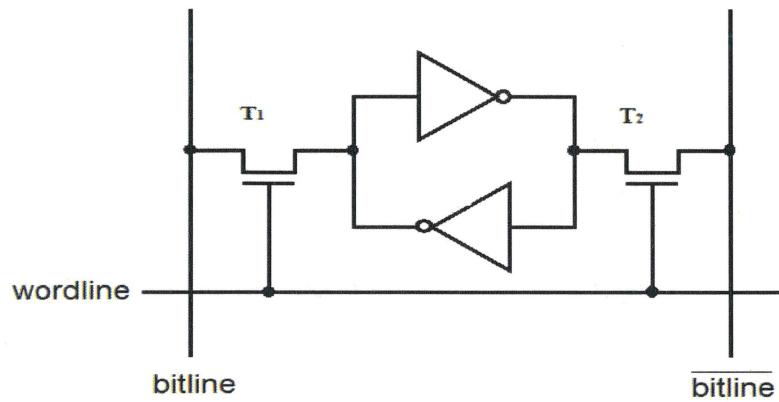


EEE225 Solutions

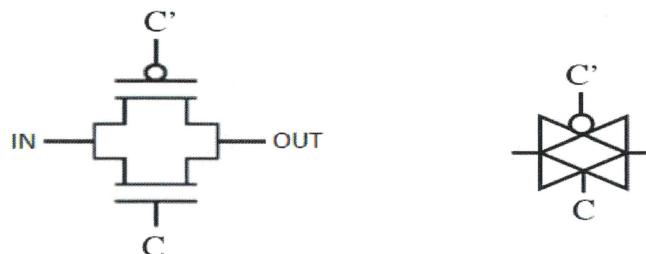
1.



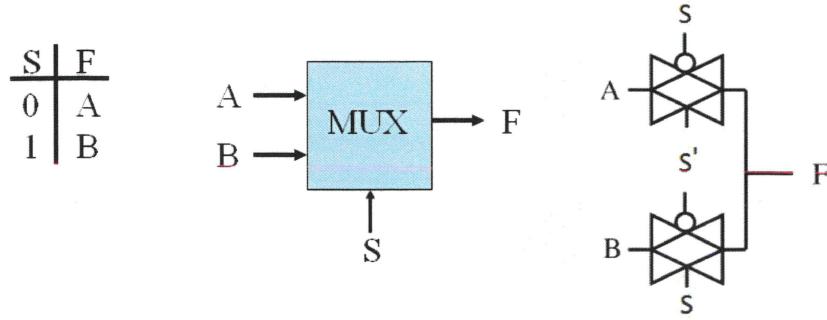
To write to the cell, *bitline* is set to the required data value and $\overline{\text{bitline}}$ is set to the complement. The controller then sets wordline = 1 which turns on transistors T1 and T2. The data values then appear in the inverter loop overwriting any previous value.

To read from the cell, *bitline* and $\overline{\text{bitline}}$ are both precharged to 1. Wordline is then set to 1. One of the enabled transistors will have a 0 at one end which will cause the corresponding precharged 1 to drop to a slightly lower voltage than a normal 1. Both of the bitlines are connected to a sense amplifier which can detect this variation and hence the data value.

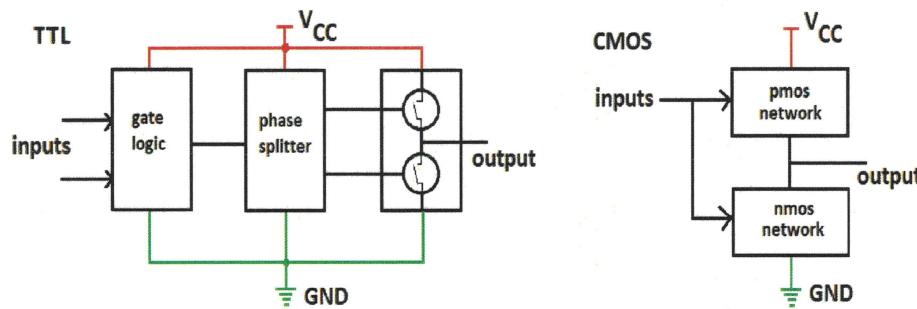
2.



Both transistors are ON or OFF simultaneously. The nmos switch passes a good zero but a poor 1. The pmos switch passes a good one but a poor 0. A bilateral switch is formed which passes a good 0 and good 1 in both directions.



3.



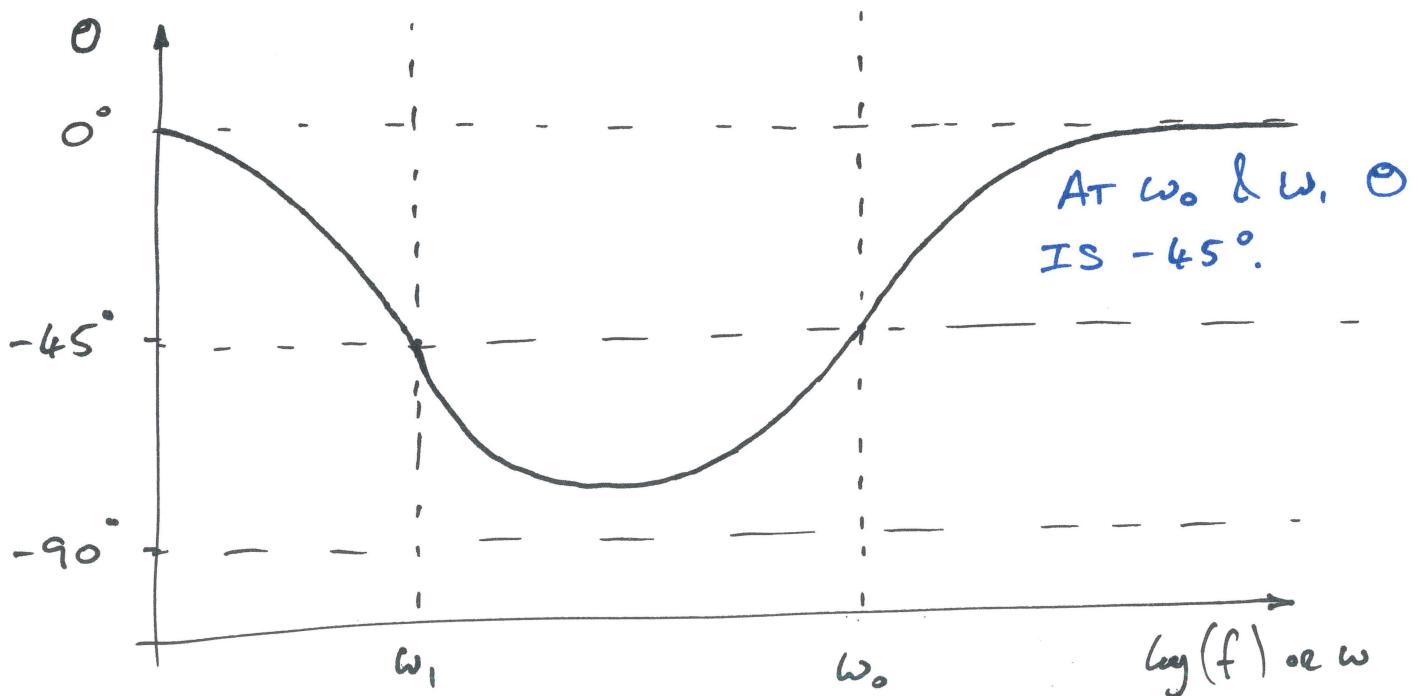
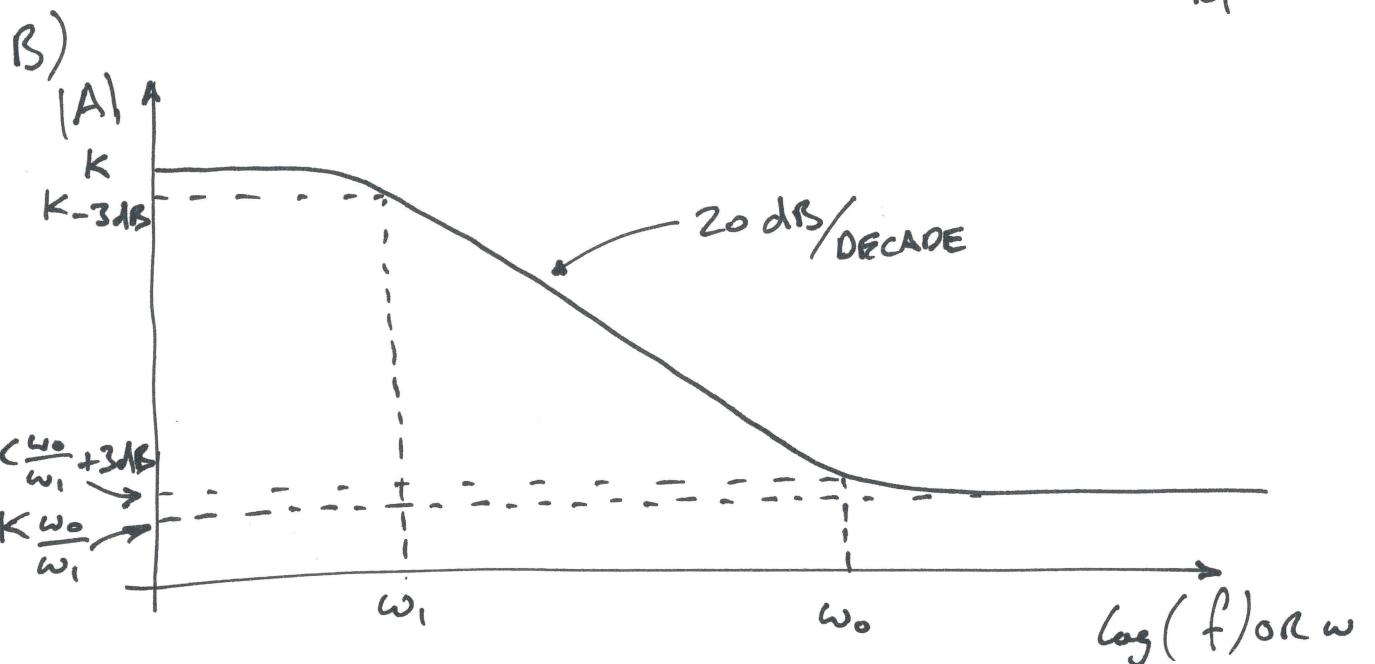
TTL – the first structural block implements the required logic. The second block is a phase splitter which is required to drive the final block which is a totem-pole output stage. In contrast, a CMOS logic gate consists of a pmos pull-up network to the positive supply rail and an nmos pull down network to ground.

In the case of TTL the gate logic consists of a multi-emitter transistor and the number of emitter connections would be increased. In the case of CMOS, an additional transistor in both the pull-up and pull-down network would be required for each extra input.

Q4

A) LF GAIN = $-\frac{R_3}{R_1}$

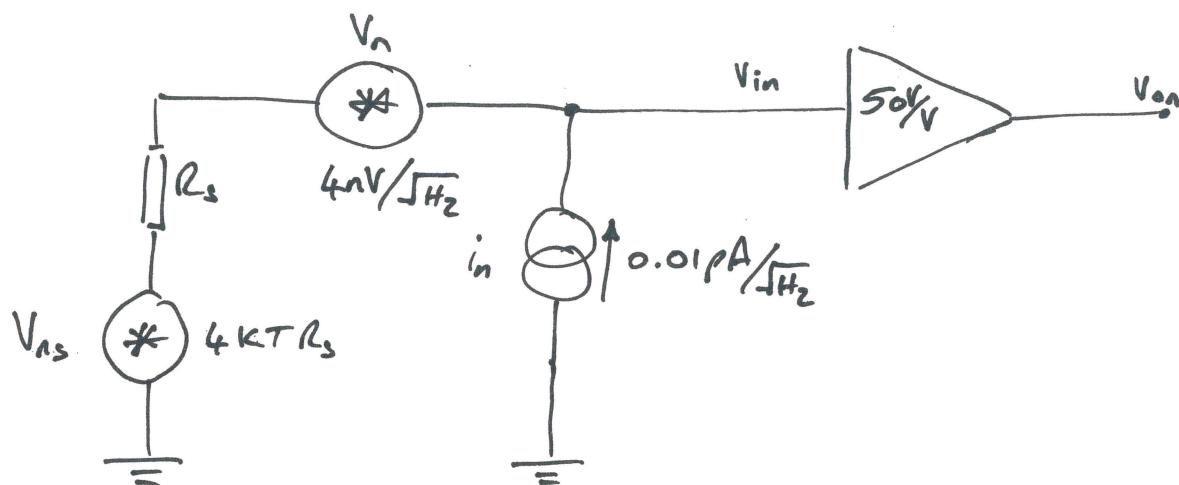
$$\text{HF GAIN} = -\frac{R_3 // R_2}{R_1} = -\left(\frac{\frac{R_3 \cdot R_2}{R_3 + R_2}}{R_1}\right)$$



NOTE: THIS QUESTION DID NOT REQUIRE STUDENTS TO PERFORM MANIPULATIONS ON THE GIVEN EQUATIONS !!

Q5

A)



$$\begin{aligned}
 B) \quad \overline{V_{on}^2} &= K^2 \left(\overline{V_{ns}^2} + \overline{V_n^2} + \overline{i^2 R_s^2} \right) \\
 &= 50^2 \left(4KTR_s + (4 \times 10^{-9})^2 + (0.01 \times 10^{-12})^2 \cdot 600^2 \right) \\
 &= 2500 \left(9.875 \times 10^{-18} + 1.6 \times 10^{-17} + 1 \times 10^{-28} \cdot 360 \times 10^3 \right) \\
 &= 2500 \left(9.875 \times 10^{-18} + 1.6 \times 10^{-17} + 3.6 \times 10^{-23} \right) \\
 &= 6.4688 \times 10^{-14} \text{ V}^2/\text{Hz} \quad \text{OR} \quad 254 \text{nV}/\sqrt{\text{Hz}}
 \end{aligned}$$

$$\begin{aligned}
 V_{on} &= \sqrt{\overline{V_{on}^2} \cdot \text{BW}} \\
 &= \sqrt{6.4688 \times 10^{-14} \cdot 20 \times 10^3} \\
 &= 35.968 \mu\text{V}_{\text{rms}}
 \end{aligned}$$

In THIS CASE IT IS ACCEPTABLE TO NEGLECT THE $\overline{i^2 R_s}$ TERM AS IT IS ~ 6 ORDERS OF MAGNITUDE BELOW THE $\overline{V_n^2}$ AND $\overline{V_{ns}^2}$ TERMS.

Q6

A) TIME DOMAIN : $V_o = V_i (1 - e^{-t/\tau})$

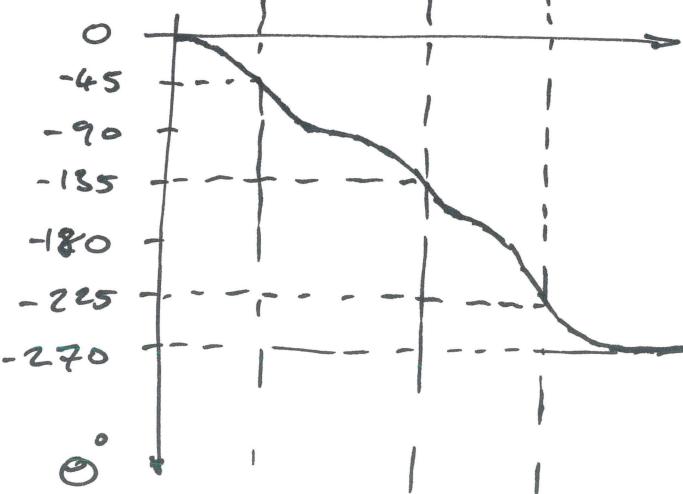
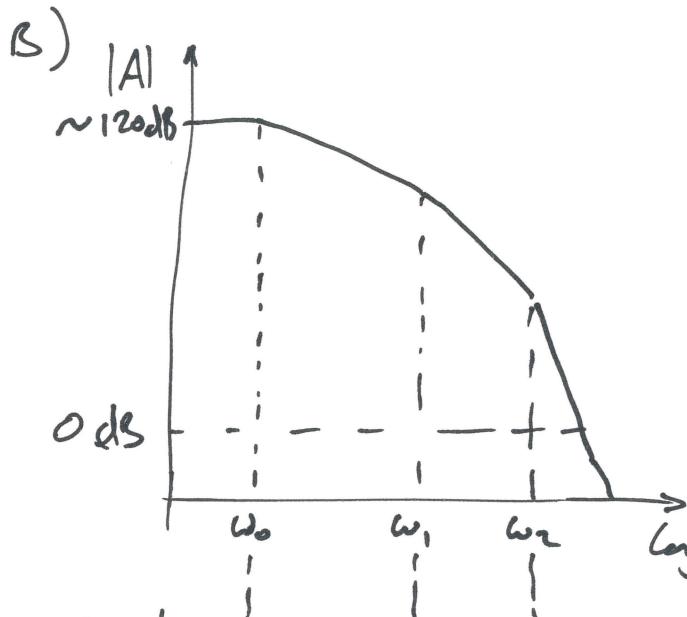
$$\underline{\tau_R = 2.2 \tau}$$

FREQUENCY DOMAIN :

$$\frac{V_o}{V_i} = K \cdot \frac{1}{1 + st} \quad \text{OR} \quad K \cdot \frac{1}{1 + j\omega / \underline{\omega_0}}$$

$$\text{OR } K \cdot \frac{1}{1 + \frac{jf}{f_0}} \quad (\text{ANY OF THESE IS OK.})$$

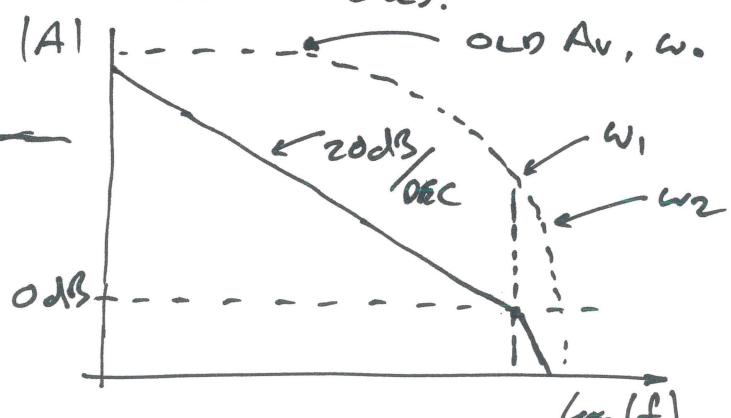
$$\underline{\tau = \frac{1}{\omega_0}}$$



- A STANDARD OPAMP HAS 3 STAGES AND EACH STAGE PROVIDES ONE POLE.

- BY MOVING THE LOWEST OR DOMINANT POLE, ω_0 , DOWN IN FREQUENCY UNTIL $A_v = 1$ @ ω_1 , THE CLOSED LOOP RESPONSE CAN BE MADE FIRST ORDER.

- THIS IS CALLED "UNITY GAIN COMPENSATION" AND YIELDS THE CLOSED LOOP CHARACTERISTICS GIVEN IN 6a).



7

Charge neutrality condition

$$n + N_a = p + N_d$$

also $n_p = n_i^2 = p_i^2$

$$n + N_a = \frac{n_i^2 + N_d}{n}$$

$$n^2 - (N_d - N_a)n - n_i^2 = 0$$

$$n = \frac{N_d - N_a}{2} + \frac{N_d - N_a}{2} \left[1 + \left\{ \frac{2n_i}{(N_d - N_a)} \right\}^{\frac{1}{2}} \right]$$

i) For n-type extrinsic, $N_d - N_a \gg n_i$

$$\therefore n = N_d - N_a \approx N_d$$

$$p = \frac{n_i^2}{N_d}$$

ii) For compensated near intrinsic

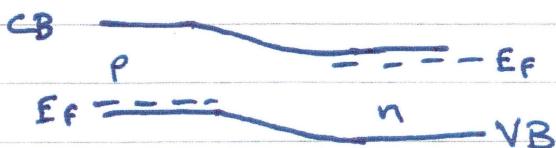
$$n_i \gg |N_d - N_a|$$

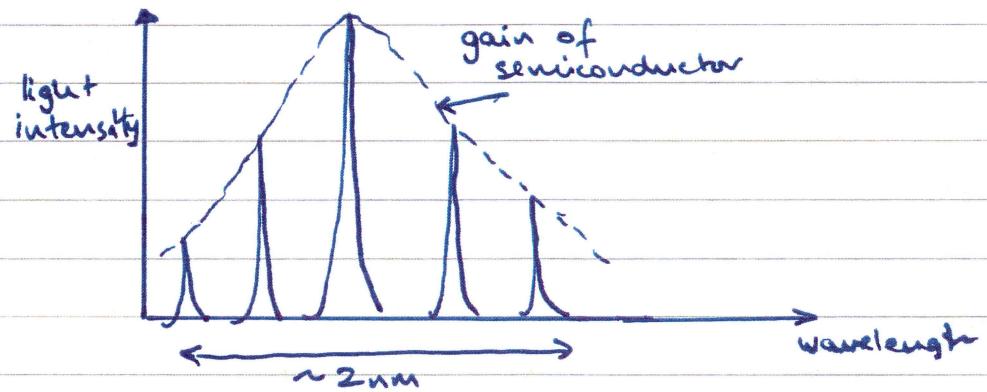
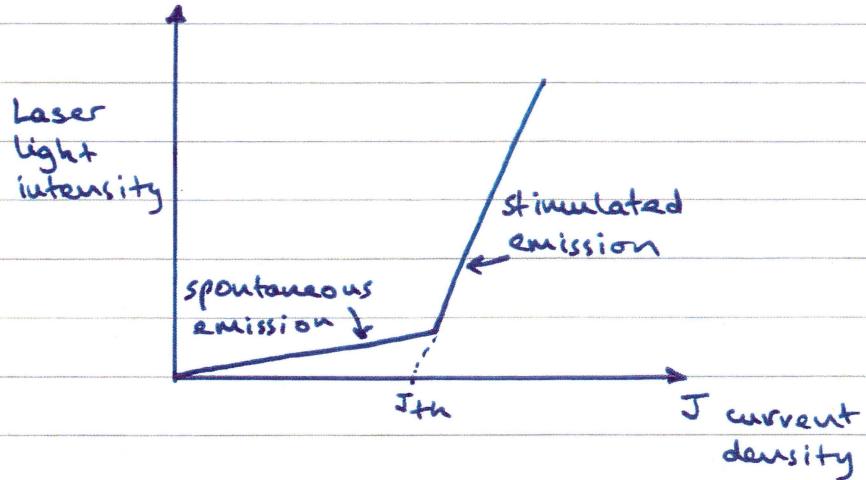
so

$$n = \frac{N_d - N_a}{2} + \frac{N_d - N_a}{2} \left[\frac{2n_i}{N_d - N_a} \right] \approx n_i$$

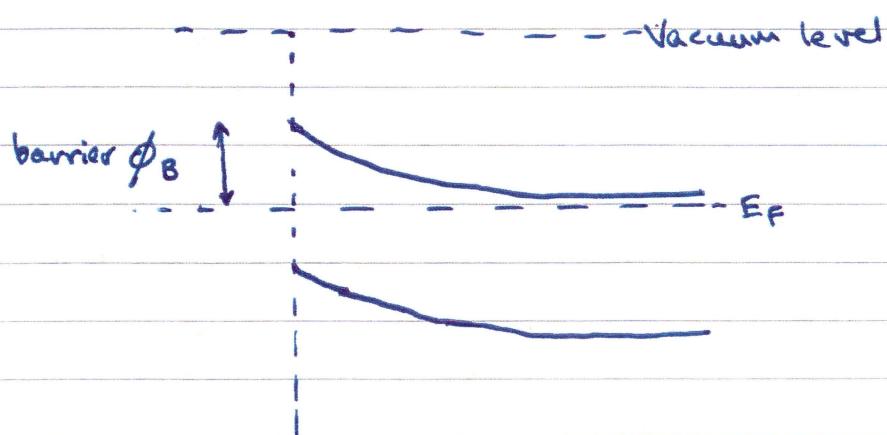
$$p = \frac{n_i^2}{n} \approx p_i \approx n_i$$

Under biasing condition, the p-n junction is forward biased, so



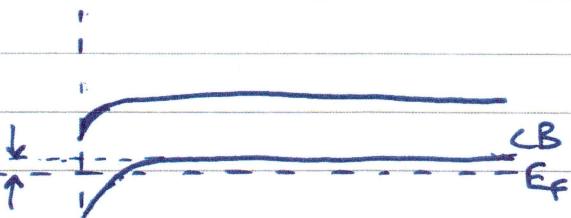


(i) Rectifying junction $\phi_m > \phi_s$ n-type



ohmic

very small
barrier



$$\phi_s > \phi_m \text{ n-type semiconductor}$$

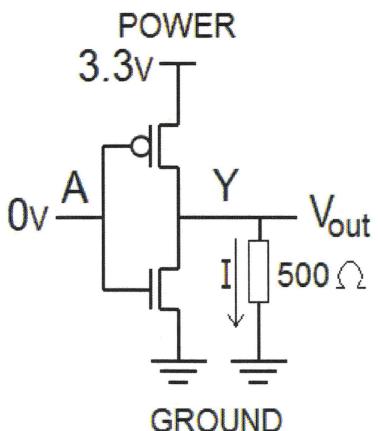
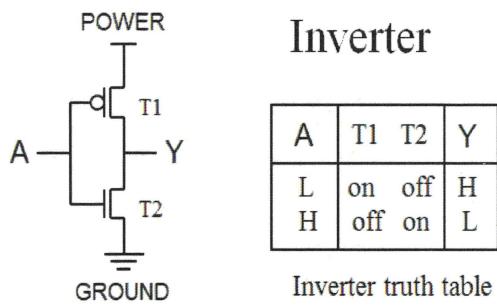
For rectifying junction, under forward bias, majority electrons flow from semiconductor to metal.
Under reverse bias, minority electrons from metal can thermionically get across the barrier ϕ_B into the semiconductor

10.

Apply $V_{out} = -\frac{V_s}{2^{n-i}}$ to all inputs that are HIGH, then sum the results.

$$V_{out}(D_0) = -\frac{3.3V}{2^{4-0}} = -0.206 \text{ V} \quad V_{out}(D_1) = -\frac{3.3V}{2^{4-1}} = -0.413 \text{ V}$$

$$V_{out}(D_3) = -\frac{3.3V}{2^{4-3}} = -1.65 \text{ V} \quad \text{Applying superposition, } V_{out} = -2.269 \text{ V}$$



pmos is on with a resistance of 75Ω

nmos is off with a resistance of $500,000 \Omega$

Load impedance is $500,000 \Omega$ in parallel with $500 \Omega \approx 500 \Omega$

$$V_{out} \approx 3.3 \times (500 / 575)$$

$$\approx 2.87V$$

$$I \approx 3.3 / (75 + 500)$$

$$\approx 5.7mA$$

Q11

- A) ANY OF THE POINTS BELOW ARE ACCEPTABLE ALONG WITH ANYTHING ELSE THAT IS TRUE AND HELPFUL.

$T_1 \& T_2$: - ARE A DIFFERENTIAL AMPLIFIER.
 - THEY SUBTRACT V^+ & V^- TO YIELD AN ERROR CURRENT THAT FLOWS IN THE COLLECTORS OF $T_1 \& T_2$.

$T_3 \& T_4$: - ARE A CURRENT MIRROR.

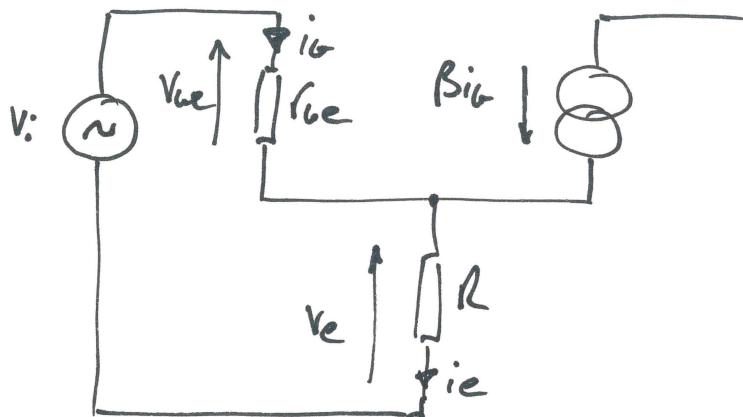
- T_4 REFLECTS THE ERROR CURRENT IN T_2 'S COLLECTOR TO T_1 'S COLLECTOR EFFECTIVELY DOUBLING THE GAIN OF THE STAGE.
- $T_4 \& T_2$ REDUCE THE DISTURBANCE T_5 IMPARTS TO $T_1 \& T_2$ EFFECTIVELY BALANCING THE DIFFERENTIAL AMPLIFIER AND REDUCING OUTPUT OFFSET.
- $T_3 \& T_4$ PROVIDE A HIGH IMPEDANCE LOAD FOR $T_1 \& T_2$ COMPARED TO A RESISTOR YET MAINTAIN SUITABLE QUIESCENT CURRENT TO PROVIDE A REASONABLE TRANSCONDUCTANCE.

$T_5 \& T_6$: - ARE A PARRINGTON PAIR.

- $T_5 \& T_6$ ARE THE "VOLTAGE AMPLIFIER" STAGE.
- $T_5 \& T_6$ - A NON-DEGENERATED COMMON Emitter AMPLIFIER.
- T_5 REDUCES THE BASE CURRENT I_b DEMANDS FROM T_1 'S COLLECTOR MINIMISING THE LOAD ON THE DIFFERENTIAL AMPLIFIER.
- $T_5 \& T_6$ PROVIDE A VERY LARGE VOLTAGE GAIN THAT IS THE MAJORITY OF A_v .
- $T_5, T_6 \& C$ SET ω_o AND AFFECT THE AMPLIFIER COMPENSATION.

Q 11

A ii)



- Sum I @ Emitter node:

$$i_e = i_o + \beta i_o \quad (1)$$

$$\frac{V_e}{R} = \frac{V_{fe}}{R_{fe}} + g_m V_{fe}$$

- Sum V Around THE INPUT LOOP:

$$V_i = V_{fe} + V_e \quad (2)$$

$$\frac{V_{fe}}{R_{fe}} + g_m V_{fe} = \frac{V_i - V_e}{R}$$

$$V_{fe} + \left(\frac{1}{R_{fe}} + g_m + \frac{1}{R} \right) = \frac{V_i}{R}$$

$$i_o R_{fe} \left(\frac{1}{R_{fe}} + g_m + \frac{1}{R} \right) = \frac{V_i}{R}$$

THESE ARE MUCH
SHORTER SOLUTIONS
THAN THIS ONE,
BUT THE ICY STAPS

(1) & (2) ARE ALWAYS
TRUE.

$$r_i = \frac{V_i}{i_o} = \left(1 + g_m R_{fe} + \frac{R_{fe}}{R} \right) R$$

$$= R + g_m R_{fe} R + R_{fe}$$

$$= R(1 + \beta) + R_{fe}$$

$$(R_{fe} = \beta / g_m)$$

R IS R_{fe}

i_o IS R_{fe}

Q11

(B) THE AMPLIFIER IS FIRST ORDER SO WILL OBEY THE USUAL EQUATIONS:

$$\frac{V_o}{V_i} = K \cdot \frac{1}{1 + j\frac{\omega}{\omega_0}} = A$$

100% dc gain.

$$\left| \frac{100}{1 + j \frac{120 \times 10^3}{f_0}} \right| = 50 \quad \text{OR} \quad \frac{1}{1 + \left(\frac{120 \times 10^3}{f_0} \right)^2} = \left(\frac{1}{2} \right)^2$$

$$\sqrt{4-1} = \frac{120 \times 10^3}{f_0} = 1.73$$

$$f_0 = \frac{120 \times 10^3}{1.73} = \underline{\underline{69.4 \text{ kHz}}}$$

$$\begin{aligned} \text{GAIN BANDWIDTH PRODUCT} &= 100 \cdot 69.4 \text{ kHz} \\ &= \underline{\underline{6.94 \text{ MHz}}} \end{aligned}$$

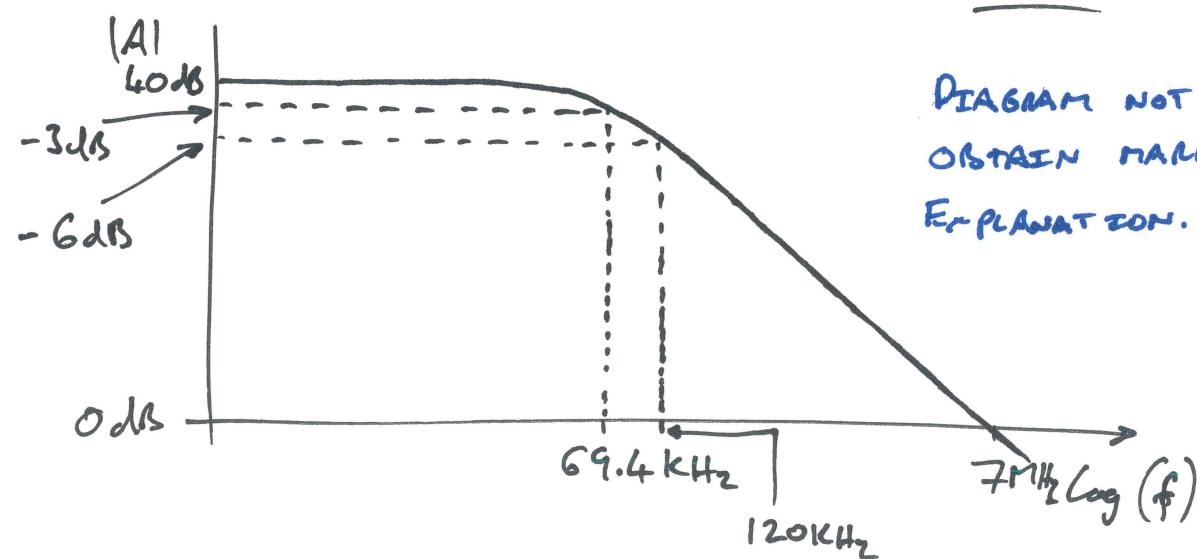


DIAGRAM NOT REQUIRED TO OBTAIN MARKS, JUST FOR EXPLANATION.

Q_{ii} B ii) THE GAIN BANDWIDTH PRODUCT IS GREATLY REDUCED TO 100 kHz.

$$\frac{V_o}{V_i} = K \cdot \frac{1}{1 + j \frac{\omega}{\omega_0}} = \frac{100}{1 + j \left[\frac{f}{\left(\frac{100 \text{ kHz}}{100} \right)} \right]} \quad \text{GBP}$$

\downarrow
 K

$$\text{At } 75 \text{ kHz, } |A| = \left| \frac{V_o}{V_i} \right| = \frac{100}{\left[1 + \left(\frac{75}{100} \right)^2 \right]^{\frac{1}{2}}} \\ = 1.333 \text{ V/V}$$

OR 2.498 dBV

$$\text{THE PHASE SHIFT, } \Theta = \angle \left[\frac{V_o}{V_i} \right] = -\tan^{-1} \left(\frac{f}{f_0} \right) \\ = -\tan^{-1} \left(\frac{75}{100} \right) = -\underline{\underline{89.236^\circ}} \\ \text{OR } -1.557^\circ$$

iii) SLEW RATE:

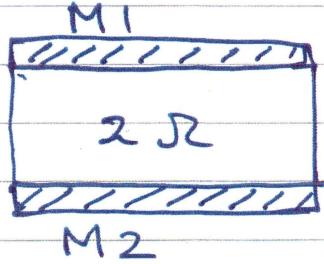
$$3V_{\text{rms}} = 3\sqrt{2} V_{\text{pk}} = 4.2426 \text{ V}$$

MAY RATE OF CHANGE OF SINE IS AT ZERO CROSSING...

$$V(t) = V_p \sin(\omega t) \quad \& \quad \frac{dV(t)}{dt} = V_p \omega \cos(\omega t)$$

Around Sine crossing zero $\cos(\omega t)$ is 1 (THE BIGGEST IT CAN BE) $\therefore \max \frac{dV}{dt}$ IS $V_p \omega$

$$\text{SR} = 4.2426 \cdot 2\pi \cdot 0.05 \times 10^6 \\ = \underline{\underline{1.3329 \text{ V/}\mu\text{s.}}}$$



$$\phi_{M1} = 4 \text{ eV}$$

$$\phi_{M2} = 1 \text{ eV}$$

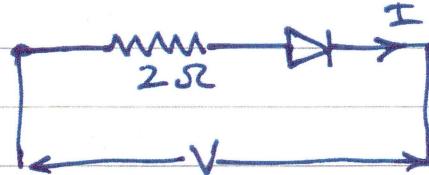
n-type semiconductor $\phi_s = 3 \text{ eV}$

$M_1/\text{semiconductor}$ = schottky contact

$M_2/\text{semiconductor}$ = ohmic contact

When a large current of 500mA flows, the $M_1/\text{s.c.}$ junction is forward biased.

Equivalent circuit :



$$I = I_o \left\{ \exp \left[\frac{e(V - 0.5 \times 2)}{kT} \right] - 1 \right\}$$

$$0.5A = I_o \times 2.25 \times 10^8$$

$$I_o = 2.22 \times 10^{-9} \text{ A}$$

When bias voltage is reversed, the $M_1/\text{s.c.}$ junction is reverse biased and only the small leakage current I_o flows.

$$I_d = \frac{\mu e C_g}{l^2} \left[V_{gs} - V_T - \frac{V_{ds}}{2} \right] V_{ds} \text{ in unsaturated region}$$

When $V_{gs} - V_{ds} - V_T < 0$, or

$V_{ds} > V_{gs} - V_T$, saturation of I_d occurs, I_{ds}

$$I_{ds} = \frac{\mu e C_g}{l^2} \left[V_{gs} - V_T - \left(\frac{V_{gs} - V_T}{2} \right) \right] (V_{gs} - V_T)$$

$$= \frac{\mu e C_g}{2l^2} (V_{gs} - V_T)^2$$

Gate and Drain connected together, so
 $V_{gs} = V_{ds}$, $\frac{\mu e C_g}{l^2} = 4 \times 10^{-4} \text{ A V}^{-2}$, $V_T = 2 \text{ V}$

$I_d = 0$ when $V_{ds} = 1 \text{ V}$ as V_{ds} (or V_{gs}) $\leq V_T$
and no channel can form

When $V_{ds} = 3 \text{ V}$, $V_{gs} = 3 \text{ V}$

$$I_d = \frac{4 \times 10^{-4}}{2} (V_{gs} - 2)^2 = 2 \times 10^{-4} \text{ A}$$

When $V_{ds} = 4 \text{ V}$, $V_{gs} = 4 \text{ V}$

$$I_d = \frac{4 \times 10^{-4}}{2} (4 - 2)^2 = 8 \times 10^{-4} \text{ A}$$