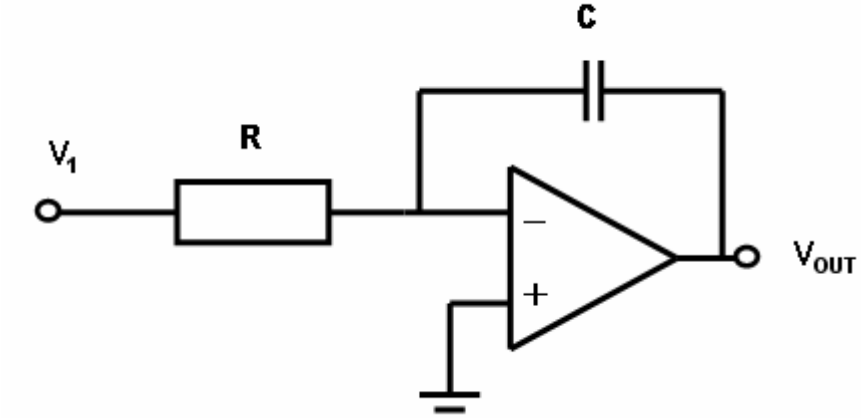
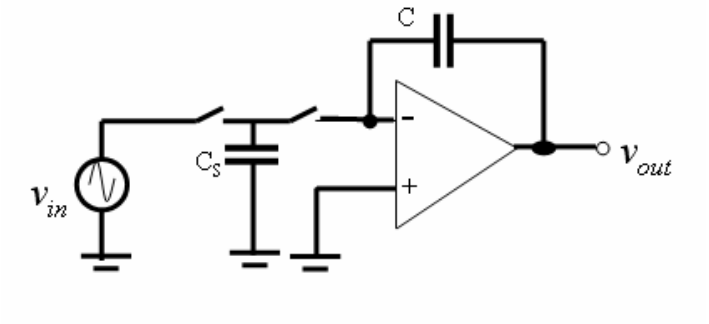
1. Design a switched-capacitor integrator (assuming CMOS VLSI) to implement the active RC integrator of Fig. 1a. Assume that the switching clock is equal to frequency of 512 KHz (50% duty cycle). You should assume that the operational amplifiers are not limited by bandwidth or slew rate. R is 1.5 MΩ and C is 5 pF.



2. Describe the behaviour of a switched capacitor integrator in Fig. 1b with an equivalent active RC circuit. Assume that the switching clock is equal to frequency of 512 KHz (50% duty cycle). You should assume that the operational amplifiers are not limited by bandwidth or slew rate. Cs is 0.5 pF and C is 5 pF.



3. Describe the signal flow graph for the leap-frog implementation of LC ladder prototype filter in Fig. 2. (Use R, C1, L2, C3, L4, C5 as the value of each component)