First Semester Organisation and Content

- Basic Principles of semiconductors
- Diodes
- Transistors
- Thyristors
- Any questions on these?

Second semester Organisation and content

- Power Metal Oxide Semiconductor Field Effect Transistor (2 lectures)
- Insulated Gate Bipolar Transistors (2 lectures)
- MOS controlled Thyristors (1 lecture)
- Wide bandgap device technologies
  - Silicon Carbide (2 lectures) – Mahmood Alwash
  - Gallium Nitride (2 lectures) – Vineet Unni

Second semester Organisation and content

- Charge Balance in Power Semiconductors (2 lectures)
  - RESURF principle
  - Double RESURF
  - Super-junction devices
- Lateral Power devices & technologies (2 lectures)
- Packaging (2 lectures – Mark Sweet)
- Guest lectures (3 lectures)
  - One from Rolls-Royce
  - One from Alstom
  - One from IXYS-UK Westcode

Power MOSFET

References books:

- POWER ELECTRONICS—CONVERTERS, APPLICATIONS, AND DESIGN, Ned Mohan, Tore M. Undeland, William P. Robbins, WILEY

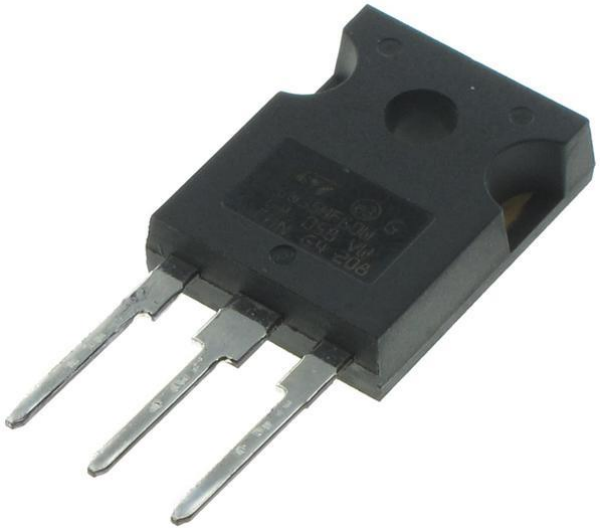
- FUNDAMENTALS OF POWER SEMICONDUCTOR DEVICES, B. Jayant Baliga, Springer

- SEMICONDUCTOR POWER DEVICES—PHYSICS, CHARACTERISTICS, RELIABILITY, Josef Lutz, Heinrich Schlangenotto, Springer

A little history for power MOSFET

- The power MOSFET has been available since 1976 as a practical commercial device
- Siliconix announced the world's first commercially-available power MOSFET in 1976.
- Almost simultaneously, Hitachi announced the classic planar design
- The standard structure—a vertical, planar four-layer semiconductor process commonly called DMOS or double-diffused MOS

Some power MOSFETs in market

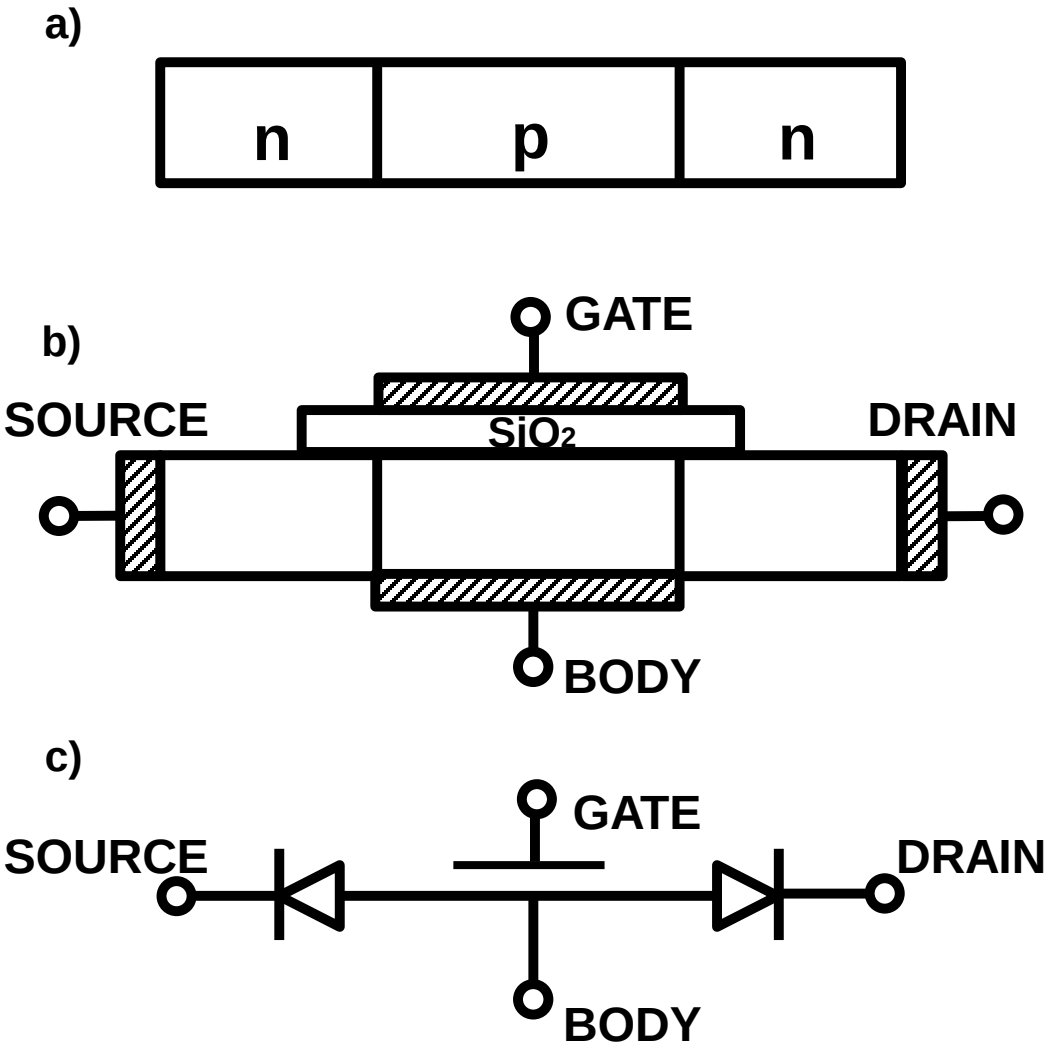


STMicroelectronics

CREE-Silicon Carbide Power MOSFET

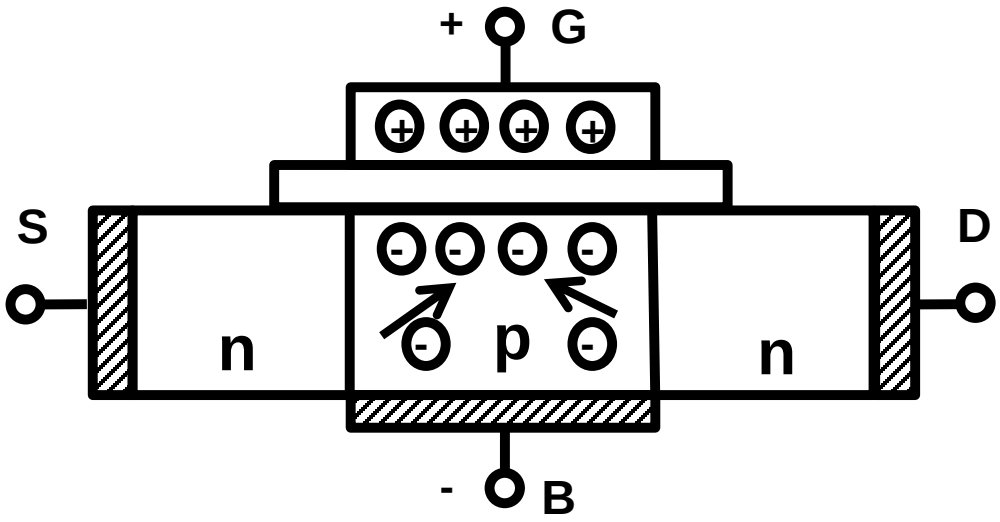
Infineon

Principles of MOSFET operation



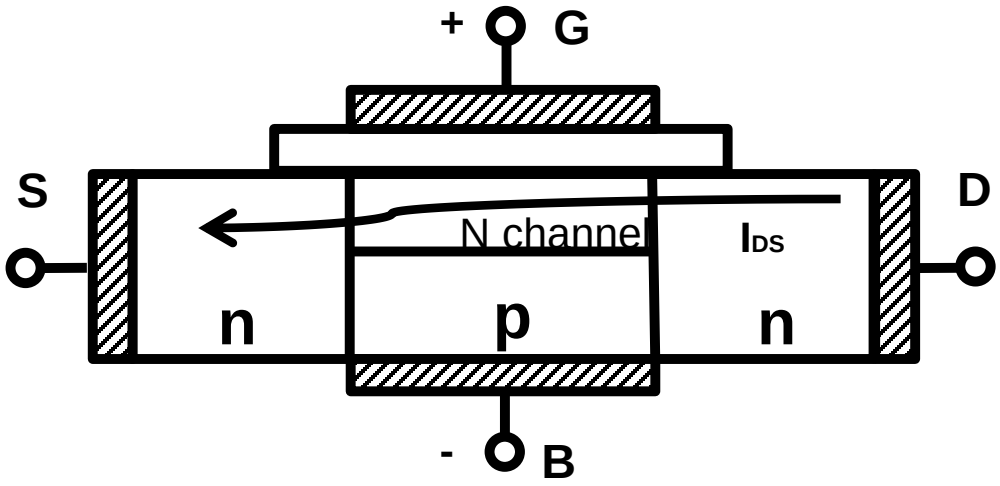
- The model chosen does not represent how practical devices are actually built
- a) shows an *npn* junction structure which is identical to a bipolar junction transistor; the differences arise from the connections made to this basic structure
- A MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) shown in b), three ohmic contacts and an insulated capacitor plate (SiO_2) capacitor plate are added to the *npn* structure.
- As long as the potential between body and gate is not positive, this device is essentially two diodes back to back (c). It is off state.

Principles of MOSFET operation

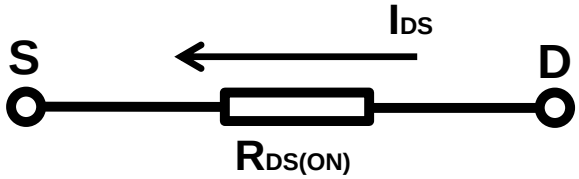


- The *p* region is doped so that there are more holes than electrons.
  - This is, by definition, what makes it a *p* region.
  - Even though the holes outnumber the electrons, there are still plenty of free electrons in the *p* region.
- If the gate is made positive with respect to the body, some of the electrons will be attracted to the gate structure.
- Due to the presence of the gate oxide insulator, the gate metal and the body semiconductor form a capacitor which accumulates charge.

Principles of MOSFET operation

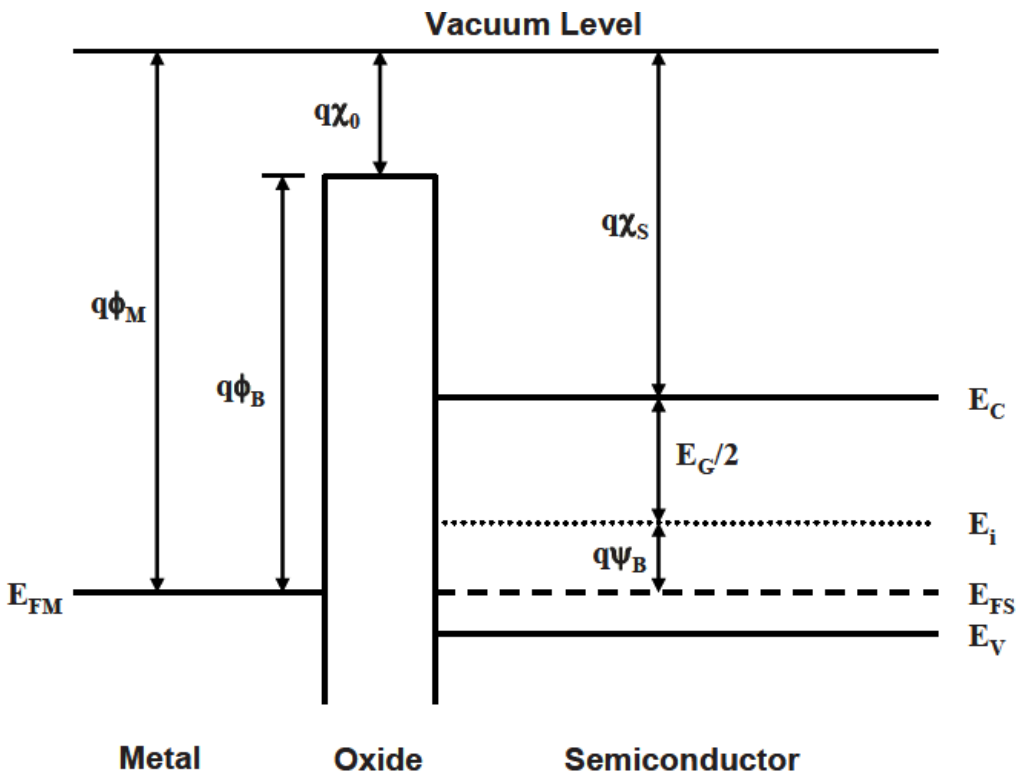


- As the gate to body potential is increased, the charge density in the body, immediately adjacent to the gate oxide, will increase to the point where the electron density exceeds the hole density.
  - A portion of the body region (the channel) inverts to become *n* rather than *p*.
- The semiconductor structure is like *n*-*n*-*n*.



- Due to the existence of the N channel, it has become simply a silicon resistor through which current can flow easily.
- This is a variable resistor in which the resistance of the channel is controlled b the potential from gate to body.

MOS interface physics



MOS structure operating under flat band conditions

At equilibrium,

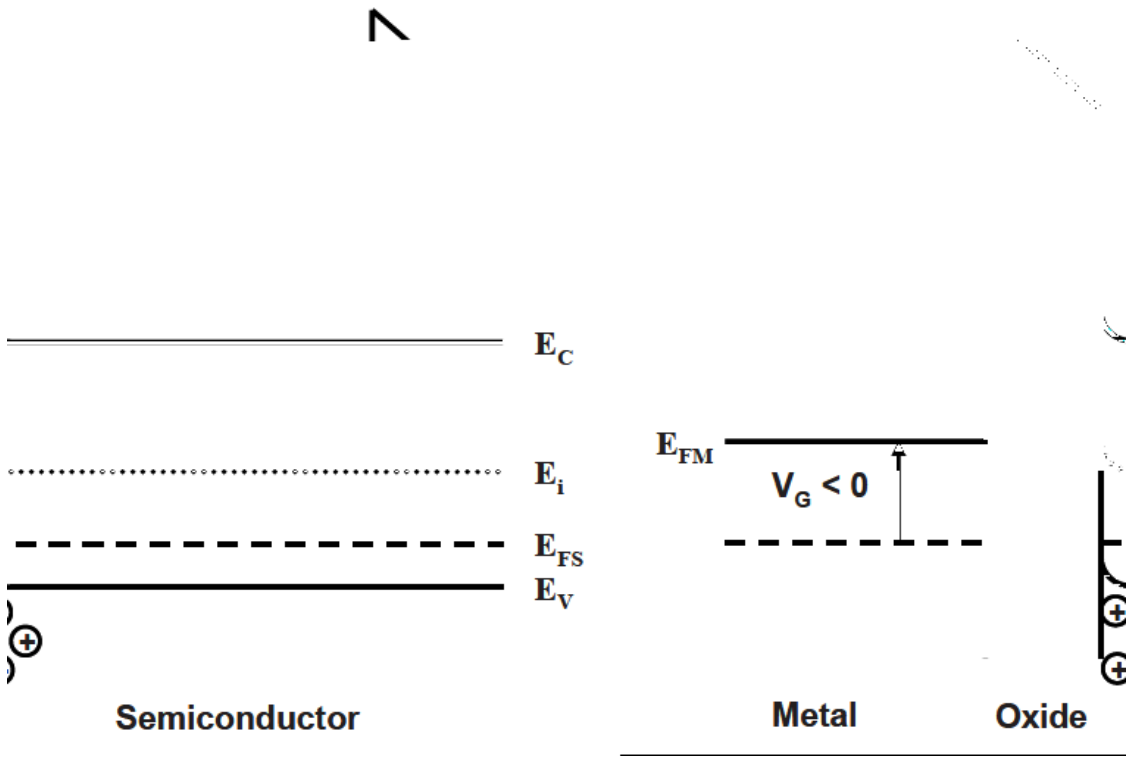
$$q\emptyset_M = q\chi_S + \frac{E_G}{2} + q\psi_B = q\emptyset_B + q\chi_O$$

Where $\emptyset_M$ is the work function for the metal, χ_S is the electron affinity for the semiconductor, E_G is the energy band gap for the semiconductor, ψ_B is the potential difference between the intrinsic and Fermi levels in the bulk of the semiconductor, $\emptyset_B$ is the barrier height between the metal and the oxide, χ_O is the electron affinity for the oxide.

$$\psi_B = \left(\frac{E_i - E_{FS}}{q}\right) = \frac{kT}{q}\ln\left(\frac{p_0}{n_i}\right)$$

Where E_i is the position of the intrinsic level, n_i is the intrinsic concentration, and p_0 is the hole concentration.

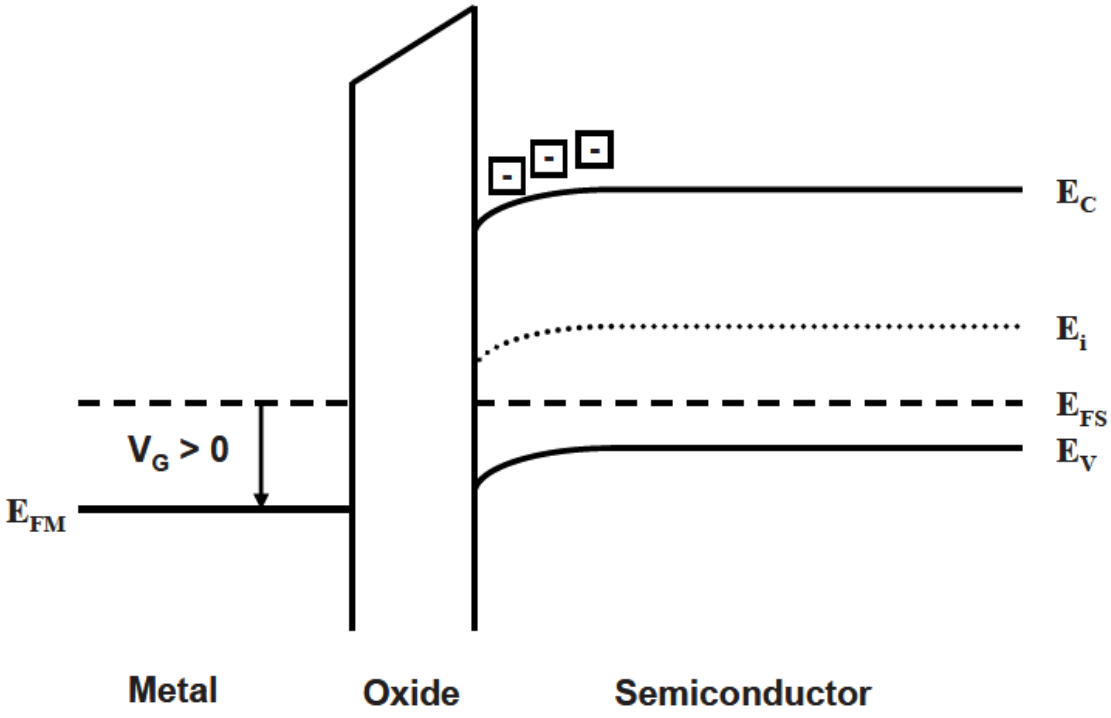
MOS interface physics - Accumulation



MOS structure operating under accumulation conditions

- When a negative bias is applied to the metal electrode, the presence of excess majority carriers at the surface of the semiconductor is referred to as ***accumulation*** of **HOLES**
- A reduction of energy difference between the Fermi level and the valence band.
- A small band bending at the surface.

MOS interface physics -



MOS structure operating under depletion conditions

- At small positive bias voltages, the semiconductor at the oxide interface becomes depleted leading to the energy band bending.
- There are no mobile charge carriers resident in the semiconductor under the oxide

MOS interface physics – Inversion and Strong Inversion

MOS structure operating under inversion conditions

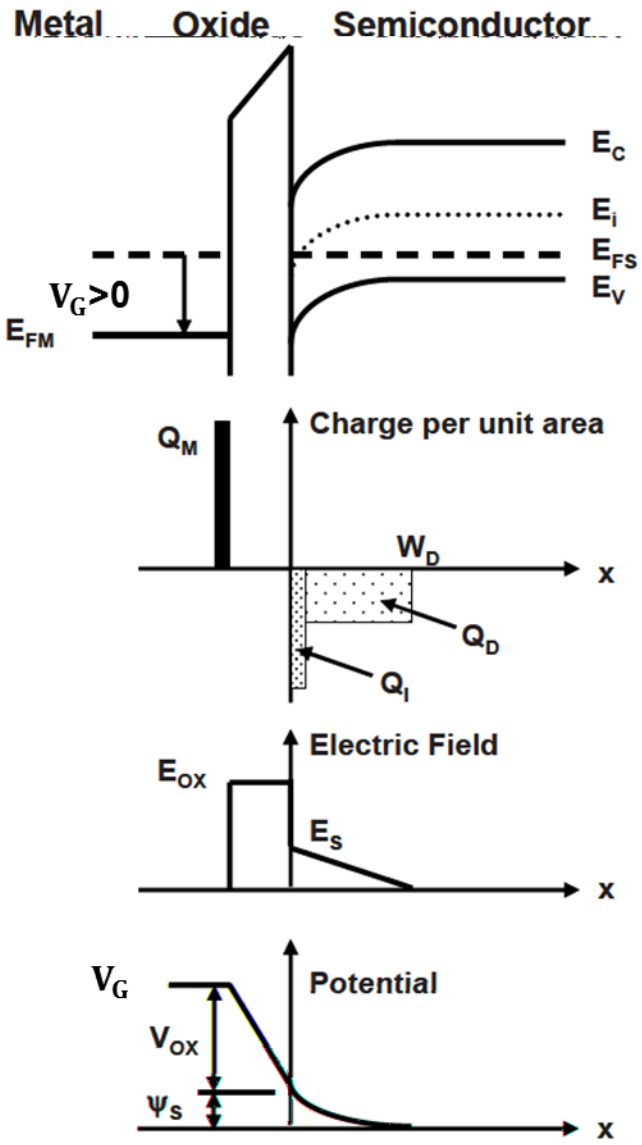
The band bending increases until the intrinsic level crosses the Fermi level.

The semiconductor surface now has the properties of an N-type semiconductor.

The free electrons created within this *inversion region* can be utilized to form the channel (*weak inversion*).

When the electron density exceeds the majority carrier density in the bulk, it is referred to as *strong inversion*.

Threshold voltage



Using the potential at the semiconductor surface (ψ_S),

$$V_G = V_{OX} + \psi_S$$

Where V_{OX} is the voltage supported across the oxide.

$$V_{OX} = E_{OX} t_{OX} = \frac{Q_S}{\varepsilon_{OX}} t_{OX} = \frac{Q_S}{C_{OX}}$$

Where C_{OX} is the specific capacitance of the oxide and Q_S is the total charge in the semiconductor.

The charge, electric field, and potential distributions under inversion conditions

Threshold voltage

- The threshold voltage V_{TH} is defined as the voltage applied to the metal electrode to achieve strong inversion.

$$V_{TH} = \frac{Q_S}{C_{OX}} + 2\psi_B$$

- The total charge per unit area under strong inversion conditions is:

$$Q_S = \sqrt{2\varepsilon_S kT n_{p0}}\, e^{q\psi_S/2kT}$$

Where n_{p0} is the concentrations for the electrons in the bulk of the semiconductor in equilibrium.

Leading to :

$$V_{TH} = \frac{\sqrt{2\varepsilon_S n_{p0}}}{C_{OX}}\, e^{q\psi_B/kT} + 2\psi_B$$

Threshold voltage

- The bulk potential ψ_B can be related to the doping concentration in the semiconductor, leading to

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln\left(N_A/n_i\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

- The first term is usually dominant in this equation for the threshold voltage of power MOSFET structures. After substituting for the specific oxide capacitance, the threshold voltage is then given by

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}}\sqrt{4\varepsilon_S kTN_A \ln\left(\frac{N_A}{n_i}\right)}$$

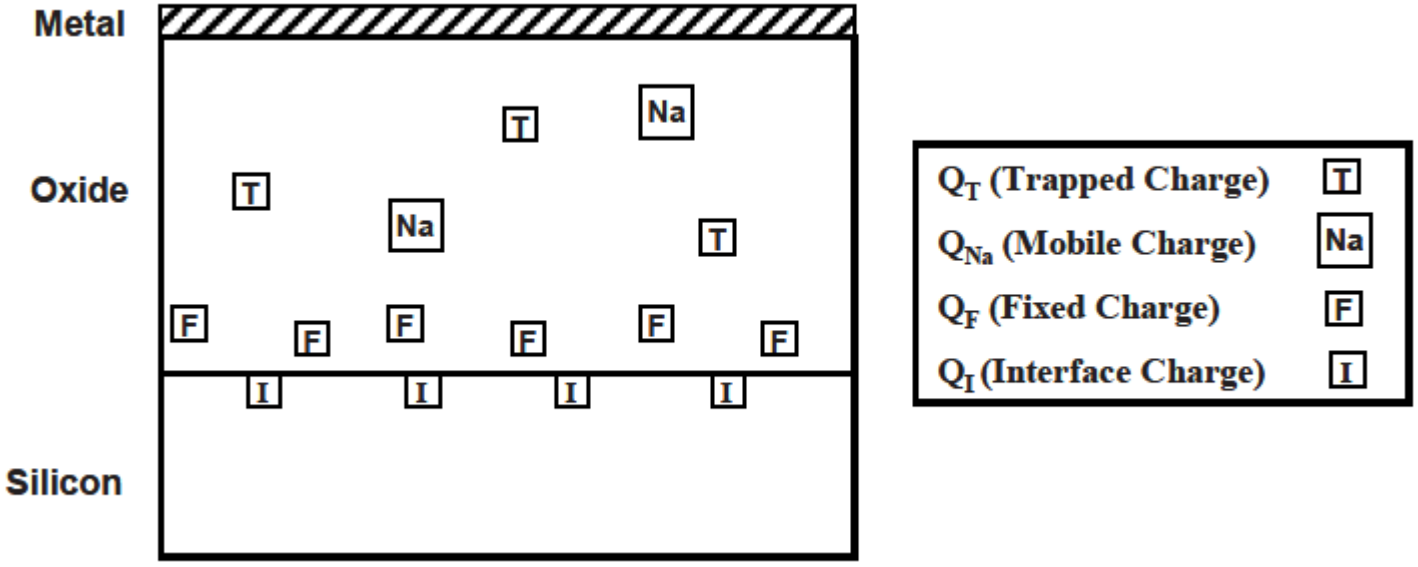
Calculate the threshold Voltage

- A MOSFET with a p body doping concentration (Na) of 1016 /cm3 and a gate oxide thickness of 100 nm, made of Silicon Dioxide. The channel length is 3 um and the channel mobility is 1000 cm2/Vsec. What is the threshold voltage at room temperature?

- $V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_S kT N_A \ln\left(\frac{N_A}{n_i}\right)}$
- V_{TH}= 2.099 V.

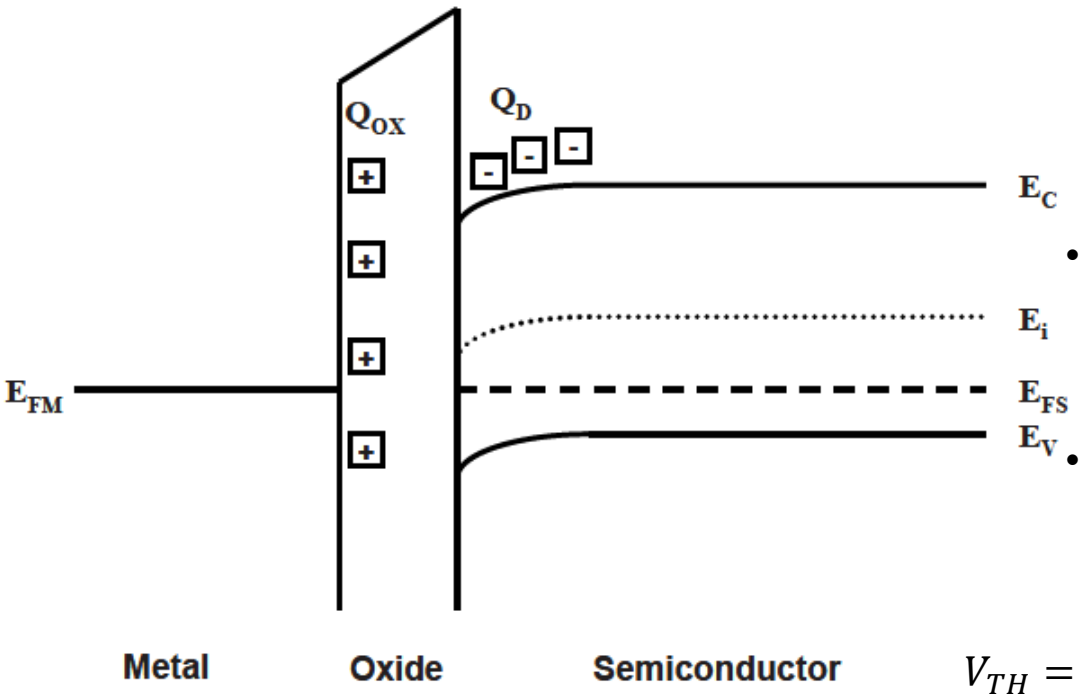
Oxide charge

- The growth of silicon dioxide on the surface of silicon is by thermal oxidation.
- The grown oxide contains a variety of positive charges.
  - Mobile ion charge – alkali based impurities such as Sodium etc
  - Fixed oxide charge – oxide charges at the interfaces
  - Trapped oxide charge – created by hot electron effects
  - Interface state charge - from ionic Silicon charges
- Under carefully controlled process conditions, it is possible to reduce the density of the fixed and interface state charges, but, these accumulate over time.



Charge in the oxide grown on silicon surfaces

Oxide charge



Energy band diagram for an MOS structure in the presence of positive charge in the oxide

- Assuming that there is an effective total positive charge in the oxide (Q_{OX})located at the metal-oxide interface .

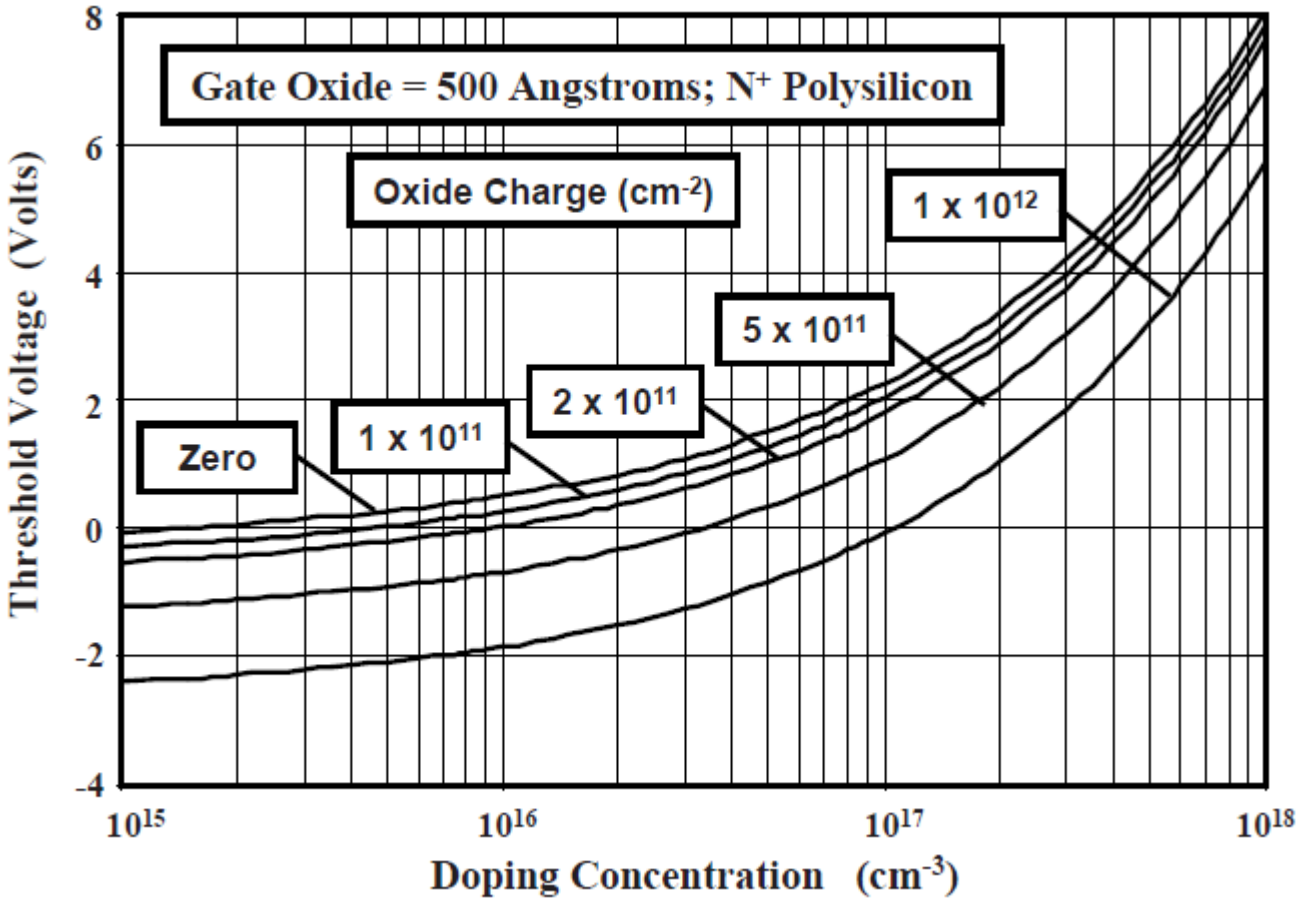
$$Q_{OX} = Q_T + Q_F + Q_{Na} + Q_I$$

- The band bending for the case of a P-type semiconductor creates a depletion region.
- The impact of the positive charge in the oxide on the threshold voltage is give by:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A/n_i)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}}$$

Oxide charge

- The threshold voltage is shifted in the negative direction.
- It is desirable from the point of view of increasing the doping concentration for P-base region.



Threshold voltage shift for silicon n-channel power MOSFET structures due to oxide charge

Calculate the threshold Voltage

- A MOSFET with a p body doping concentration (Na) of 1016 /cm^3 and a gate oxide thickness of 100 nm, made of Silicon Dioxide. The channel length is 3 μm and the channel mobility is 1000 cm^2/Vsec. What is the threshold voltage at room temperature?

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_S kT N_A \ln\left(\frac{N_A}{n_i}\right)}$$

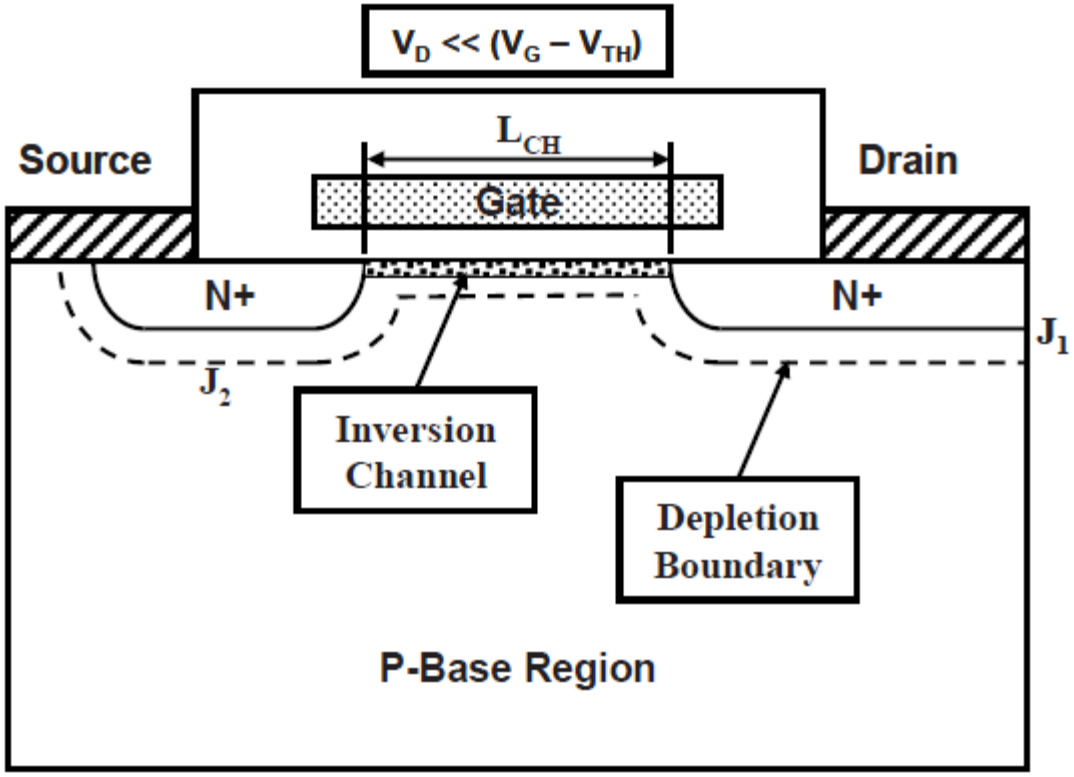
V_{TH}= 2.099 V.

- If a fixed oxide charge of 2e11/cm^2 is introduced, what is the effect?

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kT N_A \ln\left(N_A/n_i\right)}}{C_{OX}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{OX}}{C_{OX}}$$

- **If Vth of 4 V is desired, what needs to be changed and why?**

Channel resistance of a Low Voltage MOSFET



Lateral MOSFET structure representing the channel region under very small drain bias voltages

- A strong inversion layer forms due to the gate voltage above the threshold voltage.
- The on-state current flows through n channel.
- The electrical properties of the channel determine the on-state resistance and the output characteristics of the device.
- The contact to the P-base region (or substrate for the lateral MOSFET structure) is achieved by overlapping the source contact metal with the junction J_2 between source and P region.

Channel resistance

- The charge in the channel under the gate is given by:

$$Q_n = C_{OX}(V_G - V_{TH})$$

- The charge in the inversion layer is uniform throughout the channel. This is indicated as a channel with constant thickness along the entire channel.

The resistance of the channel is then given by:

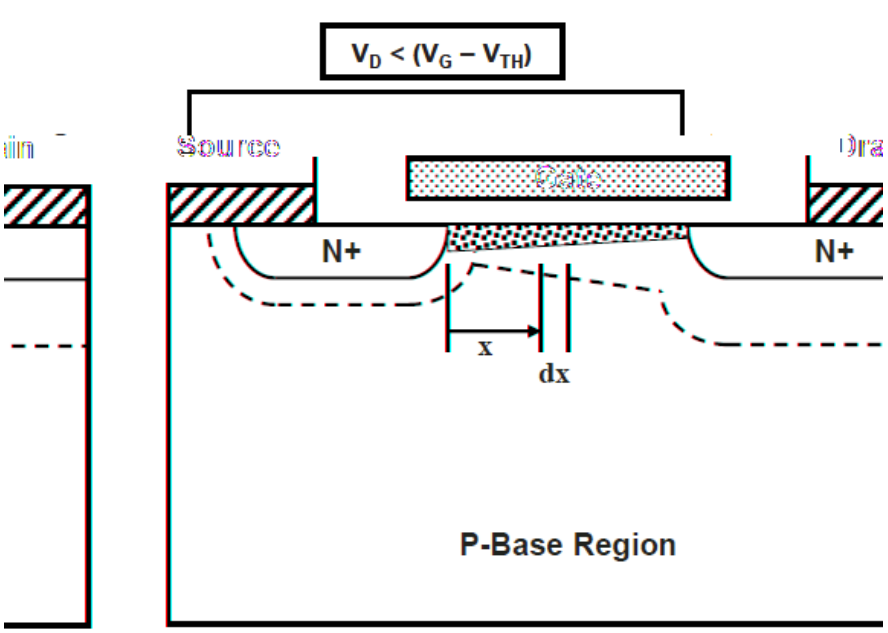
$$R_{CH} = \frac{L_{CH}}{Z\mu_n C_{OX}(V_G - V_{TH})}$$

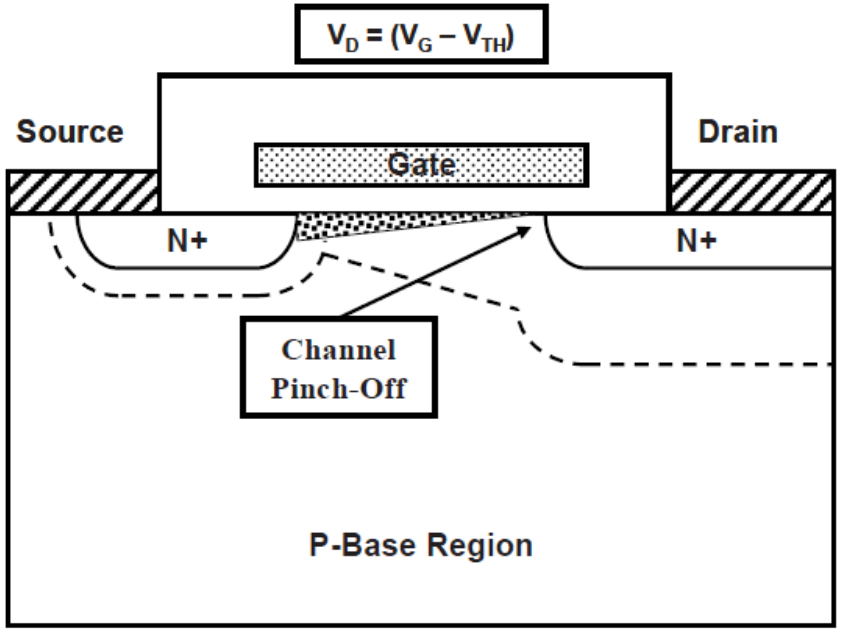
Where L_{CH} is the channel length, Z is the channel width orthogonal to the cross section, and μ_n is the inversion layer mobility for electrons.

The local channel conductivity is

$$\sigma(x) = q.\mu_n.n(x) = \mu_n Q_n(x)$$

Channel pinch-off in a LV MOSFET

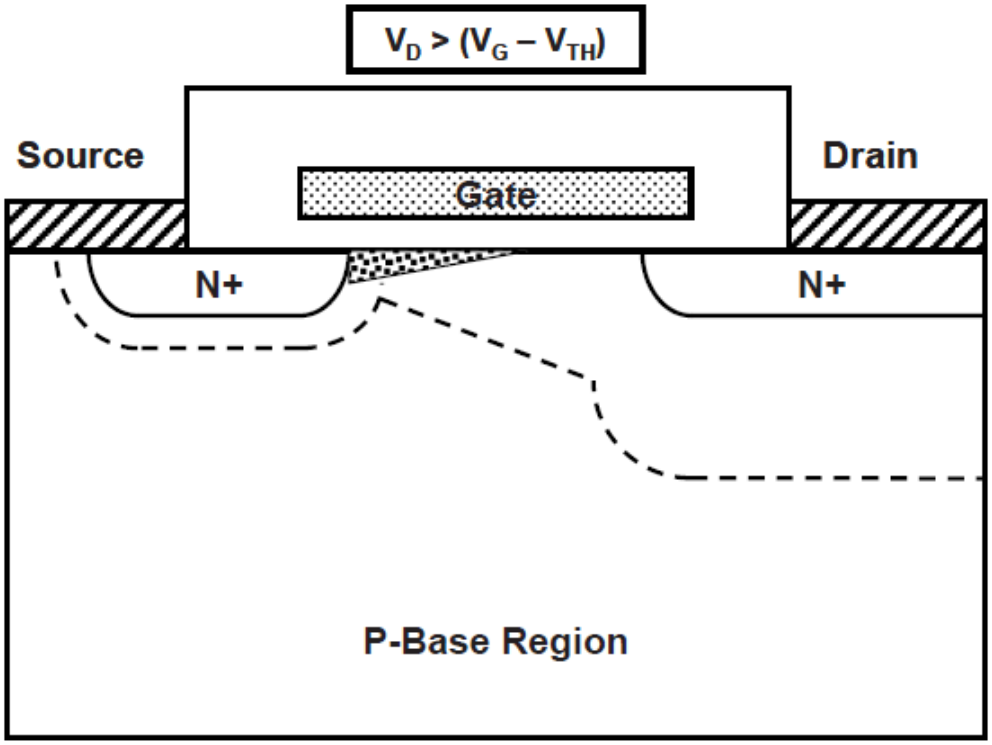




- When the current flowing through the channel increases, a finite voltage drop occurs along the channel due to its finite resistance.
- The positive voltage developed in the channel.
- The charge formed in the inversion layer becomes smaller at the drain end of the channel.

- When the drain voltage equals the difference between the gate bias voltage and threshold voltage, there is no longer sufficient voltage to produce a strong inversion layer at the drain end as shown. This situation is referred to as channel pinch-off.

Channel pinch-off in a MOSFET



- When the pinch-off conditions happen, the drain current remains constant.

- The drain current flow can still occur
  - Electrons are transported from the edge of the inversion layer through the depletion region by the prevailing longitudinal electrical field.

I-V behaviour of a LV MOSFET

$$Q_n(x) = C_{ox} \cdot [V_{GS} - V_T - V(x)]$$
$$\sigma(x) = q\mu_n \cdot n(x) = \mu_n \cdot Q_n(x)$$
$$dV = I_D \cdot \frac{1}{\sigma(x) \cdot W} \cdot dx = \frac{I_D}{\mu_n Q_n(x) W} \cdot dx$$

$$I_D dx = \mu_n W C_{ox} [V_{GS} - V_T - V(x)] \cdot dV$$

$$\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n W C_{ox} [V_{GS} - V_T - V(x)] \cdot dV$$

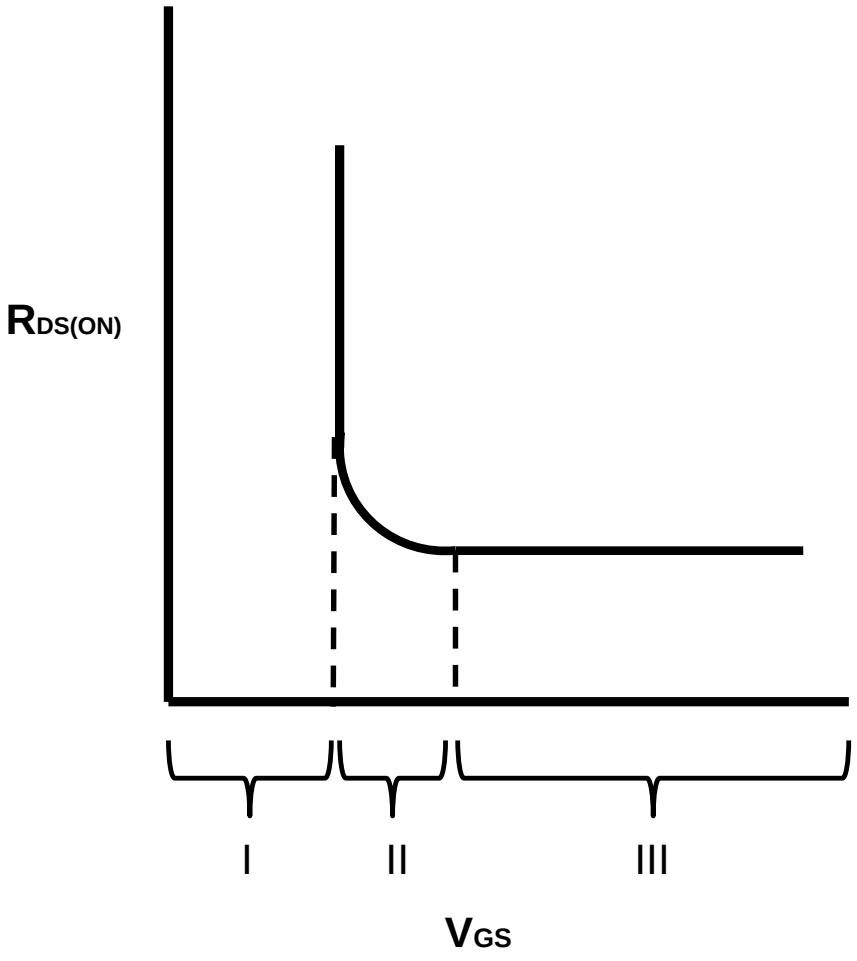
$$\boldsymbol{I_D = \mu_n \frac{W}{L} \cdot \frac{C_{ox}}{2} \cdot [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]}$$

Pinch-Off Voltage:

$$\frac{dI_D}{dV_{DS}} = 0$$

$$\boldsymbol{V_{DS(sat)} = V_{GS} - V_T}$$

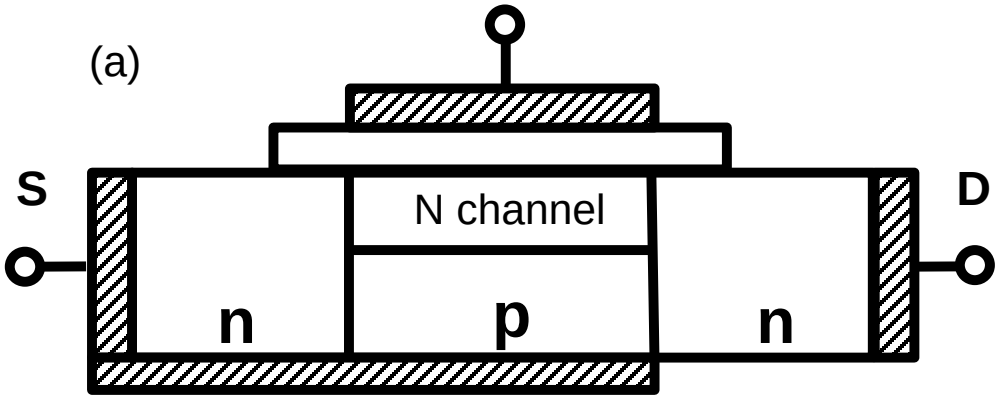
Principles of MOSFET operation

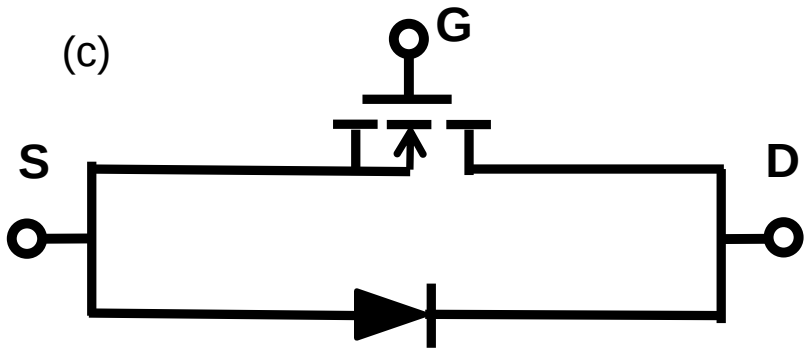


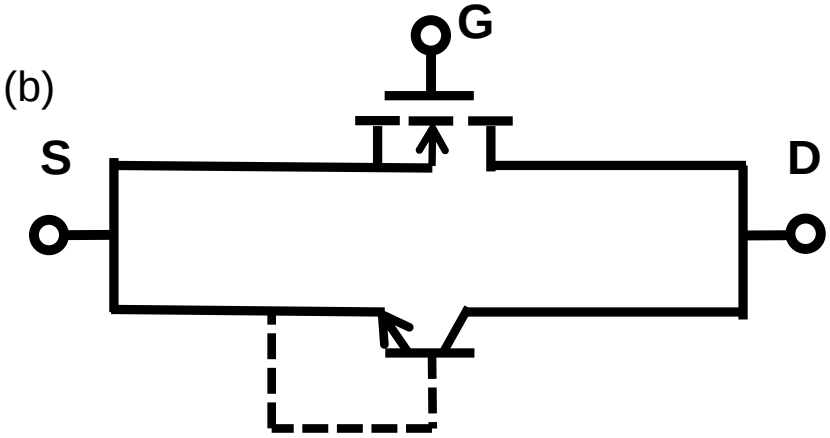
MOSFET turn-on characteristic

- As the gate-body potential is increased, more charge collects in the channel region.
- Region I corresponds to the condition when the accumulative charge is not sufficient to cause an inversion.
- Region II corresponds to the condition where sufficient charge is present to invert a portion of the *p* region, forming the channel, but not enough.
- Region III corresponds to the charge limited condition where $R_{DS(ON)}$ does not change appreciably as the gate-body potential is raised above the threshold voltage V_{th}.

The body diode in a LV MOSFET

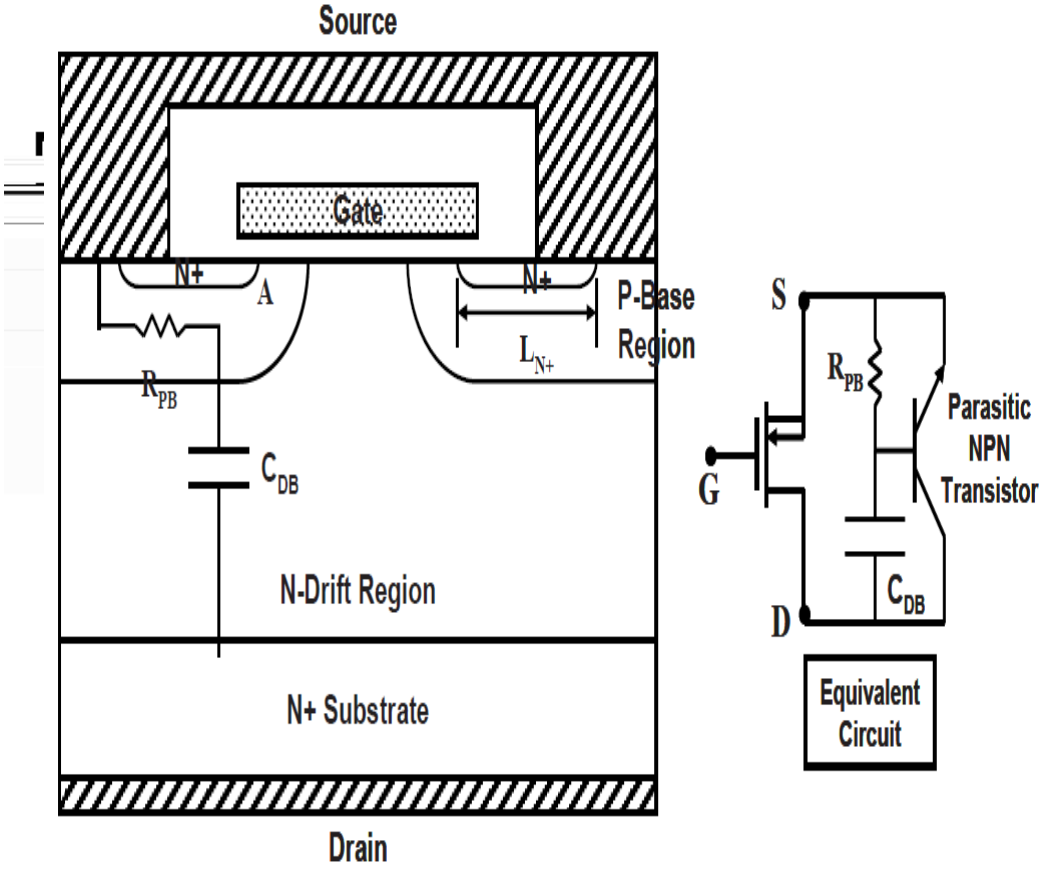






- The normal practice is to connect the body directly to the source terminal as shown in (a).
- To turn the device ON, the gate is made positive with respect to the source.
- The body-source connection places a short between the base and the emitter of the parasitic *npn* BJT as shown in (b).
- The base-collector junction is still present so that the equivalent circuit for the MOSFET is a MOSFET in parallel with a diode as shown in (c).

Power MOSFET – needs to withstand rated voltage



Vertical MOSFET structure

The power MOSFET structure is capable of supporting a high voltage.

During operation in the blocking mode, the gate electrode is shorted to the source electrode.

A positive drain bias voltage produces a reverse bias across junction J_1 between the P-base region and N-drift region.

Most of the applied voltage is supported across the reverse biased p base/N-drift region. The depletion capacitance supports the voltage.

- Avoid the depletion region in the P-base reaching through to the N-source region; this is called reach-through breakdown.

How does it block the voltage?

- The doping and thickness of the N-drift region must be chosen to achieve a parallel-plane breakdown voltage:

$$N_D = \sqrt[4/3]{\frac{5.34 \times 10^{13}}{BV_{PP}}}$$

The thickness with the above doping concentration is given by

$$t = W_D(BV) = \sqrt{\frac{2\varepsilon_S BV}{qN_D}}$$

Impact of Edge Termination

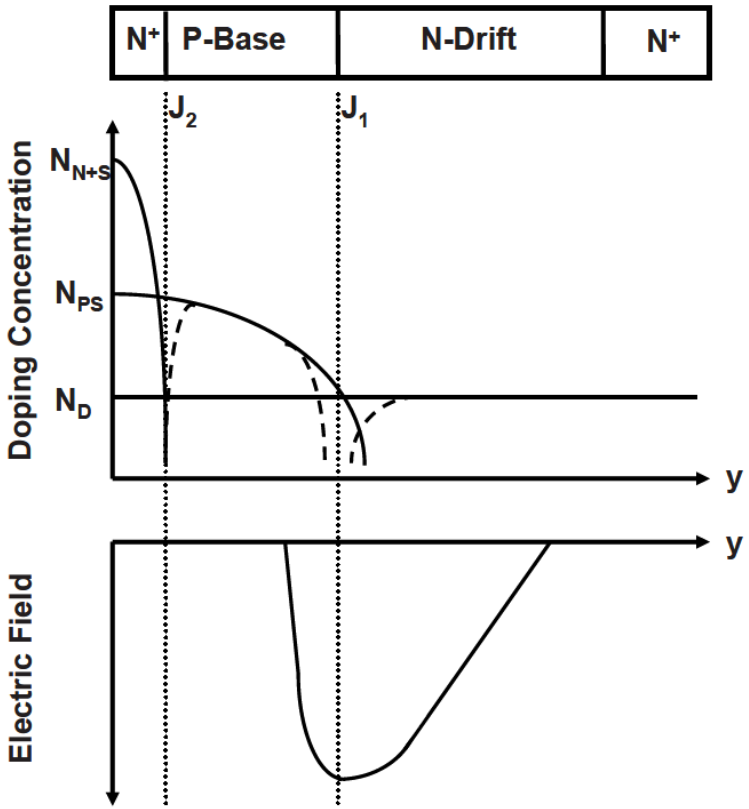
- The maximum blocking voltage (BV) is invariably decided by the edge termination surrounding the device cell structure.
- The enhanced electric field at the edges limits the breakdown voltage to about 80% of the parallel-plane breakdown voltage (BV_{pp}):

$$BV_{PP} = \frac{BV}{0.8}$$

Doping profile considerations for BV

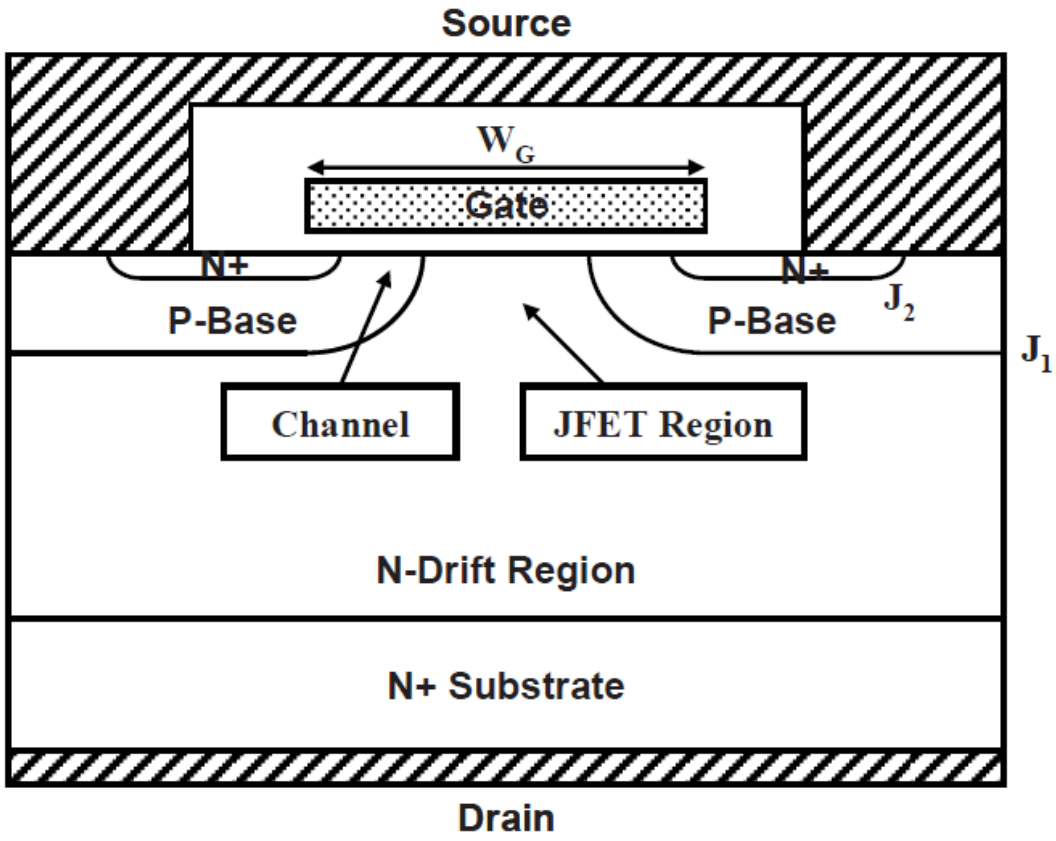
Graded Doping Profile

- A graded doping profile for the junction J_1 between the P-base region and the N-drift region
- The concentrations of the donors and acceptors are shown by the solid lines while the dashed lines represent the net doping concentration after taking into account compensation near the junction.
- The electric field extends on both sides of junction J1
- P-base region supports a portion of the applied positive drain voltage
  - The same breakdown voltage can be achieved with a larger doping concentration and a smaller thickness for the N-drift region



Doping profile and electric field distribution for the power MOSFET structure

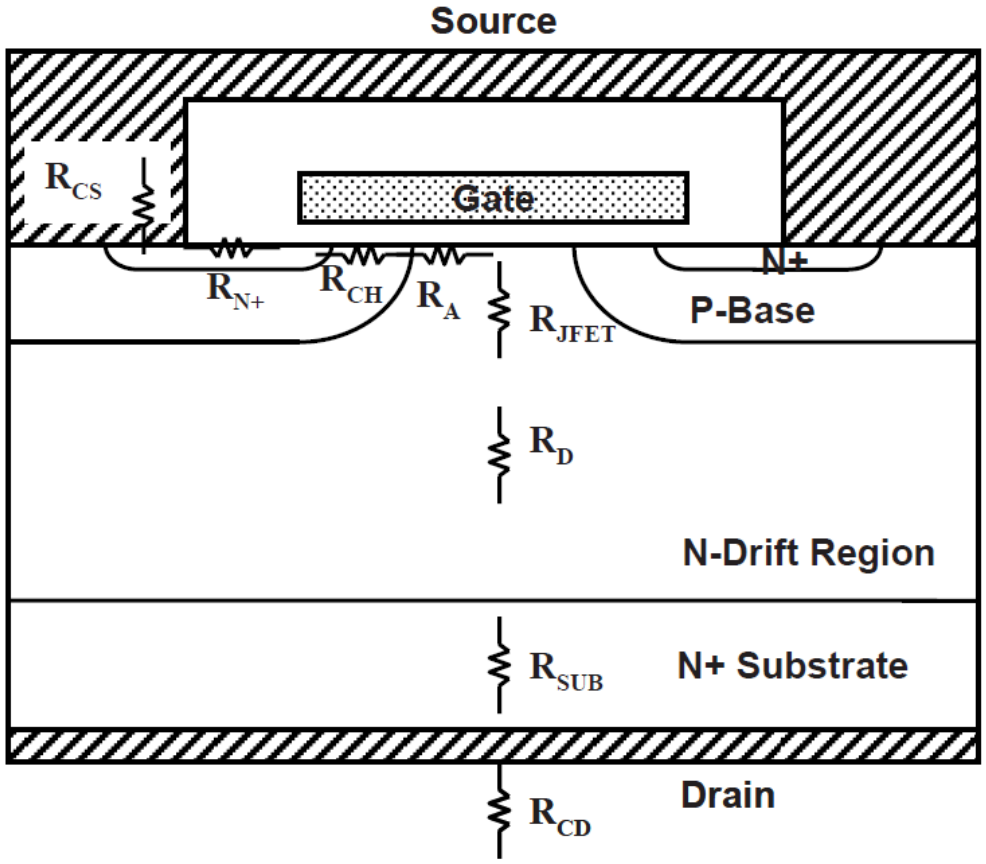
The structure of the planar MOSFET



Vertical-diffused (VD)-MOSFET structure

- Fabricated by starting with an N-type epitaxial layer grown on a heavily doped N+ substrate.
- P-base and N+ source regions are both self-aligned to the left-hand side and right-hand side of the gate region.
- High internal resistance due to the existence of a relatively narrow JFET region.
  ➢Motivation for the development of the trench-gate power MOSFET structure in the 1990s.

The on-resistance of the planar MOSFET

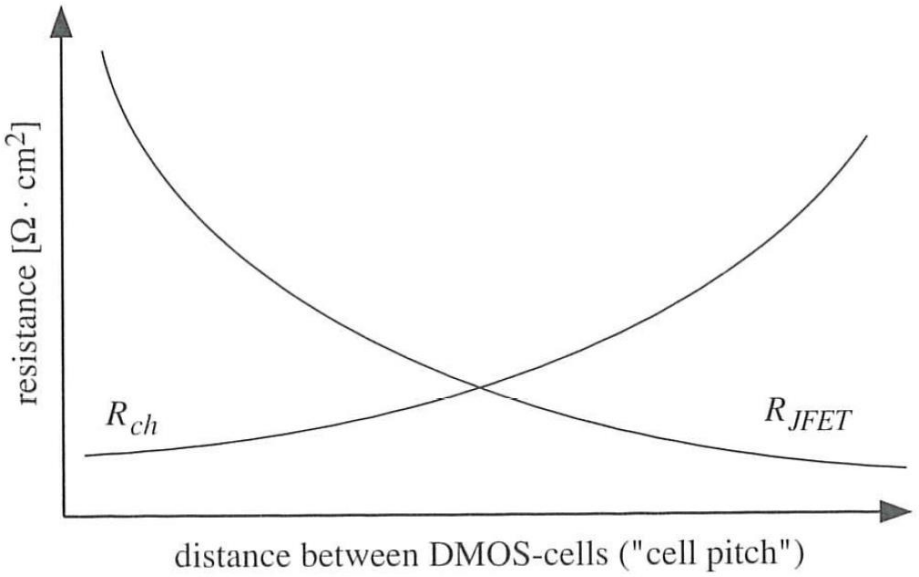


The total on-resistance is obtained by the addition of all the resistances because they are considered to be in series in the current path between the source and drain electrodes:

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD}$$

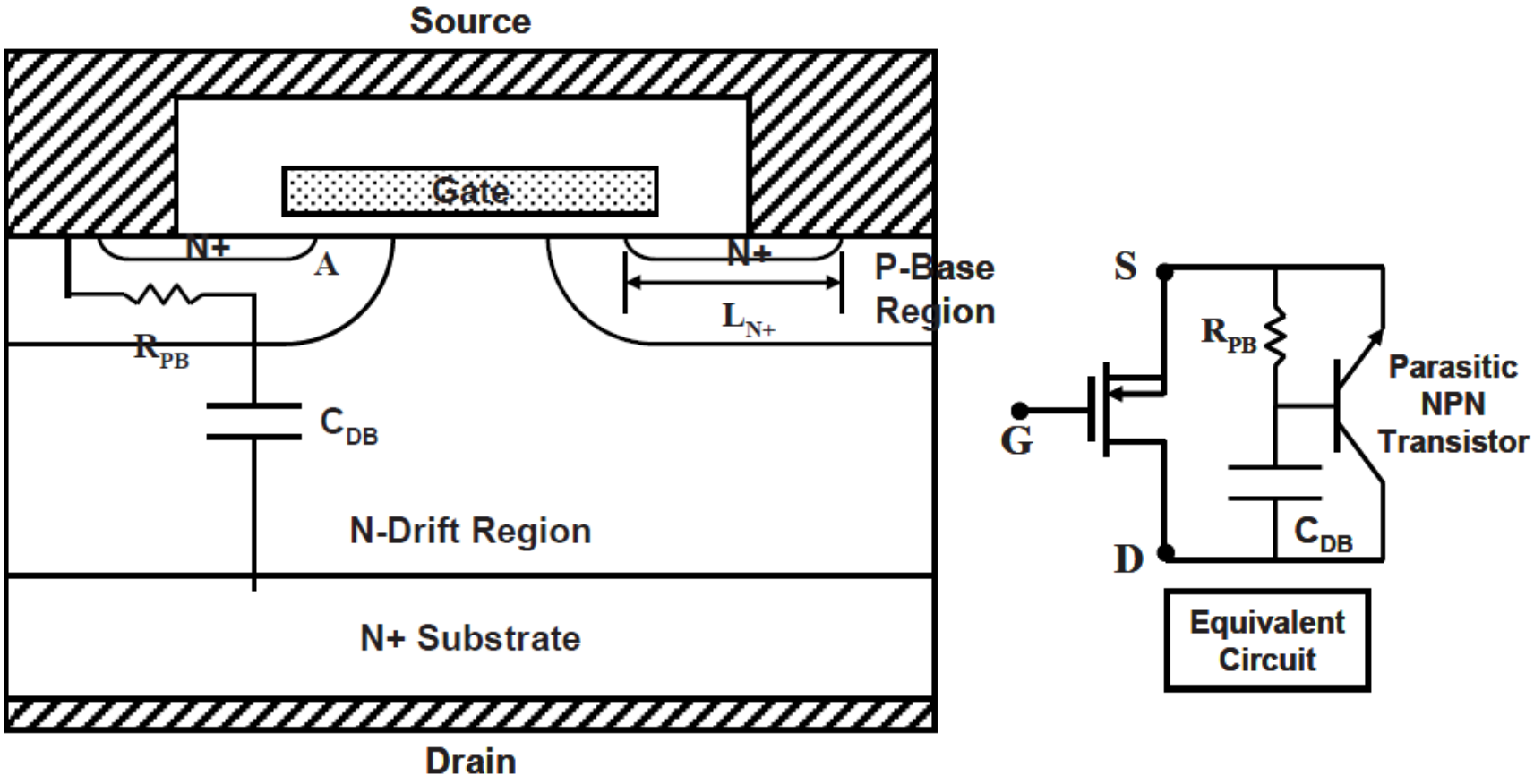
How does On-state resistance compare between 30 V MOSFET and 600 V MOSFET

$$R_{drift} \sim V_{BV}^{2.5}$$



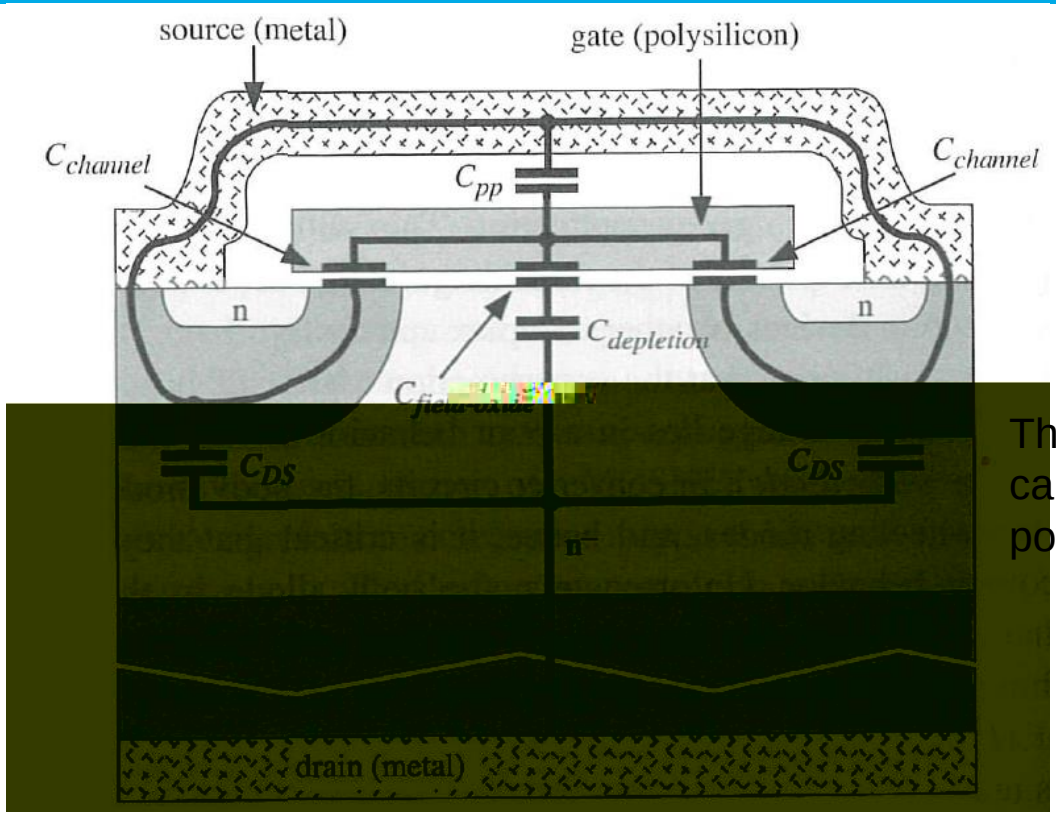
Component	$V_{br(DSS)}$ = 30 V	$V_{br(DSS)}$ = 600 V
R_{n+}	6 %	0.5 %
R_{ch}	30 %	1.5 %
$R_{acc} + R_{JFET}$	25 %	0.5 %
R_{drift}	31 %	97 %
R_{drain}	8 %	0.5 %

Bipolar turn-on in a power MOSFET



- The power MOSFET structure contains an inherent parasitic N-P-N bipolar transistor formed between the two internal junctions.
- The turn-on of the bipolar transistor is suppressed by short circuiting the junction between the source and P-base regions.

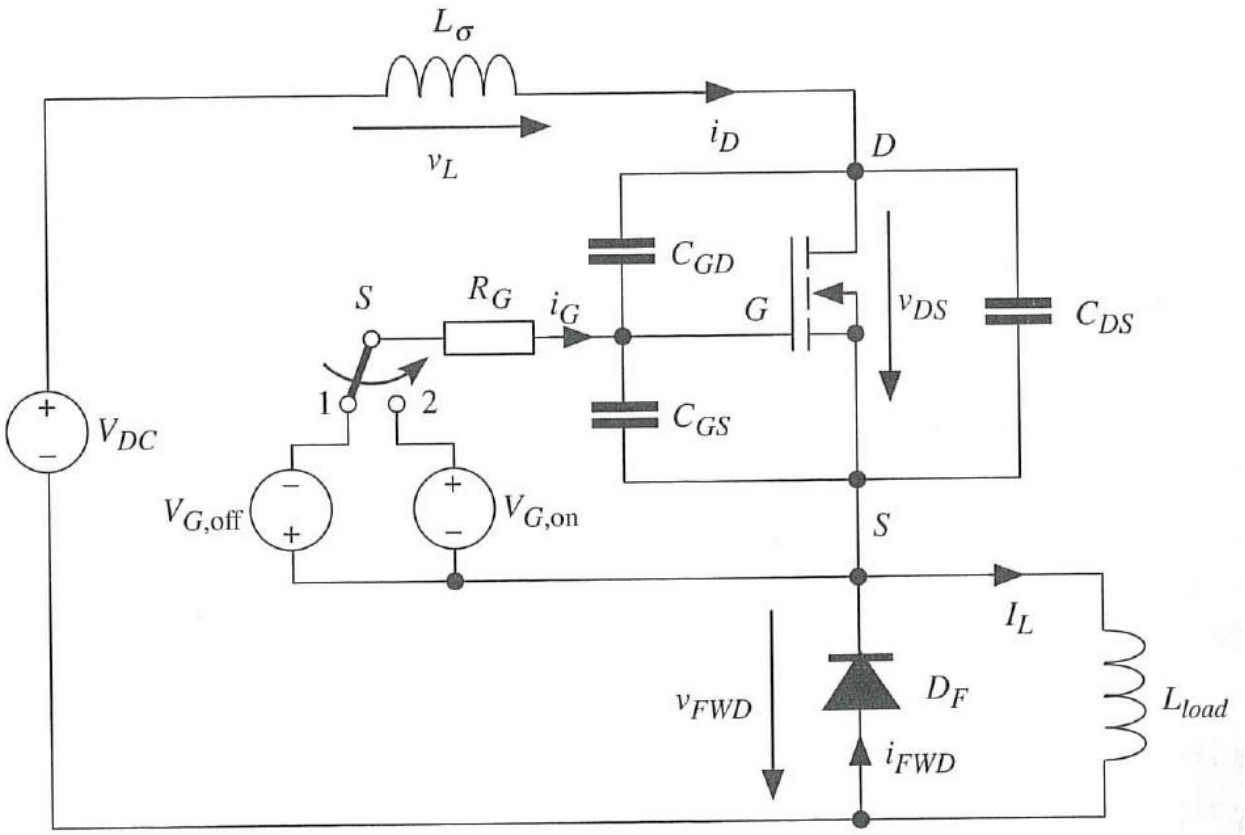
Switching performance



The internal coupling capacitances of the power MOSFET

- The switching transients are mainly determined by the charging and discharging processes of its internal capacitances.
- The Gate-Source Capacitance C_{GS}: $C_{channel}$ and C_{pp}
- The Gate-Drain Capacitance C_{GD} (***reverse transfer capacitance***): $C_{field-oxide}$ and $C_{depletion}$
- The Drain-Source Capacitance C_{DS}
- **The Input Capacitance: $C_{iss} = C_{GS} + C_{GD}$**
- **The Output Capacitance: $C_{oss} = C_{DS} + C_{GD}$**

Switching performance

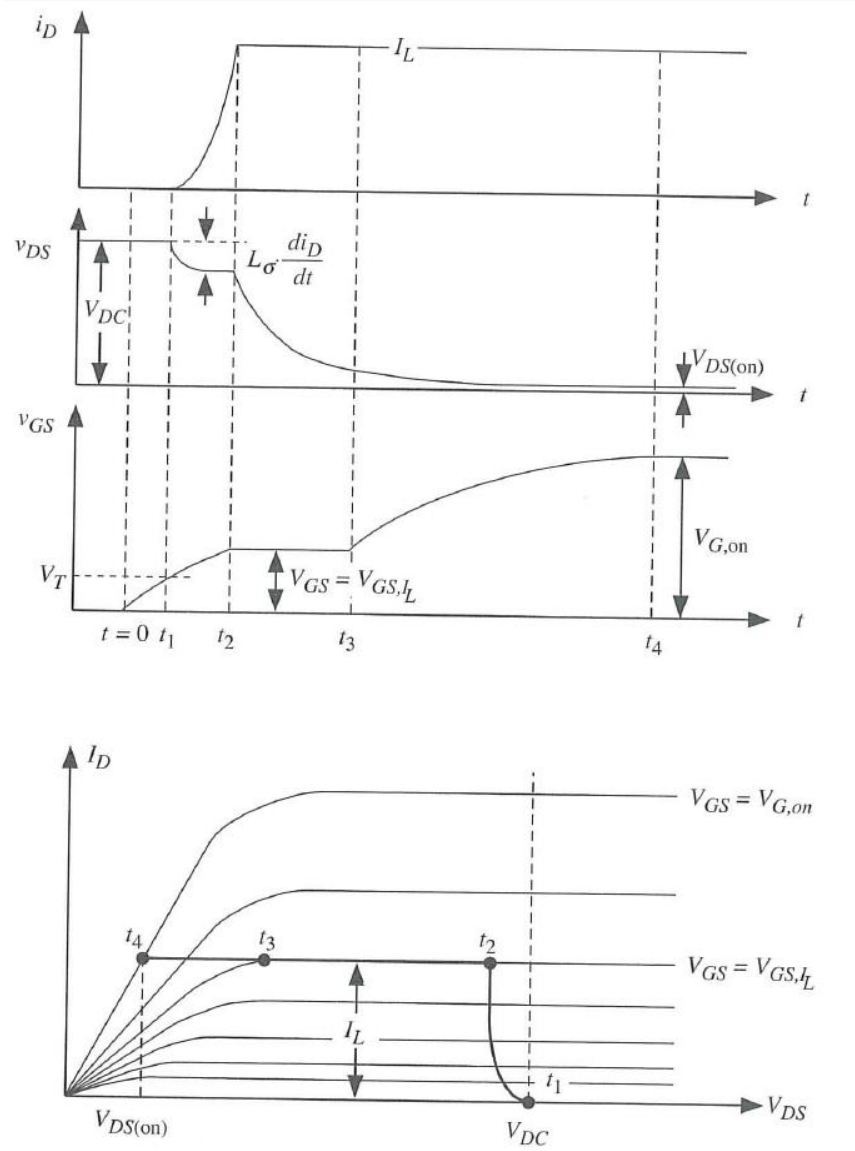


Test circuit to analyse the MOSFET's switching behaviour

- Switching test circuit for a power MOSFET
- The load inductor L_{load} and freewheeling diode D_F
- Simplifications for the switching test:
  - No reverse current for diode D_F
  - $V_{G,off}$ is zero

The Turn-

The Turn-on of the MOSFET



Turn-on of the MOSFET

Phase 3 (t2 to t3):

At time t2, the gate-source voltage has reached the value

$$V_{GS,I_L} = \sqrt{\frac{2 \cdot I_L \cdot L}{\mu_n \cdot W \cdot C_{ox}}} + V_T$$

The whole of the gate current now flows into the reverse transfer capacitance C_{GD}

$$I_G = \frac{V_{G,on} - V_{GS,I_L}}{R_G}$$

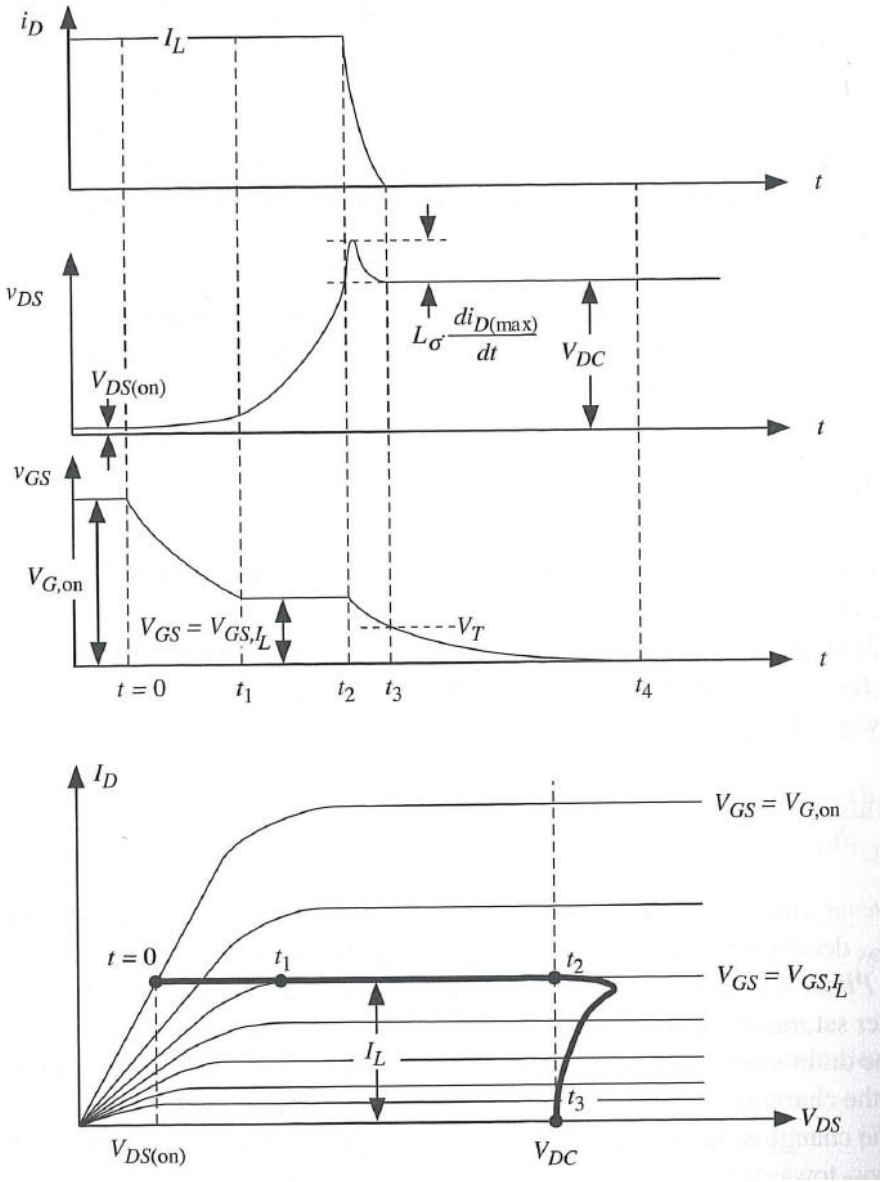
The derivative of the drain-source voltage is given by

$$\frac{dv_{DS}}{dt} = \frac{I_G}{C_{GD}} = \frac{V_{G,on} - V_{GS,I_L}}{R_G \cdot C_{GD}}$$

Phase 4 (t3 to t4):

- v_{GS} must now increase in order to support the current I_L.
- A smaller C_{iss} results in a faster reduction of v_{DS}

The Turn-off of the MOSFET



Turn-off of the MOSFET

Phase 1 (t=0 to t1):

The value of v_{GS} over time is given by

$$v_{GS}(t) = V_{G,on} \cdot e^{-\frac{t}{\tau_2}}$$

With

$$\tau_2 = R_G \cdot (Ciss)$$

Phase 2 (t1 to t2):

During the build-up phase of v_{DS}, the gate source voltage must remain at a constant value. The gate current is

$$I_G = \frac{V_{GS,I_L}}{R_G}$$

The drain-source voltage v_{DS} increases

$$\frac{dv_{DS}}{dt} = \frac{I_G}{C_{GD}} = \frac{V_{GS,I_L}}{R_G \cdot C_{GD}}$$

The Turn-off of the MOSFET

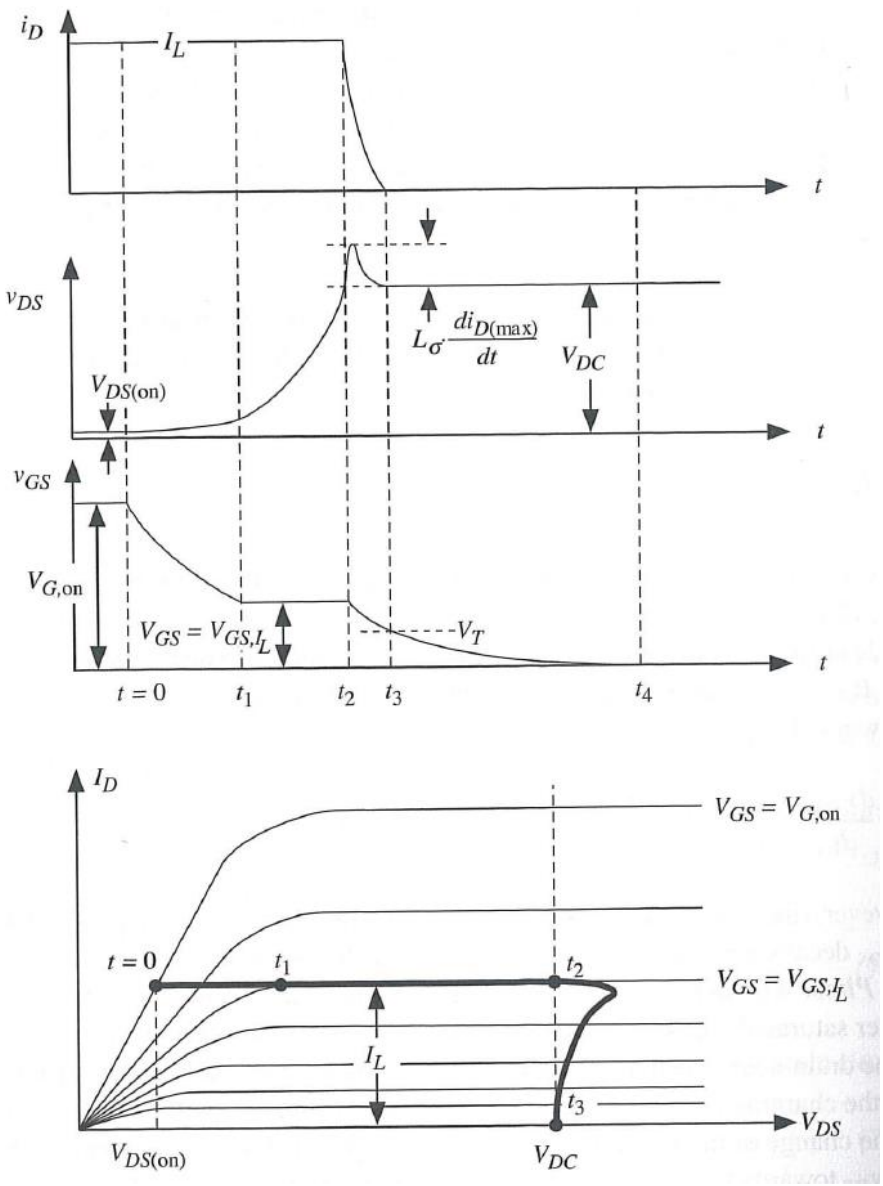


Figure 28 Turn-off of the MOSFET

Phase 3 (t2 to t3):

The discharging of C_{GS} can resume

$$v_{GS}(t - t_2) = V_{GS,I_L} \cdot e^{-\frac{t}{\tau_3}}$$

With

$$\tau_3 = R_G \cdot (Ciss)$$

The falling v_{GS} forces the drain current to drop after t2

$$i_D(t - t_2) = \mu_n \cdot \frac{W}{L} \cdot \frac{C_{ox}}{2} \cdot (V_{GS,I_L} \cdot e^{-\frac{t}{\tau_3}} - V_T)^2$$

The overvoltage peak ΔV_{max} occurs when the $\frac{di_D}{dt}$ is highest

$$\Delta V_{max} = L_\sigma \cdot \mu_n \cdot \frac{W}{L} \cdot C_{ox} \cdot \frac{V_{GS,I_L}}{\tau_1} \cdot (V_{GS,I_L} - V_T)$$

Phase 4 (t3 to t4):

At time t3, V_{GS} drops below the threshold voltage and the drain current falls to zero.

Switching power loss

- The device incurs power dissipation during the on-state due to its finite on-resistance and during the two switching intervals for each operating cycle:

$$P_T = P_{ON} + P_{TURN-ON} + P_{TURN-OFF}$$

The on-state power loss is given by

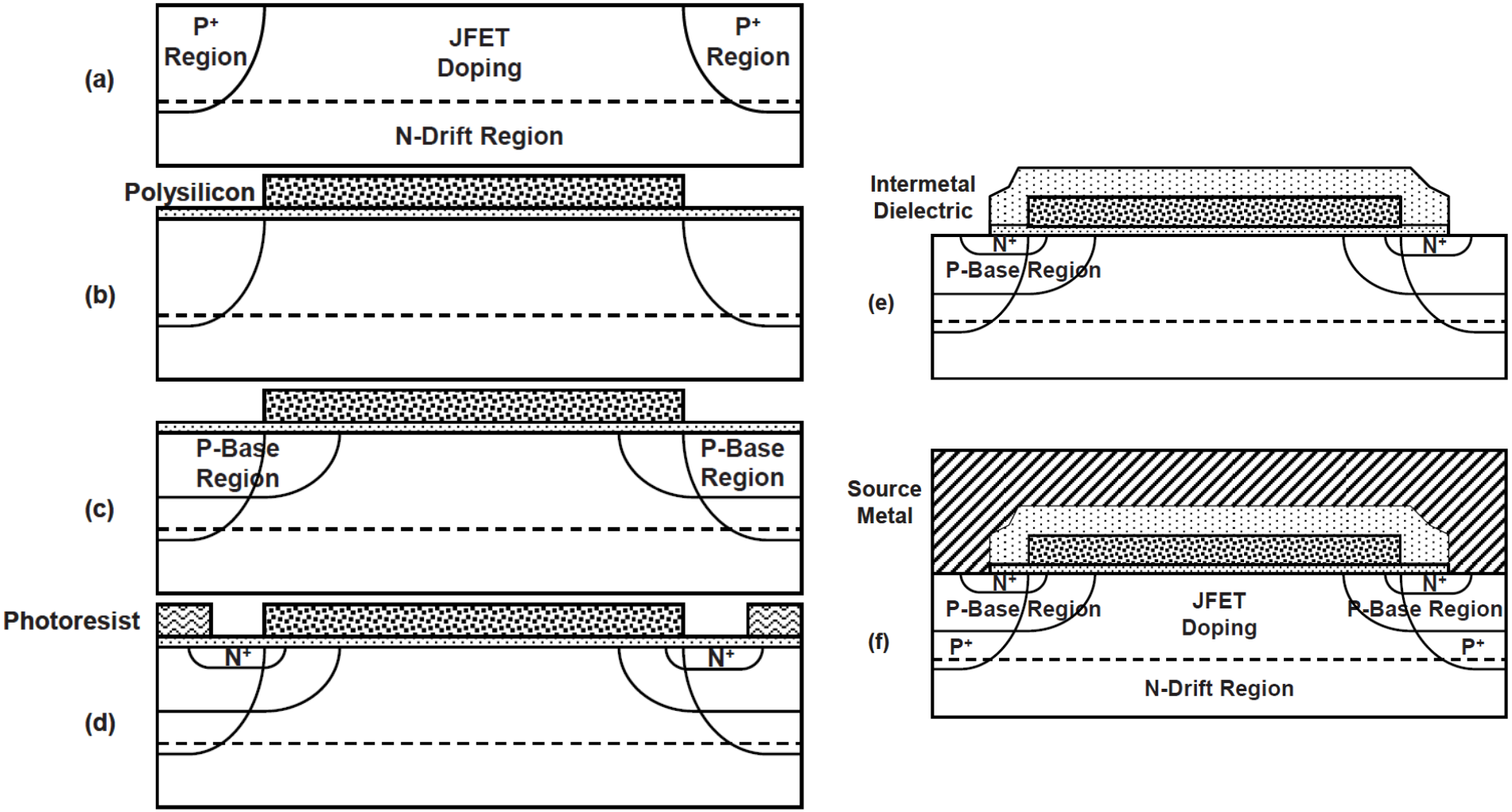
$$P_{ON} = \frac{t_{ON}}{T} R_{ON} I_L^2$$

Where the first term is the duty cycle (on-time t_{ON} divided by the period T) for the power MOSFET device.

The switching power losses are generated during the phase in which the gate-source voltage is constant (t2-t3 and t1-t2 during turn-on and turn-off, respectively). The reverse transfer capacitance must be charged and discharged as quickly as possible.

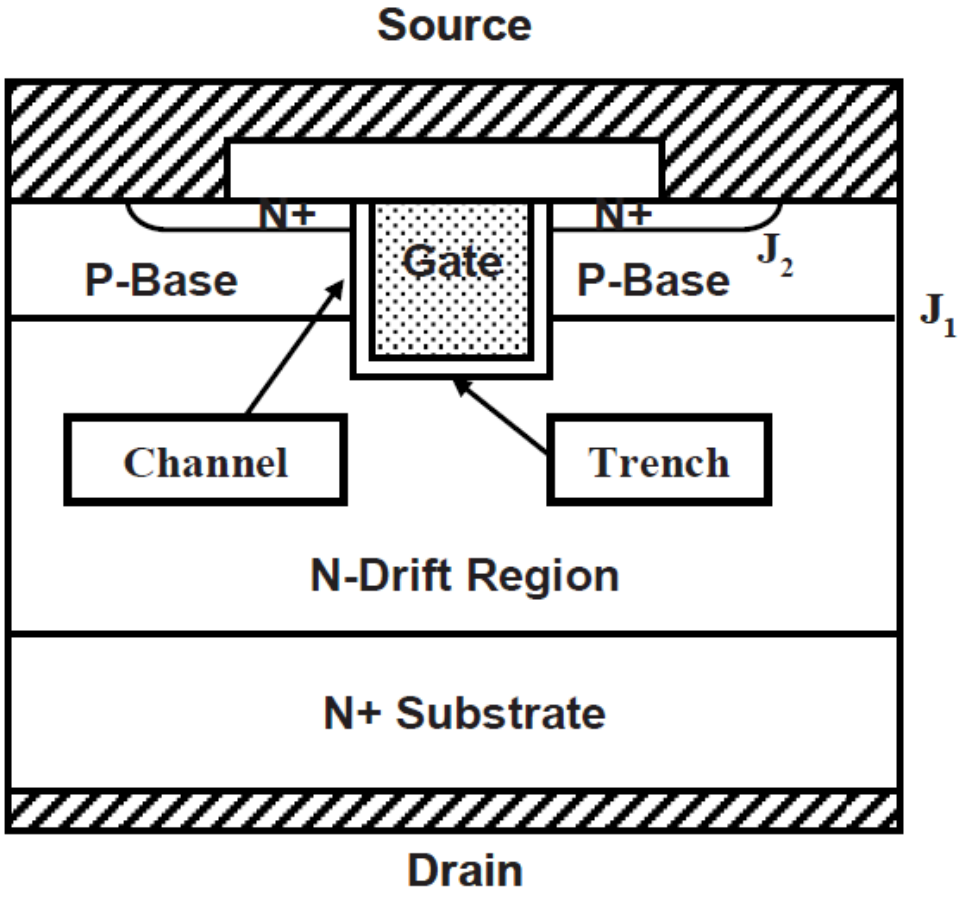
The switching power losses are proportional to the frequency of operation.

Planar MOSFET process



Fabrication process for the power VD-MOSFET structure

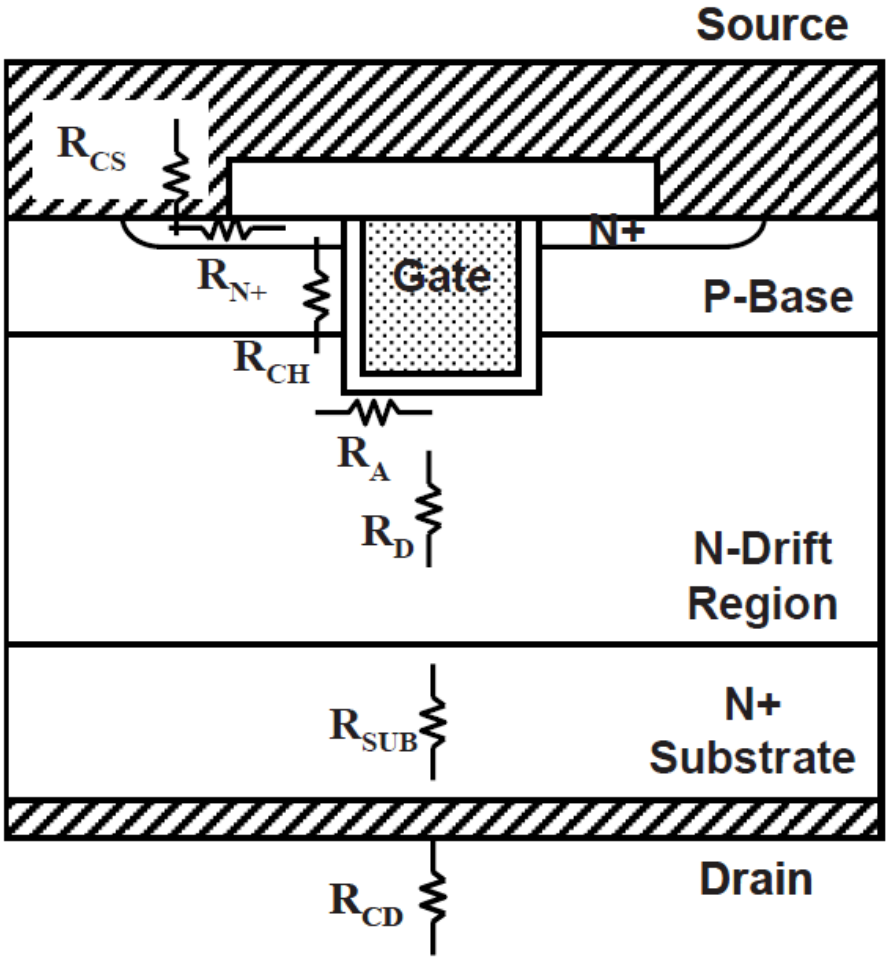
The structure of the U-MOSFET



U-MOSFET structure

- The trench extends from the upper surface of the structure through source and base regions in to the drift region.
- It is customary to round the bottom of the trench.
- No JFET region in the U-MOSFET structure.
- A significant reduction of the internal resistance when compared with VD-MOSFET.

The on-resistance of the U-MOSFET

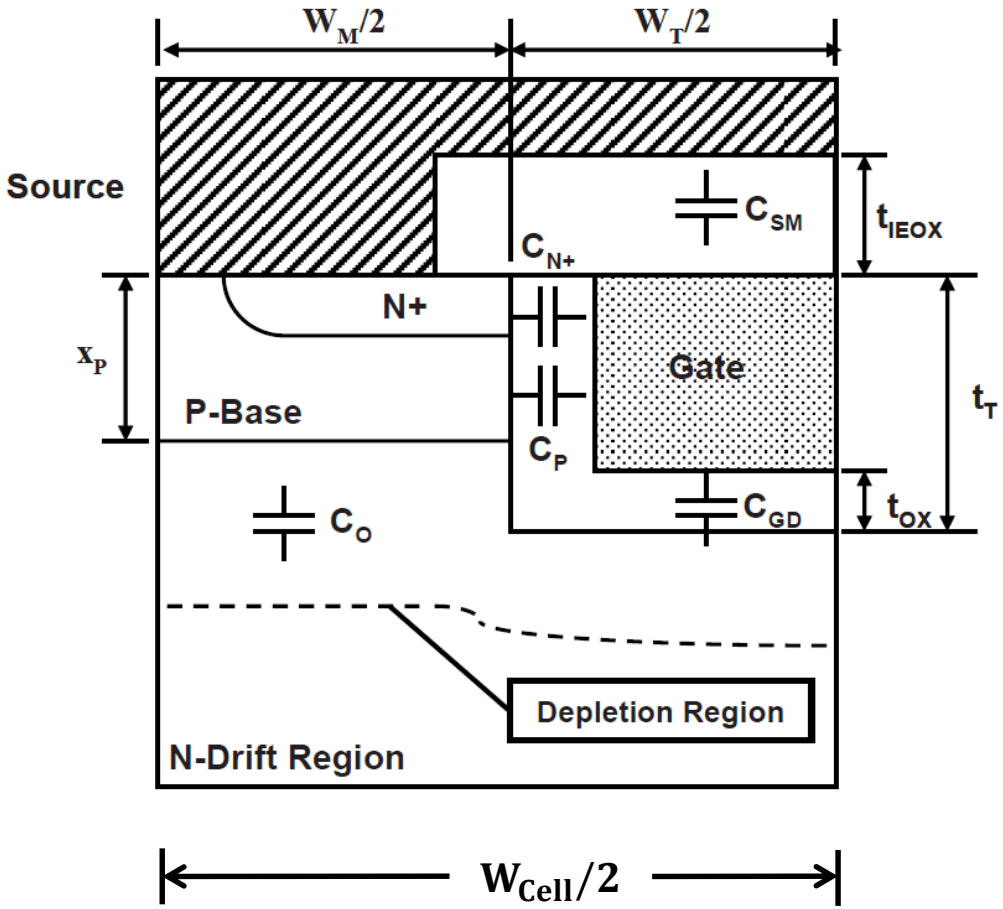


Power U-MOSFET structure with its internal resistances

It is customary to utilize the linear cell surface topology for the power U-MOSFET structure because the trench surface can be oriented in the preferred direction most favourable for producing high-quality etched surfaces

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_D + R_{SUB} + R_{CD}$$

Power U-MOSFET structure capacitances



The specific input (or gate) capacitance can be obtained:

$$C_{IN,SP} = C_{N+} + C_P + C_{SM} = \frac{2x_P}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_T}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right)$$

Where t_{OX} and t_{IEOX} are the thicknesses of the gate and interelectrode oxides.

Power U-MOSFET structure capacitances

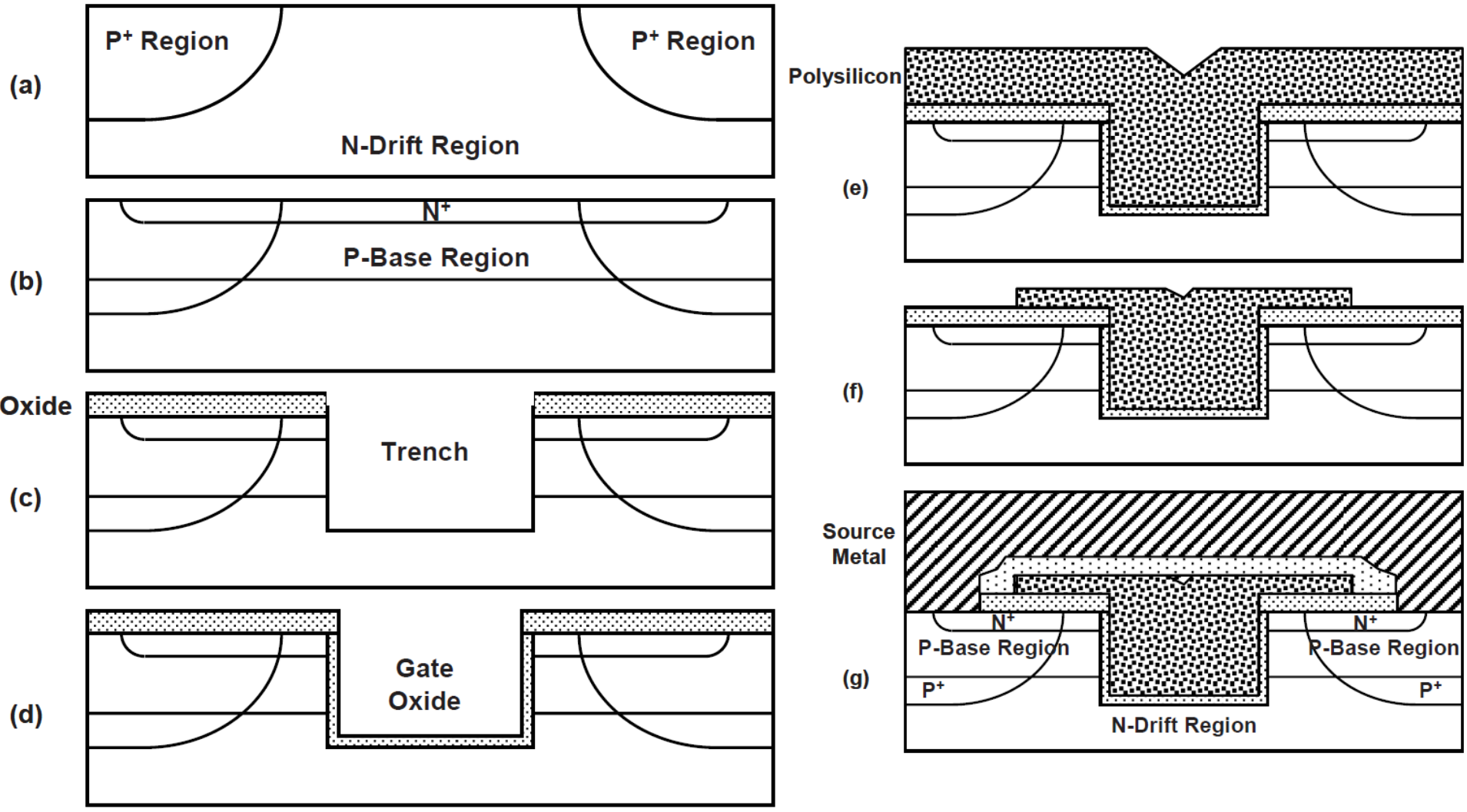
- Under depletion conditions, the gate-drain (or reverse transfer) capacitance is given by:

$$C_{GD,SP} = [\frac{W_T - 2(t_T - x_P)}{W_{Cell}}] \left(\frac{C_{OX} C_{S,M}}{C_{OX} + C_{S,M}} \right)$$

Where $C_{S,M}$ is the semiconductor capacitance under the gate oxide, which decreases with increasing drain bias voltage.

- $C_{S,M}$ can be obtained with the depletion layer width under the gate oxide as previously derived for the power planar MOSFET structure.

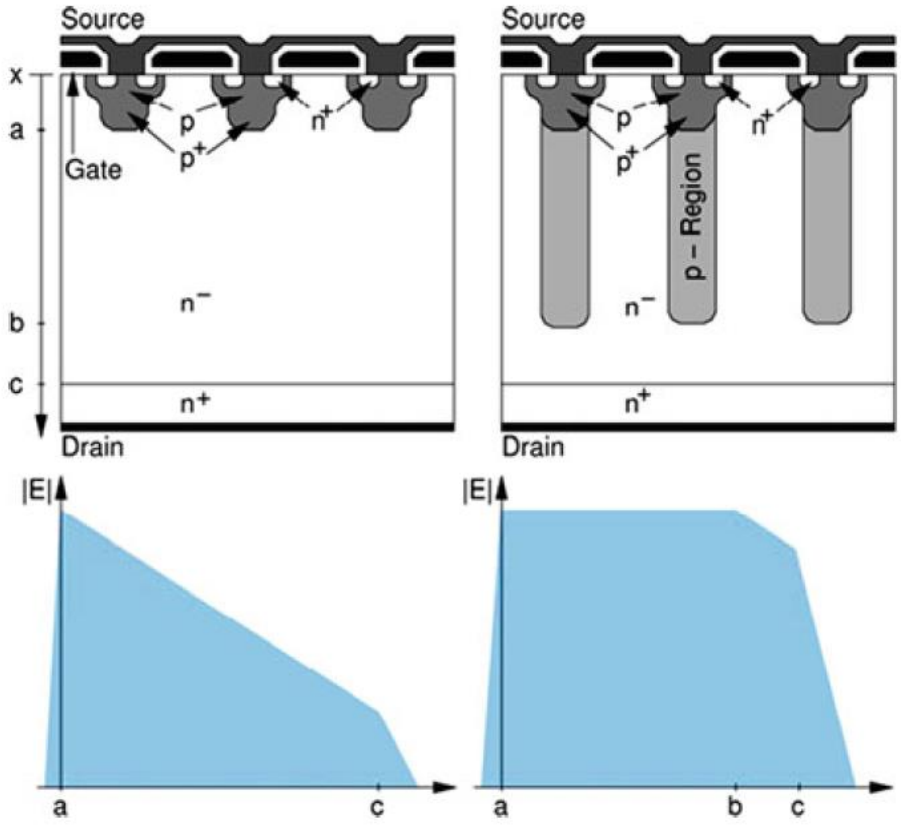
Trench U-MOSFET process



Fabrication process for the power U-MOSFET structure

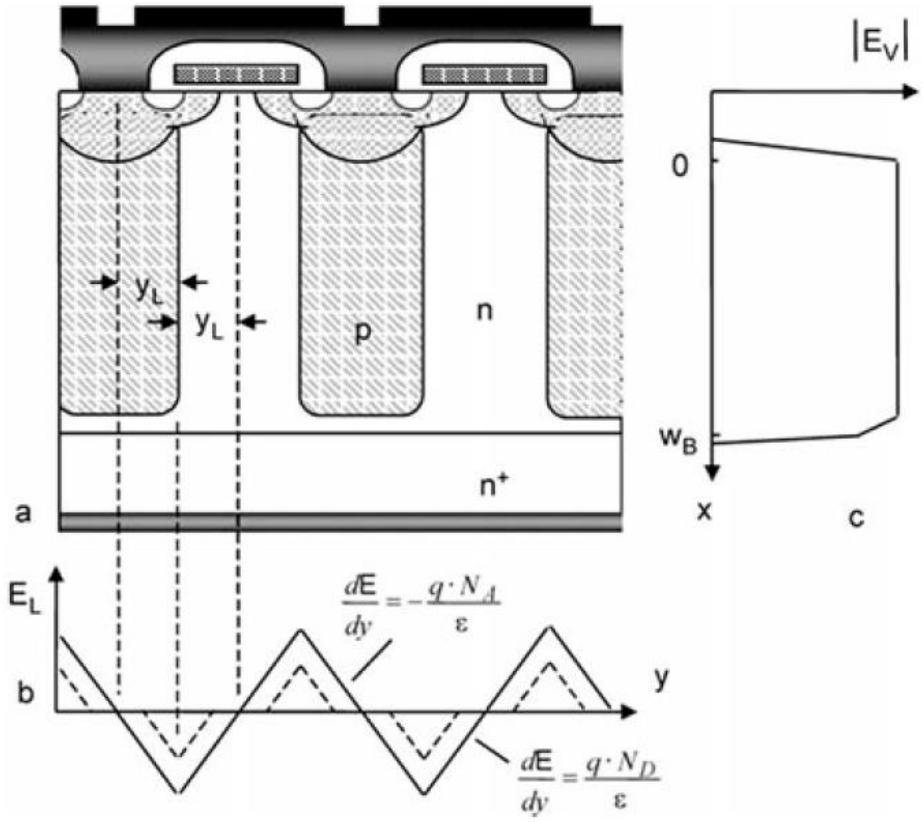
Compensation structure in Modern MOSFETs

- The compensation principle for power MOSFETs has been introduced in commercially available products in 1998 with the 600-V CoolMOS™ technology.
- In the middle layer, p-columns are arranged. Their p-doping is adjusted to the value necessary for compensation of the n-regions.
- The compensation acceptors are located in lateral proximity to the drift region donors.



- An almost rectangular shape of the electric field is obtained.
- For this filed shape, the highest voltage can be absorbed at a given thickness.

Compensation structure in Modern MOSFETs



(a) Simplified structure
(b) Electric field in lateral direction in the region of columns
(c) Electric field in vertical direction

- Under blocking conditions the space charge laterally penetrates into the n- and p-region.
- It is assumed that p- and n-regions are doped equally: $N_A = N_D$
- When a voltage is applied in reverse direction, the space charge region penetrates only laterally into the columns.

XtreMOS

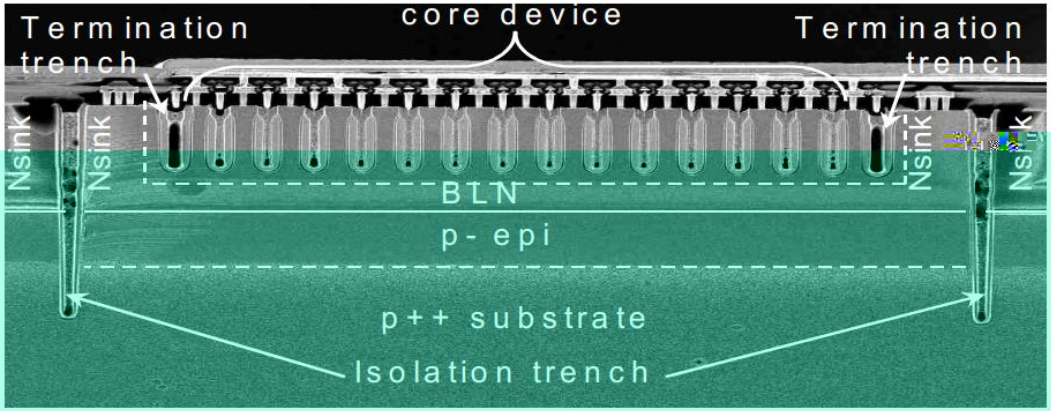


Fig. 1 : XtreMOS cross section, perpendicular to the device W (stripe geometry). The device is isolated from neighboring transistors by deep trench structures. The buried layer BLN is contacted from the top by highly doped n-sinkers, and serves as the drain contact. The dashed lines show transitions between highly and lowly doped region of the same conductivity type. Full lines show p-n junctions.

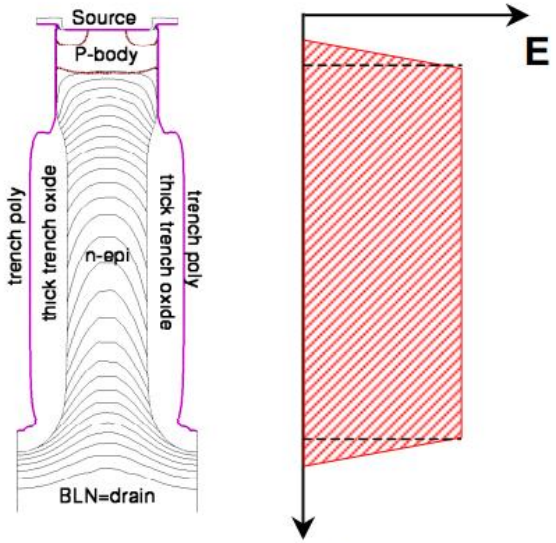


Fig. 3 : TCAD simulation of the potential line distribution at breakdown (V_{ds}=97V). Cross-section perpendicular to W (as in Fig. 1). The electric field along the cross-section is schematically shown at the right.

REF:
Moens, P.; Bauwens, F.; Baele, J.; Vershinin, K.; De Backer, E.; Narayanan, E.M.S.; Tack, M., "XtreMOS : The First Integrated Power Transistor Breaking the Silicon Limit," *Electron Devices Meeting, 2006. IEDM '06. International* , vol., no., pp.1,4, 11-13 Dec. 2006
doi: 10.1109/IEDM.2006.346933