Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (3.0 hours)

EEE339 Digital Engineering

Answer **FIVE QUESTIONS** comprising **AT LEAST TWO** each from **part A** and **part B. No marks will be awarded for solutions to a sixth question or if you answer more than three questions from parts A or B.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Part A

A1. **a.** There are two important differences between the discrete-time and continuous-time complex exponential signals (denoted by $x[n]=e^{j\omega n}$ and $x(t)= e^{j\omega t}$, respectively). Explain in detail the two differences.

(4)

b. A sequence is said to be the eigenfunction of a linear time invariant (LTI) system, when given such a sequence at its input, its output is a simple scaled version of the same sequence. Determine whether the sequence $x[n]=\alpha^n$ (α is a nonzero constant) is the eigenfunction of an LTI system. Explain your answer.

(4)

c. Two LTI systems are connected in cascade and their impulse responses are denoted by $h_1[n]$ and $h_2[n]$, respectively. Explain that the overall impulse response of the cascaded system is given by the convolution of $h_1[n]$ and $h_2[n]$.

(4)

d. Give the transformation equations for the Fourier series (complex-valued), Fourier transform, discrete-time Fourier transform (DTFT), discrete Fourier transform (DFT). (The inverse transform equations are not required). State clearly whether it is applied to periodic or non-periodic, discrete or continuous signals, and the results after transformation are periodic or non-periodic, discrete or continuous.

(8)

A2 **a.** Consider the system function

.

$$H(z)=\frac{1+2z^{-1}}{1-1.5z^{-1}+0.9z^{-2}}$$

Give its direct form I and direct form II implementation structures.

(4)

b. i) Derive the z-transform of the following sequence (4 marks)

$$x[n]=(\frac{1}{3})^n u[n]+(-\frac{1}{4})^n u[n]$$

ii) Give the pole-zero plot of the z-transform, including its region of convergence (ROC) (2 marks).

(6)

c. A discrete-time system has the following transfer function

$$\frac{Y(z)}{X(z)}=\frac{2z^3-z^2+z-0.4}{z^3}.$$

Determine the output y[n] of the system for the following input x[n]

$$x[n]=\delta[n]+\delta[n-1]+\delta[n-2]+\delta[n-3].$$

(5)

d. Consider a sequence $x_1[n]$ whose length is L points (nonzero for n=0, 1, …, L-1) and a sequence $x_2[n]$ whose length is P (nonzero for n=0, 1, …, P-1). A linear convolution of these two sequences will generate a third sequence $x_3[n]$. Describe the process involved in calculating this linear convolution using DFT.

(5)

A3. **a.** Calculate the Discrete Fourier Transform (DFT) of the discrete series x[n]={1, 2, 2, 1}.

(4)

b. i) State the Nyquist sampling theorem and determine the minimum sampling frequency f_s required for sampling the following continuous-time signal x(t) (4 marks):

$$x(t)=\sin(10\pi t)+\cos(50\pi t)$$

ii) Suppose the discrete-time signal after sampling the above x(t) by the minimum sampling frequency is denoted by x(n). Draw the block diagram of an ideal system for recovering the original continuous-time signal and give details about the input-output relationship at each stage of the block diagram (4 marks).

(8)

c. An anti-aliasing filter is to be designed for a data acquisition system and the first order lowpass filter given in the following equation is used as a prototype, where ω_b=40 rad/sec is the filter cutoff frequency.

$$H(s) = \frac{\omega_b}{s + \omega_b}$$

i. Design the digital filter using the Impulse Invariant method if the filter is implemented at a sampling frequency of 40 Hz (4 marks).

ii. Given the same sampling frequency of 40 Hz, design the digital filter using the Bilinear Transform method (4 marks)

(8)

A4. **a.** Given the spectral coefficients of a filter, *H(k)*, which are symmetrical about *k*=0, the original impulse response *h*[n] can be reconstituted using the following equation, where *N* is the total number of coefficients:

$$h[n] = \frac{1}{N}\sum_{k=-(N-1)/2}^{(N-1)/2} H(k)e^{j2\pi nk/N} = \frac{1}{N}\left(H(0) + 2\sum_{k=1}^{(N-1)/2} H(k)\cos(2\pi nk/N)\right)$$

From this you are going to design a **highpass** FIR filter with *N=5* coefficients with a passband range between *0.5*kHz and 1kHz at a sampling frequency f_s=*2*kHz.

i) Use the frequency sampling method to calculate the FIR filter coefficients (6 marks).

ii) Sketch the structure of the filter using unit-delay elements (1 mark).

iii) Derive the difference equation of the filter (1 mark).

(8)

b. Consider a first-order system function of the form

$$H(z) = (1 - re^{j\theta}z^{-1})\ (r<1,\ 0<\theta<\pi/2)$$

i) Give its pole-zero plot and indicate the corresponding pole vector and zero vector (3 marks).

ii) Derive the magnitude response and phase response of the system function in frequency domain in terms of the pole vector and zero vector (4 marks).

(7)

c. Suppose $X_1(z)$ is the z-transform of the sequence $x_1[n]$ and $X_2(z)$ is the z-transform of the sequence $x_2[n]$. Then we have the following property:

$$x_1[n] * x_2[n] \xleftrightarrow{z-transform} X_1(z)X_2(z)$$

where * denote the convolution operation. Derive the above result.

(5)

Part B

B1. a. **i)** Describe the format of a floating point number. **(4)**

ii) Outline the process whereby two binary floating point numbers are added together. **(4)**

b. The Booth algorithm can be used to multiply two integers by encoding the multiplier as follows:

00 : middle of a run of 0s, do nothing

10 : beginning of a run of 1s, subtract multiplicand

11 : middle of a run of 1s, do nothing

01 : end of a run of 1s, add multiplicand

Show how the Booth algorithm can be used to multiply the positive binary integers 011101 (multiplicand) and 01110 (multiplier). **(8)**

c. Compare the efficiency of Booth encoded multiplication with a traditional shift and add technique. How could the efficiency of Booth encoding be improved upon? **(4)**

B2. **a.** Describe the basic interrupt mechanism and explain why this is a better way of handling external events than continually polling some external status flag. **(6)**

b. What do you understand by *interrupt latency*? Give an example of an application where interrupt latency may be a critical factor. **(3)**

c. Why do some people regard interrupts as inherently unsafe? **(3)**

d. Considering the architecture of a Reduced Instruction Set Computer (RISC)

i) Why do RISC machines contain a large number of registers? **(3)**

ii) What is the principal advantage gained by reducing the number of instructions available in a RISC machine? **(2)**

iii) What is the fundamental limit on the internal clock speed of a central processing unit (CPU)? **(1)**

iv) Explain how a RISC architecture may improve this limit. **(2)**

B3. **a.** The *Harvard architecture* is frequently used in digital signal processing. Explain why this has advantages over the conventional *von Neumann* architecture for digital signal processing. In particular, what is the *von Neumann bottleneck*? **(6)**

b. Calculate $1110_2 \div 101_2$ (decimal 14 divided by 5) by non-restoring division. The data values must all be held in byte wide storage locations. Show each step of the calculation in binary. You must start the process by left shifting the divisor by three places (multiplication by 2^3) in order to demonstrate a process whereby any four bit positive integer could be divided by any three bit positive integer. **(6)**

c. A digital system is required which can produce a sine wave with a frequency of 50KHz. Draw a block diagram to show how this can be achieved using a Read Only Memory (ROM) based look-up table. The ROM is 1K x 8 and contains 1024 data samples for one complete cycle of a sine wave. Explain how your circuit gives the desired frequency.

Could the size of the ROM be reduced? If so, explain how this could be achieved. **(8)**

B4. a. Explain the difference between the following terms in the Verilog Hardware Description Language (HDL).

i) The types **wire** and **reg**. **(2)**

ii) An **initial** procedure and an **always** procedure. **(2)**

iii) A blocking assignment (=) and a nonblocking assignment (<=). **(2)**

b. Draw the circuit that will result from synthesis of the following Verilog code:

```
module pipeline (output reg [7:0] C_out, input [7:0] A_in, input clk);
  reg [7:0] A_out, B_out;
  always@( posedge clk )
  begin
    A_out = A_in;
    B_out = A_out;
    C_out = B_out;
  end
endmodule
```

How would you alter this code in order to produce three pipelined registers after synthesis? What is the advantage of using a pipeline in digital design? **(4)**

c. Develop an Algorithmic State Machine and Datapath (ASMD) chart for a shift-and-add multiplier. It should examine the least-significant bit of the multiplier (MR), add the multiplicand (MD) to the partial product (PP) if the bit is a 1, and then shift the partial product and the multiplier one bit position to the right. Draw the ASMD chart and explain what each of your states represents and the operations required in the datapath. **(10)**

NJP WL/JR