EEE225 Problem Sheet 2 - NJP

1. What is the cause of leakage current in CMOS semiconductor devices? Why is this becoming more of a problem as the technology advances?

2. Calculate the noise margins for the 5V CMOS family given on your data sheet when the output current is 20µA.

3. Draw and label (gate, drain, source) the transistor level circuit for a CMOS inverter with a 5V supply. The transistors have the following parameters:
   PMOS 'on' R_{DS} = 75 Ω , 'off' R_{DS} = 500,000 Ω
   NMOS 'on' R_{DS} = 25 Ω , 'off' R_{DS} = 500,000 Ω
   Calculate the 'no load' output voltage and static power dissipation for:
   (i) input = 0V
   (ii) input = 5V.

4. Why is the 'on' resistance of the nmos transistor lower than that of the pmos transistor in Question 3?

5. What is a *universal* logic gate? (revision from EEE119)

6. Sketch the transistor configuration for a CMOS AND gate.

7. Draw the circuit described by the following Verilog code:

```
module tut_cct (F, A,B);
output F;
input A,B;
supply1 power;
supply0 ground;
pmos (F, power, A);
nmos (F, ground, B);
endmodule
```

A tristate buffer is required that will use tut_cct as its output stage. It will have an active high enable labelled EN and an input IN. Produce a truth table for the required logic to complete the tristate buffer and hence draw the required logic circuit using universal logic gates only.

8. A bit harder, you may need to refresh your Boolean algebra! Design a tristate buffer with an active low enable. Use the same output stage as in Question 7 and draw the circuit diagram using only universal logic gates. (Hint: you may find the simplification theorem, involution and De Morgan helpful!)