Data Provided: NONE

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2006-2007 (2 hours)

Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Describe the role of packaging applied to digital ICs, considering each of the four packaging principles. **(6)**

b. State the relative advantages and disadvantages of wire bonding and tape automated bonding. In what circumstances might one wish to retain a wire bonding capability? **(5)**

c. i. A digital IC has a size of 20x20 mm and contains 5M gates. Assuming Rent's rule applies, with the Rent exponent = 0.6 and the Rent pre-multiplier = 0.2, calculate the number of I/O terminals for the IC. **(2)**

ii. Assuming the terminals can be evenly spaced, calculate the average terminal spacing for mounting in a Dual-in-line (DIP) package. **(2)**

iii. Why might this spacing be practically difficult to achieve? **(2)**

d. What type of package is most suitable for high density Input/Output interconnections such as those discussed above? Describe its advantages. How are the interconnections achieved in this case? **(3)**

2. **a.** Describe the key challenges for the packaging of edge-emitting telecommunications lasers through consideration of the four principles of packaging.

Why is the packaging simpler for a vertical cavity surface emitting laser as opposed to the edge emitting case? **(4)**

b. Under operating conditions a laser chip, of dimensions 1x5 mm, dissipates 5 W and is indium mounted to a 3 mm thick silicon nitride tile, which is in turn indium mounted to a 10 mm thick aluminium heat sink. The temperature on the surface of the heat sink is measured as 25 °C. Assuming linear heat conduction, what is the temperature of the chip? Assume the indium mounting is uniform and has a coating thickness of 200 μm. Use the following thermal conductivity data: k_{indium} = 80 $Wm^{-1}K^{-1}$, k_{SiN} = 65 $Wm^{-1}K^{-1}$, $k_{aluminium}$ = 216 $Wm^{-1}K^{-1}$ **(5)**

c. Semiconductor lasers show an average failure rate as a function of time which is typical of semiconductor devices.

Draw a graph of the average failure rate versus time and describe its three main regions.

Describe how the process of 'burn in' could be applied to these devices. What advantages might this have for the manufacturer? **(4)**

d. i. Describe what is meant by the 'accelerated testing' of semiconductor devices and why is it performed? Which stresses may we wish to accelerate? **(2)**

ii. The HAST test is a very common industry standard test. Briefly describe its procedure. What is it designed to reveal? **(2)**

iii. A company wishes to launch a new laser device which should achieve at least $1x10^5$ hours of reliable operation at 25 ^oC operating temperature. However only 5000 hours are available for testing before the project launch. Assuming the failure mechanisms are primarily thermally activated ones, with a rate of failure given by:

$$R = R_0 \exp(-E_a / k_B T)$$

where R is the rate, E_a the activation energy, k_B is Boltzmann's constant (1.38×10^{-23} m^2 kg s^{-2} K^{-1}) and T the temperature. At what temperature should the accelerated testing be performed?

Assume that E_a = 0.5 eV and electronic charge= 1.602×10^{-19} C. **(3)**

3. a. Describe the construction of a quad flat pack (QFP) surface mount package and its subsequent attachment to a printed circuit board using reflow soldering. **(6)**

b. How has the move to the use of lead-free solder affected the reflow soldering process? **(5)**

c. The junction to case thermal resistance (R_{jc}) of a 4x4 cm QFP package is 19 °C/W. If the package contains a silicon chip dissipating 5 W, what is the volume flow rate of the fan required to maintain the chip within safe operating conditions? Use the data in Figure 1 (overleaf) and detail the assumptions you have made. **(5)**

d. If the fan fails, what maximum power can safely be dissipated by the chip? How else might the package be cooled if a fan were not available? **(4)**

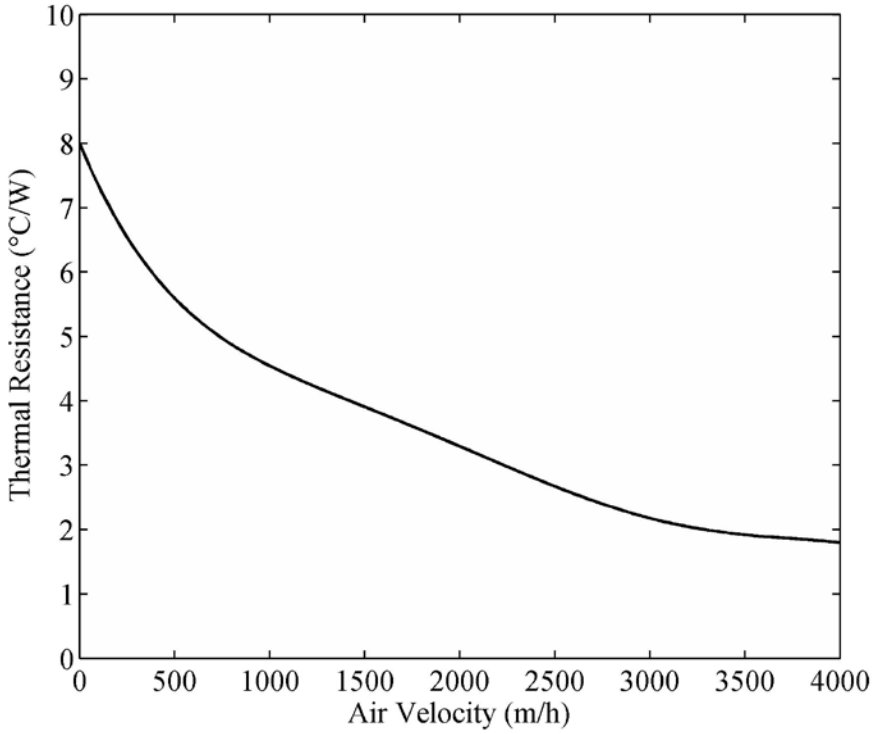

Figure 1 Thermal resistance of a heat sink – fan combination.

4. **a.** Describe the sequence of steps that are used to convert a schematic representation of a circuit into data for manufacturing a PCB board. **(6)**

b. The original version of an electronic system contains a number of devices in plated through hole (PTH) packages mounted on a two layer FR4 (epoxy/glass) printed circuit board.

Describe the enhancements that are made to this system when the PTH packaged chips are replaced by surface mount packaged devices and a six layer micro via PCB is used. Include a discussion of the measures that can be taken to ensure impendence matching between high speed devices and the PCB tracks. **(6)**

c. What width tracks should be used to realise 50Ω impedance embedded microstrip on a typical micro via PCB? State your assumptions.

Note: $Z = \frac{87}{1.41 + \sqrt{\varepsilon_r}} \ln\left(\frac{6h}{0.8w + t}\right)$

where $\varepsilon_r = 4$, h = interlayer spacing, w = track width, t = track thickness **(4)**

d. Describe how crosstalk might arise between signals in parallel tracks on this PCB. What measures can be taken to reduce the crosstalk? **(4)**

GLW-MH / NLS