The University Of Sheffield.

Data Provided:

Boltzmann constant $k_B = 1.38 \times 10^{-23}$ J K^{-1}

Electron charge $e = 1.6 \times 10^{-19}$ C

Thermal conductivity data:

$k_{silicon}$ = 120 W m^{-1} K^{-1} k_{copper} = 390 W m^{-1} K^{-1}

$k_{alumina}$ = 25 W m^{-1} K^{-1} k_{solder} = 60 W m^{-1} K^{-1}

$k_{diamond}$ = 2000 W m^{-1} K^{-1} $k_{aluminium}$ = 200 W m^{-1} K^{-1} k_{gold} = 300 W m^{-1} K^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (2.0 hours)

EEE6393 Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Draw a graph of the average failure rate versus time for an electronic component. Explain the reasons for the shape of the curve by identifying and describing its main regions. **(3)**

b. Describe the process of 'burn-in' and what advantages this might have for an integrated circuit (IC) manufacturer. **(4)**

c. A power IC fabrication process produces 360 dies per wafer. The process gives 250 random defects per wafer that obeys a Poisson distribution. Assuming that a single defect would destroy a die, calculate the function yield of the process. The Poisson distribution can be described thus: $P(x) = (e^{-\lambda}\lambda^{x})/x!$ **(3)**

d. Each power IC in **1.c.** consists of a number of separate modules. Suppose that the IC can be redesigned to include a number of spare extra modules that can be configured after fabrication to replace any modules found to be faulty. Assuming one extra module is needed to replace exactly one defective module, how many extra modules are required by each IC to insure a yield greater than 95 %? **(5)**

e. A power diode product for an automotive application needs to achieve a 15 year lifetime at an operating temperature of 90 °C. From prior experience it is known that the primary failure mechanism is a thermally activated process with an activation energy of 0.75 eV. A total of 1000 hours are available to perform an accelerated lifetime test on the product. What is the minimum temperature at which the test should be performed? **(5)**

2. **a.** A digital watch contains a single integrated circuit (IC). The IC is glued directly to a printed circuit board (PCB); wire bonds are then made to pads on the PCB and then the IC and bond wires are encapsulated with 'glob top' epoxy resin. Discuss the advantages and disadvantages of this 'chip-on-board' assembly method in comparison to packaging the IC within a surface mount package. **(5)**

b. A microprocessor with 1 million gates is flip-chip bonded onto a substrate with two routing layers. The flip chip connections are made using 100 μm diameter solder balls on a square pitch of 0.8 mm. All of the inputs and outputs need to be routed to the edge of the substrate. What is the maximum allowable pitch of the routing on the substrate in line with the edge of the chip? You may assume a Rent exponent $\alpha = 0.45$ and a Rent coefficient $\beta = 0.8$. **(5)**

c. For a ball grid array connection, explain the sequence of materials that exist between the aluminium IC bond pad and the copper PCB trace. **(5)**

d. The eutectic tin-silver-copper alloy contains 3.7 mass% silver and 0.8 mass% copper. In comparison, a commonly-used solder ('SAC305') contains 3.0 mass% silver and 0.5 mass% copper. Compare and contrast the use of these two alloys within a surface mount assembly process. **(5)**

3. **a.** The integrated circuits (ICs) on a 10×10 cm printed circuit board (PCB) dissipate a total of 6 W. The PCB has sufficient copper routing and thermal vias to assume that in operation the entire PCB becomes isothermal. What is the temperature of the PCB when the PCB is horizontal? Make use of the data below and state any assumptions that you have made.

Natural convection heat transfer coefficients for 10×10 cm horizontal plane:
Top surface: $h_{top} = 6$ W m^{-2} K^{-1} Bottom surface: $h_{bottom} = 3$ W m^{-2} K^{-1} **(5)**

b. Suggest ways in which the temperature of the PCB described in **3.a.** could be reduced *without* reducing the power. **(4)**

c. Starting from an FR4 laminate, explain the fabrication of a two layer PCB. Include a description of the steps involved in making electrical vias.

How could the generation of waste copper solution be minimised? **(4)**

d. The connections between the bond pads of a high speed IC and the legs of its quad flat pack (QFP) package have the following electrical characteristics:
L = 4 nH; C = 0.6 pF; R = 5 mΩ.

Suggest suitable dimensions for the microstrip lines on the PCB to which it is soldered. You may assume the following relationship for a microstrip line:

$$Z_0 = \frac{87}{1.41 + \sqrt{\varepsilon_{eff}}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

- where *h*, *w* and *t* are the height, width and thickness of the track and the other symbols have their usual meanings.

Why is a QFP package preferable to a dual in-line (DIP) package for this IC? **(5)**

e. Explain the positioning and purpose of the decoupling capacitors that often surround a high speed IC. **(2)**

4. **a.** The 'efficiency' of an integrated circuit (IC) packaging technology is a complex function of many parameters including the following: electrical performance; thermal performance; reliability; cost; size. For a complex, high-speed IC design, place the following five packaging technologies in order of increasing efficiency: through-hole package; system-in-package; flip-chip; surface-mount package and system-on-chip. **(2)**

b. The current design for a CMOS image sensor IC in a mobile phone consists of a rectangular array of picture elements – 'pixels'. Each pixel comprises a photodiode plus associated circuitry to generate a digital signal. The digital signals leave the image sensor IC via four levels of metallisation. Explain, with the aid of sketches, how through silicon vias (TSVs) could be used to improve the light gathering capability of the sensor. Include a discussion of the necessary TSV fabrication steps in your answer. **(8)**

c. The continued miniaturisation of microsystems is leading to the development of 'interposers', which act as very high pitch circuit boards. Most interposers are made from silicon, but there is also interest in manufacturing them from silicate glass. Compare and contrast the use of these two materials for this application. **(2)**

d. A 10×10×1 mm insulated gate bipolar transistor (IGBT) module dissipates 200 W and is packaged on a direct-bond copper (DBC) substrate, as shown schematically in Figure 4 (below). The bottom copper surface is in contact with a water cooling channel, which is maintained at room temperature. What is the temperature of the top surface of the silicon IGBT? Please show your working and indicate what assumptions you have made. Thermal conductivity data is provided at the front of the exam paper.

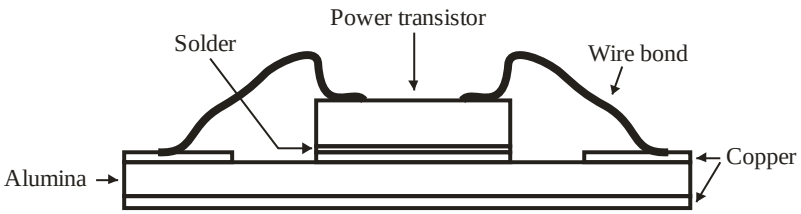

Figure 4 **(6)**

e. If the junction to case thermal resistance of the package in **4.d.** is reduced to R_{jc} = 0.1 °C/W by replacing the alumina with diamond, would it be possible to use air-cooling instead of water-cooling? Assume a heatsink / fan combination with a case to ambient thermal resistance R_{ca} = 1 °C/W is available. Explain your answer. **(2)**

GLW / MRS