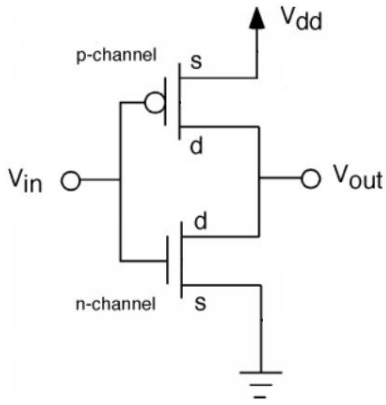
EEE225 Solution Sheet 2 - NJP

1. In modern CMOS technologies (65nm and below), gate leakage currents are the dominant source of leakage (> 90%). This occurs due to tunnelling through the thin gate oxide. Scaling of the technology results in thinner gate oxides further increasing the leakage due to tunnelling.

2. Noise Margin (High) 4.4 – 3.15 = 1.25 V , Noise Margin (Low) 1.35 – 0.1 = 1.25 V.

3. Hint: Draw the equivalent circuit with resistors, use V^2/R for power.



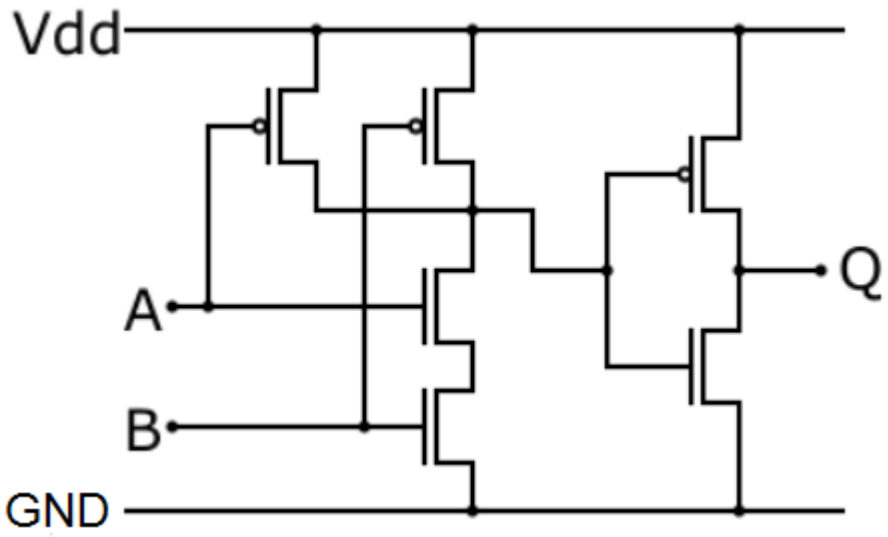
(i) V_{out} = 4.999V P_{diss} = 0.05mW

(ii) V_{out} = 0.00025V P_{diss} = 0.05mW

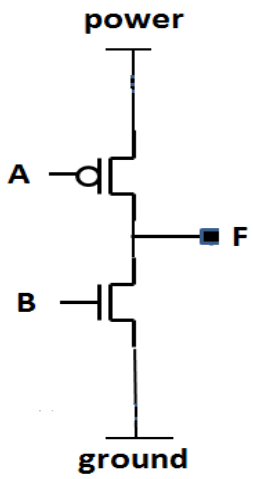
4. nmos: electrons majority carrier, pmos: holes majority carrier. Electrons have a higher mobility than holes, hence nmos has lower 'on' resistance.

5. Universal logic gates are NAND & NOR as they can be used to implement any Boolean logic function.

6.



7.



EN	IN	A	B
0	0	1	0
0	1	1	0
1	0	1	1
1	1	0	0

Remember, you want a buffer, not an inverter.

$A = \overline{EN \cdot IN}$ $B = EN \cdot \overline{IN} = \overline{\overline{EN} + IN}$ (use involution and De Morgan, circuit diagram is in your notes)

8.

EN	IN	A	B
0	0	1	1
0	1	0	0
1	0	1	0
1	1	1	0

$B = \overline{EN + IN}$

$A = \overline{EN} \cdot \overline{IN} + EN \cdot \overline{IN} + EN \cdot IN = \overline{EN} \cdot \overline{IN} + EN = EN + \overline{IN}$

$= EN + \overline{\overline{IN}}$

9.

$= EN \cdot IN$

Hence, logic diagram.

Simplification Theorem : $X + \overline{X}.Y = X + Y$ (I would not expect you to remember this theorem)