Examination Feedback for EEE6040 – Advanced Solid State Devices
Spring Semester 2010-11

Feedback for EEE6040 Session: 2010-2011

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

The paper resulted in a spread of marks from average to exceptional performance. There were however one or two fails
The majority of students went for questions 1, 3 and 4 and avoided question 2. However the ones that did that question generally did very well. Overall the students did very well on the basic description of the devices and on the calculations and showed a good understanding of some of the advanced concepts.

Question 1:

The majority of the students drew the characteristics well, though many forgot about the breakdown. Some gave good description of the various mechanisms, whilst others struggled a little. Most did the calculation well, though quite a few made silly mistakes. The description of the HEMT was generally good, but not all could describe all the device advantages. For the gm and ft calculation, most got the gm part well enough, although one or two took the wrong Vsat (should have been for GaAs). For the ft, I had wanted to use the mobility model rather than Vsat (since Vssat does not apply so well to the HEMT). If were to do this again would have made this clearer. However most used the Vsat model and I accepted this answer.

Question 2:

Many students avoided this question, despite the fact that it was probably less work than some of the others. Most who did it did well, although one or two made silly mistakes with the answer. For 2b, again this was done very well, although many students did not take the answer to the very end. I think only one completed it to the final answer of 54 electrons commented that it 'seems too low' but in fact that's what it is these days!

Question 3:

Most students did the diagrams very well, including both the MOSFET schematics and the band diagrams, although some were a little sloppy with the latter and often the two cases looked very similar. For the 'high-k' dielectric calculation, most did this fine, but a few got the units wrong (should be 2 and 4 NANOMETERS (nm). The electron affinity determined the barrier height and one needs this to be high, which rules out oxide B (there would be no effective barrier to the Si). Many did in fact suggest the use of oxide A which is the correct choice, but only a few gave the right reason .

Question 4:

Most students were able to list the delay components well and to make a good equivalent circuit diagram., although there were a few who messed this up. A few started to put some additional irrelevant points into this; I am not sure why. Most gave good answers as to what to do to improve the performance, although a few were tempted to put additional things into here without justification (should have just stuck to the facts). The HBT was explained well enough, although a few did not give all the advantages. Some were confused with the HEMT. Finally for the discussion of CMOS scaling factors most students gave a very good response. However some important facts were missing and for some students there was a tendency to write unrelated facts just to fill in more words. It also looks like some students suffered with time constraints since in many cases this was the last part in their scripts.