Examination Feedback for EEE6042 – Integrated Circuit Technology
Autumn Semester 2013-14

Feedback for EEE6042 Session: 2013-2014

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

Students have fared as expected- a Gaussian spread of marks. There has been a significantly poor response to Q1 which covers the basics of materials this year. Questions 2 and 3 were relatively well answered.

Question 1:

There were a couple of "new" questions relating to wurtzite structure and defect concentrations in solar cell manufacture, which seem to have been a cause of difficulty. Relatively fewer students attempted this question (12/29).

Question 2:

Received a good response, most students were able to recall the crystal growth techniques, as well as detailed descriptions of CVD and MOCVD. I was impressed that almost all students got the problem correct.

Question 3:

Also received a very good response, the question on wet and dry oxidation was answered correctly, as indeed the CMOS process flow and the liftoff technique.

Question 4:

The average for this question was rather low, although it was attempted by most in the class. Several candidates gave very poor response to the general question about replacement materials for silicon in future microelectronics. The problem was solved by all. The question on gettering was answered by some.