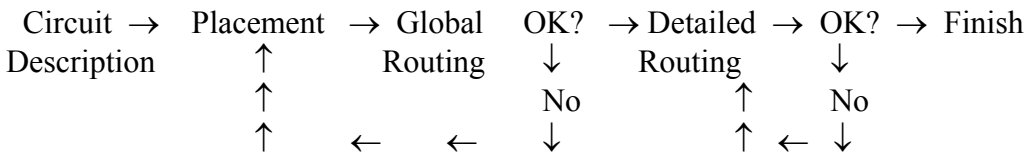
Intro to VLSI Design Jan 1999
Model Answers

1. (a) This is standard bookwork



Students need to discuss the place and route strategy, explaining that during placement we seek to put components that are heavily connected together explaining why this is important. They then need to explain (with reasons) that routing seeks to keep the interconnection length to a minimum. They also need to explain that the total silicon area needs to be minimised.

(b) This section requires the simple application of bookwork. Students should find this straightforward provided they understand the algorithms.

(i) A brief explanation of the algorithm is required noting that the interconnections act as springs controlling attractive forces between the modules. In this example the net force will be dominated by the 4 long connections to the modules below A. Thus the net force (and motion) will be downwards.

(ii) Similar details for this algorithm are required, but in this case the min-cut algorithm only looks at which side of the cut the module should reside on. In this case moving A across the cut reduces the total number of connections crossing the cut, so this motion is desirable. After the action A is therefore moved leftwards.

(iii) In min-cut it is usual only to consider modules on the side of the cut which has the larger silicon area. This prevents all the modules piling up on one side of the cut. In this example A is clearly on the with less modules, so it would not be chosen.

2.This is a standard derivation. All diligent students should be able to get this right. The switching speed is essentially the time that it takes for the load capacitance to charge or discharge through the transistors. In a separate calculation (which the students can assume) the students have seen that the switching time for an inverter t=3CR where R is an effective resistance of the transistor. For a NAND gate the n transistors are in series so that the fall time is equal to m3CR. The p-transistors are in parallel, then we should consider the worst case where the rise time is still 3CR. So the average switching time will be $T_{ave} = 3\frac{(m+1)CR}{2} = \frac{3(m+1)\left(mC_1 + C_2\right)R}{2}$

To remove the R term we calculate this relative to an inverter giving

$$\frac{T_{ave}(m)}{T_{ave}(1)} = \frac{(m+1)}{2}\frac{\left(mC_1 + C_2\right)}{\left(C_1 + C_2\right)}$$

The dynamic power dissipation is that used in charging and discharging the capacitor. For one such process the energy is $C_L V_{dd}^2 / 2$ .In one cycle the energy used is twice this. Thus with a clock cycle of frequency f, the dissipation is $C_L V_{dd}^2 f$.

In a large scale integrated circuit the routing capacitance (which does not depend on the complexity of the gates) can dominate.

The next section requires students to show that they have an understanding of these equations and can use them.

Putting numbers into the equations we can show the relative speeds of NAND with different values of m are.

M	T
1	1
2	2
3	3.3
4	5
8	15

For the circuits we need to identify the slowest branch. For (a) T=15, (b)T=5+2+1=8, for (c) the slowest branch is the bottom one where T=5+1+3.3=9.3

For power dissipation P is proportional to C_L i.e. (m+2) . We need to add up the total power for all the logic gates in each design.
(a)P proportional to 10
(b) 6+3+6+3+4=22
(c) 4+4+3+3+6+3+5=28

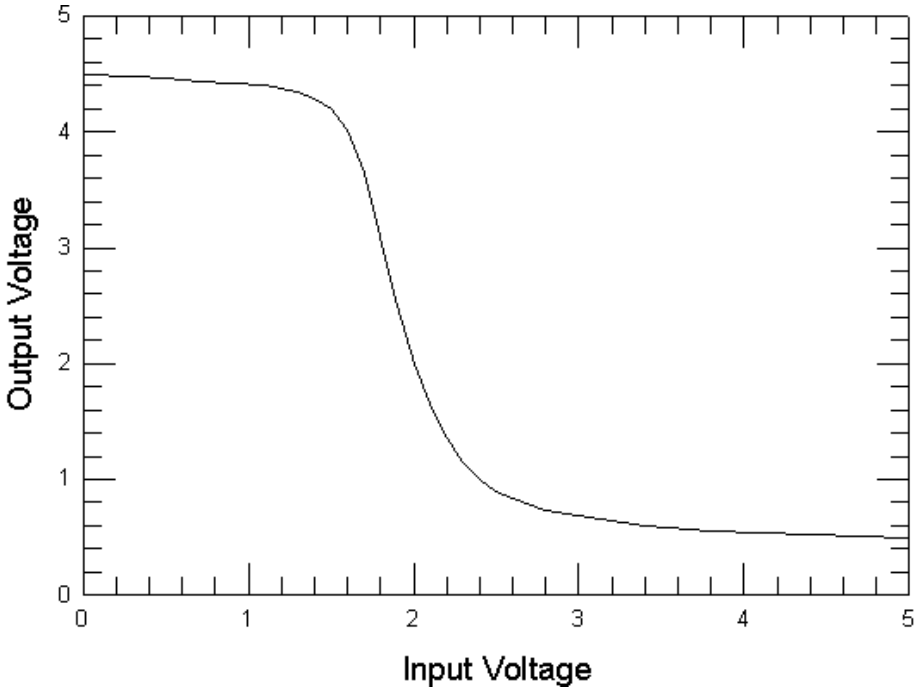
3. (a) This is bookwork. For good marks students should discuss stuck-at faults and the single fault assumption. They should explain that there is little physical justification for the stuck at fault, but this is necessary to facilitate fault simulation. The effect of the single fault assumption on the number of fault states that need to be simulated must be discussed together with the dangers of fault passes associated with this assumption.
(b) This section is to test whether students really understood the ideas above. For those students that understand this is completely trivial. The new types of fault make no difference to the number of fault states. The answer is 2Q+1.
(c) The critical part of this question is that students should understand that they must use the path-sensitisation technique. Then the argument is fairly straightforward. To test J stuck-at 0 we need inputs that attempt to force it to 1. Thus D and E must be 1. To sensitise to L we need K=0, so F=0. To then sensitise to M , D must be 1 which is consistent. Then to sensitise to the output P we need G=0. So the test is DEFG=1100 and P should be 0 if the circuit is fault free. The other inputs have no effect.

4. (a) Bookwork. The noise margin describes the amount the input voltage can vary from the nominal values before there is any significant deviation in the output voltage. There are two noise margins: 1 each for the high and low nominal values. To do this first we need to determine the nominal values, which can be determined directly from the transfer characteristics. The point at which the output value starts

to deviate significantly can be defined in two ways: either as the point at which the output value varies by 10% of the logic swing or as the point at which the gradient of the transfer curve is 1.

The noise margins are important since they describe the robustness of the design to voltage variations.

(b) This is application of the bookwork described in part (a).
The transfer curve specified looks like:



To determine the noise margins first we need to find the operating points. These are the points at which the reflection of the transfer curve will intersect with the original. We can find this by inspection form the table. The operating points will be 0.51 and 4.45V. Thus the logic swing is 3.94V. 10% of this is 0.4V. We now need to find the input voltages at which the output voltages are 4.45-0.4 and 0.51+0.4. By inspection of the table we see that these voltages are 1.55V and 2.49V. The noise margins are the separation of these input voltages from the nominal operating voltages. So the low noise margin is 1.55-0.51 =1.04V. The high noise margin is 4.45-2.49 =1.96V.
Some students may use the criteria that the slope of the transfer curve is 1. They will then get slightly different values of noise margin, but provided these are applied consistently they will still get full marks.

(c) This requires the application of a derivation in the course. It is not strictly necessary for students to carry out the derivation, but most will need to do so to get the necessary equation.
We define Vinv as the input voltage where Vin=Vout

In this case this is 2V from the table.

At this voltage both the transistors are in the saturation mode so $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$ for each of the transistors. The current in the two transistors must be the same so we can substitute appropriate values in and equate these. We then get

$$\frac{\beta_p}{\beta_n} = \left(\frac{V_{inv} - V_{tn}}{V_{inv} - V_{dd} - V_{tp}} \right)^2$$

again substituting in the values $= \left(\frac{2-1}{2-5+1} \right)^2 = 1/4$

Now $\beta \propto \mu \frac{W}{L}$ but the mobility for the n-channel device is twice that of the p-channel. So

$$\frac{\beta_p}{\beta_n} = \frac{\mu_p \left(\frac{W}{L} \right)_p}{\mu_n \left(\frac{W}{L} \right)_n} = \frac{\left(\frac{W}{L} \right)_p}{2\left(\frac{W}{L} \right)_n} = \frac{1}{4}$$

$$\therefore \frac{\left(\frac{W}{L} \right)_p}{\left(\frac{W}{L} \right)_n} = \frac{1}{2}$$