EEE225: Analogue and Digital Electronics

Lecture XII

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This Lecture

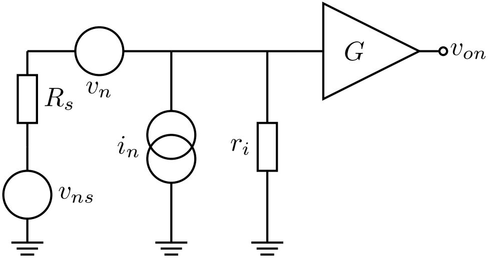
Equivalent Noise Generators

Representing noise using two or three noise sources is very attractive.

- It is a simple representation of the noise elements of large/complex circuits/systems.
- It is 'standard' – we can compare two systems performance by comparing their input noise generators.
- It provides a standard approach (we make the same analytical steps to compute the noise irrespective of the individual circuit details).
- The parameters the model needs to represent a real system are (quite) easy to measure in the lab.

The Noise Equivalent Circuit

- The added noise, N_A is represented by two generators a series voltage generator, v_n, and a parallel current generator i_n.
- Two generators are required to make the model independent of source impedance.
- These represent the voltage noise that would be in series with real resistances in the system and current noise that would be in parallel with forward biased pn junctions.



v_{ns} – noise of R_s
v_n – amplifier input noise voltage
i_n – amplifier input noise current
r_i – input resistance of the amplifier (noiseless)
G – is the gain of the amplifier.

- The equivalent noise generators can be found for a real system by selecting values of R_s and measuring the output noise.
- A true RMS voltmeter is needed with a known bandwidth Δf.
- To obtain v_n set $R_s = 0$. It can be shown using standard circuit analysis that if $R_s = 0$, i_n has no effect and $v_{on} = \sqrt{G^2 \overline{v_n^2} \Delta f}$.
- Having obtained v_n any value of $R_s > 0$ can be used to find i_n as everything else is already known. With finite R_s:

$$\overline{v_{on}^2} = G^2 \left[\overline{v_n^2} \left(\frac{r_i}{R_s + r_i} \right)^2 + \overline{v_{ns}^2} \left(\frac{r_i}{R_s + r_i} \right)^2 + \overline{i_n^2} \left(\frac{r_i R_s}{R_s + r_i} \right)^2 \right] \Delta f \quad (1)$$

$$\overline{v_{on}^2} = G^2 \left(\frac{r_i}{R_s + r_i} \right)^2 \left[\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_n^2}\, R_s^2 \right] \Delta f \qquad (2)$$

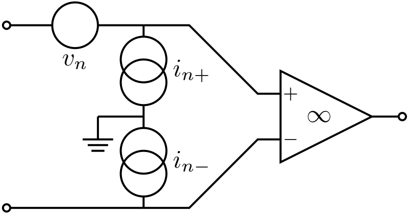
- Sometimes r_i is very large $10^{12}\ \Omega$ or so. In this case a finite R_s is necessary for i_n to flow through (and in so doing generate a noise voltage at the input w.r.t ground).
- This is often the case in FET input opamps. In a FET input opamp $\overline{i_n^2}$ is often very small say 0.01 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and $\overline{v_n^2}$ almost always dominates. Very small i_n^2 can often be neglected safely.
- If r_i is not very large say less than 10 MΩ, then R_s can be removed and (1) reduces to:

$$v_{on} = \sqrt{\left(G^2\, \overline{i_n^2}\, r_i^2\, \Delta f \right)} \qquad (3)$$

assuming v_n has already been dealt with.

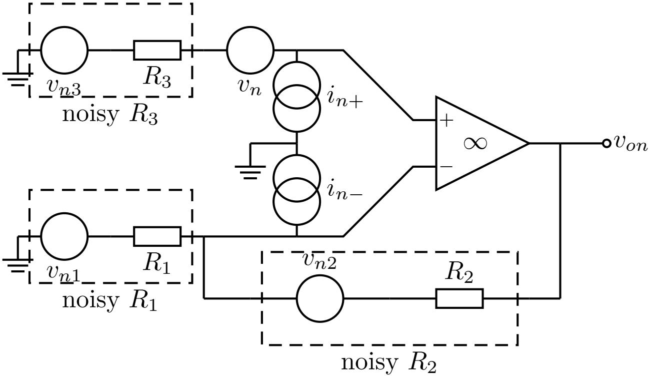
Noise in Operational Amplifiers

- Opamps can be quite complicated circuits. It's not practical to work out the noise of each resistor and transistor, and then combine them appropriately.
- SPICE does this, but having the numerical result doesn't tell the designer (you) what the dominant noise source is.
- Opamp noise is modelled in a similar way to the general unmatched amplifier.



The amplifier is ideal. v_n, i_{n+} and i_{n-} represent its noise. Other components are added around this model as if everything shown here is contained within the opamp.

A non-inverting *or* inverting amplifier with resistive feedback can be represented by



where the opamp and all resistors are replaced by their noise equivalent circuits.

- For an inverting amplifier the signal source is in series with R_1
- For a non-inverting amplifier the signal is in series with R_3

This leads to:

$$\overline{v_{on}^2} = G^2 \left[\overline{i_{n+}^2}\, R_3^2 + \overline{i_{n-}^2} \left(\frac{R_1\, R_2}{R_1 + R_2} \right)^2 + \overline{v_n^2} + \overline{v_{nf}^2} + \overline{v_{n3}^2} \right] \tag{4}$$

- G – closed loop gain $(R_1 + R_2)/R_1$.
- $\overline{v_{n3}^2}$ – noise due to R_3, $4\,k\,T\,R_3$ V^2/Hz.
- $\overline{v_{nf}^2}$ – noise due to the feedback resistors R_1 and R_2, $4\,k\,T\,R_1\,R_2/(R_1 + R_2)$ V^2/Hz.
- $\overline{v_n^2}$ – opamp noise voltage generator
- $\overline{i_{n+}^2}$ – opamp noise current generator at the non-inverting input
- $\overline{i_{n-}^2}$ – opamp noise current generator at the inverting input

It would be good if you could derive this... try superposition. G is sometimes called the “noise gain” because it affects all the terms in the square braces irrespective of inverting or non-inverting feedback configuration.

Conclusions from the Noise Model

Eq. 4 can tell us if we can improve our circuit noise given a certain opamp and closed loop gain requirement.

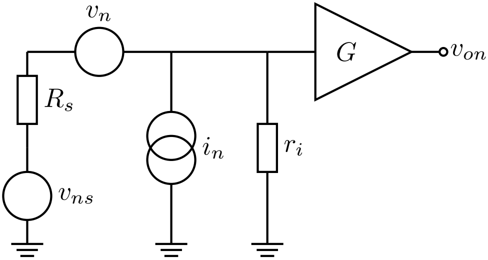
1. $i_{n+}^2\ R_3^2$ is due to the voltage across R_3 due to i_{n+}. If $R_3 = 0$ this noise goes away, but R_3 may be the source resistance or it may be there to reduce DC offset in the amplifier. If R_3 can not be reduced look for an opamp with low i_{n+}.
2. $\overline{i_{n-}^2}\left(\frac{R_1\,R_2}{R_1+R_2}\right)$ is the voltage appearing across the parallel combination of R_1 and R_2. R_1 and R_2 set the closed loop gain. Lowering both values – and keeping the ratio – is only possible to some extent. The opamp can not supply very large current and DC offset will be affected.
3. $\overline{v_n^2}$ is the opamp's noise voltage. It is irreducible – choose a different opamp.

4. $\overline{v_{nf}^2} = \frac{4\,k\,T\,R_1\,R_2}{R_1+R_2}$ – this represents the thermal noise of the feedback resistors. R_1 and R_2 are in parallel from the point of view of v_{n1} and v_{n2}. Reducing R_1 and R_2 – but keeping the ratio – is possible but has same problems as for point 2. If the gain is high $R_1 // R_2 \approx R_1$...
5. $\overline{v_{n3}^2}$ – this is the noise due to R_3. The same constraints apply as in point 1.

- A standard opamp may have $v_n = 20$ nV/$\sqrt{\mathrm{Hz}}$.
- At room temperature this is the same as the noise from about 24 $k\Omega$.
- If $R_1 // R_2$ and R_3 can be reduced below 24 kΩ points 4 and 5 (above) diminish
- FET input opamps have small current noise 0.01 pA/$\sqrt{\mathrm{Hz}}$ c.f. 0.4 pA/$\sqrt{\mathrm{Hz}}$ for a BJT. Choose a FET opamp to reduce points 1 and 2 (above).

A Simplified Opamp Noise Model

Assume that an opamp circuit has been designed so that: it's non-inverting. The thermal noise associated with R_1 and R_2 is no longer significant (points 2 and 4 above). r_i is the input resistance – noiseless because it's accounted for by v_n and i_n



$$\overline{v_{on}^2} = G^2 \left(\overline{v_n^2} \frac{r_i^2}{(r_i + R_s)^2} + \overline{v_{ns}^2} \frac{r_i^2}{(r_i + R_s)^2} + \overline{i_{ns}^2} \frac{r_i^2 R_s^2}{(r_i + R_s)^2} \right) \quad (5)$$

Example Simple Opamp Model Question

A particular amplifier has an input resistance of 100 kΩ, a voltage gain of 100 V/V and equivalent input noise voltage generator of 6 nV$\sqrt{\mathrm{Hz}}$ and 0.0075 pA$\sqrt{\mathrm{Hz}}$ respectively. The amplifier is fed by a noisy source resistance of 1 kΩ. What is the noise at the output?

$$v_{on}^2 = G^2 \frac{r_i^2}{(r_i + R_s)^2} \left(\overline{v_n^2} + \overline{v_{ns}^2} + \overline{i_{ns}^2} R_s^2 \right) \tag{6}$$

$$v_{on}^2 = 100^2 \frac{\left(100 \times 10^3\right)^2}{\left((100 \times 10^3) + (1 \times 10^3)\right)^2} \Big(\left(6 \times 10^{-9}\right)^2 + 4\,k\,T\,R_s + \left(0.0075 \times 10^{-12}\right)^2 \cdot \left(1 \times 10^3\right)^2 \Big) \tag{7}$$

Review

- Introduced the idea of equivalent noise generators
- Proposed a noise equivalent circuit consisting of two generators, making it independent of source impedance.
- Proposed a method to find the value of the noise generators for a real amplifier.
- Introduced a noise equivalent circuit for an opamp and added the noise sources of likely resistors.
- Developed an expression for the noise output in terms of the individual sources, and used this to investigate methods of minimising the noise output.
- Found a method to reconcile the simple noise equivalent circuit with the "full" opamp noise model provided some constraints are met.
- Did a quick example of a possible question using the simple model.

Thus ends this [course] on the minority field in the world of semiconductors. A field past glamour, often neglected, but undeniably essential. And a field of great satisfaction for those who know it.[1]

– Hans Camenzind

[1] His book can be downloaded free from www.designinganalogchips.com