



The  
University  
Of  
Sheffield.

### Data Provided:

Thermal conductivity ( $k$ ) data:

$$k_{\text{copper}} = 390 \text{ W / m } ^\circ\text{C}$$

$$k_{\text{silicon}} = 150 \text{ W / m } ^\circ\text{C}$$

$$k_{\text{solder}} = 50 \text{ W / m } ^\circ\text{C}$$

$$k_{\text{FR4}} = 0.2 \text{ W / m } ^\circ\text{C}$$

## DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-2015 (2.0 hours)

### EEE6214 Packaging and Reliability of Microsystems

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Discuss the factors that are causing the electronics industry to develop 3d packaging. (5)
- b. An integrated circuit (IC) dissipates 1 W and is attached using solder to the top copper layer of a printed circuit board (PCB). The PCB has four metal layers.  
  
What is the temperature difference ( $\Delta T$ ) between the bottom surface of the IC and the bottom surface of the PCB under the following conditions:  
 i) No vias between the metal layers.  
 ii) A 5×5 array of thermal vias underneath the IC.  
  
 Show your working. You should assume the following:  
 All of the heat generated in the IC is dissipated via the PCB.  
 The solder layer is 100  $\mu\text{m}$  thick.  
 Each metal layer of the PCB is 35  $\mu\text{m}$  thick copper.  
 Each dielectric layer of the PCB is 200  $\mu\text{m}$  thick FR4.  
 The IC has dimensions 10×10×0.5 mm.  
 Each thermal via has a cross-sectional area of 1 mm<sup>2</sup> and is solder-filled.  
 Thermal conductivity data is provided at the top of the exam paper. (8)
- c. What is the strategy that is used to minimise crosstalk when signals leave/arrive a PCB? (2)
- d. At which stage of the PCB design process should the connectors be considered? Explain your answer. (2)
- e. In comparison to an integrated circuit, what extra factors need to be considered when packaging a laser diode? Explain your answer and describe the practical methods by which the factors can be realised. (3)

2. a. Sketch the temperature profile experienced by an assembly passing through a set of reflow ovens when a solder paste made from eutectic tin-gold is being used. The melting point for this solder is 280 °C. (4)
- b. Suggest an enhancement to the reflow ovens in a. that would reduce the potential for oxidation of the PCB bond pads. (2)
- c. Show by a sketch how the reflow profiles for the process in 2.a. would be modified in the following circumstances:
- i) if the assembly included some components with a large thermal mass
  - ii) a non-eutectic tin-gold solder composition were used instead (2)
- d. What detrimental effect might occur if components of widely varying thermal mass are assembled in the same process?  
Suggest an alternative assembly method that could be used to avoid this detrimental effect. (3)
- e. The impedance  $Z_0$  of a microstrip transmission line on a four-layer copper/FR4 PCB is given by:

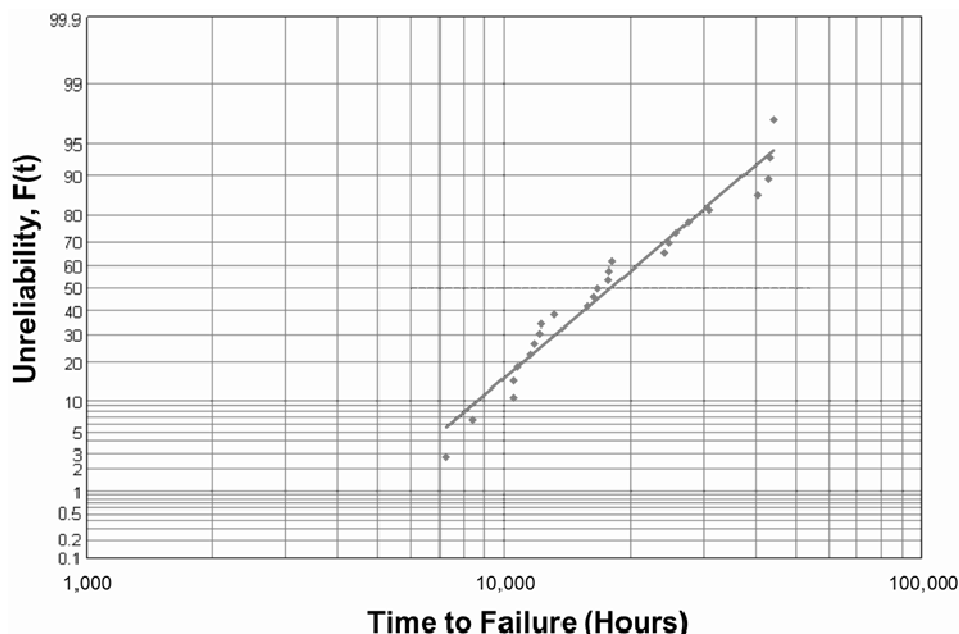
$$Z_0 = \frac{87}{1.41 + \sqrt{\epsilon_{eff}}} \ln \frac{5.98h}{0.8w + t}$$

where  $\epsilon_{eff} = 3.5$  effective permittivity;  $h$  = dielectric thickness = 127  $\mu\text{m}$ ;  $w$  = track width = 100  $\mu\text{m}$  and  $t$  = track thickness.

The transmission line is engineered to have  $Z_0 = 50 \Omega$ .

- i) Choose a suitable value for the track thickness  $t$  and then calculate the impedance  $Z_{90}$  at a sharp 90° bend in a track. (4)
- ii) What would be the impact of this change in  $Z_0$  for high speed signals? (3)
- iii) How could the change in impedance at the sharp bend be avoided and what would be the implications for the PCB design process? (2)

3. In order to investigate the reliability of your newly designed high-power laser diodes, you place a set of 25 laser diodes on accelerated life-test at 80°C. After a few weeks of operation the devices are all still working and you extrapolate the time to failure of each laser diode and construct a log-normal failure probability plot (Figure 1) to summarise your findings.



**Figure 1** Failure probability plot for batch of laser diodes at 80°C.

- a. Extract the shape parameter from Figure 1 and use it to suggest the probable cause of failures in these devices. (3)
- b. It is expected that your laser diodes could operate at 95°C for more than 12,000 hours. Using the life-test data in Figure Q3 and given MTTF of 32,000 at 60°C, answer the following questions. Show all your working.
  - i) Estimate the MTTF (time to 50% cumulative failures) at 80°C and use this to calculate the activation energy,  $E_a$ . (3)
  - ii) Use your calculated value for  $E_a$  to determine an estimate for the proportion of laser diodes that will still work after 12,000 hours operation at 95°C. Use  $k = 8.617 \times 10^{-5} \text{ eVK}^{-1}$  and assume a scaling factor,  $A = 1$ . (4)
- c. If it is determined that pn junction damage is responsible for the failure of your lasers,
  - i) Briefly outline the method of characterisation in the scanning electron microscope (SEM) that would be most appropriate in helping your investigation? (4)
  - ii) Would your choice of method change if the device under test can no longer be electrically biased? (2)
- d. Explain the process by which catastrophic optical mirror damage (COD) may occur in a laser diode, and why laser diodes manufactured in the GaAs/AlGaAs material system are more susceptible than those based on InP. (4)

4. a. The final stages in the fabrication of a copper/fiberglass printed circuit board (following the panel formation and lithography stages) involve applying various coatings to the board surfaces.

Explain the purposes of these coatings; suggest two material systems that are used and list their comparative advantages and disadvantages. (5)

- b. A fan is to be used in conjunction with a heat sink to cool an integrated circuit that dissipates 1 W. Under normal conditions (i.e. room temperature and pressure) the temperature of the surface of the heat sink is measured to be 50 °C.

Using the data given in Table 1 below, calculate the surface temperature of the heat sink if the same system were operating at an altitude of 6 km. You should assume that the convective heat transfer coefficient for the heat sink/fan combination,  $h$ , scales with the square root of the air density  $\rho$ . I.e.  $h \propto \rho^{0.5}$

Altitude (km)	Temperature (°C)	Density (kg/m <sup>3</sup> )
0	+ 20	1.35
6	- 18	0.66

**Table 1** Selected properties of the earth's atmosphere (7)

- c. Briefly describe the three methods that are used to make electrical connections to the bond pads of integrated circuits (ICs). (5)
- d. Which of the three methods in 4.c. is most appropriate for each of the following devices. Explain your answers.
- i) A high-power processor with 1000 I/Os.
  - ii) Low-volume production of an ASIC with 40 I/Os.
  - iii) High-volume production of a memory device with 100 I/Os. (3)

KG/GLW