The University Of Sheffield.

Data Provided:

Boltzmann constant (k_B) = $1.38 \times 10^{-23}\ m^2\ kg\ s^{-1}\ K^{-1}$
Electronic charge (e) = $1.602 \times 10^{-19}\ C$
Vacuum permeability (μ_0) = $4\pi \times 10^{-7}\ H\ m^{-1}$
Thermal conductivity (k): Alumina = 30 $W\ m^{-1}\ K^{-1}$, Aluminium = 216 $W\ m^{-1}\ K^{-1}$

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2011-12 (2.0 hours)

EEE6393 Microsystem Packaging

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Explain the origins of simultaneous switching noise and crosstalk. How do these two issues influence packaging design?

(4)

b. The mutual inductance (M) between two output terminals is given by:

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\left(\sqrt{1+\left(\frac{d}{l}\right)^2}\right)+\left(\frac{d}{l}\right)\right]$$

Where l is the conductor length and d the distance of separation between two adjacent conductors.

The properties of terminals on two types of package are given in Table 1. Calculate the mutual inductance between two adjacent output terminals for both types of package.

If the parasitic impedance was solely due to the mutual inductance and the terminal resistance as given in table 1, what is the maximum frequency which can be carried on these output terminals?

Type	Length *l*	Distance *d*	Resistance
Quad flat pack (QFP)	5 *mm*	0.7 *mm*	500 *mΩ*
Ball grid array (BGA)	2 *mm*	1.2 *mm*	200 *mΩ*

Table 1 Properties of the output terminals on two types of package

(8)

c. Describe, using drawings as necessary, a typical packaging scheme used for a fiber-coupled telecommunications laser.

In the final steps of packaging we need to align the output of the laser to the fiber. Describe how this process is normally accomplished. **(4)**

d. Describe what is meant by the 'accelerated testing' of semiconductor devices. Why is it performed? Which typical stresses may we wish to accelerate?

A laser device is observed to fail through a thermally-activated process. On test at 100 ^{o}C its lifetime is observed to be 900 hours. What is the expected lifetime under normal operating conditions, with the temperature at 25 ^{o}C? You may assume that the failure rate has an activation energy of 0.6 *eV*.

(4)

2. a. What is meant by the terms 'System on a Chip' (SoC) and 'System in a Package' (SiP)?

What are the relative advantages and disadvantages of the SoC approach compared to that of SiP or to just using individual integrated circuits on a printed circuit board (PCB)?

(5)

b. Table 2 lists some important parameters for two ICs, one (type A) produced 20 years ago and another (type B) which is available this year.

Processor	Year	IC area	Number of transistors	Clock speed	Power dissipation
A	1992	1 cm^2	3.1×10^6	60 MHz	8 W
B	2012	5 cm^2	2.2×10^9	3.4 GHz	130 W

Table 2: Comparison of two different types of Intel processor ICs

Over the last 20 years the power dissipation has increased because of the increased number of transistors and the increased clock speed. However, the increase is much less than expected. Why is the case?

For both ICs, apply Rent's rule to calculate the number of output terminals based on the number of gates. You may assume that 6 transistors are needed per gate, a Rent exponent of 0.4 and a Rent multiplier of 0.5.

From your results and the data above, suggest a type of packaging scheme for both types of IC, paying attention to cost and performance issues.

(5)

c. Both processor ICs from table 2 are glued with epoxy to a 5 *mm*-thick alumina substrate, which in turn is epoxy glued to a 10 *mm*-thick aluminium heat sink, as shown in Figure 1. Assume that each layer of epoxy is 100μm thick, with a

thermal conductivity of 0.5 $Wm^{-1}K^{-1}$. You may also assume that the IC and heat sink are in thermal equilibrium.

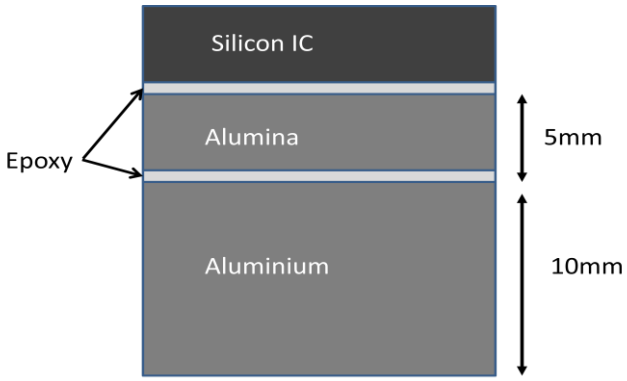

Figure 1: Heatsink arrangement for the silicon processor ICs

If the maximum allowable temperature of the IC is 85 ^oC, what is the maximum temperature that we can allow at the bottom of the heat sink for both ICs? State whether this is reasonable or unreasonable for each IC.

If we replace the standard epoxy with a silver loaded epoxy of thermal conductivity 8 $Wm^{-1}K^{-1}$, what are the two new maximum heat sink values?

(7)

d. To maintain the heat sink temperature values calculated in c) we need to use forced air cooling. A fan blows ambient temperature air over the base of the heat sink. Using Newton's law of cooling, calculate the heat removed assuming a convective heat transfer coefficient of 2 $Wm^{-2}K^{-1}$.

To improve the effectiveness of the heat sink we must increase considerably the effective area. Discuss how we might achieve this.

(3)

3. Figure 2 and Table 3 contain data on a type of IC cooling module called the 'Cool Master'.

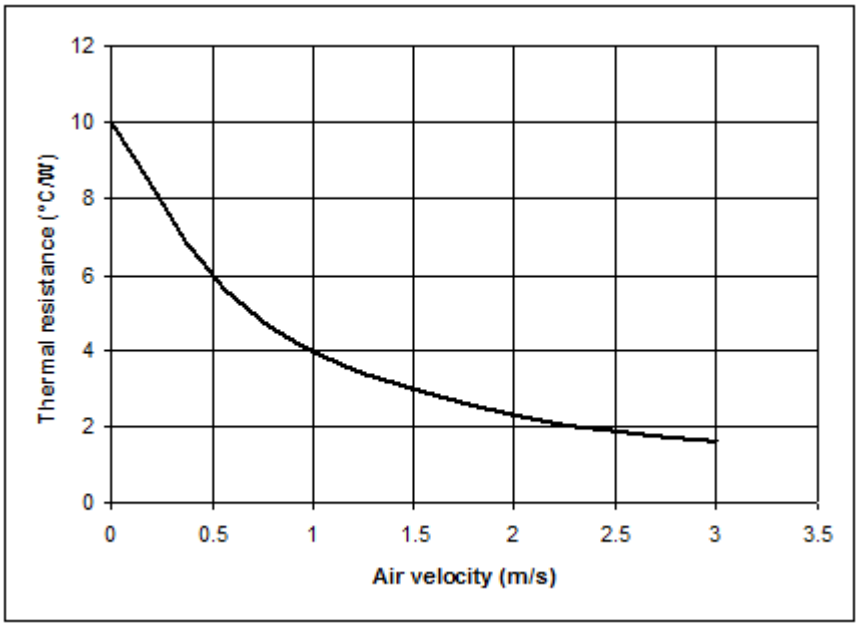

Figure 2 Thermal performance of 'Cool Master' module

'Cool Master' C14-J22C Microprocessor Cooling Module	
Application	Intel Pentium-4 3.6 *GHz* CPU
Socket Type	Intel Pentium-4 4 478-pin
Heat sink size	83 x 68.5 x 45 *mm*
Heat sink material	Aluminium with copper core
Fan size	70x70x15 *mm*
Fan speed	4300 *rpm*
Fan airflow	20 *CFM* *

Table 3 Further data on the 'Cool Master' module

(* 1 *CFM*=cubic feet per minute, 1 cubic foot = 0.0283 m^3)

a. From the information in Table 3 draw an annotated sketch of the Cool Master.

Why do you think that the Cool Master heat sink has a copper core? **(4)**

b. Using the data and graph above, calculate the thermal resistance of the Cool Master **(5)**

c. A Pentium-4 CPU attached to a Cool Master dissipates a maximum power of 25 *W*. What is the maximum thermal resistance of the Pentium-4 package R_{jc} that will keep the chip at a safe operating temperature? State any assumptions that you make. **(4)**

d. The data in Figure 2 is for operation at sea level. How would the performance of the Cool Master be affected if it was operated at high altitude? **(2)**

e. The Pentium-4 is connected via micro solder balls to a 4-layer signal redistribution PCB (printed circuit board).

Why does the PCB need four layers?

Describe the construction of the PCB. **(5)**

4. **a.** SAC305 is a common lead-free solder, with a melting point of 220 °*C*.

What is the composition of the solder?

When used for reflow soldering, what is the composition of the SAC305 solder *paste* and the purpose of each constituent?

The composition of SAC305 is very close to the eutectic composition. Why is this helpful to the surface mount assembly operator? **(6)**

b. Sketch the temperature profile of a PCB (printed circuit board) passing through a conveyor-belt reflow oven where SAC305 solder paste is being used. Annotate the different stages of the process. **(6)**

c. For high speed signals on a PCB, what track width w should be used for a microstrip transmission line, where the inter-layer spacing h = 200 μm? State the assumptions that you make.

Note, for a microstrip transmission line:

$$Z_0 = \frac{87}{1.41 + (\varepsilon_{eff})^{0.5}} ln\left(\frac{6h}{0.8w + t}\right)$$

where all dimensions are in metres and ε_{eff} = 4, t = thickness of conductor.

What is ε_{eff} and what factors govern its magnitude? **(4)**

d. What strategies can be employed in the layout of tracks on a high-speed PCB to minimise impedance mismatches and reflection losses? **(4)**

GLW / MH