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Semiconductor Materials

Lecture 22: transistors

Lecture 22: transistors

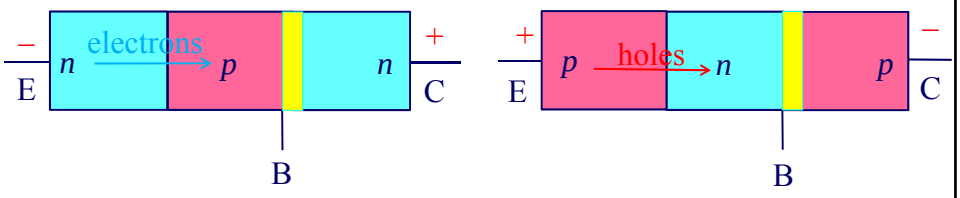
- principle of bipolar junction transistors (BJTs)
- transconductance
- transistor families
- BJT properties
- MOSFET design and properties
- multigate MOSFET devices

principle of bipolar junction transistor (BJT)

principle: connect 2 diodes with same doping back-to-back so you get a 3-terminal device and operate one diode (just) under forward bias (base-emitter, BE) and the other under reverse bias (base-collector, BC)

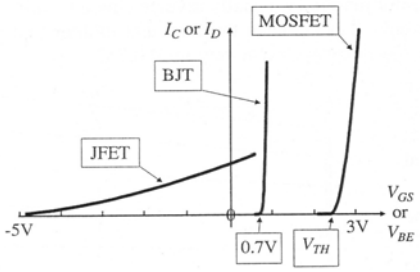
npn: V_{BE}~0.7V, V_{CB}>>1V

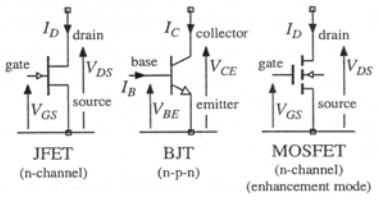
pnp: V_{BE}~−0.7V, V_{CB}<< −1V



general transistor behaviour

Transconductance is the relationship between input control voltage (V_{BE} for a BJT; V_{GS} for a FET) and output (controlled) current (I_C for BJT, I_D for FET). These curves are similar in shape for all transistor types, with a rapid current increase after some threshold is reached. The slope of these curves is called mutual conductance, g_m, or transconductance.





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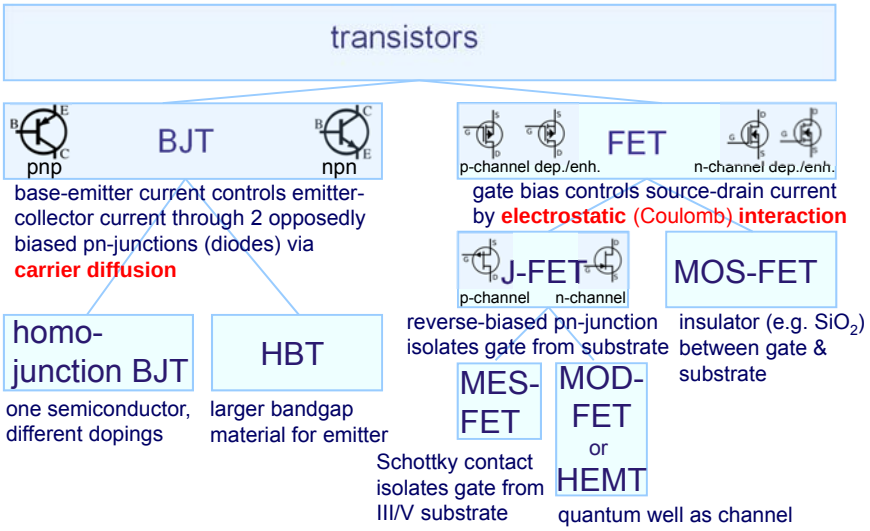
transistor families



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important BJT relationships

param.	relationship
β	small signal current gain for the current through r_{be}: $\beta = dI_c/dI_b$
g_m	transconductance, defined as

$$g_m = \left.\frac{dI_c}{dV_{be}}\right|_{V_{ce}=const}$$

From $I_C = I_{C0}\,[\exp(qV_{BE}/kT) - 1] \approx I_{C0}\,[\exp(qV_{BE}/kT)]$ we get in forward bias:

$$g_m = \frac{q}{kT} I_c \exp\left(\frac{qV_{be}}{kT}\right) \approx \frac{qI_{c0}}{kT}, \quad \text{if } h_{FE} >> 1$$

r_{be} small signal input impedance, defined as

$$r_{be} = \left.\frac{dV_{be}}{dI_b}\right|_{V_{ce}=const}$$

From $g_m = dI_c/dV_{be} = dI_c/dI_b \times dI_b/dV_{be} = \beta\, r_{be}^{-1}$ we directly get $r_{be} = \beta/g_m$

Note that in small signal terms, $r_{be} = v_{be}/i_b$, hence also $\beta i_b = g_m v_{be}$

This means the BJT can be considered as a current or as a voltage amplifier.

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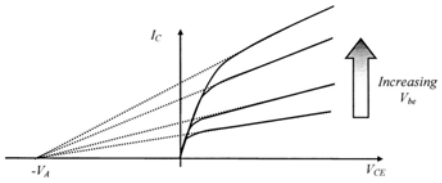
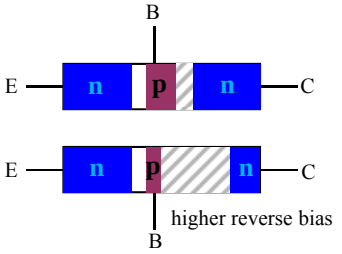
Early effect





The base-collector depletion region (hatched) increases with increasing base-collector voltage, V_{cb}. The **base width shrinks** correspondingly. Then more carriers (e^- in the case of an npn-BJT) transit the base because

1. the time for crossing the narrower base decreases and more charge carriers can transit the base without recombination, hence I_c increases.
2. the charge gradient across the base increases, hence also I_e increases.

The result of a larger net current gain α is a finite slope on the output characteristic, corresponding to a smaller output impedance, r_0. This is bad if one wants to construct a current source which ideally would have $r_0 \rightarrow \infty$ so that any voltage change across the BJT would not cause any change in the output current (all ideal curves would be horizontal). So, if the transistor has a high impedance load, such as a current source, then we need to **model the Early effect of reduced base width by including serial resistors r_{ce} (and sometimes also r_{cb}).**

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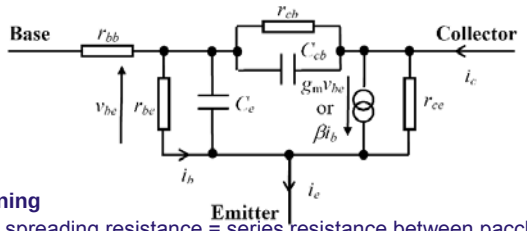
small signal circuit model of a BJT



symbol	meaning
r_{bb}	base spreading resistance = series resistance between packge wire and active part of semiconductor; can be ignored in many cases; typically $0.5\Omega < r_{bb} < 50\Omega$
r_{be}	base incremental resistance of base-emitter junction ($\propto 1/I_b$); inverse gradient of $I_b(V_{be})$
r_{bc}	feedback resistance modelling the Early effect ($\propto 1/I_c$); may be ignored for analytical purposes **unless the transistor has a high impedance load**
r_{ce}	models the small slope of output characteristic, mostly due to the Early effect ($\propto 1/I_c$); may also be ignored **unless transistor has a high impedance load**
C_{cb}	base-collector depletion capacitance ($\propto V_{cb}$)
C_e	emitter diffusion capacitance that models the transient behaviour of charge crossing the pn-junction
β	small signal current gain for the current through r_{be}
g_m	transconductance which operates on the voltage across r_{be}

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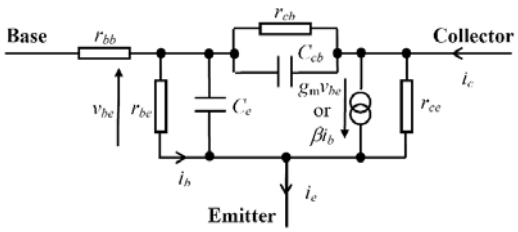
BJT cut-off frequency



param. **relationship**

C_e emitter diffusion capacitance can be determined from measurements of the transition frequency, f_t, which is the intrinsic no-load figure-of-merit of speed for a BJT

$$f_t = \frac{g_m}{2\pi(C_e + C_{cb})} \approx \frac{g_m}{2\pi C_e} \quad , \text{ if } C_e >> C_{cb}$$

deduction: Consider frequency $f=\omega/(2\pi)$ of a resonant circuit with $R_{eff}||C_{eff}$, when all energy is alternatingly stored in R_{eff} and in C_{eff}, so that $R_{eff}=1/(\omega C_{eff})$. This gives $\omega=1/(R_{eff}C_{eff})$. Here, $i_e=0$ if the voltage $v_{be}=i_b r_{be}$ across r_{be} corresponds to the voltage drop across $C_{eff}=C_e+C_{cb}$ (as C_e, C_{cb} are in parallel) where a larger current βi_b flows. Setting $r_{be}i_b=v_{be}=\beta i_b/(\omega C_{eff})$ with $r_{be}=\beta/g_m$ gives above.

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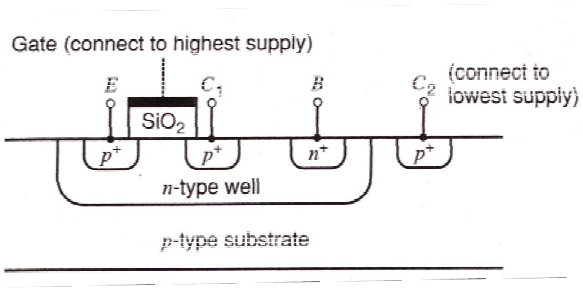
BJT design in CMOS technology



- if collector C_1 is incorporated into the well, then a **lateral pnp BJT** is formed by *E-B-*C_1 where the additional MOSFET gate ensures reverse biasing (i.e. corresponding source drain-contacts operate in the cut-off region) ***but***
- a biased substrate forms collector of a **parasitic vertical pnp BJT** formed by *E-B-*C_2 for some electrons diffusing out of the n-well

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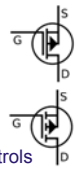
Comparison of transistor types: BJT vs. MOSFET

criterion	BJT 	JFET 	MOSFET 
principle	**diffusion** through one one forward and one reverse biased diode (depletion region)	reverse-biased pn-junction isolates gate from substrate	gate bias controls source-drain current by **electrostatic** interaction across insulating gate
input current	$i_B=i_C/\beta$ (μA)	small	$i_G\approx 0$ (pA)
input impedance	low	high	very high
I/V transfer character.	exponential (exact)	modified square law	square-law (approx.)
transcoductance	high	medium	low
carrier type	minority	minority (depletion mode)	majority
radiation resistance	low	?	high
zero-offset of $I_C(V_{CE})$ or $I_{DS}(V_{DS})$	yes	?	none
gate-channel breakdown	-	partly reversible	irreversible=destructive
applications	audio amplifiers, phototransistors	high power radio transmitters, low-noise diff. amps	switches, charge measurement devices

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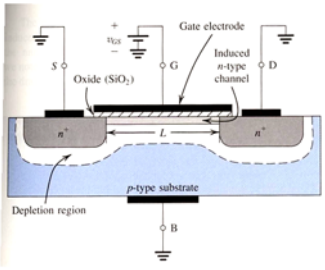
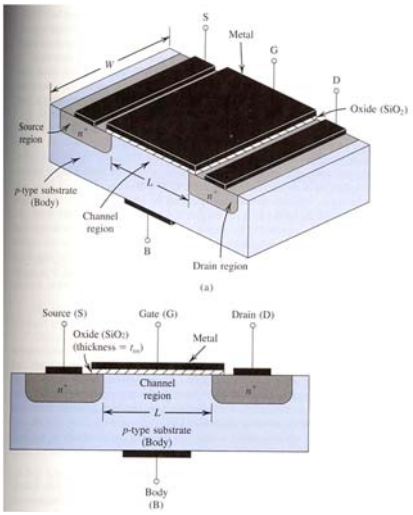
MOSFET design in CMOS technology

right: enhancement-type nMOSFET
bottom right: cross-section
bottom left: n-channel
for positive gate bias





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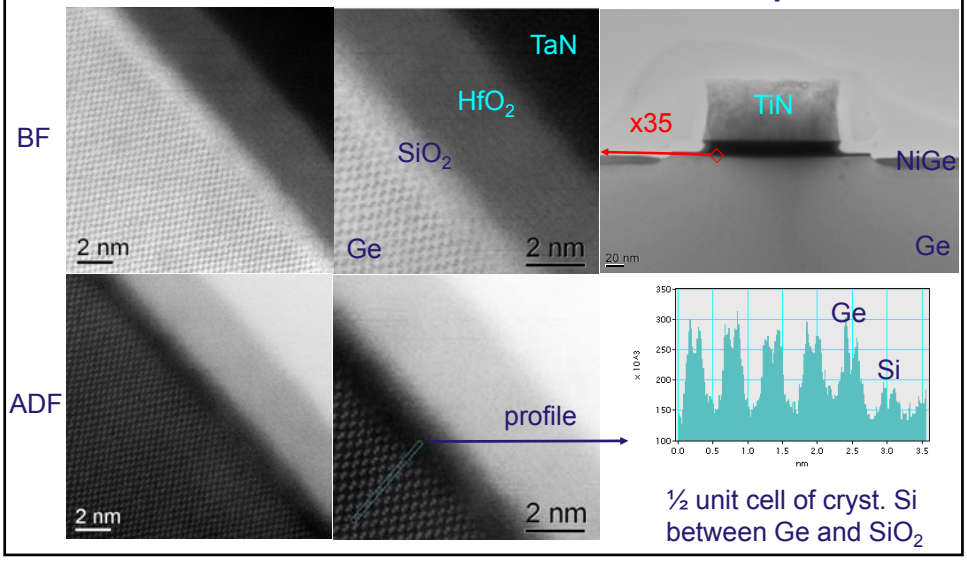
what a MOSFET gate looks like at atomic resolution by ADF imaging in a scanning transmission electron microscope



½ unit cell of cryst. Si between Ge and SiO_2

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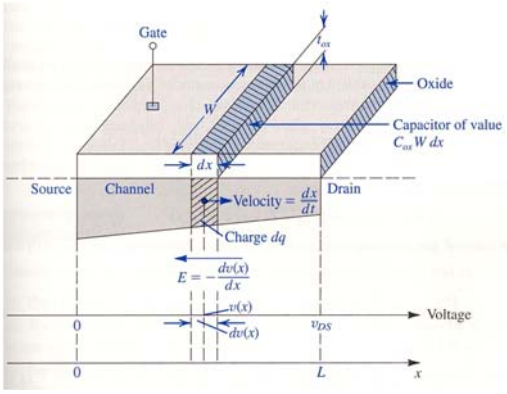
MOSFET output characteristic: derivation



- capacitance of gate oxide per unit area: $C_{ox}=\varepsilon_{SiO_2}\varepsilon_0/t_{ox}$
- capacitance of infinitesimal strip of gate at distance x from source contact: $C_{ox}W dx$
- effective voltage here: $V= V_{GS}–V_{to}–v(x)$
- charge in infinitesimal strip of n-channel: $dq=–C_{ox}\,W\,dx\,[V_{GS}–V_{to}–v(x)]$ (negative)
- electric field at this point: $E(x)=–dv(x)/dx$
  This causes the charge dq to drift towards the drain with a velocity given by the mobility of the electrons μ_n:
  $dx/dt= –\mu_n E(x)= \mu_n\, dv(x)/dx$
- resulting drift current:
  $i = dq/dt = dq/dx\; dx/dt$
  $= – \mu_n C_{ox} W [V_{GS}–V_{to}–v(x)]\; dv(x)/dx$
- drain-source current:
  $i_D = –i = \int_0^L i_D\, dx$
  where $v(0)=0$ at $x=0$ and $v(L)=v_{DS}$ at $x=L$

$$i_D= \mu_n C_{ox}(W/L)[(v_{GS}–V_{to})v_{DS} –½v_{DS}^2]$$

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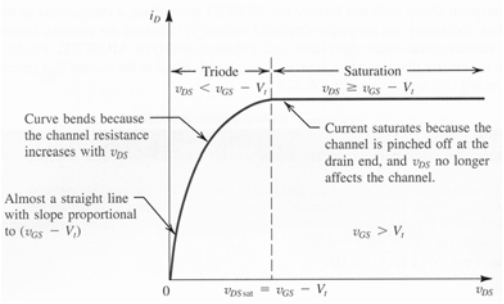
MOSFET output characteristic: modes

general: $i_D = \mu_n C_{ox}(W/L)[(v_{GS}-V_{to})v_{DS} - \frac{1}{2}v_{DS}^2]$



triode region: $V_{DS} < V_{ov}$

$i_D \approx \mu_n C_{ox}(W/L)(v_{GS}-V_{to})v_{DS}$

saturation region: $V_{DS} \geq V_{ov}$

$i_D \approx \frac{1}{2}\mu_n C_{ox}(W/L)(v_{GS}-V_{to})^2$

overdrive voltage V_{ov}

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Derivation of MOSFET transconductance

in the saturation region: $i_D \approx \frac{1}{2}\mu_n C_{ox}(W/L)(v_{GS}-V_{to})^2$

differentiating yields transconductance:

$g_m = di_D/dV_{GS} = \mu_n C_{ox}\, W/L\, (V_{GS}-V_{to}) = 2i_D/V_{ov}$

is lower than for BJTs,
as i_D is usually up to a few A, while $V_{ov} = v_{GS} - V_{to} = 0.2 - 0.5$V.
Hence, use the ratio i_D/V_{ov} as operational design parameter.

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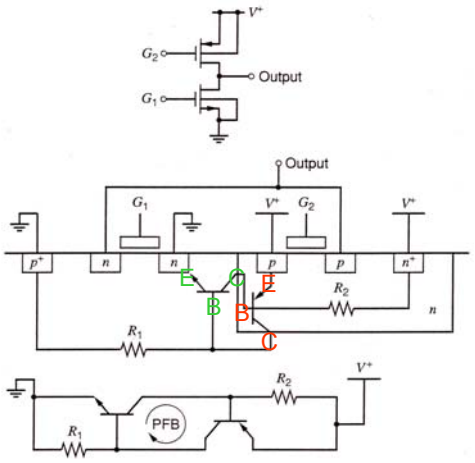
latchup in CMOS technology

typical n-channel and p-channel MOSFET device pair involves several pn-junctions to implement (e.g. as inverter)

formation of two parasitic BJTs by the n-well MOSFETs, a lateral npn a vertical pnp BJT

positive feedback occurs if the BJTs enter the active region, have β>1 and start to conduct. This can destroy the circuit.



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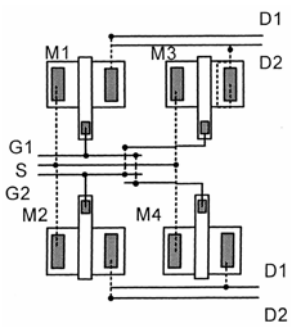
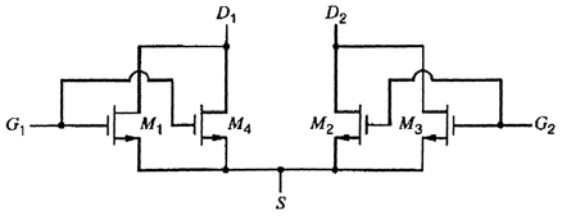
Example of typical MOSFET circuit: centroid layout

- The circuit is a differential amplifier, as the source electrodes are connected to a common current source and the diff. signals are fed into opposite base electrodes.
- Problem: diff. amplifiers are very sensitive to any mismatch between the two signal paths, which would increase the common-mode and decrease the diff. mode signal.



- Solution: replace single transistors by pairs of transistors at opposite positions on the substrate to eliminate linear process gradients, such as variations of t_{ox}, that can be decomposed into x- and y- components.
- Disadvantage: longer lines for cross-connection



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body or substrate effect in MOSFETs

- problem: substrate acts as 4th terminal (called body) which results in another pn-junction between the induced channel and the substrate
- substrate is usually common to many MOSFETs within a device and connected to most negative [positive] supply voltage in NMOS [PMOS], hence resulting reverse bias V_{SB} between source and body (in NMOS) will affect device operation by widening the depletion region and reducing the channel depth, so that V_{GS} has to be increased to maintain constant operation conditions and keep i_D constant.

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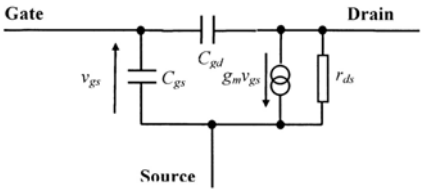
small signal circuit model of a MOSFET



NB: Occasionally, you may also see a substrate on a MOSFET small signal circuit diagram as the substrate can act like an extra gate. Usually the substrate is connected to $-V_{dd}$. This needs to be taken into account only if there is ripple on V_{dd}.

symbol	meaning
C_{gs}	capacitance between gate and source contact
C_{gd}	capacitance between gate and drain contact
V_{gs}	voltage between gate and source
V_{thresh}	threshold voltage that must be applied to the gate-source connection to create a conducting channel (enhancement mode MOSFET), typically a few volts
r_{ds}	apparent resistance of the conducting channel between source and drain. As V_{ds} is increased above V_{thresh} the conducting channel changes shape (shortens) and I_d then depends on V_{ds} in the saturation region ($V_{ds} > V_{gs}-V_{thresh}$ = '**overdrive voltage**').
I_d	**drain current:** $I_d = \frac{1}{2}\,\mu\, C_{ox}\, W/L\, (V_{gs}-V_{thresh})^2\, (1+\lambda V_{ds})$, if $V_{ds} > V_{gs}-V_{thresh} > 0$ where μ is charge-carrier mobility, C_{ox} the gate oxide capacitance per unit area, W the gate width, L the gate length and λ the channel-length modulation parameter
g_m	**transconductance** of the MOSFET device: $g_m = 2\, I_d / (V_{gs}-V_{thresh})$
f_t	**transition frequency:** $f_t \approx g_m/(2\pi C_{gs})$

Gate capacitance and high frequency behaviour of MOSFETs

Gate capacitance can be modelled by three capacitances C_{GS}, C_{GD} and C_{GB}

- MOSFET is **cut off**: channel disappears, thus

  $C_{GS}=C_{GD}= 0$, but $C_{GB}\approx \boxed{WLC_{ox}}$
- MOSFET operates in **triode region** with small v_{DS}: channel will be uniform in depth and total gate capacitance WLC_{ox} is distributed equally between source and drain ends:

  $C_{GS}=C_{GD}= ½\ WLC_{ox}$
- MOSFET operates in **saturation** where the channel has a tapered shape and is pinched off near the drain, so

  $C_{GD}=0$, $C_{GS} \approx 2/3\ WLC_{ox}$

Note: An additional small capacitance component should be added to C_{GS} and C_{GD} in all above equations due to **spatial overlap of regions where source and drain diffusion extend slightly under the oxide gate**, typically <10%

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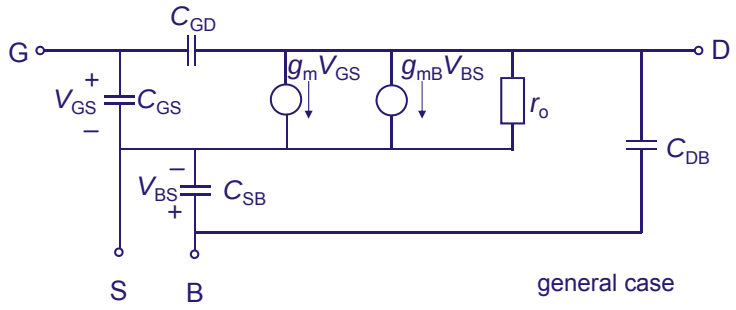
Gate capacitance and high frequency behaviour of MOSFETs

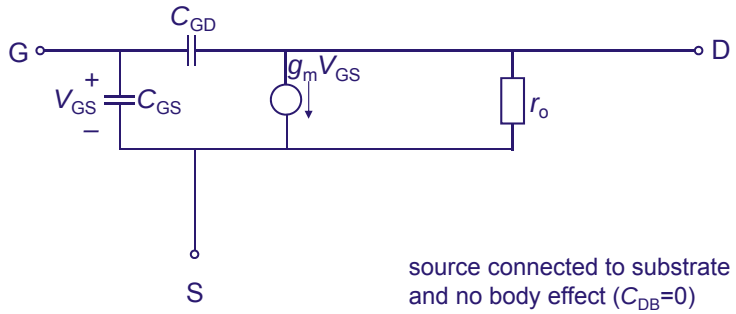
Hybrid-π model for small high-frequency signals of MOSFET



general case

Gate capacitance and high frequency behaviour of MOSFETs

Hybrid-π model for small high-frequency signals of MOSFET

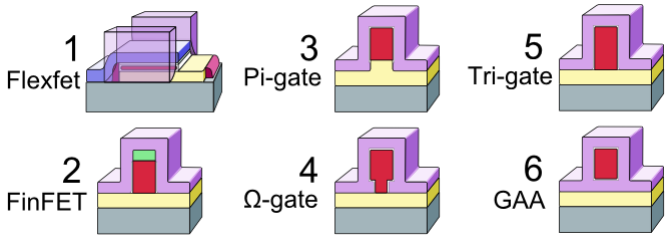


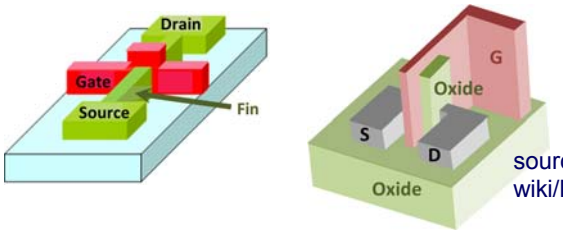
source connected to substrate (V_{BS}=0)
and no body effect (C_{DB}=0)

inject test current at gate: $i_i = j\omega(C_{GS}+C_{GD})V_{GS}$
output current at drain: $i_o = g_m V_{GS} - j\omega C_{GD} V_{GS} \approx g_m V_{GS}$
short-circuit current gain: $i_o/i_i \approx g_m/[j\omega(C_{GS}+C_{GD})]$
unity gain at frequency $f_T = g_m/[2\pi(C_{GS}+C_{GD})] = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$

multigate MOSFET devices

basic idea: wrap channel by gate extension in 3D to get better electrical control and lower leakage current; presently at 16nm gate length
problem: non-planar design is more difficult to make





source:http://en.wikipedia.org/wiki/Multigate_device