Data Provided: NONE

EEE6392 Microsystem Packaging

Spring Semester 2004-2005

Examination Solutions GLW/MH/NLS

1. a. *Describe:*

(i) the construction of a plastic dual in-line pin (DIP) package and

(ii) *its assembly using wave soldering*

Answer to part (i) to include:

Selection of good die, manufacture of lead frame, attachment of chip to lead frame using die-attach epoxy, wire bonding from chip bond pads to lead frame, overmoulding with epoxy, trimming and forming of pins.

Answer to part (ii) to include:

Requisite properties of circuit board: plated through holes of suitable diameter, solder mask layer. Insertion and clinching to secure DIP in place. Fluxing to remove oxide layers from pin and plated through holes. Pre-heating to avoid thermal shock. Passage of assembly through solder wave (including description of solder wave). Possible flux-removal. It should be pointed out that wave soldering is only possible on one side of the circuit board. **(6)**

b. *What is the junction temperature T_j for a chip dissipating 500mW when packaged in a plastic DIP16 without active cooling? (Notes: use data in Figure 1, assume ambient temperature = 20°C)*

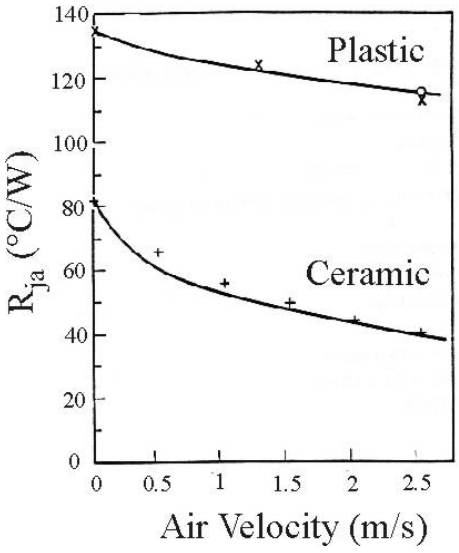

Figure 1 Thermal resistance of 16-pin DIP package as a function of air velocity from fan

Without active cooling → air velocity =0m/s, hence from Fig.1, R_{ja} = 137°C/W

From Newton's law of cooling: $\Delta T=R_{ja}Q$

hence T_j-20 = 137 x 0.5 hence: T_j = 88.5°C **(3)**

c. *What upgrades to the above packaging solution would be needed to keep the junction temperature T_j of a chip dissipating 2W below 100°C?* **(3)**

From Newton's law of cooling: $\Delta T = R_{ja} Q$,

hence $100-20 = R_{ja} \times 2$, hence $R_{ja} = 40°C/W$

From Fig.1 this implies the use of a ceramic DIP with a fan velocity > 2m/s.

d. *Why does a ceramic DIP have a lower thermal resistance than a plastic DIP?*

Typical thermal conductivity of ceramic (k~20W/mK) is ~50 times that of silica-loaded epoxy (k~0.4W/mK), therefore overall thermal resistance of ceramic DIP will be considerably lower. **(2)**

e. *Explain the physical factors that govern the data in Figure 1*

Answer to include mention of conductive, convective and radiative heat transfer:

Conduction through DIP package leading to value for package thermal resistance R_{jc}.

Convection from surface dependent on DIP surface area and orientation with respect to air flow.

Convective heat transfer coefficient *h* dependent on air velocity (turbulent or laminar flow), temperature, density, humidity, etc.

Radiative heat transfer from surface dependent on temperature of surrounding enclosure, view factor, emissivity (make item black to maximise e) **(6)**

2. a. *Describe the construction of a six-layer glass-epoxy printed circuit board (PCB) with through, blind and buried vias.*

Answer to include:

Construction of prepreg from glass-fibre mesh and uncured epoxy resin.
Lamination of copper foil with prepregs to form two-layer boards.
Via formation in two-layer boards (drilling, electroless and electroplating).
Photolithographic patterning of two-layer boards.
Lamination of processed two-layer boards with extra prepreg to produce six-layer board containing blind and buried vias.
Through via formation (drilling, electroless and electroplating). **(8)**

b. *The internal layers of a four-layer FR4 PCB are used for power and ground planes, whilst the surface layers are used for signals. State the equation for the impedance for a microstrip line and use it to calculate the impedance of a 1mm wide track on a surface layer. ($\varepsilon_{eff} = 3.5$). Comment on the calculated value.*

Microstrip impedance given by: $$Z_0 = \frac{87}{1.41+\sqrt{\varepsilon_{eff}}} \ln \frac{5.98h}{0.8w+t}$$

for $\varepsilon_{eff} = 3.5$, h = 1mm, w = 1mm and t = 35μm: $Z_0 = 28\Omega$

Comment: controlled impedence needed for high speed signals. Value of 50Ω normally sought. **(4)**

c. *What is the impedance if the track is realised as a 100μm-wide stripline on a polyimide microvia substrate? ($\varepsilon_{eff} = 4.5$)* **(4)**

Stripline impedance given by: $$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{1.9(2h+t)}{0.8w+t}$$

for ε_{eff} = 4.5, h = 200µm, w = 100µm and t = 17.5µm:

$Z_0 = 59\Omega$

d. *Discuss the measures that are taken to minimise cross talk between signals in an electronic system.*

Answer to include:

Isolate tracks on PCB as much as possible – this reduces capacitive and inductive crosstalk, but at the expense of larger substrates.

Add ground pins to connectors – this reduces inductive coupling between signals, but makes connectors more bulky. **(4)**

3. a. *Describe the three principal methods used to make electrical connections to IC die and their relative advantages and disadvantages.*

Answer must include: wire bonding, tape automated bonding (TAB) and solder bump (flip chip)

Answer to include:

Wire bonding: relative inexpensive tooling, low volume or prototype applications. Long lead lengths and large area contacts give increased parasitic impedance. Each bond is individual and so reliability is an issue. Need to get bonding tool to the contact, so spacing is wide.

TAB bonding: Fast automated method of wire bonding, tape is specific to die and therefore tooling costs are high. Each bond is made together so reliability is better. Bond lengths are still relatively long, so parasitic component are high.

Flip chip bonding. Short interconnects, so improved interconnect impedance and thermal properties. Need for precision patterned die and sub-package and assembly method involving flipping the chip is more complex and will involve more expensive tolling costs. **(6)**

b. *Why should impedances be controlled in a high-speed signal path? What are the principal sources of parasitic impedance in an IC package?*

Answer to include:

Signal waveform will be degraded at high frequency if the impedances are not controlled. Signals need to move with minimal propagation delay, low attenuation and minimal reflections.

Physical packing attributes:

Conductors, such as leads and band pads with low sheet resistances, Low mutual **(4)**

inductance and coupling capacitance between interconnects, packaging insulating materials with low dielectric constants, reductions in parasitic inductances or capacitances through appropriate package design and modeling, impedance control and matching of the chip with the package and with the package with the with the printed circuit board.*.

c. *Explain the origins of simultaneous switching noise and crosstalk. Describe how these two issues in electromagnetic interference may be minimised by appropriate packaging design.*

Answer to include:

Simultaneous switching noise:

Fluctuations in signal which result from the fluctuations in the DC supply voltage at some point in the circuit. DC supply is unable to respond to the change instantaneously. SSN is usually due to mutual inductances in the circuit, such as that between supply and signal leads and the ground plane. It can be reduced by placing decoupling capacitors in the circuit to compensate for system inductances

Crosstalk:

Signal on one line induces a signal on a nearby line. Originates from parasitic capacitance and inductance. Related to lead line resistance, cross sectional area and dielectric properties of insulators. Need transmission line modelling of package to optimise design. **(4)**

d. *Microprocessor chips generally obey Rents rule for the number of pin Input/Outputs, with Rents constant (K)= 1.5 and Rents Exponent p=0.4. Calculate the number of pin outs for a typical modern microprocessor with 10^7 logic gates. Explain why ball grid arrays offer a viable solution to packaging this type of device.*

Rents rule.

Number of pin Input/Outputs = K* (no of logic gates)^p

= 1.5 * $(10^7)^{0.4}$ = 946

Typical microprocessor ~ 25 x 25 mm, would mean 12 leads per mm

= 0.105mm between leads. Insufficient space between leads

Ball grid array offers 2 dimensional packaging solution

Average separation = 25/Sqr(946)= 0.8mm **(6)**

4. **a.** *Describe the principal advantages of flip chip packaging of ICs over that of dual in-line packages (DIP).*

Answer to include

Minimisation of interconnection thermal resistance and electrical impedance through use of solder bump as opposed to wire bond (reduction of interconnection distance and reduction in the interconnection area). Higher density of interconnects possible. Removal of intermediate wire bond step. Self alignment possible with flip chip.

(4)

b. *Describe the special considerations which need to be taken in the packaging of (i) a silicon photodetector and (ii) a fibre coupled telecommunications laser.*

Answer to part (i) to include

Package with suitable transmitting optical window, active face of die aligned to window, interconnects and contacts to have minimised interference with the optical path, minimisation of lead impedance and parasitics.

Answer to part (ii) to include

Package contains both laser and optical fibre mount. Thermal control through mounting die active face down, use of appropriate heat sink (eg: alumina), tendency towards flip chip bonding to reduce thermal resistance, need for precision alignment of laser with optical fibre, use of active alignment techniques.

(5)

c. *A 1cm^2 chip, dissipating 10W, is epoxy glued to a 5mm thick alumina substrate, which is in turn epoxy glued to a 10mm thick aluminium heat sink, as shown in Figure 4a. The chip temperature needs to be less than 120°C. Assuming linear heat conduction, what is the maximum allowed temperature at the surface of the heat sink? Assume the epoxy is coated to a thickness of 100μm.*

Data: $k_{epoxy} = 0.4W/m.K$ $k_{alumina} = 30W/m.K$ $k_{aluminium} = 216W/m.K$

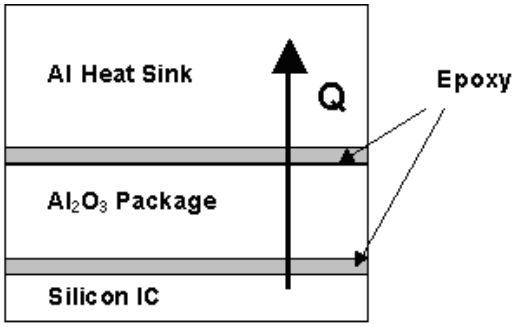

Figure 4a Thermal conduction from a Silicon IC to an Al heat sink, via an Alumina (Al_2O_3) package

$R_{th} = L/k.A$ (°C/W) and $\Delta T = Q \,.\, R_{th}$

(5)

So for Alumina R_{th}= 1.667, *Aluminium* R_{th}= 0.493 and *Epoxy* R_{th}= 2.5

So, from IC to surface, the temperature change, $\Delta T = 25+ 16.67 + 25 + 4.93 = 71.6^oC$

So heat sink surface temperature needs to be < 191.6^oC

d. *A square Aluminium plate heat sink of dimensions 50x50mm is being heated to a temperature of 80°C on one face. Forced convection is maintaining the other face at 20°C. Assuming a heat transfer coefficient (h) =110W/m²K, calculate the total heat transfer from the heatsink. If a single rectangular fin of dimensions L =50mm, W=50mm and T=5mm is now attached to the cooled side (see Figure 4b), calculate the total heat transfer from the finned heatsink. Assume the efficiency of the heat-sink is 0.8*

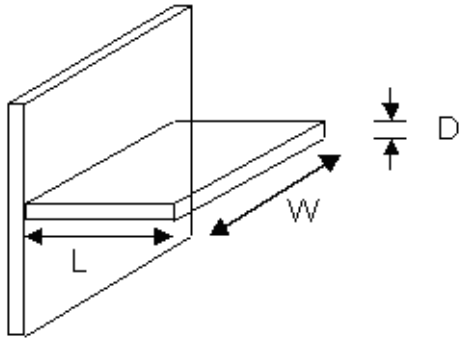

Figure 4b Schematic of finned heat sink

Heat convection from a heat sink, $Q= \eta . h. A_f. \Delta T$

(Q heat dissipation (W), η = fin efficiency, h =convective heat transfer coefficient = $110W/m^2K$, A_f= Area of the fin and ΔT= temperature difference= 60^oC)

Typical fin efficiency (η) = 0.8
No fin, efficiency (η) = 1.0

Normal Heatsink

Area=50x50mm=$2.5x10^{-3}m^2$

Q= 16.5W

Finned Heatsink

Area of fin = $2.5x10^{-3}m^2$

Q of fin = 13.2W

Area of plate heat sink = $2.5x10^{-3}m^2 – 2.5x10^{-4}m^2$ (the latter being occupied by the fin) = $2.25x10^{-3}m^2$ = 11.99W

Total conductive heat flow = 25.19W

(6)

END