Examination Feedback for the second part of EEE339: Digital Signal Processing
Spring Semester 2013-14

Feedback for the second part of EEE339: Digital Signal Processing Session: 2013-2014

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

In total, we have 57 candidates for this module. 42 chose Question 1, 56 chose Question 2, 44 chose Question 3 and 18 chose Question 4. More students chose questions in the digital signal processing section than the other one. Overall it is a good performance.

Question 1:

For 1.a, the key is to know the two main properties of the discrete complex exponential sequences, i.e. periodicity in frequency and non-periodicity in time (in general).
For 1.b, most of the students have no problem. However, some made mistakes in giving the right convolution equation.
For 1.c, the key is to understand what is impulse response and there are still some students struggling in this.
For 1.d, there are many details involved in the four Fourier-related transforms, and no one gave a 100% correct answer.

Question 2:

For 2.a, most of the students have no problem with it. Only a few of them forgot to change the sign of the coefficients.
For 2.b, many have forgotten the zero of the system at z=0.
For 2.c, it is not difficult, but some made some minor mistakes since it involves a lot of calculations.
For 2.d, only a few students struggled to give the correct process.

Question 3:

For 3.a, a standard question. Most of the students can give the correct result.
For 3.b, most of the students could not give the correct details of the block diagram for D to A conversion.
For 3.c, again a standard question. The main thing is to remember the two equations.

Question 4:

For 4.a, many made mistakes in calculating the FIR filter coefficients.
For 4.b, some could not give the correct pole vector and zero vector, and also made mistakes in giving the phase response result.
For 4.c, this may be the most difficult question and only a few can give the complete derivation.

Feedback for Digital Design part of EEE339 Session: 2013-2014

General Comments:

Many individual parts of questions were well attempted but some students could not attempt all parts of the questions that they chose to answer. You need to cover all parts of the course as an individual question may cover several topics. It was obvious that many students had a limited depth of understanding to some of the more descriptive questions. This comes from studying the material well in advance and seeking clarification at the problem classes which were very poorly attended.

Question 1:

Part(a) – Surprisingly, many students lost marks on this part which was straight from your notes. Even without doing the course, you should be able to give some description of a floating point number.
Part(b) – Generally well attempted. Remember to work out the size of the product in advance so you know what bit length to use for your arithmetic.
Part(c) – Extended bookwork requiring a good explanation. You needed to identify the three possible cases as indicated in your notes.

Question 2:

Part(a, b, c) – Well attempted by most. Part(c) required a good explanation to get the marks and many answers were too vague.
Part(d) – Most students could give good reasons for a RISC architecture but not on the advantages of having a reduced number of instructions with respect to the hardware. Many students mistakenly thought that a RISC program would require fewer instructions than a corresponding CISC program. The question required you to comment on the complexity of the control circuitry and the corresponding effect on the CPU clock speed.

Question 3:

Part(a) – Well attempted most students getting full marks for this bookwork. Remember to explain the advantages and not just describe the differences.
Part(b) – Generally well attempted. Marks lost for not working in 8-bit binary and not indicating that restoration of the remainder was required.
Part(c) – Many students had problems with this but it was the tricky part of the question. However, the technique to reduce the ROM size is more bookwork. Full marks were also given for simply reducing the number of samples held.

Question 4:

Part(a) – Well attempted but good explanations required for full marks.
Part(b) – Most students realized that non-blocking assignments were required for a pipelined solution but few drew a diagram, as required, of the original circuit synthesizing to a single register and few came up with a use for the circuit.
Part(c) – Mixed attempts at this, many solutions more closely resembled a computer flow diagram than an ASMD chart. Few students described the required states. Several students produced the circuit diagram for the multiplier shown in the notes but there were no marks for this.