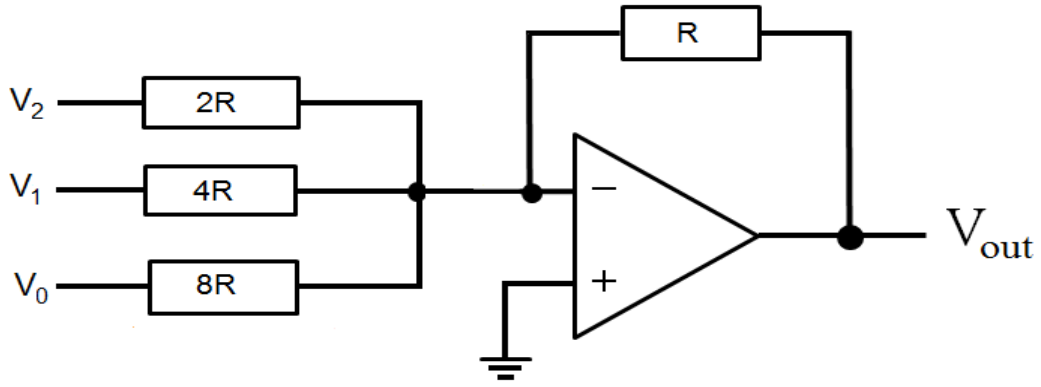
EEE225 Problem Sheet 5 – Sample Exam Questions - NJP

1. **a.** If a computer *A* has a faster clock speed than a computer *B*, does this mean that computer *A* performs faster than computer *B*? If not, why not. **(2)**

b. A certain application runs in 8 seconds on computer X, which has a 2GHz clock. We wish to design a new computer Y, which is able to run the same application in 7 seconds. It is possible to increase the clock speed for the new computer but restrictions on its architecture mean that computer Y will require 1.4 times as many clock cycles as computer X for the same program. What is the minimum clock rate that should be targeted for the new computer? **(3)**

c. A Digital-to-Analog Converter (DAC) is required to interface an FPGA to a VGA display. The circuit below is to be used for each channel.



Derive an expression for the output voltage V_{out} in terms of the input voltages and resistances shown.

For an input voltage level of 5V, what will be the output voltage level for a digital input of 110 where the LSB is applied to V_0 and the MSB is applied to V_2? **(6)**

d. In practice, the DAC shown in part (c) would not be used in higher resolution applications e.g. for an 8-bit converter. Explain the reason for this. **(4)**