Examination Feedback for EEE 6042 – Integrated Circuit Technology
Autumn Semester 2009-10

Feedback for EEE6042 Session: 2009-2010

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

My overall impression is that the candidates relied on past papers to prepare for this exam . While there was no difference in the style of questioning with previous papers, it is possible that the candidates used guess work to prepare only a selected portion of the syllabus (barring a handful). This reflects on the nature and depth of the responses.

Question 1:

This question was a generic mix of 7 short answer type questions covering the basics of material science and physics which underpins this course. The questions were on crystallography, band structure, resistivity, dislocations and gettering. Considering the fundamental nature and simplicity of the questions the students could have done better in my view. Since they are short type answers it is difficult to comment further on it.

Question 2:

This question was a test of knowledge on reactors for the CVD and the MOCVD techniques, including the construction, operation, factors affecting growth and the reagents used.

Smallest number of attempts were made on this question (which is a repeat from last year), it could smack of selectivity in choice of chapters prepared by the candidates. Because of the small numbers, it is difficult to generalize the comments on this question.

Question 3:

Question 3 was on hetero-epitaxial pseudomorphic layers, including strain and relaxation mechanisms. Part of this question was a problem on doping an ingot via the Czochralski method. The final question was to describe two techniques for implementation of an oxide and a key feature of each technique

Those candidates that got poor marks for this question were probably shooting in the dark and may not have prepared for these chapters. Amongst those that had prepared, most answered the question on hetero-epitaxy rather well, at least in terms of their understanding. Several candidates struggled with the Math in solving the problem, rather than the approach which they managed to get right. The response to the problem on oxide techniques could have been posed with more clarity (in hindsight), as it appears to have been unclear to the candidates as to whether a one-liner or a full explanation was expected. Nonetheless, the answers were varied, and did not reveal the most important techniques prevalent in industry.

Question 4:

Question 4 was based on CMOS processing: advantages and disadvantages of CMOS versus bipolar, process steps and definitions of Active Area, LOCOS and field threshold, methods of etching, salicide process and a problem on autodoping via CVD growth.

I'd consider the response as slightly disappointing. Basic definitions of the process steps and methods were not well explained despite the fact that they were often repeated in class. Most candidates answered the question on etch characteristics, which was pleasing. The problem of autodoping was also solved by most revealing that they got the Math and the approach correct.