Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2010-2011 (2 hours)

EEE6031 Advanced Computer Architectures 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. A pipelined system is required to implement the recurrence relationship for calculating *sin* and *cos* values as shown below:

$cos(\theta+\Delta) = cos\theta.cos\Delta - sin\theta.sin\Delta$

$sin(\theta+\Delta) = sin\theta.cos\Delta + cos\theta.sin\Delta$

where Δ is a small constant angular difference and $\theta=0, \Delta, 2\Delta, 3\Delta, ...$

The pipeline (without any hardware for initialisation) is organised as shown in Figure 1.

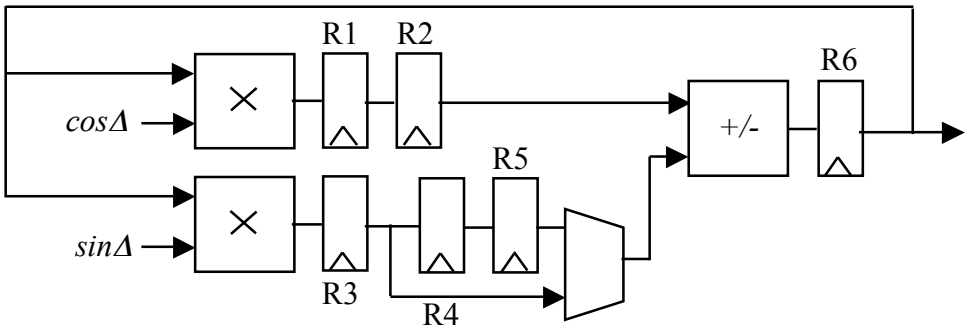

Figure 1: Pipelined System

a. Draw the reservation table for the pipeline and hence … **(7)**

b. show how the successive values of $cos\theta$ and $sin\theta$ can be calculated using this hardware. **(3)**

c. How could the hardware be initialised to produce the sequence where $\theta = 0, \Delta, 2\Delta, 3\Delta, 4\Delta, 5\Delta, \ldots$ **(2)**

d. What is the throughput of this system in terms of *sin*/*cos* pairs produced per clock cycle? **(2)**

e. Clearly, the time taken to produce a particular $sin\theta/cos\theta$ pair (θ being well away from the origin) and the accuracy with which it could be produced depends on the value of Δ. How could this process be made more rapid without sacrificing accuracy? **(6)**

2. **a.** What is the major difference between a blocking and non-blocking switch? **(2)**

b. What is the advantage of a blocking switch? **(2)**

c. **i)** Draw a schematic for a 3^3x2^3 Delta Network. **(4)**

ii) Show how digit-selectable addressing works to route a message from a source on the left hand side of the network to a destination on the right hand side of the network. **(2)**

iii) How many digits make up an address? **(1)**

iv) What would the complexity (as measured by amount of logic) of this Delta Network be compared to *Cross-Point Switch* with the same number of input and output ports? **(3)**

d. A 4 input by 8 output *CPS* is used to transfer messages in a system. Each of the four sources is generating $2x10^5$ messages per second to route across the *CPS*, randomly distributed to the 8 outputs. It takes 5μs to transfer a message. If a message fails to be routed the source re-tries (note, this does not increase the rate at which the source transmits messages across the network) until the message is transferred.

Estimate the average time taken to transfer each message. **(6)**

You can use the following expression to help you:

$$p_A = \frac{M}{NRT_{mess}}\left(1-\left(1-\frac{RT_{mess}}{M}\right)^N\right)$$

3. **a.** Describe, with the aid of a diagram, the organisation of a *superscalar* pipelined processor identifying the constraints that need to be imposed on the hardware and instruction architectures to make it work practically. **(5)**

b. **i)** What are the control dependency issues/problems that will affect the performance of such a processor? **(2)**

ii) Describe, briefly, the possible solutions to the problems caused by control dependency. **(3)**

c. A superscalar processor uses *register forwarding* to resolve data interlock problems. Show how this would operate with the following segment of a program:

```
LOAD @addr,R1          ; R1 = (addr)
ADD  R1,R3,R2          ; R2 = R1 + R3
ADD  R2,R3,R2          ; R2 = R2 + R3
SUB  R2,R4,R1          ; R1 = R4 - R2
```

(10)

4. A network of n processors is organised as shown in Figure 4. They communicate via a single time-shared bus.

Figure 4: Network Organisation

A set of m tasks is to be partitioned across these n processors. Each task exhibits a similar set of characteristics:

- each task's internal processing time is r seconds;
- each task communicates equally with every other task sending p messages to each other task;
- the time taken to transfer a message across the bus is t_b seconds and the time taken to transfer a message between two tasks on the same processor is t_i seconds where $t_b = kt_i$;
- internal processing within a task is not overlapped with its communication.

a. Show that the *speed-up* when the m tasks are mapped onto the n processors (over and above the speed achieved by mapping them all on to one of the processors) is:

$$speed-up = \frac{n\left(\frac{r}{pt_i} + m - 1\right)}{\frac{r}{pt_i} + \left(\frac{m}{n} - 1\right) + km(n-1)}$$

You may assume that congestion on the bus is not a problem.

State all assumptions made. **(8)**

b. **i)** Show that if the m, number of tasks, dominates, the *speed-up* is approximately equal to $1/k$. **(2)**

ii) What does this mean result imply? **(4)**

c. A particular application consists of 100 tasks where k=10. What ratio of r/pt_i is needed to make parallelisation just worthwhile? **(6)**

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