1. Write down De Morgan's theorems for three variables. Prove one of them by truth table. How do you know that the theorem that you have not proved is also valid?

2. Simplify F = (x + y)'(x' + y')'

3. The logical operators can be applied to strings of bits by taking each pair of corresponding bits separately. This is known as a bitwise operation. Given that X = 11010100 and Y = 10011001, find the 8-bit result for (i) X.Y (ii) $X \oplus Y$

4. (i) Draw a circuit for the function F = A.B.C using four two-input NAND gates. (Hint – Associativity , involution)
   (ii) Show how to form in inverter from (a) XOR gate (b) XNOR gate

5. Convert F = A'B + A'BC' + AC to a fundamental sum-of-products.

6. Draw the truth table and symbol for a 2-to-1 multiplexer (use table entered variables). Show how a 4-to-1 multiplexer could be formed using three 2-to-1 multiplexers.

7. Write down the truth table for $F = X.Z + X.\overline{Y} + W.Y.\overline{Z}$ and use an 8-to-1 multiplexer plus an inverter to implement it.

8. Write down the truth table for a 3-to-8 line decoder. The three input bits are A_2,A_1,A_0 and the eight output bits are $Z_7,Z_6,Z_5,Z_4,Z_3,Z_2,Z_1,Z_0$. The output should be high when selected. Write down the Boolean expression for each output and draw a logic diagram for the decoder. Show how such a decoder and one other logic gate could be used to implement the function:

   F = X'.Y + X.Z' + X'.Y'.Z

9. Draw the logic diagram of a 2-to-4 line decoder using only NOR gates.

10. An 8-to-1 multiplexer has inputs A,B,C connected to the selection inputs S_2,S_1,S_0, respectively. The data inputs I_0 through to I_7 are as follows:

    $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = \overline{D}$

    Determine the Boolean function that the multiplexer implements.