Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2011-12 (2 hours)

EEE6036 Introduction to VLSI Design

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. The pull-down network for a CMOS digital gate is as shown in Figure 1.

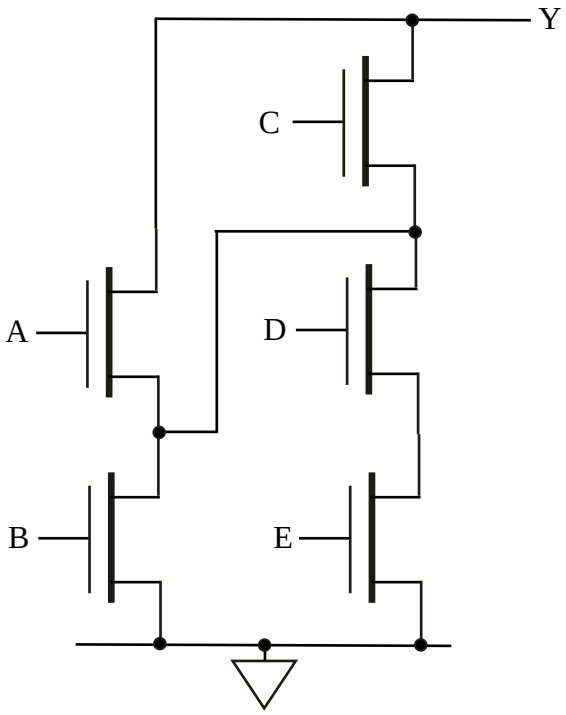

Figure 1: CMOS Pull-Down Network

i) Draw the corresponding pull-up network for the gate; **(5)**

ii) Determine the logical function of the gate; **(5)**

iii) Size the transistors in the gate, making the normal assumptions of a minimum-sized gate and that $\mu_H = 0.5\mu_E$; **(5)**

iv) The substrate connections for the transistors in Figure 1 are not shown – to which point in the circuit is it assumed that the substrates for each transistor are connected and why is this the case? **(5)**

2. **a.** **i)** Explain why might it be important to have a 2-phase non-overlapping clock generator in a clocked system? **(2)**

ii) Show how such a clock generator could be constructed; **(4)**

b. **i)** Describe, briefly, how a Delay-Locked Loop (DLL) operates; **(2)**

ii) Give one use of a DLL. **(2)**

c. A signal is to be transferred between two clock domains. The receiving clock domain is running at a clock frequency of 1.2GHz whilst the sending clock domain uses a frequency of 350MHz. In both domains, the Flip-Flops have $T_0 = t_c = 0.05$ns.

i) Show that the effect of using a simple Flip-Flop as a synchroniser would result in circa 0.6 upsets/second; **(2)**

ii) It is estimated that a rate of upsets of fewer than 1×10^{-9} upsets/second is sufficient for the overall design. Design a synchroniser capable of meeting this requirement. What would the rate of upsets be for this synchroniser? **(4)**

iii) What implications would the design of such a synchroniser have if the signal being passed from one domain to the other is acted upon in the receiving domain and a resultant signal is transferred back to the sending domain (e.g. a Request/Acknowledge handshake)? **(4)**

3. **a.** Develop a simple expression showing how power is dissipated in a digital circuit as a consequence of switched capacitance and extend this to show that the power dissipation of an entire IC is as shown in Eq 3.1:

$$P = \alpha f_{clk} V_{DD}^2 \sum_{i=1}^{N} C_i \qquad \ldots 3.1$$

defining the meaning of all of the terms. **(6)**

b. In relation to reducing power dissipation, as technology scales down, explain what happens to terms in Eq 3.1, why these changes happen and the effect that these changes have on power dissipation. **(6)**

c. An IC is composed of 10M, 2-input NAND gate equivalents. The power supply voltage is 1.5V and the IC runs with an internal clock whose frequency is 3GHz. You can assume that a minimum-sized *n*-FET has a gate capacitance of 0.5fF and that $\mu_H = 0.5\mu_E$. You can also assume that the output of each NAND gate is connected to a wire with an average capacitance to ground equal to 3fF.

Stating and justifying any other assumptions made, estimate the core power dissipation of the IC due to switched capacitance. **(8)**

4. a. A cell from a CMOS cell-library is laid-out as shown in Figure 4, below.

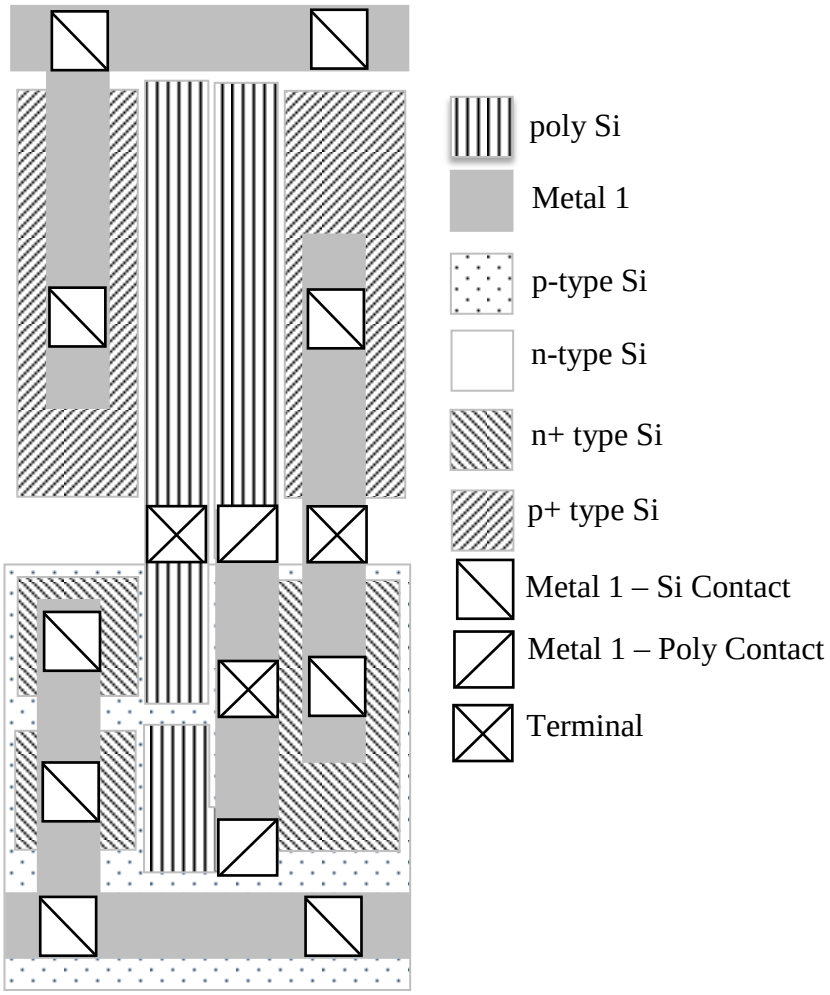

Figure 4: Layout

i) Identify the function of the gate and draw a transistor-level schematic diagram for the gate; **(8)**

ii) Estimate the ratio of μ_H to μ_E; **(2)**

iii) Identify the positive power supply (V_{DD}) and the negative power supply (V_{SS}); **(2)**

iv) What is a self-aligned gate and how is it formed? **(4)**

v) Is this an *n*-well or *p*-well process? **(2)**

vi) What is 'field oxide'? **(2)**

NLS