Next Part of Course

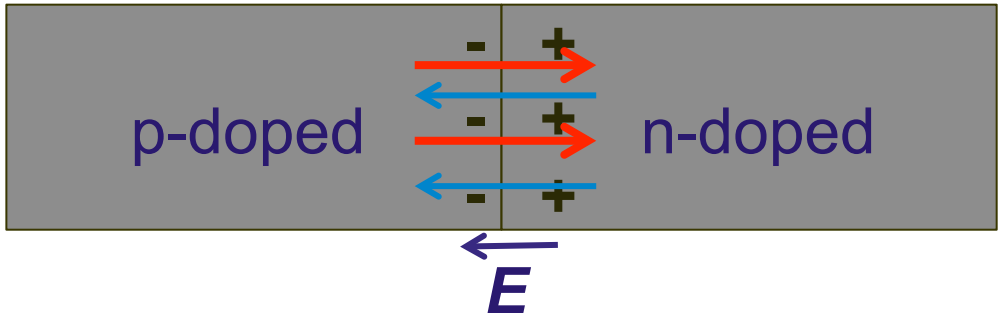
Transistors

- Use pn junctions to illustrate Junction Field Effect Transistor (JFET)
- Metal Oxide Semiconductor FET (MOSFET)
- Bipolar transistor – uses pn junctions

Lecture 14

- Review p-n junctions
- Introduction - Junction field effect transistor – JFET
- Basic operation
- Origin of output characteristics

PN Junction - *J* must be zero with no external applied voltage



- Diffusion will occur (holes as red arrows – L to R, electrons as blue arrows – R to L)
- Fixed dopant atoms near the interface form a ‘space charge’
- An electric field must be generated to oppose the diffusion and create a drift current which is equal and opposite to the diffusion current i.e. net $J = 0$ – note that the built-in field direction opposes both electron and hole diffusion current
- This electric field will appear as a built-in potential, V_0, within the junction

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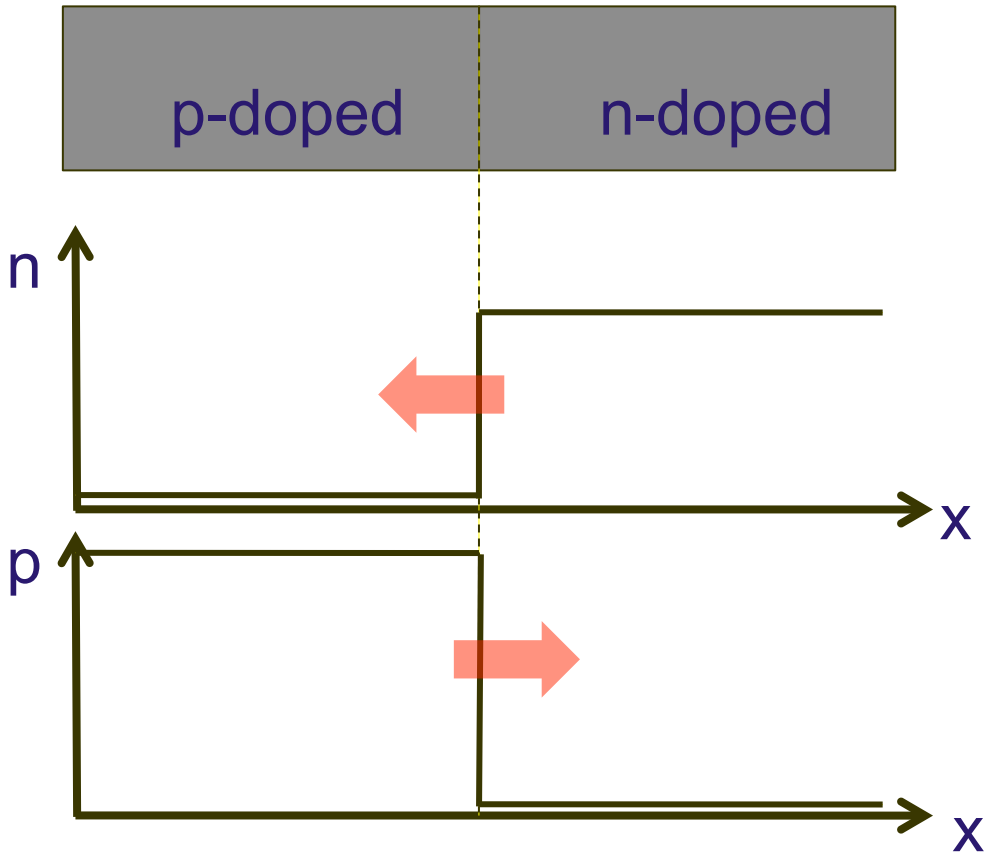
Free Carrier Diffusion

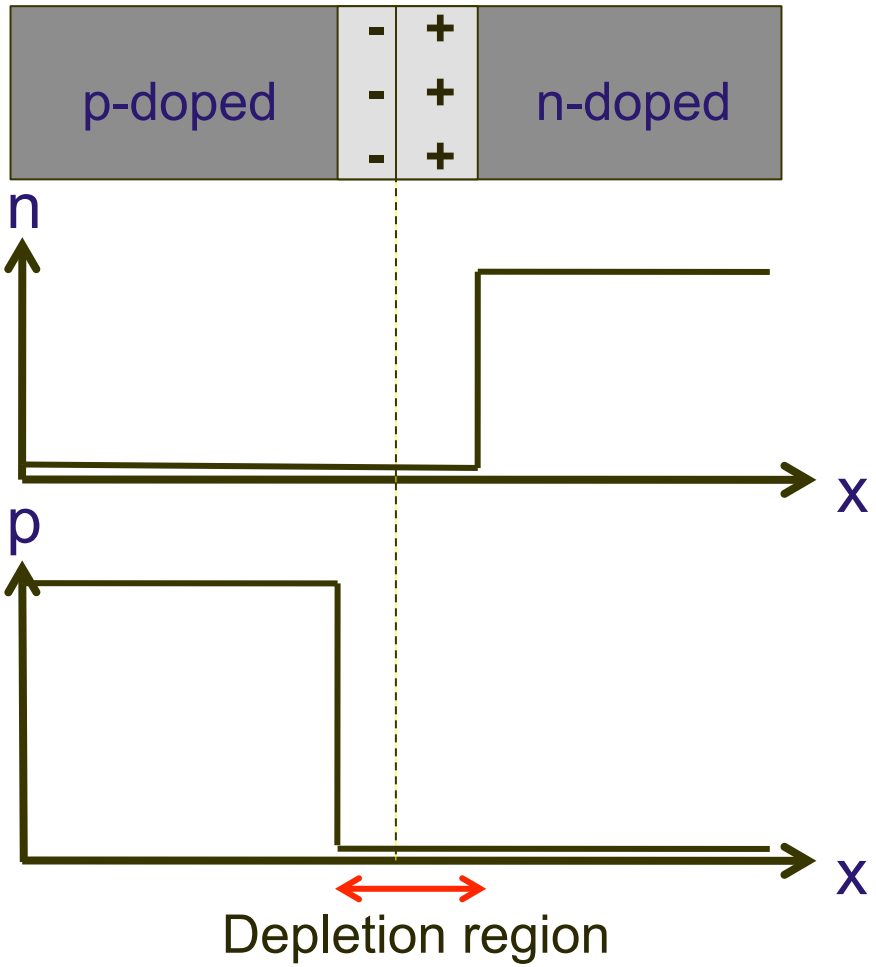
(Just after connection)

- Holes diffuse into n-material where they are minority carriers and recombine with electrons
- The holes leave behind fixed ionized (-ve) acceptors in p-region
- Similar behaviour for electrons
- Get *depletion* of free carriers at junction

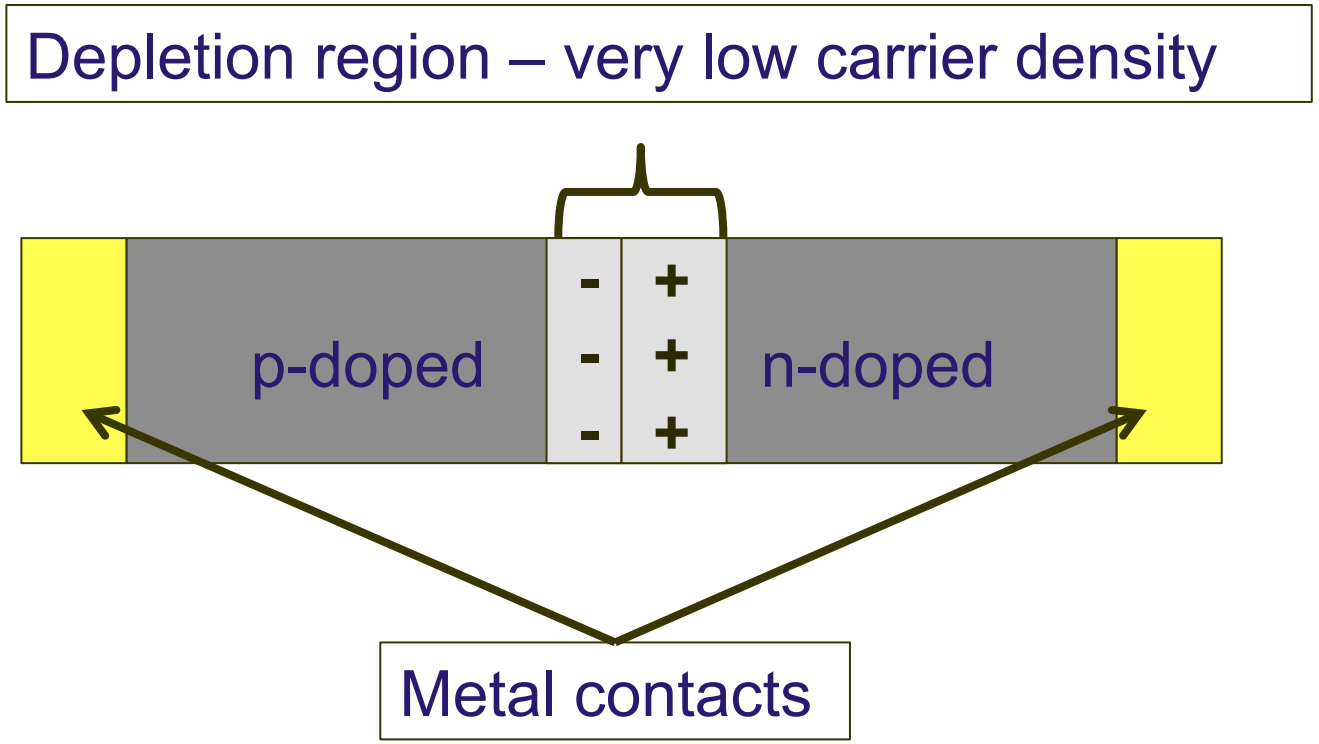


Depletion Region

- Electron diffusion right to left (current left to right)
- Hole diffusion left to right (current left to right)
- At equilibrium there must be no net current so an ***E***-field is generated
- Results in a potential difference V_0 between n and p regions



Complete Diode Structure



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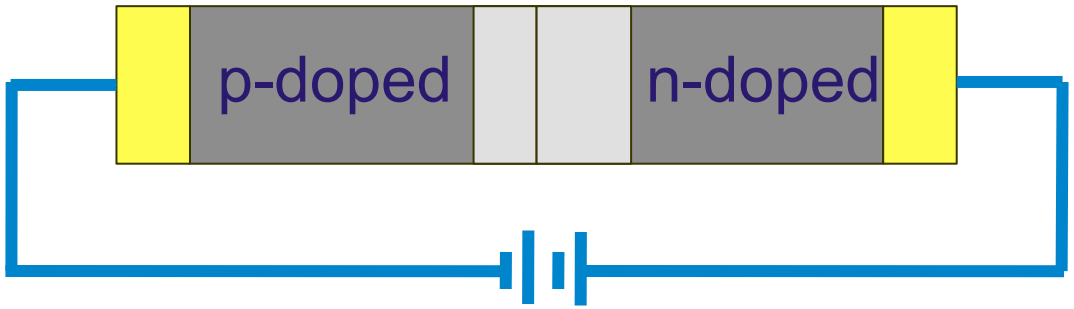
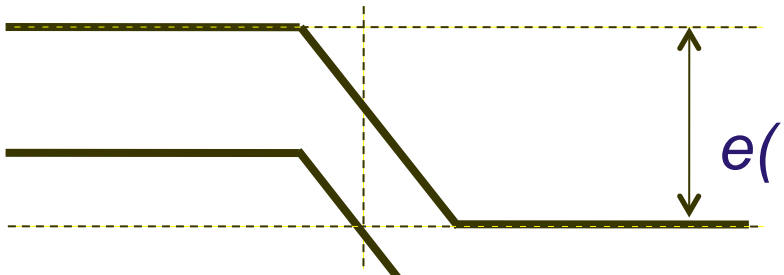
Reverse Bias, V_r

Barrier to diffusion increased by bias voltage



Conduction Band

Valence Band



$J_h^{diffusion}$ $J_e^{diffusion}$

J_h^{drift} J_e^{drift}

Reverse Bias, V_r

- Applied reverse bias - the potential barrier and the electric field is increased
- This increases the depletion region width (need more “exposed” fixed ionized dopant atoms to achieve the higher voltage)
- The potential barrier becomes larger – so get reduced diffusion current
- Drift Current – same as zero bias - very few minority carriers to contribute to drift (mostly comes from thermally generated carriers) – so very small

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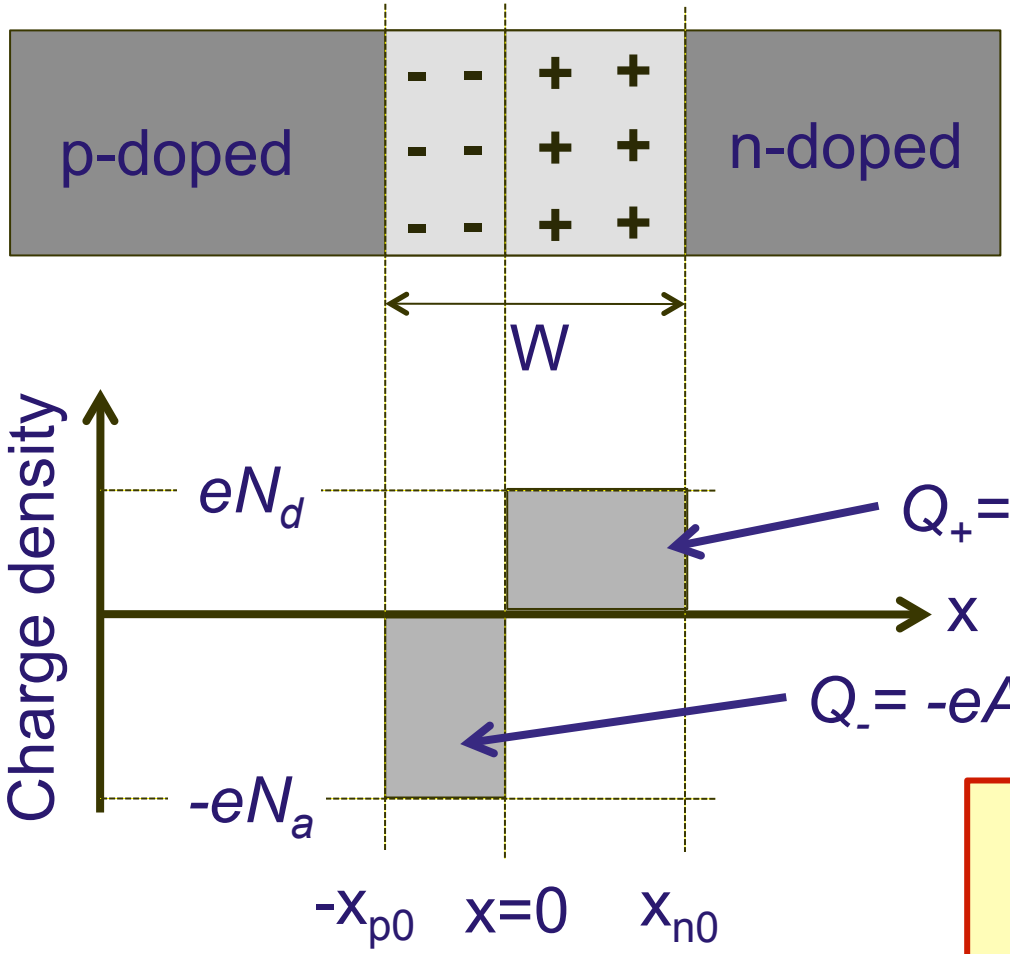
Space Charge at a pn Junction



Cross-sectional area A, doping densities of N_d, N_a for donors and acceptors, respectively.

$Q_+ = eAx_{n0}N_d$

$Q_- = -eAx_{p0}N_a$

$$x_{p0}N_a = x_{n0}N_d$$

If $N_a >> N_d$ then $x_{po} << x_{no}$

Depletion region width

We saw before (lecture 11)

External bias voltage

$$W = \left[\frac{2[V_0 + V]\varepsilon}{e} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2}$$

If $N_a >> N_d$ then depletion is mostly in the low doped n-region

$$W = \left[\frac{2[V_0 + V]\varepsilon}{e} \left(\frac{1}{N_d} \right) \right]^{1/2}$$

That is $W \alpha V^{1/2}$ if $V >> V_o$

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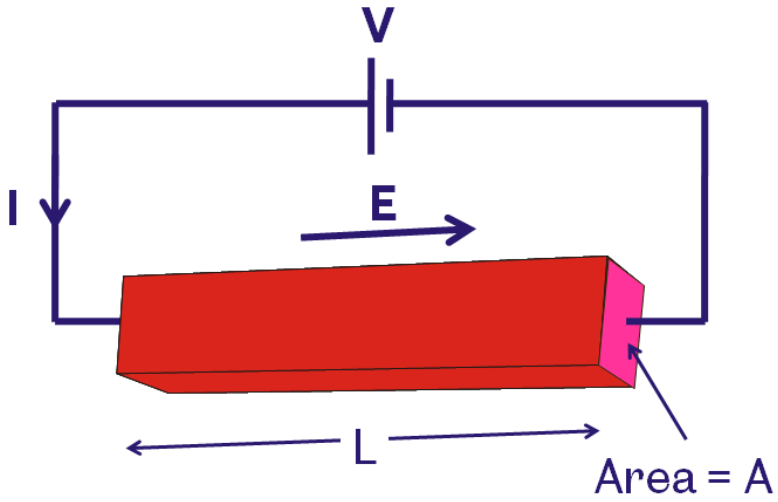
Current Flow (recap)

$$J = ne\mu E = \sigma E$$

$$I = A\sigma E$$

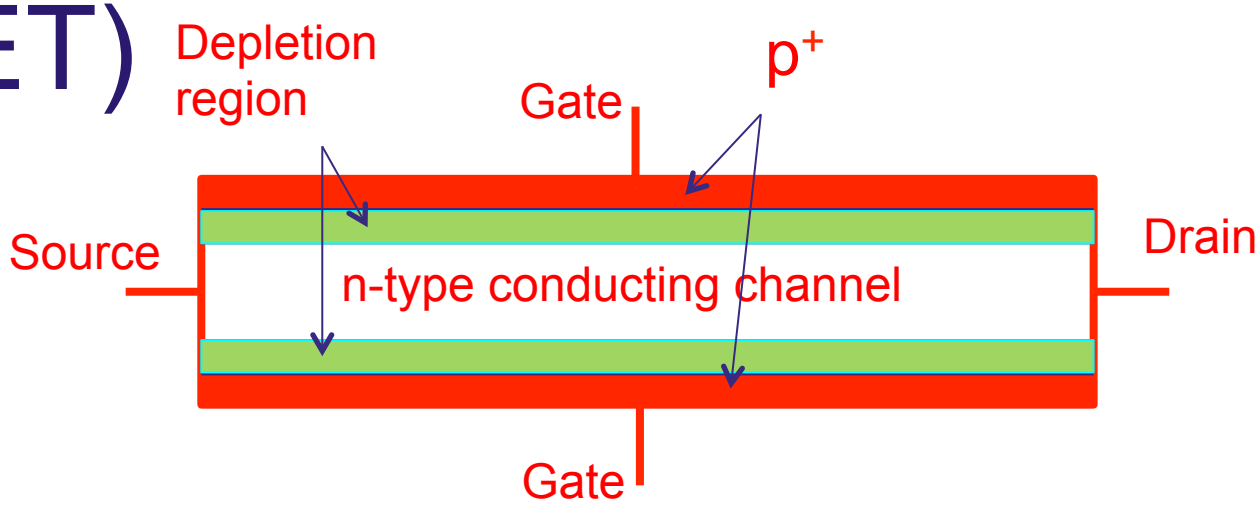
$$\sigma = ne\mu$$



If we can modulate the cross-sectional area (or the electron density, *n*) we can vary the resistance of a piece of semiconductor and hence vary the current (basis of a transistor)

- we can vary *A* with a p-n junction

Junction Field Effect Transistor (JFET)



- Electrons flow in the n-type channel between source and drain when a drain voltage is applied
- Reverse biased p^+n junction formed between gate and channel
- Channel acts as a distributed resistor
- Negative gate voltage increases depletion region in channel, reduces the cross-sectional area and therefore increases the resistance
- Most of the depletion region is in the lower doped n-type channel ($p^+>>n$)

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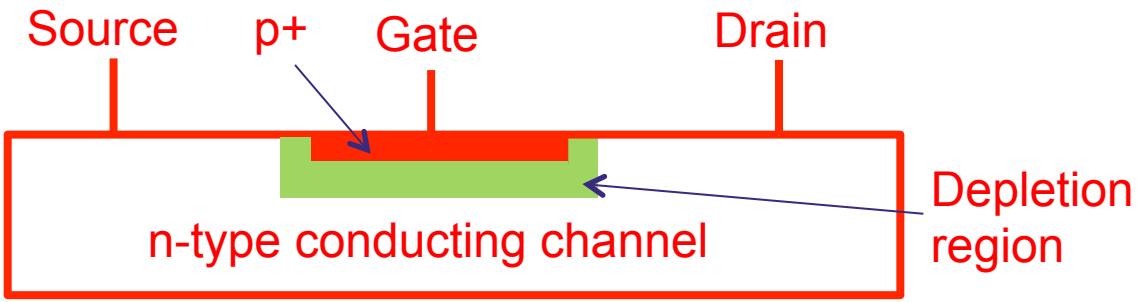
JFET – Planar Structure



- All contacts on surface (easier to make)
- Varying the gate voltage varies the cross-sectional area of the n-type channel under the gate and hence its resistance
- In this structure only the channel under the gate is modulated
- Transistor action allows drain current to be controlled by the gate voltage
- The JFET is known as a **unipolar** device i.e. uses only one type of carrier – the illustration is for an n-channel device – a p-channel device with n^+ gate regions is possible but get reduced performance due the lower mobility of holes

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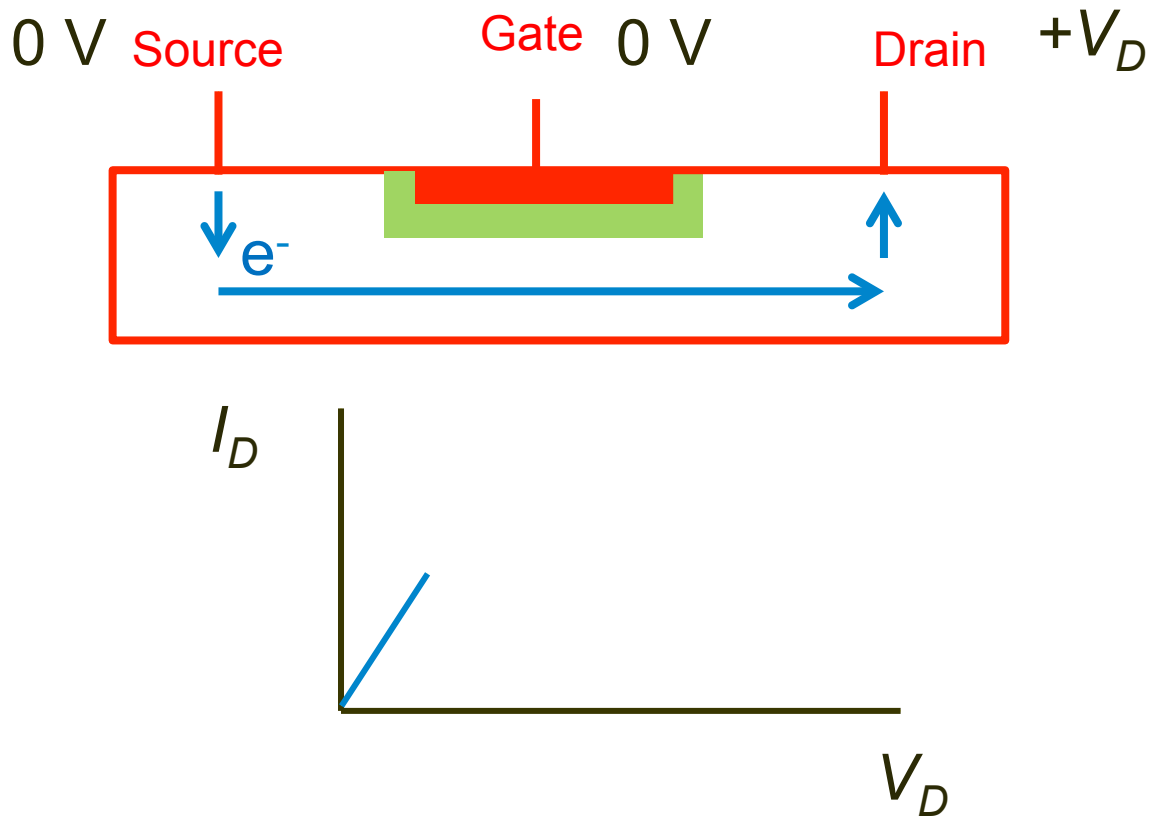
JFET – Output Characteristics



Zero gate voltage – small voltage between source and drain gives electron drift and hence drain current – behaves as a resistor.

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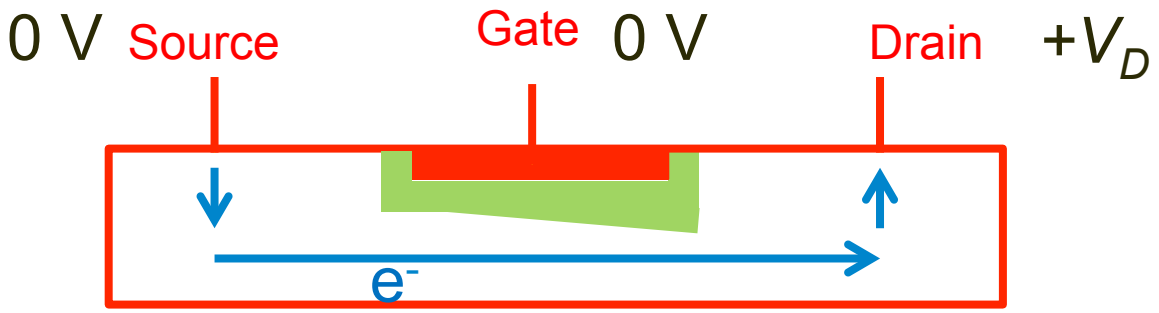
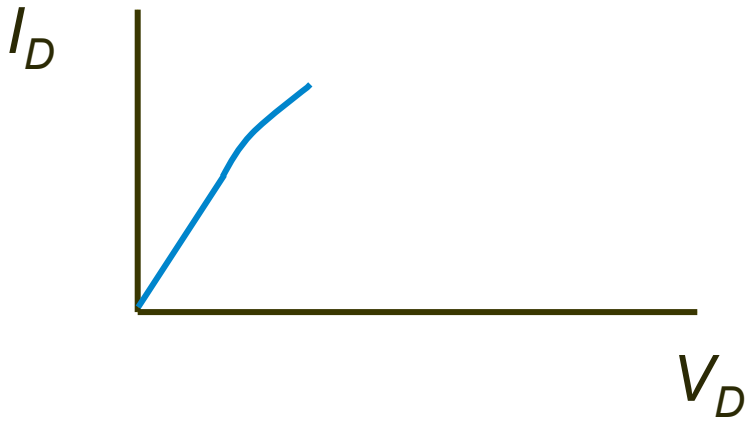
JFET – Output Characteristics





Zero gate voltage - as V_D and I_D increases further, the positive voltage at the drain increases the p^+n junction reverse bias at the drain end – increasing the depletion width there and so constricting the channel. As the resistance of the constricted channel is higher (reduced slope) – *I/V* plot is no longer linear.

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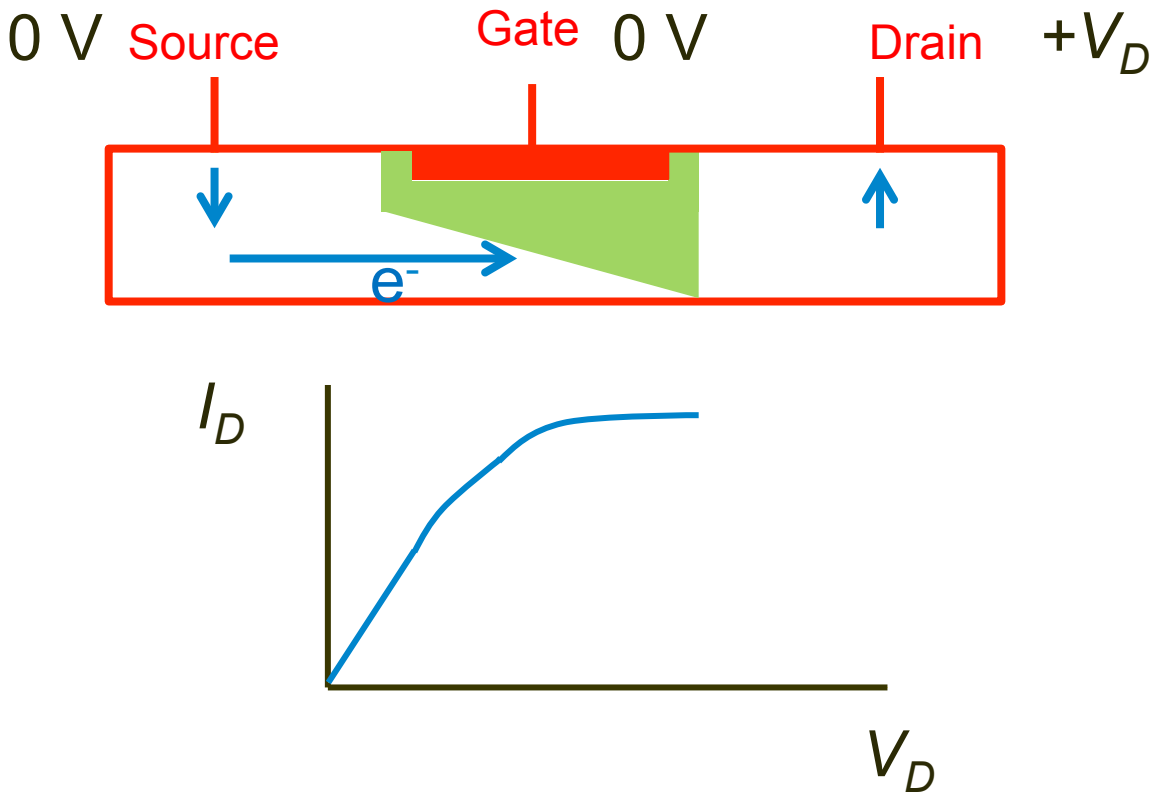
JFET – Output Characteristics



At higher V_D the depletion region closes the channel completely (called **pinch-off**) – the current I_D cannot increase with increasing V_D and it saturates (why does I_D not drop to zero?)

Summary

- N-channel JFET has a p^+-n diode gate with contacts arranged to allow a bias to vary the depletion region width
- Resistance of the channel can be controlled by the gate voltage
- Drain bias affects channel resistance and hence drain current
- This device can operate as a variable resistor or as an amplifier