Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (2.0 hours)

EEE336 Digital Design

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Describe what is meant by *cache memory* in a microprocessor. Briefly explain what you understand by the terms *direct mapping*, *fully associative mapping* and *set associative mapping* in the context of cache memory. **(8)**

b. Perform the calculation of $1111_2 \div 110_2$ (decimal 15 divided by 6) by restoring division. Show each step of the calculation using 8-bit binary arithmetic. You must start the process by left shifting the divisor by three places (multiplication by 2^3) in order to model a process whereby any four bit positive integer could be divided by any three bit positive integer. **(6)**

c. An Intel 8086 processor has a 16-bit address bus and 16-bit data registers. However, it is still able to address 1Mb of memory. Explain how this is achieved, clearly describing how the address is generated. **(6)**

2. **a.** Explain the operation of a serial multiplication circuit using shift-and-add multiplication. Be sure to carefully describe the initial circuit state. **(5)**

b. Describe the different circuit states (just before each rising clock edge) for the case of multiplying the two unsigned 4-bit binary numbers, 1010 x 0110; set out your answer as a table. **(6)**

c. Explain why basic shift-and-add multiplication does not work for multiplying 2s-complement numbers. **(6)**

d. For n-bit wide multiplicands and multipliers, what determines the maximum speed of operation of the serial multiplication circuit as n becomes moderate to large? **(3)**

3. **a.** Describe the implementation of a stack in a microprocessor. In particular, how is a stack managed and manipulated? **(4)**

b. How can a stack be used for passing parameters (arguments) to a function or procedure? **(4)**

c. A finite state machine is required which can generate a Fibonacci sequence. This is a sequence of numbers that follow the pattern:

0, 1, 1, 2, 3, 5, 8, 13, 21, 34 ……

The number in position ***i*** of the sequence is given by adding the previous two numbers:

fib(i) =

0, if i = 0

1, if i = 1

fib(i-1) + fib(i – 2), if i > 1

This component will be part of a larger system, which will supply a signal ***start*** which indicates the start of an operation and ***i*** which indicates how many numbers in the sequence to generate. The component should output the sequence itself and a signal ***done*** should go high for one cycle when the sequence is complete.

Draw an ASMD (Algorithmic State Machine with Datapath) chart for this component, clearly describing the purpose of any states that you use. **(12)**

4. **a.** With reference to the Verilog Hardware Description Language, describe with the aid of a timing diagram, what you understand by:

i) Inertial Delay

ii) Transport Delay **(6)**

b. Draw a truth table for the circuit described by the following Verilog code.

```
module mycircuit (output reg [3:0] y, input [1:0] a);
integer i;
always @ (*)
  for (i = 0; i <= 3; i = i + 1)
    if  (a == i)
      y[i] = 1;
    else
      y[i] = 0;
endmodule
```

(4)

Describe a use for this circuit.

c. Explain the function of a Barrel Shifter. Show with the aid of a suitable diagram, how a 4-bit barrel shifter could be implemented using only combinatorial multiplexers. **(6)**

d. What are the advantages of implementing a shift register in a microprocessor CPU with combinatorial logic as opposed to sequential logic based upon D-Type flip-flops. **(4)**

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