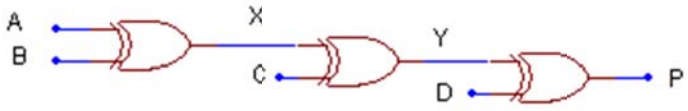
1. With the aid of a timing diagram, explain how the circuit below can be used to detect odd parity for the four bit input A,B,C,D.



If the inputs are all presented at the same time and the propagation delay for each gate is 10ns, what is the maximum theoretical speed of operation for this circuit. Is this circuit hazard free? If not, show the type of hazard present using a timing diagram. (Hint – what output results if A,B,C,D change simultaneously from 0000 to 1001). How could the circuit be redesigned using the **same gates only** to eliminate the hazard? Assume each gate has an identical propagation delay and wiring delays are zero.

2. Exam type combinatorial logic question:

(a) Derive the simplest Boolean equations that describe the operation of a single-bit full-adder. Make sure that the two data inputs, A and B, the carry-in bit C_i, the sum output S_o, and the carry-out bit C_o, are clearly represented in your answer.

(b) Show how you would connect some single-bit full-adders together to make a full adder circuit suitable for adding together two 4-bit binary integers.

(c) Simplify the equations in part (a) of this question for the case when B = 0 always.

(d) Simplify the equations in part (a) of this question for the case where B = 1 and $C_i = 0$ always.

(e) Explain briefly how you would calculate the 2's complement of a binary integer.

(f) Hence, using your answers to the previous parts of this question, design the simplest circuit you can using only AND, OR and XOR gates and inverters, that will produce the 2's complement of a 4-bit binary integer. Be careful to clearly show all of your working.

3. Explain the difference between Mealy and Moore type finite state machines.

4. Explain the difference between *Binary* and *One Hot* encoding.

5. A digital system has a clock generator that produces pulses at a frequency of 80MHz. Design a synchronous circuit that provides a clock with a period of 50ns.