Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2009-2010 (2 hours)

Integrated Circuit Technology 6

Answer **THREE** questions. **No marks will be awarded for a solution to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

1. a. Define sheet resistance. Describe diagrammatically, two methods to measure the sheet resistance of a material. **(4)**

b Given a piece of material, explain how you would determine whether it is a direct or indirect bandgap semiconductor. Use diagrams as necessary **(3)**

c Explain with the aid of a diagram what is meant by Hall effect. **(2)**

d Name 4 crystal lattice systems. **(2)**

e Explain how the Miller index of a lattice plane in crystalline silicon is defined. **(3)**

f What is a Burgers vector? Explain with the help of a diagram the method to determine the Burgers vector? **(3)**

g Name 4 unwanted transition element impurities in Si: What deleterious effect do they have? What is the name of the technique used to remove unwanted impurities of this type? **(3)**

2. a. Show by means of diagrams three generic designs of a CVD chamber. In a CVD reactor, what is a susceptor and what is it made of and why ? **(4)**

b Describe the operation of CVD and MOCVD reactors. What factors affect the growth characteristics in both cases ? **(10)**

c What are the requirements of reagent materials in a MOCVD reactor ? **(4)**

d Name common gaseous sources of Arsenic, phosphorus, boron, gallium, indium and aluminium. **(2)**

3. a. What is a hetero-epitaxial pseudomorphic layer ? Give diagrams of two such layers with built-in strain opposite to one another. How and under what conditions does such a pseudomorphic layer relax: consider separately the low misfit and high misfit regimes ? **(10)**

b A silicon ingot is grown by the Czochralski technique. The ingot is doped with

Arsenic and the initial concentration of impurity in the melt is 0.01%. If the segregation coefficient of Arsenic in Si is 0.3, what is the initial concentration of Arsenic in the grown ingot?

If C_0 is the initial concentration of the impurity in the melt, C_s is the final concentration of the impurity in the crystal, x is the fraction of melt solidified and k_0 is the impurity segregation coefficient, then, given that

$$C_S = k_0 C_0 (1-x)^{k_0 - 1}$$

Calculate the fraction of the melt solidified when the concentration of Arsenic in the ingot has risen by a factor of 30 from its initial value. **(5)**

c Describe two ways by which an oxide can be implemented on a silicon wafer ? Name one key feature of each method. **(5)**

4. **a** Name main operating advantages and disadvantages of circuits produced using CMOS and bipolar technology. **(3)**

b In a CMOS process flow what step defines the Active area ? What is the role of (a) LOCOS (b) Field threshold adjust implant **(3)**

c Name two methods of etching insulating films? What are the etch characteristics of each method ? **(4)**

d Explain what is meant by a salicide process? Name typical silicides used in modern day CMOS processes? **(4)**

e CVD is used to grow a silicon epitaxial layer upon a silicon substrate at a temperature of 1000 ºC. If the layer growth rate is 0.5 µm/min and the substrate activate is heavily doped with boron, deduce by calculation whether autodoping of the layer would be expected to be a problem? You can assume that the activation energy for boron diffusion in silicon (E_a) is 3.46 eV, the boron diffusion pre-exponential factor (D_0) is 0.76 cm^2/s and Boltzmann's constant (k) is 8.62×10^{-5} eV/K. **(6)**