The University Of Sheffield.

Data Provided:
Electronic charge (e) = -1.6×10^{-19} C
Permittivity of free space (ε_o) = 8.854×10^{-12} F.m^{-1}
Relative Permittivity (ε_r): Si=11.7, SiO_2=3.9.
Saturation velocity: Si=1.1×10^{5}m.s^{-1}, GaAs=2×10^{5}m.s^{-1}
Electron mobility (at 300K); Si=0.15m^2.v^{-1}s^{-1},
GaAs=0.80m^2.v^{-1}s^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2010-2011 (2 hours)

EEE416 High Speed Electronic Devices 4

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Draw the typical output characteristics of a MESFET for different gate voltages and indentify the linear, saturation and breakdown regions. Describe briefly the mechanisms responsible for these regions, using diagrams if necessary. **(4)**

b. Derive an expression for the cut–off frequency of a GaAs MESFET by consideration of the a.c. input and output current in the device. You may assume the drain current is given by:

$$I_D = (n_s e)V_{sat}$$

where (n_se) is the sheet charge on the gate and V_{sat} is the saturation velocity.

Calculate the cut-off frequency for a device with a 20μm gate length. If needed, you may assume a value of $n_s = 1\times10^{14}$m^{-2}. **(6)**

c. Describe the concept of the high electron mobility transistor (HEMT) with the aid of schematic diagrams. Describe how this device can give improvements in transconductance (g_m) and cut-off frequency (f_T) compared to a MESFET. **(4)**

d. The transconductance (g_m) and cut off frequency (f_T) of a MESFET and of a HEMT are dependent on the following parameters;

$$g_m \propto \frac{W_{ch}.Z.N_e.\mu_e}{L} \qquad f_T = \frac{v_{e,sat}}{2\pi L}$$

where W_{ch} is the channel width, Z the gate width, L the gate length, N_e the electron density, μ_e the electron mobility and $\upsilon_{e,sat}$ is the electron saturation velocity.

Typical values of μ, W_{ch} and N are given in table 1 for each device. You may assume that the other parameters are constant. Calculate the ratios of (i) g_m and **(6)**

(ii) f_T for the HEMT compared to the MESFET. Comment on the difference between the f_T and g_m values.

	μ_e	W_{ch}	N_e
MESFET	$0.3m^2V^{-1}s^{-1}$	500nm	$5x10^{22}m^{-3}$
HEMT	$0.9m^2V^{-1}s^{-1}$	300nm	$2x10^{22}m^{-3}$

Table 1: MESFET and HEMT device parameters

2. a. The structure of an Si IMPATT diode is shown below:

100nm p+ ($2x10^{24}m^{-3}$)	Cathode contact
100nm n ($5x10^{21}m^{-3}$)	Avalanche Region
800nm intrinsic (assume background doping = $1x10^{20}m^{-3}$ n-type)	Drift region
200nm n ($2x10^{24}m^{-3}$)	Anode contact

The device is used as a high frequency oscillator. What is its operating frequency?

Sketch (i) the carrier concentration and (ii) the electric field profiles through the device.

Calculate the threshold electric field (E_n) needed for complete ionisation in the avalanche region. The calculation requires the ionisation coefficients α and β for electrons and holes, respectively, in the silicon which is given by:

$$\alpha(E) \approx \beta(E) \approx A.\exp\left(-\frac{B}{E_n}\right)$$

You may assume values for the constants A and B of $3.8x10^7$ and $3x10^{-6}$ respectively.

What is the device breakdown voltage resulting from this value of E_n?

(10)

b. Describe the operation of floating gate flash memory, based on a Si MOSFET, with the aid of diagrams. Explain how the device can be written to achieve either an 'on' or an 'off' state and how it can be erased.

A device with a SiO_2 top insulator is addressed with a read voltage of 1.5V applied to the top gate. The threshold voltage when there is no net charge on the floating gate is 1.0V. Calculate the number of electrons required on the floating gate to change the read out to a 'zero' bit. You may assume the top insulator is 20nm thick and that the gate has dimensions of 100 x100 nm.

(10)

3. **a.** Sketch the cross-section of an n-channel enhancement mode MOSFET showing clearly the bias arrangements, the gate, source and drain contacts, the depletion regions and the conducting channel for each of the following bias conditions:

(i) Gate-source and drain-source voltage = 0
(ii) Gate-source voltage greater than the threshold voltage and much greater than the drain-source voltage
(iii) Bias as in (ii) above except that the drain-source voltage is equal to the gate source voltage minus the threshold voltage (channel pinch-off condition)

(6)

b. Draw band diagrams which describe the bias conditions in (i) and (ii) above, showing the conduction and valence bands, the position of the Fermi level in the gate and semiconductor channel and any other relevant features.

(4)

c. A CMOS foundry uses SiO_2 as a gate oxide. For its present devices it obtains a gate capacitance (C_{ox}) of $1.8x10^{-11}F.m^{-2}$. To improve performance, it wishes to increase the oxide capacitance by a factor of 2. Two new 'high-k' oxides, A and B, are under consideration. Some relevant data on these oxides is given in table 2, below.

	Si	SiO_2	Oxide A	Oxide B
Relative Permittivity, ε_r	11.9	3.9	8	16
Electron Affinity, χ, (eV)	4.1	0.95	1.0	3.7

Table 2: Data on Si and various oxides used in the CMOS foundry

Calculate the thicknesses of oxides A and B required to give the required increase of a factor of 2 in C_{ox}

By consideration of the relative electron affinities with respect to Si, discuss the overall suitability of oxides A and B for the process.

(10)

4. **a.** The cut-off frequency for an npn bipolar transistor can be expressed as a function of the total device delay time τ_{EC} as follows;

$$f_T = \frac{1}{2\pi\tau_{EC}}$$

List the individual components of τ_{EC} and identify which of these is related to junction capacitance.

Draw a small signal equivalent circuit for the device and use this to derive expressions for the current-voltage dependency of the two junction components.

Suggest methods to reduce these delay components by appropriate device design.

(9)

b. Describe how the construction of a heterojunction bipolar transistor (HBT) differs from a simple bipolar transistor. What are the advantages of the HBT in terms of increased g_m and f_T **(3)**

4. c. For each of the following parameters, describe how the process of device scaling has led to improvements in CMOS IC performance and cost over many years.

For each parameter, discuss issues affecting the future scaling in relation to physical limitations, materials problems and/or device process issues.

(i) Switching voltage
(ii) Gate dielectric thickness
(iii) Gate dielectric material
(iv) Gate length

(8)

MH / RAH