Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2007-2008 (2 hours)

Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Show how the expression for I_{DS} for a *n*-type MOSFET in the Ohmic region (shown in equation 1) can be derived.

$$I_{DS} = \frac{\mu_E \cdot C_{OX} \cdot W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS} \qquad (1)$$

Ensure that your answer includes a diagram of a FET showing how the voltages and current are conventionally defined. Additionally, you should identify the condition that results in Ohmic behaviour. **(7)**

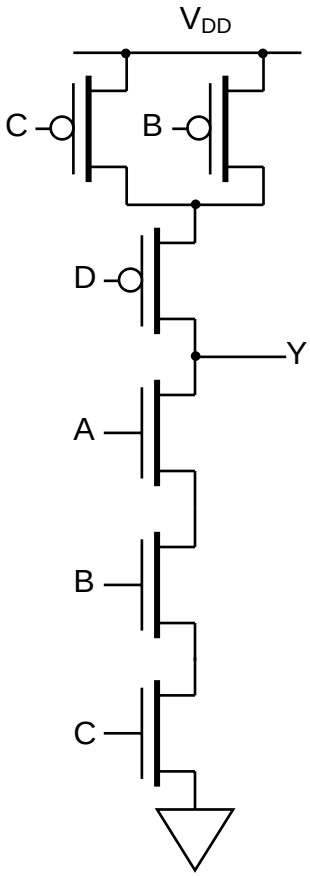
b. Describe what gives rise to the change from Ohmic to saturated behaviour for a MOSFET. **(3)**

c. Show that the small-signal resistance of a MOSFET transmission gate is approximately as shown in Equation 2, for the case where the input and output voltages of the transmission gate are between V_T and V_{DD}-V_T.

$$r = \frac{1}{\beta(V_{DD} - 2V_T)} \qquad (2)$$

All the terms have their usual meaning and $\beta=\beta_P=\beta_N$ and $V_T=V_{TN}=-V_{TP}$. **(10)**

2.



You are given an incomplete logic circuit, shown in **Figure 2** where the output Y is a function of four inputs: A, B, C, and D. You are told that to complete the circuit you need only to add transistors to the circuit without changing the way in which the existing transistors are connected. From this, you recognise that there are two possible ways in which the circuit could be completed.

i. How do you know that the circuit is incomplete? **(2)**

ii. Draw the two possible circuits that might represent the competed circuit. **(8)**

iii. Write down the logical functions of the two possible circuits. **(4)**

iv. For any *one* of the completed circuits, size the transistors assuming that you want a minimum-sized gate (assume that the mobility of holes is half that of electrons). **(4)**

v. The substrate connections are not shown in **Figure 2**. Where would the substrates be connected for the *n*- and *p*-type MOSFETs? **(2)**

Figure 2:
Incomplete Logic Circuit

3. **a.** Draw a flow diagram to represent a basic ASIC design flow, identifying the activity within each part of the design process. **(10)**

b. What are the major differences between Cell-Based ICs, Structured ASICS, Masked Gate Arrays, and Field-Programmable Gate Arrays? How might you decide which technology to use in a particular design project? **(5)**

c. You work for a fabless IC company, and your company has to develop a single IC solution for a mass-market, mobile product that will encompass a PDA, media player, and personal communications (e.g. WiFi, bluetooth and GSM). Identify the factors that will influence the choice of technology and the fabricator of the IC. **(5)**

4. **a.** **i.** Describe the *Synchronous Design Methodology* and explain why it results in reliable designs. **(4)**

ii. How does synchronous design relate to *Register Transfer Level* descriptions of circuits? **(2)**

b. What are the sources of variability in the performance/behaviour of an IC? **(3)**

c. How is the distribution of clock signals managed in a synchronous IC to ensure that the IC is clocked *synchronously*? **(3)**

d. **i.** What particular problems exist for designers as a consequence of there being more than one *clock domain* in an IC? **(2)**

ii. Is it important that designers should be able to design an IC with multiple *clock domains*? If so, why? **(2)**

iii. How do you make the transfer of signals between clock domains reliable? **(4)**

NLS / MB