The University Of Sheffield.

Data Provided:

Boltzmann constant (k_B) = 1.38×10^{-23} m^2 kg s^{-2} K^{-1}

Electronic charge (e) = 1.602×10^{-19} C

Permeability of free space (μ_o) = 1.256×10^{-6} m kg s^{-2} A^{-2}

Thermal conductivity (k):

k_{epoxy} = 1.4 W m^{-1} K^{-1}, $k_{alumina}$ = 30 W m^{-1} K^{-1}, $k_{aluminium}$ = 216 W m^{-1} K^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2009-2010 (2 hours)

Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** The incorporation of more than one integrated circuit (IC) inside a single package is now becoming commonplace. One production method for system in package (SiP) involves the vertical stacking of silicon wafers and the use of through-silicon vias (TSV) for vertical interconnections. Discuss the new technical challenges that have arisen as a result of the adoption of this technology and how they are being solved. **(8)**

b. The high pin count of a typical system in package (SiP) means that it is normally attached to the printed circuit board using a ball grid array (BGA). Describe how the array of solder balls is formed and how the BGA package it is attached to the substrate. **(4)**

c. The yield for the fabrication of 200 identical flash memory ICs on a single wafer is 99% and the yield for interconnecting one wafer to another using TSV is 98%. What would be the yield for a vertical stack of 5 wafers? **(4)**

d. A miniature camera module consists of a CMOS image sensor IC mounted on top of a controller IC which is in turn mounted on a signal redistribution substrate. Interlayer connections between all layers are made with TSVs. The wafer level yield for the manufacture of the image sensor is very low (80 %) compared to the other manufacturing steps. Suggest ways in which the yield of the finished module could be kept high. **(4)**

2. **a.** A total of 5 W needs to be dissipated into a heat sink from a 20x20 mm quad flat pack (QFP) surface mount package containing a silicon integrated circuit. The junction-to-case thermal resistance of the package R_{jc} = 8 °C/W. What thermal resistance should the heat sink have in order to maintain the silicon at a safe working temperature? State the assumptions that you have made. **(5)**

b. A revision to the IC is packaged in the same QFP described above, however it must be operated at 110 °C or below, inside an enclose with an air temperature of 40 °C. It is decided that a finned heat sink plus a fan need to be mounted on top of the IC in order to ensure safe operation. Using the graph in Figure 2, determine the minimum volume flow rate (m^3/hour) that the fan must deliver.

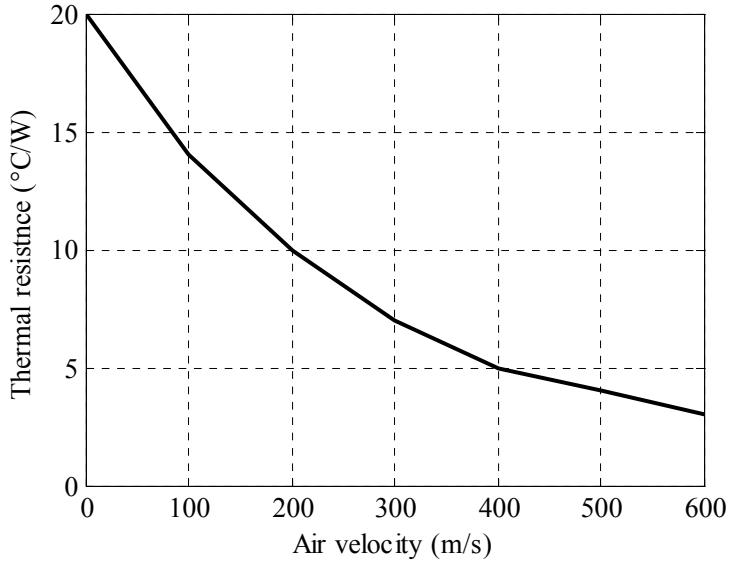

Figure 2 Performance of heat sink plus fan **(5)**

c. Why would it not be a good idea to use solder to attach the heat sink? **(2)**

d. The QFP package contains a microprocessor that needs to be connected to a separate co-processor with a high speed 64-bit bus. Discuss the possible arrangement of a multi-layer glass fibre/epoxy printed circuit board (PCB) that would allow this. **(5)**

e. What new technology is proposed to further increase inter-chip communication speed on PCBs? **(3)**

3. **a.** Describe what is meant by the terms 'system-on-a-chip' (SoC) and 'system-in-a-package' (SiP)? Describe the relative advantages and disadvantages of both approaches. **(5)**

b. A digital IC has a size 1×1 cm. It has 1.5M logic gates. Assuming Rent's rule applies, with a coefficient of 0.25 and an exponent of 0.5, calculate the number of I/O terminals. **(2)**

c. The above IC is considered for either a dual in-line package (DIP) or a quad flat package (QFP). Calculate the minimum pin to pin separation using these approaches. The wire bonding tool can accept bond pad sizes down to 100um. Why would one of these approaches be unsatisfactory? **(2)**

d. Describe suitable schemes for the packaging of semiconductor lasers when these lasers are: **(4)**

(i) a fibre-coupled edge emitting laser for telecoms transmission, and

(ii) a vertical cavity surface emitting laser array for a low cost datacoms application.

e. A laser chip has dimensions 1×1 mm^2 and dissipates 850 mW. It must operate at 20°C. The device is indium-bonded to an alumina tile of size 25x25 mm and thickness 2 mm, with minimum thermal resistance in the bond. Assuming radial heat spreading and making the necessary approximations, estimate the thermal resistance of the tile and the temperature of the far surface of the tile.

Describe a typical temperature regulated cooling scheme which would be used to achieve this. **(3)**

f. A company wishes to launch a new packaged IC which needs to demonstrate 50,000 hours of reliable operation at 20°C ambient temperature. However, only 5,000 hours are available until the launch date. From experience, the company knows that the primary failure mechanism is a thermally activated process with activation energy of 0.2 eV. At what temperature should accelerated testing be performed? **(4)**

4. a. Describe the three principal methods used to make electrical connection to ICs and discuss their relative advantages and disadvantages. **(5)**

b. A typical package has wire bonds of length 5 mm and separation 1.8 mm. Calculate the mutual inductance of the leads assuming the conductors are in parallel

Mutual inductance $M = \frac{\mu_0 l}{2\pi}\left[\frac{l}{d} + \sqrt{1+\left(\frac{l}{d}\right)^2} - \sqrt{1+\left(\frac{d}{l}\right)^2} + \left(\frac{d}{l}\right)\right]$

Where, L = length of the conductors, d = separation of the conductors

The package has additional parasitic inductances of 1.2 nH from the bond pad and 3.5 nH from the package lead. The resistance of the lead out is measured as 550 mΩ. What is the cut-off frequency of the device? **(5)**

c. A 1 cm^2 processor die dissipates 18 W. The die is epoxy bonded onto a 1 mm thick alumina substrate, which itself is bonded to a 10 mm thick aluminium heat sink. Both the substrate and the heat sink are the same area as the die. The far surface of the heat sink reaches 65°C in normal operation.

What is the maximum temperature of the processor die? Assume the epoxy is coated to a thickness of 100 μm. **(4)**

d. Draw a graph of the average failure rate versus time curve for a typical packaged semiconductor device. Explain the origin of the different regions. **(3)**

e. An accelerometer, or g-sensor, is a low cost MEMS IC found in a car airbag system. List the four principles of packaging in consideration of this device and its environment. By considering these factors, suggest a suitable package for this device **(3)**

GLW / MH