EEE105 - Electronic Devices
Lecture 17

Junction Field Effect Transistor Transfer Characteristic

In the last lecture we saw how a JFET could be used as an amplifier. In the region of the drain characteristic that is useful for this application, the drain voltage must be

than the pinch-off voltage. In this region the drain current flowing through the transistor (and our amplifier output circuit) will be controlled exclusively by the

In this situation we can plot the so-called ***transfer characteristic*** of the device where the output current of the amplifier, I_d, is plotted against the input voltage, $-V_g$.

Now the key aspect of the transistor is that small signal changes in v_{in} should give large changes in the output current, I_d.

A measure of the transistor amplification can be given by the ***transconductance,*** g_m, where: $g_m = \left.\frac{dI_d}{dV_g}\right|_{V_g}$

Note that the vertical bar on the right of this equation means "at some point".

In this case it means the slope of the transfer characteristic curve, *at some particular value of* gate bias, V_g. For an ***ideal*** JFET, the transistor transfer characteristic would be a straight line, and the transconductance would hence be a constant value as the gate voltage changed. However, in real devices this is not easy to obtain.

The units for measuring transconductance are SIEMENS, S. (=)

Hence we can write the equation: $i_d = g_m v_{gs}$

Note that if the transfer characteristic is not a perfectly straight line then the shape of the waveform of the output signal current, i_d, will not be exactly the same as the input voltage signal, v_{in} and there will be some (hopefully small) distortion of the output from our simple amplifier.

Reminder: We normally write signal voltages and currents with small, rather than capital letters, as was done for v_{in} above. More formally we can say that our transistor amplifier will amplify a small input signal, v_{gs}, to give a large output signal, i_d

Junction Field Effect Transistor Small Signal Equivalent Circuit

(CAL: Jfet(e))

In the equivalent circuit we can look at how the transistor can be represented in its electrical behaviour for the small a.c. signals that are to be amplified.

The most fundamental part is that a small signal voltage between the source and gate, v_{gs}, gives an output current. We can therefore represent the output as a current source giving a current out equal to $g_m v_{gs}$.

Now in the transistor we also have a number of potential resistances:

Clearly there is the possibility of there being some leakage current between the gate and the source and drain.

These resistances can be characterised by r_{gs} and r_{dg}. Note that as the gate is reverse biased with respect to both the source and drain we expect both these resistances to be high, typically many Mega-ohms (MΩ).

The output resistance r_{ds} requires a little more explanation. This can be done by looking again at the drain characteristic. Up until now we have said that in the amplifier region, the drain current is constant with drain voltage. In reality there is often a small increase in the drain current as the drain voltage increases. The slope of this line is the reciprocal of the output resistance.

That is: $r_{ds} = \left.\frac{dV_d}{dI_d}\right|_{V_g(,V_d)}$ on the graph $r_{ds} =$

Usually the output resistance is high, typically in the range of 100s kΩ to one or two MΩ.

In a many cases we can simplify the equivalent circuit by ignoring the input resistances to give:

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

(CAL: MOS1, MOS2)

These devices can also be known by other names:

Metal Insulator Semiconductor Field Effect Transistor:

Insulated Gate Field Effect Transistor:

These devices are very important as they are used extensively in very large scale integrated circuits (VLSI) due to their ease of fabrication.

In the devices a (thin) oxide layer is formed between the gate and the channel. This can be very easily done in silicon by controllably oxidising the surface to form SiO_2. (Silicon dioxide is a very good insulator.)

The device is shown schematically here. It is formed by starting in this case with a piece of p-type Silicon. Two regions that are heavily doped n-type are then created. The oxide is then formed and finally the metal regions deposited. The source and drain contacts conduct easily, but clearly the oxide between the gate metal and the semiconductor prevents current flow through this contact.

In order to examine what happens in this device we need to concentrate on the effect of the gate contact on the device.

When no voltage is applied to the gate then no current can flow from source to drain as in effect we have two back-to-back p-n junction diodes.

Let us now consider the situation when we apply a positive gate bias to the device. The holes in the p-type material under the gate will see the positive charge on the gate and be

Thus the p-region under the gate will become gradually depleted of holes. In this situation the positive charge on the gate will be balanced by

As the gate voltage increases, then in addition to the above, electrons from the n^+ regions flow out along the surface of the semiconductor to help balance out the positive charge on the gate. This will form a thin, n-type conducting channel between the source and drain.

It the diagram the n-type conducting channel is thinner at the drain end than the source end. This triangular shape is caused by the effect of the positive bias on the drain terminal.

This means that the bias creating the channel is less at the drain end (as the gate-drain potential difference is smaller than the gate-source potential difference.)

For a constant applied gate voltage, V_g, then as the drain voltage, V_d, increases so the channel width at the drain end will become progressively narrower. Eventually the channel at the drain end will "pinch-off", in the same manner as described for the JFET, and the drain current will saturate at a particular value determined by the gate voltage.

Thus we end up with a family of curves very similar to those for the JFET, except that in this case the drain current increases as the magnitude of the gate voltage increases.

Note that for this device to operate we need to exceed some minimum gate voltage to induce a channel between the source and drain. This voltage is called the ***threshold voltage,*** V_T.

This device is called an "***ENHANCEMENT MODE"*** MOSFET as applying a gate voltage ENHANCES CONDUCTION from a "normally off" state.

The circuit symbol for the enhancement mode MOSFET is:

Key Points to Remember:

1. Plotting the drain current against gate voltage gives the transfer characteristic of a JFET.
2. The transconductance is a figure of merit for the field effect transistor. It is a measure of how much the output current can rise as the input signal voltage is increased.
3. The transistor can be represented as a current source for a small a.c. input signal, with both input and output resistances.
4. The Enhancement mode MOSFET consists of a p-type region with n^+ regions for the source and drain. The p-type region is insulated from the gate using an oxide.
5. Applying positive bias to the gate repels the holes from the p-type material and eventually drags in electrons from the n^+ regions to form an n-type channel.
6. The channel can be pinched off at the drain end in a similar way to that outlined for the JFET.