Examination Feedback for EEE6393 Microsystems Packaging
Spring Semester 2011-12

Feedback for EEE6393 Session: 2011-2012

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

Students generally answered 2 questions from the 'components' section, with Q1, 2 and 3 being a popular choice. Performance was good overall, but with some poor scores. Occasional evidence of a lack of time or missing parts of questions.

Question 1:

Most answered part a) very well, but a few failed to distinguish between the two. Part b) was answered well, but there were some errors in the calculation. Some rough diagrams and lack of detail cost a few marks in part c). Most knew what 'accelerated testing was, but few were able to do the calculation well.

Question 2:

Some generally good answers to a), but quite a few lacking in any real detail. In b) only a few could say why the power dissipation has not scaled (this is related to the operating voltage which is itself related to the MOSFET threshold- it has been difficult to scale this down as much as expected. Most did the Rents rule calculation OK. Most had a reasonable packaging scheme. Most did OK on the heat transfer, but there were quite a few errors in the calculation and a few very strange answers. Very few were able to get part d) right, although it's a relatively easy calculation. A few forgot that its asks for the heat loss, Q, and not the temperature change.

Question 3:

a) Lots of students did not even attempt to draw sketch of heat sink/fan assembly. Most failed to mention TCE as reason for copper over aluminium.
b) Generally done, well, though some students failed to use correct *area* when calculating flow rate.
c) Generally done well, though most students failed to mention the thermal resistance of the heat sink/package interface.
d) All students failed to note that fan delivers constant *volume* flow rate, hence at lower density (high altitude) the *mass* flow rate will be lower and hence thermal resistance will increase.
e) Lots of reasons given for having a 4-layer PCB, but the question asked specifically about the P4 *redistribution* PCB. In this case, the main reason for 4 layers is to cope with high density of connections from the P4. The book work section on PCB construction was done surprisingly badly.

Question 4:

Not a popular question. Though it was correctly laid out, I wonder if students missed it because it was overleaf on the last page?
a) Despite being book work, few students were able to correctly describe SAC305 solder and solder paste. Most students had a fair idea of a eutectic composition.
b) Most students were able to draw the correct qualitative graph and annotate the 4 stages. Many forgot to mention flux activation.
c) Most students assumed reasonable values for Z_0 and t, though the manipulation of the equation let some down. All students failed to spot that ε_{eff} for microstrip depends on both the dielectric and air.
d) Generally done well by those that attempted it.