DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (2.0 hours)

Answers to EEE335 Integrated Electronics, Question 1..2

1. ***Figure 1*** *shows the schematic for a digital circuit.*

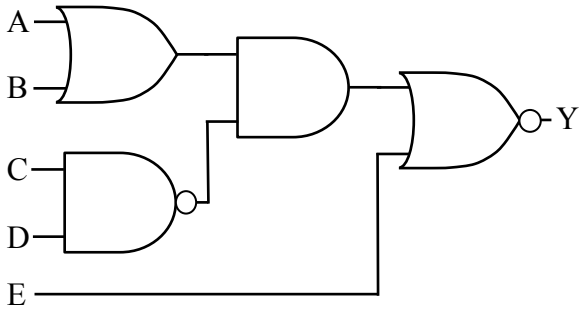


Figure 1: Digital Circuit

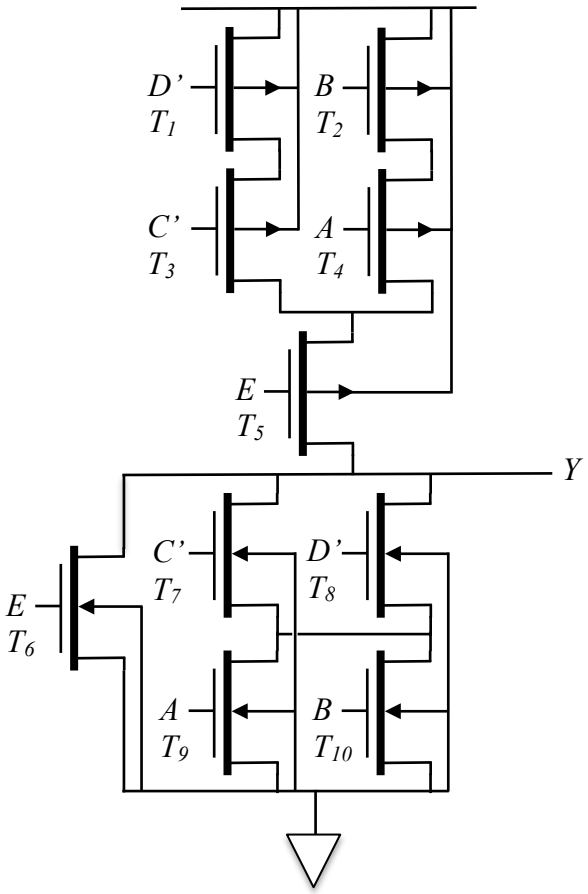
a. *Derive the logic function of the circuit in* ***Figure 1****.*

$$Y = \overline{E + \overline{C.D}.(A+B)} = (\bar{A}.\bar{B} + C.D).\bar{E}$$ **(2)**

b. *Draw the transistor-level schematic diagram for a CMOS circuit that would implement the function in* ***Figure 1****. There may be more than one way to implement this function: justify the way in which you have implemented the circuit.*

C' is not *C*

D' is not *D*



(6)

c. *Size the transistors in the circuit that you have drawn, assuming that the gate is minimum-sized (using the normal definition for this).*

$T_1 = T_2 = T_3 = T_4 = 8$ (if $T_5 = 4$) or 6 (if $T_5 = 6$)

$T_6 = 1$, $T_7 = T_8 = T_9 = T_{10} = 2$

For the transistors in the inverter for *C*, p-type (T_{11}) = 2, n-type (T_{12}) = 1.

For the transistors in the inverter for *D*, p-type (T_{13}) = 2, n-type (T_{14}) = 1.

The assumption is that $0.5\mu_E = \mu_H$ **(4)**

d. *Assuming that the gate capacitance associated with a minimum-sized n-type FET is 0.5fF, estimate the capacitance associated with each of the connections (wires connecting inputs and output, and any intermediate wires between separate sub-circuits) in your transistor-level circuit.*

$A = C_G(2+6) = 4$fF, $B = C_G(2+6) = 4$fF

$C = C_G(2+1) = 1.5$fF, $D = C_G(2+1) = 1.5$fF

$E = C_G(1+6) = 3.5$fF, $C' = C_G((2+1)/2+6+2) = 4.75$fF

$D' = C_G((2+1)/2+6+2) = 4.75$fF **(2)**

e. *Rather than implement the circuit in Figure 1 as a specific circuit, you decide to implement each of the individual logic gates separately as CMOS circuits. What would be the important differences between the implementation of the circuit as a whole and as separate, individual parts.*

A basic two input, minimum sizes inverting logic gate is made up from 4 transistors, and the size of the transistors for each of the gates would be (relative to minimum width):

NOR: 2 pull-up pFET 4x minimum width, 2 pull-down nFET 1x minimum width

NAND: 2 pull-up pFET 2x minimum width, 2 pull-down nFET 2x minimum width

Each inverter for the non-inverting gates adds: 1 pull-up pFET 2x minimum width, 1 pull-down nFET 1x minimum width

Consequently, composed of individual parts, the circuit consists of 20 individual FETs:

Pull-up: 2, 4x; 1, 2x; 2, 2x; 1, 2x; 2, 4x; 2, 2x; 1, 2x= 30 minimum width FETs

Pull-down: 2, 1x; 1, 1x; 2, 2x; 1, 1x; 2, 1x; 2, 2x; 1, 1x= 15 minimum width FETs

In total, the area is equivalent to 15 minimum sized FETs.

For the composite circuit above, there are 14 FETs, however, the equivalent number of minimum sized FETs is identical = 45.

However, in terms of delay, a signal propagating from A to Y has to pass through a chain of 3 inverting gates and 2 inverters to reach the output in the circuit made up from individual gates. In the composite circuit, a signal from C to Y has to pass through 1 similar strength gate and 1 inverter. Consequently, the composite circuit is likely to be considerably faster. **(6)**

2. a. *A pass transistor is incorporated in a circuit as shown in Figure 2.*

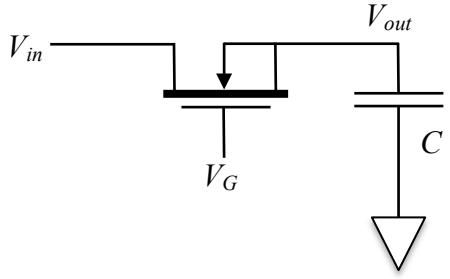


Figure 2: Pass Transistor Circuit

Initially (and for some time), V_{in}=0V, V_G=V_{DD} (a voltage which is above the threshold voltage, V_T, of the transistor). You may assume that the gain of the transistor is K_N.

i). *At time, t=0, the input V_{in} is changed to V_{DD}. Verify that the response of V_{out} as a function of t in the period $t \geq 0$ is:*

$$V_{out}(t) = (V_{DD} - V_T) - \frac{(V_{DD} - V_T)}{1 + \frac{K_N (V_{DD} - V_T) t}{2C}}$$

When V_{in} is increased to V_{DD} at t=0, V_D=V_G and so V_{GS} = V_{DS}. Consequently, the transistor is saturated and so

$$I_{DS} = \frac{K_N}{2}(V_{GS} - V_T)^2 = \frac{K_N}{2}(V_{DD} - V_{out} - V_T)^2 = C\frac{dV_{out}}{dt}$$

$$\frac{K_N}{2C}\int dt = \int \frac{dV_{out}}{(V_{DD} - V_{out} - V_T)^2} + A$$

$$\frac{K_N}{2C}t = \frac{1}{(V_{DD} - V_{out} - V_T)} + A$$

When t=0, V_{out} = 0. Consequently,

$$A = -\frac{1}{(V_{DD} - V_T)}$$

$$\frac{K_N}{2C}t = \frac{1}{(V_{DD} - V_{out} - V_T)} - \frac{1}{(V_{DD} - V_T)}$$

Rearranging:

$$\frac{K_N}{2C}t + \frac{1}{(V_{DD} - V_T)} = \frac{1}{(V_{DD} - V_{out} - V_T)}$$

$$(V_{DD} - V_{out} - V_T) = \frac{1}{\frac{1}{(V_{DD} - V_T)} + \frac{K_N}{2C}t}$$

$$V_{out} = (V_{DD} - V_T) - \frac{1}{\frac{1}{(V_{DD} - V_T)} + \frac{K_N}{2C}t}$$

$$V_{out} = (V_{DD} - V_T) - \frac{1}{1 + \frac{K_N (V_{DD} - V_T)}{2C}t}$$

(4)

ii). *Identify the value of voltage to which V_{out} becomes asymptotic. Explain why this is the case.*

As $t \rightarrow \infty$, $V_{out} \rightarrow V_{DD} - V_T$

At this point, $V_{GS} = V_T$. At this point the transistor is just on the point of switching off. If the transistor is perfect then there is no current flowing and, therefore, the capacitor cannot charge anymore and the voltage remains at $V_{DD} - V_T$.

(2)

b. *With the capacitor, C, disconnected, what is the small signal impedance of the point labelled V_{out} to ground when:*

i). $V_{in}=0$

When $V_{in} = 0$,

$$I_{DS} = -\frac{K_N}{2}(V_{DD} - V_{out} - V_T)^2$$

where we now define I_{DS} as going into the source of the transistor

$$\frac{dI_{DS}}{dV_{out}} = -\frac{K_N}{2}(V_{DD} - V_{out} - V_T)(-1) = \frac{K_N}{2}(V_{DD} - V_{out} - V_T)$$

$$r = \frac{dV_{out}}{dI_{DS}} = \frac{2}{K_N(V_{DD} - V_{out} - V_T)}$$

When V_{out} is close to 0 then $r = \frac{2}{K_N(V_{DD} - V_T)}$

ii). $V_{in}=V_{DD}$

Again $r = \frac{dV_{out}}{dI_{DS}} = \frac{2}{K_N(V_{DD} - V_{out} - V_T)}$

(3)

However, as the capacitor charges up, V_{out} changes and the value of r increases until V_{out} reaches its limiting value of V_{DD}-V_T. When this point is reached then $r=\infty$.

Comment on the use of the transistor as an electronic switch in this circuit.

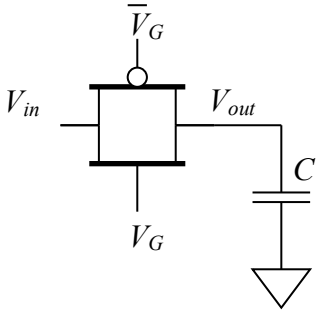
(3)

As long as V_{in} is low then the switch (whose state is controlled by V_G) is relatively low when switched on and the difference between input and output voltage is small. However, when the input voltage is high, the output impedance is high and there is a difference between input and output voltage is non-zero. Consequently, the switch is quite poor.

(2)

c. *If you were to make a good electronic switch for use in a digital circuit, identify how this might be done. You do not need to do a detailed analysis of the switch's performance but you do need to relate the behaviour of the electronic switch to the behaviour of a perfect switch.*

An *n*-channel FET used as a switch will pass a low voltage but is poor when passing a high voltage. Conversely, a *p*-channel FET will pass a high voltage well and act as a good switch but will, conversely, be poor when passing a low voltage. Consequently, by marrying the two types of switch together, a good switch can be formed.



When analysed the on-state resistance of the switch can be found to be $r = \dfrac{2}{K\left(V_{DD} - 2V_T\right)}$ for a range of voltages more than V_T away from either supply.

(6)

NLS/AM / TWANG

EEE 335

2014/2015 exam answers (Q3 & Q4).

(3)

a i.

$$I_D = \frac{k_n}{2}\frac{W}{L}V_{ov}^2$$

$$\therefore V_{ov} = \sqrt{\frac{2I_DL}{k_nW}} = \sqrt{\frac{2.100.0.4}{150.2}} = 0.52V$$

$$V_{gs} = V_{ov} + V_{TO} = 1.12V.$$

ii.

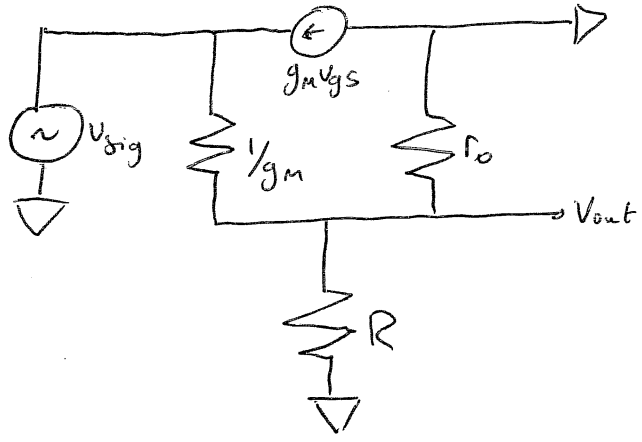
Channel length doubled = <u>half</u> drain current

V_{ov} doubled = 4x drain current

For triode operation $V_{DS} < V_{ov}$. Doubling V_{ov} could lead to this condition being satisfied.

b.

i.



$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05.150\mu A} = 133k\Omega$$

$$V_{ov} = \sqrt{\frac{2I_DL}{k_nW}} = \sqrt{\frac{2.150.0.6}{200.6}} = 0.39V.$$

$$\therefore g_m = 200\times10^{-6}.\frac{6}{0.6}.0.39 = 0.77mS.$$

ii. Since R=10kΩ and the bias current given is 150μA, the source of M1 sits at 0.15.10 = 1.5V. Since V_{ov} = 0.39V a suitable value for V_{bias} is $1.5 + V_{ov} + V_{TO} = 1.5 + 0.39 + 0.5 = 2.39V.$

(3) b iii.

From the small signal model, r_o is in parallel with R, so that the output voltage can be computed as a potential divider between $1/g_m$ and $r_o \| R$:

$$V_{out} = \frac{R \| r_o}{R \| r_o + 1/g_m} \cdot V_{sig}$$

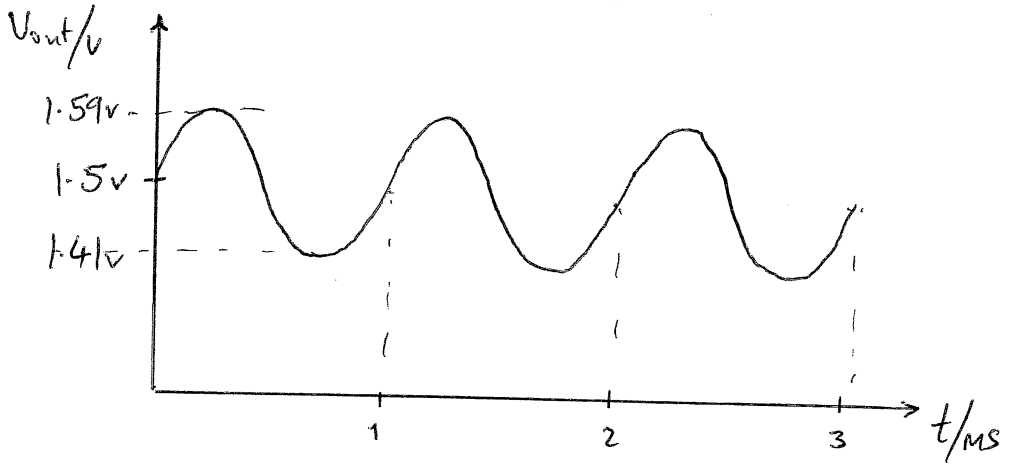
$$\therefore A_v = \frac{V_{out}}{V_{sig}} = \frac{g_m (R \| r_o)}{1 + g_m (R \| r_o)}$$

$$\simeq \frac{g_m R}{1 + g_m R}.$$

for $R = 10k\Omega$, the gain is

$$\frac{0.77mS \cdot 10k\Omega}{1 + 0.77mS \cdot 10k\Omega} = 0.89 V/V$$

iv.



(4.)

a.

Current steering:

An IC amplifier generally requires several biasing currents of different values, each biasing an individual stage of amplification. Current steering is the process of deriving these biases from a single reference current source via a parallel set of current mirrors with appropriate channel aspect ratios.

Transconductance:

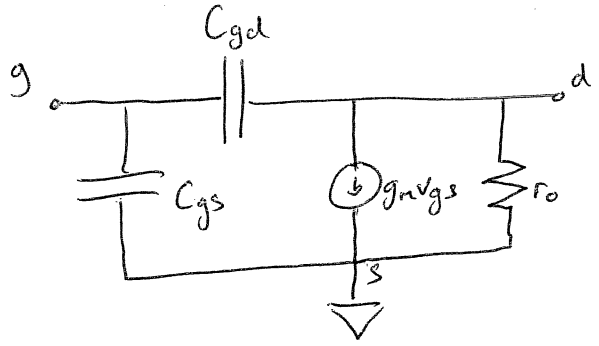
A transistor takes an input voltage (e.g v_{gs} for an FET) and converts this into an output (drain) current. The transconductance parameter indicates the amount by which this output current changes for a small change in the input voltage. i.e. a $1mV$ change in v_{gs} results in a $1mV \times g_m$ change in i_d.

Channel length Modulation:

The current through an FET increases with the drain-source voltage until the 'pinch off' point, when $V_{DS} = V_{ov}$ and the channel height is zero at the drain end. As $|V_{DS}|$ increases beyond this point, the channel gradually recedes towards the source, resulting in an approx. linear increase in I_D. This effect is called Channel length modulation.

(4)

b i.



ii.

$V_{gs} = 1V$, $V_{TO} = 0.4V \Rightarrow V_{ov} = 0.6V$.

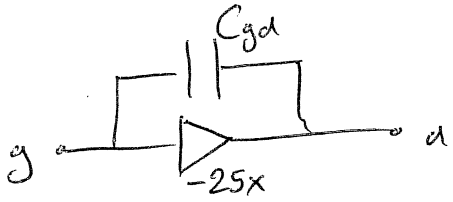
$$\therefore I_D = \frac{k_n}{2}\frac{W}{L}V_{ov}^2 = 94.5\mu A$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.1 \cdot 94.5\mu A} = 106k\Omega$$

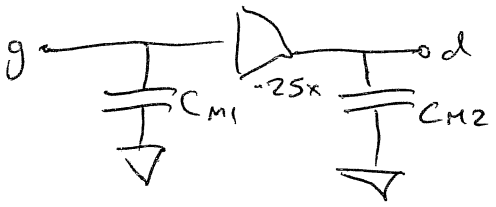
$$g_M = k_n \frac{W}{L} V_{ov} = 0.32mS.$$

iii.

We have this situation:



Using the Miller transform this becomes:



Where $C_{M1} = (1-k)C_{gd} = 26 \times 2pF = 52pF$

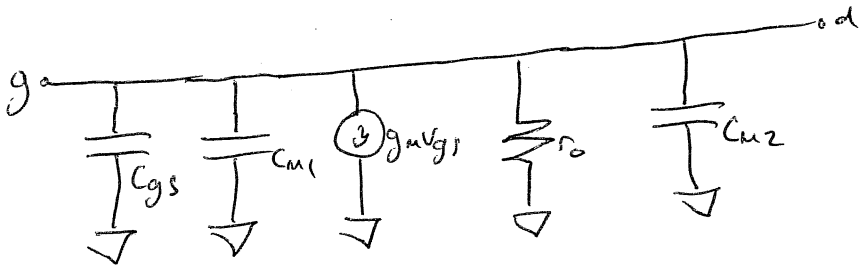
$$C_{M1} = \left(1-\frac{1}{k}\right)C_{gd} = 1.04 \times 2pF = 2.08pF.$$

(4)

b

iii. contd...

The modified small signal model is:



C.

i. $I_D = 150\mu A = \frac{k_p}{2}\frac{W}{L}V_{ov}^2$

$$\therefore V_{ov} = \sqrt{\frac{I_D \cdot 2 \cdot L}{k_p \cdot W}} = 0.61V$$

$$\therefore |V_{gs}|_{M1} = V_{ov} + V_{TO} = 1.11V.$$

The voltage across R is then $5 - 1.11 = 3.89V$, since $V_{DS} = V_{gs}$ for M1.

$$\Rightarrow R = \frac{V}{I} = \frac{3.89}{150\mu A} = 26.5k\Omega.$$

ii. $V_{DS(M2)}$ reduces by 0.5V. Since the output resistance of M2 is $\frac{1}{2I_D} = \frac{1}{0.04 \times 150\mu A} = 167k\Omega$, the change in output current is $\simeq \frac{-0.5}{167k\Omega} = -3\mu A$.

– This error is minimised in more advanced current mirrors by their much higher output impedance (usually at the expense of voltage headroom).