1a) Simultaneous switching noise

Transients in the power drawn by various parts of the circuit (eg: MOSFETs switching) causes a transient in the power supply line (or in the ground line). This then effects the operation of other parts of the circuit

Needs low impedence source and ground interconnects (short leads, multiple power and ground leads. Can be reduced by the introduction of decoupling capacitors to compensate for the parasitic inductance of the supply + ground lea

Cross-Talk

Signal on one line induces a signal on another line due to electromagnetic coupling. Usual problem is the mutual inductance between two lines/pin-outs This is a function of the overall length of the lines & their cross sectional area and of their separation. So one needs to minimise the lead length ~~and~~ use as wide a possible separation and use as large as possible area. May also use well separated pin-outs on the package for important signals (rather than adjacent ones)

1b)

QFP $\quad l/d = 7.14 \qquad d/l = 0.14$

BGA $\quad = 1.62 \quad = \quad 0.6$

QFP

$$\ln\left(7.14 + \sqrt{1 + (7.14)^2} - \sqrt{1 + (0.14)^2} + 0.14\right)$$

$$\ln(7.14 + \sqrt{51.9} - \sqrt{1.02} + 0.14)$$

$$\ln(13)$$

$$M = \frac{\mu_0 l}{2\pi}(\quad)$$

$$7.034\times10^{-12} \times \ln 13 = 1.80\times10^{-11}\ \text{H}$$

18pH

~~44.5~~ 1.8nH.

BGA

$$\ln(1.62 + \sqrt{1 + (1.62)^2} - \sqrt{1 + 0.6^2} + 0.6)$$

$$\ln(1.62 + \sqrt{3.79} - \sqrt{1.36} + 0.6)$$

$$\ln(3.05)$$

$$m = 2.816\times10^{-12} \ln(3) = 3.09\times10^{-12}\text{H}$$

QFP = ~~44.5~~ 36nS 44.5MHz 3pH

BGH 1.4nS 111MHz 0.288nH

Time constant $= L/R$

QFP $= \dfrac{18\times10^{-11}}{\Omega\cdot S} = \dfrac{2.78\times10^{-10}\ S}{36\text{p sec}}$ $f_{3\text{dB}} = 1/36\times10^{-12}$

1c) From notes, with a diagram expected

Important elements are

The overall package - typically the butterfly type

The use of a TE cooler - needs a thermistor on the package

The fiber held by a ferrule and glued/welded at final allignment.

The use of a monitoring photodiode.

The use of wire banding (often multiple bonds)

Final alignment

Output of the fiber is monitored whilst the laser is operated and the fiber input face is moved on an x-y-z stage until the output is peaked. Once positioned the fiber holder is glued or welded into place.

1d) Accelerated testing

Testing under more extreme conditions than normal in order to induce accelerated failure. From this we can estimate the failure rate under normal conditions (assuming we know the dependence)

Done because testing components for 10^4–10^6 hours is impracticable before product launch.

Stresses: Temperature, Voltage, Current, Temp cycling, humidity, mechanical.

$$R = R_0 e^{-E_a/k_B T} \qquad \text{time} = R^{-1}$$

↗ rate

$$\frac{t_1}{t_2} = \frac{R_2}{R_1} = e^{\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$\ln\left(\frac{t_1}{t_2}\right) = \frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

$T_2 = 100°C = 373K$ $\quad \frac{1}{T_2} = 2.681 \times 10^{-3}$

$T_1 = 25°C = 298K$ $\quad \frac{1}{T_1} = 3.356 \times 10^{-3}$

$E_a = 0.3eV$ $\quad \frac{E_a}{K_B} = \frac{0.3 \times 1.6 \times 10^{-19}}{1.38 \times 10^{-23}} = \frac{3478}{6956}$

$$\frac{1}{T_1} = \frac{\ln\left(\frac{t_1}{t_2}\right)}{(E_a/k_B)} + \frac{1}{T_2}$$

$$\ln\left(\frac{t_1}{t_2}\right) = 6956\left(3.356 - 2.681\right) \times 10^{-3}$$

$$= 4696$$

$$t_1/t_2 = e^{4696} = 109.6$$

$$t_2 = 25^\circ C$$

$$t_2 = 900 \quad t_1 = 9.8 \times 10^4$$

2a

SoC - Integration of all (or most) discrete IC's onto a single silicon die

S.P - Retain individual silicon die and package together on a single substrate with interconnects.

SoC advantages

Dense packaging/routing - short interconnects - low parasitics compared to the other approaches (esp. individual ICs). Better for high speed. Good for low noise since there are no internal off-die interconnects

Reduction in PCB complexity - simplifies the assembly of the electronic system

Improved architecture - not now designing individual ICs to have external interconnects - frees up real estate and allows greater packing densities leading to smaller and more efficient / more complex systems. + economies of scale

Disadvantages

compared to S.P

Expensive design exercise and new tooling whereas SiP uses individual ICs which already exist. May not be cost effective

Difficult to integrate diverse technologies eg: CMOS, Bipolar, RF, MEMS. SiP retains individual ICs so no fundamental issues.

Difficult to isolate different functions - crosstalk as SSN due to other signals

2b) We discuss the power dissipated in CMOS switching in the lectures. This will scale according to the frequency and the no. of transistors. If it did this the power dissipated would be 320 kW!!

There has been a ~~bit~~ reduction in the supply voltage to compensate for this. This comes from a progressive reduction in the MOSFET threshold voltage. Latest processors are using $V_s \approx 0.8$-0.9V rather than ≥ 5V. Capacitance has also been reduced, as has the switching factor (through systems design)

Rents rule

$$T = q\,G^{p}$$

(T: Terminals; G: Gates)

A (Pentium) 3 1E6 transistors → 5×10^5 Gates

B (Core i7) $\sim 2.2\times10^9$ transistors → 3.3×10^8 gates

A) $T = 9\times190$ $\quad T = 95$

B) $T = 9\times266$ $\quad T = 1333$

For device A, 95 terminals could possibly be done using a Quad surface mount package – eg: QFP, however 95 terminals is a bit too much – thus did use a Pin grid array

Still is probably too much to use a plastic package ceramic

For IC(B) 1333 terminals dictates the use of a full sized Ball grid or Pin grid array (actually uses a PGA. Package is ceramic - with metal layers in a composite.

2D)

Heat transfer

$R_{TH} = L/KA \qquad \Delta T = \Phi R_{TH} = \frac{QL}{KA}$.

		A	B
R_{TH} Alumina	$= \frac{5\times10^{-3}}{30A}$	162	3.33×10^{-1}
R_{TH} Aluminium	$= \frac{10\times10^{-3}}{216A}$	4.63×10^{-1}	9.3×10^{-2}
R_{TH} Epoxy	$= \frac{100\times10^{-6}}{0.5A}$	2	4×10^{-1}

$R_{TOTAL} = R_{TH\,Alumina} + R_{TH\,Aluminium} + 2\times R_{TH\,Epoxy}$

Totals

$A \Rightarrow 6.13$

$B \Rightarrow 1.222$.

$Q_{pentium} = 8W$ $\Delta T = 8 \cdot 6.13 = 49°C$

$Q_{core\ i7} = 130W$ $\Delta T = 130 \cdot 1.227 = 150°C$

$85 - 49 = 36°C$ Reasonable

$85 - 150°C = -65°C$ Unreasonable.
-74

'New' Epoxy.

$R_{TH\ New} = \frac{100 \times 10^{-6}}{8A}$

	Pentium	Core i7
R_{TH}	1.25×10^{-3}	2.5×10^{-4}
R_{TOTAL}	2.13	0.43
ΔT	17	56
T	$68°C$ / 66	$29°C$ / 23.5

Both reasonable.

2c

Newtons law of cooling

$Q = h \times A \times \Delta T$ ← Assume $T_{amb} = 20°C$

Pent A $= 2 \times 0.01^2 \times 48 =$ ~~0.48~~ 0.96 96mW

i7 B $= 2 \times 0.05^2 \times 9° =$ ~~0.45~~ 0.9 0.9mW

This is 1W of cooling, which is totally insufficient. We need to dramatically increase the effective area, which we can do by adding fins to the heat sink.

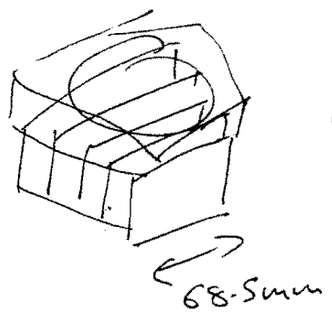
A typical assembly then has a fan blowing air over a multiply-finned heat sink. We are going to have to increase the effective area considerable up to 100x for IC B.

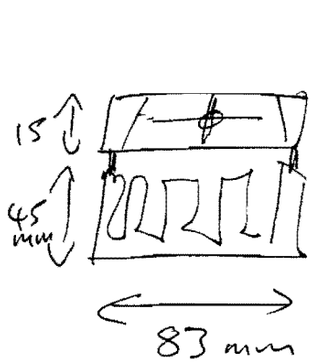
EEE6393 2012

1

Solutions

A



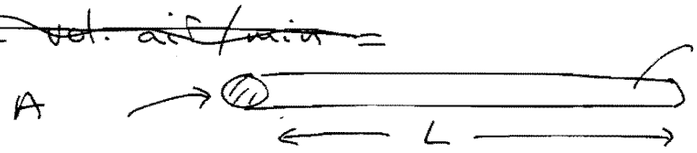


~~B~~ Copper used to increase thermal conductivity and lower thermal expansion coef.

~~B~~ from data: Airflow = 20CFM = 20×0.0283
$= 0.566\ m^3/min$

from data: cross-sectional area of fan = $\pi . r^2$
$r = 35$ mm (half of fan size)
$= \pi (35 \times 10^{-3})^2$
$= 38.5 \times 10^{-4}\ m^2$

~~Hence vol. air/min =~~

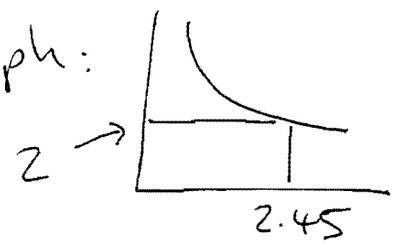


$V = AL$

$V = 0.566\ m^3$, $A = 38.5 \times 10^{-4}\ m^2 \Rightarrow L = \frac{0.566}{38.5 \times 10^{-4}} = 147\ m$

$\Rightarrow$ in one second: $\frac{L}{60} = 2.45\ m$ ie velocity = $2.45\ m/s$

From graph:



$R = 2°C/W$

1

(C) $Q = 25W$

Assume: $T_{max} = 125°C$ $T_{Room} = 20°C \Rightarrow \Delta T = 105°C$

$$\frac{\Delta T}{Q} = R_{P4} + R_{cooler} + R_{interface}$$

Assume $R_{interface} \sim 0$

$$\therefore R_{P4} = \frac{\Delta T}{Q} - R_{cooler}$$

↖ from (C). if not, then make assumption...

$$= \frac{105}{25} - 2$$

$$= \underline{\underline{2.2\ °C/W}}$$

(D) At high altitude air pressure is less, therefore lower mass of air forced onto heatsink (same volume of air). Heat transfer is by conduction from heatsink surface to gas, hence less gas = less conduction. ~~ie fewer~~, ie higher thermal resistance.

(E) Large number of tracks (478 pins) ⇒ high density. 4 layer board necessary to cope with this high density. For A 2 layer board the track pitch would be too high.

(F)
- cloth + resin → prepreg.
- prepregs + copper ~~foil~~ + heat → 2 layer laminate
- Photolith + vias (blind through)
- 2 × 2 layer board + prepreg + heat → 4 layer board. Vias
- Solder mask.

2

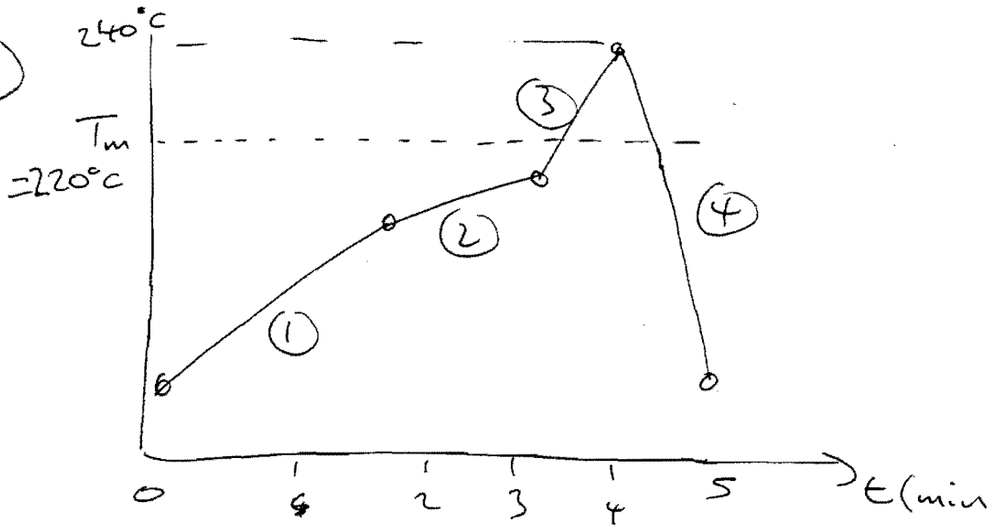
(A) SAC305

Sn	96.5 wt%	Tin
Ag	3.0 wt%	Silver
Cu	0.5 wt%	copper

(B)
Solder microspheres - electrical connection, etc
Flux (organic acid) - remove surface oxide
Solvent (organic) - enables paste to be spread
Binder/Rheology modifier - make it easier to spread.

(C) Eutectic - lowest melting point for the ternary Sn-Ag-Cu system, hence lower heating costs and thermal shock to components.
Also, eutectic composition goes direct from solid → liquid, without liquid/solid mixtures of varying composition hence accurate melting point, making process control easier.

(D)



1. Preheat - gradual, to avoid thermal shock. Solvent evap. Moisture removed
2. Soak - ensure isothermal, flux activated
3. Reflow - rapid heating above Tm 'Reflow' of solder.
4. Cooling - rate critical to avoid stresses and grain growth.

2

(E)

$$Z_0 = \frac{87}{(1.41+\varepsilon_{eff})^{1/2}} \ln\left(\frac{6h}{(0.8w+t)}\right)$$

(K_1)

Given: $h = 200\times10^{-6}$ m $\varepsilon_{eff} = 4$

Assume: $Z_0 = 50\,\Omega$ $t = 35\times10^{-6}$ m (1oz copper)

Rearranging: $Z = K_1 \ln K_2 \therefore e^{Z/K_1} = K_2$

$K_3 = e^{Z/K_1} = e^{50/(\frac{87}{1.41+\varepsilon})^{1/2}} = e^{1.9598} = 7.0979$ ✓

$K_2 = \frac{6h}{0.8w+t} \therefore w = \left((6h/K_2) - t\right)\times 0.8$

$K_2 = K_3$ ✓

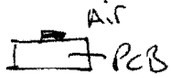
$$\therefore w = \left(\left(\frac{6\times 200\times10^{-6}}{7.0979}\right) - 35\times10^{-6}\right)\times 0.8$$

$= 107\ \mu m$

$t = 0\,\mu m \Rightarrow w = 135\,\mu m$
$t = 1\,\mu m \Rightarrow w = 134$
$t = 10\,\mu m \Rightarrow w = 127$
$35\,\mu m \Rightarrow 107$

$100\,\mu m \Rightarrow 55\,\mu m$
$500\,\mu m \Rightarrow$ -ve!
$170\,\mu m \Rightarrow 0$

(F) ε_{eff} - effective dielectric constant.
- made up from ε_{air}, ε_{PCB}



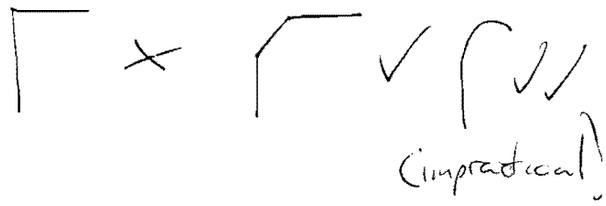
(G) Crosstalk - changing current in one conductor induces voltage in another. $V \sim 30$mV - significant, BUT if we have 32 tracks, then $V \cong 32\times30 \sim 1V$ - sizeable spike!

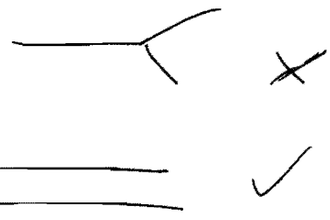
(H) Make track further apart.
Switch to stripline.

PTO ↓

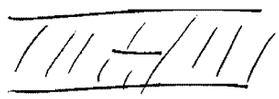
new d.

Strategies to minimise impedance changes on PCB tracks:

Avoid sharp corners: 

Avoid junctions: 

Use ground planes to surround signal – stripline:



with vias:

nearest approx. to coax.

Avoid slots in ground plane beneath tracks.