The University Of Sheffield.

Data Provided:

Boltzmann constant $k_B = 8.6 \times 10^{-5}$ eV K^{-1}

Thermal conductivity data:

$k_{glass} = 1.2$ W m^{-1} K^{-1}

$k_{silicon} = 120$ W m^{-1} K^{-1} $k_{copper} = 390$ W m^{-1} K^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (2.0 hours)

EEE6393 Microsystems Packaging

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1.

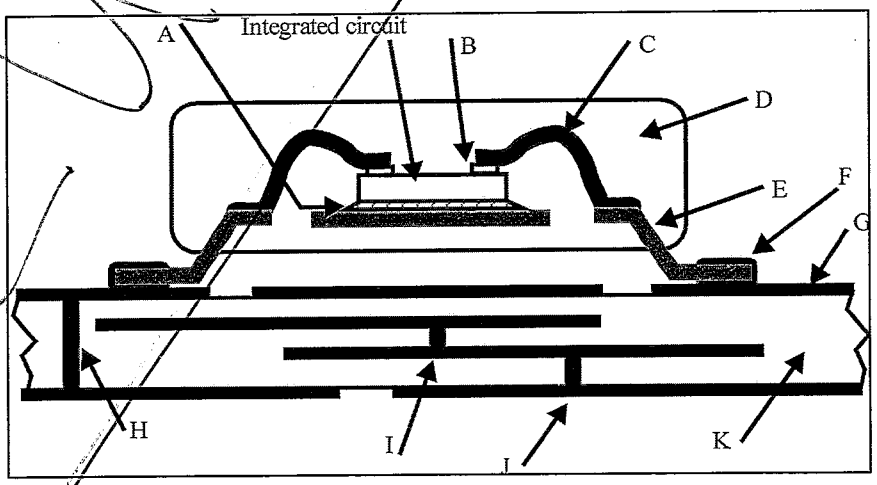


Figure 1 Cross-section of a packaged silicon chip and substrate (not to scale)

With reference to Figure 1, answer the following questions:

a. What are typical dimensions and compositions of A, B and C? **(3)**

A – die-attached adhesive, silver loaded epoxy or solder, ~ 50 μm thickness

B – bond pad, aluminium, ~ 1 μm thickness

C – wire bond, gold (or alumnium), 25 – 300 μm diameter

b. What is the typical composition of D? **(1)**

		Silica-loaded epoxy resin	
	c.	What is E and how is it made? *Tape-automated bond (TAB) frame, formed by etching of photolithographically-patterned metal/polymer foil/film.*	**(2)**
	d.	What is the typical composition and purpose of F? *Solder – low melting point metal alloy, for electrical/thermal/mechanical connections between chip package and substrate*	**(2)**
	e.	What material/materials are typically used for G and K? *G – electrical conductor (copper)* *K – dielectric (epoxy/glass laminate or ceramic)*	**(2)**
	f.	Identify the features H, I and J. *H – through via, I – buried via, J – blind via*	**(2)**
	g.	During testing it is found that the signals between the integrated circuit (IC) and a simliarly-packaged ajacent IC are too slow and are distorted. Describe how the IC packaging and substrate could be changed to solve these problems. *Shorten interconnect length by switching from TAB frame packages to flip chip packages with ball grid arrays.* *Reduce the signal distortion on the PCB by implementing the interconnections as controlled impedence transmission lines (stripline, etc).*	**(4)**
	h.	Packaged silicon chips are subject to the highly accelerated steam and temperature test (HAST) and are found to have a failure rate of 0.087. Inspection of the failed devices shows electrochemical corrosion, which is known to have an activation energy E_a of 0.6 eV. What is the estimated failure rate at 20 °C, 50 % relative humidity? You may assume that the failure rate (F) is proportional to the reciprocal of the cube of the relative humidity (H), i.e. $F \propto 1/H^3$. *Recall HAST conditions: $T = 120$ °C, $RH = 85\%$* *Assume Arrhenius equation is valid: $F(H,T) = H^{-n} \exp(-E_a/k_B T)$* *Hence, acceleration factor $AF = (0.85/0.5)^{-3} \exp(-E_a/k_B(1/393 - 1/293) = 87$* *Hence $F(20) = 0.087/87 = \underline{0.001}$*	**(4)**

2. **a.**

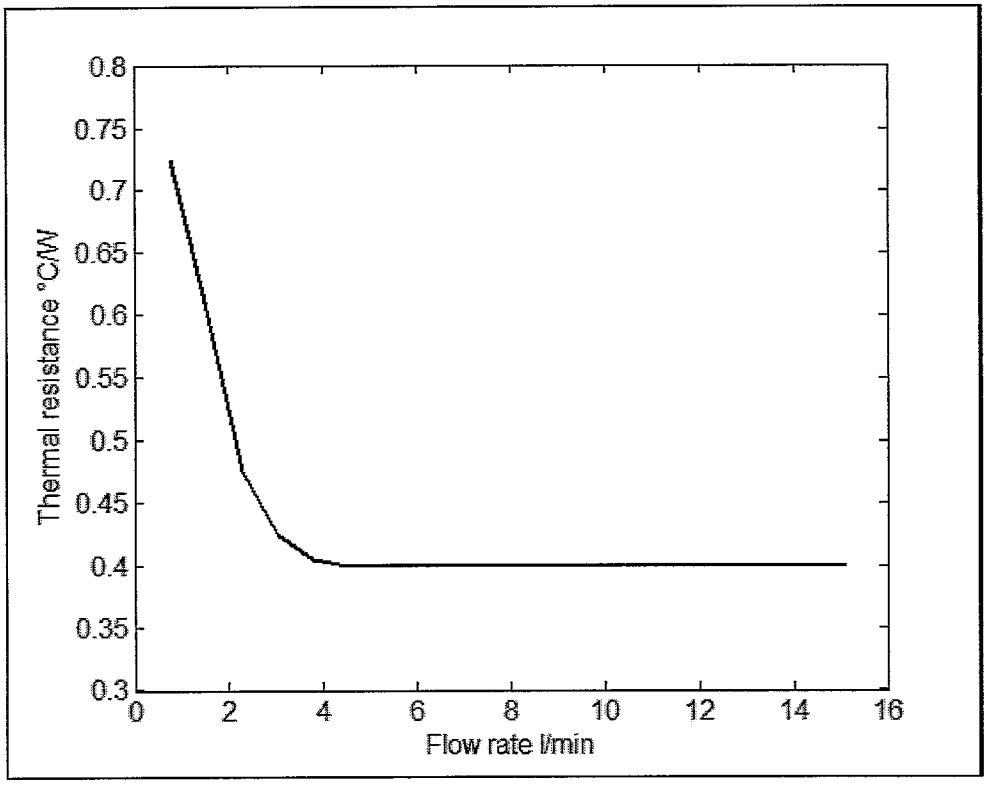


Figure 2 Thermal resistance of heat exchanger as function of fluid flow rate

Ten printed circuit boards (PCBs) are stacked in a rack that forms part of an avionics system that must operate at a high altitude. Each PCB dissipates 10 W and is cooled via a heat exchanger clamped along one edge of the PCBs. A fluid at 15 °C flows through the heat exchanger. The thermal resistance of the heat exchanger as a function of fluid flow rate is shown in Figure 2. What is the minimum thermal resistance of the PCBs that will keep their average temperature below 40°C? State all the assumptions and approximations that you make.

$\Delta T = 40\text{-}15 = 25°C$

Consider one board in centre of stack and ignore edge effects, hence $Q = 10$ W

Assume no heat loss by radiation (equal emission/absorption from/to each PCB).

Assume no convection (high altitude = low air pressure).

Assume fluid flow rate > 5 l/min, hence $R_{heatexchanger} = 0.4$ °C/W (min. value).

Fourier's Law of (conductive) heat flow: $\Delta T = QR$

Where: $R = R_{PCB} + R_{heatexchanger}$

Hence: $R_{PCB} = \Delta T/Q - R_{heatexchanger} = 25/10 - 0.4 =$ 2.1 °C/W **(6)**

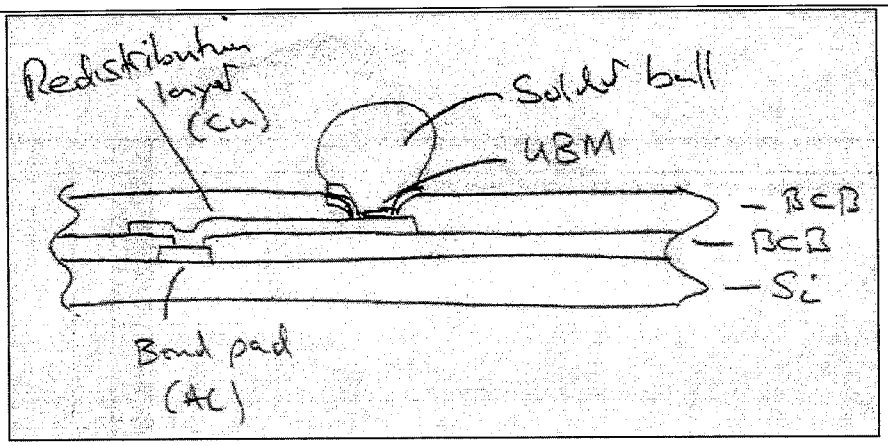
b. For the scenario described in **2.a.**, suggest what factors in the PCB construction would help achieve a low thermal resistance between the components attached to the PCB and the heat exchanger.

Thick, continuous metal heat spreader layer(s) extending to the edge of the PCB that is clamped to heat exchanger. Ground layer in direct contact with heat spreader (using multiple thermal vias if necessary). **(2)**

c. Some temperature sensitive bio-sensor chips need to be attached to a substrate. **(4)**

		The maximum temperature which the chips can withstand is 100°C. Describe two ways in which the attachment can be made, with reference to the electrical, mechanical and thermal performance. *Low temperature bonding, therefore cannot use solder. Use conductive adhesive instead - either isotropic (ICA) or anisotropic (ACA). Minimal surface tension, so no self-alignment, unlike with solder.* *ICA* *ICA = silver flakes in thermoset (epoxy) polymer. Deposit onto substrate bond pads by screen printing. Bond pads need to have noble metal finish for reliability. Assembly then needs separate underfill step.* *ACA* *ACA = conductive microspheres in epoxy. Deposit onto substrate as a continuous layer. Tall (noble metal finish) bond pads needed to provide compression during bonding. Microsphere density must be high enough to generate conductive path under compression, but low enough to prevent lateral conduction. High bond force needed. No need for separate underflow step.*	
	d.	Explain the differences between performing surface mount assembly with a eutectic and non-eutectic solder alloy. *Eutectic – lowest melting point for alloy system, hence lowest energy costs and lowest residual stress when system cooled to room temperature. Eutectic has abrupt melting point, rather than an extended softening zone. This may be beneficial or detrimental, depending on process.*	**(4)**
	e.	Describe how through-glass and through-silicon vias are made. *Drill holes (laser/plasma/wet etch). Stress-relief layer deposition. Seed layer deposition (electroless plating). Hole filling (copper electroplating). Attach wafer to carrier. Back thin (grinding and chemical/mechanical polishing).*	**(4)**

3.	**a.**	Explain the advantages of a system in package (SIP) over discretely packaged devices. *Shorter interconnections, therefore higher performance.* *Reduced size/mass.* *Heterogeneous integration possible.* *Higher yield, due to testing of individual devices prior to assembly.* *Simpler to design than SoC.*	**(4)**
	b.	i) Calculate the thermal resistance between the top and bottom surfaces of a 200 μm thick glass interposer with a surface area of 5×10 mm. *i)* $R_{glass} = L/k_{glass}A_{glass} = 200x10^{-6} / (1.2 \times 50x10^{-4}) =$ <u>*0.033 °C/W*</u>	**(2)**
		ii) A 100×200 array of 40 μm diameter copper through glass vias (TGVs) are added to the interposer. Calculate the revised thermal resistance. *ii)* $A_{via} = \pi \times (20x10^{-6})^2 = 1.2x10^{-9}\ m^2$ $A_{vias} = A_{via} \times 100x200 = 24x10^{-6}\ m^2$ $R_{via} = L/k_{Cu}A_{via} = 200x10^{-6} / (390 \times 1.2x10^{-9}) = 408\ °C/W$ $R_{vias} = R_{via}/(100x200) = 0.0204\ °C/W$ *New glass area* $A_{new} = A_{glass} - A_{vias} = 50x10^{-4} - 24x10^{-6} = 4.96x10^{-4} \sim A_{glass}$ *Hence, revised thermal resistance (resistors in parallel):* $R_{new} = (R_{glass} \times R_{vias})/ (R_{glass} + R_{vias}) = (0.033x0.0204)/(0.033 +0.0204)$ $=$ <u>*0.013 °C/W*</u>	**(3)**
		iii) Comment on your results. *iii) Despite their negligible cross-sectional area (<1%), the vias reduce the thermal resistance of the interposer by 30 %.*	**(1)**
	c.	There is considerable heat generation on a power semiconductor. What are the sources of this heat and what measures can be taken to reduce it and accommodate it? *Heat sources: Joule heating (I^2R) in conductors; on state; off-state (leakage current); capacctance; transients.* *Mitigation: use SiC rather than Si (can operate at higher T); transistor architecture; direct-bond copper heat sinks*	**(4)**
	d.	A wafer-level packaging scheme first involves spin coating a layer of photo-imageable polymer (BCB) on top of the fully-processed CMOS devices. i) Describe the remaining steps necessary to form a chip scale packages with a ball grid array (BGA) interconnections. You may wish to include an annotated diagram of the package. *i) Pattern BCB lithographically to open vias to chip bond pads (Al). Deposit metal (Cu) layer by sputtering. Deposit resist and then pattern copper to form redistribution layer and BGA pads. Deposit another layer of BCB, pattern to open vias to BGA bond pads. (Test.) Deposit UBM onto bond pads (sputtering). Screen-print solder paste onto bond pads. Reflow to form BGA. Dice.*	**(4)**

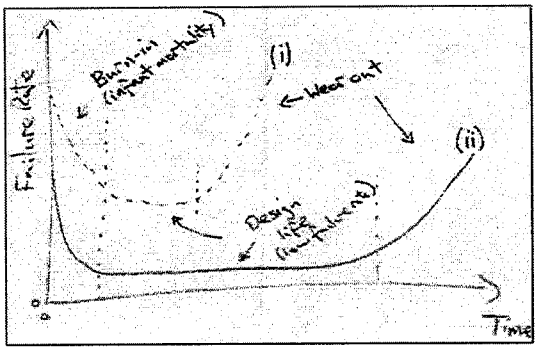


ii) What are the benefits of this wafer-level packaging approach in comparison to a standard BGA package?

ii) Benefits: cheaper and smaller. Justification needed for full marks. **(2)**

4. a. Draw a single sketch to show the failure rate as a function of time for these two electronic microsystems: i) an integrated circuit inside an electric toothbrush, ii) an integrated circuit inside the control system for an aircraft. Identify the various parts of the curves.

ANSWER:



(4)

b.

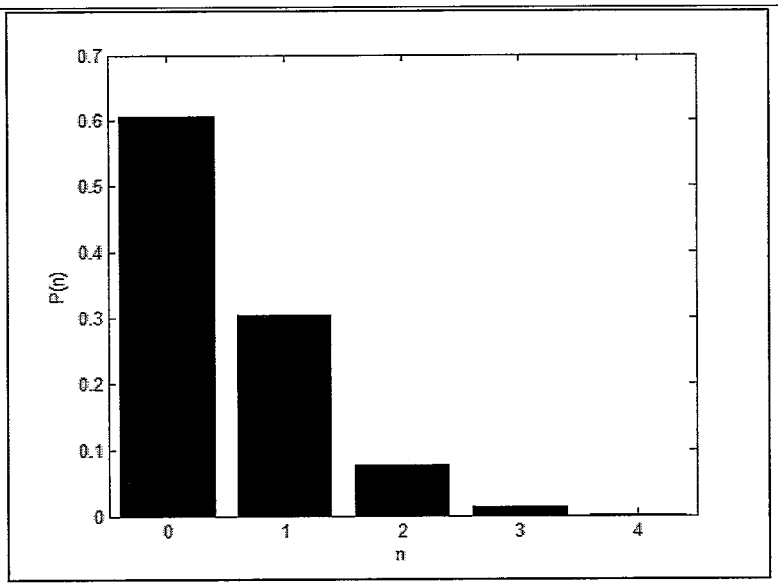


Figure 3 Defect data for lithographic process

A lithography system is used to pattern wafers containing 200 individual devices. The probability, *P*, of there being *n* defects on an individual device is given by the data in Figure 3. A laser system can be used to repair some of the defects. The probability that an individual defect can be repaired is $\eta = 0.5$.

On a single wafer, how many devices remain faulty after the repair process?

From the table: P(0)= 0.6, P(1) = 0.3, P(2) = 0.05, P(3)=0.02

Yield $= P(0) + \eta(P1) + \eta^2 P(2) + \eta^3 P(3) = 0.6 + 0.5x0.3 + 0.25x0.05 + 0.125x0.02 = 0.765$

Hence number of faulty devices = (1-0.765)x200 = 47

(3)

c. An edge-emitting laser diode is flip-chip bonded onto a silicon substrate. Describe how the anisotropic etching of silicon can be used to accomplish the coupling of an optical fibre to the diode.

Anisotropic etching (KOH or TMAH) of a {100} orientated silicon wafer results in 54.7° sloping side walls, hence simple photolith. + etching enables V grooves of precise width to be made. Fibres can be seated in groove

(4)

	d.	Explain the fabrication process for a 'thick film' hybrid substrate containing copper conductors and integrated resistors. The substrate is to be used to house a high-performance silicon IC. Explain how a hermetic lid is attached to the substrate. *Deposition of layers of paste onto ceramic substrate. Deposition via screen printing on pre-formed layers ('green tape'). Insulating paste made from ceramic powder plus glass and organic binder. Conductive paste made from metal powder plus glass and organic binder. Resistors made from refractory metal oxides plus glass and binder. Once all layers are assembled, the stack if fired at high temperature to firstly remove binder (pre-heat stage) and then melt low T_m glass. ~15% chrinkage during firing. For LTCC, T~800 °C – non-refrcatory metals (Au, Ag, Pd)) can be used, for HTCC, T~ 1800 °C refractory metals used (W, Mo).* *Hermetic (metal) lid added with hermetic seal formed by brazing or soldering with a metal alloys or with a low melting point glass.*	**(5)**
	e.	How does the cross-sectional shape and surface finish of the electrical conductors on a printed circuit board (PCB) effect the propagation of high speed signals (frequency > 1 GHz)? *Skin effect (due to self-induction phenomenon) means that high speed AC flows only in outer sheath of conductor, hence resistance increases, hence larger attenuation and slower propogation. Surface roughness of conductor may also start to play a part in altering resistance/velocity.*	**(4)**

GLW