Power Semiconductor Devices and Technologies

EEE6206

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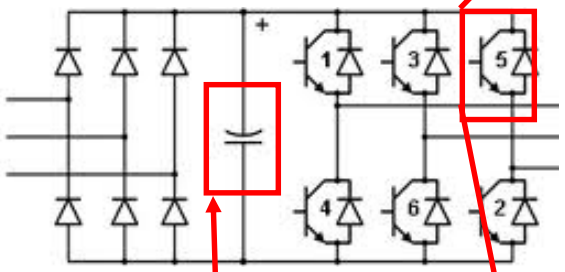
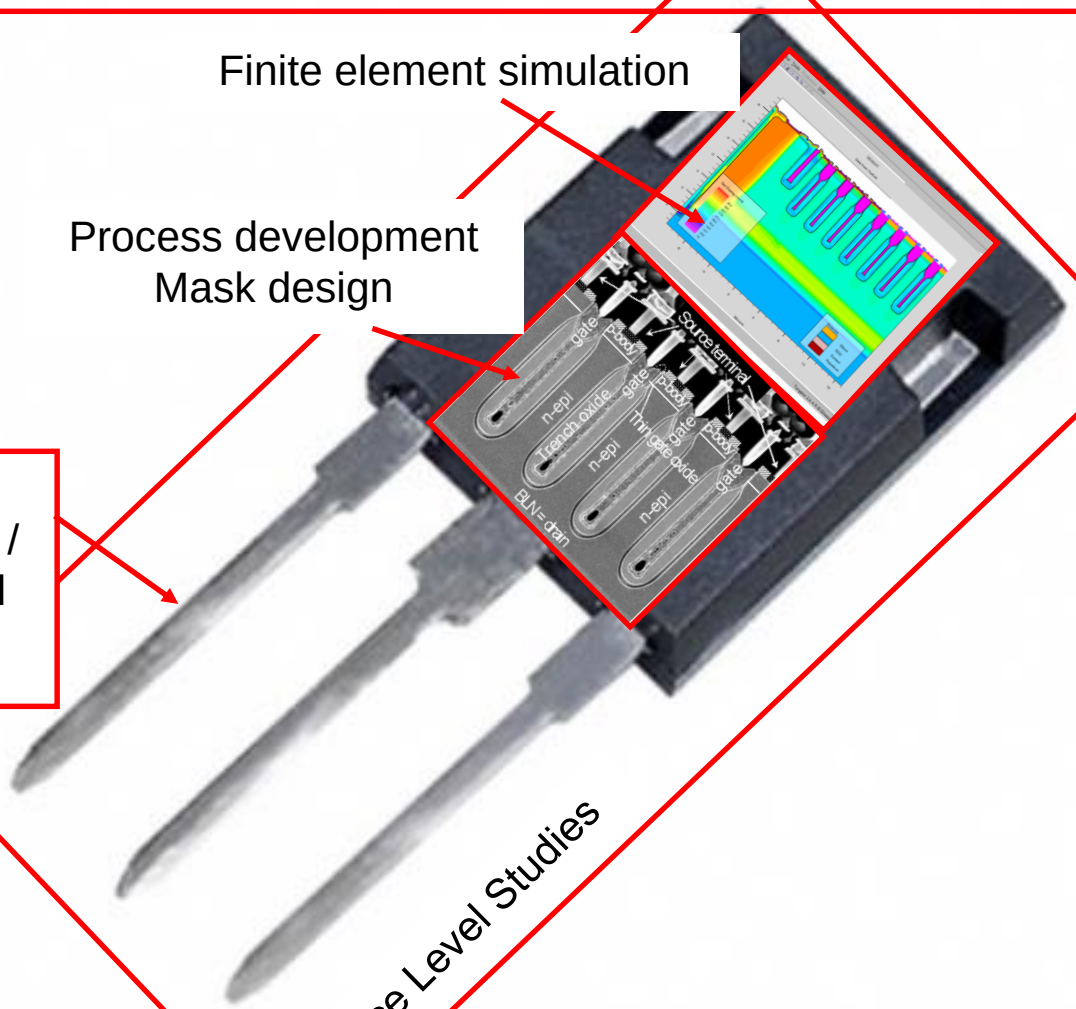
Research Domains

Converter Level Studies



Finite element simulation

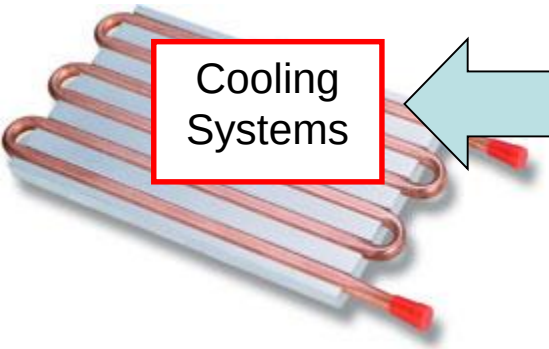
Process development
Mask design



Advanced Gate Drives / device level layout

Filter designs

Cooling Systems



Device Level Studies

Module Packaging

Aims for this module

- Introduce and develop an understanding of power semiconductor devices - physics, technologies, design, fabrication and characterisation
- Evaluate suitability of various semiconductor device concepts for specific power electronic applications
- Device integration concepts such as device assembly, packaging and thermal constraints

Lecture delivery plan

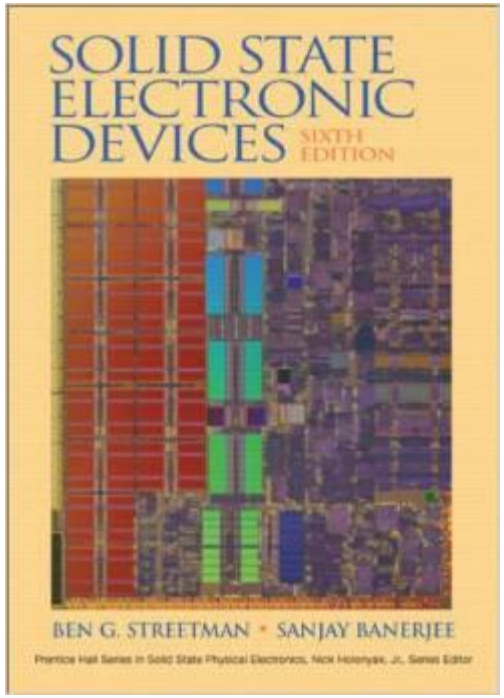
- Introduction to semiconductor device physics
  - Properties of semiconductors
  - Carrier transport processes
- Bipolar device technologies
  - Power Diodes, Transistors and Thyristors
    - Basic structure
    - Breakdown mechanisms
    - On-state/transient behaviour
    - State of the art technologies
- Unipolar and MOS bipolar device technologies
  - MOSFET and IGBT device physics
    - Modes of operation, static and dynamic characteristics
    - Physical limits of MOSFET structures (material limit)
    - IGBT evolution

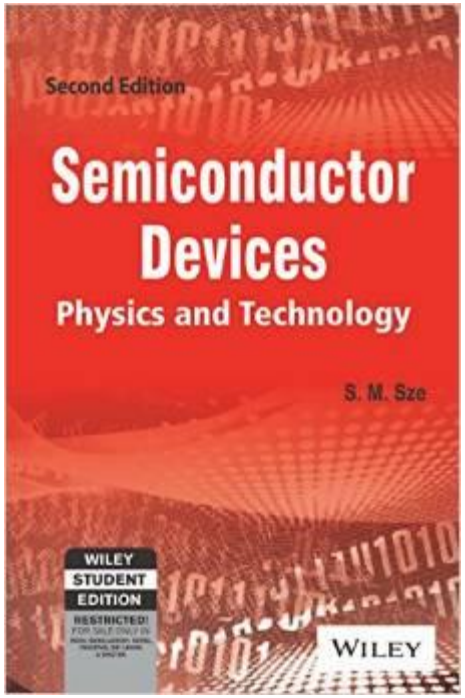
- Power device processing
  - Fabrication techniques
    - Power IC and Discrete technologies
  - Device layouts
    - Active area and termination zones
- Power device packaging and evaluation
  - How to read datasheets
  - Electrical characterisation techniques
  - Power loss analysis and cooling
  - Discrete and multi-chip module packaging design and processes
- Future of power device technologies
  - Wide band gap semiconductors
    - SiC and GaN device technologies
  - Future power device and packaging materials

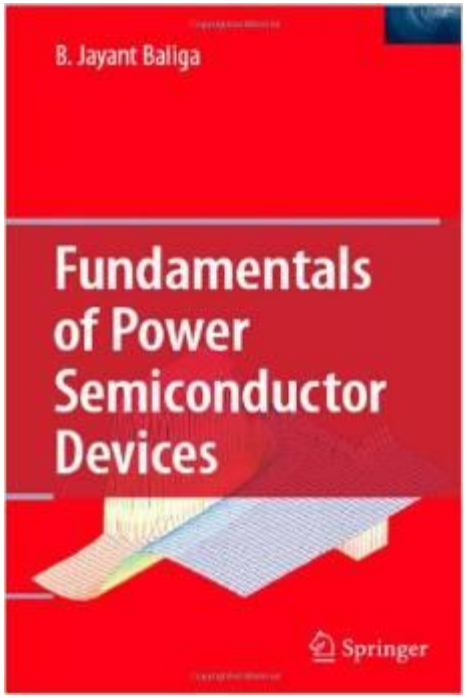
Module details

- Time Allocation
  - 36 lectures, 62 hours independent study
  - Recommended for additional material
    - EEE337: Semiconductor Electronics
    - EEE307: Power Electronics
- Assessment
  - 3 out of 4 questions: 2 hour examination
- Beware of units!!!
  - Intrinsic carrier density calculation atoms/m^3
    - Semiconductor equations use atoms/cm^3
  - Bipolar technologies: cm
    - E.g. Current densities J=A/cm^2
  - CMOS: mm
    - E.g. Specific on-state resistance mΩ mm^2

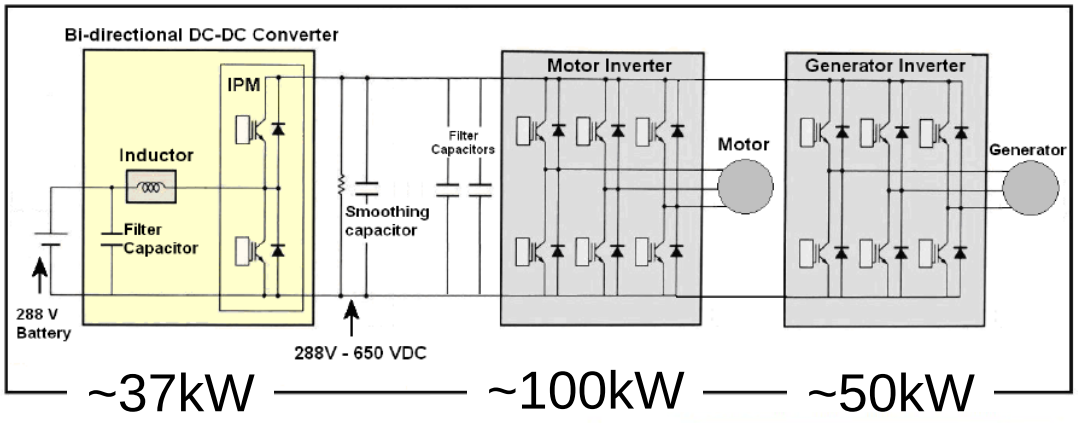
Recommended books



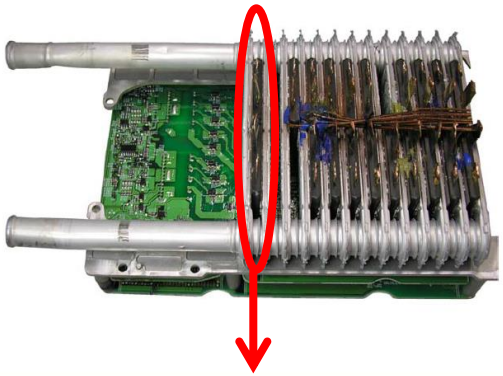


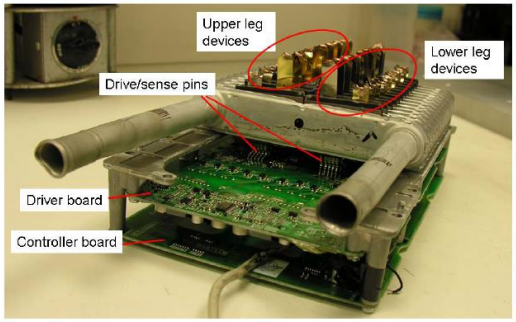


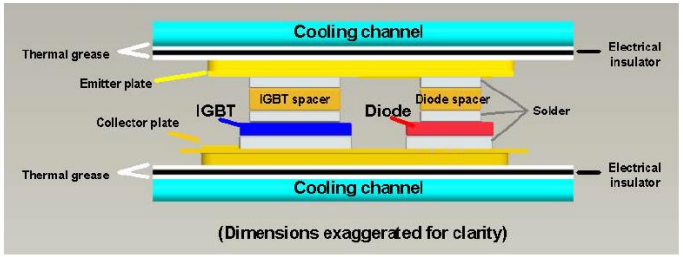
Typical Power Converter Architecture: HEV

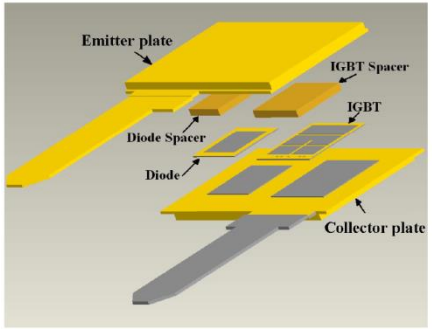


~187kW









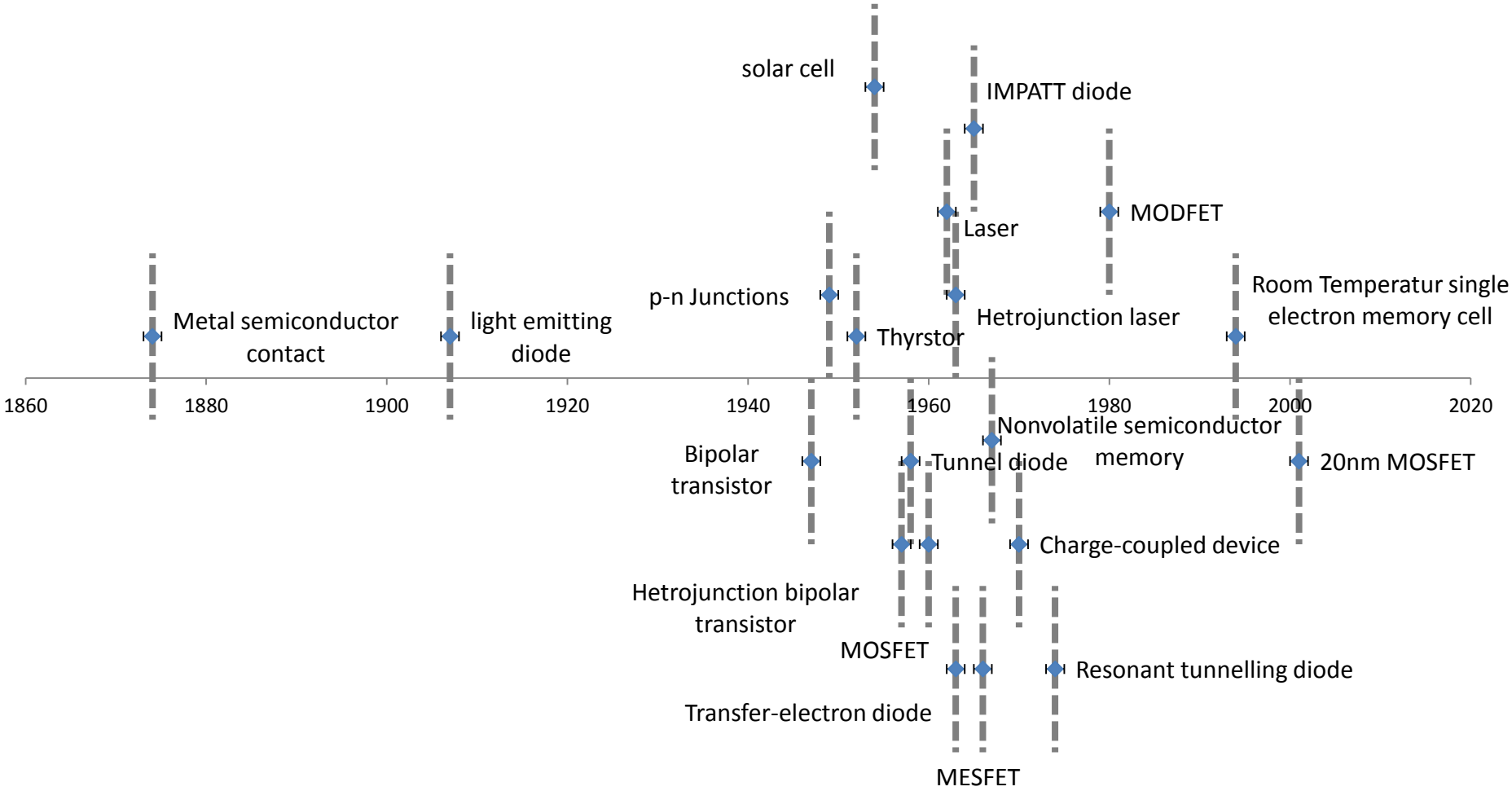
Semiconductor building blocks

- Semiconductor devices have been studied for 125 years
  - To date we have 60 major devices with over 100 device variations
  - All theses devices can be constructed from smaller device building blocks
- Metal semiconductor contact: First building block studied (1874)
  - Used as an rectifying contact (unidirectional current flow) or a ohmic contact (bidirectional current flow with negligible barrier voltage)
- Second building block is the P-N junction formed between an n type and p type semiconductor
  - Key building block for most semiconductor devices, theory of PN junctions serves as the foundation of semiconductor device physics
  - One PN junction: PN diode / Two: Bipolar transistor, Three: Thyristor

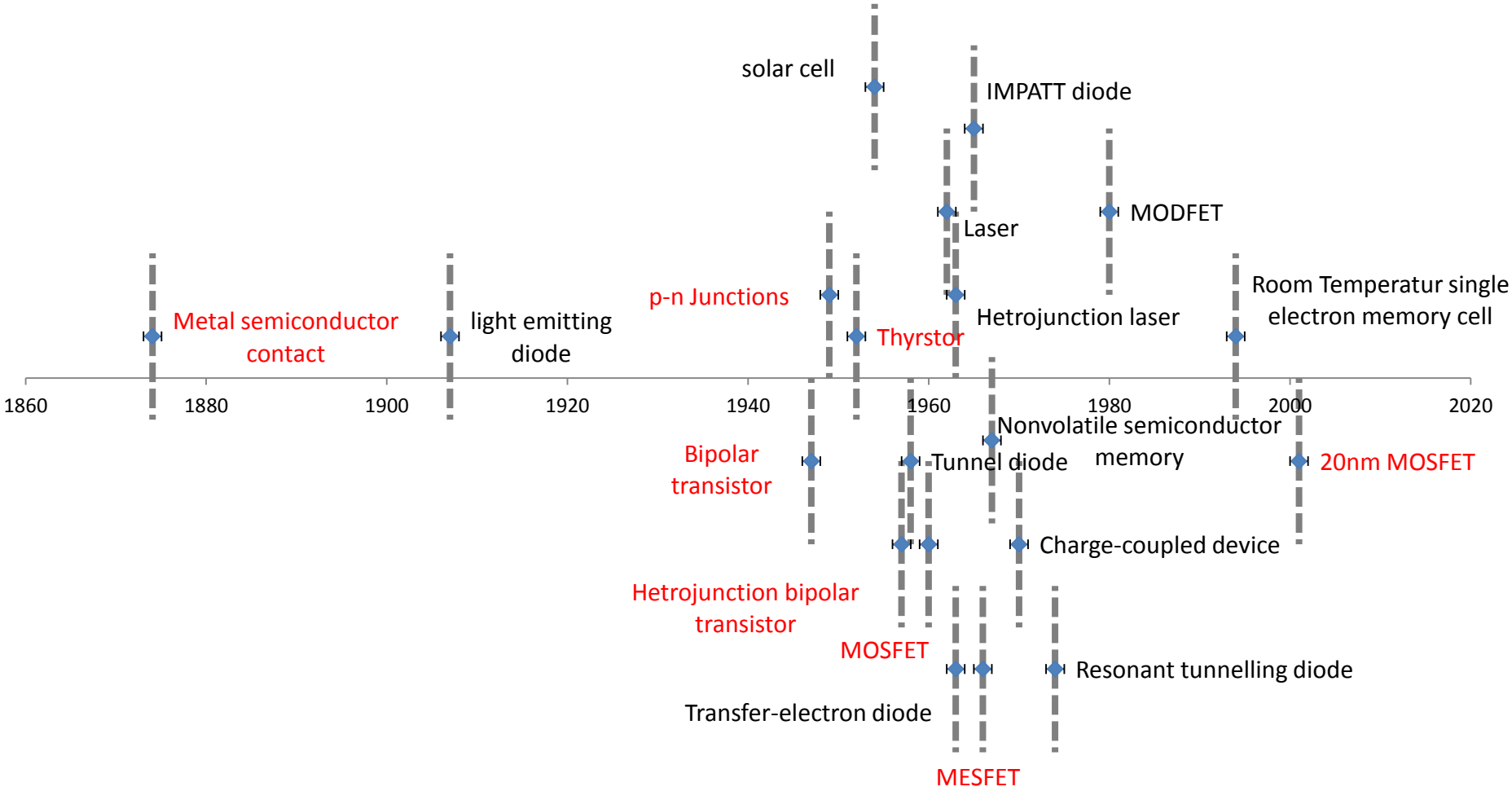
- Third building block: Heterojunctions: Interface between two dissimilar semiconductors, i.e. GaN / AlGaN
  - Key components for high speed and photonic devices
  - Architecture for next generation high voltage devices

- Forth building block: Metal oxide semiconductor structure
  - Combination of a metal-oxide interface and an oxide-semiconductor interface
  - Combining the metal oxide interface with pn junctions forms MOSFETs
    - Most important devices for large scale power devices and integrated circuits

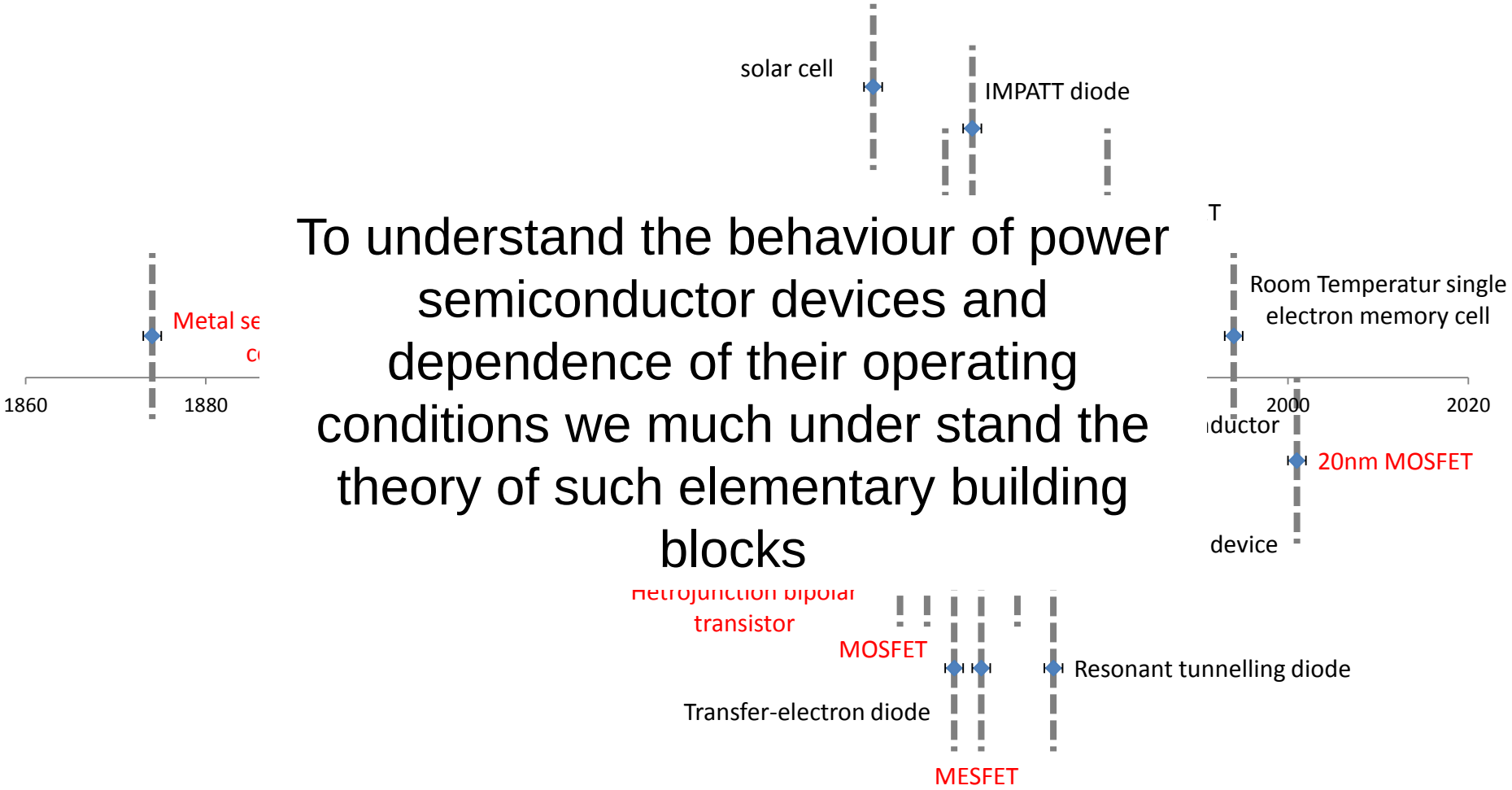
Major semiconductor device developments



Power semiconductor building blocks



Power semiconductor building blocks

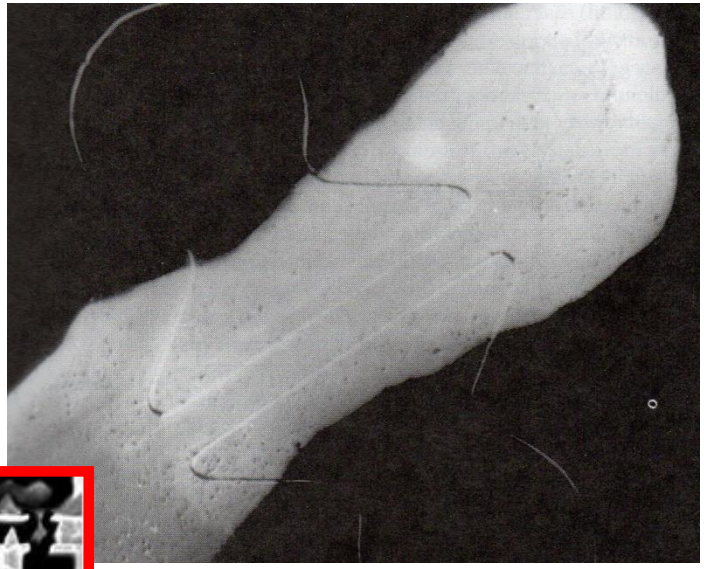


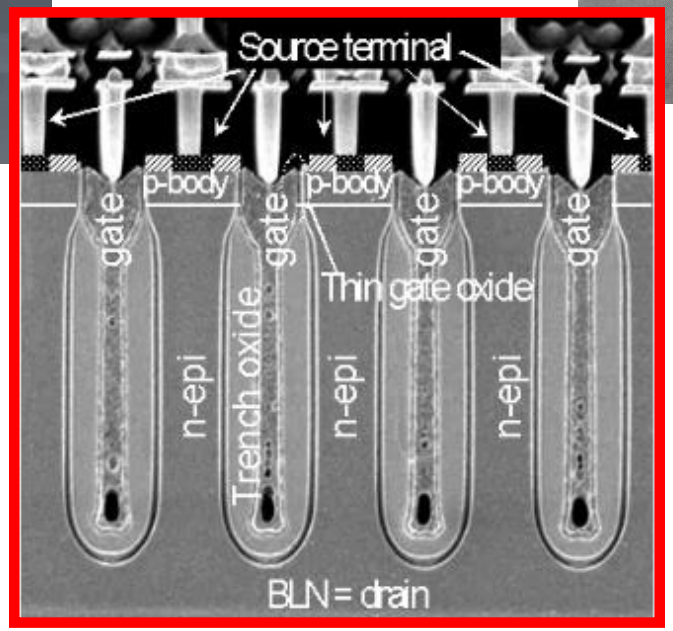
To understand the behaviour of power semiconductor devices and dependence of their operating conditions we much under stand the theory of such elementary building blocks

Technological development

First Bell laboratories Transistor (Crystal triode) ~1947

First Bell laboratories MOSFET ~1960





XMOS: ~ 2004
Vertical power MOSFET

- 0.35μm technology node
- Trench gate
- Vertical RESURF

Section 1: Properties of Semiconductors

Semiconductor materials

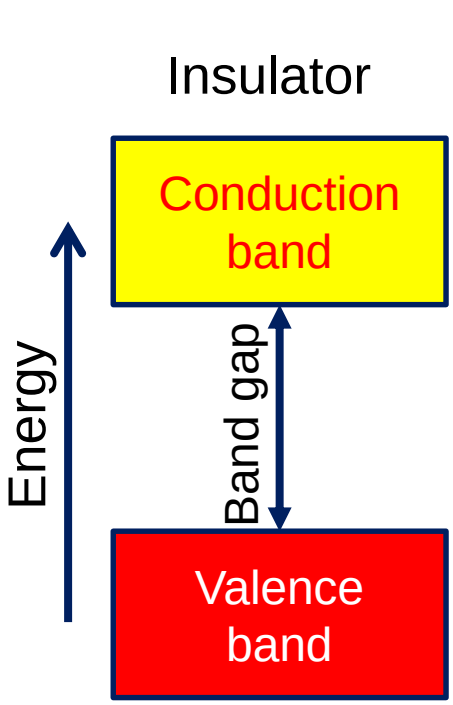
- Solid state materials can be grouped into three classes
  - Insulators, semiconductors and conductors
- Insulators, such as fused quartz and glass have low conductivities (1e-18-1e-8 S/cm)
- Conductors, aluminium silver have high conductivities (1e4 – 1e6 S/cm)
- Semiconductors conductivity lies between insulators and conductors
  - Conductivity sensitive to temperature, illumination, magnetic fields and impurity atoms
    - This sensitivity of conductivity is the most important feature of a semiconductor
  - Current and future semiconductors used for power devices:
    - Silicon, Silicon-Carbide, Gallium Nitride and Diamond

- **Trivia: What is the difference between a semiconductor and a metal?**

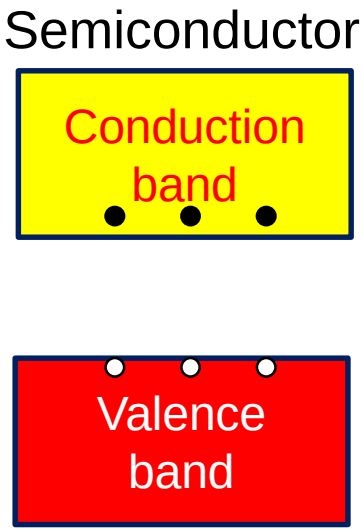
Charge Carriers and Semiconductor Band Structure

- Electrons in a semiconductor may exist in one of the two conditions
  - Free (in a interstitial position)
  - Bound (as in a covalent bond)
- Allowed energy levels of **bound** electrons make up the **valence band**
- Allowed energy levels of **free** electrons make up the **conduction band**
- These states are separate by an energy barrier
  - **Band gap**

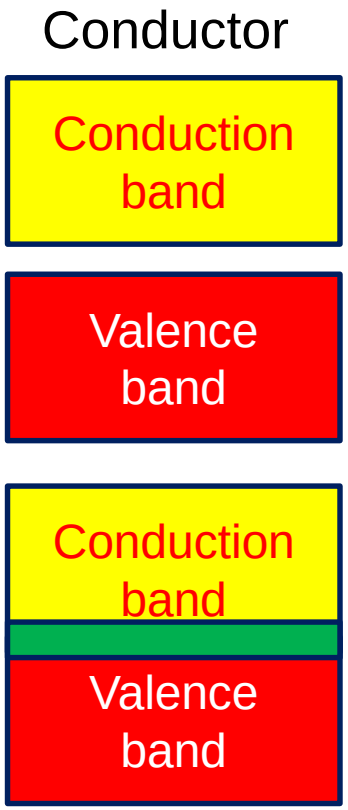
Insulators, Semiconductors and Conductors



Energy gap ~ 9eV
Conduction band empty
(electrons in bound state)

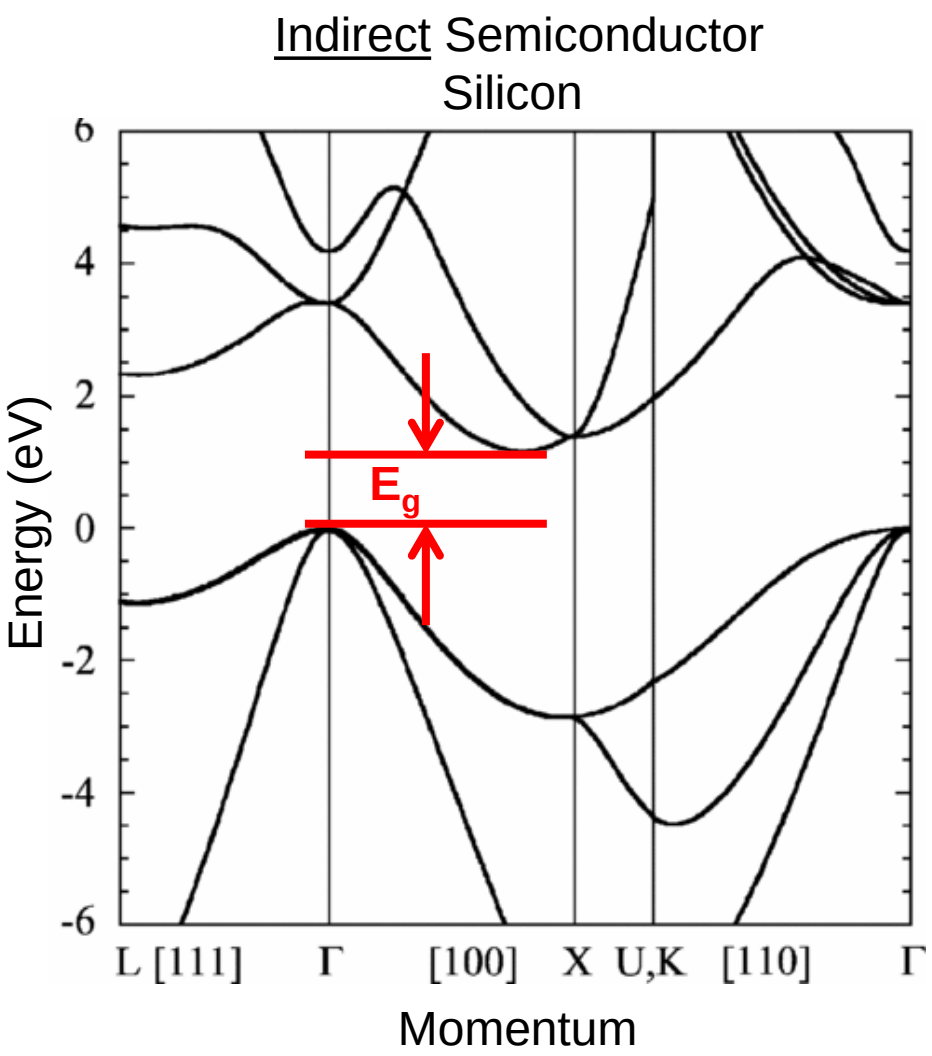


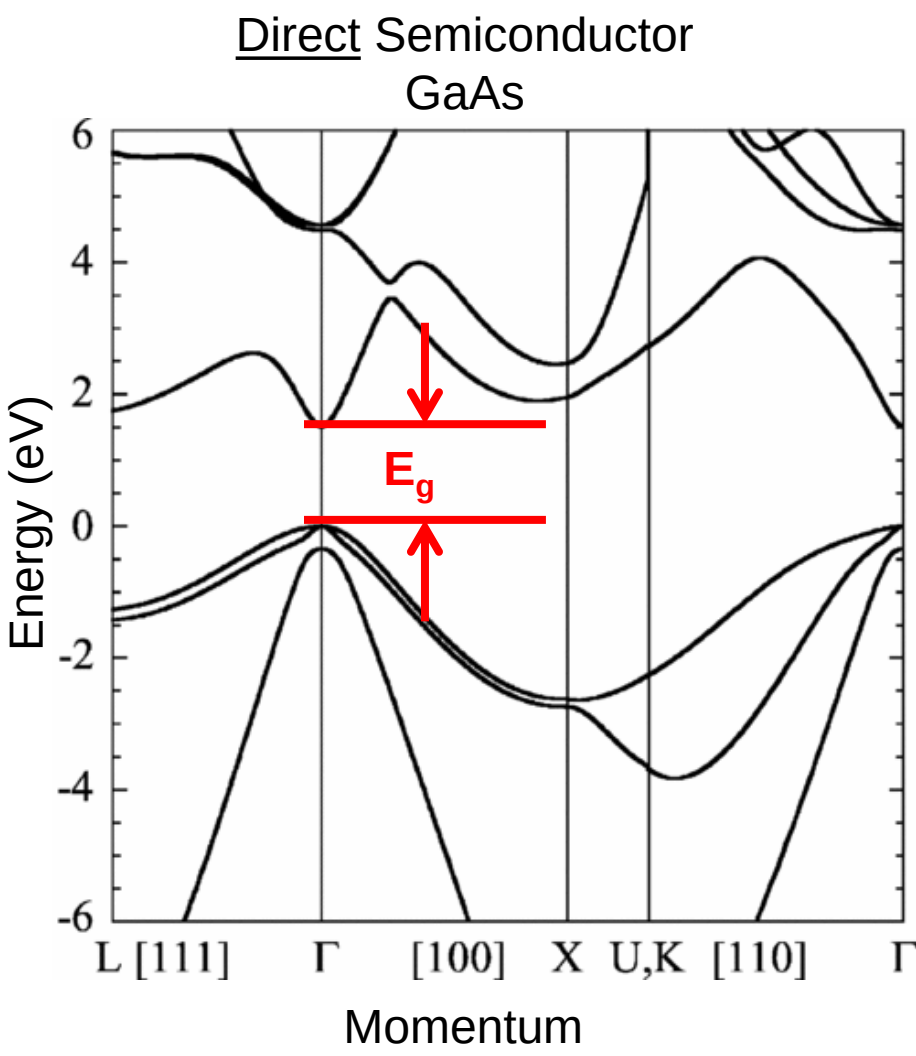
Energy gap ~ 1eV
Conduction and valence bands contain free electrons/holes



Two possibilities exist:
Partially filled conduction band (Cu)
Overlapping bands (Zn/Pb)

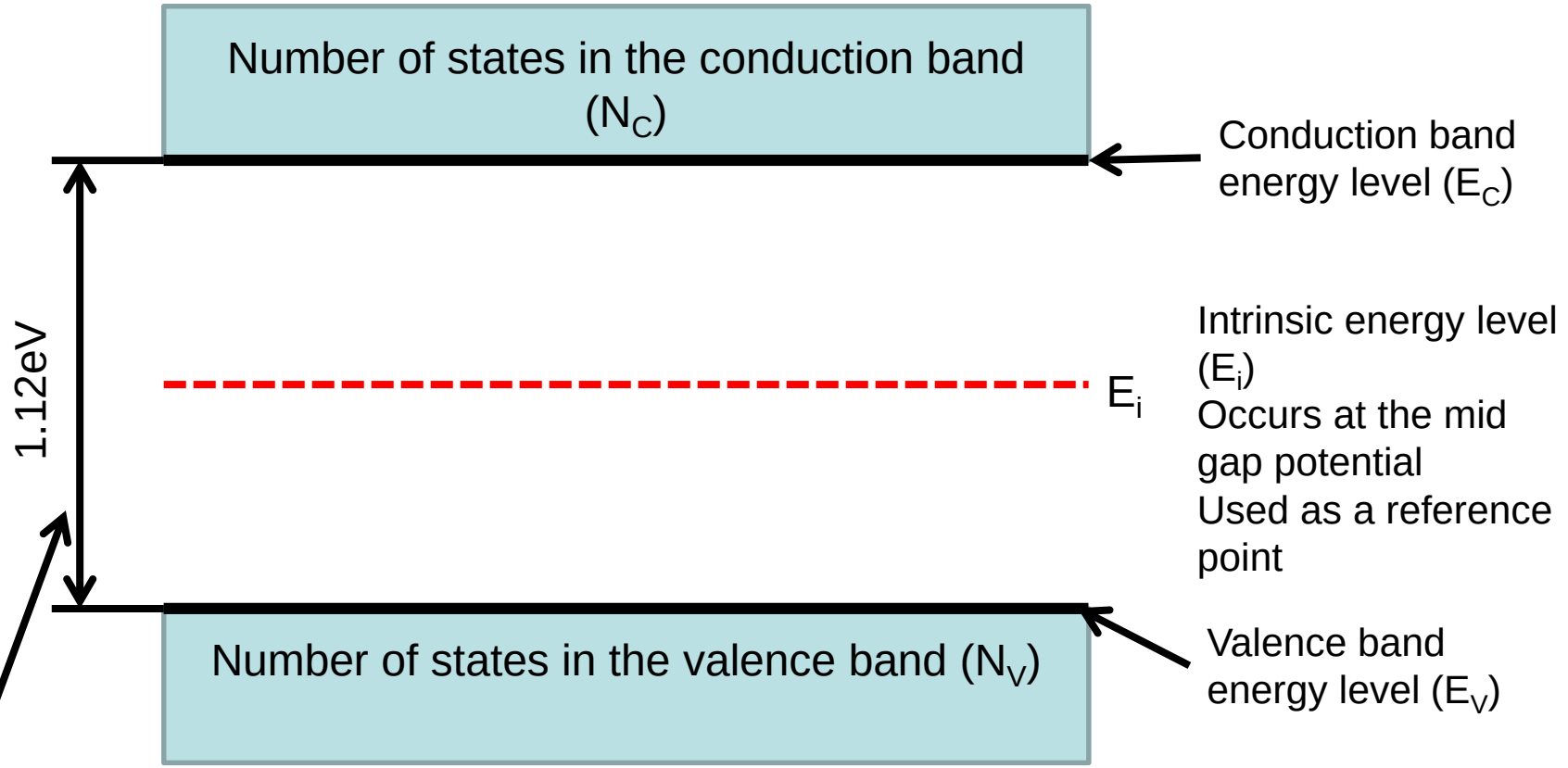
Direct – indirect band diagrams





Energy transitions in an indirect band gap material involve phonons

Semiconductor energy diagram: Silicon



Band Gap

- Pure semiconductor (no impurity atoms)
- No energy levels available to occupy an electron
- Band gap represents an energy level which needs to be overcome by electron to be promoted into the conduction band
- Once in the conduction band, electrons are free to move.

Intrinsic carrier concentration

- Under a steady state thermal equilibrium condition
  - Without any external excitation; such as light, pressure or electric field
  - Continuous thermal agitation results in the excitation of electrons from the valence band into the conduction band leaving an equivalent number of holes
- An intrinsic semiconductor is one that contains relatively small amounts of impurities compared to the thermally generated electron hole pairs
- To obtain electron density firstly we need to…
  - Evaluate the electron density in an incremental energy range (dE)
  - This density n(E) is given by:

$$n(E) = N(E)F(E) \quad (1)$$

  - Where: N(E) - Number of allowed energy states (including spin) per energy rate per unit volume and F(E) - Probability of the state being occupied

- Integrating this from the bottom to top of the conduction energy levels obtains the electron density

$$n = \int_{E_{bottom}}^{E_{top}} N(E)F(E)dE \qquad (2)$$

  - For simplicity 0 = bottom energy level of the conduction band
- The probability function, F(E), is given by the Fermi-Dirac distribution function

$$F(E) = \frac{1}{1+e^{\frac{E-E_f}{kT}}} \qquad (3)$$

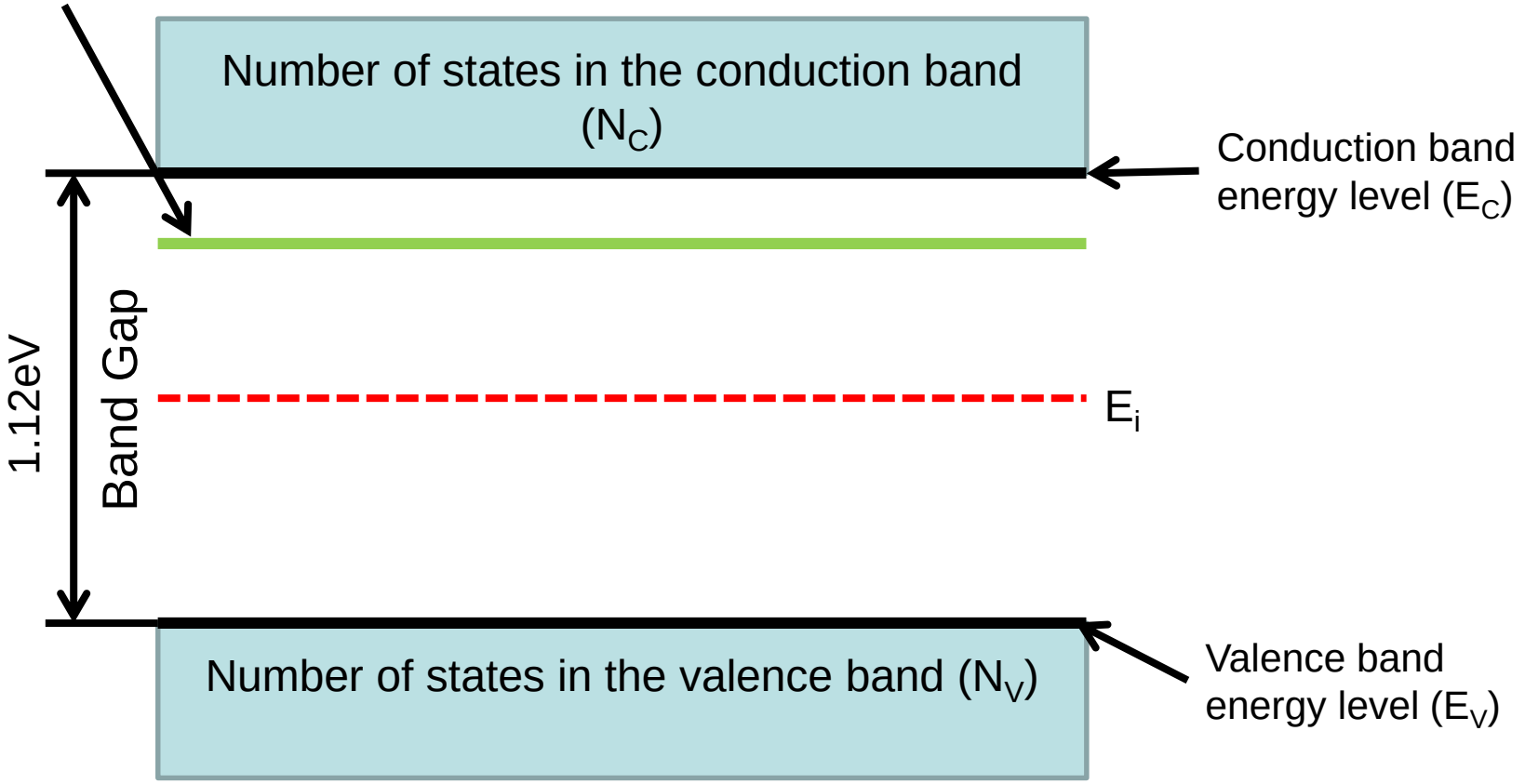
- Where:
  - E_f is the Fermi energy and is the energy level at which the probability of finding an electron in the conduction band is exactly 0.5

- If E_f <-3kT, i.e. the Fermi level lies sufficiently deep in the band gap, the semiconductor is said to be **non-degenerate**

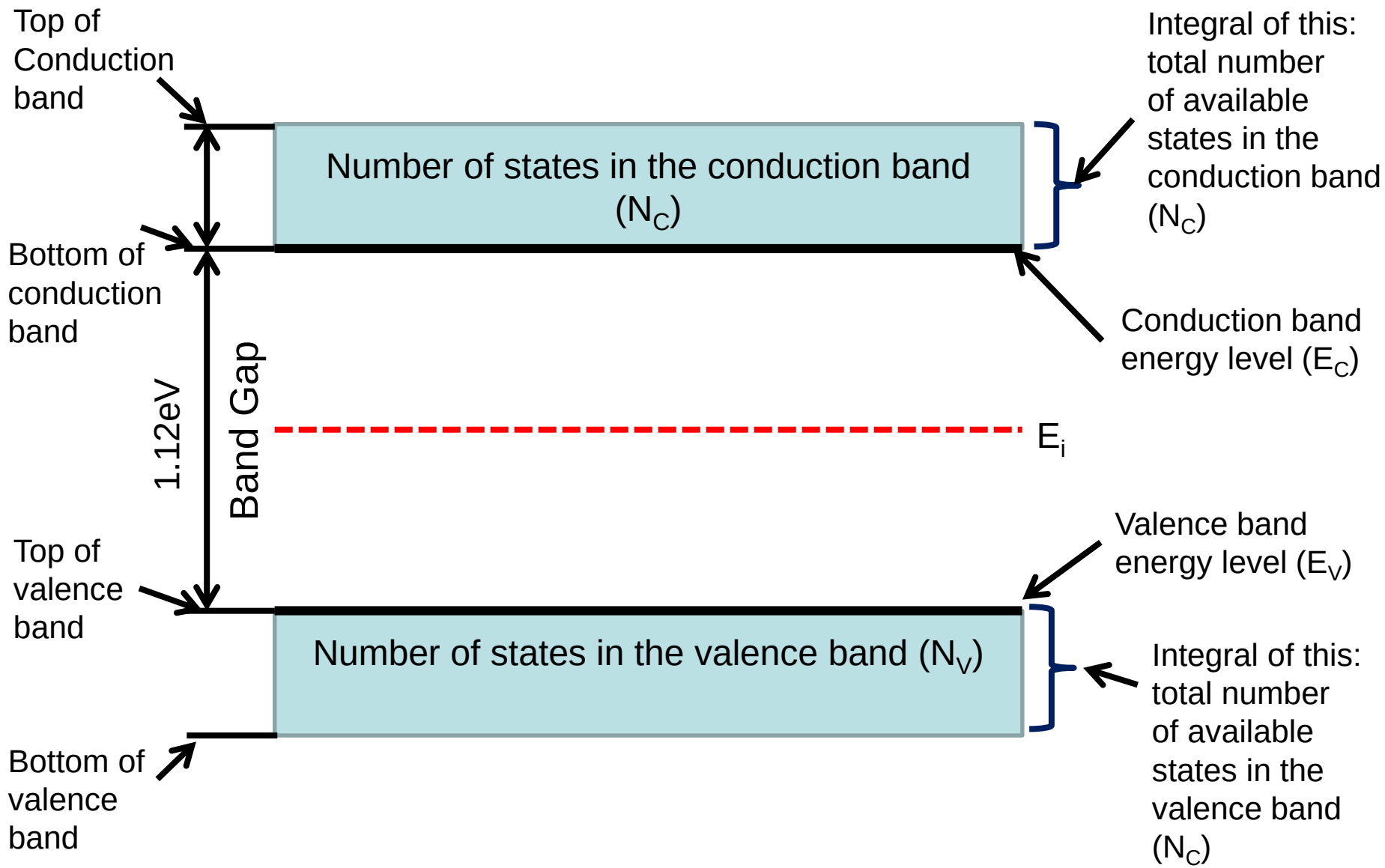
Semiconductor energy diagram: Fermi level

Fermi Energy Level (E_F)
When probability of finding an electron in the conduction band = 0.5

A Note on probability:
If probability = 0
Electron will exist in the valence band (bound state)
If probability = 1
Electron will exist in the Conduction band (free to move)
Probability = 0.5
Electron could be either in the conduction or valence band



Semiconductor energy diagram: Silicon number of states



- Combining equations 2 and 3 obtains

$$n = N_c \exp \frac{E_f}{kT}$$

- Referring to the bottom of the conduction band as Ec we obtain the electron and hole density in the conduction and valence bands:

$$\boldsymbol{n = N_C exp \frac{-(E_c - E_f)}{kT}} \qquad \boldsymbol{p = N_V exp \frac{-E_V - E_F}{kT}}$$

- Where N_C and N_V is the effective density of sates

$$\boldsymbol{N_c \equiv 2\left(\frac{2\pi m_e\, kT}{h^2}\right)^{3/2}} \qquad \boldsymbol{N_v \equiv 2\left(\frac{2\pi m_h\, kT}{h^2}\right)^{3/2}}$$

- For Silicon the temperature dependence of the density of states can be simplified to:

$$N_C = 4.83x10^{21}T^{\frac{3}{2}} \qquad N_V = 1.71x10^{21}T^{\frac{3}{2}}$$

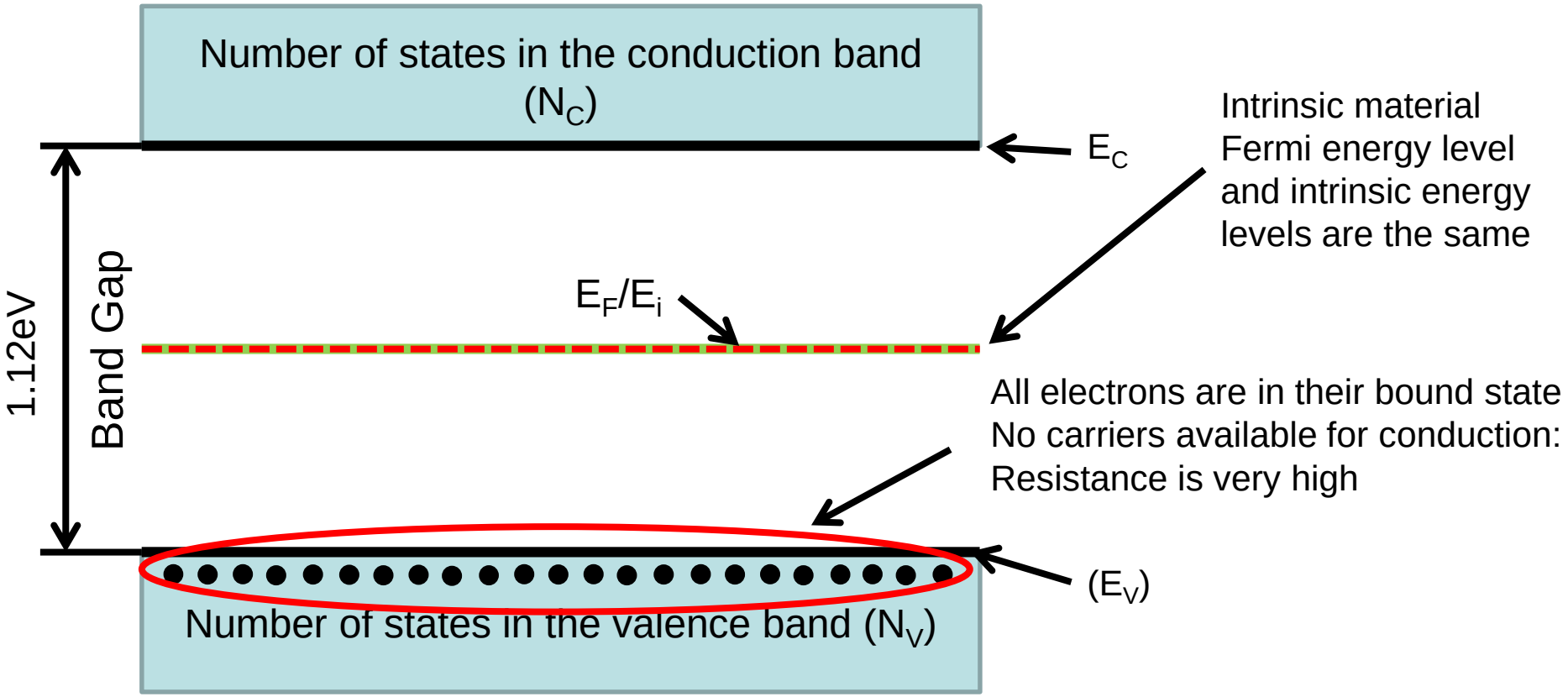
- Product of electron and hole concentrations is independent of Fermi level position and depends upon temperature and band structure

$$np = N_v N_c exp \frac{-E_G}{kT} = {n_i}^2$$

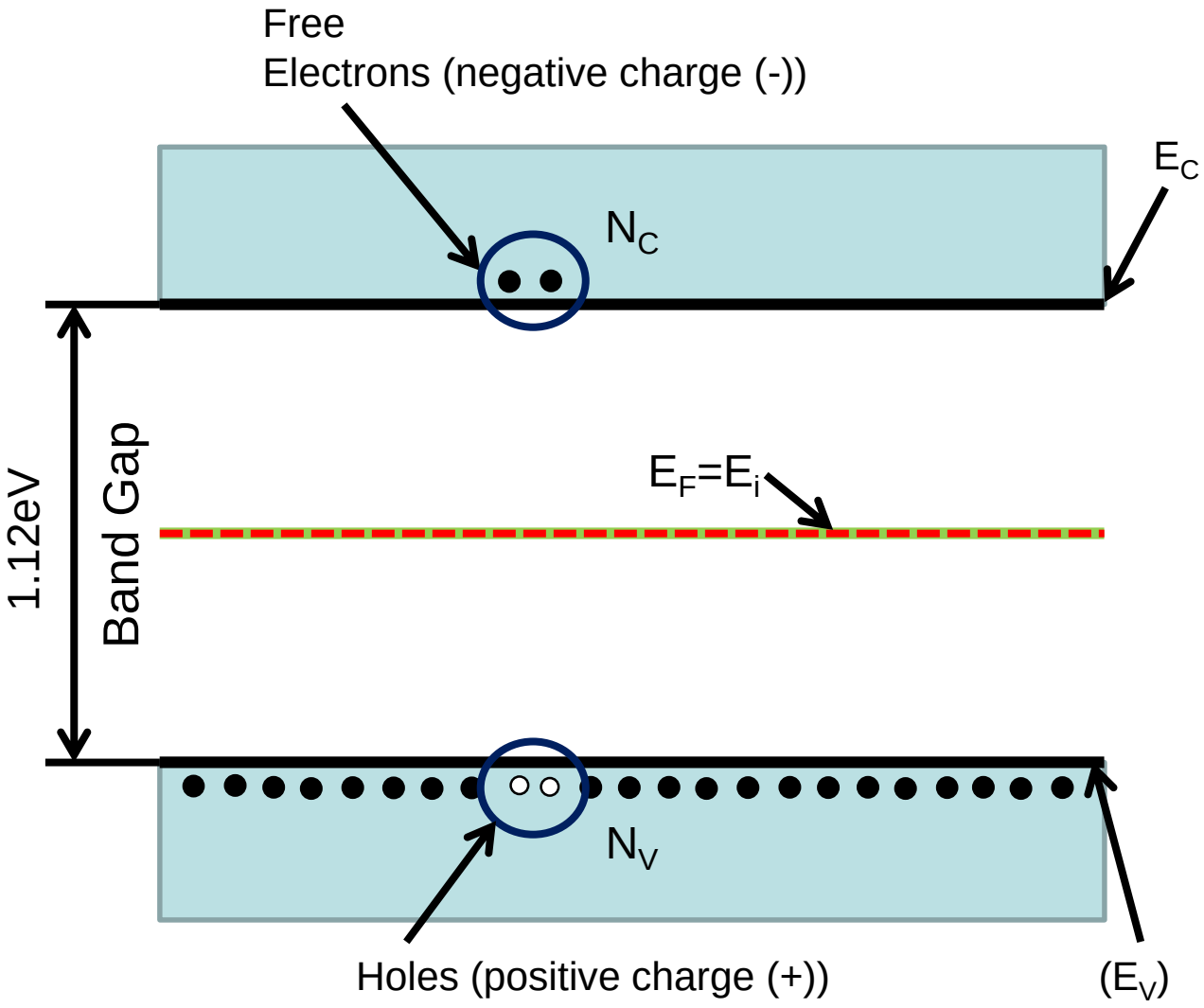
- n_i is known as the intrinsic carrier concentration
  - Carrier concentration in a semiconductor with no impurities or defects
- As band gap energy decrease with increasing temperature, for silicon the variation of intrinsic carrier concentration with temperature can be simplified to:

$$n_i = 3.86x10^{23} T^{\frac{3}{2}} \exp\left(\frac{T}{565} - \frac{6838}{T}\right)$$

Recap: Semiconductor energy diagram: Intrinsic Silicon 0 Kelvin



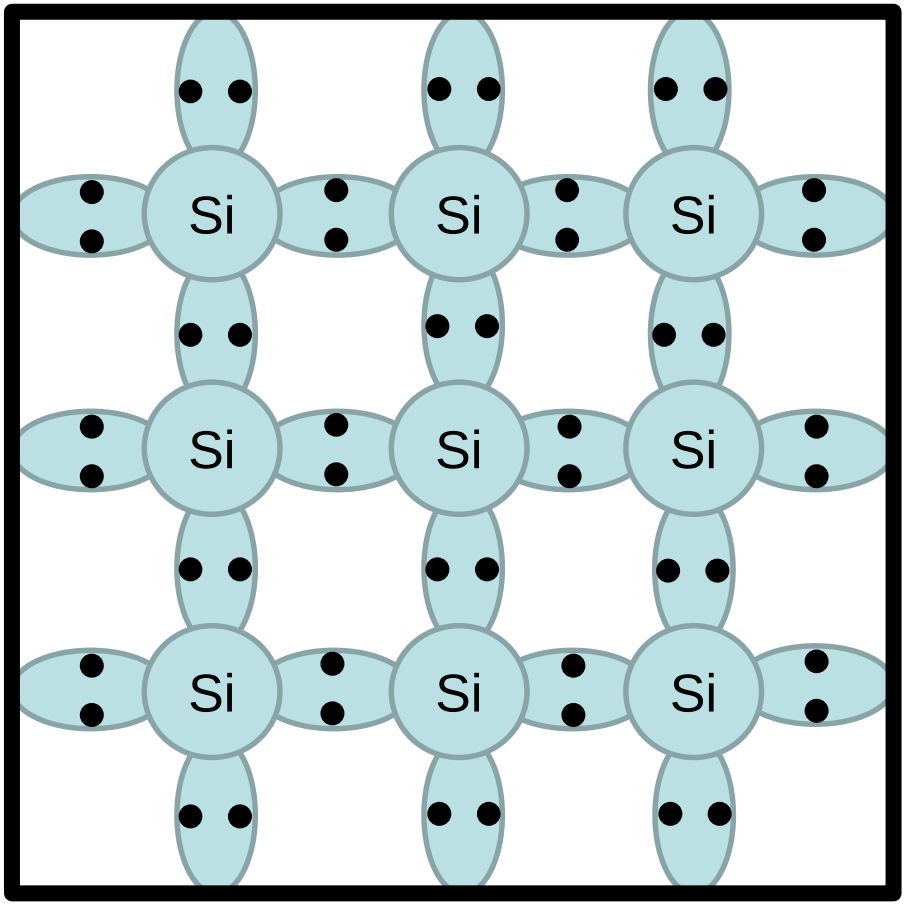
Semiconductor energy diagram: Intrinsic Silicon T > 0 Kelvin



- Temperature is greater than 0 Kelvin
- Carriers have enough energy to overcome the band gap and enter into the conduction band
- Electrons entering the conduction band leave holes in the valence band (positive charge)
- These electrons and holes are now free to move under the influence of a bias
- Therefore resistance reduces with temperature

Basic bond representation of intrinsic silicon

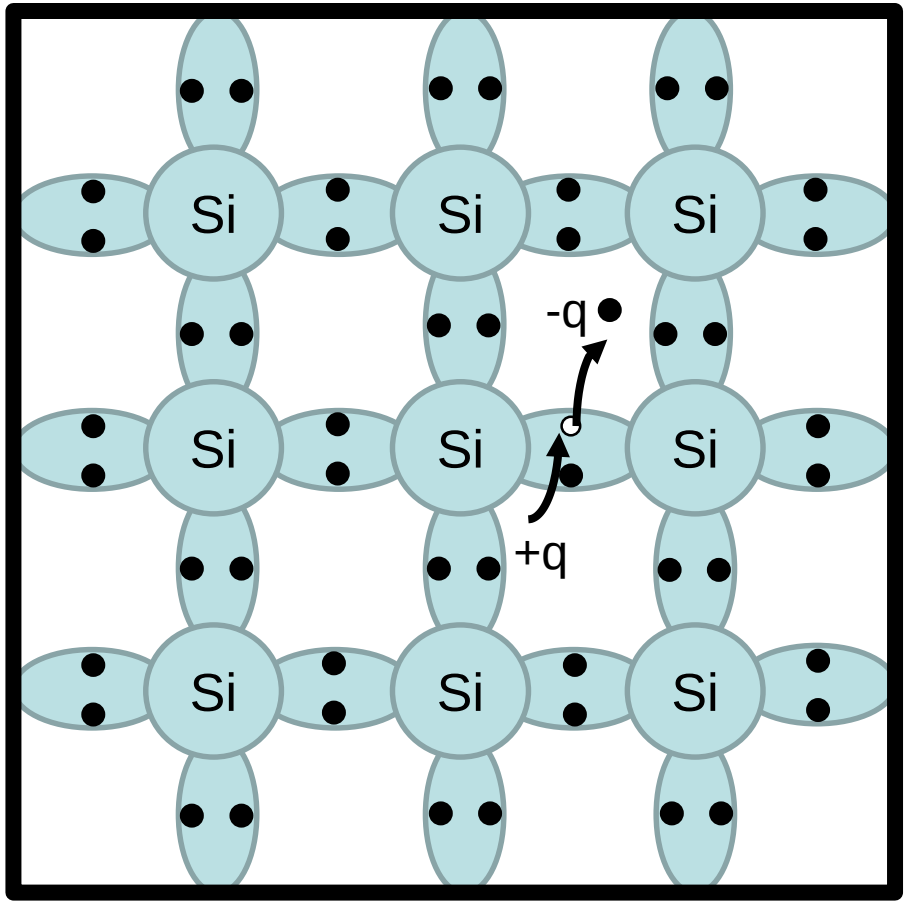
Silicon at zero Kelvin



All electrons in the bound state

Intrinsic carrier concentration (ni) = 0

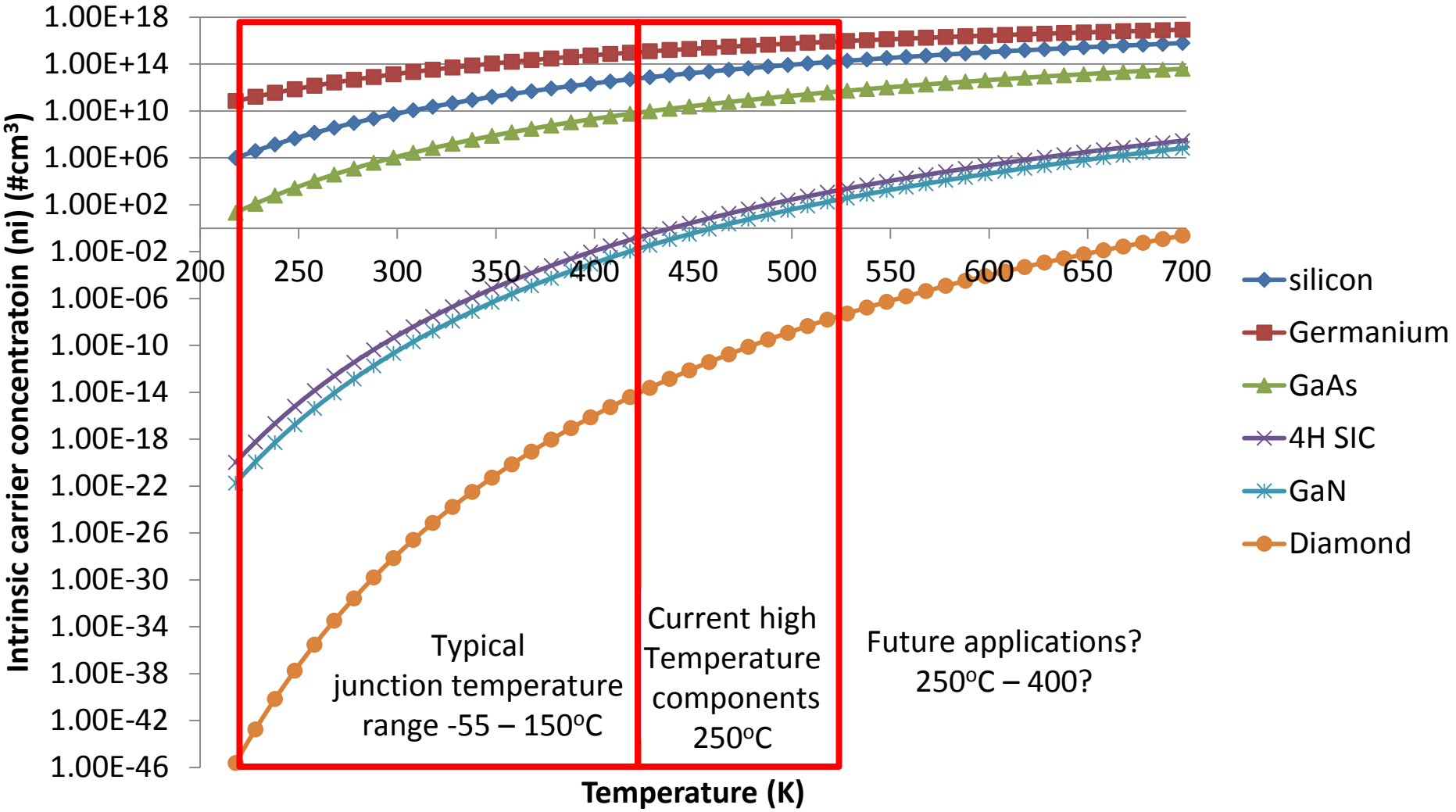
Silicon at room temperature



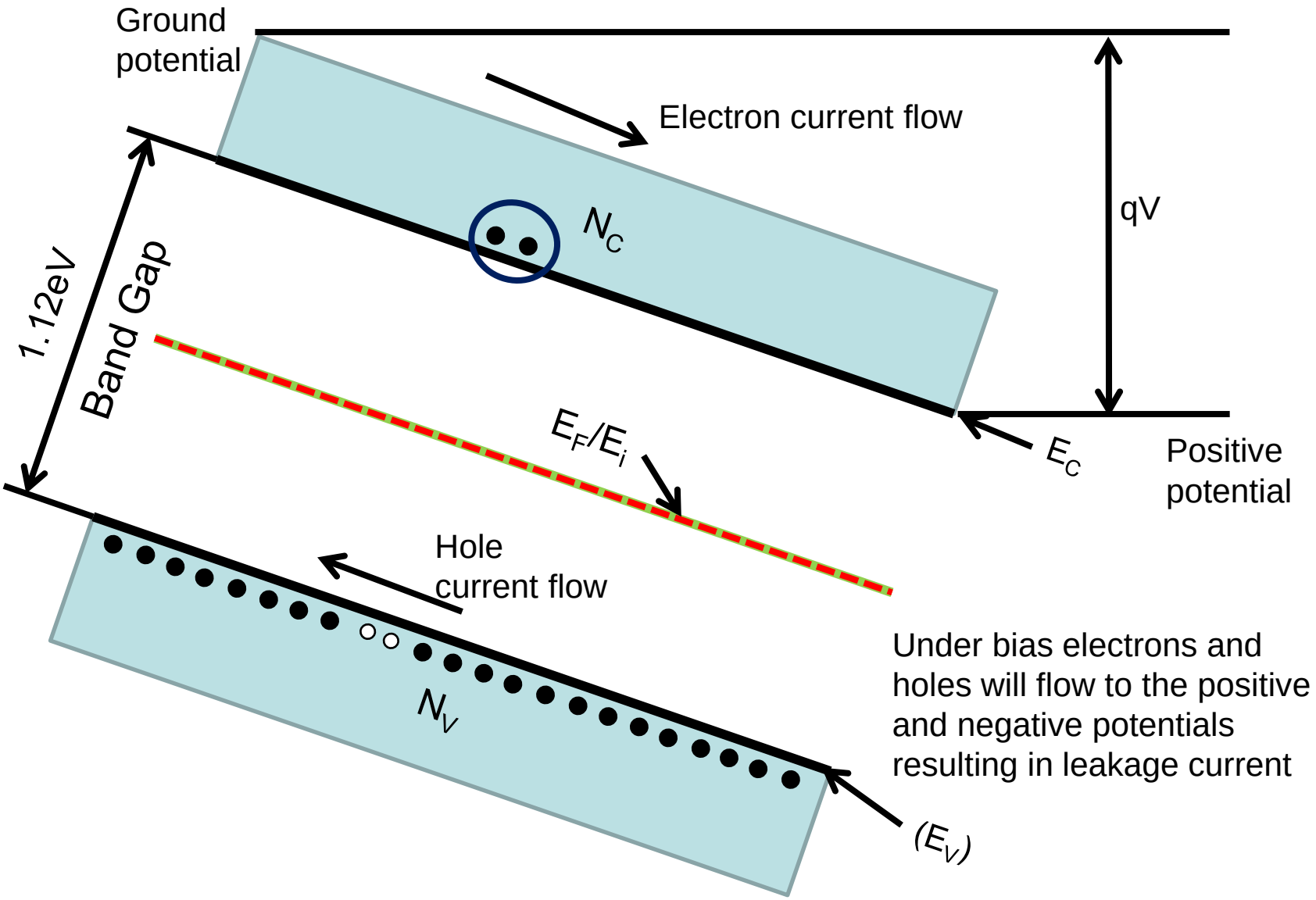
Energy generated an electron hole pair

n_i~ 1e10 # / cm^3

Intrinsic carrier concentration vs temperature (-55 – 430°C)



Semiconductor energy diagram: Intrinsic Silicon under bias

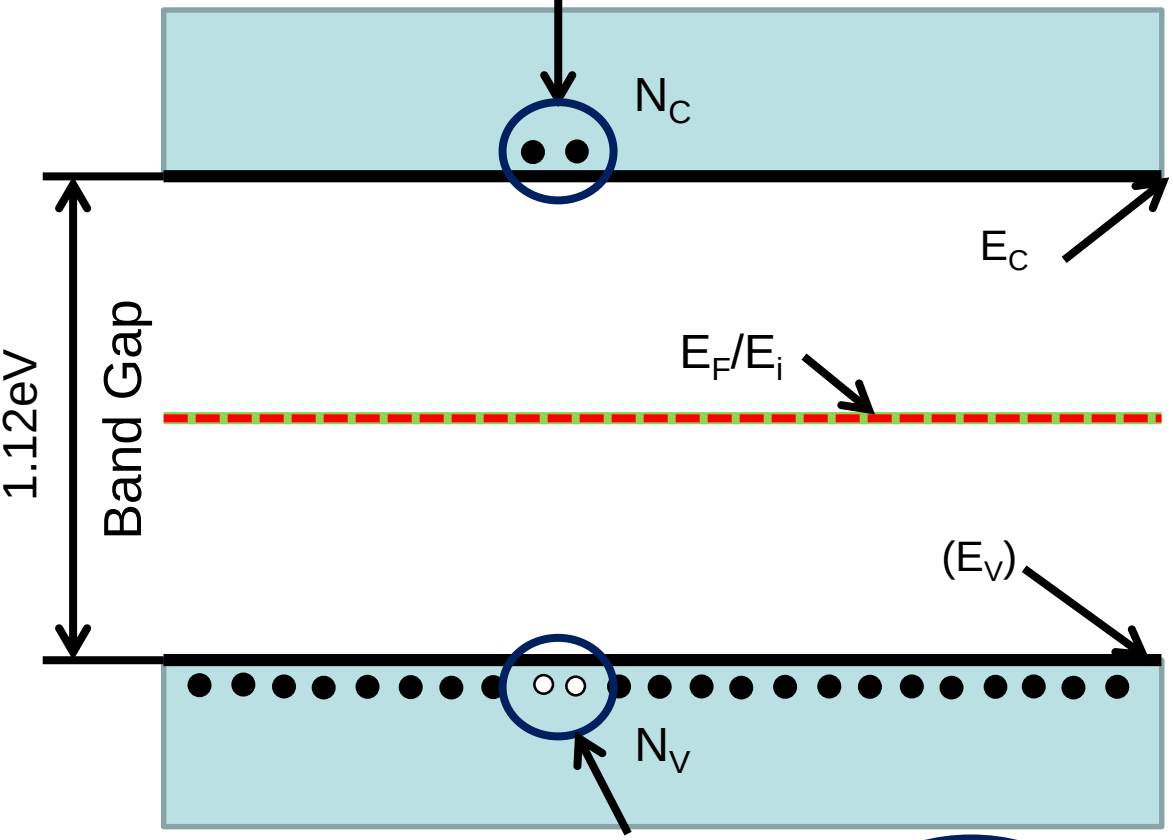


Semiconductor energy diagram: number of free carriers

$$number\ of\ free\ electrons\ (n) = N_C exp\frac{-(E_c - E_f)}{kT}$$

Density of available states

Probability of finding an electron



As semiconductor is intrinsic:

$$np = N_v N_c exp\frac{-E_G}{kT} = {n_i}^2$$

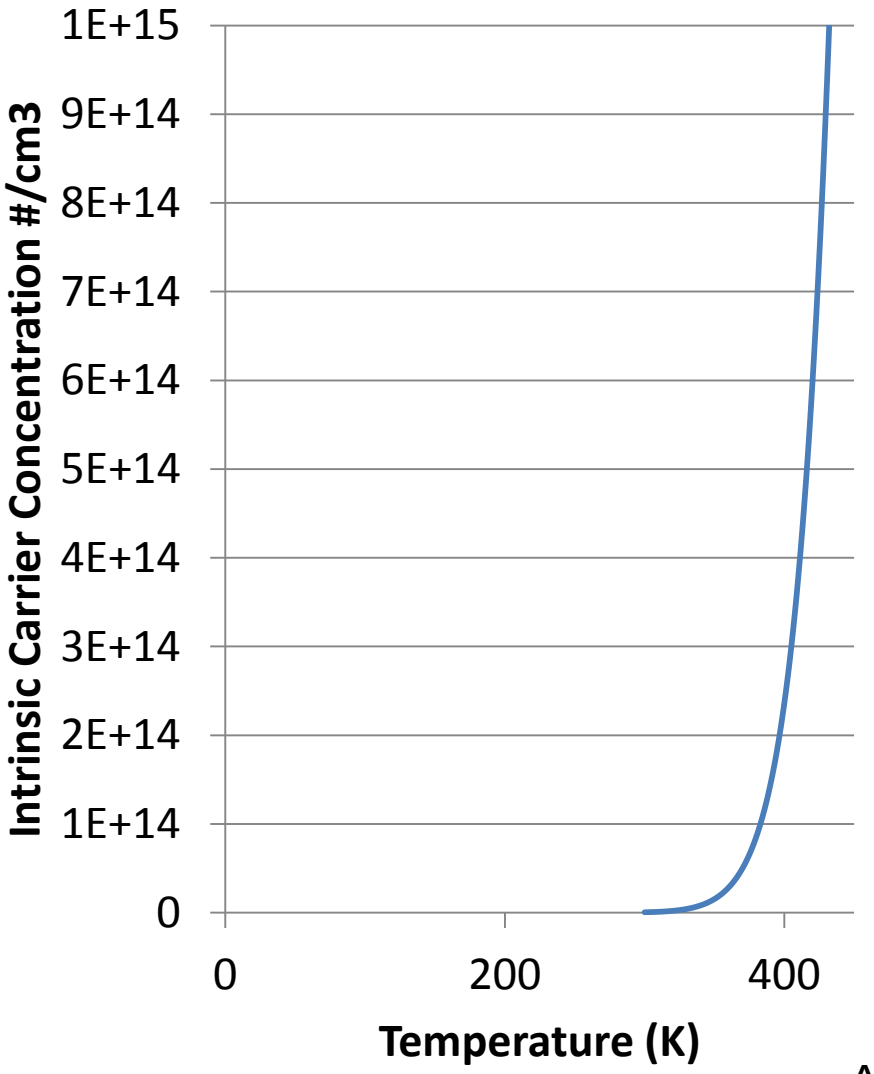
n_i is the **intrinsic carrier** concentration
i.e. the **number** of electron and holes available to conduct current in an intrinsic semiconductor

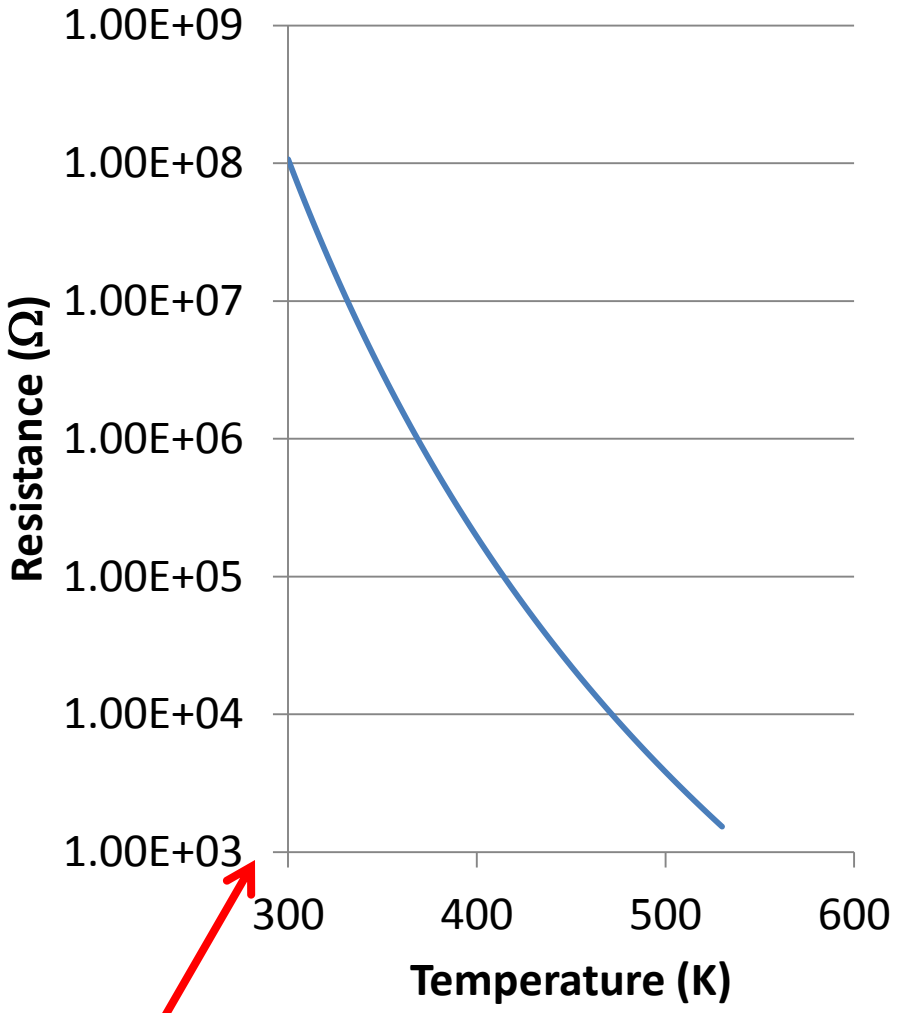
$$Number\ f\ free\ holes\ (p) = N_V exp\frac{-E_V - E_F}{kT}$$

Density of available states

Probability of finding a hole

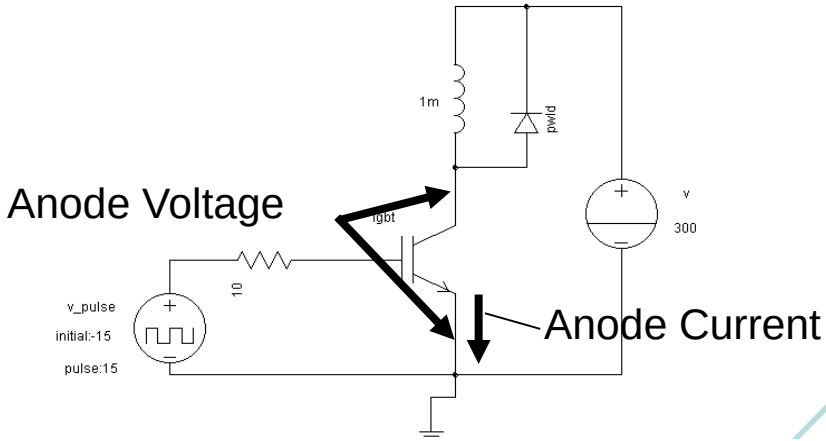
Intrinsic carrier concentration vs temperature in Silicon



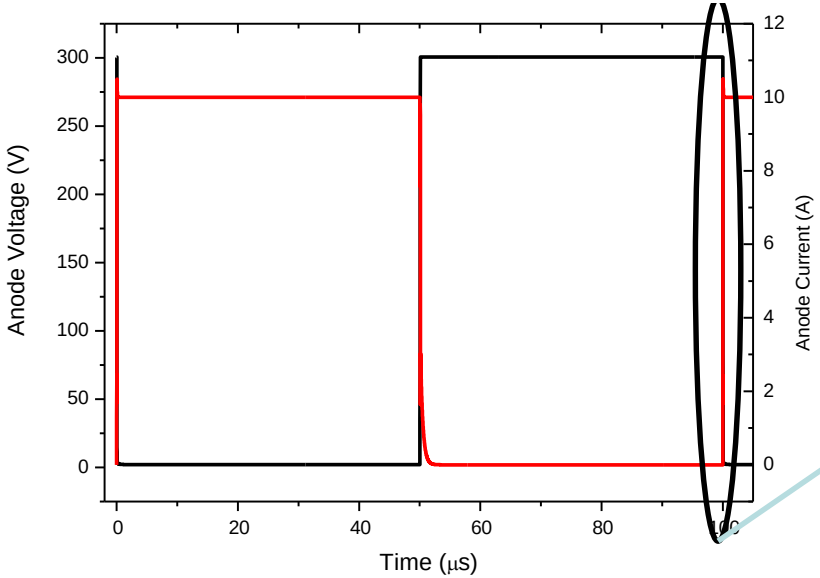


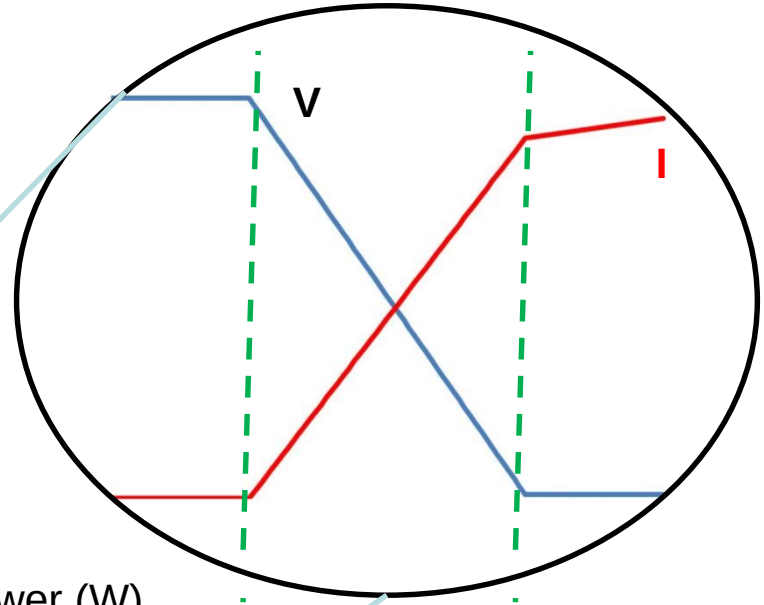
Assuming a 5x5mm die and length of 500μm

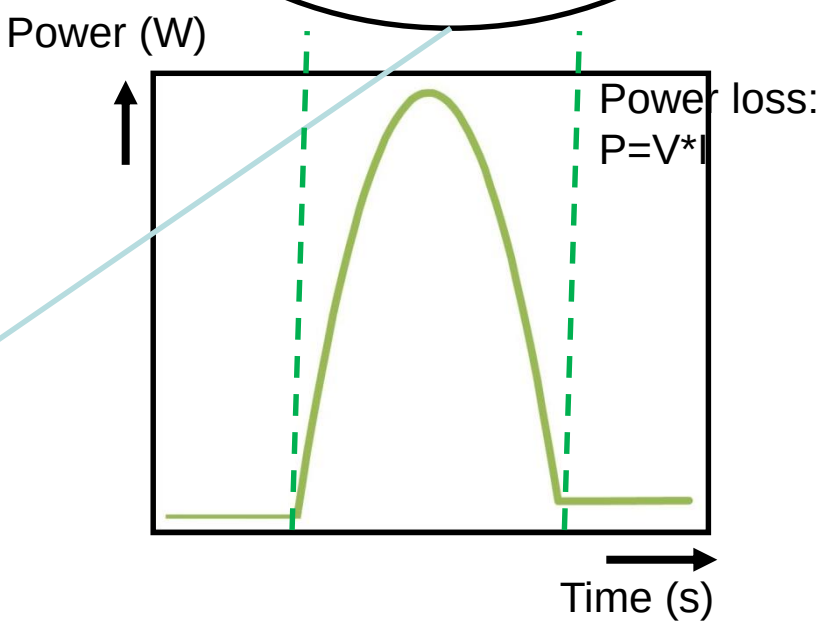
Semiconductor Power Loss: 10A 400V Chopper



Typical IGBT Current/Voltage Waveforms at 10kHz







Instantaneous Power Loss: Per Cycle

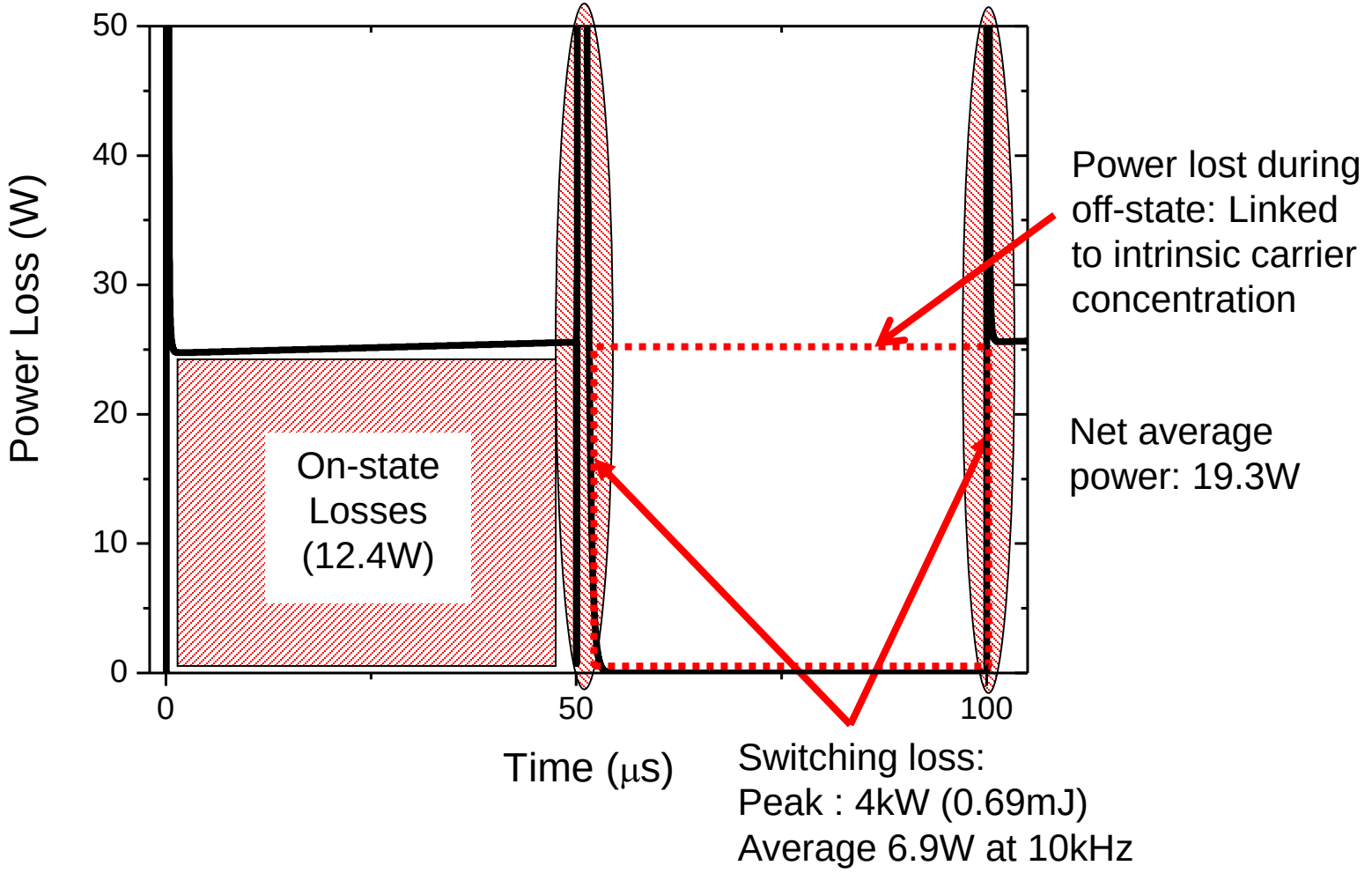
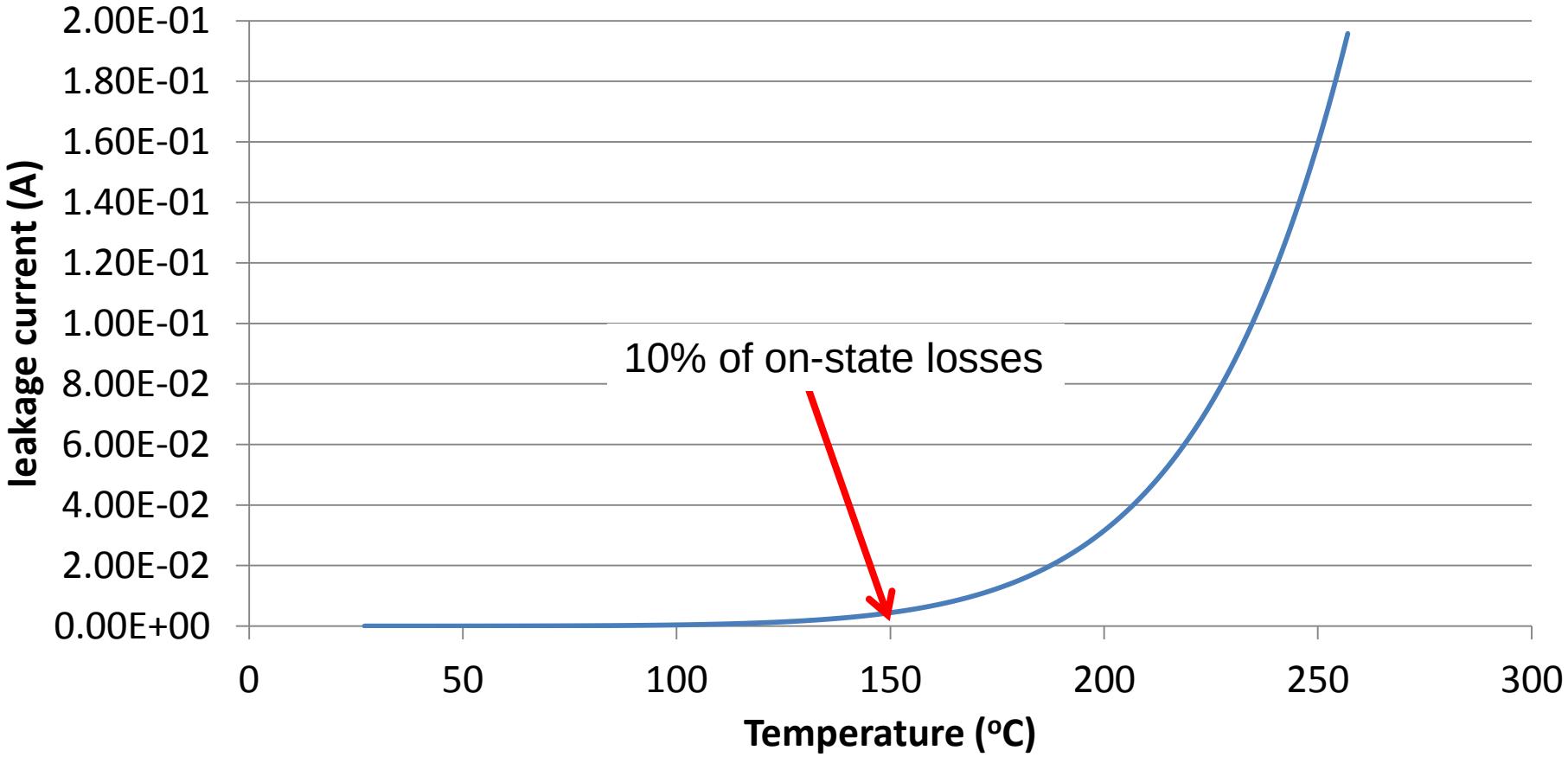


***Figure cropped to highlight on-state losses

Leakage current at 300V



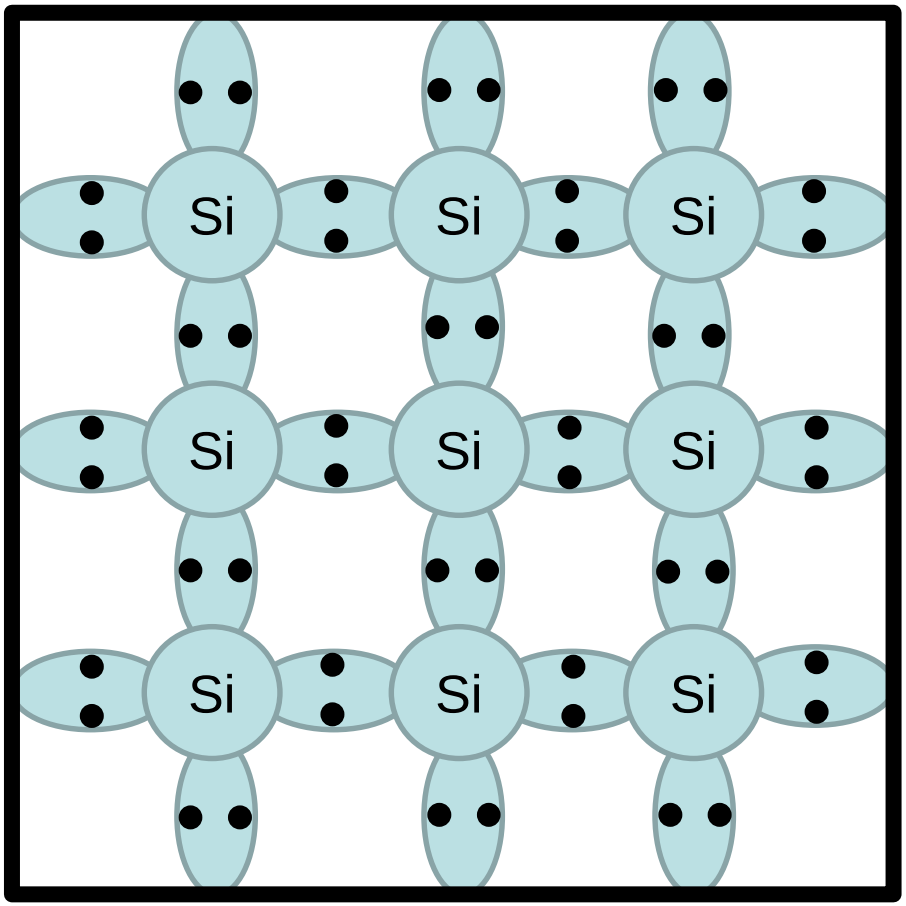
- As intrinsic carrier concentration is reached, leakage current increases exponentially causing more power loss:- results in higher junction temperature
- Positive feedback mechanism as leakage current is related to temperature
- Termed: Thermal runaway

Donors and Acceptors

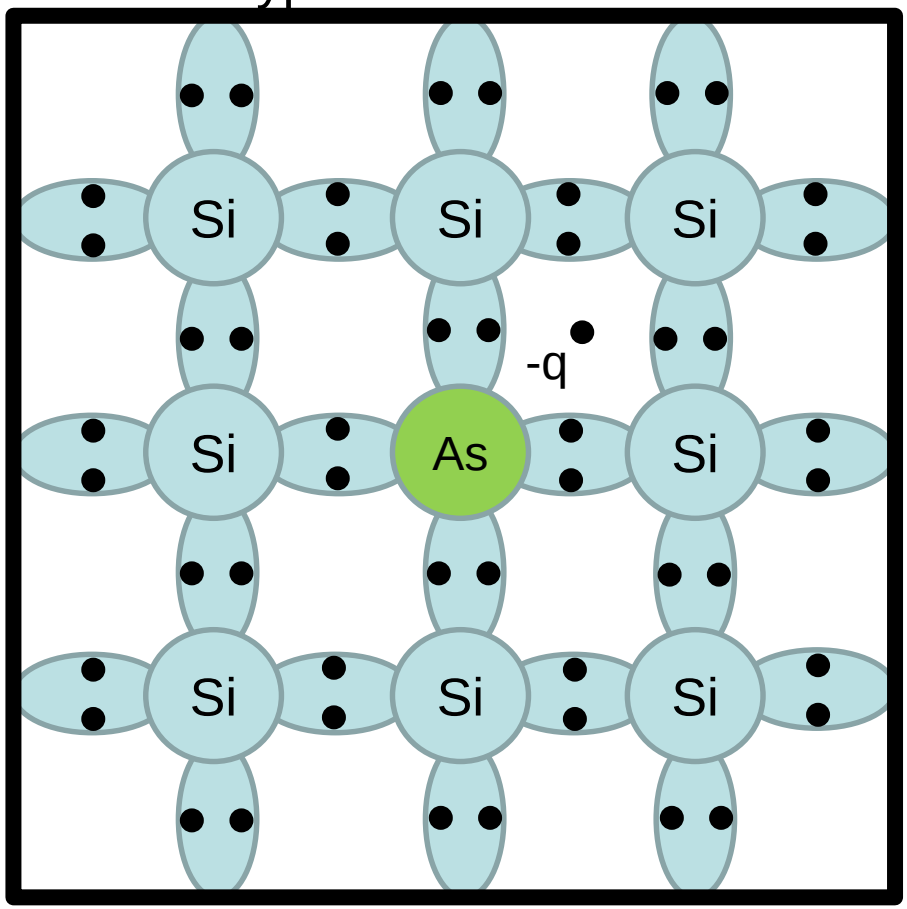
- When semiconductor is doped with impurities is becomes extrinsic and impurity levels are introduced into the band structure
  - Generally performed by ion implantation followed by a diffusion (heat treatment) to activate implanted impurities
- Dopants are characterised into two types
  - Donors in Silicon: elements which donate electrons into the band structure; Phosphorous, Arsenic, Antimony
    - Creates n type material
  - Acceptors in Silicon: elements which donate holes into the band structure; Boron, Aluminium, Gallium
    - Creates p type material
- Device technologies, or technology node, are built around precise control of these n type and p type dopants to form structures:
  - This theory is applicable in Silicon and Silicon Carbide.

Intrinsic silicon (G4) and n type (Arsenic (G5) doped)

Intrinsic silicon

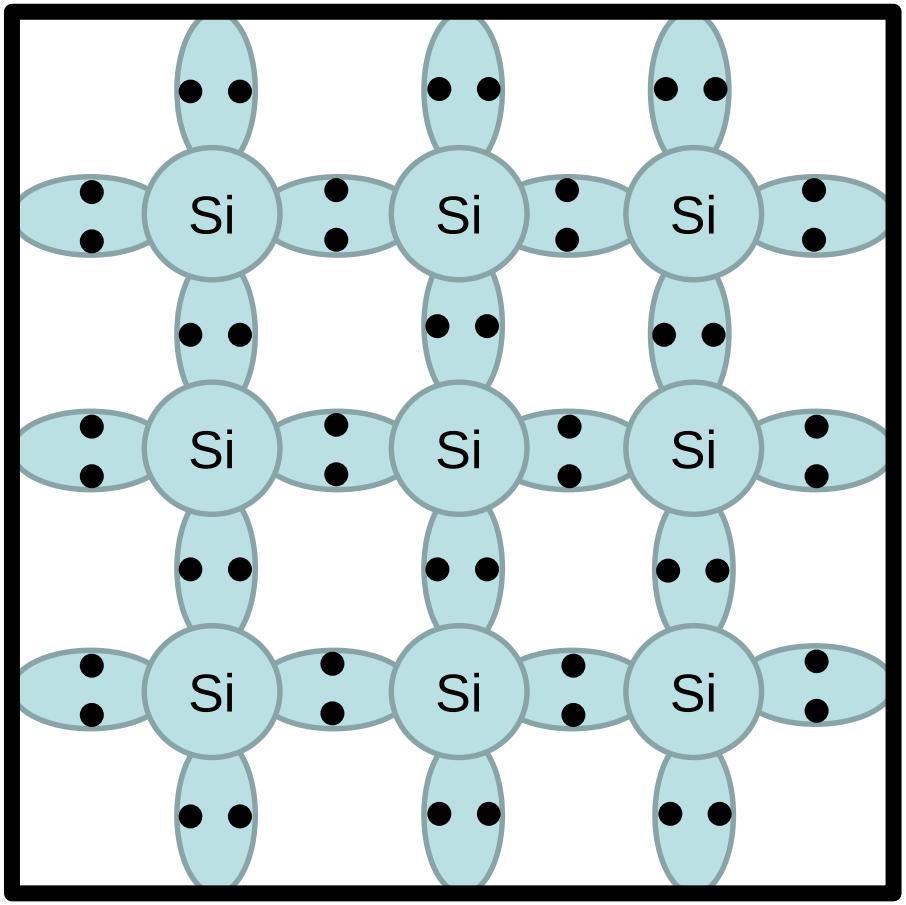


N type silicon

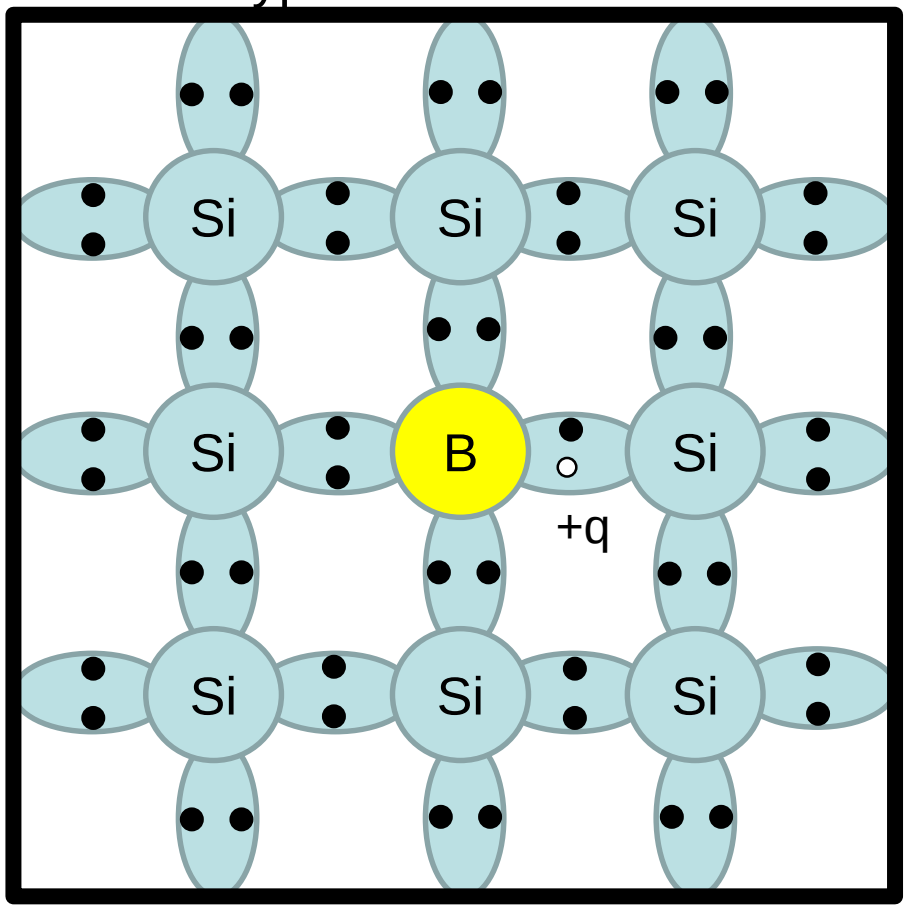


Intrinsic silicon (G4) and p type (Boron (G3) doped)

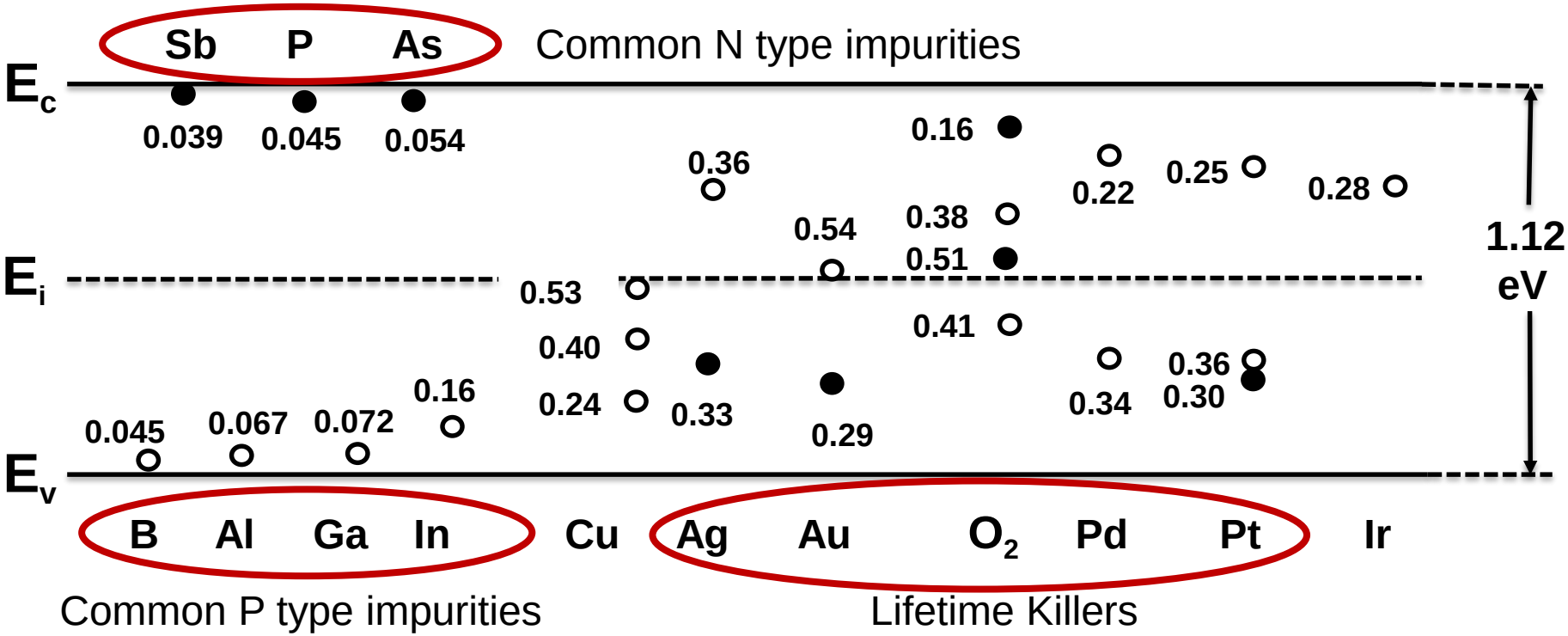
Intrinsic silicon



P type silicon

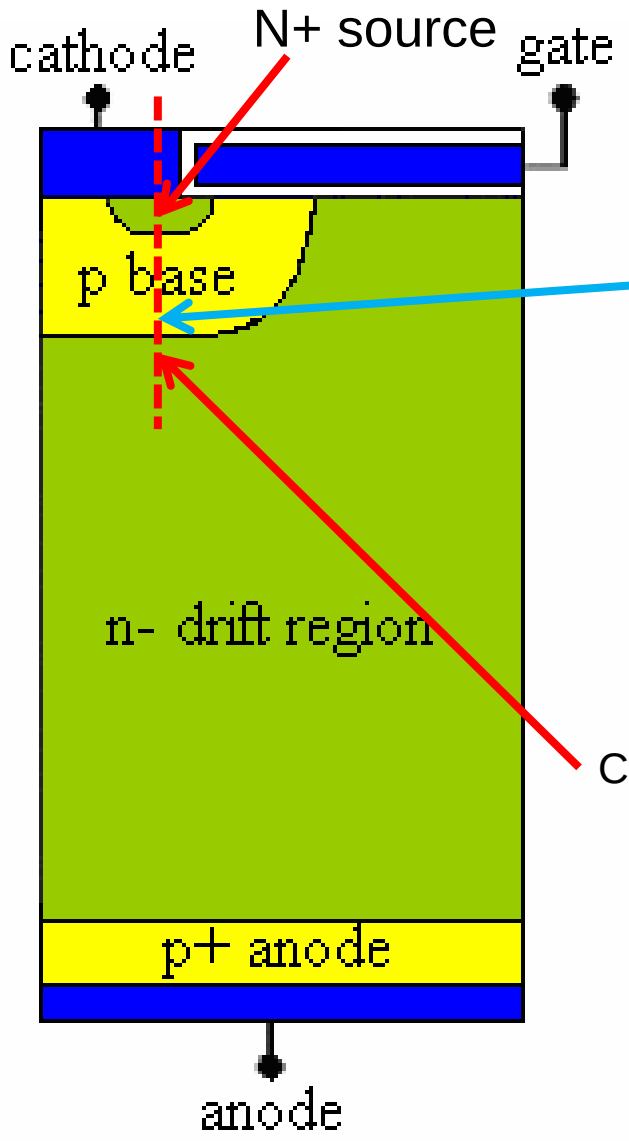


Common impurity trap levels in silicon



- Generally Boron and Phosphorous are the most common p and n type impurities
- For shallow n+ junctions, Arsenic is used due to its reduced diffusion coefficient compared to phosphorous
- Lifetime killers are avoided in fabrication foundries: seen as contaminants
  - Lifetime killing performed post process by electron or proton irradiation

Heavy v. light impurity dopants: Practical example (planar IGBT)

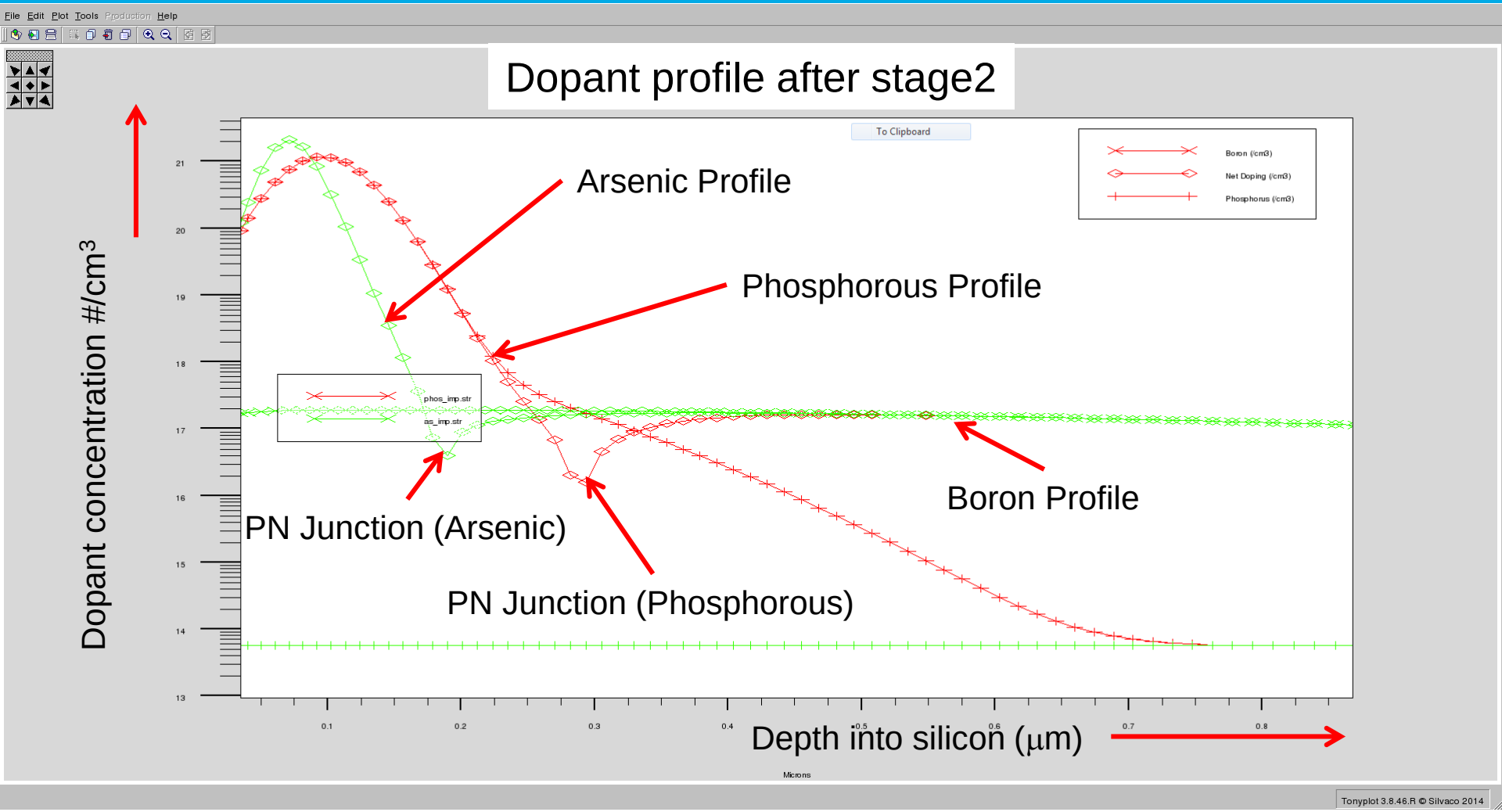


- **N+ junction critical design feature**
- Needs high concentrations: low contact resistance
- Shallow junction depth: maintaining pbase profile

Simplified IGBT N+ source process flow

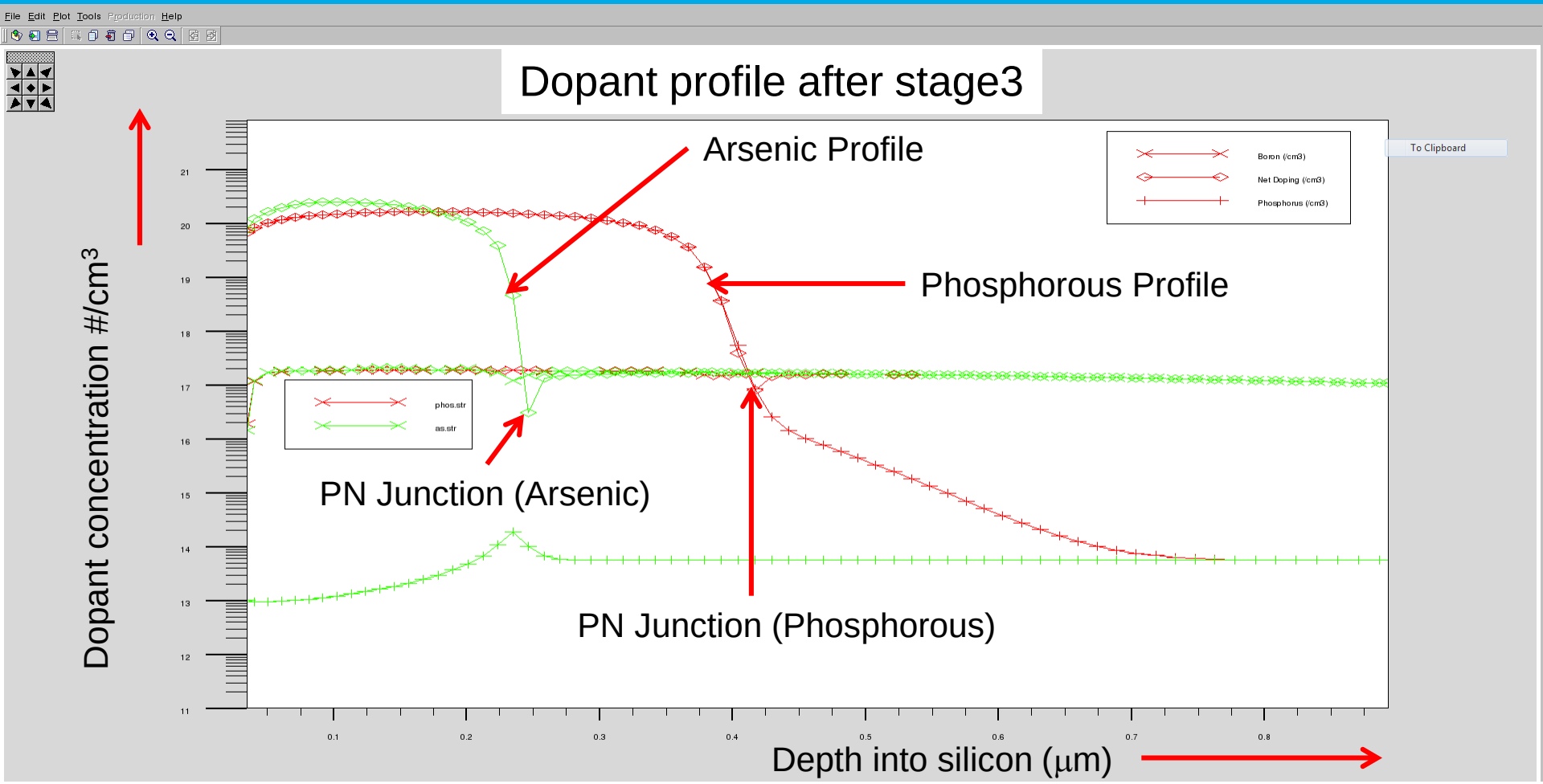
- Process starts with n- bulk wafer (N_D=5e13 atoms/cm^3 (phosphorous))
- Stage1 : p base implantation and anneal
  - Pbase implantation: species= Boron, Dose=2e13 atoms/cm^2: energy=50keV
  - Pbase anneal: 50mins at 1190^{o}C
- Stage2: n+ source implantation
  - Wafer implanted with arsenic or phosphorous: 8e15 atoms/cm^2: energy=50keV
- Stage3: n+ source activation
  - Wafer annealed for 30min at 950^{o}C to activate impurities

Comparison of implantation profile: Arsenic vs. Phosphorous



- Cross-section through sample to 0.9μm after Stage2 (n+ source implantation)
- Stage2:
  - Samples implanted with arsenic/phosphorous: 8e15 atoms/cm^2: energy=50keV

Junctions after activation anneal (30mins at 950°C)



- After 30 min implant activation anneal: causing impurity to bond with Silicon atoms
- Heavier atom (Arsenic) provides the shallow junction improving device performance
- If a deep junction was required: Phosphorous would be selected at the junction can be achieved with a reduced furnace anneal time

Impurity trap levels and Fermi level

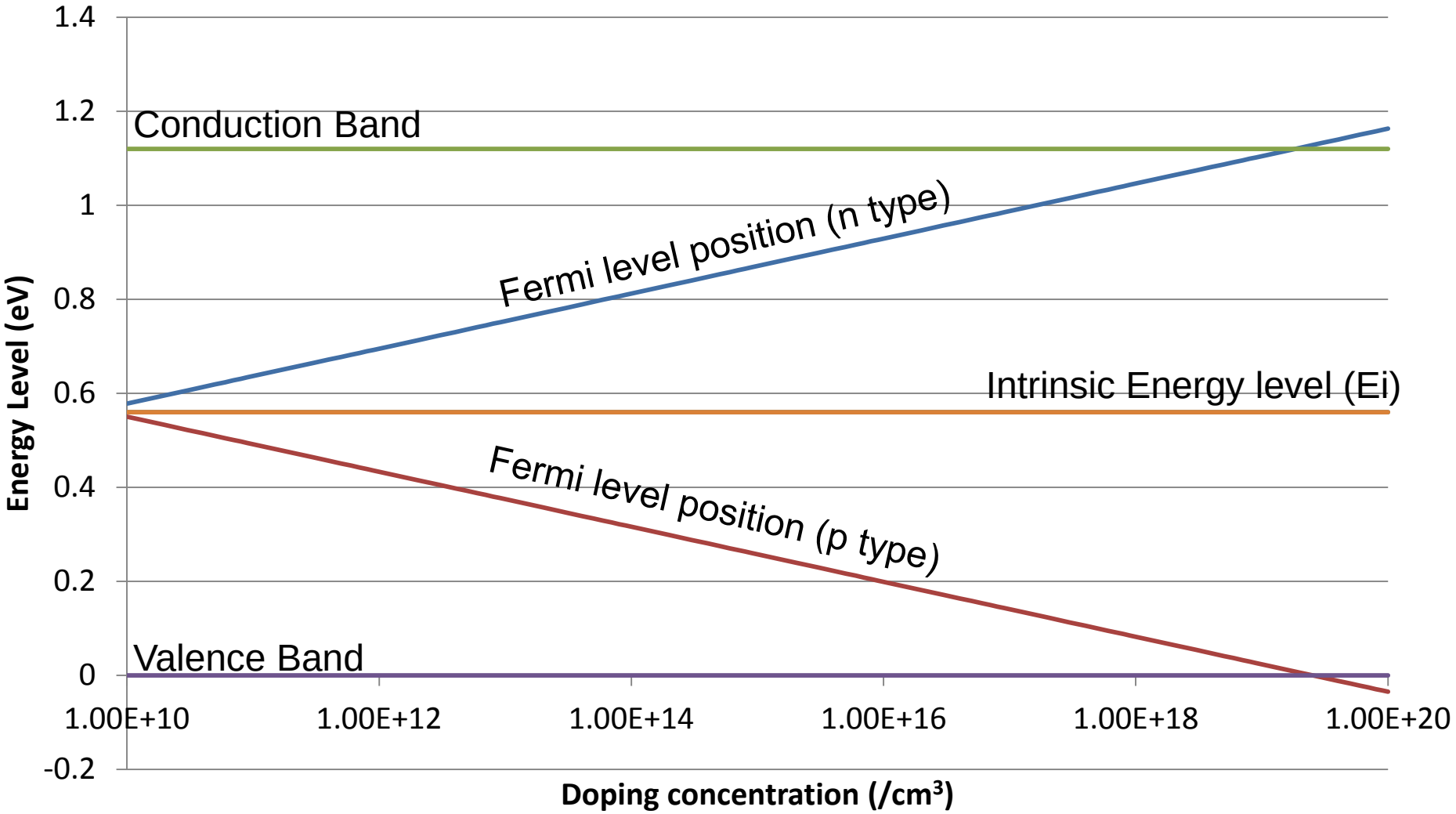
- For shallow donors or acceptors in silicon there is usually sufficient thermal energy to ionize all impurities at room temperature and supply the same number of electrons to the conduction band or holes to the valence bands
  - **Termed complete ionisation**
- Under this condition we can write the electron density in the conduction band or hole density in the valence band as:

$$n = N_D \qquad p = N_A$$

- Combining this condition with: $n = N_C exp \frac{-(E_c - E_f)}{kT}$
- Obtains the Fermi level in terms of the effective density of states and impurity concentration:

n type semiconductor	*p type semiconductor*
$E_c - E_F = kT\ ln\left(\frac{N_C}{N_D}\right)$	$E_F - E_V = kT\ ln\left(\frac{N_V}{N_A}\right)$

Influence of doping concentration upon Fermi level (Si)



- Intrinsic energy level is often used as the energy reference:
- From:

$$n = N_c exp\left[\frac{-(E_C - E_F)}{kT}\right]$$

$$n = N_c exp\left[\frac{-(E_C - E_i)}{kT}\right] exp\left[\frac{(E_F - E_i)}{kT}\right]$$

- Due to the mass action law:

$$\boldsymbol{np = n_i{}^2 = N_V\, N_c exp\left[\frac{-(E_C - E_V)}{kT}\right]}\; n_i = N_c exp\left[\frac{-(E_C - E_i)}{kT}\right]$$

- Electron/hole free carrier concentrations are determined by:

$$\boldsymbol{n = n_i\, exp\left[\frac{(E_F - E_i)}{kT}\right]} \qquad \boldsymbol{p = n_i\, exp\left[\frac{(E_i - E_F)}{kT}\right]}$$

- This is a convenient way of referring to electron and hole concentrations

Example calculation#1: Fermi level position n type semiconductor

Silicon ingot with 1e17 Arsenic atoms/cm^3

Find the Fermi level at room temperature: assuming an intrinsic carrier concentration of 9.65e9 atoms/cm^3

$n \approx N_D = 10^{17}$ /cm^3

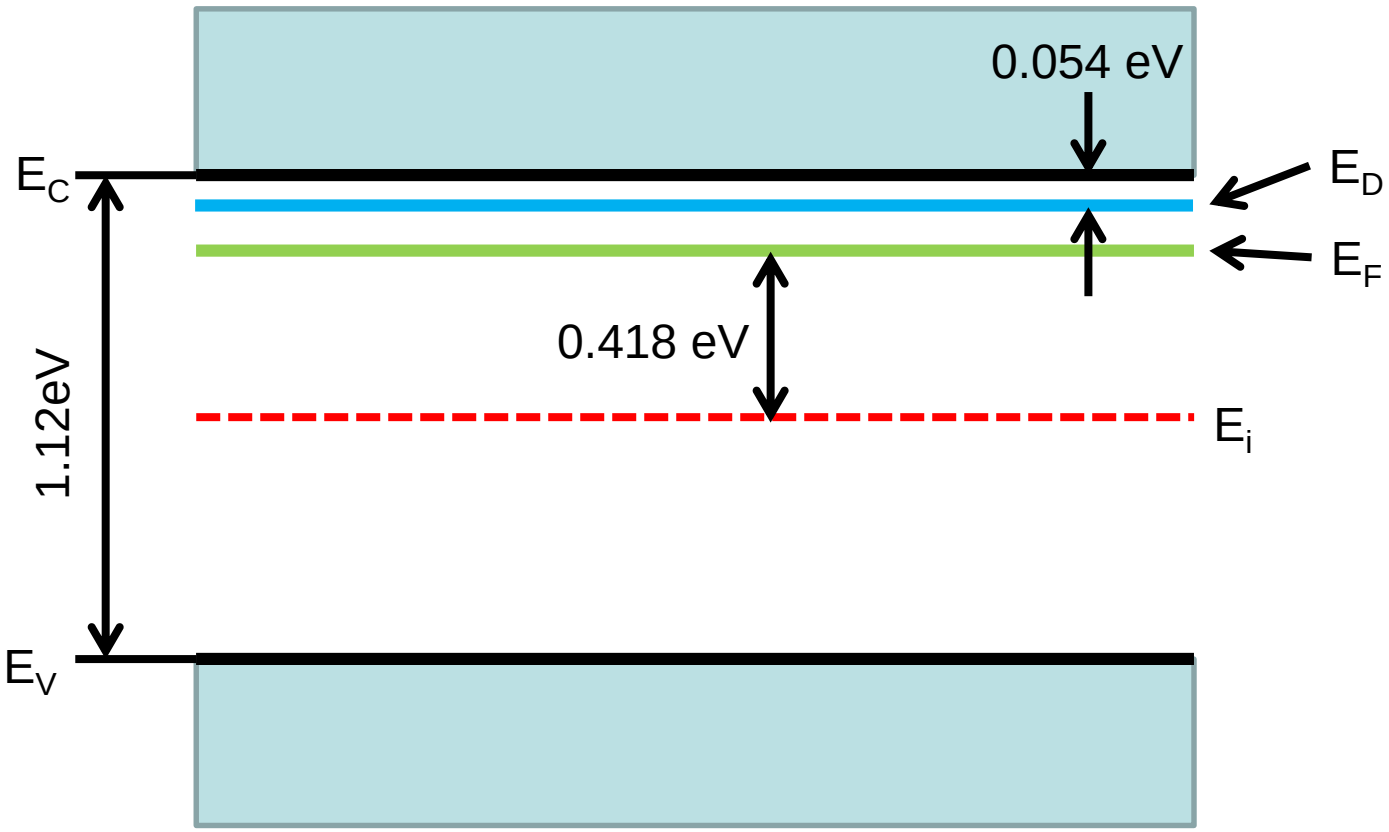
From mass action law the minority carrier concentration can be determined:

$$n \approx \frac{{n_i}^2}{N_D} = \frac{(9.65 \times 10^9)^2}{10^{17}} = 0.931 \times 10^3 \; cm^{-3}$$

Fermi level measured from the intrinsic energy level:

$$E_F - E_i = kT \ln\left(\frac{N_D}{n_i}\right) = 0.0259 \ln\left(\frac{10^{17}}{9.65 \times 10^9}\right) = 0.418\text{eV}$$

Example #1 Band diagram



Example calculation#2: Fermi level position

Silicon ingot with 1e15 Boron atoms/cm3

Find the Fermi level at room temperature: assuming an intrinsic carrier concentration of 9.65e9 atoms/cm^3

$$p \approx N_A = 10^{15}$$

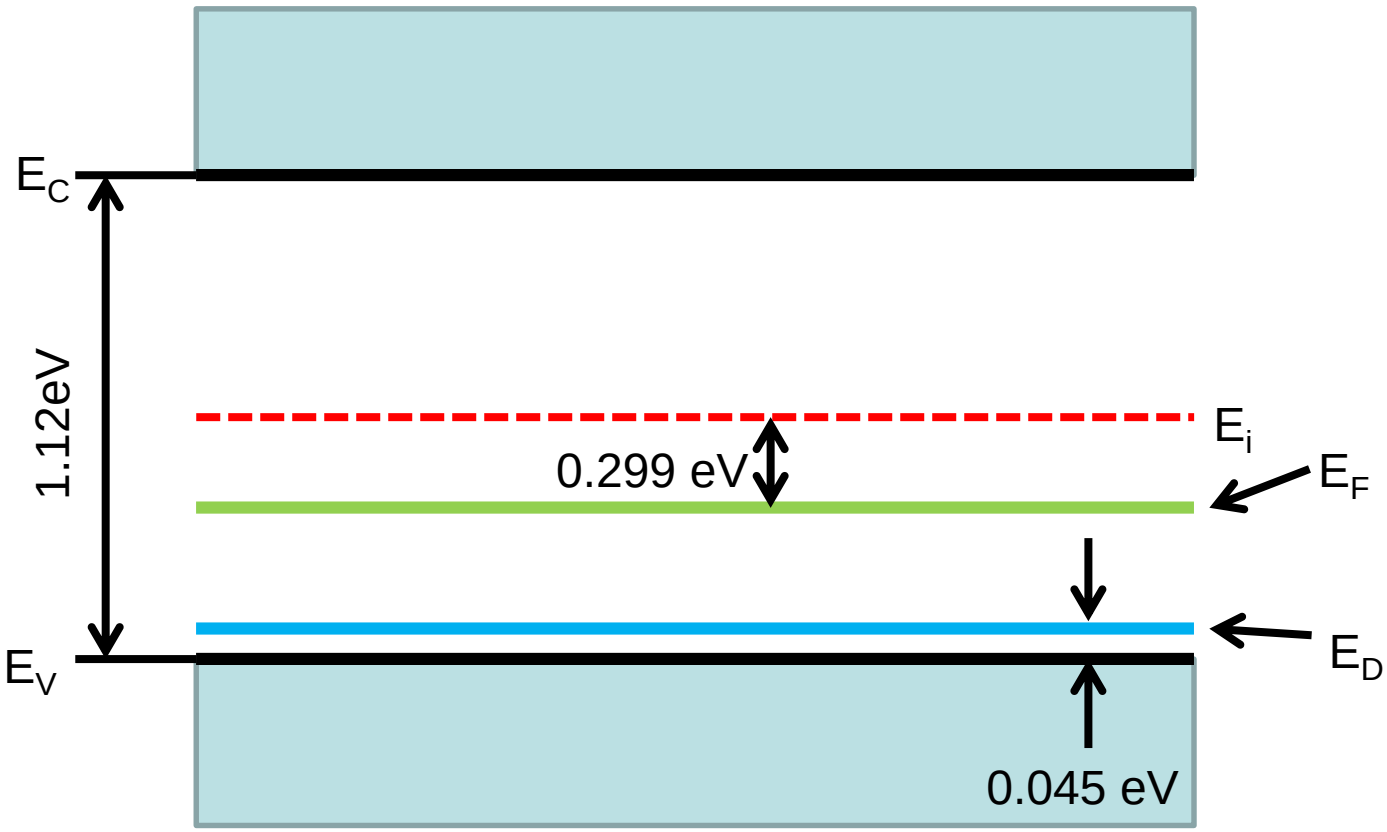
From mass action law the minority carrier concentration can be determined:

$$p \approx \frac{{n_i}^2}{N_A} = \frac{(9.65 \times 10^9)^2}{10^{15}} = 93.2 \times 10^3 \; cm^{-3}$$

Fermi level measured from the intrinsic energy level:

$$E_i - E_F = kT \ln\left(\frac{N_A}{n_i}\right) = 0.0259 \ln\left(\frac{10^{15}}{9.65 \times 10^9}\right) = 0.299\text{eV}$$

Example #2 Band diagram

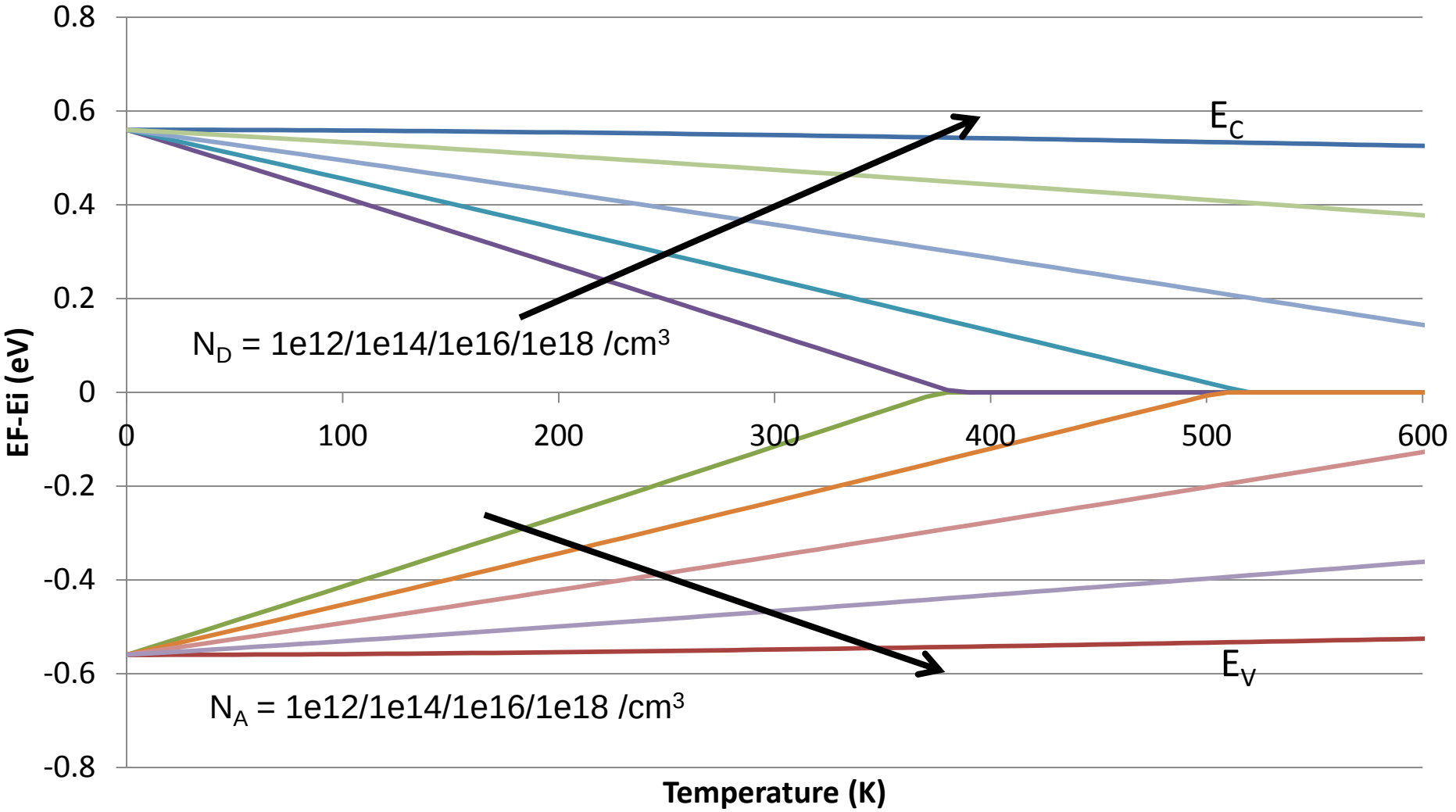


Band gap Narrowing

- Generally the magnitude of net impurity concentration exceeds the intrinsic carrier concentration
- As doping concentration increases (in the range of 10^{16}-10^{17} atoms/cm^3) band gap starts to narrow
  - Impurity levels broadens into bands forming tails into the conduction and valence bands
  - Minority carriers electrically screened the high concentration of majority carrier
    - Reduces the thermal energy for electron hole pair generation
    - Band gap reduction can be calculated by:
      - Concentration dependency: $\Delta E_G = 22\left(\frac{N}{10^{18}}\right)^{0.5}$
      - Temperature dependency: $\Delta E_G = \frac{\alpha T^2}{T+\beta}$

- **Trivia: What is a degenerate semiconductor?**

Fermi Levels for Silicon as a function of temperature



Semiconductor operational temperature range

- As temperature increases: semiconductor enters three zones
  - Carrier Freeze out region
    - Insufficient energy for impurities to be promoted from their energy trap level
  - Extrinsic region
    - Sufficient energy for impurity promotion to the valence/conduction band
    - $N_D/N_A >> n_i$: Non degenerate semiconductor
  - Intrinsic region
    - Intrinsic carrier concentration greater than impurity
- Maximum temperature can be deduced when intrinsic concentration is less than impurity doping concentration
- As impurity concentrations are dependent upon band gap a wide band gap semiconductor is more suitable for high temperature applications.
- **TRIVIA:** Can you calculate the maximum temperature of operation of a silicon with a p type doping of $1x10^{14}$ /cm^3

Solution:

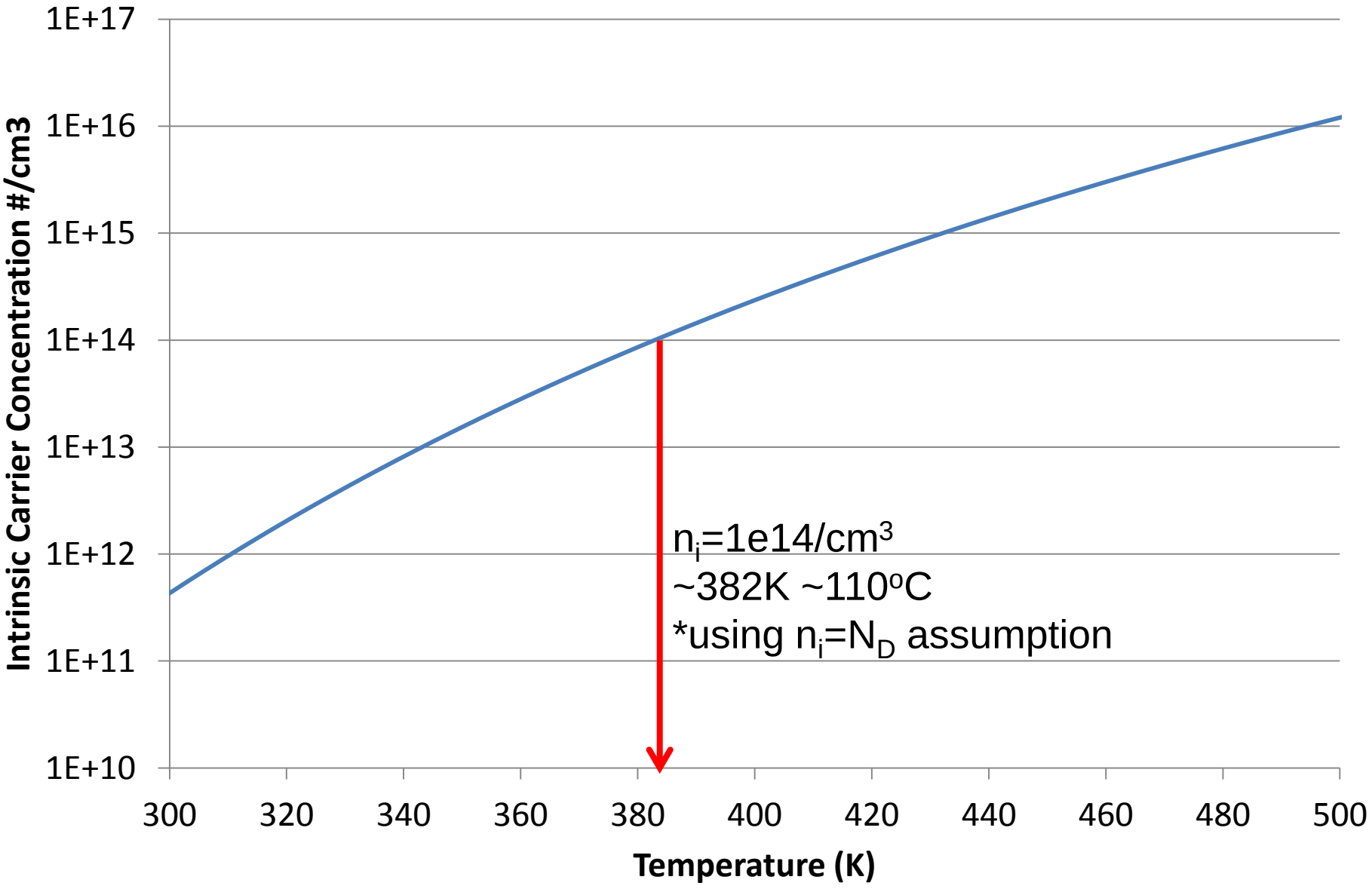
- From: $N_D = n_i \, exp\left[\frac{(E_F - E_i)}{kT}\right]$

$$E_F - E_i = \frac{kT}{q} ln\left[\frac{N_D}{n_i}\right]$$

- Setting an intrinsic condition i.e. $E_F - E_i = 0$
- Therefore intrinsic condition is reached when:

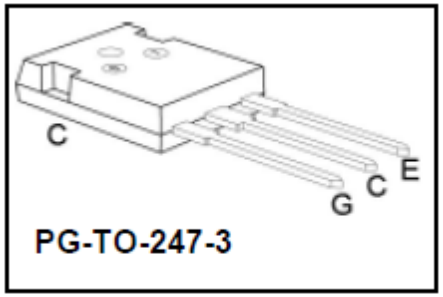
$$N_D = n_i$$

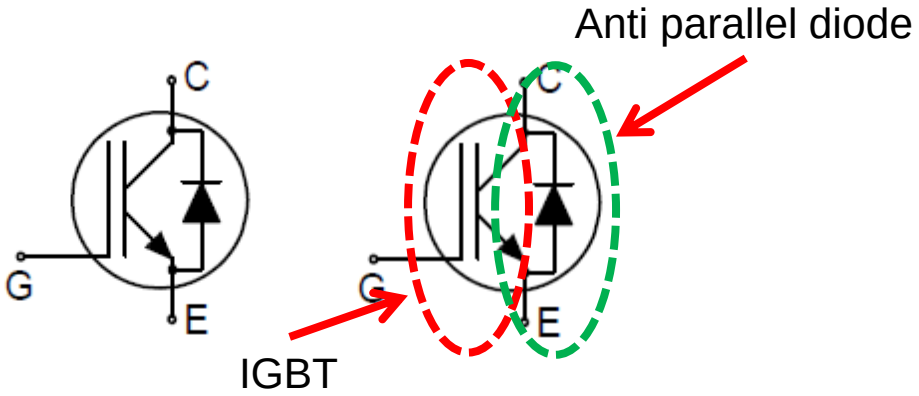
Intrinsic carrier concentration of Silicon



Sanity check….

- An n type device with a 1e14/cm^3 doping concentration would be rated at 1200V
  - Including pass band
    - Pass band: over voltage rating of components to guarantee voltage rating
      - Normally ~ 20% i.e. 1200V component would actually breakdown at ~1500V
      - Takes into account processing variations such as substrate thickness and resistivity
  - A commercially available 1200V 25A IGBT with anti parallel diode:
    - Infineon IKW25T120





Datasheet IKW25T120

positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Low Gate Charge
- Very soft, fast recovery anti-parallel Emitter Controlled HE diode
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Complete product spectrum and PSpice Models : http://www.infineon.com/igbt/

Type	V_{CE}	I_C	$V_{CE(sat),Tj=25°C}$	$T_{j,max}$	Marking Code	Package
IKW25T120	1200V	25A	1.7V	150°C	K25T120	PG-TO-247-3

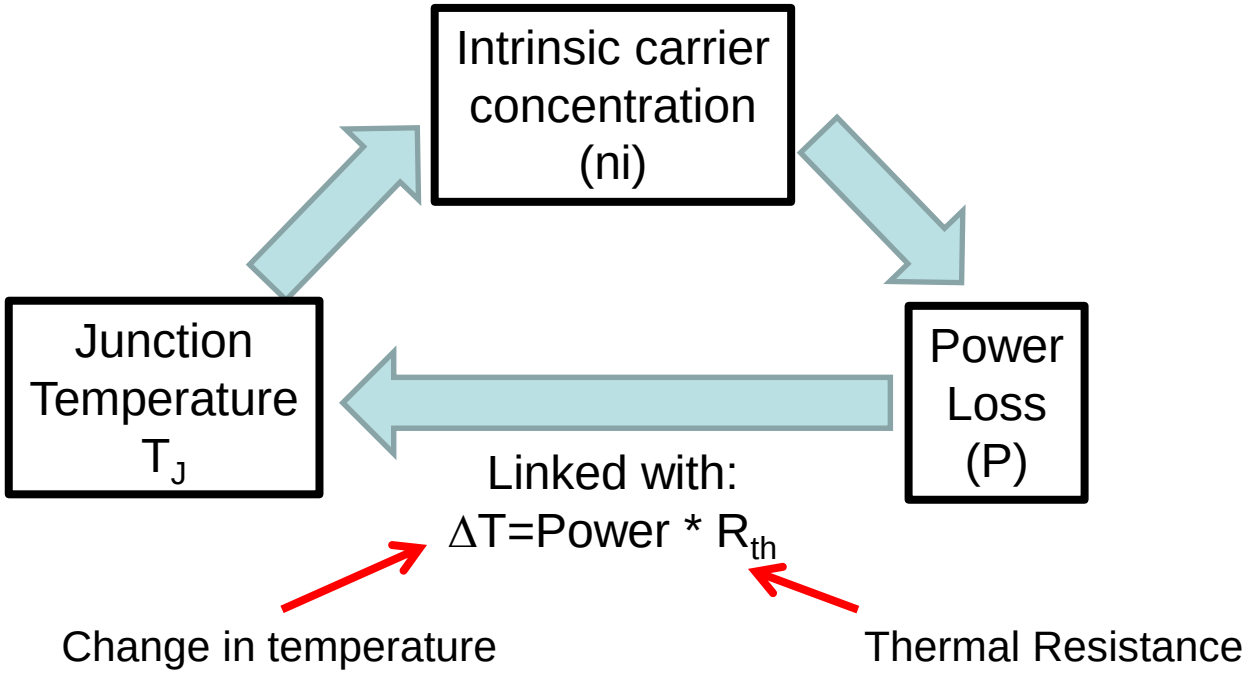
Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current T_C = 25°C T_C = 100°C	I_C	 50 25	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	75	
Turn off safe operating area $V_{CE} \le 1200V$, $T_j \le 150°C$	-	75	
Diode forward current T_C = 25°C T_C = 100°C	I_F	 50 25	
Diode pulsed current, t_p limited by T_{jmax}	I_{Fpuls}	75	
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time[2] V_{GE} = 15V, $V_{CC} \le 1200V$, $T_j \le 150°C$	t_{SC}	10	µs
Power dissipation T_C = 25°C	P_{tot}	190	W
Operating junction temperature	T_j	-40...+150	°C
Storage temperature	T_{stg}	-55...+150	

Maximum Junction temperature 150°C
Big difference from our 110°C calculation

[1] J-STD-020 and JESD-022
[2] Allowed number of short circuits: <1000; time between short circuits: >1s.

- Setting the condition of maximum temperature when the semiconductor becomes intrinsic significantly under-estimates the maximum operating condition
- The main limit to maximum temperature is thermal run-away



- Physical limit of the semiconductor as band gap is related to intrinsic carrier concentrations
- To obtain high temperatures a wide band gap semiconductor is required

Electron density as a function of temperature for Si: Nd=1e14/cm^3