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The University Of Sheffield.

Answers to Introduction to VLSI Design 3, VLSI Design 6

1. ***Figure 1*** *shows a simplified layout of a logic circuit, with the inputs (A, B, C, D) and output (Y) labelled:*

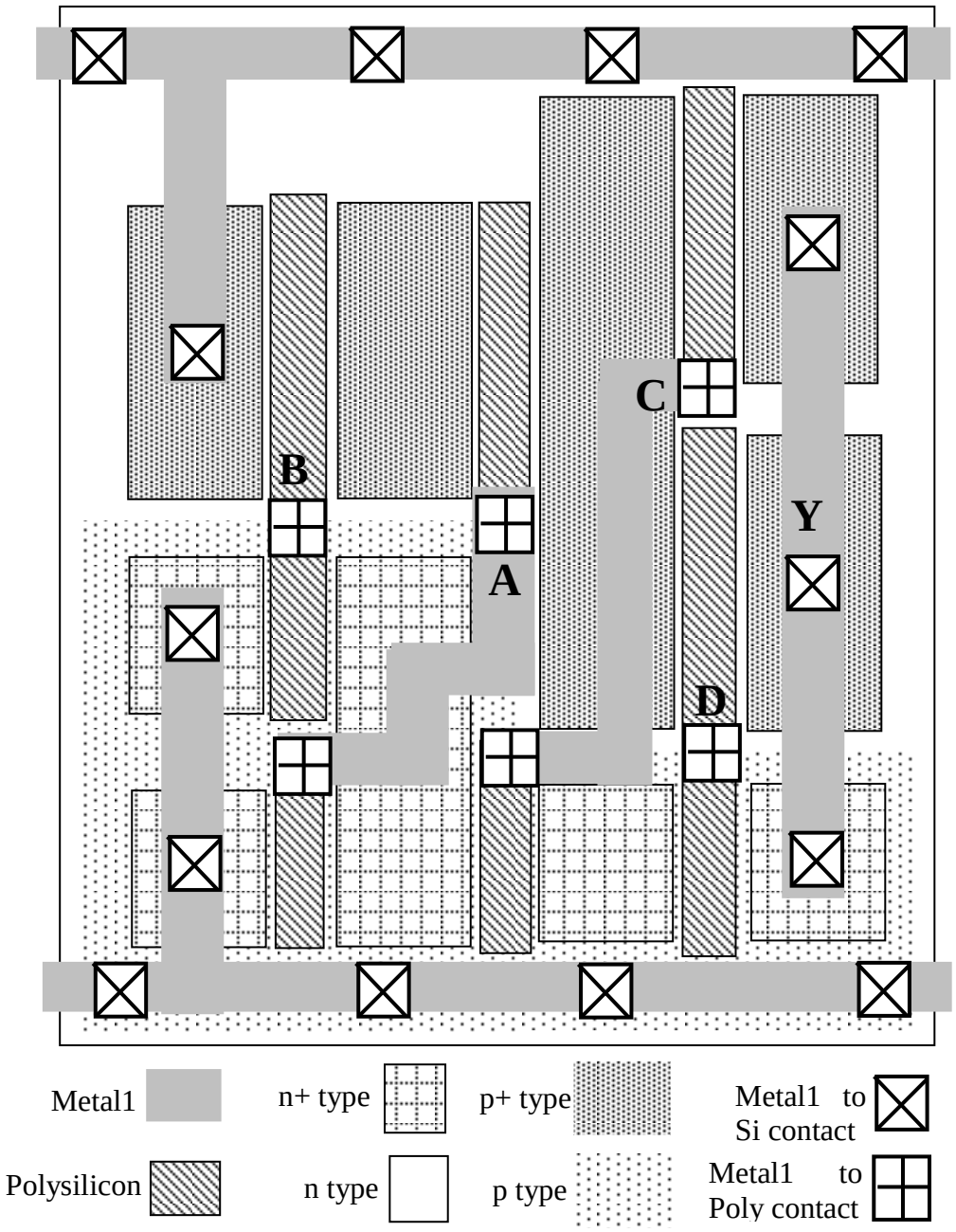
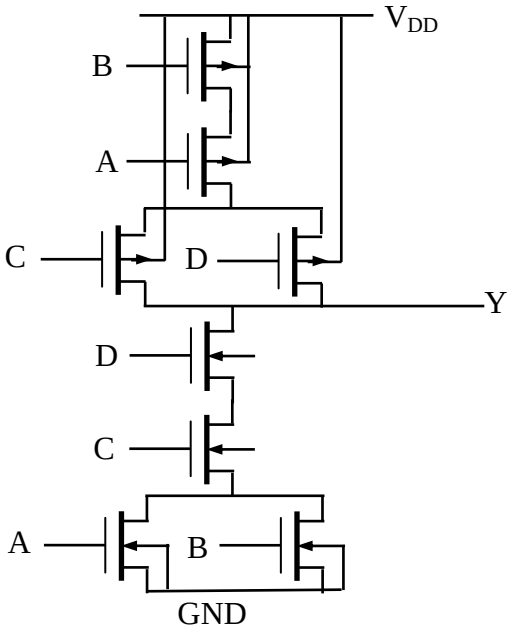


Figure 1: Circuit Layout

a. *Draw a circuit diagram that is an accurate representation of the layout in **Figure 1**.*



(8)

b. *Write down the logical function of the circuit.*

$Y = \overline{(A + B)CD}$

(4)

c. *There are rows of four contacts along the top and bottom of the cell connecting the power supply lines to the underlying silicon. What is their function and why are there so many contacts?*

They are body contacts used to define the value of the substrate voltage. Those in the p-well define the substrate voltage for the *n*-FETs and are connected to the most negative point in the circuit, GND. Those on the n-substrate define the substrate voltage for the *p*-FETs and are connected to the most positive point, V_{DD}. There are so many because the substrate material is relatively high resistivity and the number tends to reduce the resistance between the supply voltages and the region directly under each channel. Without a low resistance, the voltage under the channel can change, giving rise to unwanted behaviour of the FET.

(4)

d. *What can you say about the mobilities of electrons and holes from looking at the layout?*

Roughly speaking the width of the *p*-FETs seems to be 2x that of the *n*-FETs. Assuming that the circuit is designed such that the current drive of the pull-up network is the same as the pull-down network (a reasonable assumption that gives rise to symmetric behaviour) and all other things being equal, the hole mobility would be ½ that of the electrons and this would be countered by the *p*-FETs being twice as wide as the *n*-FETs, remembering that:

$$\beta = \frac{\mu \varepsilon_0 \varepsilon_r W}{t_{ox} L}$$

(4)

2. *A logic circuit is shown in **Figure 2**.*

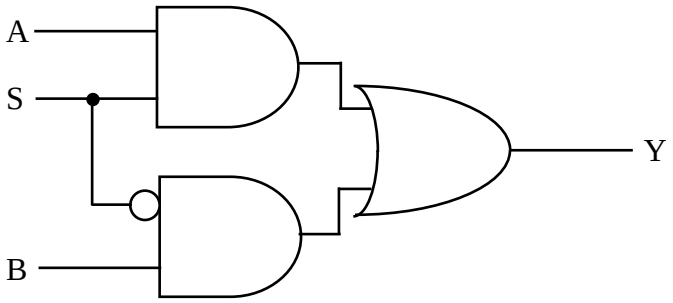


Figure 2: Logic Circuit

a. *Convert the logic circuit into a standard-CMOS transistor-level circuit.*

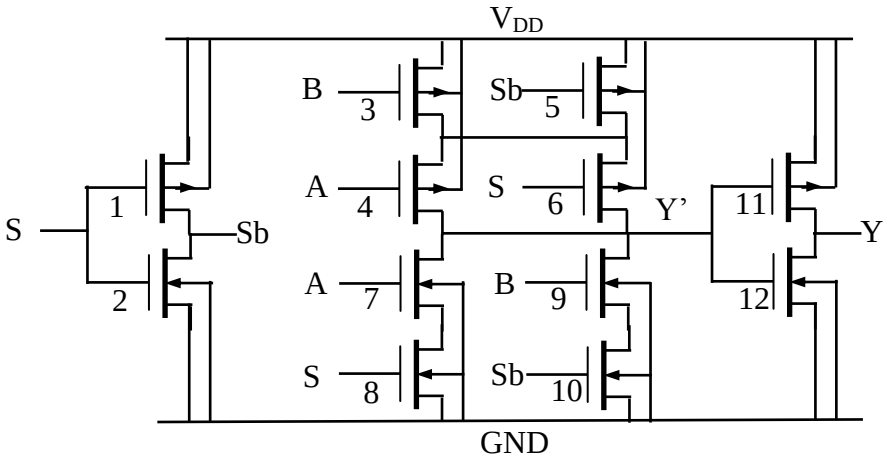
$Y = AS + B\overline{S}$

$Y' = \overline{Y} = \overline{AS + B\overline{S}}$

$\overline{Y'} = AS + B\overline{S}$

Therefore, the pull-down circuit to generate *Y'* consists of two transistors controlled by *A* and *S* in series, in parallel with two transistors controlled by *B* and *Sbar* in series.

The pull-up network is complementary. *Y'* must be inverted to form *Y* and *S* must be inverted to produce *Sb*.



(8)

b. *Size the transistors (as a multiple of a minimum-sized n-type FET) for a minimum sized logic circuit, stating any assumptions that you make.*

If a minimum *n*-FET is width *W* then:

2, 12 = W

1, 7, 8, 9, 10, 11 = 2*W*

3, 4, 5, 6 = 4*W*

This ensures that each pull-up/down network behaves similarly to a single minimum width *n*-FET acting as a pull-down. **(6)**

c. *Estimate the capacitance associated with each of the inputs and wires within the circuit (you can neglect the interconnect capacitance), given that the gate*

capacitance of a minimum-sized n-type FET is 1fF.

The capacitance on A is the gates of 4 and 7 and this is 2x1fF + 4x1fF = 6fF

The capacitance on B is the gates of 3 and 9 and this is 2x1fF + 4x1fF = 6fF

The capacitance on S is the gates of 1,2, 6 and 8 and this is 1fF + 2x1fF + 2x1fF + 4x1fF = 9fF

The capacitance on Sb is the gates of 5 and 10 and this is 2x1fF + 4x1fF = 6fF

The capacitance on Y' is the gates of 11 and 12 and assume half the gate capacitance of the FETs whose drains drive Y' (4, 6, 7, and 9) and this is 2x1fF + 2x1fF + 0.5x(4x1fF + 4x1fF + 2x1fF + 2x1fF) = 12fF

The capacitance on Y is assumed to be half the gate capacitance of the FETs whose drains drive Y (11 and 9) and the load capacitance and this is 0.5x(2x1fF + 1fF) + C_{load} = 3fF + C_{load}. **(4)**

d. *Can you give the more common or standard name given to the type of circuit shown in* ***Figure 2.***

It is a 2-input multiplexer. **(2)**

3. **a.** *For the two FETs shown in **Figure 3**, write down the equations for I_{DSN} and I_{DSP} in the saturated mode of operation (using the usual terms and ignoring channel length modulation).*

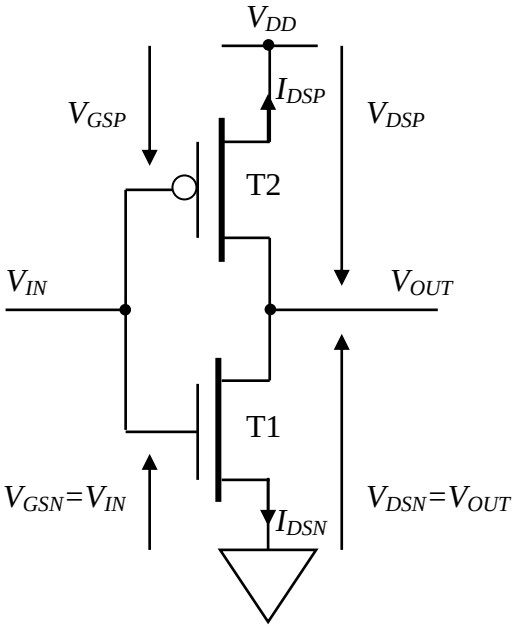


Figure 3: CMOS Inverter

$$I_{DSN} = \frac{\mu_E \cdot \varepsilon \cdot W}{2 \cdot t_{OX} \cdot L} \cdot \left(V_{GSN} - V_{TN}\right)^2 = \frac{\beta_N}{2} \cdot \left(V_{GSN} - V_{TN}\right)^2$$

for $V_{TN} \le V_{GSN}$, $V_{GSN} - V_{TN} \le V_{DSN}$

$$I_{DSP} = -\frac{\mu_H \cdot \varepsilon \cdot W}{2 \cdot t_{OX} \cdot L} \cdot \left(V_{GSP} - V_{TP}\right)^2 = -\frac{\beta_P}{2} \cdot \left(V_{GSP} - V_{TP}\right)^2$$

for $V_{TP} \ge V_{GSP}$, $V_{GSP} - V_{TP} \ge V_{DSP}$ **(4)**

b. *Show that the value of the input voltage, $V_{IN|switch}$, when the output of the inverter in **Figure 3** switches is identified by the following equation:*

$$V_{IN|switch} = \frac{V_{DD} - V_T\left(1 - \sqrt{\frac{\beta_N}{\beta_P}}\right)}{\left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)}$$

where β_N and β_N have their usual definitions and the threshold voltages of the FETs is such that $V_T = V_{TN} = -V_{TP}$.

The switching point is defined as being when $V_{IN} = V_{OUT}$ and this means that $V_{GSP} = V_{IN} - V_{DD}$ and $V_{DSP} = V_{OUT} - V_{DD}$. Clearly, I_{DSP} and I_{DSN} can be equated, mindful of direction.

$$I_{DSN} = -I_{DSP} = \frac{\beta_N}{2} \cdot \left(V_{IN} - V_{TN}\right)^2 = \frac{\beta_P}{2} \cdot \left(V_{IN} - V_{DD} - V_{TP}\right)^2 = \frac{\beta_P}{2} \cdot \left(V_{TP} + V_{DD} - V_{IN}\right)^2$$

From this (picking the appropriate root of the equation),

$$\sqrt{\frac{\beta_N}{\beta_P}} \cdot (V_{IN} - V_{TN}) = (V_{TP} + V_{DD} - V_{IN})$$

Hence:

$$V_{IN} \cdot \left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right) - \sqrt{\frac{\beta_N}{\beta_P}} \cdot V_{TN} = V_{DD} + V_{TP}$$

$$V_{IN} = \frac{V_{DD} + V_{TP} + \sqrt{\frac{\beta_N}{\beta_P}} \cdot V_{TN}}{\left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)}$$

If we assume that $V_T = V_{TN} = -V_{TP}$ and $V_{IN} = V_{IN|switch}$ then:

$$V_{IN|switch} = \frac{V_{DD} - \left(1 - \sqrt{\frac{\beta_N}{\beta_P}}\right) \cdot V_T}{\left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)}$$

(8)

c. *What would the normal value of the switching voltage be and how is this achieved practically?*

Normally the the transistors are sized so that $\beta_P = \beta_N$ and this expression reduces to:

$$V_{IN|switch} = \frac{V_{DD}}{2} = V_{OUT|switch}$$

(2)

d. *Are there any circumstances in which you might want to alter the switching voltage, how might this be achieved, and what are the limitations likely to be.*

Sometimes it is advantageous to have a logic circuit that switches at a level other than $V_{DD}/2$ because the point in time, during a logic transition occurs can then be shifted away from the point in time when other circuits are transiting. This can allow, for example, level restoration in non-complementary pass transistor logic without incurring excessive power consumption by switching on a level restoring transistor after the majority of the transition has taken place.

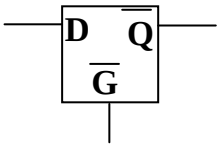
This can be achieved by changing the ratio of β_N to β_P and this can normally be achieved by altering the length or width of one or both of the transistors. However, because of the root relationship and the effect on $V_{IN|switch}$ and the fact that the change in the denominator conteracts the change in the numerator, significant changes in width/length are needed for modest changes in voltage and these changes will normally give rise to increasing size and capacitive loading, both of which are undesirable.

(6)

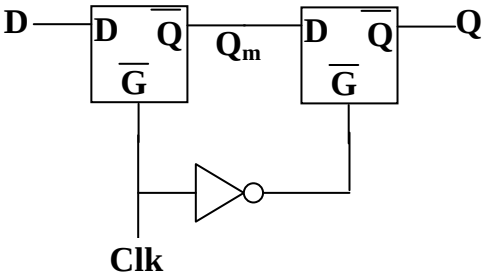
4. a. *Show how a rising-edge-triggered master-slave D-type Flip-flop can be constructed from two basic latches. Ensure that you describe how the pair of latches behave.*

The simplest way of making a master slave flip-flop depends upon using two latches. The latch has the form and truth table shown below.

D	$\overline{G}$	Q_{new}
X	1	Q_{old}
D	***0***	$\overline{D}$



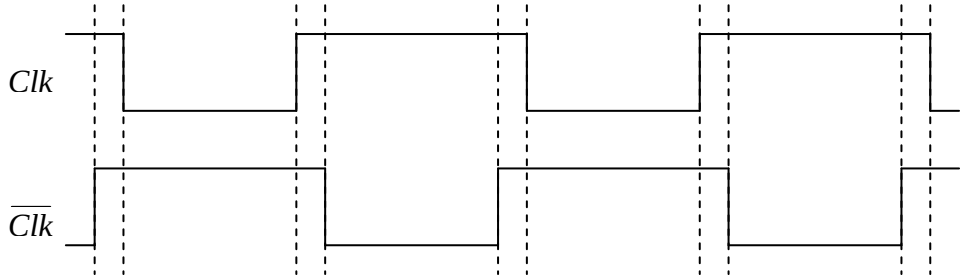
Two latches connected together make a master-slave flip-flop:



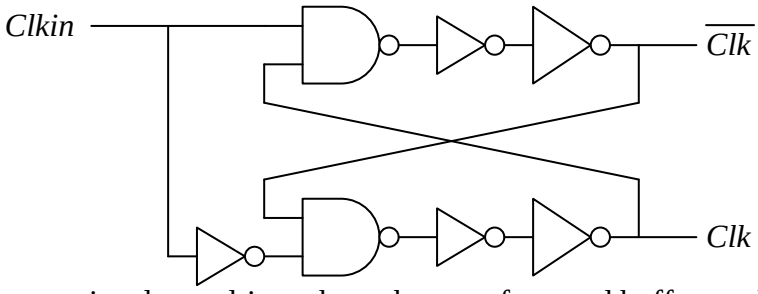
When Clk goes from 0→1, the LH latch closes trapping the inverse of the value of D (around the time of the rising edge) = D_s at the output Q_m. At the same time, the enable on the RH latch goes from 1→0 making this latch transparent allowing the inverse of Q_m (i.e. D_s) appear at the output. It is held constant because the LH (master) latch is closed. As Clk goes from 1→0, the LH latch opensm beoming transparent. However, before the value of $D_s$bar is lost from its output (and it is important that this is a guaranteed condition), the enable input of the RH (slave) latch goes from 0→1 trapping the value of D_s at the Q output for the low part of the Clk period. **(6)**

b. i) *Draw a schematic to show how you can construct a clock generator that will produce a clock signal and its inverse, which do not overlap in the low state.*

Two non-overlapping clock signals would be as shown below:



A circuit for generating signals like this is shown below:



The output signals are driven through a set of tapered buffers and when one of these output signals first becomes 1 (the other will still be 1), it must pass through the other NAND gate changing the state to 0 and the other set of tapered buffers before the other output signal changes from 1 to 0. Thus, both outputs will be 1 for a period of time that is determined by the delay through the chains of buffers. The tapering can allow the load

(4)

ii) *Why is it important, in some types of design, to have two clocks that do not overlap?*

The problem exemplified by the need to ensure that the slave latch closes before the master latch opens *and* that the master latch closes before the slave latch opens in the flip-flop can be solved by having these non-overlapping clock *phases*.

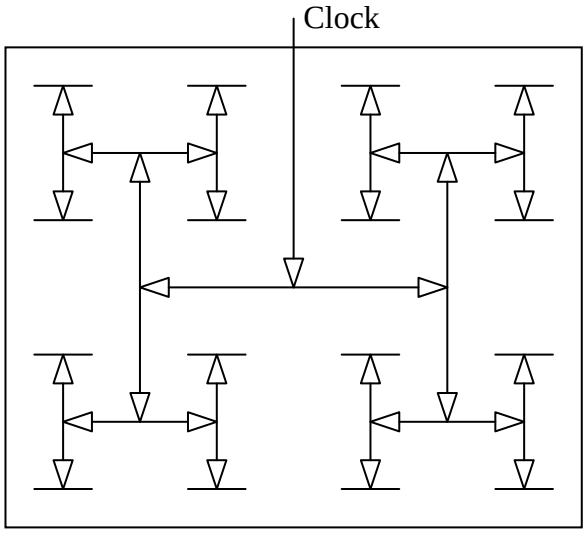
(2)

c. i) *What is a clock tree and why is it so important for the synchronous design methodology?*

A clock tree is the logic circuit, normally automatically generated during P+R that ensures that the primary clock signal supplied to the IC is distributed over the surface of the IC such that the edges appear at flip-flops at, essentially, the same instant (subject to a small, known error) wherever they are on the surface of the IC. By doing this, race hazards between clock signals and delayed signals passing through logic from one flip flop output to another's input can be avoided independent of PVT (i.e. the clock edge that gives rise to a logic transition will always appear at the clock of a receiving flip-flop *before* the logic transition has time to propagate to the data input of the receiving flip-flop. This ensures that the signal stored at a flip-flop is always as a result of the values stored in other flip-flops in the previous clock cycle. This certainty is the underpinning cornerstone of the synchronous design methodology, allowing circuits to

be designed and manufactured reliably. **(4)**

ii) *Show how a clock tree might be constructed*



The clock signal is buffered repeatedly and split recursively to drive a smaller part of the IC. The symmetry ensures that interconnect and buffer delays between the root (input) of the tree and all of the leaves (where flip-flops are driven) are essentially equal. **(2)**

iii) *What is metastability?*

This problem arises when the input, *D*, to a flip-flop is changing state at a critical point in time when *Clk* is rising. Essentially, this can cause the flip-flop to enter a metastable state (neither 1 nor 0). This indeterminate output value will relax to a defined state (near exponentially with time). At the limit, the bistable element forming a latch can be balanced only relaxing to a stable state when noise is applied. **(2)**

NLS