Feedback for EEE310/6036 Session: 2012-2013

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

Generally, the paper was addressed quite badly. The key problems seemed to be that: people mixed up things – providing answers for another question (possibly because they had mixed things up); people just hadn't mastered the material; simple algebraic manipulations seem to be beyond people's reach.

Question 1:

This question was generally done quite well. A few people had difficulties with the function, *Y*, mixing up inverses and parallel .v. series combinations.

Question 2:

Not many people attempted this question and in part b) some people described the process of splitting a long wire up with buffers rather that what was being asked for: driving through a set of exponentially wider buffers to drive a large capacitance. Additionally, in part d) people just took Ro and multiplied it by 400Cin rather than using a set of 6 buffers ln(400)=6 to drive this each one of which has an effective RC of $RoCine^1$ (i.e. a buffer of width e^{i-1} driving a capacitance of $e^i Cin$. Consequently the overall time should be $0.7*6*RoCine^1$.

Question 3:

In part a) many people just produced a diagram of two latches in series although the question specifically says 'transistor level schematic'. Additionally, some people drew a non-overlapping clock buffer based on an RS FF – this was not what was asked for. In part c) most people could not describe the terms of the equation adequately. I note that, as printed, there is a mistake in this equation the exponent should have a negative sign. This did not affect the ability to undertake part c) but could have affected part f) and so where it was clear that this had caused a problem in part f) I provided some benefit.

Question 4:

The derivation in part a), which I specifically said in the lectures was a derivation that I 'could' put in an exam paper, was done quite badly. People mixed up V_{TN} and V_{TP} or merely hoped that I would notice the sudden changes of sign. Additionally, people forgot to take the negative root when square-rooting each side of the equation, or forgot that $I_{DSP} = -I_{DSN}$ (look at how they are defined in the figure). Consequently, the manipulations included a lot of sign changes from line to line to make the answer correct (I am capable of noticing this kind of subterfuge). In part c) despite having done this in the lectures, the TG based circuits for the logical functions were weird and odd. For a TG, the signal and its inverse should be applied to the two gates – not two separate signals! To make a complete logic function, there should be two TGs: one controlled by a signal, the other controlled by the inverse of the *same* signal!