Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (2.0 hours)

EEE310 Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. The schematic in **Figure 1** is the pull-up network for a CMOS circuit.

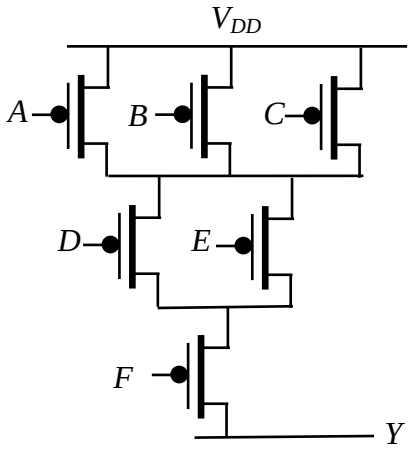

Figure 1: Pull-up Network

a. Draw the corresponding pull-down network **(5)**

b. Write down the function, *Y*, in terms of the inputs *A*, *B*, *C*, *D*, *E* and *F*. **(5)**

c. Size the transistors (in both the pull-up and pull down network) assuming that this is a *minimum-sized* gate and that $\mu_H = 0.4\mu_E$. **(5)**

d. Is there any significance in the ordering of the transistors i.e. *A, B, C* closest to the supply voltage; *F* closest to the output? **(5)**

2. **a.** Explain the problem with interconnect in integrated circuits as technology shrinks. **(4)**

b. What is the optimum way to drive a large capacitance? Show that the relevant expressions to describe how to drive a large capacitance, C_{load}, starting from a minimum sized inverter with input capacitance C_{in}, are as follows.

$$N = ln\left(\frac{C_{load}}{C_{in}}\right)$$

$$k = e^1$$

where *k* and *N* have their usual meanings in this context **(6)**

c. What, if any, are there any constraints on the value of *N* **(2)**

d. A minimum sized inverter has an input capacitance of C_{in} and the output resistance of the inverter can be simply modelled as:

$$\frac{2}{\beta(V_{DD} - V_T)}$$

where the terms have their usual meanings. A load, C_{LOAD}, equivalent to $400C_{IN}$ is to be driven. The switching voltage for the inverters is $0.5V_{DD}$ and calculation shows you that the time taken for the output of a first order system, with a step input, to reach 0.5 of its asymptotic value is $0.7RC$. Estimate the time (in terms of β, V_{DD}, C_{in} and V_T) taken to drive the load capacitance from its resting state at V_{DD} or 0 to $0.5V_{DD}$. State any assumptions made. **(8)**

3. **a.** Draw a transistor level schematic diagram for a master-slave D-type Flip Flip and explain its operation. **(5)**

b. What is metastability. Explain how it arises and what the consequences are? **(3)**

c. Identify and explain the terms in the following expression, that models the number of *upsets* per second arising from metastability.

$$upsets = T_0 e^{t_r/t_c} f_{clk} f_{data}$$ **(2)**

d. Metastability is likely to occur at the boundary between two clock domains – why is this the case? **(2)**

e. How can the upsets per second at the boundary between two clock domains be reduced? What is a metastability-resistant sampler and how would it be constructed? **(4)**

f. An 8 bit bus crosses a clock domain. The clock frequency on the receiving side of the boundary is 0.7GHz and the clock frequency on the sending side is 50MHz. Assuming random data, what would the sampler on the receiving side need to look like to ensure fewer than one upset every three years on data crossing the boundary. You can assume that both T_0 and t_c are equal to 0.1ns. **(4)**

4. a. For the circuit shown in **Figure 4**:

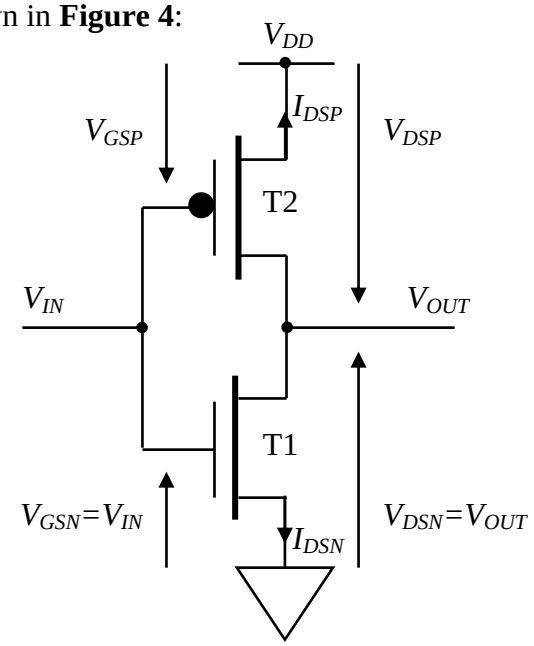

Figure 4: Inverter

show that the switching voltage (defined as the voltage when $V_{IN} = V_{OUT}$) occurs when:

$$V_{IN|switch} = \frac{V_{DD} - V_T\left(1 - \sqrt{\frac{b_N}{b_P}}\right)}{\left(1 + \sqrt{\frac{b_N}{b_P}}\right)}$$

and that when the gains of the transistors are equal, this is when $V_{IN} = V_{DD}/2$.

to solve this problem you may use the characteristics for n- and p-channel FETs, as follows:

n-FET *I*/*V* characteristic

$$I_{DSN} = \frac{\mu_E \times C_{OX} \times W}{2L} \times \left(V_{GSN} - V_{TN}\right)^2 \qquad (V_{TN} \le V_{GSN},\quad V_{DSN} \ge V_{GSN} - V_{TN})$$

$$= \frac{\mu_E \times C_{OX} \times W}{L} \times \left(V_{GSN} - V_{TN} - \frac{V_{DSN}}{2}\right) \times V_{DSN} \qquad (V_{TN} \le V_{GSN},\quad V_{DSN} < V_{GSN} - V_{TN})$$

$$= 0 \qquad (0 \le V_{GSN} < V_{TN})$$

p-FET *I*/*V* characteristic

$$I_{DSP} = -\frac{\mu_H \cdot C_{OX} \cdot W}{2L} \cdot \left(V_{GSP} - V_{TP}\right)^2 \qquad (V_{TP} \ge V_{GSP},\ V_{DSP} \le V_{GSP} - V_{TP})$$

$$= -\frac{\mu_H \cdot C_{OX} \cdot W}{L} \cdot \left(V_{GSP} - V_{TP} - \frac{V_{DSP}}{2}\right) \cdot V_{DSP} \qquad (V_{TP} \ge V_{GSP},\ V_{DSP} > V_{GSP} - V_{TP})$$

$$= 0 \qquad (0 \ge V_{GSP} > V_{TP})$$

$$\beta_P = \frac{\mu_H C_{OX} W}{L} \qquad \beta_N = \frac{\mu_E C_{OX} W}{L}$$

(6)

b. Draw the schematic for a transmission gate. **(2)**

c. Show how, using transmission gates and inverters only, the following logic functions can be implemented:

i). XOR **(2)**

ii). AND **(2)**

iii). OR **(2)**

iv). Multiplexer **(2)**

d. **i).** What are the limitations of using transmission gates to implement logic? **(2)**

ii). How might you deal with these limitations? **(2)**

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