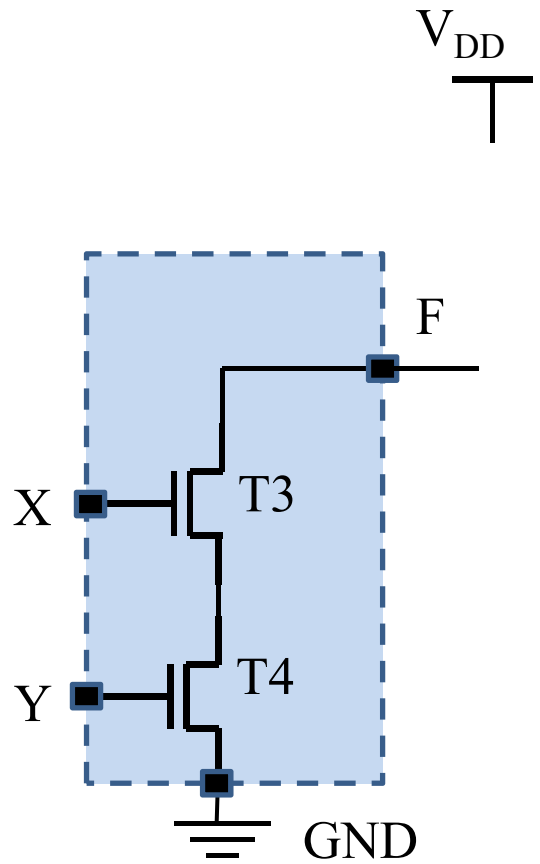
CMOS Logic Circuits

- Output Stages
- Wired Logic
- Tristate Gates
- Transmission Gates

http://www.youtube.com/watch?v=FN87Ua_QaTQ

Open-Drain Gates

Open-Drain refers to a device where the drain terminal of the output transistor is unconnected. It must be externally connected to V_{DD} by an external pull-up resistor.



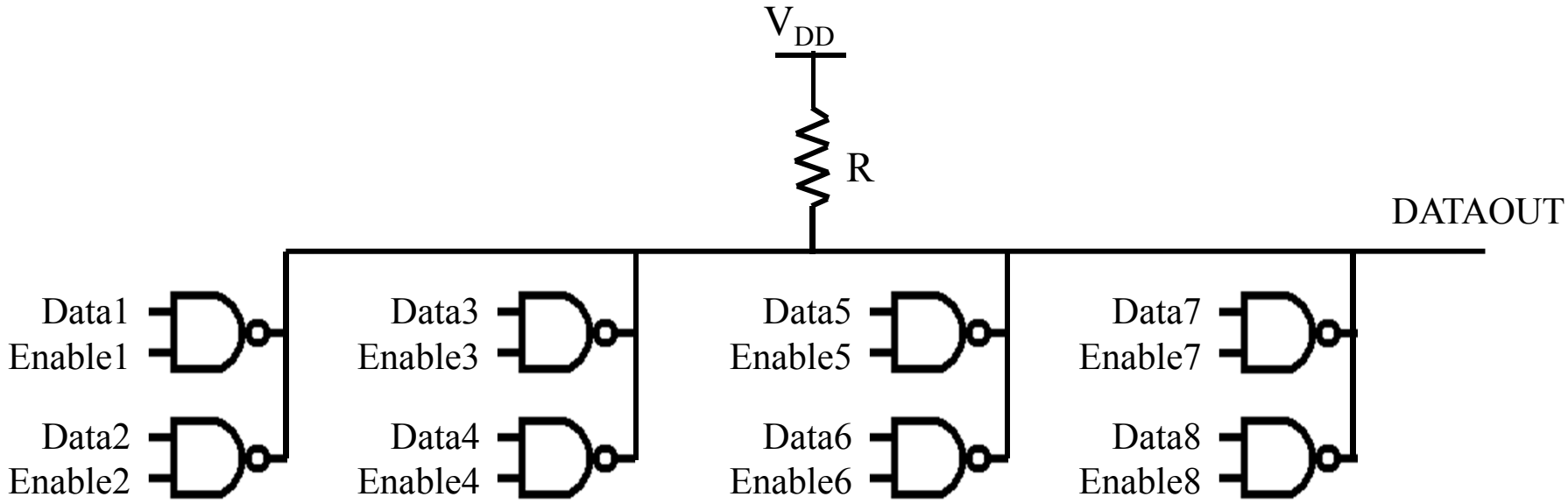
NAND with open-drain output

X	Y	T3	T4	F
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

Can be used for:

1. Driving LEDS
2. Driving multisource buses
3. Performing wired logic

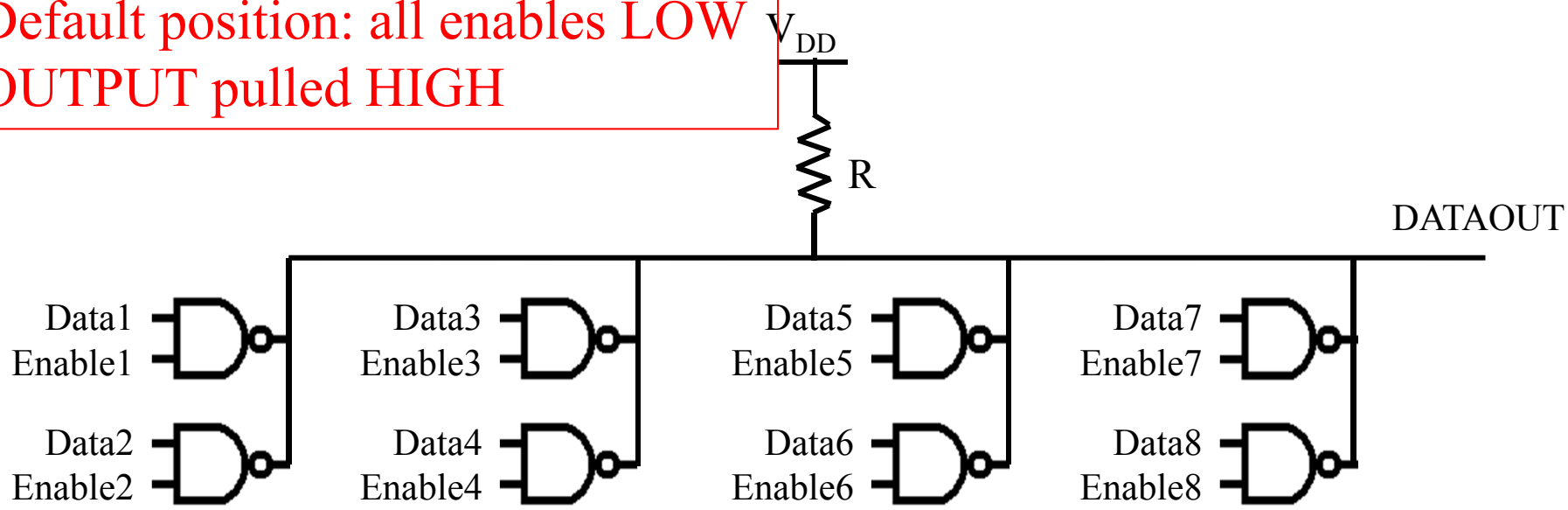
Multisource Bus using Open-Drain NAND gates



This configuration allows several devices to put data onto a common bus. Only one device at a time can drive this bus, all other devices must be in the 'open' state and will be pulled **HIGH**.
The driving device will take its enable line **HIGH** (all other enables must be **LOW**). If its data input is **LOW** the output is pulled **HIGH**. If its data input is **HIGH**, the output is driven **LOW**.

Multisource Bus using Open-Drain NAND gates

Default position: all enables LOW
OUTPUT pulled HIGH



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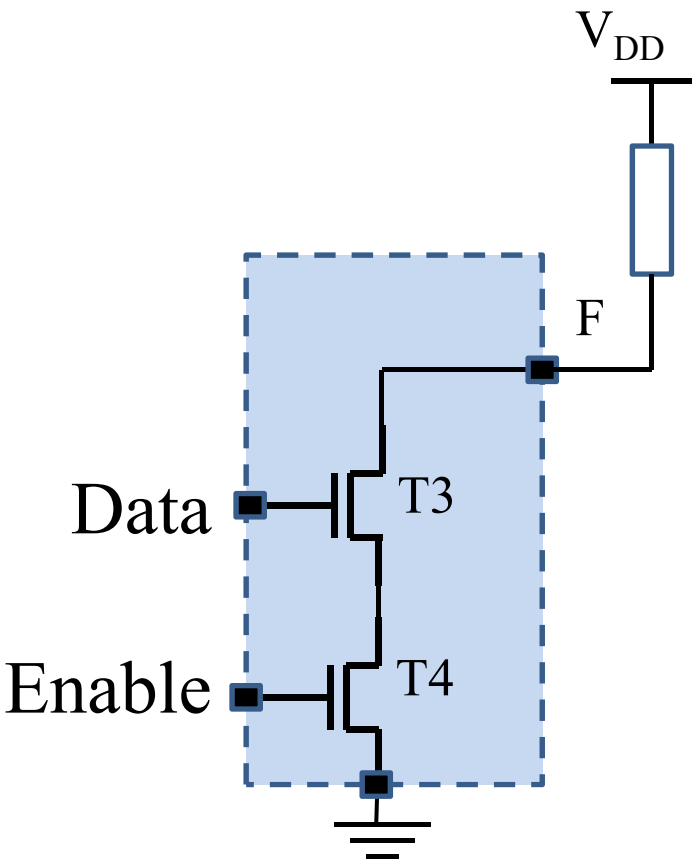
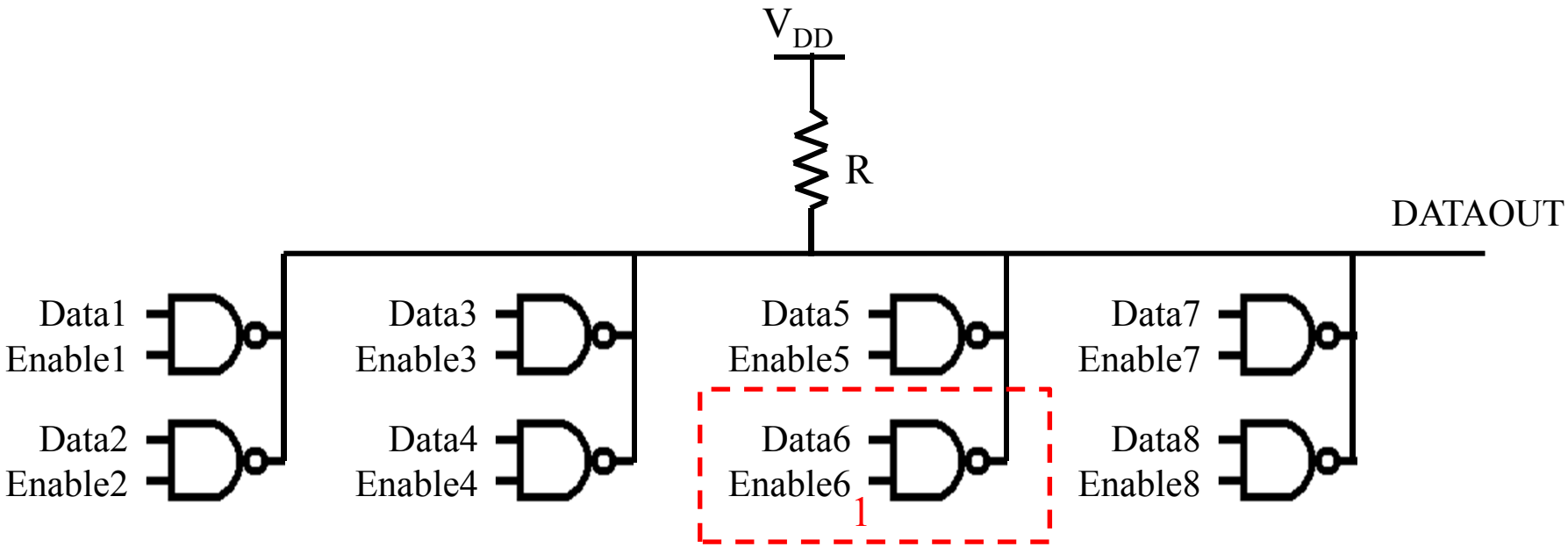

V_{DD}
F
Data
T3
Enable
T4
GND

Multisource Bus using Open-Drain NAND gates



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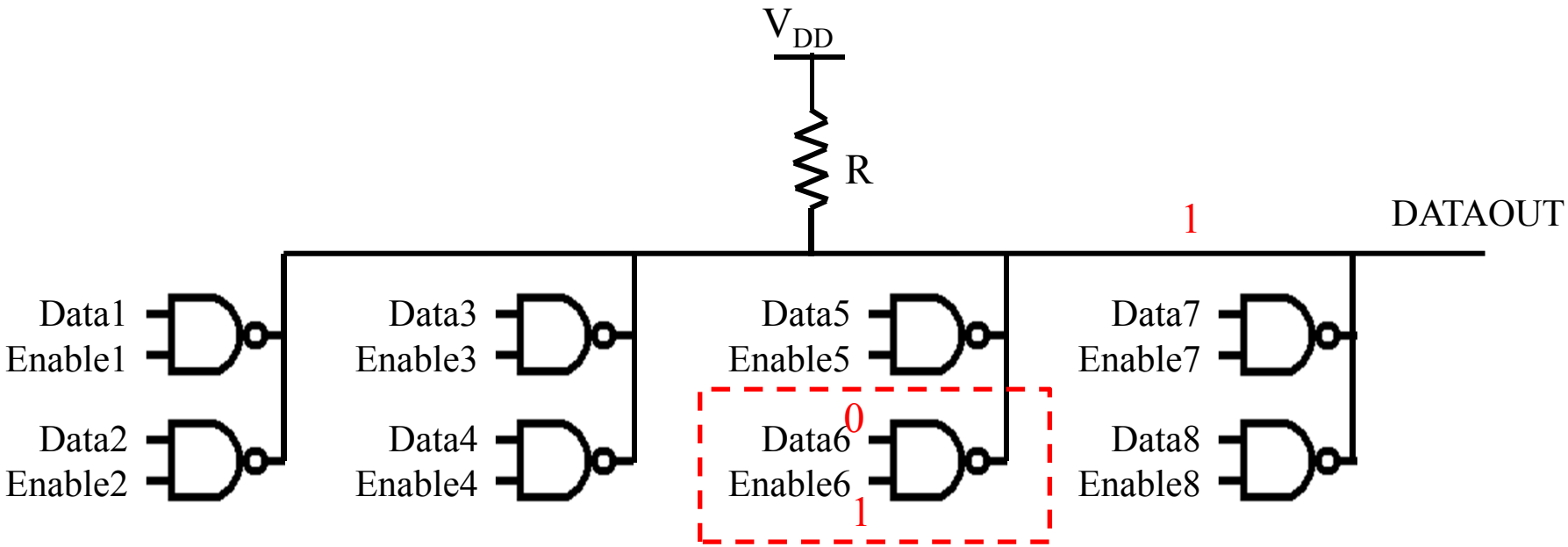
Multisource Bus using Open-Drain NAND gates



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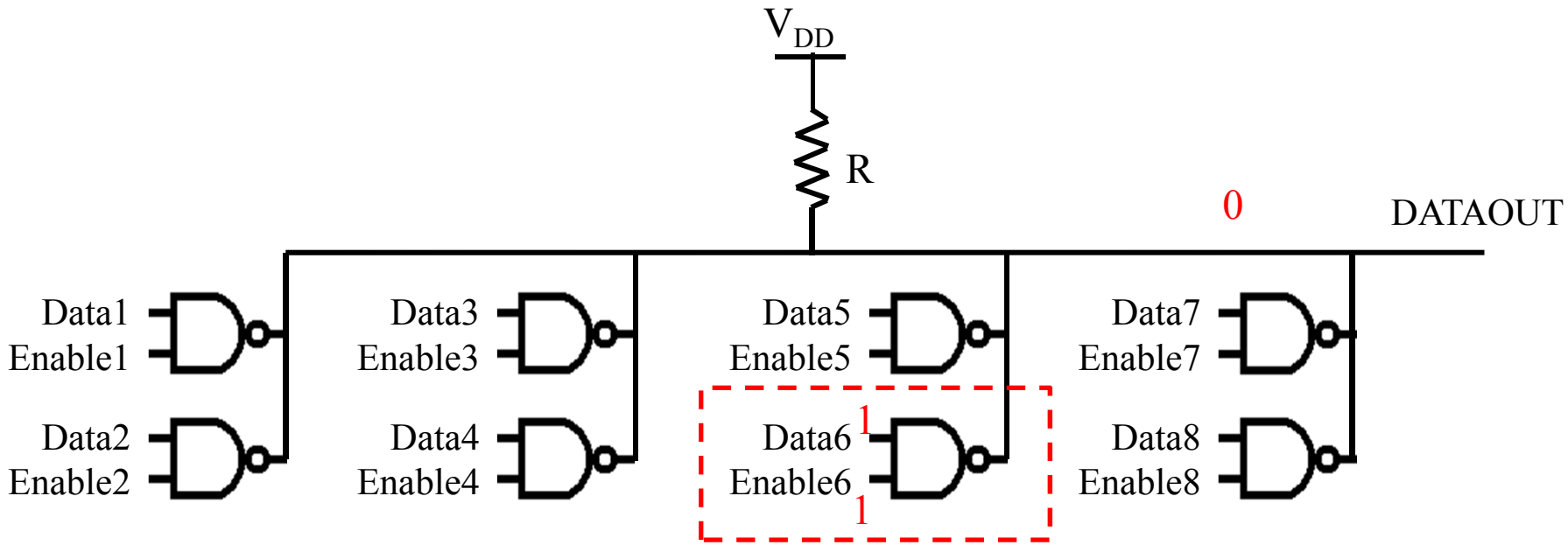
Multisource Bus using Open-Drain NAND gates



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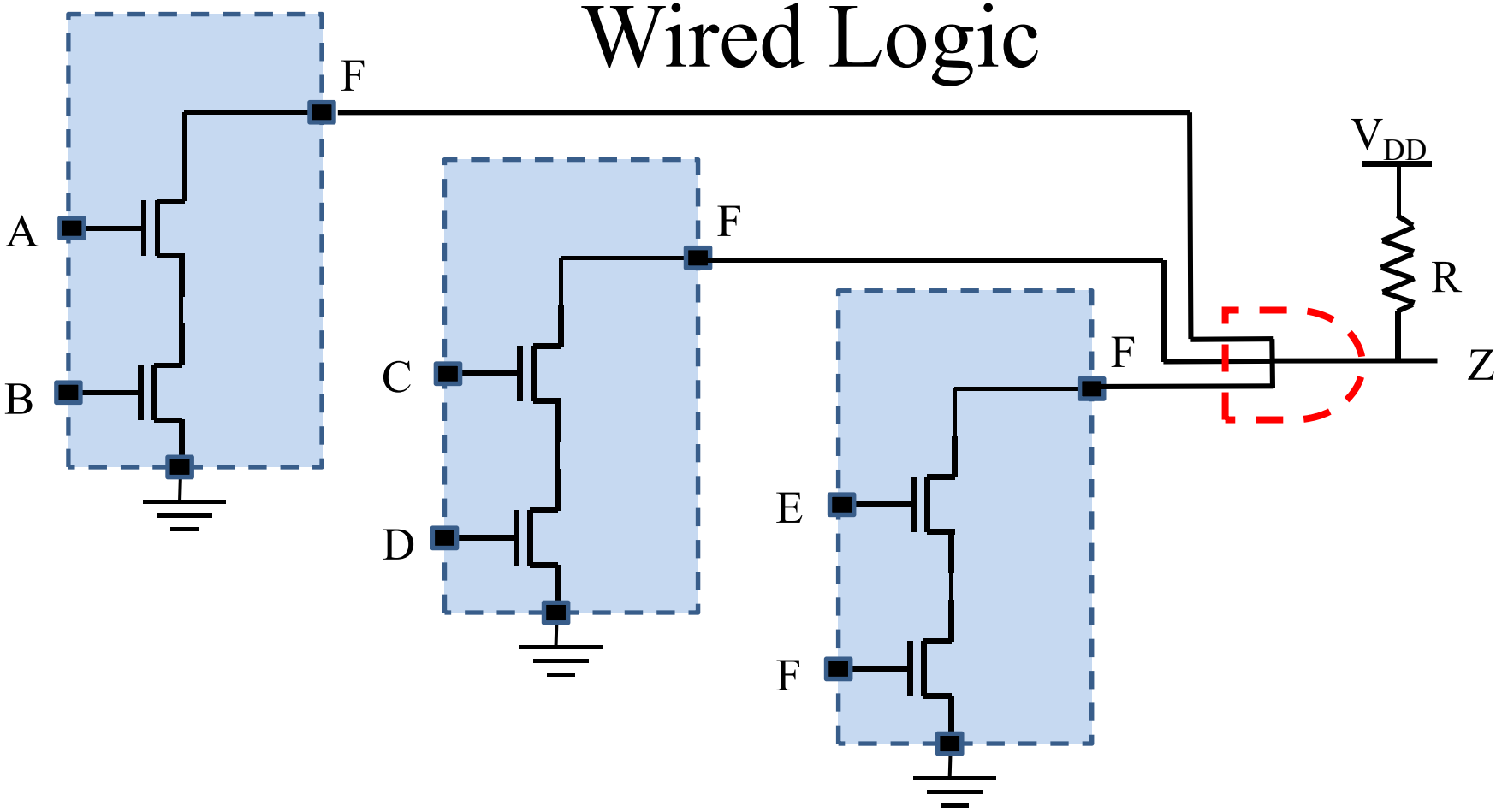
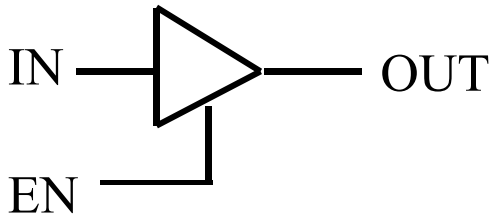
Wired Logic



Wired logic is performed when the output of several open-drain gates are tied together with a single pull up resistor. In this case the **AND** function is obtained as the wired output is **HIGH** if and only if the individual gate outputs are **HIGH** (open).

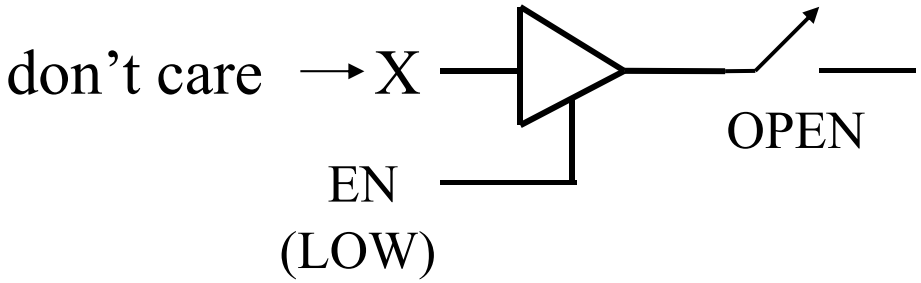
Tristate Output

A tristate gate has three output states, HIGH, LOW, high-impedance (high-Z).



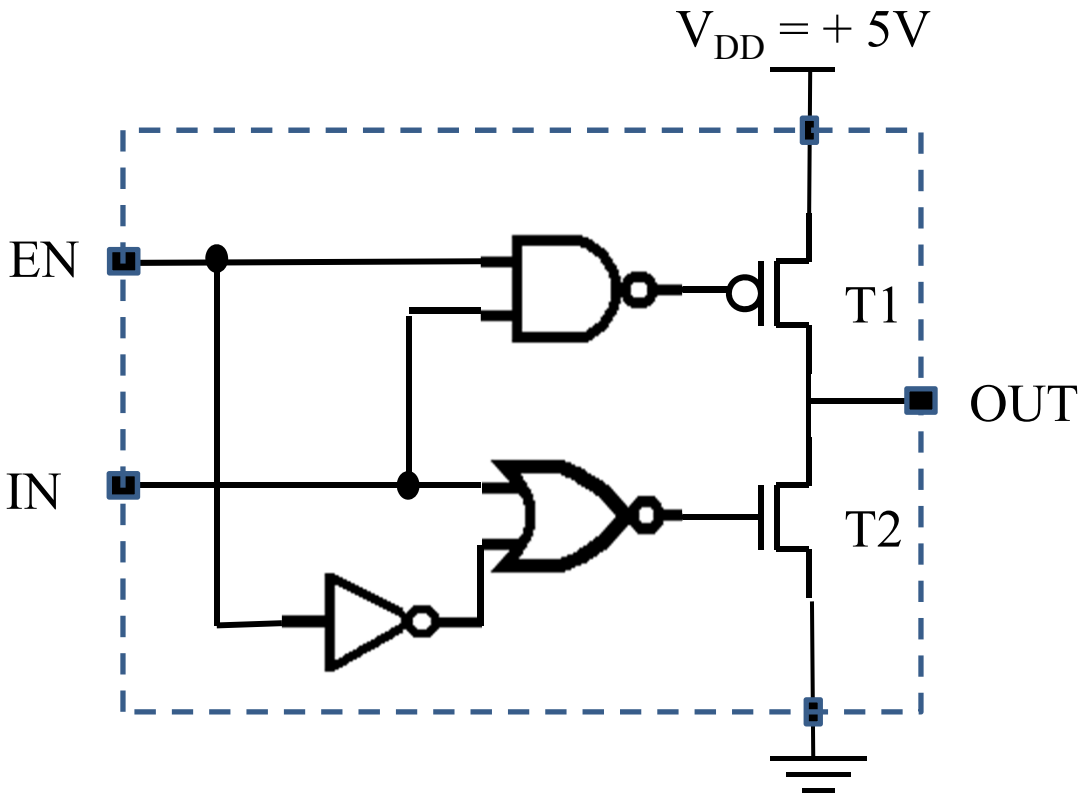
When enable (EN) is **HIGH**, the gate will function as normal, in this case, acting as a straight buffer. Setting enable **LOW** selects high-impedance operation. The output is effectively disconnected from the rest of the circuit by internal circuitry.

This allows us to connect outputs together which may otherwise destroy the gates.



Tristate buffer CMOS Gate Circuit

When enable is **LOW**, the NAND gate output will be driven **HIGH** and the NOR gate output will be driven **LOW** turning off transistors T1 and T2.



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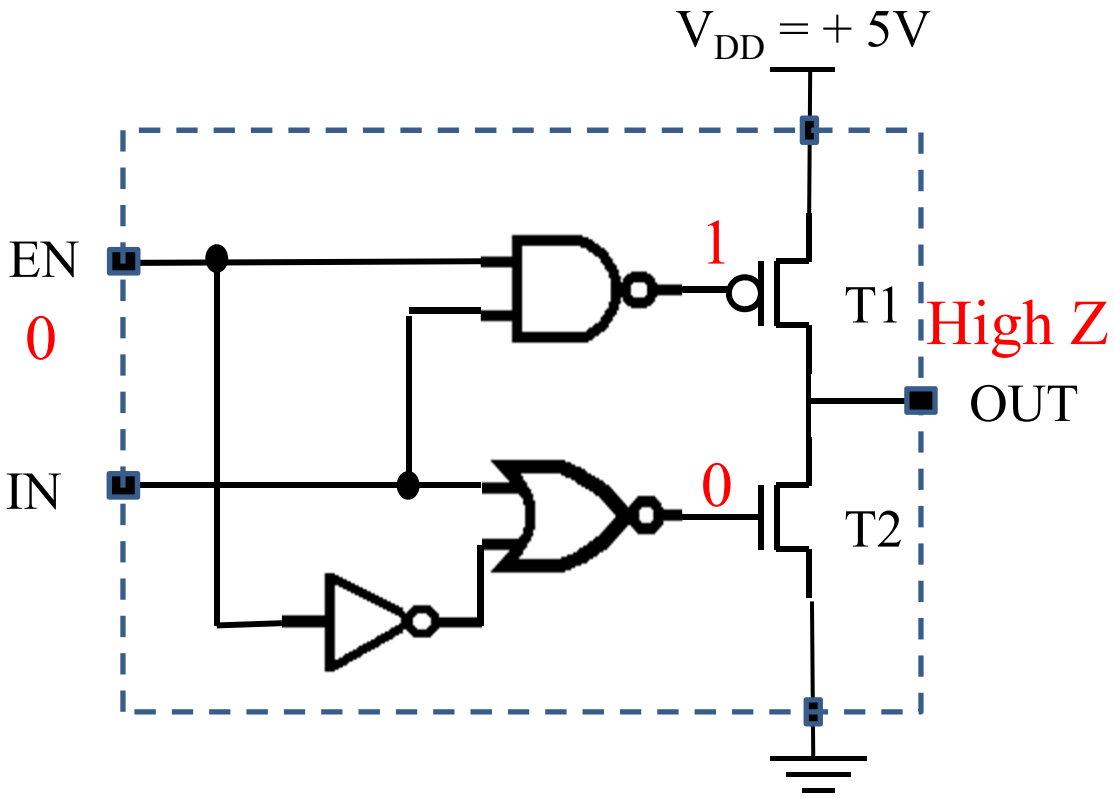


A LOW drives a NAND gate HIGH
A HIGH drives a NOR gate LOW

Tristate buffer CMOS Gate Circuit

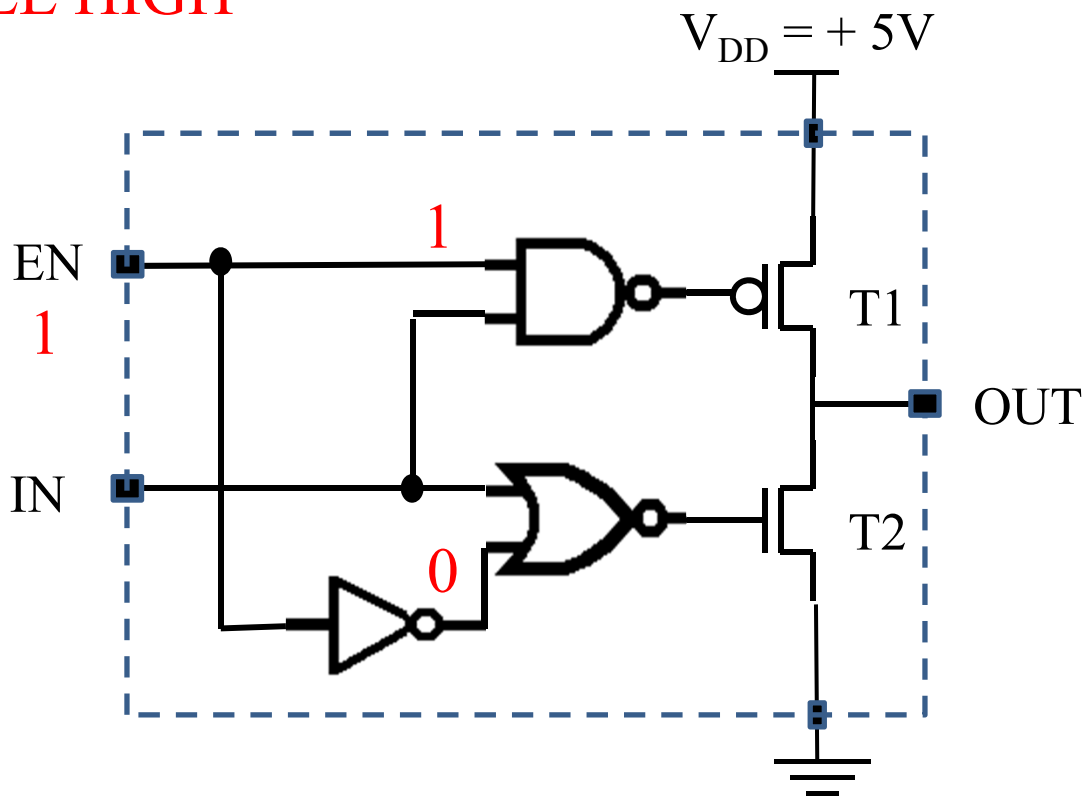
ENABLE HIGH

X	Y	$\overline{X.Y}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND

X	Y	$\overline{X+Y}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR



Tristate buffer CMOS Gate Circuit

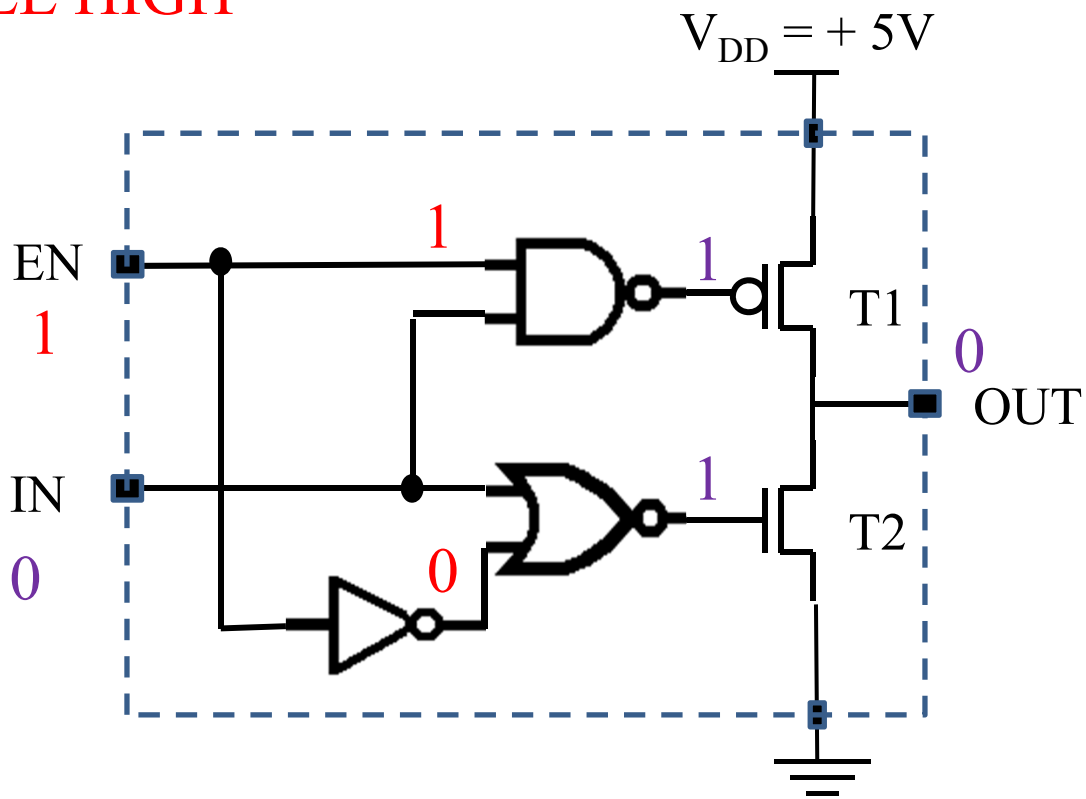
ENABLE HIGH

X	Y	$\overline{X.Y}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND

X	Y	$\overline{X+Y}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR



Tristate buffer CMOS Gate Circuit

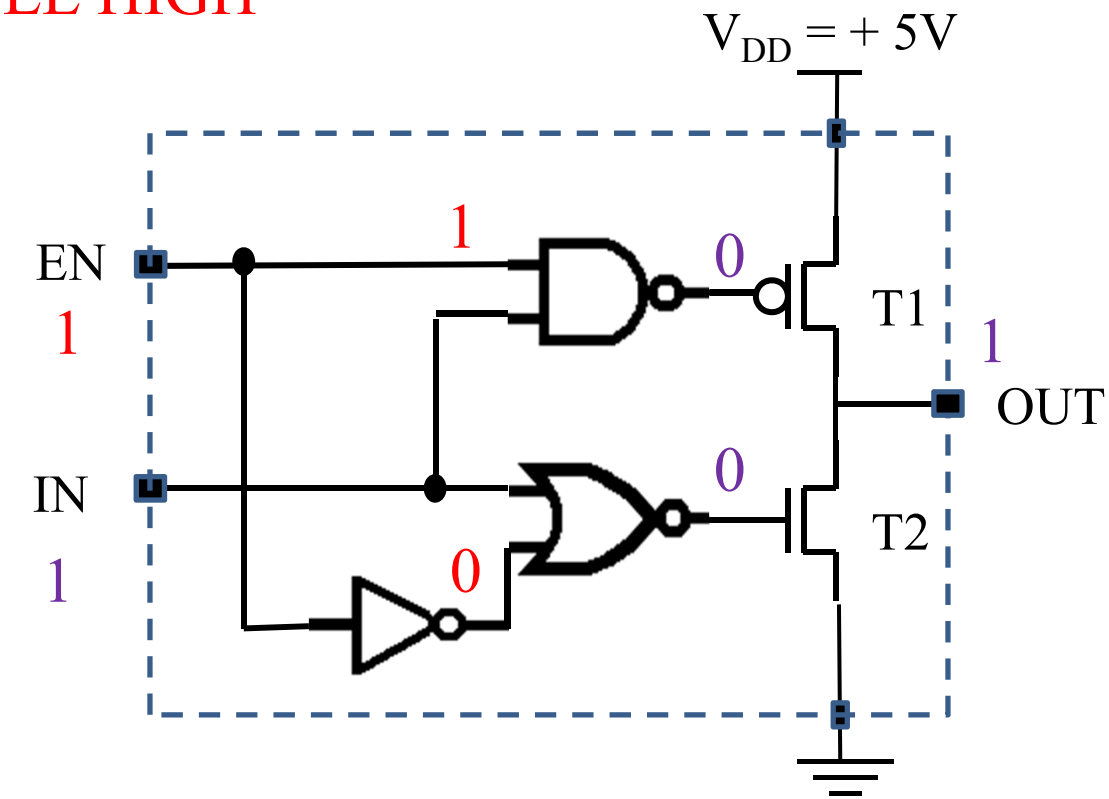
ENABLE HIGH

X	Y	$\overline{X.Y}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND

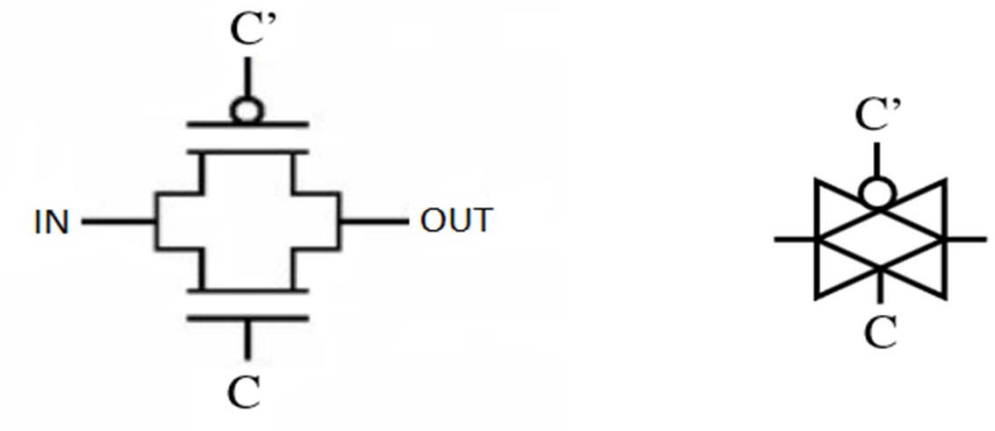
X	Y	$\overline{X+Y}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR



CMOS Transmission Gates

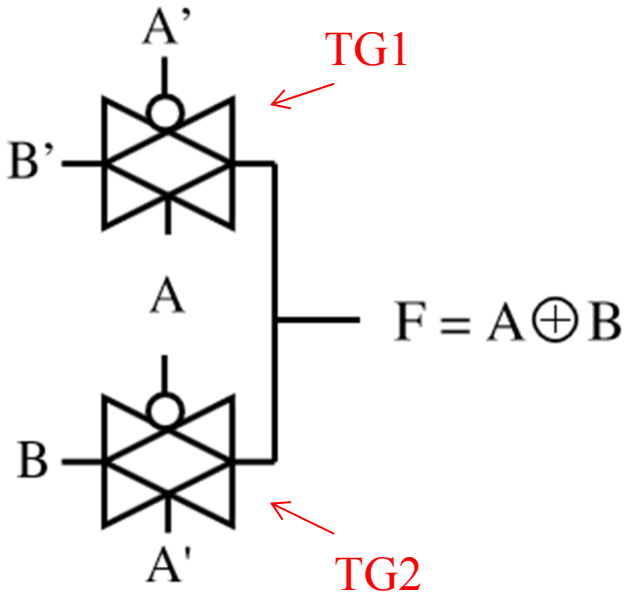
A transmission gate is formed when an nmos transistor is connected in parallel with a pmos transistor. It functions as an electronic switch controlled by input logic levels.



- Both transistors are ON or OFF simultaneously.
- The nmos switch passes a good zero but a poor 1.
- The pmos switch passes a good one but a poor 0.
- A bilateral switch passing a good 0 and good 1 in both directions.

XOR Function

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0



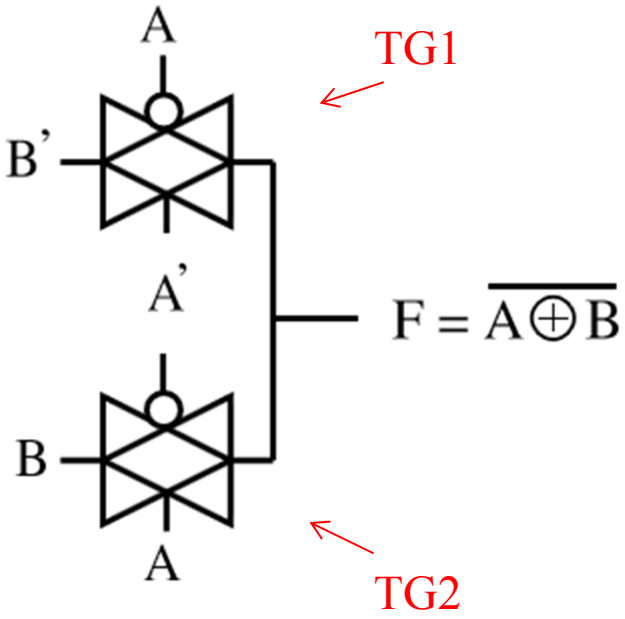
A	B	TG1	TG2	F
0	0	close	open	0
0	1	close	open	1
1	0	open	close	1
1	1	open	close	0

if A = 0 ⟶ F = B (pass B to F)

if A = 1 ⟶ F = B' (pass B' to F)

XNOR Function

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1



A	B	TG1	TG2	F
0	0	open	close	1
0	1	open	close	0
1	0	close	open	0
1	1	close	open	1

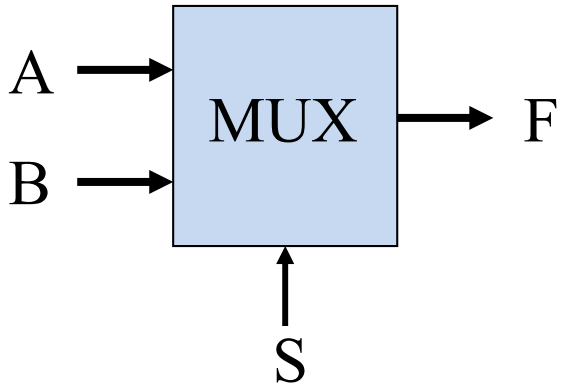
if A = 1 ⟶ F = B (pass B to F)

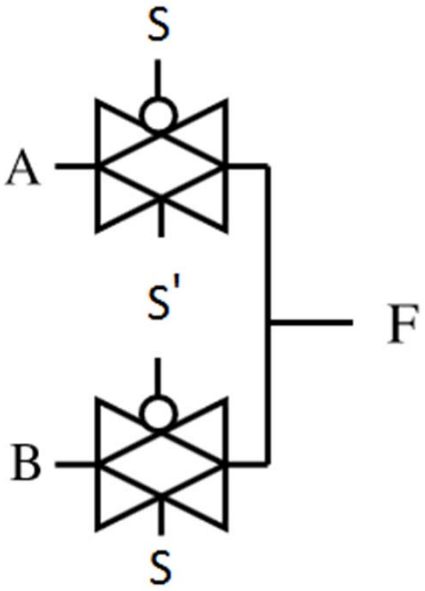
if A = 0 ⟶ F = B' (pass B' to F)

Multiplexer

S	F
0	A
1	B

Table entered variable





Transmission gates can be used to give an efficient solution for ‘steering’ logic. This is where a data path needs to be selected to switch one of several inputs to the output.