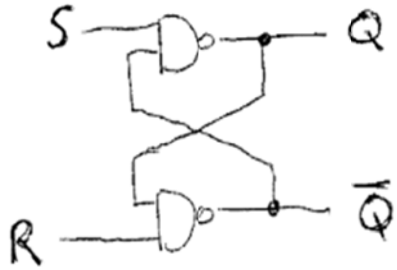
1.



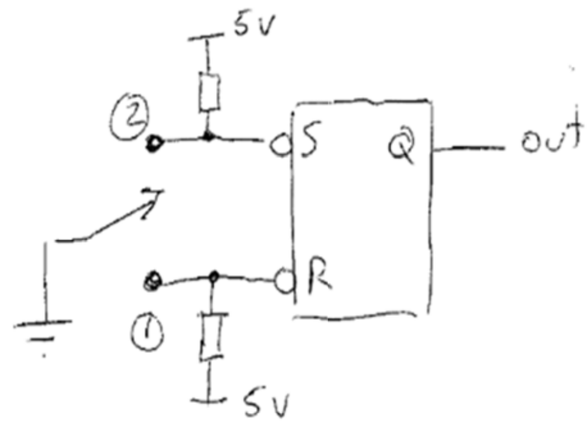
SR	Q'
00	not allowed
01	1
10	0
11	unchanged

Active low SR latch.
S = 0 set latch
R = 0 reset latch

$\overline{Q}$ must be inverse of Q

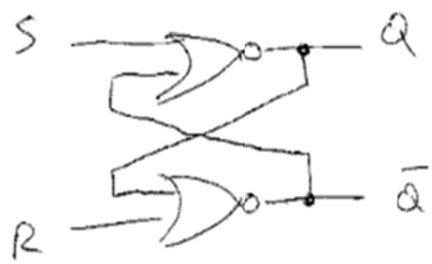
S = R = 1 no change
S = R = 0 not allowed as $Q = \overline{Q} = 1$

SR latch can be used to eliminate 'contact bounce' in a switch. Any bounce will be back to the 'unchanged' state.



See lecture notes for complete explanation.

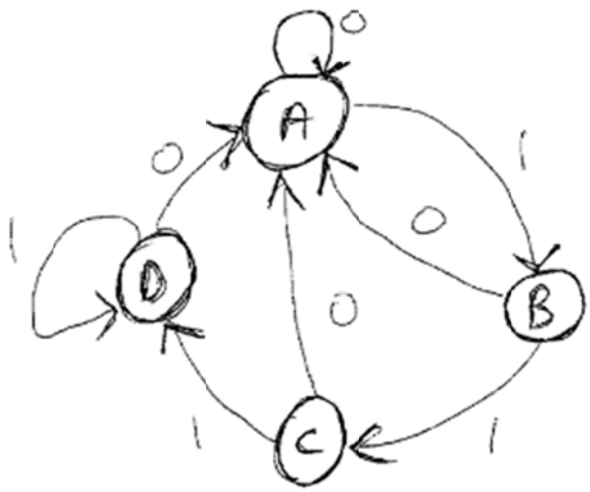
For active high inputs use NOR gates



SR	Q
00	unchanged
01	0
10	1
11	not allowed

2.

States
- A ⇒ no 1's found (reset state)
- B ⇒ first 1 found
- C ⇒ two ones found
- D ⇒ three ones found (at least)

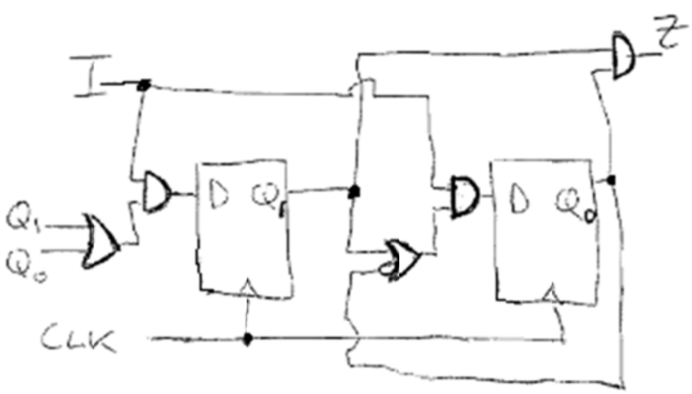


	Present state Q_1	Q_0	I	Next state Q_1'	Q_0'	Z
A	0	0	0	0	0	0
			1	0	1	0
B	0	1	0	0	0	0
			1	1	0	0
C	1	0	0	0	0	0
			1	1	1	0
D	1	1	0	0	0	1
			1	1	1	1

$$Z = Q_1 Q_0$$

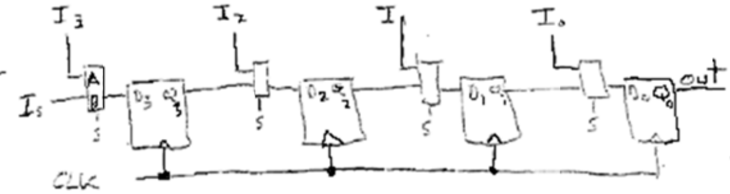
$$\begin{aligned} Q_1' &= \bar{Q}_1 Q_0 I + Q_1 \bar{Q}_0 I + Q_1 Q_0 I \\ &= \bar{Q}_1 Q_0 I + Q_1 I \\ &= (\bar{Q}_1 Q_0 + Q_1) I \\ &= (Q_1 + Q_0) I \quad * \end{aligned}$$

$$\begin{aligned} Q_0' &= \bar{Q}_1 \bar{Q}_0 I + Q_1 \bar{Q}_0 I + Q_1 Q_0 I \\ &= \bar{Q}_1 \bar{Q}_0 I + Q_1 I (\bar{Q}_0 + Q_0) \\ &= \bar{Q}_1 \bar{Q}_0 I + Q_1 I \\ &= (\bar{Q}_1 \bar{Q}_0 + Q_1) I \\ &= (Q_1 + \bar{Q}_0) I \quad * \end{aligned}$$



* Final steps make use of simplification theorem.

3.



	I_s	Q_3	Q_2	Q_1	Q_0
Initial state	0	x	x	x	x
↑	1	0	x	x	x
↑	0	1	0	x	x
↑	1	0	1	0	x
↑	x	1	0	1	0

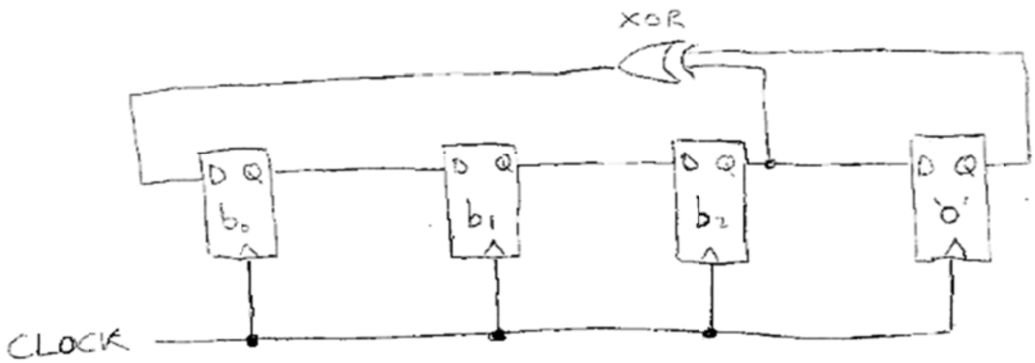
select chooses between $||^e$ load or serial shift

Parallel load uses 1 clock pulse, serial load uses 4.

Serial – over 1 wire slow/cheaper

Parallel – over several wires fast/expensive

4.



The rule for producing Gray Code tells us to copy down the MSB (same in Gray and Binary)
The 'hint' tells you how to do this in the circuit. Load the register as shown initially.

	b_0	b_1	b_2	0
↑	g_2	b_0	b_1	b_2
↑	g_1	g_2	b_0	b_1
↑	g_0	g_1	g_2	b_0

Three clocks later, the binary has been replaced with Gray Code.

5.

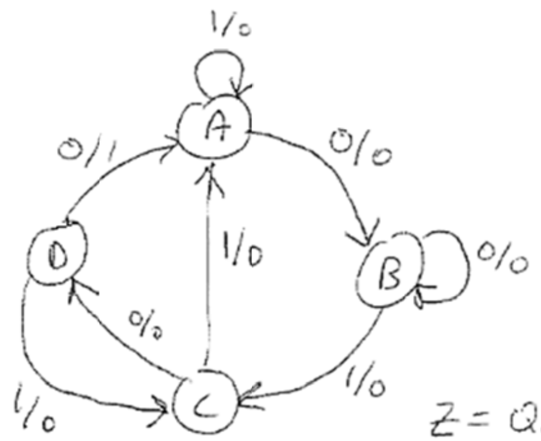
Find '0100'

A no bits found

B first '0' found

C found '01'

D found '010'



$Z = Q_1 Q_0 \overline{I}$

	Present State	Input I	NEXT STATE	OUTPUT
A	00	0	01	0
		1	00	0
B	01	0	01	0
		1	10	0
C	10	0	11	0
		1	00	0
D	11	0	00	1
		1	10	0

$$Q_0' = \overline{Q}_1\overline{Q}_0\overline{I} + \overline{Q}_1 Q_0 \overline{I} + Q_1\overline{Q}_0\overline{I}$$
$$= \overline{Q}_1\overline{I} + Q_1\overline{Q}_0\overline{I}$$
$$= \overline{I}(\overline{Q}_1 + Q_1\overline{Q}_0)$$
$$= \overline{I}(\overline{Q}_1 + \overline{Q}_0) = \overline{I}\,\overline{Q}_1 + \overline{I}\,\overline{Q}_0$$

[as $x + \overline{x}y = x + y$]

$$Q_1' = \overline{Q}_1 Q_0 I + Q_1\overline{Q}_0\overline{I} + Q_1 Q_0 I$$
$$= Q_0 I + Q_1\overline{Q}_0\overline{I}$$

Several circuit solutions are possible depending on your simplification of the equations.