**Data Provided: None**

The University Of Sheffield.

**DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING**

**Spring Semester 2015-16 (2.0 hours)**

**EEE6208 Advanced Integrated Electronics**

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

**You may require the following:**

*The Shichman-Hodges model:*

In the *triode* region:

$$I_D = K_n \frac{W}{L}\left(V_{OV} - \frac{V_{DS}}{2}\right)V_{DS}$$

In the *saturation* region:

$$I_{D0} = K_n \frac{W}{L}\frac{{V_{OV}}^2}{2}$$

In the *ohmic* region:

$$I_D \approx K V_{OV} V_{DS}$$

Regardless of the region:

$$I_S = I_D$$

$I_G = 0$

*Channel length modulation:*

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

*The overdrive voltage:*

For an NMOS device: $V_{GS} = V_{TO} + V_{OV}$

For a PMOS device: $V_{GS} = -(|V_{TO}| + |V_{OV}|)$

*MOSFET output resistance:*

$$r_o = \frac{1}{\lambda I_{D0}}$$

*MOSFET transconductance:*

$$g_m = K_{n,p}\frac{W}{L}V_{OV}$$

**1. a.** An NMOS transistor has the following parameters: $K_n$=150µA/V$^2$, $\lambda$=0.05V$^{-1}$, W/L=10µm/0.5µm,

**i)** What drain current results when this transistor runs with an overdrive voltage of 0.5V and a drain-source voltage, $V_{DS}$, of 2V? **(2)**

**ii)** What is the transistor's drain-source resistance, $r_o$, under these conditions? **(1)**

**iii)** If $V_{DS}$ increases to 2.5V, what is the corresponding change in drain current? **(2)**

**b.** The transistor described in **part a** is to be used, together with a PMOS active load transistor (M2), in the common-source amplifier configuration shown in **Figure 1.1**. Transistor M2 has an output resistance, $r_o$=200kΩ, transconductance parameter, Kp=200µA/V$^2$, turn-on voltage $V_{TO}$= -0.25V and channel aspect ratio W/L=20µm/2µm. The amplifier is to be operated with a bias current of 150µA.

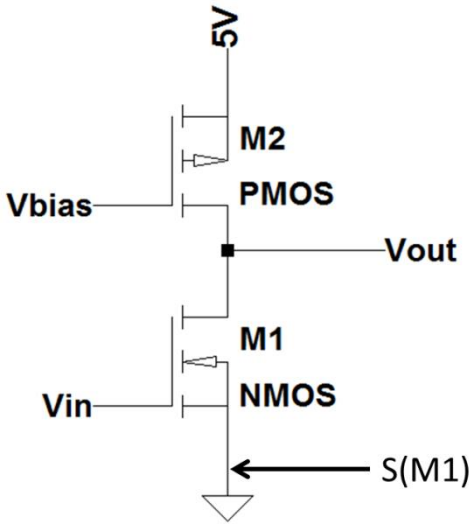


**Figure 1.1**: An actively-loaded common source amplifier.

**i)** Calculate a suitable value for $V_{bias}$ - the voltage at the gate of transistor M2. **(3)**

**ii)** Draw the small signal model of the circuit in **Figure 1.1** and calculate values of output resistance, $r_o$, and transconductance, $g_m$, to include in your diagram. **(5)**

**iii)** Calculate the gain of the amplifier from the small signal model. Show your working. **(3)**

**iv)** To realise the biasing of transistor M1, a current mirror or a resistor could be attached at the point labelled 'S(M1)' in **Figure 1.1**. Briefly describe the advantages of biasing at point S(M1) rather than using a potential divider at the gate of M1. Also briefly describe the advantages of using a current mirror rather than a resistor. **(4)**

**2. a.**

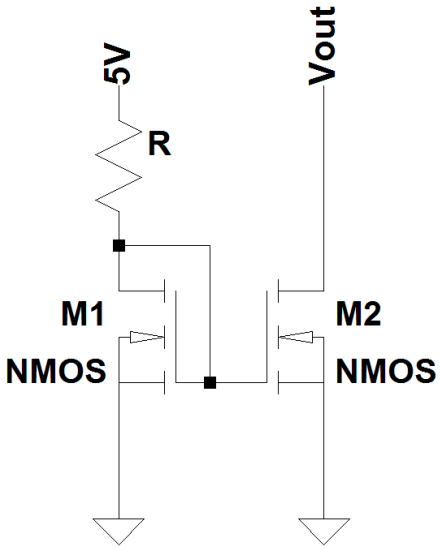


**Figure 2.1**: A basic current mirror

**Figure 2.1** shows a simple n-channel current mirror, implemented using two identical NMOS transistors, M1 and M2. Both transistors have transconductance parameter $K_n$=200μA/V$^2$ and turn-on voltages of $V_{TO}$=0.6V. They have channel dimensions W/L = 8μm/1μm.

**i)** Ignoring channel length modulation effects, calculate the value of R required to set the drain current through M1 at 100μA. **(4)**

**ii)** What is the minimum value of the voltage across M2, $V_{out}$, in order that the mirror operates correctly? What region of operation will M2 fall into if $V_{out}$ falls below this value? **(2)**

**iii)** Given that the transistors have a channel length modulation parameter $\lambda$=0.04V$^{-1}$, find the change in the current through M2 if $V_{out}$ reduces by 1V. **(3)**

**b.**

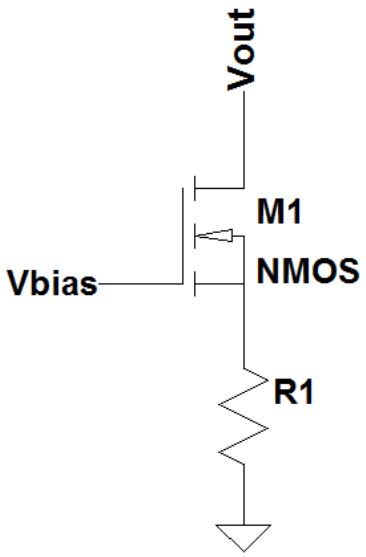


**Figure 2.2**: The output side of a source-degenerated current mirror.

**Figure 2.2** shows the output side of a source-degenerated current mirror, with source resistance $R_1$.

**i)** Draw the small-signal model of this circuit. **(3)**

**ii)** Use nodal analysis to show that the output resistance, $R_{out}$, of the current mirror in Figure 2 is given by:

$$R_{out} = \frac{1}{g_o}(1 + R_1(g_o + g_m))$$

**(6)**

Where $g_m$ is the transconductance of transistor M2, $g_o=1/r_o$ is the drain-source conductance of transistor M2.

**iii)** Give conditions under which $R_{out}$ can be approximated by: $R_{out} \approx g_m R_1 r_o$ **(2)**

**3. a.** **i)** Explain what is meant by *strained silicon* technology. How does this improve the performance of CMOS transistors? **(4)**

**ii)** Describe what you understand by the term *FinFET*. What are the advantages of FinFET technology? **(4)**

**b.** Consider the circuit shown in **Figure 3.1**. You may assume that the inverter switches at $V_{DD}/2$.

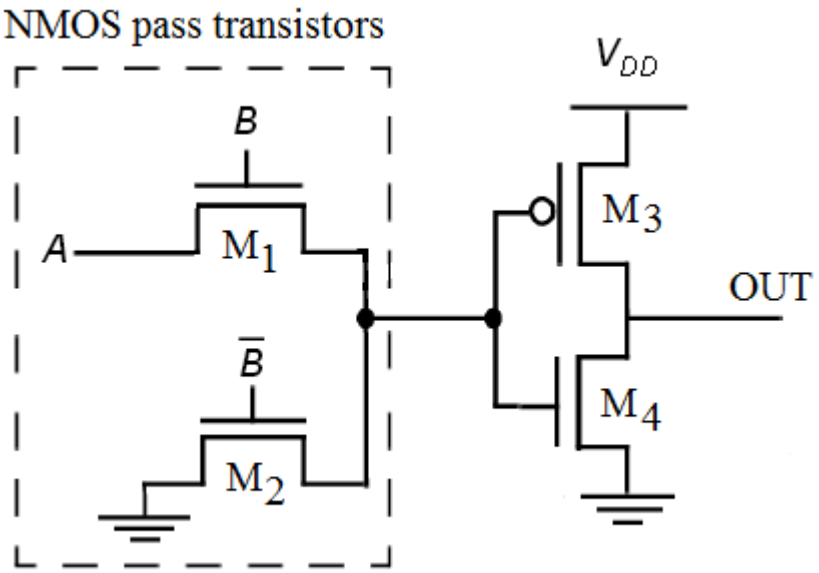


**Figure 3.1** Pass transistor circuit

**i)** Determine the logic function performed by this circuit. **(3)**

**ii)** Assuming that gate leakage can be ignored, explain why the circuit has non-zero static power dissipation. **(4)**

**iii)** Using only one additional transistor, show how the circuit can be modified to reduce the static power dissipation. **(2)**

**iv)** Explain how you would determine the size of the additional transistor. **(3)**

**4.** **a.** Two NMOS transistors are to be connected in series using a bulk CMOS process. Describe with the aid of a diagram what is meant by:

**i)** Isolated contacted diffusion **(2)**

**ii)** Shared contacted diffusion **(2)**

**iii)** Merged diffusion **(2)**

**b.** **i)** Describe the capacitances associated with a MOSFET device. **(3)**

**ii)** The diagram in **Figure 4.1** shows a unit inverter driving a unit inverter load. Explain with the aid of a diagram why the equivalent RC load of the driving inverter has a resistance of R and a capacitance of 6C. You may ignore interconnect capacitance. **(4)**

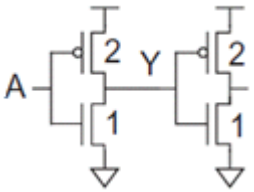


**Figure 4.1** Unit inverters

**c.** **i)** Draw the circuit diagram for a static CMOS 2-input NOR gate. Determine the transistor widths required to achieve effective rise and fall resistances equivalent to that of a unit size inverter. **(3)**

**ii)** The NOR gate is required to drive *h* identical NOR gates. Using the Elmore delay model, derive an expression for the RC propagation delay of the driving NOR gate for a rising transition on its output. Assume that isolated contacted diffusions are used for every source and drain. **(4)**

**AM/NJP/IF**