Data Provided: MIL-HDBK-217F, 6.4 Transistors, Low Frequency, Si FET

The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2005-2006 (2 hours)

Reliability and Failure EEE6008

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Suppose the fraction of transistors that fail up to time, t, is given

$$F(t) = 1\text{-}\exp(-0.003t),$$

where t is measured in hour.

i) Calculate the probability that a new device will fail after 100 hours and after 200 hours. Work out the probability of device failure after operating between 100 hours and 200 hours. **(4)**

ii) Show that the failure rate, $\lambda(t)$, is independent of time and hence obtain the mean time to failure, MTTF, for the devices tested. **(5)**

b. The constant failure rate model such as that based on specifications given by the MIL-HDBK-217F has been used by many companies.

i) Using the MIL-HDBK-217F specifications supplied at the end of the paper, calculate the failure rates for a low-frequency silicon field-effect-transistor.
(*Assume plastic encapsulated small signal switching MOSFET operating at 40^{o}C and used in space flight* (S_F)). **(5)**

ii) Outline three advantages and three drawbacks of using the MIL-HDBK-217F. **(6)**

2. a. List two possible defects or contaminants that can be introduced in **each** of the following IC processing steps: chemical vapour deposition, ion implantation, plasma processing and lithography. **(8)**

b. i) Sketch illustrations of films under residual tensile and compressive stress, when the film and the substrate have different coefficients of thermal expansion. **(4)**

ii) Describe how the tensile and compressive stress can develop in film/semiconductor layers. **(4)**

c. Explain the reasons for vacancy and interstitial defects in semiconductor materials. Discuss whether these defects are likely to cause failures in silicon-based ICs. **(4)**

3. a. Explain the key differences between electrical overstress and electrostatic discharge (ESD). **(4)**

b. i) Explain how electrostatic discharge can cause junction burnout in a semiconductor device. **(3)**

ii) List three strategies to minimise the risk of ESD damage to sensitive electronics. **(3)**

c. Draw the equivalent circuit for the human-body model commonly used for simulating ESD. **(4)**

d. A pulse of 3000 V is discharged from a person into a photodiode with an area of 4×10^{-8} m^2 and a resistance of 20Ω. Assume negligible voltage drop across the photodiode and the human-body model is valid.

i) Calculate the time constant of the discharge and estimate the time span over which the discharge occurs. **(3)**

ii) Calculate the maximum current density flowing through the photodiode. **(3)**

4. **a.** i) Draw a basic schematic diagram of a scanning electron microscope (SEM), labelling the key features clearly. **(4)**

ii) Briefly describe how a SEM works. **(6)**

b. Outline the principles of operation of the electron beam induced current (EBIC) mode in SEM. **(2)**

c. An electron beam is scanned across a p-n junction from position A to position B, as illustrated in Fig. Q.4.1.

i) Describe and explain the expected behaviour of the EBIC current as the beam is scanned. **(3)**

ii) Sketch and label the current induced as a function of beam position. **(2)**

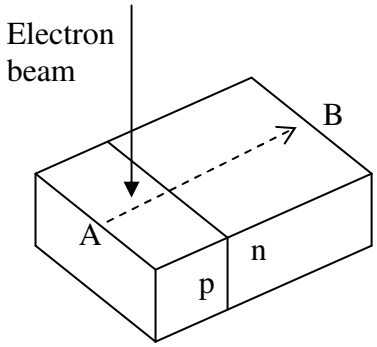

Fig. Q.4.1

d. Describe how the EBIC mode can be used to characterise defects of a p-n junction. **(3)**

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