Exam Feedback: EEE225 June 2013

General Comments on Q1 and Q2. If a question asks you to 'explain' something with 'the aid of a diagram', you are required to write down an explanation **and** draw a diagram to get the marks. A diagram or explanation alone will not get full marks.

Q1: A very disappointing attempt was made at part (a) which was just bookwork. Most students knew what a tri-state output was but very few could explain open-drain and wired-AND even though this was straight from the notes. This should have been 8 easy marks. Part (b) was well attempted by most students. Part (c) was a bit harder but actually, could be viewed as extended bookwork with a more difficult explanation. It required a deeper understanding and few students showed this.

Q2: Part (a) generally well attempted. Part (b) was poorly attempted. Many diagrams contained oval Mealy type output boxes even though the question asked for a Moore type solution. More explanation was required to define what the states and variables represented. Part (c) was poorly attempted. It required you to use your digital knowledge to divide down a clock frequency and combine this with material from the final lecture in which problems with clock skew were detailed and clock skew avoidance strategies discussed.

General Comments on Q3 and Q4: I was quite pleased by your attempt at questions 3 and 4. The paper followed the same style as the relevant parts of the old EEE204 and most people had no problems understanding what was wanted. Many marks were lost because of silly numerical and algebraic errors and whilst each error only loses one mark, some of you were totting up quite a few that you could ill afford. There was very little checking of whether an answer was sensible. **If you are doing an analysis, you need to draw a circuit diagram** – how else can I credit correct formulation of equations describing the circuit? You need to explain briefly (three or four words is usually enough) what you are doing so that I can follow your thinking.

Q3: Most people managed part (a). Those who didn't tried to manage without drawing a circuit diagram so I couldn't follow what they were doing. About three people stated their assumptions. In part (ii) some highly original combinations of transistors were sketched - between half and two thirds of them were acceptable. Part (iii) was attempted in the main by people who had attempted part (ii). Most managed one advantage but a smaller number managed two. In part (b) (i) most people successfully worked out the 3dB bandwidth. In part (ii) it was necessary to recognise that you were dealing with a first order system with known dc gain and -3dB frequency. It was then a case of working out the modulus and phase of a complex expression - too many people for comfort have not mastered this first year skill. In part (iii) most people could find the gain but in part (iv) the answer was reached by only a few. Quite a few recognised that they were looking for the -1.5 dB frequency in each section of the cascade to get the overall -3dB frequency. The commonest error in working out the -1.5 dB frequency was forgetting the 2π that links Hz to radians per second.

Q4: In part (a) (i) most of you got the right answer. The ones that didn't had trouble with the R_1-C arm in figure 4 which becomes infinite impedance at 0 Hz. Most managed the transfer function analysis of part (ii). In part (iii) the most common problem was interpreting the transfer function correctly to identify what part of it was related to the - 3dB frequency. In part (a)(iv) most people drew labelled sketches and got the marks. One or two drew completely unlabeled lines that looked as if they had suffered a nervous twitch while their pencil happened to be in contact with the paper. No labels and, in some cases, no axes. In part (b) (i) the first challenge was remembering the definition of noise factor. Most people did remember this but a significant number forgot that it was a power (or mean squared voltage) ratio. In part (b) (ii) most people knew what signal to noise ratio was although many forgot that it was a power ratio. Many of you weren't quite sure what to do with the bandwidth.

General comments on Q5 and Q6. Both these questions have appeared in many forms over the last few years.

Q5: Part (a) is the same as the first part of one of the questions in at least each of the last three years. The main problem was a failure to answer all four parts of the question - it is important to read questions very carefully. In part (b) most people found n_i and N_D but then didn't use that information to answer the question asked. Very few of you managed to explain correctly what would happen if the temperature was reduced. Most people made a successful attempt at part (c) and in part (d) the diagrams were generally good but the explanations poor

Q6: Part (a) has cropped up quite frequently in the past and, as in the past, the main problem was a lack of care in the drawing that led to small but crucial errors that could not be overlooked. In part (b) many of you simply stated the required relationship when the question asked you to derive it. In part (c) only a few of you realised that if drain and gate are connected together, VGS = VDS. Some people realised that in part (d) V_T was 3 V. Many of those who did were not able to use this deduction sensibly. There were very few suggestions as to possible uses for this device