Data Provided: None

The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2004-2005 (2 hours)

Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. i) Explain why the interconnect (or wiring) between gates on a typical ASIC is becoming increasingly important and problematic and how the problems worsen as technology shrinks. **(6)**

ii) what can be done to address the problems identified in **i)**? **(2)**

b. i) Show how using repeaters can reduce the delay experienced by a signal passing along a long wire. **(4)**

ii) What other benefits arise from inserting repeaters **(2)**

c. In a particular technology, for the only available buffer, the output capacitance, C_{out}, is 10fF whilst its input capacitance, C_{in}, is 1.5fF and its effective output resistance is 400Ω. The capacitance per unit length of the wiring is 0.3fF/μm and its resistance per unit length is 2.9Ω/μm. A circuit is set up as shown in **Figure 1**.

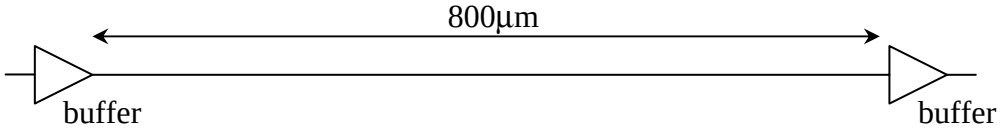

Figure 1

i) Estimate the original delay; **(2)**

ii) Identify how the circuit might be improved to minimise its delay; **(2)**

iii) Estimate the minimised delay. **(2)**

2. **a.** Show that the relationship between the applied voltages and drain current for a *n*-channel FET with a long channel can be expressed as:

$$I_{DS} = \frac{\mu_E \cdot C_{OX} \cdot W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

where the terms have their normal meanings – ensure that your answer includes a schematic of the FET with the voltage polarities and current directions shown. **(6)**

b. An n-channel transistor in a digital CMOS circuit might be simply modelled as a resistance whose effective value, R_o, is:

$$R_o = \frac{2}{\beta(V_{DD} - V_T)}$$

where the terms have their usual meaning. What is the significance of this equation for circuit performance (especially when sub-threshold conduction is considered)? **(4)**

c. A CMOS circuit has the pull-up network shown in **Figure 2**:

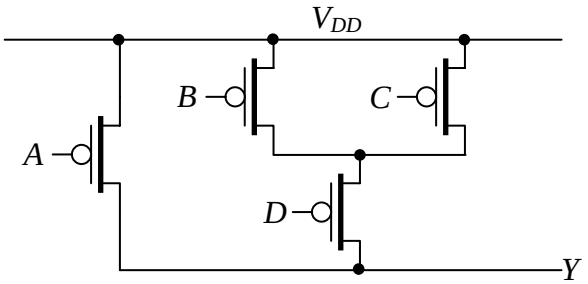

Figure 2: CMOS Pull-Up Network

For this pull-up network:

i) draw the corresponding pull-down network; **(3)**

ii) determine the function, *Y*, of the logic gate; **(3)**

iii) size all of the transistors for a minimum-sized gate (assuming that the mobility of holes is half that of electrons) in terms of the minimum transistor width, *W*. **(4)**

3. An IC fabricated in 0.13μm CMOS technology contains 20 million, two-input, minimum sized NAND gate equivalents and approximately 500m of interconnect. For the fabrication technology, you know that a minimum-sized *n*-channel FET is 0.13μm long and 0.3μm wide, the gate oxide ($\varepsilon = 3.45\times10^{-11}$F/m) is 5nm thick, and that the hole mobility is half that of electrons. Furthermore, it is known that the average width of the interconnect wire is 0.75μm and the ratio of height to width of each interconnect wire is 1.6 and it is estimated that the average thickness of dialectric ($\varepsilon = 3.1\times10^{-11}$F/m) around each interconnect wire is approximately 0.75μm also.

a. For a NAND gate equivalent (without any interconnect attached), estimate:

i) the input capacitance of each input; **(3)**

ii) the output capacitance **(3)**

b. Estimate the total capacitance due to the interconnect on the IC. **(3)**

The power supply voltage to the core logic is 1.2V. It is estimated that I/O pads consume 30% of the total power consumed by the IC and that leakage currents in the core logic consume another 10% of the total power. The core logic in the IC is clocked at 1GHz and 5% of the interconnect and 5% of the logic circuits are dedicated to clock distribution. It is estimated that in the remainder of the core logic, the signals change state on the rising edge of the 1GHz clock with a probability of 0.2.

c. Show that the dynamic power consumption as a consequence of switched capacitance in a CMOS circuit is:

$$P_{sw} = \alpha . f_{clk} . V_{DD}^2 \sum_{i=1}^{n} C_i$$

ensure that you define the terms and any approximations that are made in reaching this result. **(4)**

d. Estimate the total amount of power consumed by the IC and comment on the figure. **(7)**

4. **a.** Show how the cost associated with a processed Si wafer might be estimated. **(4)**

b. **i)** What is yield and what factors influence it? **(2)**

ii) Give one expression that has been used to model random yield. **(2)**

c. How does process variation affect the functioning of an IC? Ensure that you distinguish between variation across a population of ICs and within an IC, and give an example. **(4)**

d. Distinguish between the following and identify the factors that are making each of them increasingly difficult and problematic:

i) Verification **(4)**

ii) Manufacturing Test **(4)**

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