Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2006-2007 (2 hours)

High Speed Electronic Devices 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

You may require :- Electron saturation velocity (Si or GaAs) $v_{sat} = 1 \times 10^5$ ms^{-1}

1. a. Sketch the cross-sectional arrangement for the basic CMOS inverter cell, showing the various doped regions and location of the gates, sources and drains. What is the main advantage of the CMOS layout? **(4)**

Using a basic circuit, explain how the cell operates from an inverter logic point of view. **(4)**

b. During the process of miniaturisation of an NMOS device, the dimensions and voltages are scaled (reduced) by a scale factor K (>1). Assuming that the p-doping is increased by K, outline the reasons why the gate capacitance per unit area increases by K and drain current remains constant with K, provided velocity saturation applies to transport under the gate. Similarly indicate how the switch delay, the power consumption per device and power-delay product are affected by this scaling factor under velocity saturation conditions. **(8)**

How is the power density under velocity saturation conditions affected by this scaling and what are the implications of this for cooling as chips get larger and more complex? At some point voltage cannot be scaled as fast as the device dimensions. What effect on power density will this have? **(4)**

2. a. The breakdown condition for a Schottky diode with an effective depletion length, d, is

$$\int_0^d \alpha dx = 1$$

where α is the ionisation coefficient for electrons. A HEMT power device is required to operate at a drain-source voltage of 10 V. By calculation, indicate whether this operating voltage is compatible with the gate-drain breakdown voltage where $\alpha = 1\times10^{-30}\,E^5$ m^{-1} and E is in Vm^{-1} and the gate-source distance is 1

μm. Assume that the pinch-off voltage is much smaller than the breakdown voltage and that the semiconductor above the channel is undoped. **(6)**

The breakdown voltage of FETs can be increased by increasing the gate-drain spacing. Explain the disadvantage of this in terms of speed of operation and how this might affect the output characteristics. **(4)**

b. Fig 2 shows the simplified small signal equivalent circuit model of an FET where v_{GS} is the ac voltage signal applied to the gate-source terminals and g'_m is the extrinsic transconductance. Assuming that $R_G << R_S$, the output conductance, g_D, is zero and C_{DG} and C_{DS} can be neglected compared to C_{DS}, use the definition of the cut–off frequency, f_T (frequency where ratio of drain current to gate current = 1), to derive an expression from this circuit which shows that f_T is independent of the source resistance, R_S.

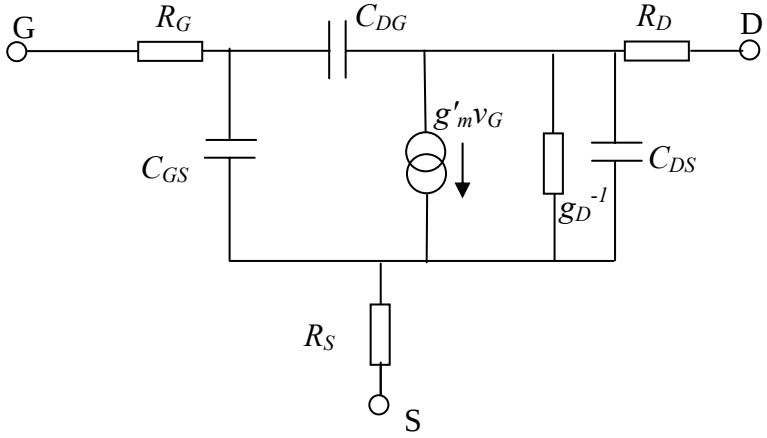

Fig 2

(8)

c. The limits of UV photolithography do not allow device feature line-widths below about 0.5 μm. *Estimate* the maximum cut-off frequency possible in a GaAs MESFET under this limit. State any assumptions made. **(2)**

3. a. Explain, with the aid of diagrams, the principal differences between a MESFET and a high electron mobility transistor (HEMT), emphasising the main advantage resulting from the HEMT design. Increasing the channel conductance is desirable in power devices. What are the problems in increasing the channel thickness in MESFETs to achieve this? **(8)**

b. The intrinsic transconductance per unit gate width of a MESFET can be described by

$$g_m \propto \frac{aN_d\mu}{L}$$

where a, N_d and L are the channel thickness, doping concentration and length respectively. If the 77 K mobility, μ, in GaAs is the same for HEMTs and MESFETs (0.3 $m^2V^{-1}s^{-1}$) what relative increase in g_m is expected for the HEMT as both devices are cooled to 10 K? You can assume that $\mu \propto T^{1.5}$ for the MESFET between 10 K and 77 K and is constant with temperature in the HEMT. **(6)**

c. Calculate the transit time frequency in the two devices at 10 K with the same geometry (gate length 0.5 μm) and source-drain voltage of 1 V. Suggest reasons why these values be an overestimate? **(6)**

4. **a.** Fig 4 shows a simplified small signal equivalent circuit for a bipolar transistor. Interpret this circuit in relation to the heterojunction bipolar transistor (HBT) and identify which of those parameters shown will be improved over a Si bipolar transistor, leading to higher gain *and* operating frequency when a typical HBT structure is used. Explain why this improvement comes about in each case.

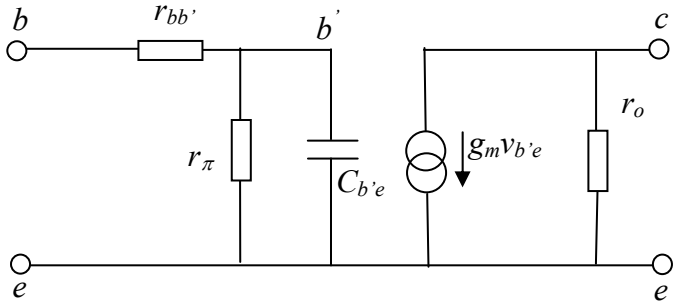

Fig 4 **(6)**

b. An HBT is made from an AlGaAs emitter (band gap 1.9 eV) and a GaAs base and collector (band gap 1.43 eV). *Estimate* the electron-to-hole injection ratio improvement from this HBT over a Si bipolar device with the same doping levels *(hint: the current across a barrier is proportional to the exponential of the respective barrier height presented to the charge carriers)*. You may assume that the emitter/base junction in the HBT has been graded compositionally so that it does not have a discontinuity in the conduction band. Describe the main mechanism likely to limit the gain of an HBT. **(8)**

c. Consider the layout differences between FETs and bipolar transistors and decide which might offer better high power performance. Compare the ease of fabrication of these devices with regard to very high frequency operation. **(6)**

PAH / RAH