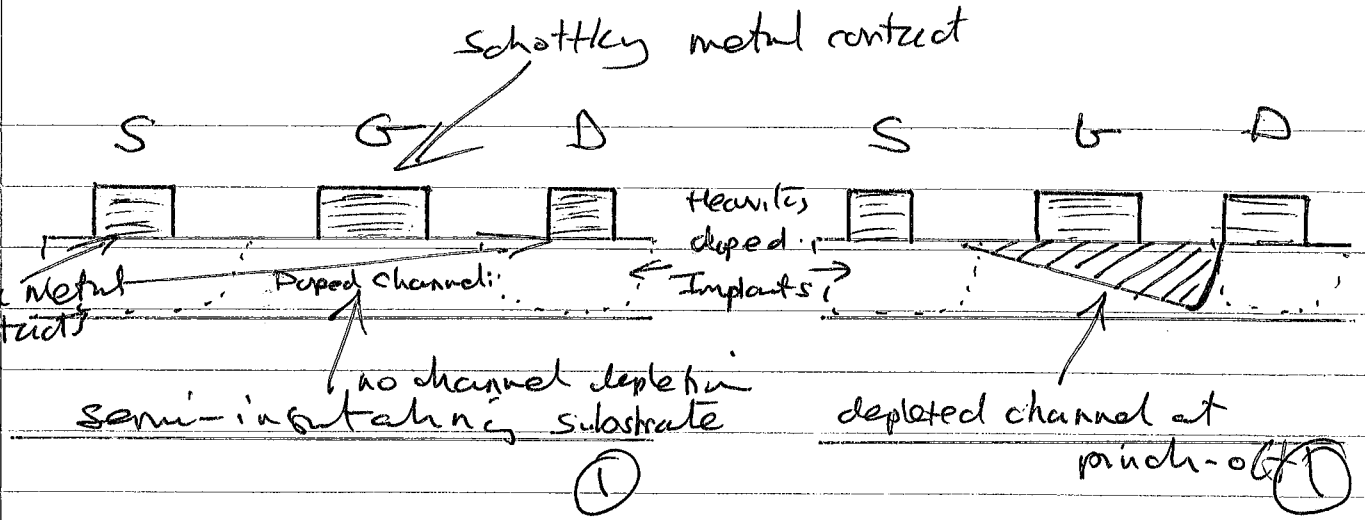
1a)



(1)

Channel at pinch-off – low, but finite conductivity. Channel cannot completely close otherwise charge would just accumulate and electrostatically oppose the depletion. Depletion width can only extend towards the drain.

Very high fields under very narrow remaining channel – carriers at saturation velocity (2)

Further increases in V_G ($+V_D$) increase the field between Gate and Drain. E-field sufficient to cause impact ionisation – large current flows, (1) unstable unless current regulated.

1b) MOSFET – Structurally similar except for thin oxide (dielectric). No metal schottky contact → no electron flow from metal to semiconductor. MOSFET relies on a polarisation or image charge.

Precise design depends on the MOSFET mode.
- Enhancement – channel created by inversion of opposite semiconductor type
- depletion – more similar to MESFET conducting channel created. (by implanting) (1)

1b) cont

(ii) MOSFET – both enhancement (normally off) + depletion (normally on) modes (1)

MESFET – Depletion only (1)
– Enhancement generally not possible due to finite Schottky barrier (typ < 1V)

(iii) MOSFET – Channel at surface (semi-oxide iff) low mobility due to carrier scattering (charge trapping, surface states etc)

MESFET – Channel away from surface higher (bulk like) mobilities. (1)

(iv) MOSFET – Needs high quality oxide/dielectric Interface relatively inert/stable Excellent reproducibity in modern process

MESFET – Needs high quality metal-semi schottky contact. Can easily be affected by surface quality and complex semi-metal chemistry harder to achieve reproducable process. (1)

MESFET – Difficult to create enhancement mode – Normally ON (1)
static power dissipation

MOSFET has largely displaced MESFET, yet – (1)
MESFET has some advantages in:

- High speed – reflecting higher mobility
- Low noise – reduced effect of trapped charge
- High power – high mobility + current density better scalable with increasing gate width. (1)

1c) Drain current 50μA at $V_G = 1.0$

-value at 2.0V, 3.0V.

$$I_D = \left(\frac{Z\mu}{L} C_{ox}\right)\left[V_G - V_T - \frac{V_D}{2}\right] V_D \quad (1)$$

$Z = 20\mu m$, $C_{ox} = 2\times10^{-6}$, 0.06, $L = 500nm$

(4.8×10^{-5})

$$I_{D1} = (\quad)\left[V_{G1} - V_T - \frac{V_D}{2}\right] V_D \quad (1)$$

$$I_{D2} = (\quad)\left[V_{G2} - V_T - \frac{V_D}{2}\right] V_D \quad (1)$$

$$I_{D2} - I_{D1} = (\quad)\left[V_{G2} - V_{G1}\right] V_D$$

$V_G = 2V$

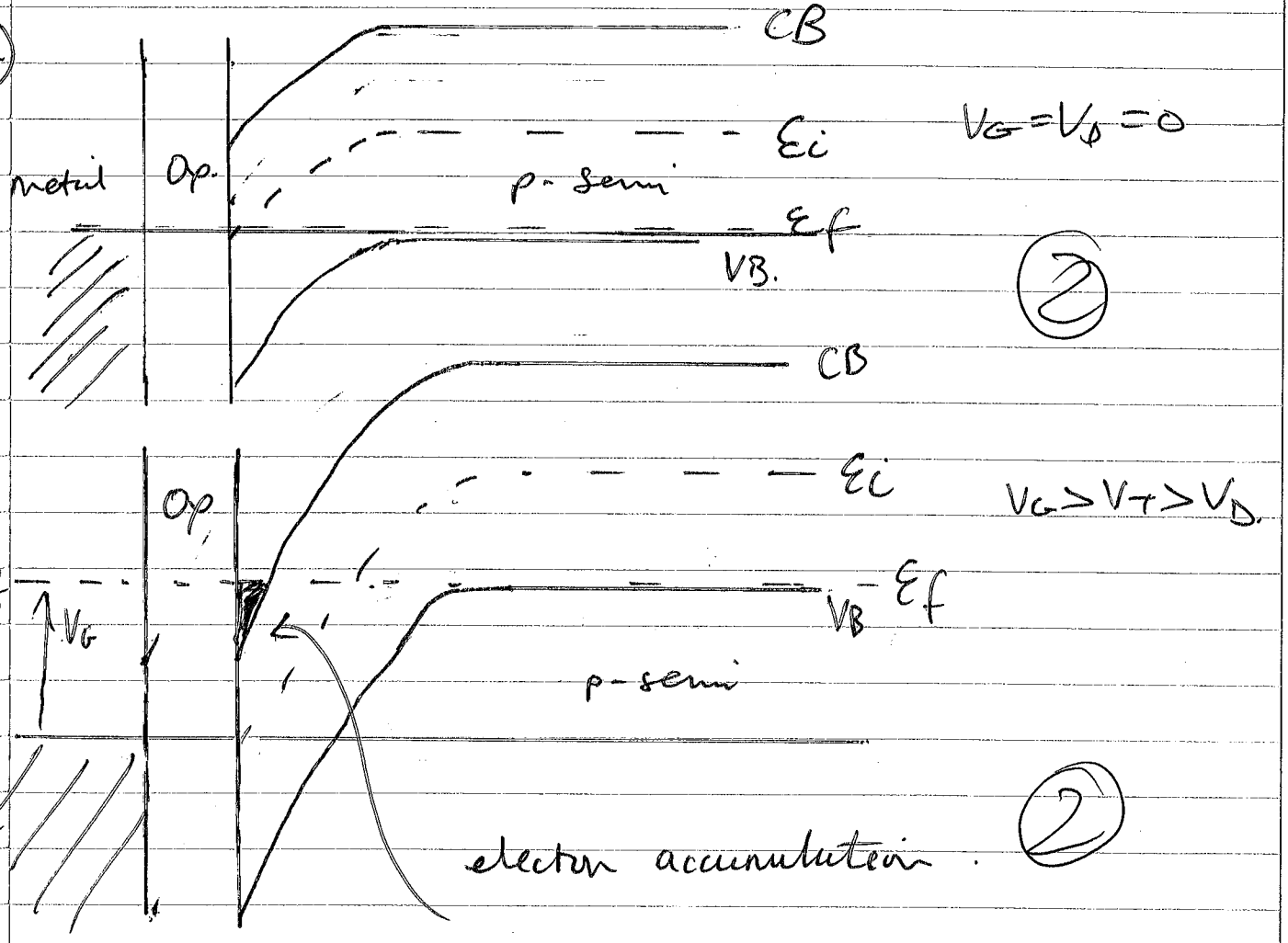
$$I_{D1} - I_{D2} = (\quad)\left[1.0\right] 0.4$$

$$= 19\mu A$$

$V_G = 2V \quad I_D = 50 + 19 = 69\mu A$ (1)

$V_G = 4V \quad I_D = 69 + 38 = 107\mu A$ (1)

1(d)


CB
$\mathcal{E}_i$
$V_G = V_D = 0$
metal
Op.
p-semi
$\mathcal{E}_f$
V_B.
2
CB
$\mathcal{E}_i$
$V_G > V_T > V_D$.
Op.
$\mathcal{E}_f$
V_G
V_B
p-semi
electron accumulation.
2

~~2~~)

2a

(i) Lithography

- Needed for device scaling - gate length μm → nm
- reduced gate length improves f_t, f_{max}, g_m, allows for higher transistor density

Critical feature size $\propto \frac{\lambda}{N_A}$

- reduce λ - visible - UV - EUV
  or ebeam, xray - short de Broglie wavelength
- increase N_A - immersion optics
- also 'tricks' - double patterning etc.

Depth of focus a problem

EUV technology difficult / expensive (sources, optics) (2)

(ii) High K.

Scaling down device size tends to mean a reduction in C_{Gate}. Need to maintain this otherwise I_D, g_m etc would be reduced. Effect $\propto \frac{1}{d_{ox}}$

yet cannot indefinitely reduce t_{ox} due to increase in tunnelling

High oxides, such as HfO_2 have been developed with substantially increased dielectric constant

- can offset this trend to low oxide thickness. (2)

Other rare-earth oxides / nitrides available, but have complex chemistries

(iii) Strain

- lifts degeneracy of valence band and alters the relative energy of conduction band satellites

29 cont) Compressively strained SiGe pMOS
- major improvement in hole mobility, increases g_m, f_T etc and makes the pMOS device more complementary to the nMOS performance

Tensile strained nMOS SiC stressors.
- small improvement in nMOS performance due to influence on CB satellite valleys.

Amount of ~~strain~~ strain is limited by strain relaxation processes (dislocations). (2)

(iv) III-V materials
III-V materials such as GaAs, InGaAs, InP have substantially higher electron mobilities ~~and~~ and saturation velocities
Their use could substantially increase g_m & f_T especially for nMOS. (2)

Current thinking - InGaAs nMOS, SiGe pMOS

Challenge is to integrate these materials - strain relaxation, polar or non polar etc,

Ultimate application may lie with narrow gap III-Vs such as InSb. However the mismatch is higher and the narrow gap is an issue for breakdown.

More Moore - Moores law of device scaling continues. ~~Materials, processes~~ advance and physical barriers to scaling are overcome.

More than Moore

device advances do not follow the established scaling route but instead develop using an entirely new approach or by adding increased functionality

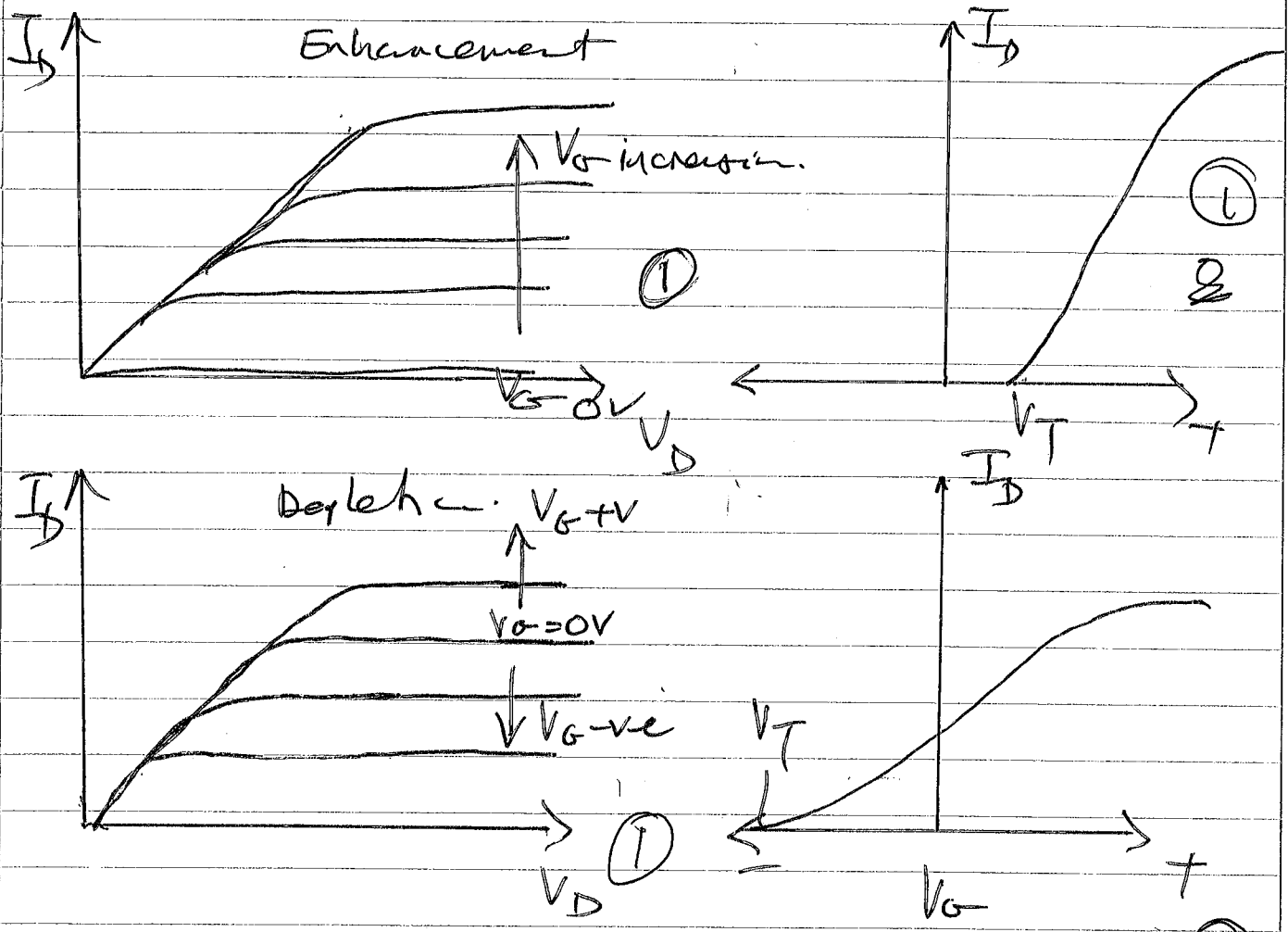
29 cont'

There are many examples, but these could include Entirely new physical processes; - quantum point transistor, quantum computing, photonic integration, integration of diverse technologies such as MEMS, multidimensional topographies, biological computing

(1)

(1)

2b)



Enhancement - Normally off device - zero or v. low power dissipation in off state (below V_T)
Depletion - difficult to realise digital logic with normally-on device. Higher power dissipation
Depletion mode can suffer variabilities in V_T - process is more demanding

~~Registered~~ ~~Depletion~~ mode - Circuits requiring normally-on switching characteristics, current/power regulation (depletion mode FET acting as a variable resistor)

~~Removed~~

2c $f = f_T$ when current gain = 1

output $= g_m V_G$ (1)

input $= W C_{ox} 2L V_G$ (1)

output = input $\quad g_m = \dfrac{W_T C_{ox} 2L \cancel{V_G}}{\cancel{V_G}}$

$g_m = 2\pi f_T \, 2L$

but $g_m = \dfrac{2\mu C_{ox}}{L}[V_G - V_T]$ (1)

$f_T = \dfrac{2\mu C_{ox}}{2\pi L^2 2}[V_G - V_T]$ (1)

increased related by $\dfrac{1}{L^2}$ small gate length critical

increased related by μ = high mobility (1)

increased by C_{ox}

decreased by 2

3a) $\tau_{EC} = \tau_{BE} + \tau_{BC} + \tau_B + \tau_C$ (1)

τ_{BE} - Time required to charge the base-emitter junction - capacitance related (1)

τ_{BC} - Time required to charge the base collector junction - capacitance (1)

Both

$$\tau_{BE} = \frac{dQ_{BE}}{dI_E} = C_{BE}\frac{dV_{BE}}{dI_E}$$

$$= \frac{kT}{qI_e} C_{BE} \simeq \frac{kT}{qI_C} C_{BE}$$

since $I_e \simeq I_C$ (1)

Similarly

$$\tau_{BE} = C_{BE}\frac{dV_{BC}}{dI_C}.$$

Kirchoffs law $\Delta V_{BC} = \Delta V_{BE} + \Delta I_C(r_e + r_c)$

$$\tau_{BC} = C_{BC}\left(\frac{dV_{BE}}{dI_C} + r_e + r_c\right)$$

~~since~~ I_C Capacitance + resistance

$$= C_{BC}\left(\frac{kT}{qI_C} + r_E + r_E\right)$$

τ_B - electron diffusion through base (1)

$\tau_B \frac{W_B^2}{2D_e}$ pure resistance. (1)

$\tau - \tau_C = \frac{W_C}{2v_{sat}}$ pure resistance (1)

To improve τ_{EC}

- increase I_C, I_E – high bias
- reduce parasitic resistances
- reduce capacitances – reads

(2)

(i) $\tau_{BE} = C_{BE}\left(\frac{kT}{qI_C}\right)$ $\qquad \frac{kT}{qI_C} = 0.26$ ← 10mA

$C_{BE} = 20pF \cdot \tau_{BE} = 5.2ps$

(1)

(ii) $\tau_{BE} = C_{BC}\left(\frac{kT}{qI_C} + r_E + r_C\right)$

$C_{BC} = 15pF \qquad 15(0.26 + 0.3 + 0.2) = 11.4ps.$

$r_B = 0.3\Omega$

$r_C = 0.2\Omega$

(1)

(iii) $\tau_B = \frac{W_B^2}{2D_E} = \frac{(0.25\times10^{-6})^2}{2\times3.9\times10^{-3}} = 8.0ps$

$W_B = 0.25$

(1)

(iv) $\tau_C = \frac{W_C}{2v_{sat}} = 3.0ps$

$W_C = 0.6$

$\tau_{EC} = 5.2 + 11.4 + 8 + 30 = 27.6ps$ (1)

$f_T = \frac{1}{2\pi\tau_{EC}} = 5.8GHz$

(1)

3 b) Capacitance must remain constant, since it effects I_D versus V_t characteristics

$$C \propto \frac{\varepsilon_r}{t_{ox}} \quad (1) \qquad \frac{\varepsilon_{r,SiO_2}}{\varepsilon_{r,HfO_2}} = \frac{3.9}{25} = 0.156 \quad (1)$$

$$t_{ox,HfO_2} = \frac{1}{0.156} \times 1.2\,nm = 7.7\,nm.$$

$$\frac{I_{tn,SiO_2}}{I_{tn,HfO_2}} = \frac{\sqrt{\frac{0.55}{0.11}}}{\frac{3.9}{25}\cdot\frac{3.15}{2.1}} \cdot \frac{e^{-K\frac{3.15^{1.5}}{2.5\times10^{8}}}}{e^{-K\frac{2.1^{1.5}}{3.9\times10^{7}}}} \quad (6)$$

ϕ_b Si-SiO_2 = 3.15 eV

ϕ_b Si-HfO_2 = 2.1 eV (1)

$$E \propto \frac{V_G}{t_{ox}} \quad SiO_2 \Rightarrow \frac{0.3}{1.2\times10^{-9}} \quad 2.5\times10^{8}\ V_m^{-1}$$

$HfO_2 \Rightarrow \frac{0.3}{7.7\times10^{-9}}$ $3.9\times10^{7}\ V_m^{-1}$. (6)

$$\frac{I_{tn,SiO_2}}{I_{tn,HfO_2}} = \frac{\sqrt{5}}{0.234} \cdot \frac{e^{-2.27}}{e^{-7.8}} = 2440 \quad (1)$$

$$\frac{}{} \quad 6.5 \qquad 252$$

I_{tn,HfO_2} = 50pA. (1)

Main reduction comes from lower E field due to larger thickness (1)

4 a) Transistor small signal equivalent circuit

$r_{bb'}$ – Base access resistance. (1)
– lateral current spreading resistance + base contact resistance

C_{BE} – Base-emitter capacitance – related to dopin (1)

r_π input dynamic resistance $\left(\frac{dI_E}{dV_{BE}}\right)^{-1}$ (1)

this is equal to $\left(\frac{q I_e}{kT}\right)^{-1}$ or $\frac{kT}{qI_e}$.

r_o output conductance $\left(\frac{dI_c}{dV_{CE}}\right)^{-1}$ due to Early effect. I_c not constant at saturation (1) collector-base depth width increases, shortening the base and increasing I_c.

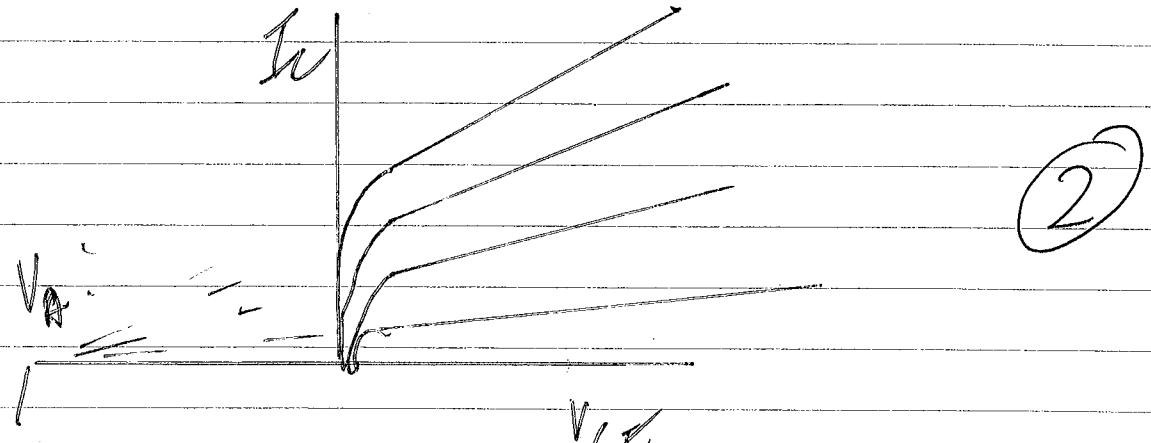
$r_{bb'}$ – increase doping or use higher mobility base material

r_π improves with I_e – higher bias, better dynamic resistance. (1)

r_o – reduce Early Effect – increase Early voltage (1)

increase device area – ~~be~~ increase doping

b) Early Effect associated with r_o.



(2)

All in cm

b) cont $|V_A| = \frac{q A_c N_B W_B}{C_{BC}}$ $\frac{1.6\times10^{-19}(10^{-4}\,10^{17}\,2\times10^{-5})}{1\times10^{-12}}$ (2)

$= 32\,V$

c) input $i_b = i_{bo} + j\omega C_{BE} V_{BE}$ (1)

output $i_c = g_m V_{BE}$

gain $\frac{\text{output}}{\text{input}} = \frac{g_m V_{BE}}{i_b^0 + j\omega C_{BE} V_{BE}}$ (1)

or just $\frac{i_c}{i_b^0 + j\omega C_{BE} V_{BE}} = \frac{1}{\frac{i_{bo}}{i_c} + j\omega C_{BE}\frac{V_{BE}}{i_c}}$

$\beta = i_c/i_b$ DC gain $i_c = g_m V_{BE}$

So $h_{FE} = \frac{1}{\frac{1}{\beta} + \frac{j\omega C_{BE}}{g_m}}$

low freq $\omega \to 0$ $\frac{1}{\beta} \gg \frac{j\omega C_{BE}}{g_m}$

$h_{FE} = \beta$ as expected (1)

high freq $\frac{1}{\beta} \ll \frac{j\omega C_{BE}}{g_m}$

$h_{FE} = \frac{g_m}{\omega C_{BE}} = 1$ when $f = f_T$ (1)

or when $\omega \to \omega_T = 2\pi f_T$

so $\frac{g_m}{2\pi f_T C_{BE}} = 1$.

a) cont.

$f_T = \frac{g_m}{2\pi C_{BE}}$

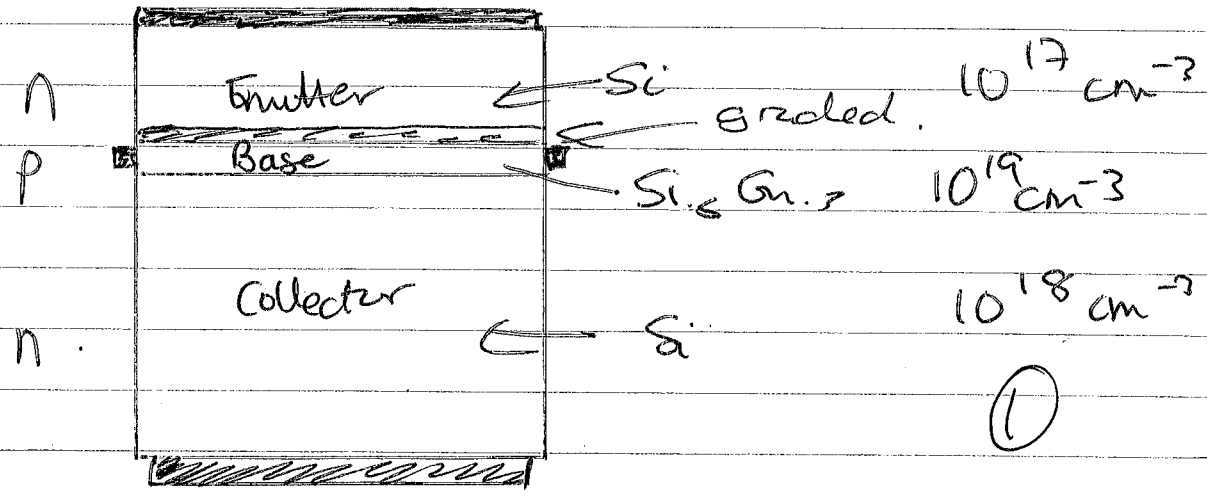
need high g_m value — high mobility

and/or

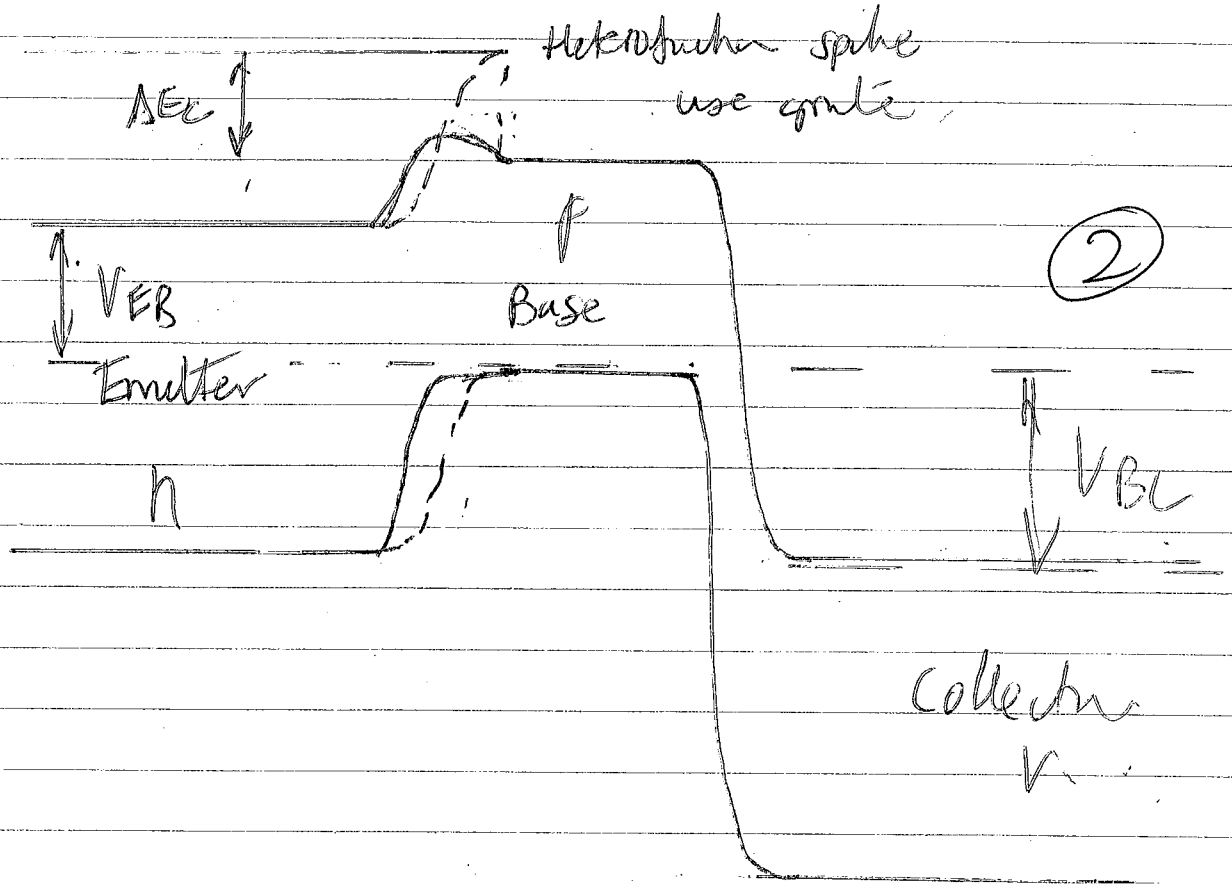
small C_{BE} — lower doping

(1)

a)



(1)



(2)

d) cont

Wide gap emitter – reduced barrier height for electrons as opposed to holes
- reduces hole current
- base doping can be increased
- r_{bb} reduced so increased – more current. (1)

Narrow gap base:
- Some improvement in mobility from lower SiGe effective mass. (1)

f_{max} increased due to reduction in r_{bb}
g_m improved by mobility improvement.

EEE 6040 FEB 2014

Q 1d $V_{threshold}$ labelled V_D should be V_T ✓

Q 2b Reword "Why is the enhancement mode device generally ....". ✓

Q 2b Exam script indicates 5 marks but answer sheet indicates 6 ?
Section deleted

IAN ROSS.

Date MH 15/2/2014