Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (2.0 hours)

EEE335 Integrated Electronics

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **Figure 1** shows the schematic for a digital circuit.

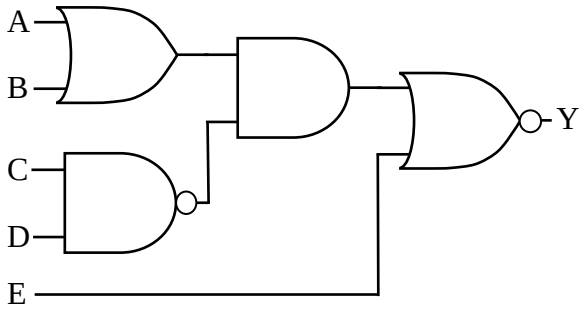

Figure 1: Digital Circuit

a. Derive the logic function of the circuit in **Figure 1**. **(2)**

b. Draw the *transistor-level* schematic diagram for a CMOS circuit that would implement the function in **Figure 1**. There may be more than one way to implement this function: justify the way in which you have implemented the circuit. **(6)**

c. Size the transistors in the circuit that you have drawn, assuming that the gate is *minimum-sized* (using the normal definition for this). **(4)**

d. Assuming that the gate capacitance associated with a minimum-sized *n*-type FET is 0.5fF, estimate the capacitance associated with each of the connections (wires connecting inputs and output, and any intermediate wires between separate sub-circuits) in your *transistor-level* circuit. **(2)**

e. Rather than implement the circuit in Figure 1 as a specific circuit, you decide to implement each of the individual logic gates separately as CMOS circuits. What would be the important differences between the implementation of the circuit as a whole and as separate, individual parts. **(6)**

2. a. A pass transistor is incorporated in a circuit as shown in **Figure 2**.

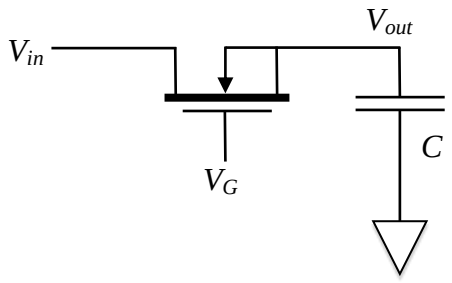

Figure 2: Pass Transistor Circuit

Initially (and for some time), V_{in}=0V, V_G=V_{DD} (a voltage which is above the threshold voltage, V_T, of the transistor). You may assume that the gain of the transistor is K_N.

i). At time, t=0, the input V_{in} is changed to V_{DD}. Verify that the response of V_{out} as a function of t in the period $t \geq 0$ is:

$$V_{out}(t) = (V_{DD} - V_T) - \frac{(V_{DD} - V_T)}{1 + \frac{K_N(V_{DD} - V_T)t}{2C}}$$

(4)

ii). Identify the value of voltage to which V_{out} becomes asymptotic. Explain why this is the case. **(2)**

b. With the capacitor, C, disconnected, what is the small signal impedance of the point labelled V_{out} to ground when:

i). V_{in}=0 **(3)**

ii). V_{in}=V_{DD} **(3)**

Comment on the use of the transistor as an electronic switch in this circuit. **(2)**

c. If you were to make a *good* electronic switch for use in a digital circuit, identify how this might be done. You do not need to do a detailed analysis of the switch's performance but you do need to relate the behaviour of the electronic switch to the behaviour of a perfect switch. **(6)**

3. a. i. An n-channel MOSFET has W/L = 2μm/0.4μm, V_{TO}=0.6V and a process transconductance parameter K_n=150μA/V^2. Ignoring channel modulation and assuming the transistor is operating in saturation, calculate the values of V_{OV} and V_{GS} required for this transistor to be biased at a drain current of 100μA. What is the minimum value of V_{DS} required to ensure the transistor is saturated? **(2)**

ii. For the transistor in part **i**, and assuming operation in the saturation region, what will happen to the drain current when the following device dimensions and voltages are changed:

- The channel length is doubled,
- V_{OV} is doubled.

Which of these changes could lead to the transistor falling into the triode region of operation and why? **(3)**

b. **Figure 3** shows a SPICE model of a source-follower, or common drain, amplifier. The transistor M1 operates at a drain current of 150μA, and you can assume that its parasitic capacitances can be neglected at the frequencies under consideration. The transistor has the following parameters:

$Kn = 200\mu A/V^2$, $W/L = 6\mu m/0.6\mu m$, $\lambda = 0.05V^{-1}$ and $V_{TO} = 0.5V$.

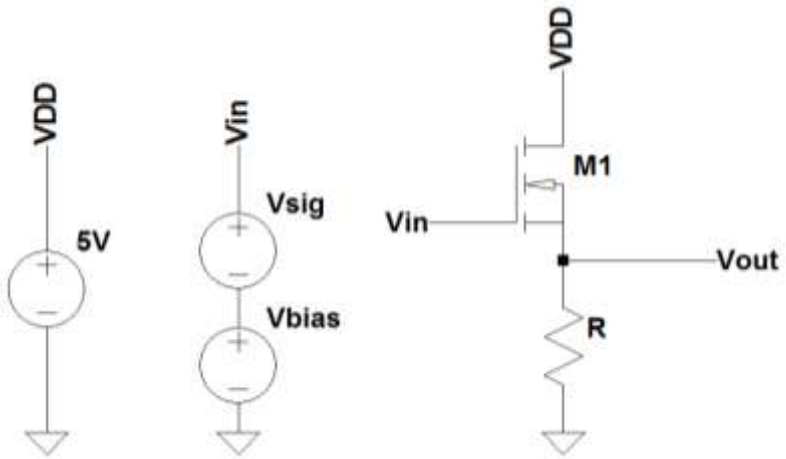

Figure 3: a SPICE model of a source follower

i. Draw the small signal model of the circuit in **Figure 3**, using the T-model for the transistor M1 and including the transistor output impedance r_o. Calculate the values of r_o, and g_m. **(5)**

ii. For R=10kΩ, calculate a suitable value for Vbias. **(3)**

iii. Use your small signal model to derive an expression for the gain of the source follower (show your working). Calculate the value of the gain for R=10kΩ. **(4)**

iv. Sketch a graph of the output voltage, Vout, of the circuit in **Figure 3** over time. Assume R=10kΩ and Vsig is a 0.2V pk-pk sine wave at 1kHz. Include numbered axes on your graph to show the maximum, minimum and average (DC) output voltages, as well as suitable values along the time axis respectively. **(3)**

4. a. Give a short description of the following terms:

i. Current steering,
ii. the transconductance parameter, g_m,
iii. channel length modulation. **(5)**

b. Consider an NMOS transistor having the following parameters:

V_{TO}=0.4V, K_n=175μA/V^2, λ=0.1V^{-1}, W=3μm, L=1μm, Cgs=Cgd=2fF.

i. Draw the small signal π model of the MOSFET described by the parameters above with the source terminal at ground. Include the dominant parasitic capacitances and the output resistance r_o. **(3)**

ii. Calculate the values of r_o and g_m, assuming V_{GS}=1V. **(2)**

iii. The FET is attached to a circuit such that the voltage at its drain is -25x that at its gate: compute the Miller equivalent capacitances and redraw your small signal model to show them. **(4)**

c. **Figure 4** shows a basic PMOS current mirror driven by a **5V** power supply and with the reference current set by a resistor **R**. M1 and M2 are matched transistors having V_{TO}=-0.5V, K_p=200μA/V^2, λ=0.04V^{-1}and W/L = 2μm/0.5μm.

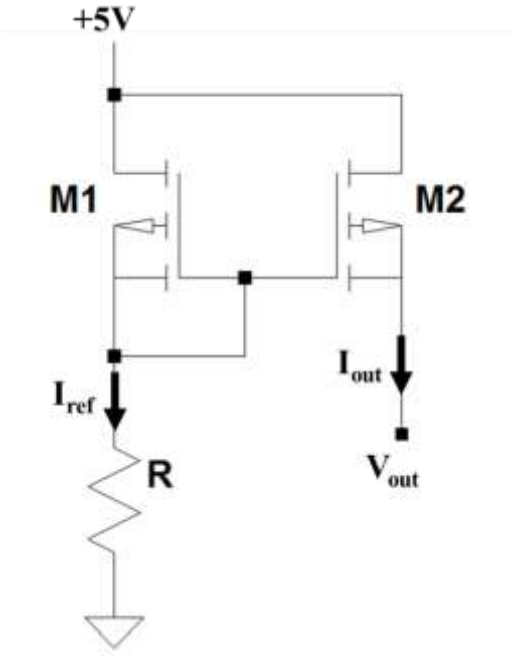

Figure 4: a PMOS current mirror

i. Determine an appropriate value for the resistor **R** in order to set $\mathbf{I_{ref}}$, the reference current through M1, at 150μA. **(3)**

ii. V_{DS} for M1 and M2 in **Figure 4** are initially identical. A change in the circuit to which the current mirror is attached causes $\mathbf{V_{out}}$ to increase by 0.5V. What will the resultant current error be (i.e. the difference between $\mathbf{I_{ref}}$ and $\mathbf{I_{out}}$)? What feature of more advanced current mirrors minimises the current error resulting from changes such as those described? **(3)**

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