The University Of Sheffield.

Data Provided:

Electronic charge (e or q) = -1.6×10^{-19} C
Permittivity of free space (ε_o) = 8.854×10^{-12} F.m^{-1}
Relative Permittivity (ε_r): Si=11.7, SiO_2=3.9, GaAs-12.9
Saturation velocity: Si=1.1×10^5m.s^{-1}, GaAs=2×10^5m.s^{-1}
Electron mobility (at 300K); Si=0.15m^2.V^{-1}s^{-1}, GaAs=0.80m^2.V^{-1}S^{-1}
Semiconductor band gaps: GaAs =1.43eV, AlAs=2.16eV
Electron diffusion coefficient in Si (D_e) =0.026 m^{2}sec^{-1}
Breakdown field (GaAs) = 3×10^7V.m^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2011-12 (2.0 hours)

EEE416 High Speed Electronic Devices

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Draw a schematic diagram of an n-channel MOSFET under conditions where the channel reaches the pinch-off condition. Carefully label the different elements of the device including the semiconductor, insulator and metal layers, the position of the channel and that of the depletion region.

(3)

b. Draw typical transfer (I_D versus V_{GS}) and drain (I_D versus V_{DS}) characteristics for this device. On the transfer characteristic indicate the threshold voltage (V_T). On the drain characteristics indicate the linear and saturation regions and the pinch-off point.

Explain how avalanche breakdown may introduce additional behaviour into the above characteristics. Add this region to the drain characteristics you have drawn above.

(5)

c. The expression for the threshold voltage of a Si n-channel MOSFET is given by:

$$V_T = -\left|V_{FB}\right| + 2\left|V_B\right| + \frac{\sqrt{2q\epsilon_r\epsilon_o N_A \left|2V_B\right|}}{C_{ox}}$$

where V_{FB} is the 'flat-band' voltage, V_B is the voltage separation of the between the midgap energy and the bulk Fermi level of the semiconductor, ε_s is the semiconductor dielectric constant, q is the electronic charge and C_{ox} is the gate oxide capacitance per unit area. The oxide in this case is SiO_2

(5)

Calculate the threshold voltage (V_T) for a device with an acceptor doping (N_A) =1 x $10^{22}m^{-3}$ and an oxide thickness of 20nm.. Assume V_{FB} = 0.32 and that V_B =0.35

d. A drain current of 130 µA and 210 µA flows in an n-channel MOSFET at gate-source voltages of 1.5 V and 2.5 V. The drain-source voltage is 0.1 V and this is well below pinch-off. Calculate the corresponding channel mobility for the MOSFET.

The calculated value is less than that of the electron bulk mobility. Suggest reasons for this discrepancy.

For the calculation you may assume the gate length is 0.1 µm, the gate width is 1mm and the gate oxide capacitance is 1 x 10^{-6} Fm^{-2}. You will require the expression for the drain current in the linear region of a MOSFET given by:

$$I_D = \frac{Z\mu C_{OX}}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where the symbols have their usual meaning.

(7)

2. a. Figure 1 shows a simplified small signal equivalent circuit for a Si bipolar transistor.

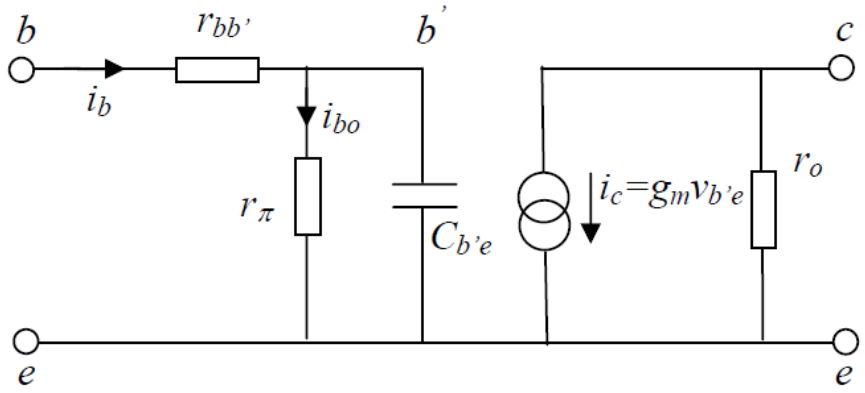

Figure 1: Small signal circuit diagram of a BJT

Draw a schematic diagram of the transistor and use it to explain the origin of the base access resistance $r_{bb'}$ in the small signal circuit.
What are the origins of the resistances r_π and r_o? Provide equations which relate these to the emitter and collector currents respectively.

(4)

b. Using figure 1, derive an expression for the small-signal circuit current gain, h_{fe}, as a function of the frequency. Simplify this to give expressions for the h_{fe} at (i) low frequency ($\omega \rightarrow 0$) and (ii) high frequency ($\omega \rightarrow \infty$).

At high frequency the gain reduces until it reaches a value of unity. Use this information to derive an expression for the cut-off frequency f_T. By consideration of this expression, state which parameters need to be improved to give high f_T values. How might we accomplish this?

(7)

c. The heterojunction bipolar transistor (HBT) represents an improvement on the basic bipolar junction transistor (BJT) design.

Explain the differences between the design of a HBT and that of a BJT.
How do these differences improve the device performance?
How will the resistances in figure 1 be affected by these improvements?
Finally, describe how these improvements will affect the f_{max} value, the transconductance and on the general form of the output characteristics?

(5)

d. The HBT uses a wide gap $Al_{.5}Ga_{.5}As$ emitter and a narrow gap GaAs base. When these two materials are combined, it is known that 30% of the band gap offset lies in the conduction band and 70% lies in the valence band.

What are the values of the conduction and valance band offsets, ΔE_c and ΔE_v?
(you may assume the band gap of AlGaAs varies linearly over the whole composition range). What effect would this have on the relative emitter-base and base-emitter currents for electrons and holes?

(4)

3. **a.** What is meant by 'Moore's law' of Integrated Circuits? What design philosophy has enabled Moore's law to be followed for almost 40 years?

Describe the trends which have taken place in the following CMOS technological parameters over the last 40 years. Describe the present day (2012) status of these parameters.

i). Switching Voltage
ii). Oxide thickness and material
iii). Gate length

For each of the parameters, describe the technological and fundamental device operation limits which may limit Moore's law in the future.

Briefly discuss one alternative technological approach which could in the future replace Si CMOS in switching circuits. What are the main advantages of this approach and what current issues need to be overcome for this to be applicable?

(10)

b. The power consumed by a single MOSFET during a switching cycle is given by:

$$P = \alpha \frac{1}{2} f C V_s^2$$

where α is the switching probability, C the gate capacitance, V_s is the supply voltage and *f* is the clock frequency. The gate of the MOSFET has dimensions of 45 x 100nm and a $Si0_2$ oxide layer of 2nm is present between the gate metal and the semiconductor. The IC has a clock frequency of 3 GHz, a supply voltage of 1.1 V. A switching probability of 0.5 can be assumed.

Calculate the power dissipated by a processor IC containing $1x10^9$ MOSFETS.

The IC also dissipates power even if all the MOSFETs are in their off-state. What is the main origin of this so-called 'static' power dissipation?

(5)

c. Estimate the cut-off frequency using the transit time method for two MOSFET devices, one with a gate length of 10μm and another with a gate length of 0.1μm. V_{GS} = 3.5V and V_T = 2V for both devices
You may assume that the velocity of an electron (v_e) in the channel is described by the following expression

$$v_e = 1x10^5 . \left(\frac{E}{7+E}\right) \text{ m.sec}^{-1}$$

where *E* is the electric field in $kV.cm^{-1}$. The device is biased at the minimum V_{DS} value to achieve output saturation.

(5)

4. **a.** The cut-off frequency, f_T, for an npn bipolar transistor can be expressed as a function of the total device delay time τ_{EC} as follows;

$$f_T = \frac{1}{2\pi\tau_{EC}}$$

List the individual components of τ_{EC} and identify which are capacitance related and which are resistance related. Discuss how we could reduce each of the individual components of τ_{EC} and thereby increase f_T.

(5)

b. In a particular type of silicon bipolar transistor it is found that the only significant delay components are the base transit time and the collector transit time.

The base transit time (τ_B) is related to carrier diffusion. It is given by the expression: $\tau_B = \frac{w_B^2}{2D_e}$ where w_B is the base width and D_e is the electron diffusion coefficient. For the collector transit time, assume the electrons travel at their saturation velocity across the collector.

Calculate f_T for a device of base width of 0.2μm and a collector width of 0.5μm

(5)

c. Describe the process of avalanche breakdown. How might an avalanche photodiode use this effect to detect low fluxes of photons?

A GaAs p+i-n^+ diode, designed as an avalanche photodetector, has a residual n-type doping of $1x10^{21}m^{-3}$ within the nominally intrinsic i-region. The thickness of that region is 1μm

Calculate the voltage required for the multiplication of incident photons.

You may assume that the ionisation coefficients $\alpha(E)=ß(E)= 1x10^{-24}E^4m^{-1}$ where E is the electric field.

(5)

d. Starting from the surface, a GaAs IMPATT diode consists of a 0.5μm layer doped with acceptors at $10^{22}m^{-3}$, a 1μm layer doped with donors at $10^{20}m^{-3}$ and a 0.5μm layer doped with donors at $10^{22}m^{-3}$.

Sketch (i) the doping profile and (ii) the electric field profile through the device.

What is the oscillation frequency of this device and what is the upper limit on the applied voltage?

(5)

MH / TWANG