**Data Provided: None**

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

**Spring Semester 2008-2009 (2 hours)**

**High Speed Electronic Devices 6**

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

**1. a.** For an n-channel MOS structure as used in a MOSFET, sketch the ***band structure*** (i.e. energy diagram) for each of the following bias conditions:

(i) no gate bias (equilibrium)

(ii) positive gate bias such that carrier depletion occurs in the semiconductor (but not inversion)

(iii) positive gate bias greater than the threshold for inversion to occur.

In your sketches carefully show, in each case, the relative positions of the Fermi levels and the conduction and valence bands, the bending of the bands, how the gate bias is represented and the formation of the inversion layer. **(9)**

**b.** The threshold voltage for a Si n-channel MOSFET is given by

$$V_T = -|V_{FB}| + 2|V_B| + \frac{\left(2q\varepsilon_s N_A |2V_B|\right)^{\frac{1}{2}}}{C_{OX}}$$

where $V_{FB}$ is the 'flat-band' voltage or built in potential of the gate MOS diode, q$V_B$ represents the separation of the mid-gap energy and the bulk Fermi level in the semiconductor, $\varepsilon_s$ is the semiconductor dielectric constant, $N_A$ is the p-doping concentration in the semiconductor, q is the electronic charge and $C_{ox}$ is the gate capacitance per unit area.

Describe how $V_T$ is altered by the change in the parameters in this equation as the process of miniaturisation of CMOS devices takes place. Why is it important to reduce $V_T$ when reducing device size? From this equation, explain why it has been difficult to continue to reduce $V_T$ during recent developments in CMOS technologies. **(8)**

**c.** Electrons with a charge equivalent to $5\text{x}10^{-6}$ C/cm$^2$ are trapped at the semiconductor/oxide interface of a Si n-channel MOSFET. What is the change in $V_T$ for an oxide thickness of 50 nm ($\varepsilon(Si0_2)$=3.45 x $10^{-13}$ Fcm$^{-1}$)? **(3)**

**2.** **a.** Briefly describe the process of avalanche multiplication and explain why it is particularly important for high-speed devices. **(4)**

**b.** A $p^+nin^+$ IMPATT diode oscillator has an 0.05 μm long avalanching *n*-region ($n = 3\times10^{21}$ m$^{-3}$) and a 1 μm long undoped (*i*) drift region ($n^+$, $p^+$ >> $n$ >> *i*-doping). Using the relative magnitudes of the doped regions given and Poisson's equation, $dE/dx=en/\varepsilon$ (usual meaning of symbols) , sketch the field profile under reverse bias and calculate the applied reverse bias between the device terminals required to initiate breakdown in the avalanching region.

For simplicity you may assume that no avalanching occurs in the *i*-region, there is a constant $\alpha$ in the *n*-region (corresponding to the average field there) and the electron and hole ionisation coefficients are equal. Under these assumptions, the electron initiated multiplication, $M_n$, over a distance $w$ is given by

$$1-\frac{1}{M_n}=\int_0^w \alpha dx,$$

where $\alpha$, the electron ionisation coefficient, is given by

$$\alpha(E)=3.8\times10^7 \exp\left(\frac{-3\times10^6}{E}\right) \text{ m}^{-1}$$

where $E$ is the magnitude of the electric field. You may need $\varepsilon = 1.17\text{x}10^{-10}$ Fm$^{-1}$ and the electronic charge, $-1.6\text{x}10^{-19}$ C. **(14)**

At what frequency would you expect the device to oscillate? **(2)**

**3.** **a.** Figure 3a shows a simplified small signal equivalent circuit for a Si bipolar transistor. Using a bipolar transistor sketch, explain the origin of the resistors in this circuit in terms of the physical device parameters.

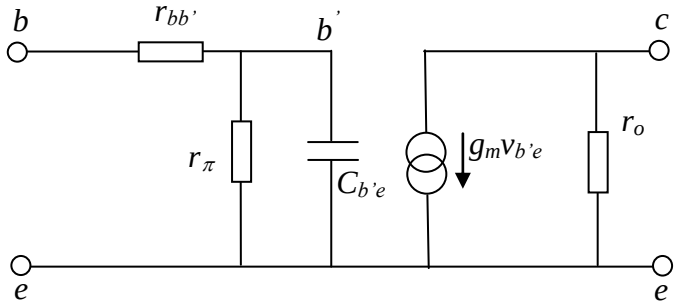


Figure 3a

Identify those resistors which are affected by the design changes possible with a heterojunction bipolar transistor. Explain the resulting benefit. **(10)**

**b.** $C_{b'e}$ in figure 3a is the only parameter in that circuit which can account for time delays that limit the high frequency performance. Explain the various components for the total time delay, how they are represented by a capacitance and how together they can be represented by $C_{b'e}$. **(10)**

**4.** **a.** The simplified expression for the saturated drain current of an n-channel MOSFET is

$$I_D = \frac{Z\mu C_{OX}}{2L}(V_{GS} - V_T)^2,$$

where Z and L are the gate width and length respectively, $C_{OX}$ is the gate oxide capacitance per unit area, $\mu$ is the electron mobility, and $V_{GS}$ and $V_T$ are the gate-source and threshold voltages respectively (drain-source voltage, $V_{DS} \geq V_{GS}-V_T$). From this equation, derive the expressions for the intrinsic transconductance, $g_m$, and the cut-off frequency, $f_T$, in terms of these parameters.

What limits $g_m$ and $f_T$ to values below that predicted by these equations as the devices get smaller?

Why is it desirable to increase the gate oxide capacitance per unit area, $C_{OX}$, as well as reduce the lateral dimensions during the scaling process? **(10)**

**b.** Use the 'transit-time' expression to calculate $f_T$ for one transistor with a gate length of 5 μm and another for a gate length 0.1 μm, assuming $V_T$ = 2 V and $V_{GS}$ = 5 V in each case. You may assume that the velocity of an electron in the channel is given by

$$v = 1\times10^5\left(\frac{E}{(7+E)}\right) ms^{-1},$$

where the electric field, $E$, is in units of $kVcm^{-1}$, and that the device is biased at the minimum $V_{DS}$ required to achieve device saturation.

Comment on the relative $f_T$ values obtained for the different gate lengths. **(6)**

**c.** From your knowledge of the ongoing miniaturisation process in CMOS to achieve increasing chip complexity (Moore's Law) and performance, briefly comment on *two* technological or physical aspects which could lead to the ultimate limit to this process. **(4)**

**PAH / RAH**