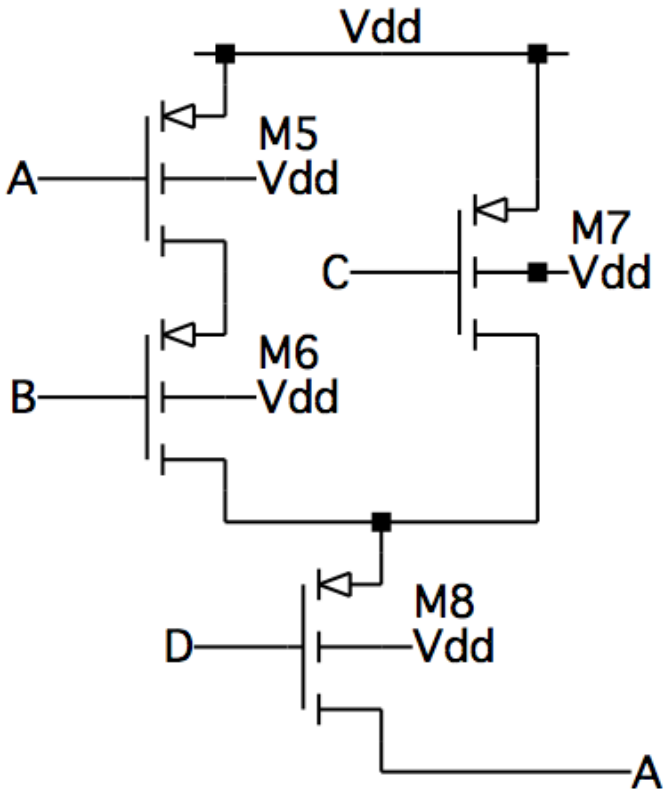
EEE335 exam solutions 2016: AM

(X) indicates allocation of marks.

1.

a.



(4)

b. To find Y, we can construct the expression from the arrangement of transistors (using the analogy with a set of switches controlled by the logical state of the input). That is when the logic input is TRUE, the switch is on and an electrical path is made through the switch. The state of the output is the converse of whether a path is made between Y and the negative supply. Parallel transistors/switches implies an OR operation and series implies AND. Normal precedence of operations applies. (1)

This gives rise to:

$\bar{Y}$ = ((A OR B) AND C) OR D = (A+B).C+D (1)

Therefore,

$Y = \overline{(A+B).C+D} = \overline{(A+B).C}.\bar{D} = \bar{A}.\bar{B}.\bar{D} + \bar{C}.\bar{D}$ (2)

c. The minimum –sized gate assumption is that the drive strength of the pull-down/up network is equivalent to a minimum- sized transistor. That is an n-type transistor of length L_{min} and width W_{min}. Consequently, the transistors M1 to M4 will all be minimum length and will of width, which will be a multiple of W_{min} as follows: for M1=2, M2=2, M3=2, and M4 = 1. (1 for each)

d. Dependent on the type of process, all of these transistors will be in a common area of p-type substrate or in a common p-well (this is the normal way in which the layout will be organised and ensures that the area of the design is minimised). (1)

Consequently, all the transistors in the common area must share the same substrate connection. The substrate connection must be connected to a point that is at least as negative as the minimum voltage at the inputs or outputs of the circuit and this, in turn, should be the negative supply rail. (1)

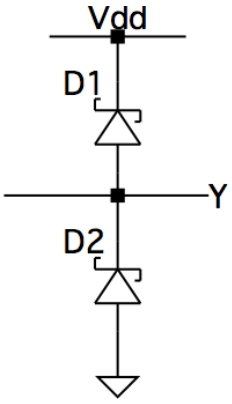
The problem that could arise is that for transistors further up a chain of n-type transistors, the voltage between the source and the substrate could be negative (increasing the threshold voltage for the transistor). This could cause the transistor to exhibit a lower drive and, potentially, disrupt the behaviour of the circuit (this is the body effect). (1)

For example, if the pull-up network is on and M1 is on but M3 is off then the source of M2 will be close to Vdd but the substrate will be at 0V. Consequently, the threshold voltage of M1 will be bigger than expected. If the pull-up network were to switch off and M3 were to switch on then, initially, the ability of the M1/M3 path to discharge the output would compromised until the intermediate node had discharged to a low enough voltage to allow a) M1 to switch on and b) for it to supply a significant amount of current. (1)

e. Over/undershoot is often experienced in real circuits because of issues like ground bounce, and transmission line effects. If, in this case, the output undershoots below 0V then there is the potential to switch on the pn junction formed by the drain n+ region and the p substrate. (1)

If this happens and a big enough current flows then this could damage this region of the transistor. Potentially, this could happen because the transistors are small and, therefore, not robust. (1)

The solution is to connect diodes on the output of the circuit (from the IC to the rest of the PCB – not at individual outputs within an IC) to limit the excursion of the output signal, e.g.



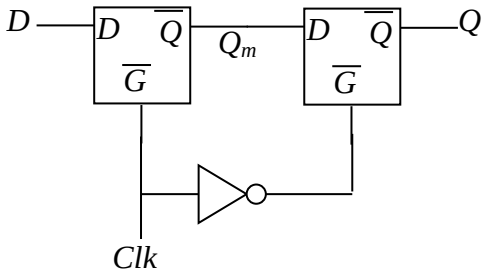
(1)

These diodes (which may be schottky devices so that V_f is lower than the V_f for silicon pn junctions) prevent the pn junctions from being forward biased and are normally large enough to absorb the energy involved (without compromising circuit performance too much). (1)

2.

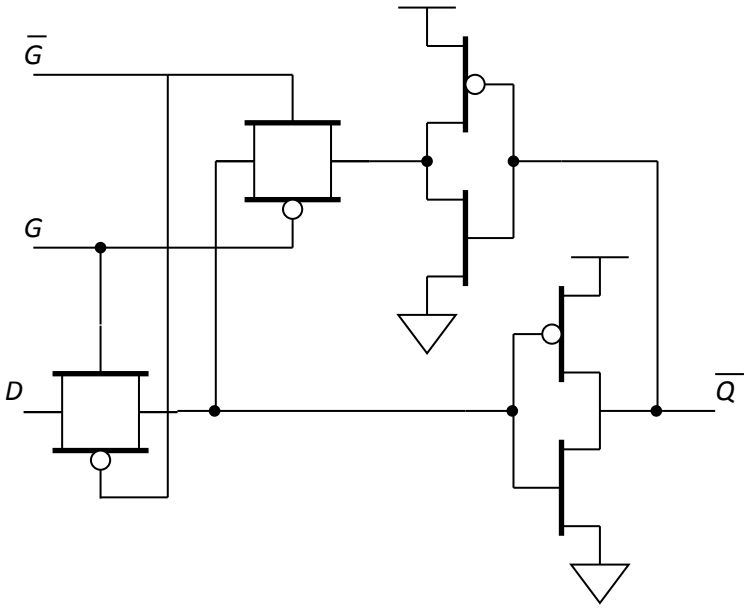
a.

The schematic for the D-type is:



(2)

And the schematic for each latch is:

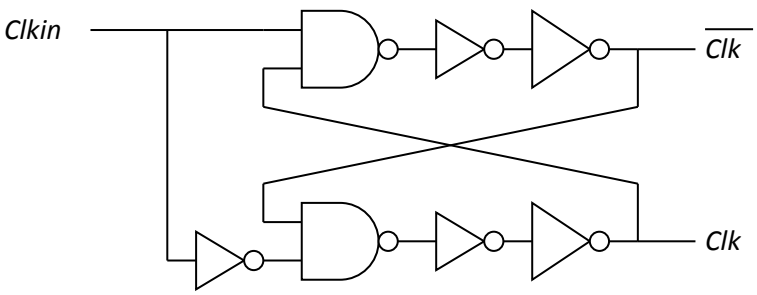


(2)

b.

The constraint is that the clock (G) input to the second (slave) latch must go high – trapping the input data in the slave latch before the master latch G input goes low, allowing the current D input to propagate through and, potentially be latched in the slave latch. Unfortunately, the inverter between the two latch enable signals may help to violate this constraint. (2)

The alternative is deriving clock and its inverse separately in such a way as to ensure that they two signals overlap only in the high state.



Essentially, this is an RS flip-flop with delays (and drivers on the outputs). A change in Clkin will force the low output high. It should also force the high output low but this cannot happen until after the low output has gone high and this effect is propagated through the chain of inverters driving the high output low. (2)

c.

Metastability is a condition that can occur if the D input to a flip-flop is changing whilst the clock is sampling the input value. During this time the bistable at the heart of the latch will be in an unstable or quasi-stable state where both the input and output of the latch are at voltage levels above $V_{I/oL|max}$ and below $V_{I/OH|min}$. After the bistable is connected, the output will be in an undefined state and will take time to relax to a defined state (indeed, if the bistable is exactly balanced it may not relax until perturbed by noise).(1)

The key to not observing a metastable state is to waiting longer before examining (or using) it. As the state will relax over time. This can be done by waiting or by transferring the metastable data into another flip-flop (or indeed chain of flip flops). The advantage of doing this (rather than merely waiting longer) is that it allows you to keep a high data throughput – but the data still suffers from latency.(1)

d.i)

upsets/second = $f_{data}*f_{clck}*T_o*\exp(-t_r/t_c)$ where T_0 and t_c are defined values, t_r is the observation time, f_{data} is the effective data frequency (half the clock frequency in the sending domain) and f_{clk} is the clock frequency in the receiving domain.(1)

The observation time is the time between the data being sampled on one clock edge (leading to the potentially metastable value arriving at X) and the next flip flop observing X by sampling its value at the next clock edge. That is $t_r=1/110x10^6$. (1)

So, upsets per second = $25x10^6x110x10^6x0.5x10^{-9}x\exp(-1/(110x10^6x0.5x10^{-9}) = 0.01746\approx 0.0175$ (2)

d.ii)

No. It is not reasonable. 0.0175 upsets/second means that the system could, potentially, fail every 57.2 seconds. Additionally, if a large number of systems are in the 'field' then the mean time to failure of any of the systems will be very small indeed – the figure needed depends on the reliability of the system of which this forms a part.(2)

The way to decrease the upsets/second is to put a series of flip-flops leading to X – each flip flop added will increase the observation time by $1/110x10^6$.(2)

d.iii)

So, with one flip flop, the upsets/second = 0.0175. With two flip flops $t_r = 2/110x10^6$ and so

upsets per second = $25x10^6x110x10^6x0.5x10^{-9}x\exp(-2/(110x10^6x0.5x10^{-9}) = 2.217x10^{-10}$

and this meets the requirement of there being fewer than $2.5x10^{-10}$ per second. That is, one upset every $4.5x10^9$ seconds. Clearly, with a large number of deployed systems, the MTTF will be a lot smaller than this.(2)

3.

i.

The overdrive voltage is the amount by which the gate-source voltage exceeds the turn-on or threshold voltage of an FET. **(1)**

ii.

The transconductance, gm, of a MOSFET is the slope of the transistor's vgs vs id curve at a given point. It is the amps per gate-source volt that a MOSFET sinks. **(1)**

iii.

The channel between the source and drain of a MOSFET has a shape that changes with the drain-source voltage. Above the MOSFET pinch-off point, where vds=vov, the channel begins to recede back towards the source: this effect is called channel length modulation and causes an increase in drain current with increasing vds. **(1)**

b.

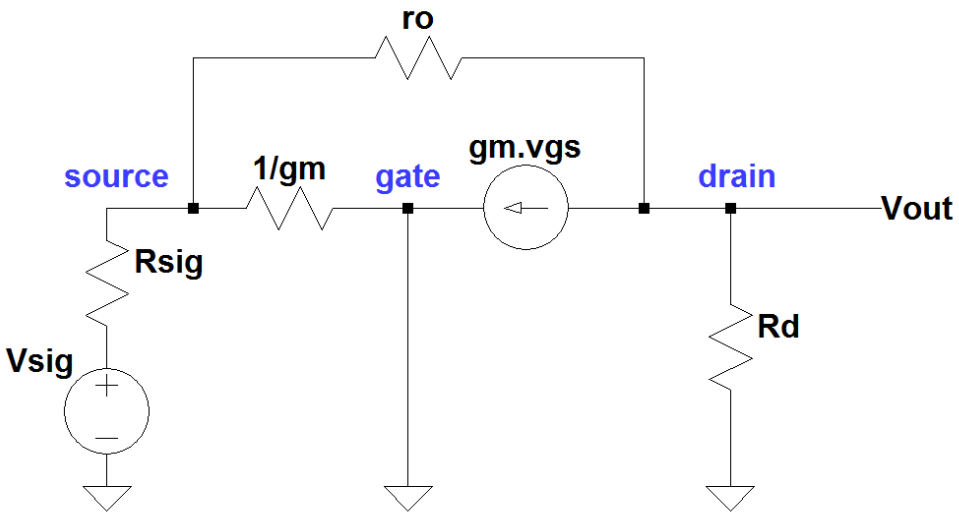
i.

$$V_{OV} = \sqrt{\frac{2LI_D}{K_n W}} = \sqrt{\frac{2\times1\times150\times10^{-6}}{100\times10^{-6}\times8}} = 0.61V \quad \textbf{(1)}$$

$$g_m = K_n \frac{W}{L} V_{OV} = 100 \times 10^{-6} \times \frac{8}{1} \times 0.61 = 0.49mS \quad \textbf{(1)}$$

$$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.05\times150\times10^{-6}} = 133\text{k}\Omega \quad \textbf{(1)}$$

ii.



(5) marks allocated for: signal ground of power supply and Vbias, correct 'T' model for MOSFET.

iii.

Ignoring channel length modulation equates to assuming that 1/gm<<ro. Under this condition, the voltage at the source of M1 can be approximated using a potential divider between Rsig and 1/gm, so that:

$$v_{out} = -R_d g_m v_{gs} \quad \textbf{(½)}$$

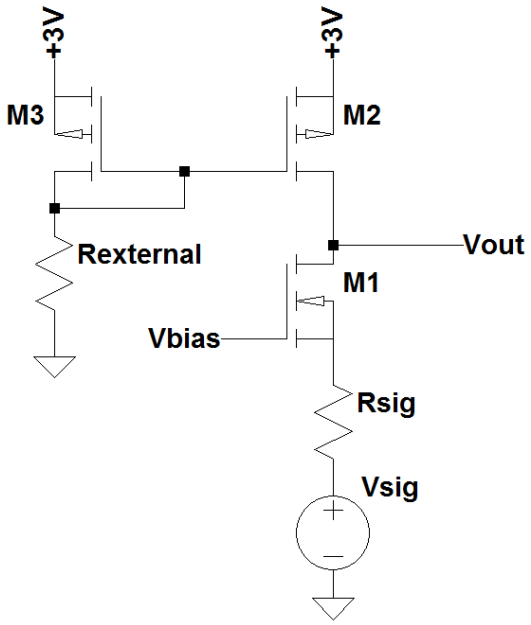
$$v_{gs} = 0 - v_{sig}\frac{1/g_m}{1/g_m + R_{sig}} = -v_{sig}\frac{1}{1+g_m R_{sig}} \quad \textbf{(1)}$$

$$\therefore A_v = \frac{v_{out}}{v_{sig}} \approx \frac{g_m R_d}{1+g_m R_{sig}} \quad \textbf{(½)}$$

For R_{sig}=5kΩ, R_d=50kΩ:

$$A_v \approx \frac{g_m R_d}{1+g_m R_{sig}} = \frac{0.49\times 50}{1+0.49\times 5} = 7.1\text{V/V} \quad \textbf{(1)}$$

c.



(4) marks for: back-to-back PMOS, correct position for external resistance, diode connected PMOS on reference arm.

ii.

The output resistance of transistor M2 in **part i** is calculated as:

$$r_{o(M2)} = \frac{1}{\lambda I_{D0}} = \frac{1}{0.025\times150\times10^{-6}} = 267\text{k}\Omega \qquad \textbf{(1)}$$

The revised gain can be calculated using exactly the same small signal gain equation from part i:

$$A_v \approx \frac{g_m r_{o(M2)}}{1+g_m R_{sig}} = \frac{0.49\times267}{1+0.49\times5} = 38\ \text{V/V} \qquad \textbf{(1)}$$

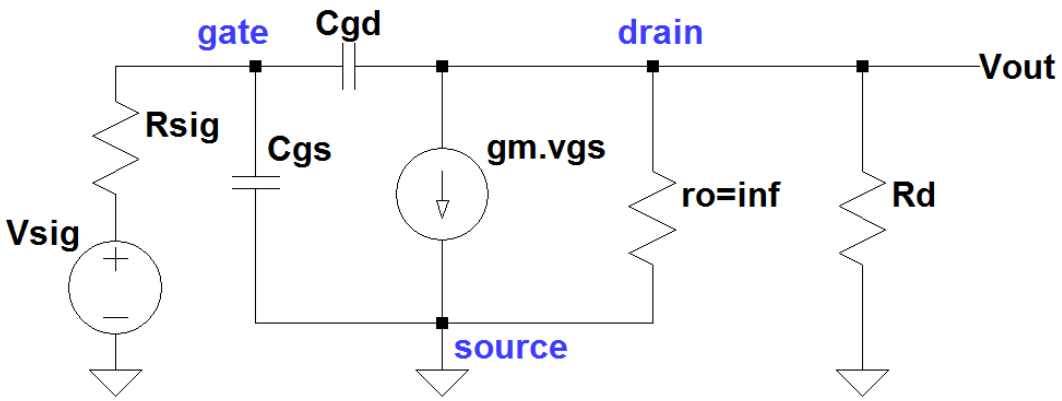
4.

a.

Biasing using a potential divider is not easy to implement on an IC: the large value resistors required would use up huge areas of silicon **(1)**. It is also undesirable because amplifier's using this bias do not incorporate any feedback mechanism to stabilise the operating point **(1)**: if, for example, the transistor in the amplifier heats up and its transconductance changes as a result, the gain of the circuit will alter in an uncontrolled manner. In contrast, bias that employs feedback is able to adjust vgs of the circuit to compensate for operating point changes due to e.g. temperature variations **(2)**. An example of this would be to add a current mirror bias at the source terminal of M1. **(1)**

b.

i



(5) marks for: correct signal grounding of power supply and Vbias; correct 'π' model of MOSFET; correctly setting r_o=infinity (or leaving it out).

ii.

At midband frequencies, we assume the two parasitic resistances are effectively open circuit **(1)**, so the resistance R_{sig} of the source has no effect on the gate-source voltage. The gain can therefore be calculated as follows:

$$v_{out} = 0 - R_d g_m v_{gs} = -R_d g_m v_{sig} \quad \textbf{(1)}$$

$$\therefore A_v = \frac{v_{out}}{v_{sig}} = -R_d g_m = -5 \times 1.5 = -7.5 \text{ V/V} \quad \textbf{(1)}$$

iii.

The capacitance C_{gd} can be split into a Miler capacitance C_{M1} between the gate and source **(½)** and a second Miller capacitance C_{M2} between the drain and source **(½)**.

$$C_{M1} = (1 - K)C_{gd} = 8.5 \times 10 \times 10^{-15} = 85\text{fF}$$ **(1)**

$$C_{M2} = (1 - 1/K)C_{gd} = 1.13 \times 10 \times 10^{-15} = 11.3\text{fF}$$ **(1)**

iv.

Assuming we can use the midband gain of the amplifier to approximate its gain at the cutoff frequency **(½)**, the Miller capacitances from **part iii** can be used in the calculation. We need to calculate the two time constants associated with the input and output sides of the amplifier:

$$\tau_1 = R_{sig}(C_{M1} + C_{gs}) = 100000 \times (85 \times 10^{-15} + 10 \times 10^{-15}) = 9.5\text{ns}$$ **(1)**

$$\tau_2 = R_d C_{M2} = 5000 \times 11.3 \times 10^{-15} = 56.5\text{ps}$$ **(1)**

Since $\tau_1 \gg \tau_2$ we can apply a dominant pole assumption **(½)** and calculate an approximate upper cutoff frequency as:

$$f_{\text{cutoff}} = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi \times 9.5 \times 10^{-9}} = 17\text{MHz}$$ **(1)**