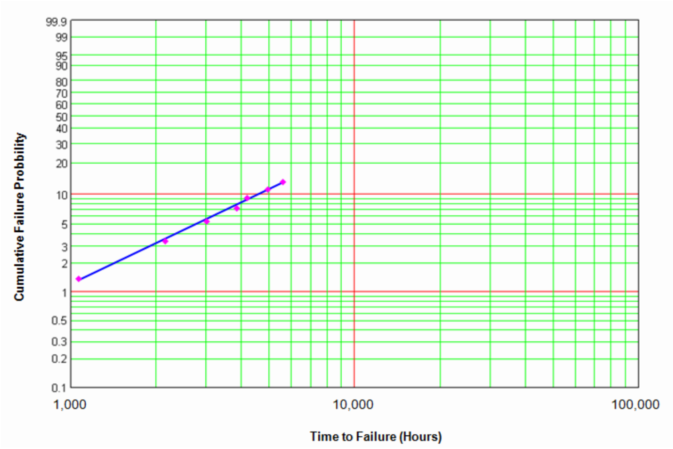
Solutions – EEE6008 2011-12

Q1.



EEE6008 Reliability + Failure 2011–12 Solutions

Q1.

a) i)

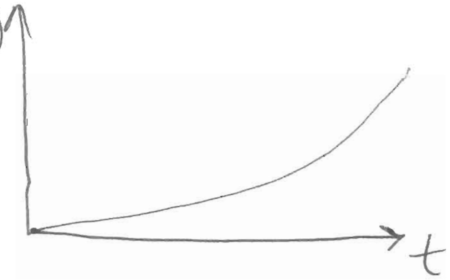
Rank	t_f	$F_i(t)$
1	1050	1·39
2	2120	3·37
3	2970	5·54
4	3820	7·34
5	4150	9·36
6	4885	11·31
7	5550	13·3

→ plot $F_i(t)$ vs t_f on the Weibull paper.

iii) $\eta = 22500$

$\beta = 1{\cdot}4$

iv) $\lambda(t)$



Wearout region, eg. electromigration, junction spiking, dielectric breakdown.

v) MTTF = 17400 hours.

After 20,000 hours, 60% will have failed.

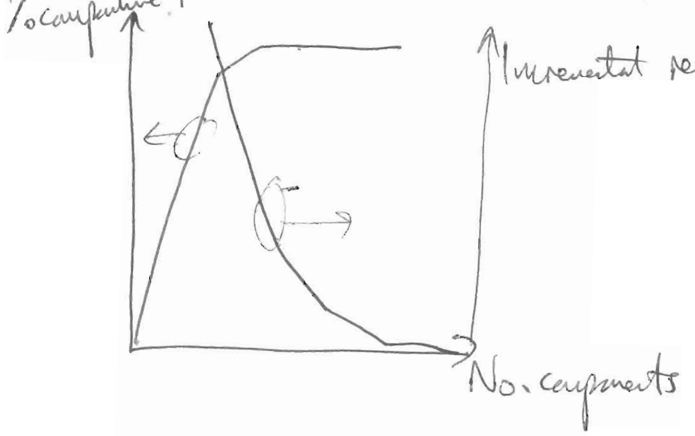
b) i) $0{\cdot}97 = R^{10} \Rightarrow R = 0{\cdot}97^{1/10} = 0{\cdot}997 = 99{\cdot}7\%$

ii) $R_s = 0{\cdot}85^{10} = 0{\cdot}197 \sim 20\%$

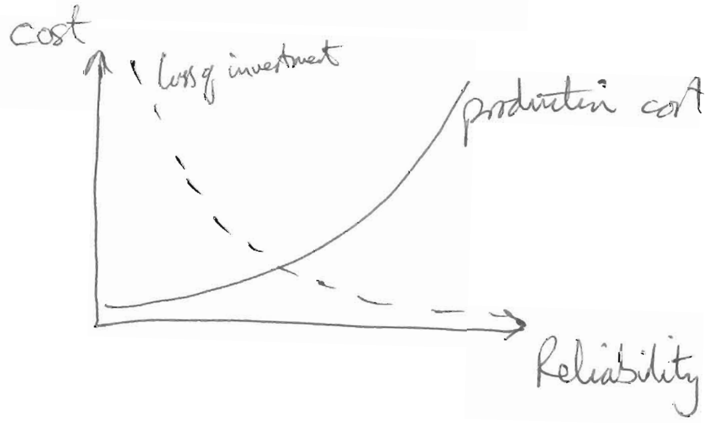
iii)

No. components	R_P	Incremental Rel	%age change
1	0·85		
2	0·9775	0·1275	15%
3	0·996625	0·019125	17·25%
4	0·9995	0·002875	17·56%

↑ uses $R_P = (1 - F_P)$, $F_P = (1-R_1)(1-R_2)(1-R_n)$



iv)



Expensive to manufacture highly reliable chips (comp. process development)

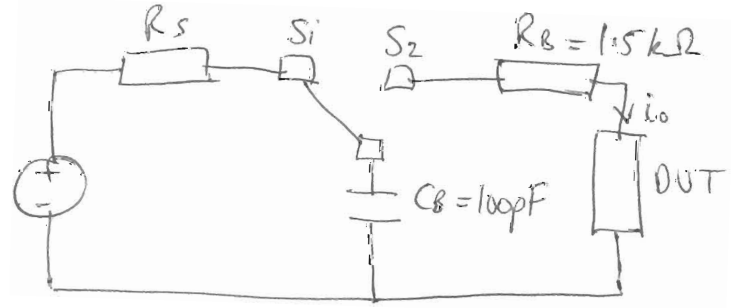
Expensive to manufacture low rel. components (lost mkt share, low yield)

Parallel systems increase reliability but increase cost.

Q2. a) i) High voltage pulses produced by ESD can produce large current of short duration. This current leads to electromigration causing spiking or shorting.

ii) Wrist straps, antistatic gloves/smocks, grounded tools, chairs, antistatic bags, control humidity, damping/protection circuits, shunt capacitors, pack chips tightly, don't touch leads, store in conductive containers, inject conductive ions, conductive flooring.

b) i)



ii) $V_{HBM} = 3000V \quad R_d = 20\Omega$

$\tau = (R_B + R_d)C_B = (1500 + 20)100 \times 10^{-12} = 0.152\,\mu s$

Discharge occurs over $\sim 5\tau = 0.76\,\mu s$.

iii) Max. current, $i_o = \frac{V_{HBM}}{R_B + R_d} = \frac{3000}{1500+20} = 1{\cdot}97\,A$

$$\therefore \text{Max } J = \frac{1{\cdot}97}{4\times10^{-8}} = 49{\cdot}3\times10^{6}\ Am^{-2}$$

c) EBIC can be used to localise diffusions and defects. Defects produce local variations in junction that vary recombination current, hence the EBIC signal.
EBIC signal superimposed with secondary electron image → correlation of recombination centre with defects.
Induced EBIC current provide e^-h^+ pairs, which recombine if cannot be swept away or if high defect density. As e-beam scanned across, areas appear white if low defect density or black if high.
EBIC shows position of junction. Any change to this, due to the ESD incident, will also show up in the EBIC analysis.

d) Photodiode: Charge buildup in surface passivation layers, enhanced surface leakage, recombination of photogenerated carriers reduces signal, increased number of generation centres → ↑ leakage current.

Laser diode: Permanent increase in J_{th} due to displacement damage, generates e^-h^+ pairs and dislocations (non-radiative recombination centres).
Degradation of monitor PD also (degradation of PDs > lasers).

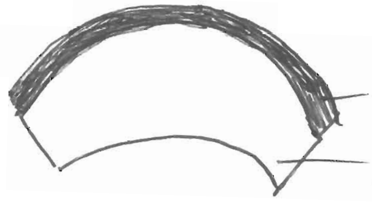
Optical fibres: Creates e^-h^+ pairs which are trapped in defect sites → new energy levels to absorb light → increases loss (darkening of fibre), Luminescence.

Q3. a) i)

$$\text{Stress} = \frac{E}{1-\nu_f}(\alpha_f - \alpha_s)(T - T_0) = \frac{158\text{ GPa}}{1-0.25}$$

$$= \frac{158\text{ GPa}}{1-0.25}\left[(2-4)\times10^{-6}\right]\left[300-27\right] = -0.115\text{ GPa}$$

ii)



b) Impurities from precursor gases, thin films build-up on chamber walls, particulates from gas-phase environment ("snow"), poor adhesion, non-uniform film growth due to local gas flow rate. (3 from these)

c) Weak spots from radiation damage, presence of mobile ions (Na^+), contamination, impurities, material defects, pin holes, interface charges (structural defects → dangling bonds), dangling bonds in oxide.

If pin holes, current flows through these → heat → more current flow → thermal runaway → oxide failure / rupture at these spots → short circuit.

Excessive electric fields (EOS / ESD, too thin an oxide layer etc)

→ weaker spots allow thermal runaway, generation of e^- h^+ pairs in oxide → avalanche breakdown → high currents flow → heat damage.

Trapped charges in oxide increase with time → effective oxide layer thickness reduces → electric field increases → high current through weak spots → thermal runaway.

c) Describe are form
1) Drain avalanche hot carriers
2) Channel hot electrons
3) Substrate hot carriers
4) Secondary generated hot carriers

... using descriptions in the notes (under section "Dielectric breakdown + hot carrier effects")

Reduce influence by:

i) Reduce electric field – reduce operating voltage or modify doping profiles to reduce peak field.

ii) Reduce carrier trapping in gate oxide and at $Si-SiO_2$ interface (through process control, material purity, annealing)

iii) Reduce time that device undergoes high field – apply safe operating procedures and conditions to ensure device spends minimum time at high fields.

d)

2 distributions. Main population centred on high fields, other over broad range of low fields. Weibull best describes impact failures. Metal contaminants during processing causes breakdown at lower fields than would occur of intrinsic breakdown.

1) a) i) Thinning : mechanical damage, excessive stress, broken edges/gouges, deformation, corrosion.

ii) Die attach : die cracking, void formation in adhesive due to oxide + contaminants → delamination, gas or moisture absorption → voids.

iii) Wire bond : Wire fracture, ball lifting, Kirkendall voids,

iv) Moulding : Stress induced cracks (thermal mismatch), incomplete filling / voids, fluid flow → bond ~~wire~~ removal, lead frame deflection.

b) Popcorn cracking : During solder reflow, moisture penetrates into package via metal-plastic interfaces and is absorbed by moulding compound. During reflow soldering this condensed moisture expands to form a pressurised dome of steam which can form cracks and delaminate. Such cracks/delamination form conditions for accelerated corrosion.

Can be detected using X-ray radiography + SAM (describe one using notes).

c) Stress gradient in thin metal generates force to counter the atom movement due to electromigration.

Under high current densities, electromigration causes migration of conductor atoms from cathode to anode. If conductor is shorter than a critical length, a stress gradient can develop → flow of atoms from anode to cathode. This flow counters the movement due to electromigration

Electron wind induced force, $Z^* q \rho j_e$ = stress-induced force, $-\Omega \frac{d\sigma}{dx}$

at a critical length, $L_c = \dfrac{\Omega \sigma_c}{Z^* q \rho j_{e(c)}}$

d) 1) Single crystal (no grain boundary) → thickness ÷ width ~1 gives single grained crystal.

2) Bamboo structures 

3) Multilayers with refractory metals such as Ti, W, TiN.

4) Use stiff dielectric layers to prevent deformation of metal, increases resistance to electromigration.

5) Incorporate metals to reduce grain boundary diffusion coefficient (eg: Cu in Al to form Al-Cu alloy (Cu raises E_a for Al migration).