The University Of Sheffield.

Data Provided:

Boltzmann constant $k_B = 8.6 \times 10^{-5}$ eV K^{-1}

Thermal conductivity data: $k_{glass} = 1.2$ W m^{-1} K^{-1} $k_{copper} = 390$ W m^{-1} K^{-1}

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (2.0 hours)

EEE6393 Microsystems Packaging

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1.

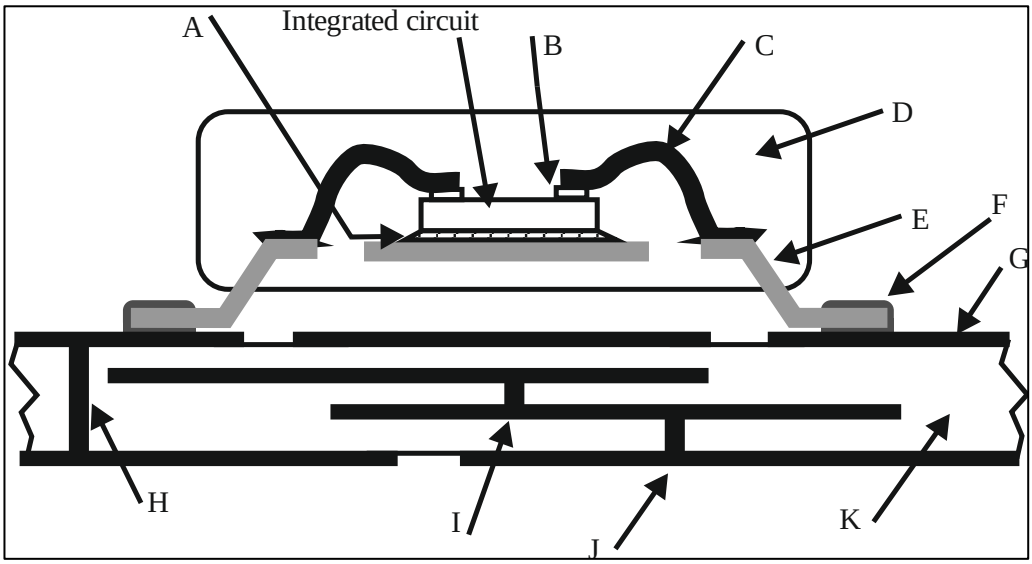

Figure 1 Cross-section of a packaged silicon chip and substrate (not to scale)

With reference to Figure 1, answer the following questions:

a. What are typical dimensions and compositions of A, B and C? **(3)**

b. What is the typical composition of D? **(1)**

c. What is E and how is it made? **(2)**

d. What is the typical composition and purpose of F? **(2)**

e. What material/materials are typically used for G and K? **(2)**

f. Identify the features H, I and J. **(2)**

g. During testing it is found that the signals between the integrated circuit (IC) and a simliarly-packaged ajacent IC are too slow and are distorted. Describe how the IC packaging and substrate could be changed to solve these problems. **(4)**

h. Packaged silicon chips are subject to the highly accelerated steam and temperature test (HAST) and are found to have a failure rate of 0.087. Inspection of the failed devices shows electrochemical corrosion, which is known to have an activation energy E_a of 0.6 eV. What is the estimated failure rate at 20 °C, 50 % relative humidity? You may assume that the failure rate (F) is proportional to the reciprocal of the cube of the relative humidity (H), i.e. $F \propto 1/H^3$. **(4)**

2. a.

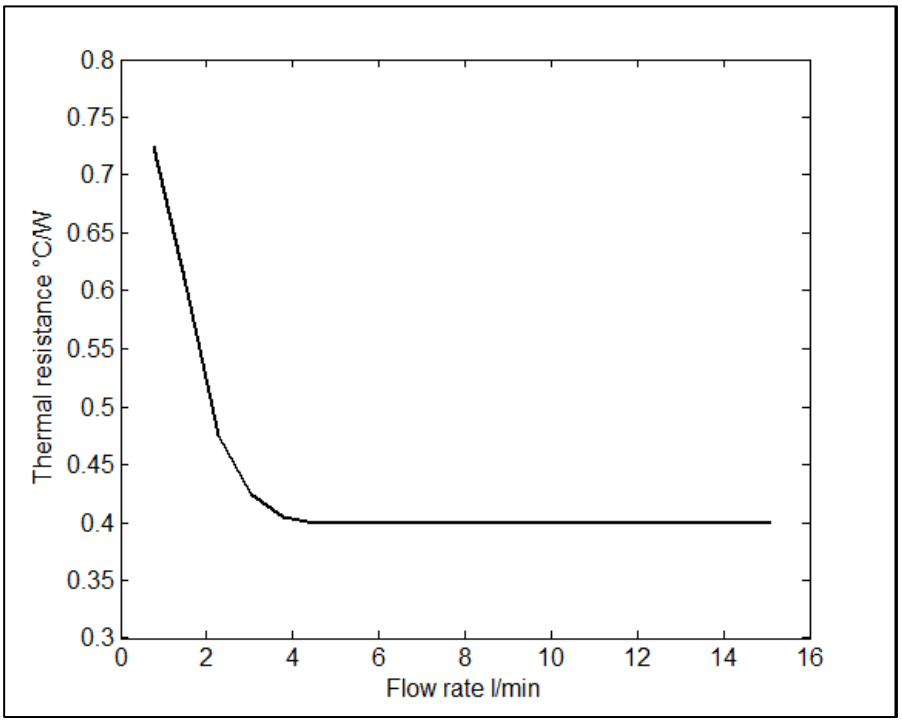

Figure 2 Thermal resistance of heat exchanger as function of fluid flow rate

Ten printed circuit boards (PCBs) are stacked in a rack that forms part of an avionics system that must operate at a high altitude. Each PCB dissipates 10 W and is cooled via a heat exchanger clamped along one edge of the PCBs. A fluid at 15 °C flows through the heat exchanger. The thermal resistance of the heat exchanger as a function of fluid flow rate is shown in Figure 2. What is the minimum thermal resistance of the PCBs that will keep their average temperature below 40°C? State all the assumptions and approximations that you make. **(6)**

b. For the scenario described in **2.a.**, suggest what factors in the PCB construction would help achieve a low thermal resistance between the components attached to the PCB and the heat exchanger. **(2)**

c. Some temperature sensitive bio-sensor chips need to be attached to a substrate. The maximum temperature which the chips can withstand is 100°C. Describe two ways in which the attachment can be made, with reference to the electrical, mechanical and thermal performance. **(4)**

d. Explain the differences between performing surface mount assembly with a eutectic and non-eutectic solder alloy. **(4)**

e. Describe how through-glass and through-silicon vias are made. **(4)**

3. a. Explain the advantages of a system in package (SIP) over discretely packaged devices. **(4)**

b. i) Calculate the thermal resistance between the top and bottom surfaces of a 200 µm thick glass interposer with a surface area of 5×10 mm. **(2)**

ii) A 100×200 array of 40 µm diameter copper through glass vias (TGVs) are added to the interposer. Calculate the revised thermal resistance. **(3)**

iii) Comment on your results. **(1)**

c. There is considerable heat generation on a power semiconductor. What are the sources of this heat and what measures can be taken to reduce it and accommodate it? **(4)**

d. A wafer-level packaging scheme first involves spin coating a layer of photo-imageable polymer (BCB) on top of the fully-processed CMOS devices.

i) Describe the remaining steps necessary to form a chip scale packages with a ball grid array (BGA) interconnections. Include an annotated diagram of the package in your answer. **(4)**

ii) What are the benefits of this wafer-level packaging approach in comparison to a standard BGA package? **(2)**

4. **a.** Draw a single sketch to show the failure rate as a function of time for these two electronic microsystems: i) an integrated circuit inside an electric toothbrush, ii) an integrated circuit inside the control system for an aircraft. Identify the various parts of the curves. **(4)**

b.

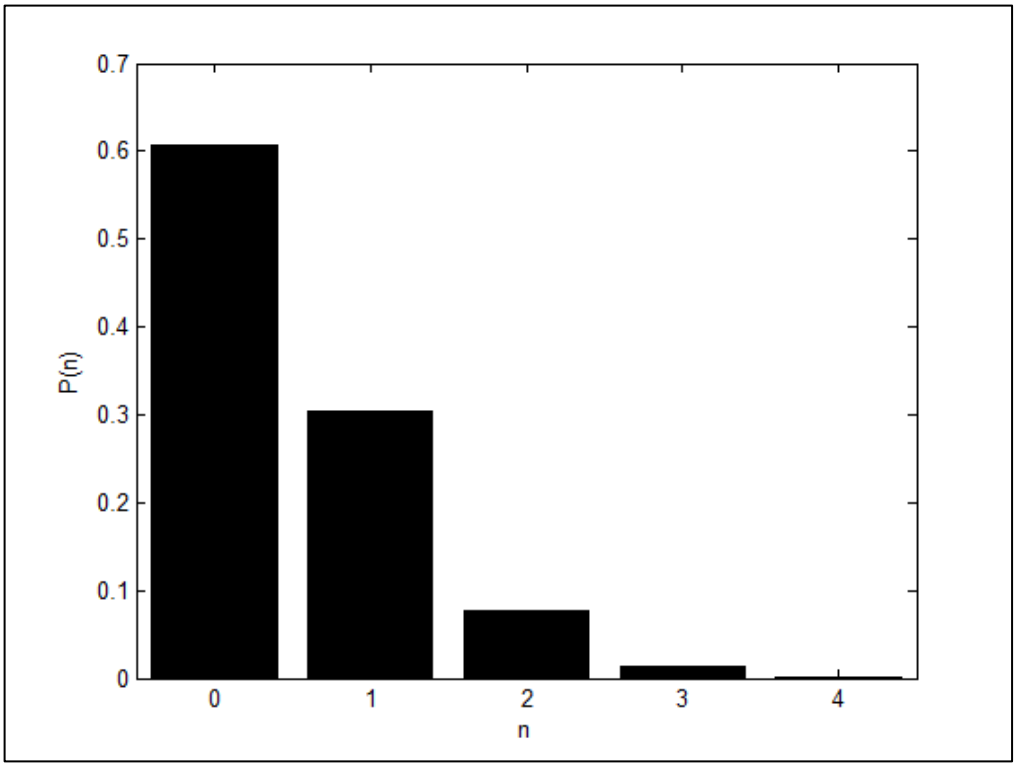

Figure 3 Defect data for lithographic process

A lithography system is used to pattern wafers containing 200 individual devices. The probability, *P*, of there being *n* defects on an individual device is given by the data in Figure 3. A laser system can be used to repair some of the defects. The probability that an individual defect can be repaired is $\eta = 0.5$.

On a single wafer, how many devices remain faulty after the repair process? **(3)**

c. An edge-emitting laser diode is flip-chip bonded onto a silicon substrate. Describe how the anisotropic etching of silicon can be used to accomplish the coupling of an optical fibre to the diode. **(4)**

d. Explain the fabrication process for a 'thick film' hybrid substrate containing copper conductors and integrated resistors. The substrate is to be used to house a high-performance silicon IC. Explain how a hermetic lid is attached to the substrate. **(5)**

e. How does the cross-sectional shape and surface finish of the electrical conductors on a printed circuit board (PCB) effect the propagation of high speed signals (frequency > 1 GHz)? **(4)**

GLW