The University Of Sheffield.

Data Provided:
Electronic charge q = 1.6×10^{-19} C
Dielectric constant of free space $\varepsilon_o = 8.85\times10^{-12}$ Fm^{-1}
Relative dielectric constant ε_r (Si) = 12
Electron saturation velocity (Si, GaAs)
v_{sat} = 1 x 10^5 ms^{-1}
Breakdown field (GaAs) = $3x10^7$ $V.m^{-1}$

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2009-2010 (2 hours)

High Speed Electronic Devices 4

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Draw energy band diagrams for the n-channel MOSFET under the following conditions

i) In equilibrium, with the gate voltage= 0

ii) the gate voltage just exceeds the threshold voltage and V_{DS} is low ($V_{DS} << V_{GS} > V_T$)

Show the position of the conduction and valence bands, the Fermi level and all other relevant features in each case **(4)**

b. Sketch a cross section of a typical n-channel MOSFET under conditions where the drain-source voltage reaches the pinch-off condition ($V_{DS} \approx V_{GS} - V_T$). Show the elements of the device, position of the channel and the bias arrangement.

At the pinch off condition the drain current saturates and becomes solely controlled by the gate voltage. Discuss the reasons for this behaviour in terms of the behaviour of the channel. **(5)**

c. The transconductance of the MOSFET is given by $g_m = \frac{Z\mu C_{ox}}{L}[V_{GS} - V_T]$

Use the above to derive an expression for the cut off frequency (f_T) of the MOSFET. From your result, state which device parameters are important for high speed operation. In state-of-the-art CMOS devices how is this achieved? **(6)**

d. The drain current of a MOSFET operating in the linear region is given by $I_D = \frac{Z\mu C_{Ox}}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$. The MOSFET has a drain current of 40μA at V_{GS} = 1.0 V and of and 90 μA at V_{GS} = 2.0 V respectively at V_{DS} = 0.1 V (i.e. in the linear region). Calculate the electron channel mobility for this device which has a gate length (L) of 50nm and width (Z) of 200μm. Assume C_{OX} = 1 x 10^{-6} Fm^{-2}. **(5)**

2. **a.** Explain, using a band diagram, how an n-p-n heterojunction bipolar transistor (HBT) gives improved performance over a conventional bipolar transistor. What steps are needed at the emitter-base interface to achieve this improvement? **(4)**

b. The current gain (ß) of an AlGaAs/GaAs HBT is reported to be 600. Assuming the base is ultrathin and highly doped; such that the base transport factor can be assumed to be ~1, calculate the base and collector currents for an emitter current of 5µA.

Sketch a graph of the typical small signal current gain, h_{FE} versus frequency (f) response for the above device. Show clearly the expected value of h_{FE} when f =0 and when f=f_T **(4)**

c. Bipolar transistors are generally preferred to FETs for high power analogue circuitry. Describe the differences in the device geometry between these two devices that give rise to this preference. Describe how the BiCMOS process combines both FET and Bipolar approaches to achieve a good compromise between power handling and consumption. **(5)**

d. The equivalent circuit for a SiGe HBT is shown in figure 1.

Three separate fabrication runs of SiGe HBTs produce the parameters listed in table 1. The HBT has a base width of 75 nm and a collector thickness of 200nm. Assume an electron mobility is 0.05 $m^2 V^{-1} s^{-1}$, with other values as listed in the date provided section on page 1.

Using the information supplied estimate the cut-off frequency, f_T, and the maximum oscillation frequency, f_{max}, in each case

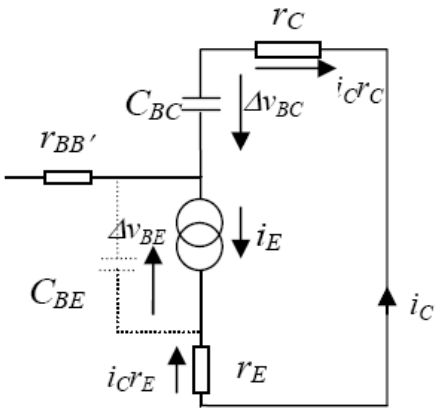

Figure 1

HBT equivalent circuit

Table 1

Parameter	**Run1**	**Run2**	**Run3**
R_C (Ω)	45	22	25
R_E (Ω)	26	26	30
$R_{BB'}$ (Ω)	300	380	170
C_{BC} (fF)	4.0	4.0	5.0
C_{BE} (fF)	14.0	10.5	9.6

(7)

3. a. Describe what is meant by 'Moore's law' of scaling in integrated circuits. What factors could limit further downscaling of planar Si CMOS dimensions?

(4)

b. For each of the following CMOS device parameters describe how technological advancement has led to continual improvements in progress in line with Moore's law. Describe both the current technological approach and comment whether the approach is close to the ultimate limits of the technology. State how any limits could possibly be overcome in the future by using alternative approaches.

i). Switching Voltage

ii). Oxide thickness and material

iii). Gate length

iv). Interconnects

(8)

c. The threshold voltage of a Si n-channel MOSFET is given by:

$$V_T = -|V_{FB}| + 2|V_B| + \frac{\left(2q\varepsilon_r\varepsilon_o N_A |2V_B|\right)^{0.5}}{C_{OX}}$$

where V_{FB} is the flat band voltage, qV_B is the energy separation between the bulk Fermi level and the mid gap energy of the semiconductor, ε_r is the relative dielectric constant of Silicon, q is the electronic charge and C_{OX} is the gate capacitance per unit area.

Table 2 shows measured parameters for a low voltage (LVP) and ultra low voltage CMOS (ULVP) processes. Calculate the threshold voltage V_T in both cases.

Table 2

	Oxide thickness (nm)	**Oxide relative dielectric constant**	**Doping (m^{-3})**	**V_{FB} (V)**	**V_B (V)**
LVP-CMOS	**10**	**3.9**	**$1x10^{22}$**	**.35**	**.38**
ULVP-CMOS	**5**	**7.5**	**$5x10^{22}$**	**.48**	**.40**

In both processes a fixed interfacial charge of 10^{-3} $C.m^{-2}$ was observed to form at the oxide/semiconductor interface. Calculate the revised values of V_T for both processes.

Practically how might one correct for this fixed charge by means of a suitable bias arrangement?

(8)

4. **a.** Sketch the cross section of a typical GaAs IMPATT diode. One such diode is used as an oscillator for the generation of 85GHz RADAR emission. Determine (i) the length if the device and (ii) the upper limit on the applied voltage. You may make use of the 'data provided' on page 1 for your calculation **(5)**

b. A GaAs p^+n diode, designed as a avalanche photodetector, has an n-type doping of $2x10^{21}m^{-3}$. Calculate the voltage required for avalanche multiplication of incident photons to occur given that $\alpha(E)=ß(E)= 1x10^{24}E^4 . m^{-1}$ **(5)**

c. Sketch the band structure of a GaAs/AlGaAs high electron mobility transistor (HEMT), showing the position of the bands and of the Fermi level. Discuss how this structure can give rise to devices offering both a high transconductance (g_m) and large cut-off frequency (f_T). In recent years pseudomorphic (p-HEMT) and metamorphic (m-HEMT) approaches have been used. What is mean by these terms and what are the possible improvements and limitations of this approach?

(5)

d. Estimate the maximum intrinsic g_m and f_T for a HEMT with a 150nm gate length, a 250nm gate width and a 2DEG of sheet concentration of $3\times10^{16}\ m^{-2}$ and a mobility of $1.6\ m^2 V^{-1} s^{-1}$.

In practice the g_m value calculated can never be realised due to velocity saturation. Calculate a revised g_m value assuming electrons reach their saturation velocity as soon as the gate voltage reaches pinch-off at 0.2V.

(5)

MH / RAH