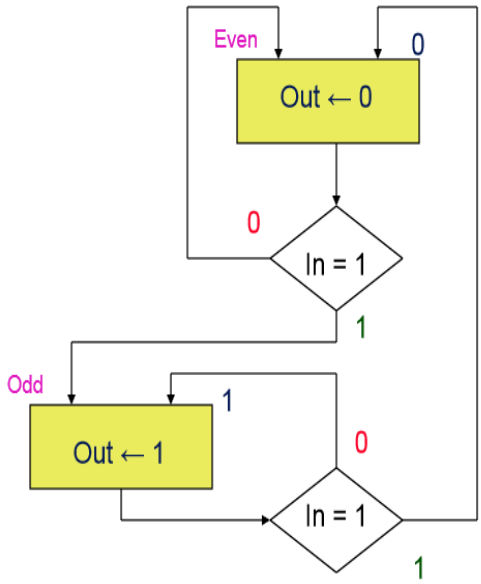
EEE336/339 Solution Sheet 4 – NJP

1.



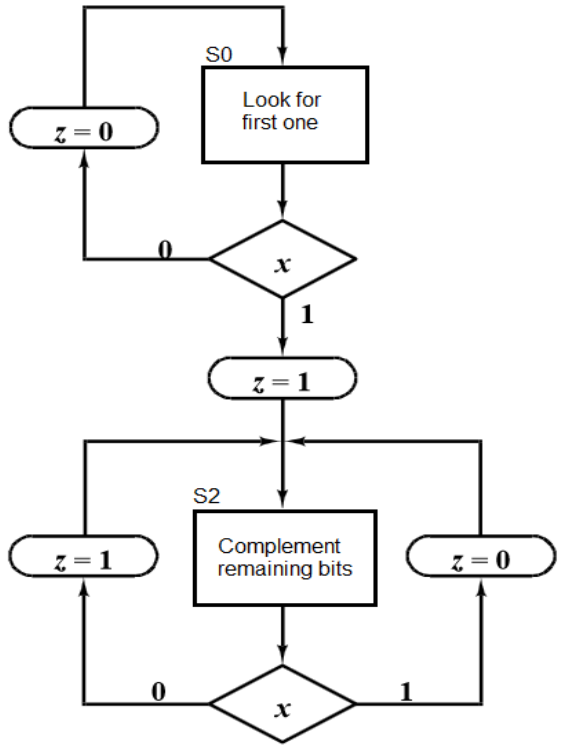
State Even – an even number of 1's received up to that point, output a 0.

State Odd – an odd number of 1s received to that point, output a 1.

In – single bit input stream

Out – single bit output

2.



Problems 1 & 2 just show the ASM for the data processing part of the machine. They do not include an interface to any controlling circuitry. That can be achieved as shown in problem 3.

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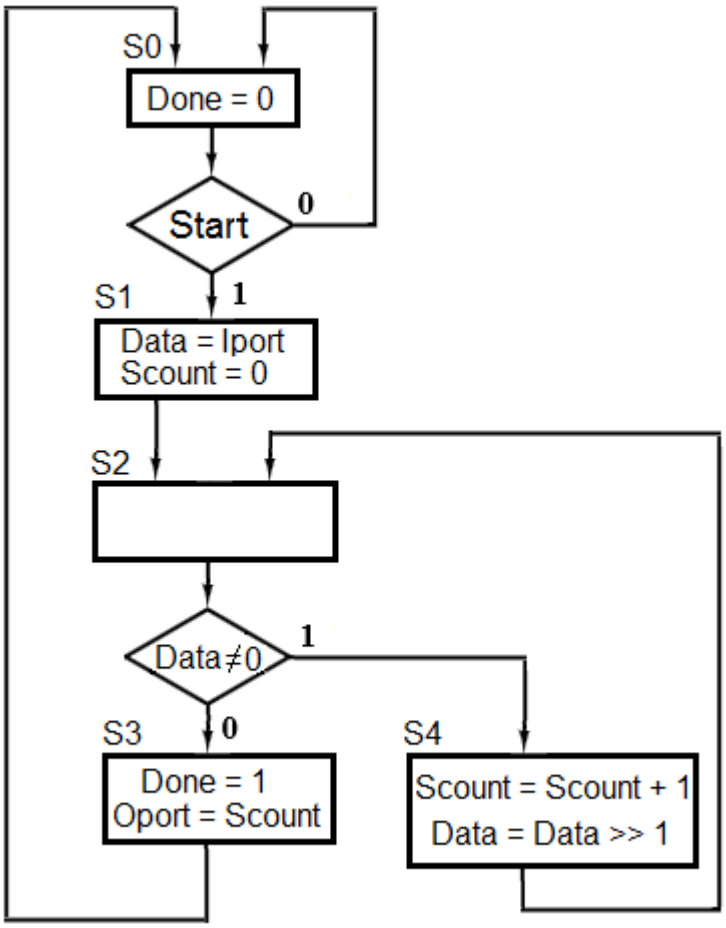
3.



State **S0** is a reset state. The **Done** signal is reset to 0 and the **Start** signal is examined each cycle to find out when to begin an operation.

When **Start** = 1, state **S1** is entered. During this cycle, the input port is read into a register called **Data** and the shift counter **Scount** is reset to 0.

In state **S2** the value of **Data** is examined. If it is not equal to zero, then it must contain ones.

In state **S3**, there are no more ones in data. The signal **Done** is set to one to indicate the end of the conversion. The value of **Scount**, the number of shifts that it took to get rid of all of the ones, is sent to the output port.

In state **S4**, a shift of one place to the right takes place and **Scount** is incremented.

Remember that the register updates happen at the end of the cycle.