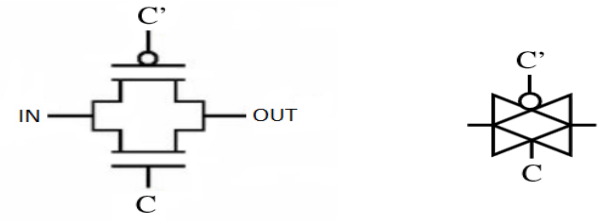
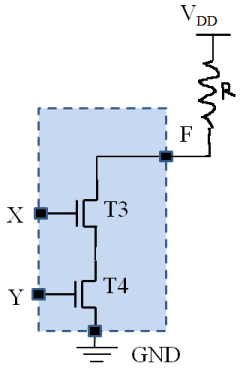
1. a. **i)** A transmission gate is formed when an nmos transistor is connected in parallel with a pmos transistor. It functions as an electronic switch controlled by input logic levels.



Both transistors are ON or OFF simultaneously, the nmos switch passes a good 0 but a poor 1. The pmos switch passes a good 1 but a poor 0. A bilateral switch results which passes a good 0 and good 1 in both directions. **(5)**

ii) Open-Drain refers to a device where the drain terminal of the output transistor is unconnected. It must be externally connected to V_{DD} by an external pull-up resistor.



When x = 0 y = 0 > T3 & T4 both off

x = 0 y = 1 > T3 is off

x = 1 y = 0 > T4 is off

Output F will be pulled HIGH in each case.

When x = 1 y = 1 > T3 & T4 are both on.

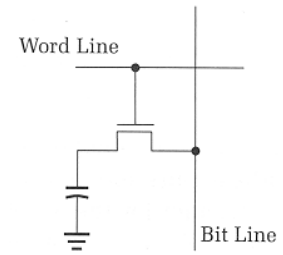
Output F will be connected to ground and LOW.

This gives the NAND function. **(5)**

b. The NAND gate will generally perform faster than the NOR gate. This is because nmos transistors have a lower 'on' resistance than pmos transistors. Thus a series connection of *k* nmos transistors will have a lower 'on' resistance than *k* pmos transistors for a given silicon area. As the NAND gate has a series connection of nmos devices, it can perform faster than the NOR gate which has pmos devices in its series connection. **(4)**

c. In a DMA transfer, a direct memory access controller (DMAC) receives a signal that a peripheral is ready to transfer data. As a result, the DMAC asserts a HOLD signal to the CPU which responds with a hold acknowledgement, HOLDA; at the same time, the CPU tri-states its data bus, address bus and control lines thus relinquishing control of the memory/IO space to the DMAC. At this point the DMAC transfers data between source and destination via itself by generating the necessary addresses and control signals. On completing the transfer, the DMAC de-asserts the HOLD signal whereupon the CPU de-asserts HOLDA and reclaims control of the busses. DMA is typically used for transferring significantly sized blocks of data between memory locations or between memory and the I/O space. The reason DMA is used is because transferring large blocks of data via the processor is very inefficient – most of the time involved is taken up by internal register transfers and 'housekeeping' tasks within the CPU resulting in a poor data transfer rate. **(6)**

2. a.

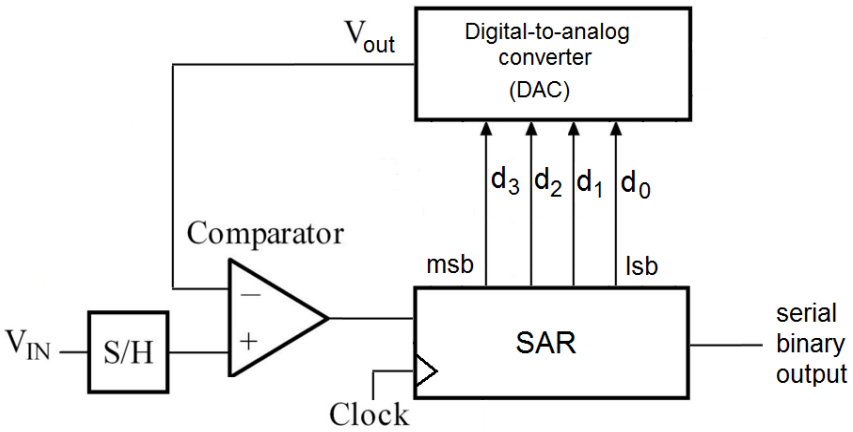


The data is stored on a capacitor which is accessed through a MOS transistor. The cell is accessed by setting the word line HIGH. **(2)**

To store a **1**, a HIGH voltage is placed on the bit line which will charge the capacitor through the 'on' transistor. To store a **0**, a LOW voltage placed on the bit line discharges the capacitor. **(2)**

To read from the cell, the bit line is pre-charged to a voltage halfway between HIGH and LOW. The word line is then set HIGH. The pre-charged bit line is pulled slightly higher or lower depending whether the capacitor voltage is HIGH or LOW. A sense amplifier is used to detect this small change and recover a **1** or **0** accordingly. **(3)**

b.



(6)

Starting with the msb, each input to the DAC is set to a '1' one at a time in decreasing order of significance. For each setting, the DAC produces an output V_{out} which is compared with the input voltage $V_{in.}$ If $V_{out} > V_{in}$ the comparator will give a high output and the set bit in the register is retained. When all bits have been tried, the conversion is complete.

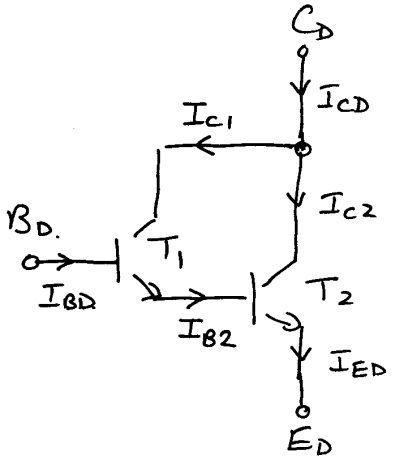
Step1, set SAR to 1000 22.3 is greater than 16 so keep bit
Step2, set SAR to 1100 22.3 is less than 24 so reset bit
Step3, set SAR to 1010 22.3 is greater than 20 so keep bit
Step4, set SAR to 1011 22.3 is greater than 22 so keep bit

Hence 1011 = 22V is the approximation of 22.3V **(4)**

c. The sampling theorem states that the sampling frequency of a signal must be at least twice the highest frequency occurring in the sampled signal. The low-pass filter is necessary to remove frequency components above the Nyquist frequency in order to eliminate aliasing. **(3)**

EEE 225 June 2014 Q3 + Q4 solution guide.

Q3 (a) (i) The solution to this question lies in finding I_{CD} in terms of I_{BD}. so that the ratio I_{CD}/I_{BD} can be found.



$I_{C1} = h_{FE1} I_{BD}$.

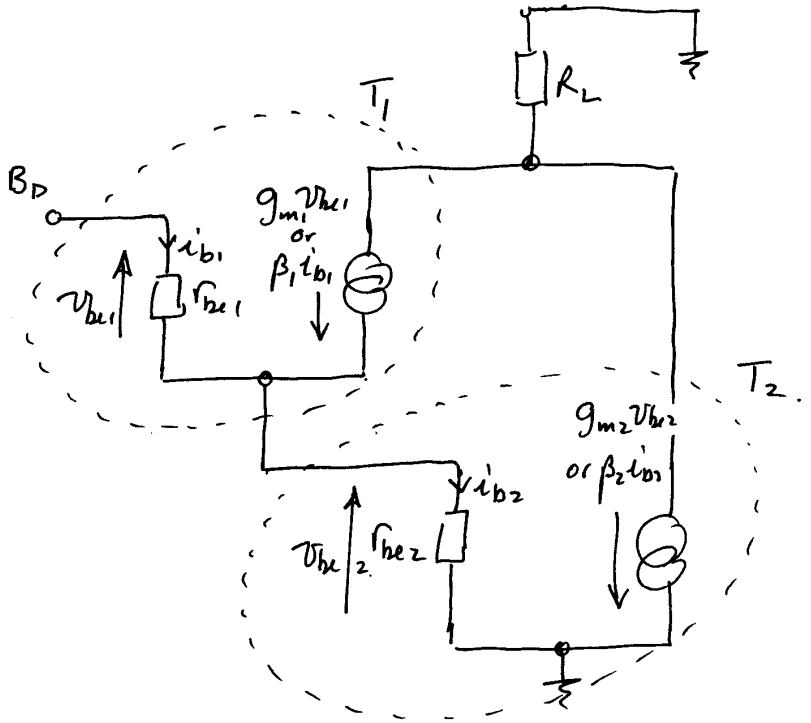
$I_{B2} = I_{E1} = I_{C1} + I_{BD} = h_{FE} I_{BD} + I_{BD}$.

$I_{C2} = h_{FE2} I_{B2}$.

$I_{CD} = I_{C1} + I_{C2}$.

collect terms together and find $\frac{I_{CD}}{I_{BD}}$.

(ii)



(ii) it is important first to recognise that the collector current of T_1 is considerably smaller than that of T_2 since

$$I_{B2} = I_{E1} = \frac{I_{C2}}{h_{FE2}}.$$

You can assume if you like that $I_{E1} \approx I_{C1}$. If you don't make that assumption..

$$I_{E1} = I_{C1} + I_{B1} = I_{C1}\left(1 + \frac{1}{h_{FE1}}\right).$$

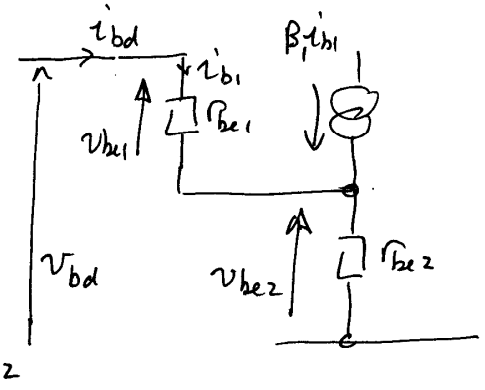
Then you can calculate g_{m1} and g_{m2} and from those obtain r_{be1} and r_{be2}.

[0.385 mA/V, 38.5 mA/V, 520 kΩ, 5.2 kΩ].

$$r_i = \frac{v_{bd}}{i_{bd}} = \frac{v_{bd}}{i_{b1}}$$

$$v_{bd} = v_{be1} + v_{be2}$$

$$i_{b1} r_{be1} \qquad i_{b1}(1+\beta_1) r_{be2}$$



This allows v_{bd} to be expressed in terms of i_{b1} so r_i is easily obtained.

[1.057 MΩ]

Q3(b) (i)

(i) BW of amplifier with gain of 50 and GBP of 40 MHz is given by

$$BW = \frac{GBP}{gain}.$$ [No].

(ii) Here you need to remember that for a first order system, $\tau = \frac{1}{\omega_{3dB}} = \frac{1}{2\pi f_{3dB}}$.

and that rise time $= 2.2\tau$.

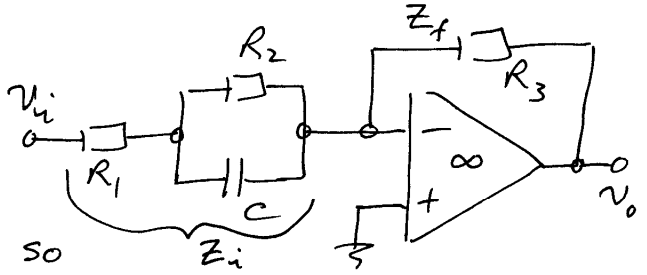
[438 ns].

(iii) You need to remember that the max rate of change of voltage in a sinusoidal waveshape is $V_p\omega$. Note that the question asks for $V_{peak\ to\ peak}$:

[7.96 V]

In parts (ii) + (iii) if you cannot remember the relationships needed they can be derived within a few minutes!

Q4 a.(i)



For l.f. $X_C \to \infty$ so
the $R_1 + R_2 \| \frac{1}{sC} \Rightarrow R_1 + R_2$.

For h.f. $X_C \to 0$ so
the $R_1 + R_2 \| \frac{1}{sC}$ combination $\Rightarrow R_1$
The amplifier is inverting so gain $= -\frac{Z_f}{Z_i}$

(ii) This is simply a matter of manipulating the three relationships given.

$$k = \frac{R_3}{R_1 + R_2} = \frac{R_3/R_1}{1 + \frac{R_2}{R_1}}$$

$$\frac{f_1}{f_0} = \frac{\frac{R_1 + R_2}{2\pi C R_1 R_2}}{\frac{1}{2\pi C R_2}} = 1 + \frac{R_2}{R_1}$$

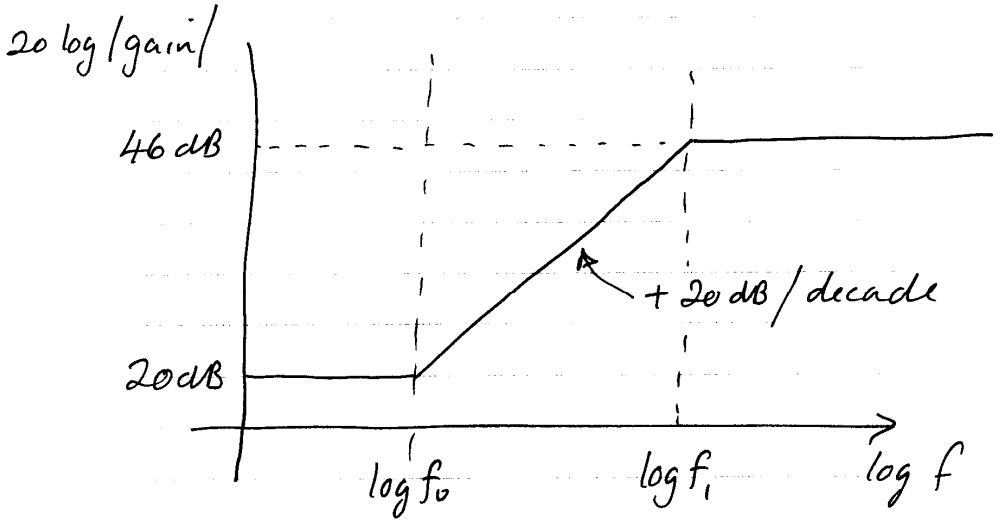
finding $\frac{R_3}{R_1}$ and $\frac{R_2}{R_1}$ from here is straightforward.

$f_0 = \frac{1}{2\pi C R_2}$ leads directly to CR_2

$$\left[3{\cdot}18\,\text{mS},\ 200,\ 19\right]$$

R_3 should have a value somewhere in the range 2kΩ to 1MΩ. A number of combinations of component value are OK.

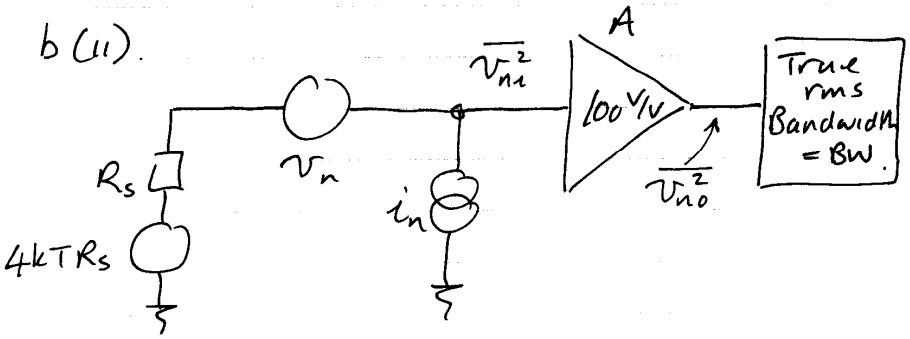
Q4 a.(iii).



You should be able to tell easily from the $\frac{v_o}{v_i}$ expression that l.f. gain < h.f. gain – even if you got part (i) wrong.

b (i) Signal to Noise ratio is what it says. The only thing you need to remember is that it is a mean-squared voltage ratio. S/N measures signal quality at some point in the circuit so it cannot provide any system noise information.

b (ii).



The noise at the amplifier input is due to three contributors

$$\overline{v_{ni}^2} = 4kTR_s + \overline{v_n^2} + \overline{i_n^2}R_s^2 \qquad V^2Hz^{-1}$$

$$\overline{v_{no}^2} = A^2\overline{v_{ni}^2} \qquad V^2Hz^{-1}$$

The meter reads the root of the integrated noise

$$v_{meter} = \sqrt{\overline{v_{no}^2} \times BW} \quad V$$

$[111\mu V]$

b(iii). To get an output signal to noise ratio of unity

$$P_{signal} = \text{integrated output noise}$$

or $$\frac{V_p^2}{2R} = \frac{\overline{v_{no}^2}\, BW}{R}$$

and because R is common to both signal and noise it can be cancelled. This gives V_p^2 at the amplifier output – the question asks for V_p at the input which is of course A times smaller than V_p at the output

$[1.57\mu V]$

EEE 225 2014 Solutions

Q5

a (i) Given N_A and N_D

If $|N_A - N_D| \gg n_i$ it is extrinsic

If $|N_A - N_D| < n_i$ it is intrinsic (2)

(ii) $N_A \approx p$ at RT (1)

(iii) $np = n_i^2$ (1)

(iv) The Fermi Level is the energy where the probability of occupancy by an electron is 50% or 0.5 (2)

b (i) $\sigma = n_i e(\mu_e + \mu_h) = 2\times10^{12} \times 1.6\times10^{-19} \times 0.89$

$= 2.85 \times 10^{-7}$ (1)

Doping it increases conductivity by 5×10^5, so

$2.85\times10^{-7} \times 5\times10^5 = 0.1425$

$n e \mu_e = 0.1425$

$n = 0.1425 / (0.85 \times 1.6\times10^{-19})$

$= 1.05 \times 10^{18} m^{-3}$ (2)

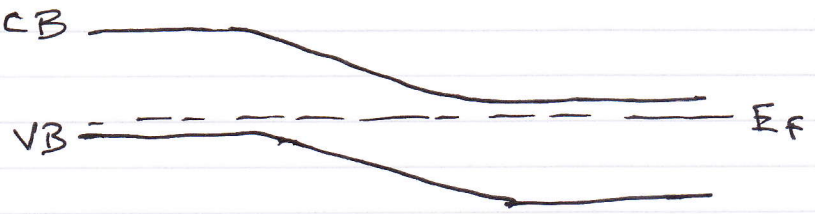
* To get an LED we need a p-n junction so dope top layer with acceptors

$10^{21} m^{-3}$ is sufficient to make it a p-type semiconductor as $(10^{21} - 10^{18}) \gg n_i$ (3)

(ii) Top layer $N_A = p = 10^{21} m^{-3}$

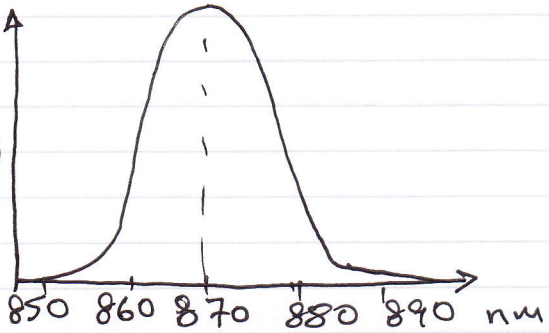
$n = \frac{n_i^2}{p} = \frac{(2\times10^{12})^2}{10^{21}} = \frac{4\times10^{24}}{10^{21}} = 4\times10^{3} m^{-3}$ (2)

(c)



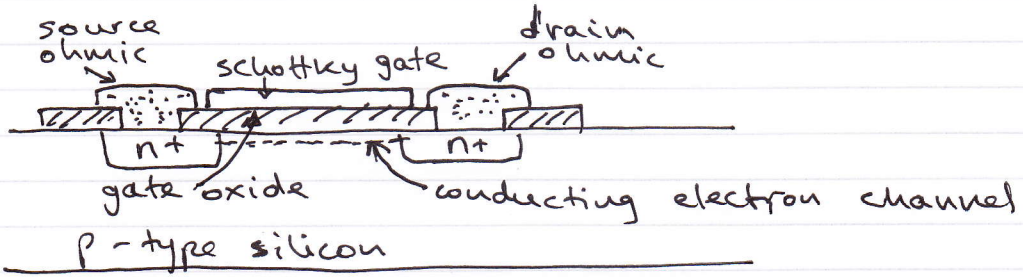
LED Band structure in equilibrium (3)

(d)



(3)

Q6 (a)



(4)

At low tive gate voltage, holes repelled from under gate. At higher V_g, electrons accumulate and form a conducting channel between Source + drain. V_{ds} causes a current to flow between S + D when channel is formed. (2)

(b) Saturation of drain current occurs when

(i) $V_{ds} \geq V_{gs} - V_T$

(ii) To obtain I_{ds}, substitute $V_{ds} = V_{gs} - V_T$ into the expression given

$$I_{ds} = \frac{\mu_e C_g}{l^2} \frac{(V_{gs} - V_T)^2}{2} .$$

(iii) Trans conductance $(g_m) = \left.\frac{d\,Id}{d\,Vgs}\right|_{Vd\ constant}$

$$g_m = \frac{\mu_e C_g}{l^2}(V_{gs} - V_T)$$

(c) $V_{ds} = V_{gs}$ when drain connected to gate

$$I_{ds} = \frac{\mu_e C_g}{l^2}\left(\frac{V_{ds} - V_T}{2}\right)^2$$

$I_{ds} = 1mA$ when $V_{ds} = 4V$
$I_{ds} = 2.77mA$ when $V_{ds} = 5V$

$$1mA = \frac{\mu_e C_g}{l^2}\left(\frac{4 - V_T}{2}\right)^2$$

$$2.77mA = \frac{\mu_e C_g}{l^2}\left(\frac{5 - V_T}{2}\right)^2$$

$$2.77 = \frac{(5 - V_T)^2}{(4 - V_T)^2}, \text{ taking square root}$$

$$(4 - V_T)\,1.66 = 5 - V_T$$
$$6.64 - 5 = 1.66\,V_T - V_T$$
$$1.66 = 0.66\,V_T$$
$$V_T = 2.51\,V \qquad (2)$$

$$1mA = \frac{\mu_e C_g}{l^2}\left(\frac{4 - 2.51}{2}\right)^2 = \frac{\mu_e C_g}{l^2}\,1.11$$

$$0.9\,mA\,V^{-1} = \frac{\mu_e C_g}{l^2} \qquad (1)$$

When $V_{ds} = 6V$, $I_{ds} = 0.9\times10^{-3}\left(\frac{6 - 2.51}{2}\right)^2 = 5.48\,mA$ (3)

(d) $\frac{\mu_e C_g}{l^2} = 0.9\times10^{-3}\,AV^{-1}$

$$l^2 = \frac{0.15\times10^{-12}}{0.9\times10^{-3}} = 0.166\times10^{-9}\,m^2$$

$l = 12.9\,\mu m$ channel length (2)