Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2011-2012 (2 hours)

Integrated Circuit Technology

Answer **THREE** questions. **No marks will be awarded for a solution to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

1. a. Describe the electronic configuration of silicon (atomic number 14) and graphite (atomic number 6) in terms of their s and p orbitals? Draw a lattice diagram to describe their bonding configuration. **(5)**

b State the stacking sequences for an HCP lattice and a FCC lattice. Show the diagrammatic 3D (non-planar) crystal structure with the atoms for each plane named clearly by its representative alphabet. What is the difference between a diamond cubic lattice and a FCC lattice ? **(5)**

c With the aid of simple diagrams, give the close packed plane stacking sequences corresponding to intrinsic and extrinsic stacking faults in the diamond cubic lattice. By means of a diagram show how the Burgers vector of the intrinsic fault may be calculated. **(5)**

d Explain with the aid of a diagram two methods to measure electrical sheet resistance. **(5)**

2. a. Explain why the Czochralski technique is not directly applicable for making GaP wafers? What are the two modifications to the process to overcome these problems? How is the control of the ingot diameter achieved and monitored in this method. **(5)**

b Describe the apparatus and processes required for the chemical vapour deposition of epitaxial Si. Indicate the way in which the deposited material is doped and comment on factors that affect layer quality: include diagrams of the apparatus and the range of deposition chamber designs. **(6)**

c CVD is used to grow a Si epitaxial layer upon a Si substrate at a temperature of 1250ºC. If the layer growth rate is 0.5µm/min and the substrate is heavily doped with boron, deduce by calculation whether autodoping of the layer would be expected to be a problem. You can assume that the activation energy for boron diffusion in Si (E) is 3.46eV, the boron diffusion pre-exponential factor (D_0) is 0.76cm^2/s and Boltzmann's constant (k) is 8.62 x 10^{-5}eV/K. **(5)**

d Describe the materials issues which affect the growth of GaN on Silicon. Describe an application area in which GaN on Si is receiving considerable attention. **(4)**

3. a. Starting from a basic p-type substrate, show diagrammatically the most important steps in a CMOS process flow consisting of adjacent p and n MOS devices. **(10)**

b Explain the process of formation of contacts to Silicon in modern day IC technology. What material is likely to replace silicon in CMOS applications and why? Name good contacts for n and p type GaAs. **(5)**

c Explain with the aid of a diagram how metal tracks can be formed using the lift-off process. **(5)**

4. a List the most common long term failure mechanisms of electronic devices. Explain the processes causing the different types of failure and how to mitigate them **(7)**

b Metal interconnect tracks are to be fabricated on an oxide surface. Before patterning the sheet resistance is evaluated to be 0.5 ohms/sq. Calculate the resistance of final tracks that are 4 mm long and have widths that are 1 micron and 5 micron respectively. If a current of 1 milliamp is measured through the outer two probes in the four-probe method, what is the voltage measured at the inner probes for these two tracks, given k_p=4.53 **(3)**

c Describe the MBE and MOCVD processes for growth. Also highlight key differences between the two. **(10)**