EEE225: Analogue and Digital Electronics

Lecture III

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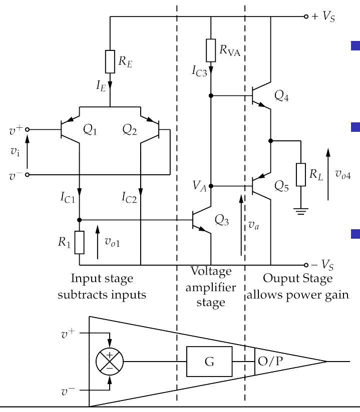
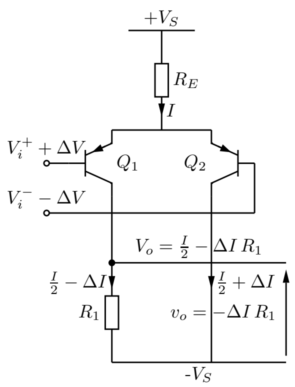
This Lecture

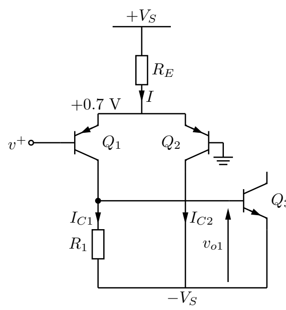


- Input stage: differential amplifier or "long tailed pair". Subtracts the inputs.
- Voltage amplifier stage (VAS): common emitter amplifier. Provides majority of voltage gain.
- Output stage: emitter follower. Increases current capability of VAS (voltage × current = power… hence "power gain".

- Opamp will not work properly without feedback. Feedback controls the gain of the circuit but also helps define the DC conditions. Feedback adjusts v_i in order to achieve the internal voltage drops required for proper operation. If $v_o = 0$, v_i will be at the value it needs to be in order to make $v_o = 0$. Feedback is *not* shown on prior slide.
- If $v^+ \approx v^- \approx 0$, V_{E1} and $V_{E2} \approx 0.7$ so $I_E \approx (+V_S - 0.7)/R_E$.
- I_E splits between Q_1 and Q_2 to form I_{C1} and I_{C2}.
- I_{C1} has two functions 1) create a voltage drop of 0.7 V across R_1 in order to bias Q_3 into conduction. 2) Provide the base current for Q_3. I_{C1} will be $0.7/R_1 + I_{C3}/h_{FE3}$.
- The value of I_{C3} varies with V_A and hence with V_{o4} but assuming $V_A = 0$, $I_{C3} = +V_S/R_{VA}$.
- I_{C2} is returned directly to the negative supply.
- In the case where $v^+ \approx v^- \neq 0$, there is a common mode input voltage, v_{cm}, and $I_E \approx (+V_S - v_{cm})/R_E$.

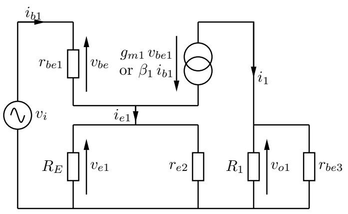


- If v^+ increases by Δv_i and v^- decreases by Δv_i, the average of v^+ and v^- is unchanged so I_E is unchanged because V_{be} is unchanged.
- If v^+ and v^- increase or decrease by Δv_i, v_i is called a "common mode signal" ideally the differential amplifier will not amplify any common mode component of the input.



We must consider the effects of three transistors. Q_1 and Q_2 are the input differential pair.

Q_3 must also be considered now because its input resistance forms part of Q_1's collector load resistance. If the input signal is regarded as v^+ with respect to ground, Q_2 looks like a common base connection and can be represented by its common base input resistance $1/g_{m2}$. The collector current of Q_1 sees two resistors in parallel, R_1 and the input resistance of Q_3. Q_3 is a common emitter amplifier *without* degeneration. Its input resistance is r_{be3}.



A small signal equivalent circuit describes the three transistor circuit block according to our simplifications.

This small signal model is very similar to the common emitter *with* degeneration from Lecture 1. In this case $R_S = 0$ and R_E and R_L are parallel combinations $R_E // r_{e2}$ and $R_1 // r_{be3}$. Since $R_E >> r_{e2}$, r_{e2} dominates. The gain expression for the circuit is (based on the degenerated CE analysis)

$$\frac{v_{o1}}{v_i} \approx -\frac{g_{m1} \cdot R_1 // r_{be3}}{2} \qquad (1)$$

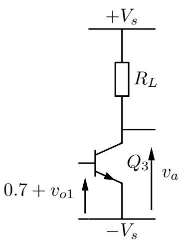
- To maximise gain make both R_1 and r_{be3} as big as possible.
- Could try to increase g_{m1} however, since $g_{m1} = \frac{e I_{C1}}{k T}$ increasing g_{m1} would require an increase of I_{C1}. I_{C1} can't change without decreasing R_1 in order to maintain the DC conditions of $I_{C1} R_1 = 0.7\ V$. There is no advantage in trying to increase g_{m1} to yield a larger gain. Other factors such as base currents and frequency dependent behaviour would also be affected.

The input resistance of the circuit is given by

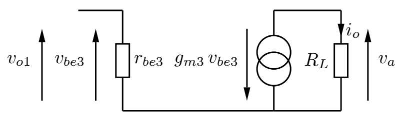
$$r_i = r_{be1} + (\beta_1 + 1)\ r_{e2} \qquad (2)$$

which is similar to the common emitter amplifier *with* degeneration. If $I_{C1} \approx I_{C2}$ and $\beta_1 \approx \beta_2$ i.e. Q_1 and Q_2 are balanced and identical, $r_i = 2\, r_{be1}$.

Voltage Amplifier Stage



The VAS is a non-degenerated common emitter circuit.



1. A small signal equivalent circuit describes the voltage amplification stage.
2. We can neglect any R_S because the effects of the finite output resistance of the differential stage have already been taken into account - we included r_{be3} in our earlier calculations.
3. v_{o1} and v_{be3} are equal.

Voltage Amplifier Stage Gain

The resistance a small signal sees looking out from Q_3's collector is the parallel combination of:

1. The input resistance of Q_4, r_{i4}.
2. The input resistance of Q_5, r_{i5}.
3. The Early resistance of Q_3, r_{ce3}.
4. The resistor R_{VA}.

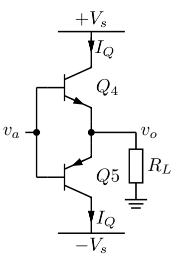
R_{VA} is much smaller than any of the others and so dominates the value of R_L. $R_L \approx R_{VA}$.

Some standard analysis...

$$v_a = i_o\, R_L \qquad (3)$$
$$i_o = -g_{m3}\, v_{be3} \qquad (4)$$
$$\text{so } v_a = -g_{m3}\, v_{be3}\, R_L \qquad (5)$$
$$\text{but } v_{be3} = v_{o1} \qquad (6)$$
$$\text{so } v_a = -g_{m3}\, v_{o1}\, R_L \qquad (7)$$
$$\frac{v_a}{v_{o1}} = -g_{m3}\, R_L \qquad (8)$$

For typical values the gain of the voltage amplifier stage when R_{VA} is a resistor is a few hundred.

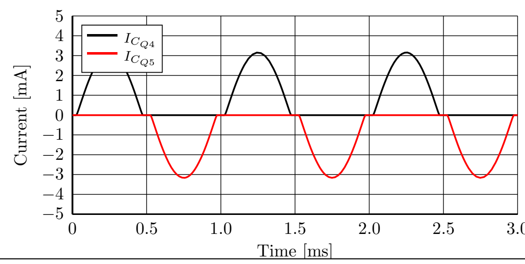
The Output Stage



An NPN and PNP emitter follower.

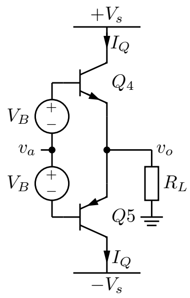
- The output stage operates on "large" signals.
- Q_4 deals with positive currents - from $+V_s$ into the ground via R_L
- Q_5 deals with negative currents - from the ground via R_L into $-V_s$
- The signals are "large" because the quiescent current I_Q is *not* many times bigger than the signal currents.
- The signal currents upset the quiescent conditions. It is not fruitful to draw a small signal diagram.

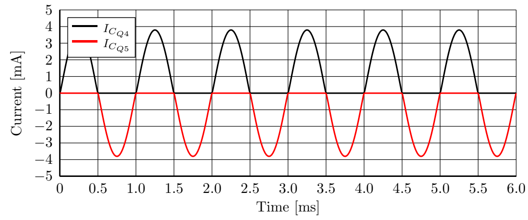
- The voltage gain of the output stage is approximately unity.
- The objective of the output stage is to increase the VAS's ability to drive current into the load resistance.
- The combination of the VAS and OPS provide power gain.
- The transistors must be turned on by the signal, consequently a kind of distortion - "Crossover Distortion" exists around the transistion between Q_4 conduction and Q_5 conduction.

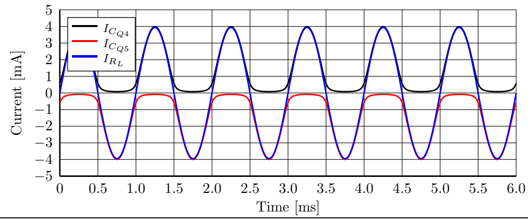


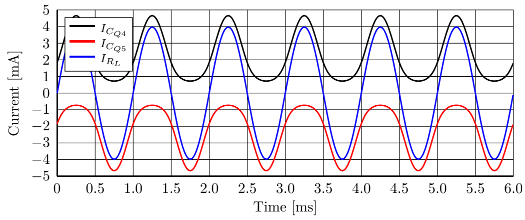
Biasing the Output Stage

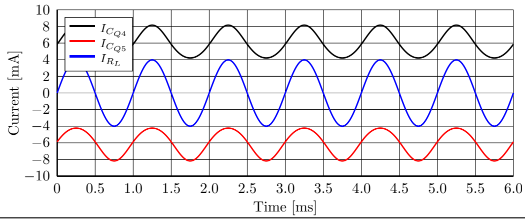
- Biasing the transistors into conduction can lessen the effect of crossover distortion a great deal.
- It also allows us to think about the relationship between the quiescent current and the signal current in the push pull stage.
- These thoughts can be widely generalised.
- Consider five sets of V_B which yield differing "angles of conduction".
- Without any bias each transistor conducts for slightly less than 1/2 a cycle $< 180°$











Review

- Reviewed structure of the Opamp.
- Considered DC conditions of the input and voltage amplifier stages.
- Described the gain and input resistance of the input stage to a differential signal.
- Analysed the voltage amplification stage from a small signal perspective.
- Qualitatively described the push-pull emitter follower output stage.
- Introduced the idea of "classes" of amplifier and "conduction angle".
- Noted that the relative size of the quiescent current and the signal current will determine the conduction angle and so the class of amplifier.