The University of Sheffield, Department EEE

Electronic Devices in Circuits Tutorial Solutions: Power Amplifiers

In the answers to these questions, the symbols used are as follows:

V_L	=	load voltage
V_{LP}	=	peak value of load voltage waveform
V_{LPM}	=	maximum possible value of V_{LP}
V_S	=	supply voltage
I_S	=	supply current
I_L	=	load current
I_{LP}	=	peak value of I_L
I_{LPM}	=	maximum possible value of I_{LP}
P_D	=	power dissipated in output transistor(s) (averaged over one cycle of V_L)
P_{DM}	=	maximum possible value of P_D as V_{LP} is varied
P_L	=	load power (averaged over one cycle of V_L)
P_{LM}	=	maximum possible value of P_L as V_{LP} is varied
P_S	=	power supplied by power supply
R_L	=	load resistance

It is necessary to know (and know how to derive) the relationships describing the rms and average values of the three waveforms in these questions in terms of their peak values.

1 (a) SINUSOIDAL SIGNAL

(i) The assumption that the output devices can work with a V_{CE} as low as 0V means that V_{LP} can equal V_S. The amplifier must supply a maximum power of 150W and maximum power will be delivered to the load when the voltage across the load is largest, ie when $V_{LPM}=V_S$. Thus

$$P_{LM} = 150\text{W} = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LPM}^2}{2R_L} \text{ since for a sinusoid } V_{RMS} = V_P/2^{1/2}.$$

This gives $V_{LPM} = V_S = \pm 49\text{V}$

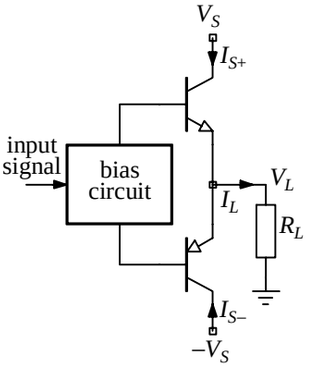

Figure 1a

(ii) At maximum power output, $V_{LP} = V_S$ and since V_{LP} appears across the resistive load, I_{LP} must be $V_S/R_L = 6.13\text{A}$

(iii) At maximum power output, $V_{LP} = V_S$. The amplifier is class B so the output transistors are never "on" together and never "off" together. In figure 1a, the top transistor deals with the positive half cycles and the bottom transistor deals with the negative ones. This means that the positive supply provides the load current in positive half cycles and the negative supply provides the current for the negative half cycles. The current waveforms supplied by the

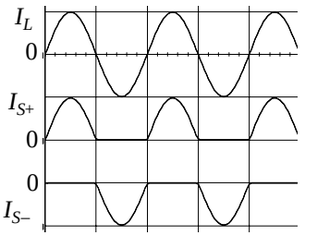

Figure 1b

power supplies are thus half wave rectified versions of the load current waveform, as shown in figure 1b.

Efficiency (η) is 100 x [output power (P_L) over input power (P_S)]

$P_S = \frac{1}{T}\int_0^T V_S\, I_S(t)\, dt = V_S\, \frac{1}{T}\int_0^T I_S(t)\, dt = V_S\, I_{S(AVE)} = V_S \frac{I_{LPM}}{\pi} = \frac{V_S^2}{\pi R_L}$ per supply giving a total supply power (from both supplies) of $\frac{2V_S^2}{\pi R_L}$

$P_L = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LPM}^2}{2R_L} = \frac{V_S^2}{2R_L}$ and thus $\eta = 100 \text{ x } \frac{P_L}{P_S} = \frac{100\pi}{4} = 78.5\%$.

(iv) To find the V_{LP} at which P_D is a maximum, it is necessary to express P_D as a function of V_{LP} and then differentiate to find the V_{LP} condition that maximises P_D. Using the principle of energy conservation, $P_S = P_D + P_L$.

$P_S = 2V_S\, I_{S(AVE)}$, as shown in part **(iii)**, and $I_{S(AVE)} = I_{LP} / \pi = V_{LP} / \pi R_L$ per supply. Thus total $P_S = 2V_S \frac{V_{LP}}{\pi R_L}$. $P_L = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LP}^2}{2R_L}$ since V_L appears across a simple resistive load. P_D is therefore given by:- $P_D = P_S - P_L = \frac{2V_S V_{LP}}{\pi R_L} - \frac{V_{LP}^2}{2R_L}$. Differentiating and equating to zero to find the maximum gives:

$\frac{dP_D}{dV_{LP}} = \frac{2V_S}{\pi R_L} - \frac{2V_{LP}}{2R_L} = 0$ or P_D is a maximum when $V_{LP} = 2V_S / \pi = 31.2$V.

(v) The maximum power dissipation in the output stage can be worked out using the expression for P_D, and the V_{LP} for maximum P_D, worked out in part **(iv)**:-

$P_{DM} = \frac{2V_S V_{LP}}{\pi R_L} - \frac{V_{LP}^2}{2R_L} = \frac{2V_S\left(\frac{2V_S}{\pi}\right)}{\pi R_L} - \frac{\left(\frac{2V_S}{\pi}\right)^2}{2R_L} = \frac{2V_S{}^2}{\pi^2 R_L} =$ 60.8W in total or 30.4W per transistor.

(vi) Both transistors are mounted onto the same heatsink, so 30.4W flows through the junction-to-case and case-to-sink thermal resistances, θ_{JC} and θ_{CS} respectively, and 60.8W flows through the sink-to-air thermal resistance, θ_{SA}. Since there are two conditions set, a trial assuming one and testing the other must be made to find the maximum θ_{CS} that can be used while still satisfying **both** conditions. In this case one can proceed as follows:

Suppose the junction temperature of 150°C is the limiting condition here. Each transistor dissipates 30.4W which must flow through a θ_{JC} of 0.75°C W^{-1} and a θ_{CS} of 1.0°C W^{-1} to reach the heatsink.

Thus $T_S = T_J - P_D(\theta_{JC} + \theta_{CS}) = 150 - 30.4(0.75 + 1.0) = 96.8$°C. This figure, based on the maximum allowed junction temperature, is higher than the maximum allowed heatsink temperature so the heatsink temperature must be the limiting condition; the initial supposition was wrong.

Using the heatsink temperature condition, $T_S = 90^oC = T_A + 2P_D\theta_{SA}$ or maximum θ_{SA} that can be used is $0.9^oC\ W^{-1}$.

1 (b) TRIANGULAR SIGNAL

The arguments here are exactly the same as those for the sinusoidal case. The difference is due to the fact that rms and average values are for the triangular waveform are different from those appropriate for a sinusoid.

(i) The difference here is the rms value of a triangular wave:-

$P_{LM} = 150W = \dfrac{V_{LRMS}^2}{R_L} = \dfrac{V_{LPM}^2}{3R_L}$ since for a sinusoid $V_{RMS} = V_P/3^{1/2}$. This gives $V_{LPM} = V_S = \pm 60V$

(ii) At maximum power output, $V_{LP} = V_S$ and since V_{LP} appears across the resistive load, I_{LP} must be $V_S/R_L = 7.5A$

(iii) The differences here are the rms value of a triangular wave and the average value of a half wave rectified triangular wave:-

$P_S = \dfrac{1}{T}\int_0^T V_S\, I_S(t)\, dt = V_S\, \dfrac{1}{T}\int_0^T I_S(t)\, dt = V_S\, I_{S(AVE)} = V_S \dfrac{I_{LPM}}{4} = \dfrac{V_S^2}{4R_L}$ per supply giving a total supply power (from both supplies) of $\dfrac{2V_S^2}{4R_L}$

$P_L = \dfrac{V_{LRMS}^2}{R_L} = \dfrac{V_{LPM}^2}{3R_L} = \dfrac{V_S^2}{3R_L}$ and thus $\eta = 100 \times \dfrac{P_L}{P_S} = \dfrac{100 \times 2}{3} = 67\%$.

(iv) The differences here are the rms value of a triangular wave and the average value of a half wave rectified triangular wave:-

$P_S = 2V_S\, I_{S(AVE)}$ and $I_{S(AVE)} = I_{LP} / 4 = V_{LP} / 4R_L$ per supply. Thus total $P_S = 2V_S \dfrac{V_{LP}}{4R_L}$.

$P_L = \dfrac{V_{LRMS}^2}{R_L} = \dfrac{V_{LP}^2}{3R_L}$ since V_L appears across a simple resistive load. P_D is therefore given by:-

$P_D = P_S - P_L = \dfrac{2V_S V_{LP}}{4R_L} - \dfrac{V_{LP}^2}{3R_L}$. Differentiating and equating to zero to find the maximum gives: $\dfrac{dP_D}{dV_{LP}} = \dfrac{2V_S}{4R_L} - \dfrac{2V_{LP}}{3R_L} = 0$ or P_D is a maximum when $V_{LP} = 3V_S / 4 = 45V$.

(v) As in part **(a) (v)** :

$P_{DM} = \dfrac{2V_S V_{LP}}{4R_L} - \dfrac{V_{LP}^2}{3R_L} = \dfrac{2V_S\left(\dfrac{3V_S}{4}\right)}{4R_L} - \dfrac{\left(\dfrac{3V_S}{4}\right)^2}{3R_L} = \dfrac{3V_S{}^2}{16R_L} =$ 84.4W in total or 42.2W per transistor.

(vi) Suppose the junction temperature of 150°C is the limiting condition here. Each transistor dissipates 42.2W which must flow through a θ_{JC} of 0.75°C W^{-1} and a θ_{CS} of 1.0°C W^{-1} to reach the heatsink.

Thus $T_S = T_J - P_D(\theta_{JC} + \theta_{CS}) = 150 - 42.2(0.75 + 1.0) = 76.2$°C. This figure, based on the maximum allowed junction temperature, is lower than the maximum allowed heatsink temperature so the junction temperature must be the limiting condition; the initial supposition was correct.

Using this heatsink temperature, $T_S = 76.2$°C $= T_A + 2P_D\theta_{SA}$ or maximum θ_{SA} that can be used is 0.49°C W^{-1}.

1 (c) SQUARE WAVEFORM

Again, the arguments are as before but the answers are different because the waveshape is now square - the square wave is probably the easiest of the three.

(i) Here the rms value of a square wave must be used:-

$P_{LM} = 150\text{W} = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LPM}^2}{R_L}$ since for a square wave $V_{RMS} = V_P$. This gives $V_{LPM} = V_S = \pm$ 34.6V.

(ii) At maximum power output, $V_{LP} = V_S$ and since V_{LP} appears across the resistive load, I_{LP} must be $V_S/R_L = 4.33$A

(iii) The rms value of a square wave and the average value of a half wave rectified square wave must be used here:-

$$P_S = \frac{1}{T}\int_0^T V_S\, I_S(t)\, dt \;=\; V_S\, \frac{1}{T}\int_0^T I_S(t)\, dt \;=\; V_S\, I_{S(AVE)} \;=\; V_S\, \frac{I_{LPM}}{2} \;=\; \frac{V_S^2}{2R_L}$$ per supply giving a total supply power (from both supplies) of $\frac{2V_S^2}{2R_L}$

$$P_L \;=\; \frac{V_{LRMS}^2}{R_L} \;=\; \frac{V_{LPM}^2}{R_L} \;=\; \frac{V_S^2}{R_L}$$ and thus $\eta \;=\; 100 \text{ x } \frac{P_L}{P_S} \;=\; \frac{100 \text{ x } 1}{1} \;=\; 100\%$.

(iv) Again the rms and average voltages used must be appropriate for a square load voltage waveform:

$P_S = 2V_S\, I_{S(AVE)}$ and $I_{S(AVE)} = I_{LP} / 2 = V_{LP} / 2R_L$ per supply. Thus total $P_S = 2V_S \frac{V_{LP}}{2R_L}$.

$P_L = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LP}^2}{R_L}$ since V_L appears across a simple resistive load. P_D is therefore given by:-

$P_D = P_S - P_L = \frac{2V_SV_{LP}}{2R_L} - \frac{V_{LP}^2}{R_L}$. Differentiating and equating to zero to find the maximum gives: $\frac{dP_D}{dV_{LP}} = \frac{V_S}{R_L} - \frac{2V_{LP}}{R_L} = 0$ or P_D is a maximum when $V_{LP} = V_S / 2 = 17.3$V.

(v) As in part **(a) (v)** :

$$P_{DM} = \frac{V_S V_{LP}}{R_L} - \frac{V_{LP}^2}{R_L} = \frac{V_S\left(\frac{V_S}{2}\right)}{R_L} - \frac{\left(\frac{V_S}{2}\right)^2}{R_L} = \frac{V_S{}^2}{4R_L} = 37.5\text{W in total or } 18.8\text{W per transistor.}$$

(vi) Suppose the junction temperature of 150°C is the limiting condition here. Each transistor dissipates 18.8W which must flow through a θ_{JC} of 0.75°C W^{-1} and a θ_{CS} of 1.0°C W^{-1} to reach the heatsink.

Thus $T_S = T_J - P_D(\theta_{JC} + \theta_{CS}) = 150 - 18.8(0.75 + 1.0) = 117^oC$. This figure, based on the maximum allowed junction temperature, is higher than the maximum allowed heatsink temperature so the heatsink temperature must be the limiting condition; the initial supposition was incorrect.

Using this heatsink temperature, $T_S = 90^oC = T_A + 2P_D\theta_{SA}$ or maximum θ_{SA} that can be used is 1.47°C W^{-1}.

2 In each answer to this question, **(a)** is for the sinusoid, **(b)** is for the triangular wave and **(c)** is for the square wave. In some cases the answer is the same as for the appropriate wavefom in Q1.

(i) The peak load voltage required to achieve the specified load power is unchanged by the conditions of Q2. The magnitude of the supply will have to be 5V greater than the peak load voltage in order to support the needs of the IC.

(a) VS = ± (VLPM + 5)V = ± 54V

(b) VS = ± (VLPM + 5)V = ± 65V

(c) VS = ± (VLPM + 5)V = ± 39.6V

(ii) No change to **(a) (b)** and **(c)**.

(iii) This will change because there is a bigger voltage drop across the output transistors than there was in Q1. The value of P_L has not changed from Q1 to Q2 but the value of P_S has.

$$P_L = \frac{V_{LRMS}^2}{R_L} = \frac{V_{LPM}^2}{2R_L} = \frac{V_S^2}{2R_L} \text{ and } P_S = 2V_S\, I_{S(AVE)} = 2V_S\,\frac{I_{LPM}}{\pi} = 2V_S\,\frac{V_{LPM}}{\pi R_L}$$

so $\eta = 100 \times \frac{P_L}{P_S} = \frac{100\pi V_{LPM}}{4R_L}$ = 71% for **(a)**, 61.5% fo**r (b)** and 87.6% fo**r (c)**.

(iv) The analysis here is the same as before and although the result is the symbolically the same, it is numerically different because V_S is numerically different.

(a) V_{LP} = 34.4V

(b) V_{LP} = 48.8V

(c) V_{LP} = 19.8V

(v) The symbolic answers here are as in Q1 but numerical answers are all dependent on V_S and hence have changed.

(a) P_{DM} = 36.9W per transistor or 73.8W for the whole IC.

(b) P_{DM} = 49.5W per transistor or 99W for the whole IC.

(c) P_{DM} = 24.5W per transistor or 49W for the whole IC.

(vi) The same test as was used in Q1 must be used here to find out which of the two limiting conditions, junction temperature or heatsink temperature, govern the heatsink requirements. The total device dissipation now flows through θ_{JC} and θ_{CS} since in an IC both transistors are integrated onto the same silicon chip. Note that the maximum junction temperature is lower than in Q1 - often the case for ICs.

(a) θ_{SA} = 0.22^{o}C W^{-1} governed by maximum junction temperature.

(b) θ_{SA} = -0.09^{o}C W^{-1} see note below.

(c) θ_{SA} = 0.84^{o}C W^{-1} governed by maximum junction temperature.

The answer to **(b)** is negative. This means that the temperature drop across the junction to case thermal resistance at full power dissipation is bigger than the difference between the maximum junction temperature specification and the ambient temperature. It is thus impossible to heatsink this IC so that it will operate under the specified conditions. Options would be either to use a different IC or arrange for a lower ambient by using some form of refrigeration.