EEE331 Analogue Electronics

general course description of EEE331 / EEE6037:

1. description and explanation of generic integrated circuit (IC) elements and their properties, such as operational amplifiers (OpAmps), filters etc.
2. analysis and design of very large-scale integration (VLSI) circuits and systems

teaching:

- 10 lectures, Tuesdays, 11:00-12:50, SG LT04 on the following days in 2013: 12, 19, 26 Feb.; 5, 12 March; 16, 23, 30 April; 7, 14 May
- examination: exam; consisting of 2 questions on analogue IC building blocks and 2 on high-level implementation; 3 of 4 questions must be answered
- course notes (revised 2012) : http://www.shef.ac.uk/eee/t_walther.html
- old tutorial and exam sheets are posted on: http://hercules.shef.ac.uk/eee/teach/resources/eee331/eee331.html

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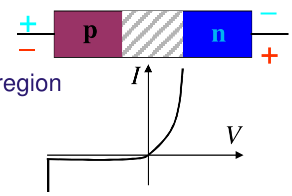
Outline syllabus first half:

- circuit operating characteristics of transistors:
  - BJTs
  - MOSFETs
- Miller transformation
- single transistor circuit elements:
  - common emitter
  - common base
  - emitter follower
- two transistor circuit elements:
  - Darlington pair
  - cascode pair
- simple IC topologies:
  - differential amplifiers
  - current mirrors
  - output stages of amplifiers

Outline syllabus second half:

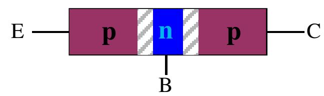
- BJT vs MOSFET
- CMOS OpAmps
- leapfrog design and signal flow graphs of analogue filters:
  - LC ladders
  - active RC filters
  - switched capacitor filters (SCF)
  - g_m-C filters

Introduction, part I: diode vs. transistor



- **diode** = single pn-junction
- diode conducts under forward bias
- diode blocks under reverse bias due to depletion region
- diode has a single *I-V* characteristic like so:

- **transistor** consists of 2 diodes, one forward and one reverse biased, with *3 terminals*:
- hence *2 types* (pnp, npn) and *4 characteristics*

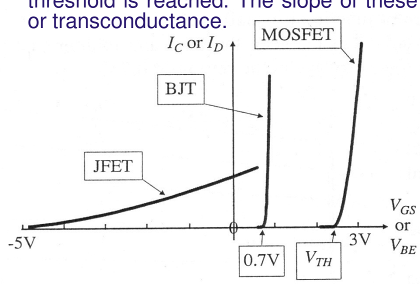


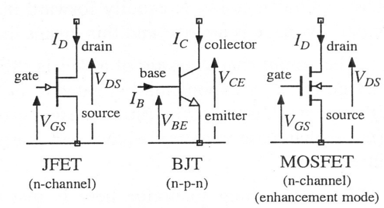
textbooks recommended for further reading:

- P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer: Analysis and design of analog integrated circuits, Wiley (New York), 2001, 4th ed.
- J. Millman and A. Grabel: Microelectronics, McGraw-Hill (Singapore), 1988, 2nd ed.
- R. Schaumann and M.E. van Valkenburg: Design of analog filters, Oxford University Press (New York), 2001
- A.S. Sedra and K.C. Smith: Microelectronic circuits, Oxford University Press (New York), 2004, 5th ed.

Introduction, part II: general transistor behaviour

- **3 terminal devices** with 1 terminal common to control input and current flow path (usually the emitter [source] for a BJT [FET]). The MOS-FET has an extra terminal called 'substrate' connected either to the source or to the most negative part of the circuit, i.e. minus of power supply.
- **output characteristic:** relationship between controlled current (output) and voltage across current flow path terminals
- **transconductance:** relationship between input control voltage (V_{BE} for a BJT; V_{GS} for a FET) and output (controlled) current (I_C for BJT, I_D for FET). These curves are similar in shape for all transistor types, with a rapid current increase after some threshold is reached. The slope of these curves is called **mutual conductance,** g_m, or transconductance.





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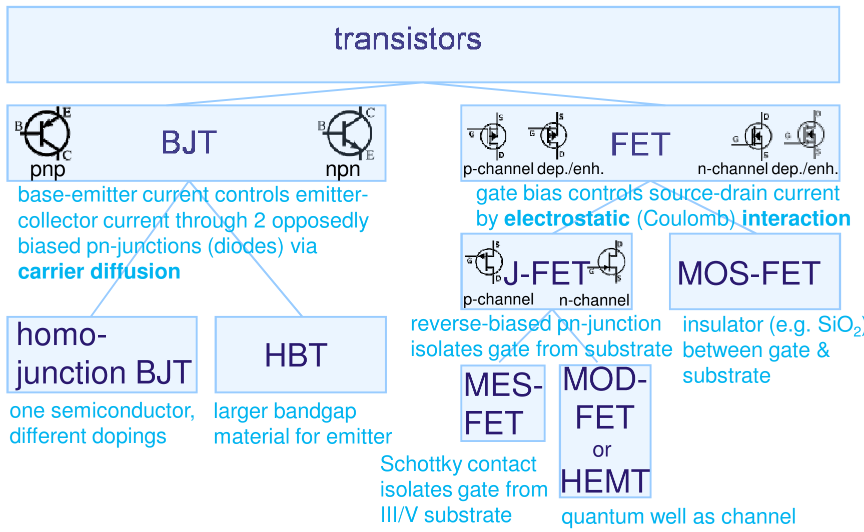
Introduction, part III: transistor families



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Introduction, part IV: comparison of BJT vs. MOSFET

criterion	**BJT**	**MOSFET**
invented	1948	1960
typical material	Si (mainly), GaAs	Si, Ge, SiGe
principle	diffusion through depletion region	field effect creates conducting channel
carrier type	minority	majority
advantage	high frequency operation, higher output currents	almost no current (~pA) when off, hence low power consumption
applications	analogue HF amplifiers	VLSI for computer chips

output characteristic

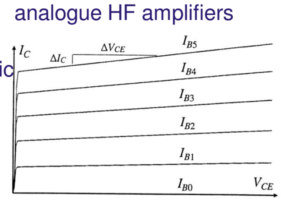


Figure 2

A BJT output characteristic.

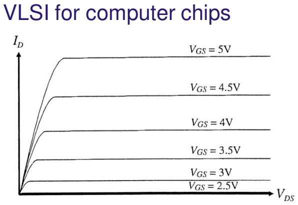


Figure 3

The output characteristics of a MOSFET

transconductance

BJT: $\boxed{I_C = I_{C0}\,[\exp(qV_{BE}/kT) - 1] \approx I_{C0}\,\exp(qV_{BE}/kT)}$

MOSFET: $\boxed{\text{for } V_{GS} > V_{thresh}\ \&\ V_{DS} > V_{GS} - V_{thresh}:\ I_D = \text{const.} \times (V_{GS} - V_{thresh})^2}$

Introduction, part V: small signal behaviour

general:

- **large signal behaviour:** appropriate for DC conditions or any signals large enough to alter the biasing conditions significantly, e.g. slew rate limiting

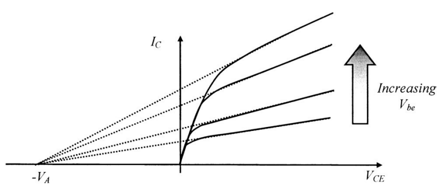
  The large signal current gain of a BJT transistor is defined as the ratio $\boxed{h_{FE}=I_C/I_B}$

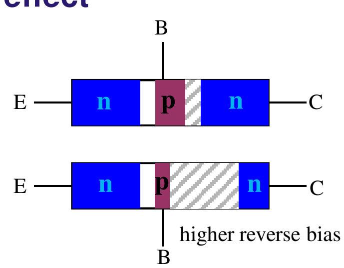
- **small signal behaviour:** appropriate for small perturbations on top of DC conditions that do not change the properties of the device significantly, e.g. high-frequency amplification of a small AC signal using a transistor near mid-point operation. Small signal models are helpful in understanding how circuit parameters affect circuit performance.

- We use lower case characters to describe small signal voltages and currents, whereas large signal quantities are denoted by Upper Case letters. For example, a DC bias voltage may be written as V_1, and a small voltage varying in time (e.g. input into an audio amplifier) may be written as v_s.

  The small signal current gain of a BJT transistor is defined as the slope $\boxed{\beta = dI_C/dI_B}$.

Introduction, part VI: the Early effect





The base-collector depletion region (hatched) increases with increasing base-collector voltage, V_{cb}. The **base width shrinks** correspondingly. Then more carriers (e^- in the case of an npn-BJT) transit the base because

1. the time for crossing the narrower base decreases and more charge carriers can transit the base without recombination, hence I_c increases.
2. the charge gradient across the base increases, hence also I_e increases.

The result of a larger net current gain α is a finite slope on the output characteristic, corresponding to a smaller output impedance, r_0. This is bad if one wants to construct a current source which ideally would have $r_0 \rightarrow \infty$ so that any voltage change across the BJT would not cause any change in the output current (all ideal curves would be horizontal). So, if the transistor has a high impedance load, such as a current source, then we need to **model the Early effect of reduced base width by including serial resistors r_{ce} (and sometimes also r_{cb}).**

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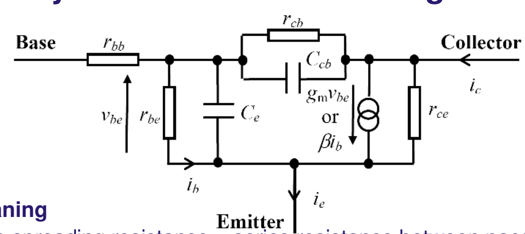
BJT, part I: hybrid-π model of small signal circuit of a BJT



symbol	meaning
r_{bb}	base spreading resistance = series resistance between pacckge wire and active part of semiconductor; can be ignored in many cases; typically 0.5Ω < r_{bb}< 50Ω
r_{be}	base incremental resistance of base-emitter junction ($\propto 1/I_b$); inverse gradient of $I_b(V_{be})$
r_{bc}	feedback resistance modelling the Early effect ($\propto 1/I_c$); may be ignored for analytical purposes **unless the transistor has a high impedance load**
r_{ce}	models the small slope of output characteristic, mostly due to the Early effect ($\propto 1/I_c$); may also be ignored **unless transistor has a high impedance load**
C_{cb}	base-collector depletion capacitance ($\propto V_{cb}$)
C_e	emitter diffusion capacitance that models the transient behaviour of charge crossing the pn-junction
β	small signal current gain for the current through r_{be}
g_m	transconductance which operates on the voltage across r_{be}

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BJT, part II: important relationships

param. **relationship**

β small signal current gain for the current through r_{be}: $\boxed{\beta = dI_c/dI_b}$

g_m transconductance, defined as

$$\boxed{g_m = \left.\frac{dI_c}{dV_{be}}\right|_{V_{ce}=const}}$$

From $I_C = I_{C0}\,[\exp(qV_{BE}/kT) - 1] \approx I_{C0}\,[\exp(qV_{BE}/kT)]$ we get in forward bias:

$$\boxed{g_m = \frac{q}{kT} I_{C0} \exp\left(\frac{qV_{be}}{kT}\right) \approx \frac{qI_{c0}}{kT} \text{ , if } h_{FE} >> 1}$$

r_{be} small signal input impedance, defined as

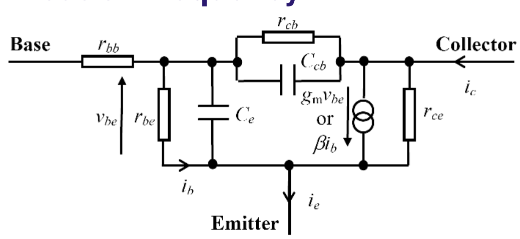
$$r_{be} = \left.\frac{dV_{be}}{dI_b}\right|_{V_{ce}=const}$$

From $g_m = dI_c/dV_{be} = dI_c/dI_b \times dI_b/dV_{be} = \beta\, r_{be}^{-1}$ we directly get $\boxed{r_{be} = \beta/g_m}$

Note that in small signal terms, $r_{be} = v_{be}/i_b$, hence also $\boxed{\beta i_b = g_m v_{be}}$

This means the BJT can be considered as a current or as a voltage amplifier.

BJT, part III: cut-off frequency



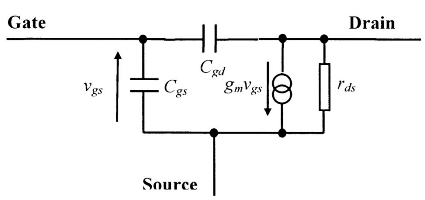
param. **relationship**

C_e emitter diffusion capacitance can be determined from measurements of the transition frequency, f_t, which is the intrinsic no-load figure-of-merit of speed for a BJT

$$\boxed{f_t = \frac{g_m}{2\pi(C_e + C_{cb})} \approx \frac{g_m}{2\pi C_e}\ \text{, if } C_e >> C_{cb}}$$

deduction: Consider frequency $f=\omega/(2\pi)$ of a resonant circuit with $R_{eff}||C_{eff}$, when all energy is alternatingly stored in R_{eff} and in C_{eff}, so that $R_{eff}=1/(\omega C_{eff})$. This gives $\omega=1/(R_{eff}C_{eff})$. Here, $i_e=0$ if the voltage $v_{be}=i_b r_{be}$ across r_{be} corresponds to the voltage drop across $C_{eff}=C_e+C_{cb}$ (as C_e, C_{cb} are in parallel) where a larger current βi_b flows. Setting $r_{be}i_b=v_{be}=\beta i_b\ /\ (\omega C_{eff})$ with $r_{be}=\beta/g_m$ gives above equation.

The small signal circuit of a MOSFET



NB: Occasionally, you may also see a substrate on a MOSFET small signal circuit diagram as the substrate can act like an extra gate. Usually the substrate is connected to $-V_{dd}$. This needs to be taken into account only if there is ripple on V_{dd}.

symbol	meaning
C_{gs}	capacitance between gate and source contact
C_{gd}	capacitance between gate and drain contact
V_{gs}	voltage between gate and source
V_{thresh}	threshold voltage that must be applied to the gate-source connection to create a conducting channel (enhancement mode MOSFET), typically a few volts
r_{ds}	apparent resistance of the conducting channel between source and drain. As V_{ds} is increased above V_{thresh} the conducting channel changes shape (shortens) and I_d then depends on V_{ds} in the saturation region ($V_{ds}> V_{gs}-V_{thresh}$ = '**overdrive voltage**').
I_d	**drain current:** $\boxed{I_d= ½\ \mu\ C_{ox}\ W/L\ (V_{gs}-V_{thresh})^2\ (1+\lambda V_{ds})}$, if $V_{ds}>V_{gs}-V_{thresh}>0$ where μ is charge-carrier mobility, C_{ox} the gate oxide capacitance per unit area, W the gate width, L the gate length and λ the channel-length modulation parameter
g_m	**transconductance** of the MOSFET device: $\boxed{g_m=2\ I_d\ /\ (V_{gs}-V_{thresh})}$
f_t	**transition frequency:** $\boxed{f_t\approx g_m/(2\pi C_{gs})}$

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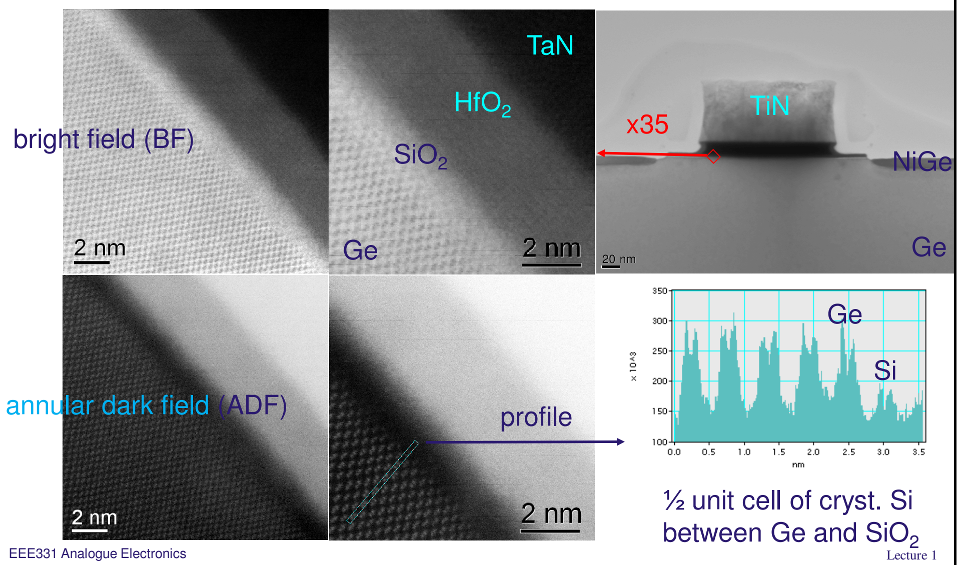
STEM ADF imaging of MOS-FET gate at atomic resolution



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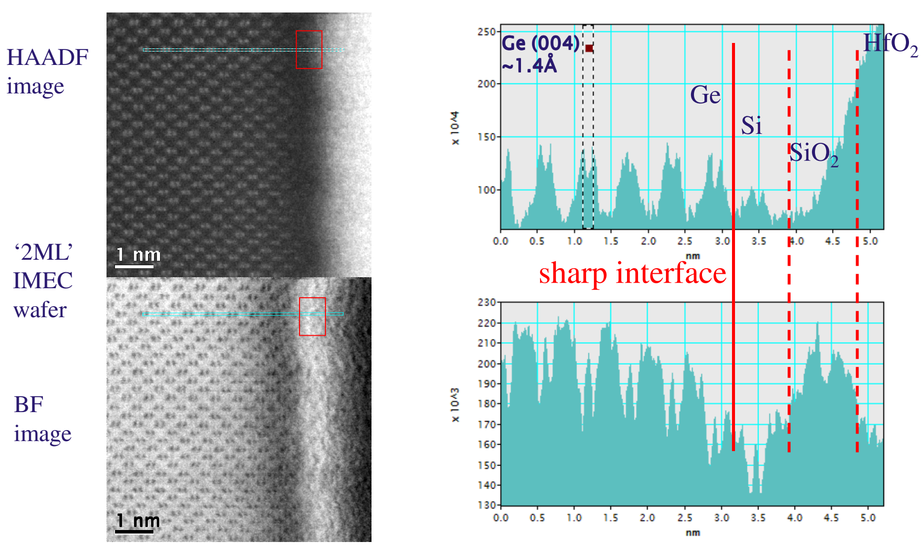

STEM ADF imaging of MOS-FET gate at atomic resolution

HAADF image

'6ML' IMEC wafer

BF image