**Examination Feedback for EEE6393 – Microsystem Packaging**
**Spring Semester 2013-14**

**General Comments:**

Students found this exam hard. I think that this is because, compared to previous year's, the paper required the candidates to demonstrate slightly more knowledge of the microsystem fabrication processes and there was a slightly lower mathematical component.

**Question 1**:

a.-f. First half of question (identifying features from a packaged chip cross-section) was generally answered well, though many candidates failed to state that potting compound consisted of silica-loaded epoxy resin.

g. Shorten interconnect length by switching from TAB frame packages to flip chip packages with ball grid arrays. Reduce the signal distortion on the PCB by implementing the interconnections as controlled impedance transmission lines (stripline, etc).

h. Recall HAST conditions: T = 120 °C,RH = 85%

*Assume Arrhenius equation is valid:* $F(H,T) = H^{-n} \exp(-E_a/k_B T)$

*Hence, acceleration factor* $AF = (0.85/0.5)^{-3} \exp(-E_a/k_B(1/393 - 1/293) = 87$

*Hence* $F(20) = 0.087/87 = \underline{0.001}$

**Question 2**:

a. $\Delta T = 40\text{-}15 = 25°C$

Consider one board in centre of stack and ignore edge effects, hence Q = 10 W

Assume no heat loss by radiation (equal emission/absorption from/to each PCB).

Assume no convection (high altitude = low air pressure).

Assume fluid flow rate > 5 l/min, hence $R_{heatexchanger}$ = 0.4 °C/W (min. value).

Fourier's Law of (conductive) heat flow: $\Delta T = QR$

Where: $R = R_{PCB} + R_{heatexchanger}$

Hence: $R_{PCB} = \Delta T/Q - R_{heatexchanger} = 25/10 - 0.4 = \underline{2.1\ °C/W}$

b. Thick, continuous metal heat spreader layer(s) extending to the edge of the PCB that is clamped to heat exchanger. Ground layer in direct contact with heat spreader (using multiple thermal vias if necessary).

c. Low temperature bonding, therefore cannot use solder. Use conductive adhesive instead - either isotropic (ICA) or anisotropic (ACA). Minimal surface tension, so no self-alignment, unlike with solder.

ICA = silver flakes in thermoset (epoxy) polymer. Deposit onto substrate bond pads by screen printing. Bond pads need to have noble metal finish for reliability. Assembly then needs separate underfill step.

ACA = conductive microspheres in epoxy. Deposit onto substrate as a continuous layer. Tall (noble metal finish) bond pads needed to provide compression during bonding. Microsphere density must be high enough to generate conductive path under compression, but low enough to prevent lateral conduction. High bond force needed. No need for separate underflow step.

d. Eutectic – lowest melting point for alloy system, hence lowest energy costs and lowest residual stress when system cooled to room temperature. Eutectic has abrupt melting point, rather than an extended softening zone. This may be beneficial or detrimental, depending on process

e. Drill holes (laser/plasma/wet etch). Stress-relief layer deposition. Seed layer deposition (electroless plating). Hole filling (copper electroplating). Attach wafer to carrier. Back thin (grinding and chemical/mechanical polishing).

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**Question 3**:

a. Shorter interconnections, therefore higher performance. Reduced size/mass. Heterogeneous integration possible. Higher yield, due to testing of individual devices prior to assembly. Simpler to design than SoC.

b.i. $R_{glass} = L/k_{glass}A_{glass} = 200x10^{-6} / (1.2 \times 50x10^{-4}) = \underline{0.033\ °C/W}$

b.ii. . $A_{via} = \pi \times (20x10^{-6})^2 = 1.2x10^{-9}\ m^2$ $A_{vias} = A_{via} \times 100x200 = 24x10^{-6}\ m^2$

$R_{via} = L/k_{Cu}A_{via} = 200x10^{-6} / (390 \times 1.2x10^{-9}) = 408\ °C/W$

$R_{vias} = R_{via}/(100x200) = 0.0204\ °C/W$

New glass area $A_{new} = A_{glass} – A_{vias} = 50x10^{-4} – 24x10^{-6} = 4.96x10^{-4} \sim A_{glass}$

Hence, revised thermal resistance (resistors in parallel):

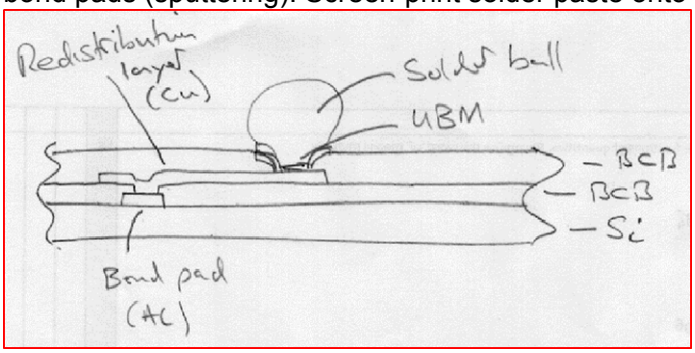
$R_{new} = (R_{glass} \times R_{vias})/ (R_{glass} + R_{vias}) = (0.033x0.0204)/(0.033 +0.0204)$

$= \underline{0.013\ °C/W}$

b.iii. Despite their negligible cross-sectional area (<1%), the vias reduce the thermal resistance of the interposer by 30 %.

c. Heat sources: Joule heating ($I^2R$) in conductors; on state; off-state (leakage current); capacctance; transients. Mitigation: use SiC rather than Si (can operate at higher T); transistor architecture; direct-bond copper heat sinks.

d.i. Pattern BCB lithographically to open vias to chip bond pads (Al). Deposit metal (Cu) layer by sputtering. Deposit resist and then pattern copper to form redistribution layer and BGA pads. Deposit another layer of BCB, pattern to open vias to BGA bond pads. (Test.) Deposit UBM onto bond pads (sputtering). Screen-print solder paste onto bond pads. Reflow to form BGA. Dice.




d.ii. Benefits: cheaper and smaller. Full justification needed for full marks.

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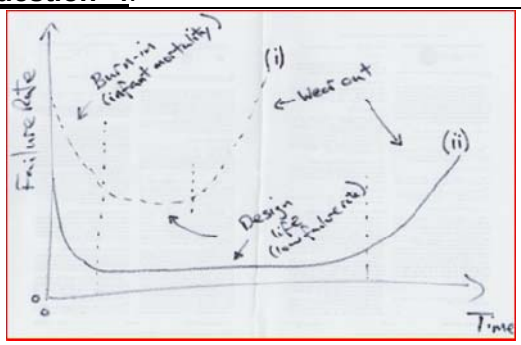
**Question 4**:

a. 


Many students drew two separate graphs and failed to indicate the differences between the two.

b. From the table: P(0)= 0.6, P(1) = 0.3, P(2) = 0.05, P(3)=0.02

Yield = $P(0) + \eta(P1) + \eta^2 P(2) + \eta^3 P(3)$ = 0.6 + 0.5x0.3 + 0.25x0.05 + 0.125x0.02 = 0.765

Hence number of faulty devices = (1-0.765)x200 = 47

c. Anisotropic etching (KOH or TMAH) of a {100} orientated silicon wafer results in 54.7° sloping side walls, hence simple photolithography plus etching enables V grooves of precise width to be made. Fibres can be seated in groove.

d. Deposition of layers of paste onto ceramic substrate. Deposition via screen printing on pre-formed layers ('green tape'). Insulating paste made from ceramic powder plus glass and organic binder. Conductive paste made from metal powder plus glass and organic binder. Resistors made from refractory metal oxides plus glass and binder. Once all layers are assembled, the stack is fired at high temperature to firstly remove binder (pre-heat stage) and then melt the low $T_m$ glass. ~15% shrinkage during firing. For LTCC, T~800 °C – non-refractory metals (Au, Ag, Pd)) can be used, for HTCC, T~ 1800 °C refractory metals used (W, Mo).

Hermetic (metal) lid added with hermetic seal formed by brazing or soldering with a metal alloys or with a low melting point glass.

e. Skin effect (due to self-induction phenomenon) means that high speed AC flows only in outer sheath of conductor, hence resistance increases, hence larger attenuation and slower propagation. Surface roughness of conductor may also start to play a part in altering resistance/velocity.

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