**Data Provided: None**

The University Of Sheffield.

**DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING**

**Spring Semester 2016-17 (3.0 hours)**

**EEE225 Analogue and Digital Electronics**

In **Part A**, answer **FIVE** questions. **No marks will be awarded for solutions to a sixth question. In Part B,** answer **all questions**. Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

## Physical constants:

| | |
|---|---|
| Charge on electron: | $-1.602 \times 10^{-19}$ C |
| Free electron rest mass: | $m_0 = 9.110 \times 10^{-31}$ kg |
| Speed of light in vacuum | $c = 2.998 \times 10^{8}$ m s$^{-1}$ |
| Planck's constant: | $h = 6.626 \times 10^{-34}$ Js |
| Boltzmann's constant: | $k = 1.381 \times 10^{-23}$ JK$^{-1}$ |
| Melting point of ice: | 0 °C = 273.2 K |
| Permittivity of free space: | $\varepsilon_0 = 8.854 \times 10^{-12}$ Fm$^{-1}$ |
| Permeability of free space: | $\mu_0 = 4\pi \times 10^{-7}$ Hm$^{-1}$ |

# PART A

**1.** With reference to digital logic gates, explain what is meant by the terms *Noise Margin* and *Fan-Out*. **(4)**

**2.** Figure 2 shows a diode logic circuit. Produce a truth table for all combinations of the input variables A and B.

The input voltage level is 5V and the diode forward voltage drop is 0.7V. What is the logic function of this circuit? What is the HIGH output voltage level?

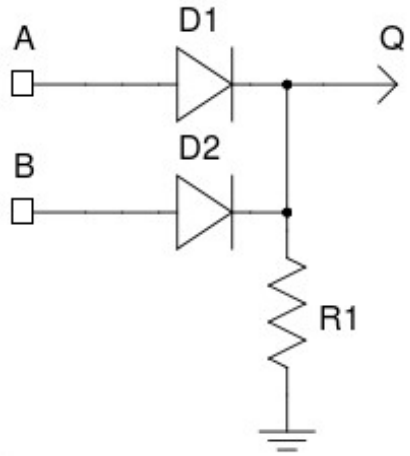


**Figure 2. Diode Logic** **(4)**

**3.** With the aid of a diagram, briefly explain the operation of a 4-bit successive-approximation Analogue-To-Digital Converter (ADC). **(4)**

**4.** Show that the output resistance of the one transistor current source in Figure 3 is given by

$$r_o = r_{ce}[1 + g_m(r_{be} /\!/ R_E)] \quad ,$$

where the symbols have their usual meaning and // signifies a parallel combination.

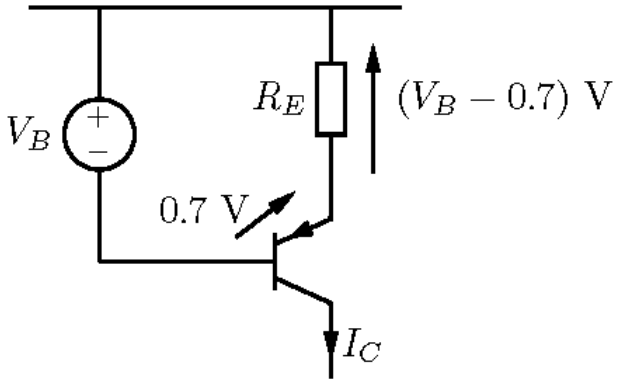


**Figure 3. One transistor current source.** **(4)**

**5.** A wideband amplifier in a matched 50 Ω system is made from two thin film amplifier modules with gains of 25 dB and 15 dB and noise figures of 4.50 dB and 7.00 dB, respectively, such that the overall amplifier bandwidth, $\Delta f$, is 1000 MHz.

**a.** What is the gain of the series combination? **(1)**

**b.** What is the noise factor of each amplifier module? **(1)**

**c.** What is the noise figure of the combination if the higher gain module is at the input end of the amplifier? **(2)**

**6.** An operational amplifier is configured as a non-inverting voltage amplifier with a dc gain of approximately 500 V/V using two resistors $R_1$ = 250 kΩ and $R_2$ = 500 Ω. The measured gain at low frequencies is 496 V/V. The -3dB frequency is observed by experiment to be 20 kHz. The roll-off above 20 kHz is 20 dB/decade, and the phase shift at 20 kHz is -45°.

You have determined, by circuit analysis, that the closed loop voltage gain expression is,

$$\frac{V_o}{V_i} = \frac{1}{\frac{1}{Av} + \frac{R_2}{R_1 + R_2}},$$

where the symbols have their usual meaning.

Determine the dc open loop gain, $A_0$, of this amplifier. **(4)**

**7.** Give 4 advantages that silica based optical fibres have over copper cables for transmitting data. **(4)**

**8.** With the aid of energy versus momentum (E-p) diagrams of a direct and indirect band-gap semiconductor, explain why one is preferred for making light emitting diodes. Mark the axes clearly and identify the band-gap energy. **(4)**

# PART B

**9. a.** When considering signal conditioning at the input stage of a sampled system:

What do you understand by the term aliasing? **(3)**

An analogue signal is to be digitised. Describe any necessary circuitry which is required before the Analog-to-Digital Converter (ADC). **(5)**

**b.** Figure 9 shows a 6-bit digital to analog converter with resistance values in Ohms.

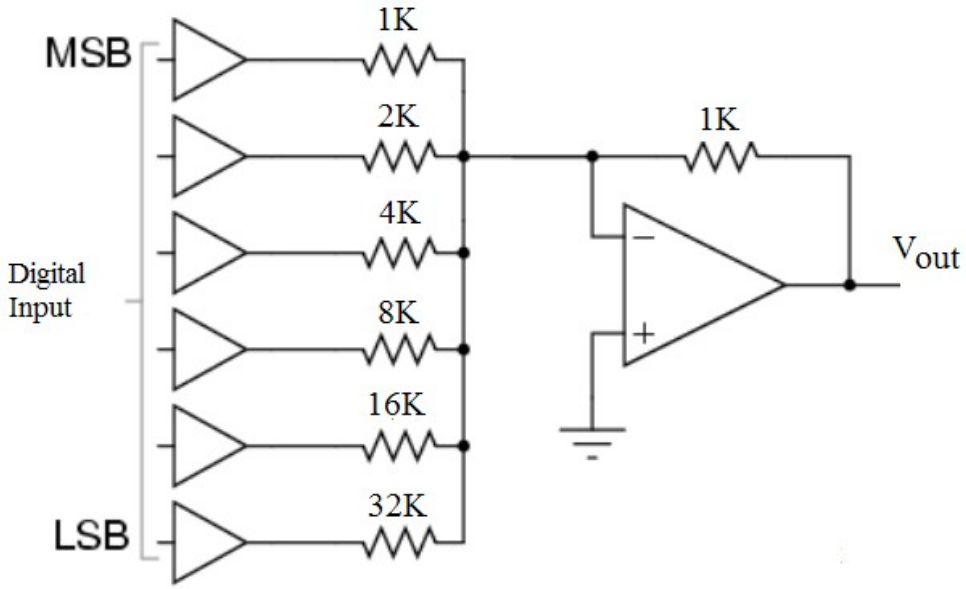


**Figure 9. Digital-to-Analog Converter**

**i)** Briefly explain the operation of the circuit. **(4)**

**ii)** Calculate the output voltage for a binary value of 110001 assuming a voltage of 5V for a high input logic level. **(4)**

**iii)** In practice, the DAC shown in Figure 9 would not be used in higher resolution applications e.g. for a 16-bit converter. Explain the reason for this. **(4)**

**10. a.**

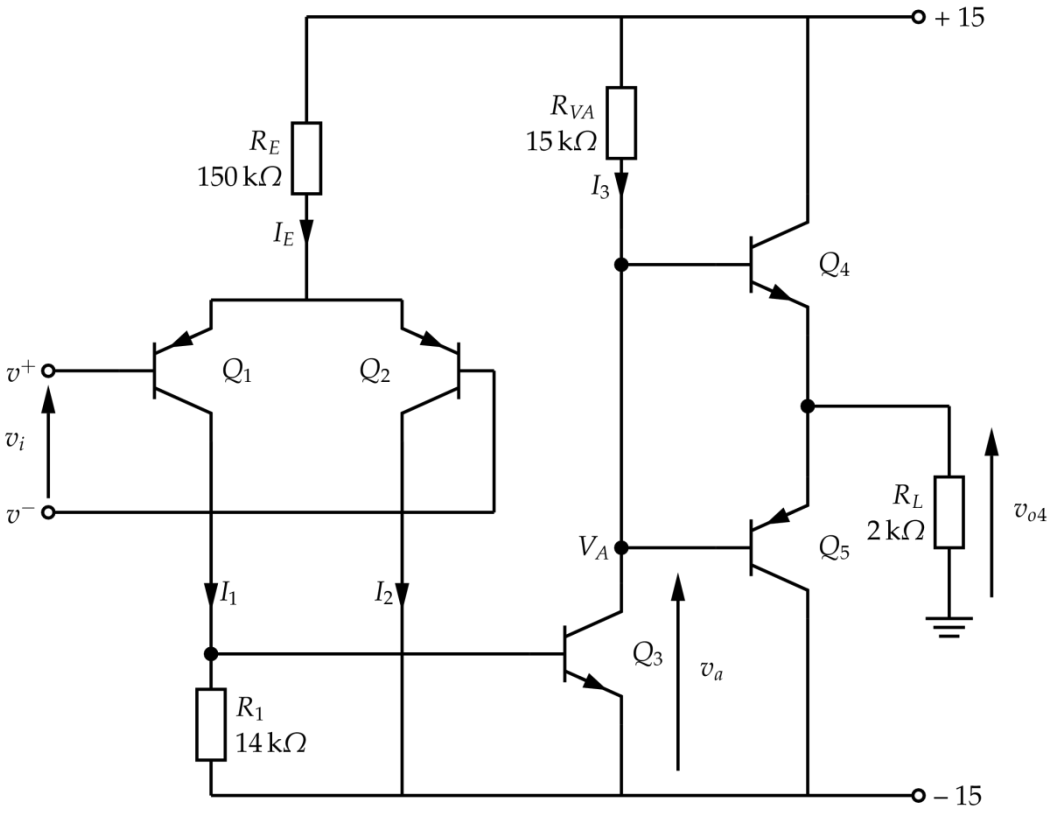


**Figure 10**

**a.** Figure 10 shows the simplified circuit diagram of a typical operational amplifier. All the transistors used have large signal and small signal current gains of 100.

**i)** Describe (with a diagram and some equations), how the circuit of Q1 and Q2 could be improved by a current mirror. Include the effect of the mirror on $I_1$ and $I_2$ by considering a small change in current and compare this with the resistively loaded case shown in Figure 10. **(9)**

**ii)** List some advantages of using a mirror in place of $R_1$. **(4)**

**b.** **i)** The circuit in Figure 10 may be improved by adding another transistor before Q3 to form a Darlington pair. Draw the circuit diagram of a Darlington pair and label the new transistor Q6. **(1)**

**ii)** Using a small signal equivalent circuit show that the input resistance of the your Darlington pair combination is approximately,

$$r_i \approx r_{be6} + \beta_6 r_{be3}$$

Where the symbols have their usual meanings. **(6)**

You can assume throughout this question that $r_{ce}$ is so large that its effects can be neglected. The relation $\beta = g_m r_{be}$ may be useful.

**11.** You apply a bias to a semiconductor p-n junction such that it works as a photodiode.

**i)** Draw the p-n junction under this bias condition. Mark clearly on the diagram the band-gap, the conduction and valence bands, the Fermi-levels, and the voltage that is being applied. **(6)**

**ii)** What is the minimum level of doping needed to achieve this p-n junction? **(6)**

**iii)** Will you dope it with acceptors or donors? **(1)**

You decide to use a level of doping that ensures that the conductivity of the p-type top layer you created is ten times that of the original n-type semiconductor.

**iv)** Estimate the electron concentration in this top layer. **(5)**

**v)** What is the longest wavelength of light this photodiode can detect and why is there this limit? **(2)**

The resistivity of intrinsic silicon at room temperature is $5\times10^{3}$ Ω-m, and $\mu_e = 0.12\ m^2\ V^{-1}\ s^{-1}$, $\mu_h = 0.05\ m^2\ V^{-1}\ s^{-1}$ and $E_g = 1.1$ eV. (Note: all the symbols have their usual meaning.)

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