

# EEE225: Analogue and Digital Electronics

## Lecture IIII

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# This Lecture

## 1 Problems with the Basic Opamp

- Differential Stage
- VAS and OPS
- Problems with the Output Stage

## 2 Solutions...

- Input Stage Balance and Gain
- Voltage amplification stage biasing current and input resistance
- Voltage amplification stage load resistance

## 3 Review

## 4 Bear

## Differential Stage Problems

### Problems with the input (differential) stage

- 1 Half of the differential signal is wasted. The collector of  $T_2$  is connected to the negative supply. The output from the differential stage is  $\Delta I$  for a given  $\Delta V$  input (see lecture 3 slide 5) but we can do better...
- 2 The balance of collector current in  $T_1$  and  $T_2$  is difficult to maintain due to loading effect of  $T_3$  - this leads to DC offset at the output.
- 3 The current flowing into the base of  $T_1$  and  $T_2$  is quite high. This input current has to be supplied by the signal source. The basic opamp has a low input resistance compared to a commercial opamp.
- 4 The effective load resistance of the differential stage (approximately // combination of  $R_1$  and  $r_{be3}$ ) is very low so the differential stage has low gain.

## VAS and OPS Problems

### Problems with the voltage amplification stage

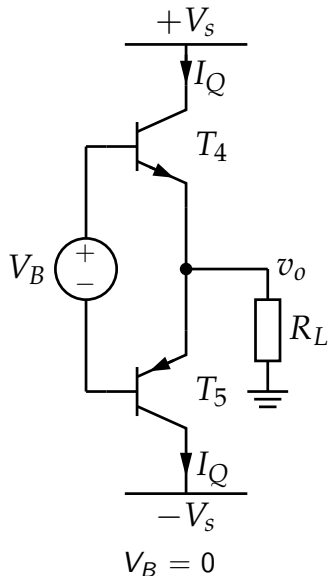
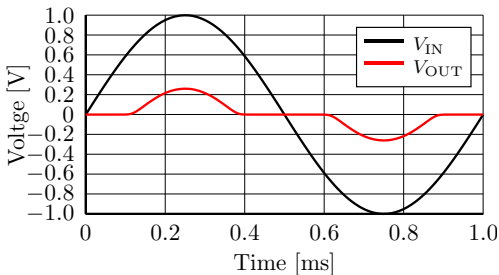
- 1  $R_{VA}$  needs to be quite small to maintain correct DC (quiescent) conditions – the quiescent current of  $T_3$  flows through  $R_{VA}$  – but the gain of the VAS is proportional to  $R_{VA}$  so a very large value is desirable which the DC current does not permit.

### Problems with the output stage

- 1 The input resistance of  $T_4$  and  $T_5$  depends on the external opamp load resistance, this affects the effective load resistance of the VAS altering its gain.
- 2 The output resistance of the emitter follower is dependent on the source resistance driving it.
- 3 Without OPS biasing  $T_4$  and  $T_5$  will give rise to severe **crossover distortion** (as per Amplifier Lab).

Briefly discussed in Lecture 3, where OPS biasing was considered,

- 1 In terms of the magnitude of the signal current compared to the quiescent current.
- 2 In terms of the **angle of conduction** of  $T_4$  and  $T_5$  as a fraction of one cycle ( $360^\circ$ )



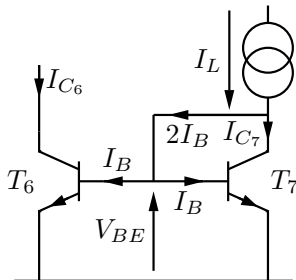
## Input Stage Balance and Gain - Current Mirrors

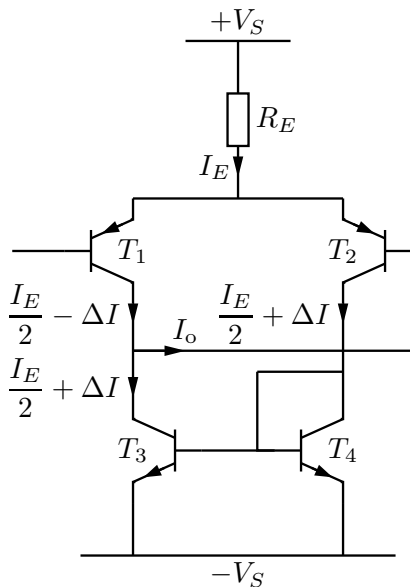
- Assume  $T_6$  and  $T_7$  are identical
- Circuit tries to make  $I_{C6} = I_L$
- Collector and base of  $T_7$  connected together
- Base of  $T_6$  and  $T_7$  connected together
- Emitters of  $T_6$  and  $T_7$  connected together
- $V_{BE}$  identical for both transistors

$I_L$  develops a  $V_{BE}$  sufficient to make  $T_7$  conduct a current  $I_{C7} = I_L - 2I_B$

$$I_L = I_{C7} \left( 1 + \frac{2}{h_{FE}} \right) \quad (1)$$

$$I_{C7} = I_L \frac{h_{FE}}{2 + h_{FE}} \quad (2)$$





Suppose  $T_1$ 's base is slightly positive with respect to  $T_2$ 's. Considering the action of the current mirror we can sum currents at the collector of  $T_3$ .

$$I_o = \frac{I_E}{2} - \Delta I - \left( \frac{I_E}{2} + \Delta I \right) \quad (3)$$

$$I_o = -2\Delta I \quad (4)$$

The output signal current from the differential stage has been doubled. And the quiescent currents in  $T_1$  and  $T_2$  are now nearly identical.

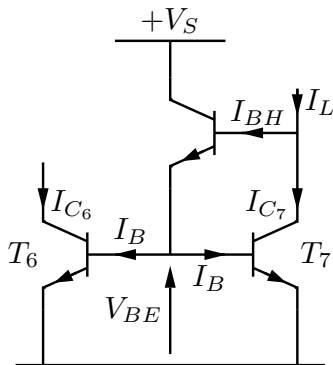
- The mirror is not perfect however as the mirroring depends on  $h_{FE}$ .
- In reality the transistors will not be identical.
- The error due to finite  $h_{FE}$  can be reduced by using a “ $\beta$  helper” transistor.

Assuming all transistors have the same  $h_{FE}$

$$I_{BH} = \frac{2I_B}{h_{FE}} \quad (5)$$

$$I_L = I_{C7} + I_{BH} \quad (6)$$

$$= I_{C7} \left( \frac{h_{FE}^2 + 2}{h_{FE}^2} \right) \quad (7)$$



For small signals,  $h_{FE}$  becomes  $\beta$  and the small signal Early resistance of  $T_7$ ,  $r_{ce}$  conducts a small part of  $i_L$  into the negative rail.



The main cause of imbalance of current in the differential pair collectors is the base current flowing into the VAS. A second transistor can be added to the VAS to form a Darlington pair.

$$I_{E3} = I_{C3} + I_{B3} \quad (8)$$

$$I_{E3} = h_{FE3} I_{B3} + I_{B3} \quad (9)$$

$$I_{E3} = I_{E8} (h_{FE3} + 1) \quad (10)$$

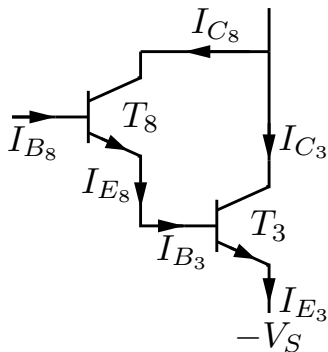
similarly

$$I_{E8} = I_{B8} (h_{FE8} + 1) \quad (11)$$

Eliminating  $I_{E8}$ ...

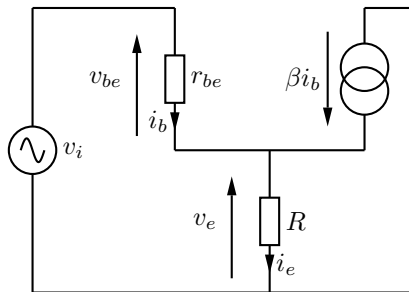
$$I_{E3} = I_{B8} (h_{FE8} + 1) (h_{FE3} + 1) \quad (12)$$

If  $h_{FE3}$  &  $h_{FE8} \gg 1$ ,  $I_{E3} = I_{C3}$   
and  $\frac{I_{C3}}{I_{B8}}$  is very large.



For small signals,

- Assume that the input resistance of  $T_3$  is “R”.
- Draw a small signal diagram.
- Sum currents at the emitter.
- Sum voltages round the input loop.

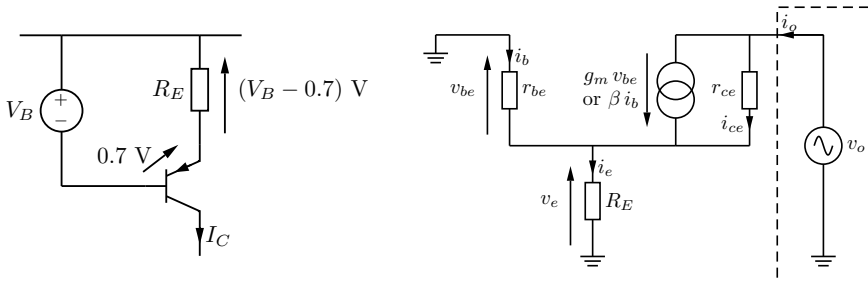


See handout “Small Signal Input Resistance of a Darlington Pair” for a possible solution. But in brief,

$$r_i = r_{be8} + \beta_8 r_{be3} \quad (13)$$

$r_i$  is increased by the  $\beta$  of the (new) upper transistor multiplied by the input resistance of the lower transistor. Remember quiescent currents in  $T_3$  and  $T_8$  will be different and so their  $g_m$ 's will be different as a consequence  $r_{be8} \neq r_{be3}$ . more precisely  $r_{be8} \gg r_{be3}$ .

From lecture 3, the resistance looking out of  $T_3$ 's collector is  $\approx R_{VA}$ . Increasing the value of  $R_{VA}$  is desirable as it increases gain. However  $T_3$ 's quiescent collector current has to flow through  $R_{VA}$  limiting its value.  $R_{VA}$  can be replaced by a current source (left) and its small signal model (right).



The effective resistance looking into the current source output – it's output resistance – will become the new  $R_{VA}$ . For analysis see handout “Small Signal Output Resistance of a Simple Current Source”. In brief  $r_o \approx r_{ce}(1 + \beta)$ .

## Review

- Considered problems related to input stage, voltage amplification stage and output stage of the simple opamp.
- Introduced current mirrors (two kinds)
- Introduced the Darlington pair
- Introduced a one transistor current source

The key points about these integrated circuit building blocks are,

- 1 To understand the bigger circuits one must first be confident with all their various circuit blocks.
- 2 To put the circuit blocks together one must appreciate how they are likely to interact.
- 3 Reducing the problem to the components which are dominant is one key to an easy analogue life...
- 4 ...the other is practice.

