Data and Equations provided at end of paper

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE6215 Nanoscale Electronic Devices

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Draw a schematic diagram of the structure of a MOSFET made from a p+ silicon wafer. Show all the main structural elements, the position of the channel and the depletion region **(3)**

b. Draw energy band diagrams for the n-channel MOSFET under the following conditions

i) In equilibrium, with the gate voltage= 0
ii) In accumulation, with a large positive gate voltage
iii) In inversion, with a negative gate voltage that just exceeds the threshold voltage

Show the position of the conduction and valence bands, the Fermi level and all other relevant features in each case **(6)**

c. Use the expression for the transconductance of a MOSFET to derive an expression for the cut off frequency (f_T). From your results, list which parameters are important for high speed operation. Discuss how state-of-the-art CMOS achieves high speed operation through modification of each of these parameters **(6)**

d. A Si MOSFET has a drain current of 40μA at V_{GS} = 1.0 V and 70 μA at V_{GS} = 2.0 V for V_{DS} = 0.1 V. Calculate the electron channel mobility for a device which has a gate length (L) of 50nm and width (Z) of 200μm. Assume $C_{OX} = 1 \times 10^{-6}$ Fm^{-2}.

Compare your mobility value with the Si bulk value and comment on the possible reasons for any difference. **(5)**

2. **a.** Figure 1 shows a simplified small signal equivalent circuit for a bipolar transistor.

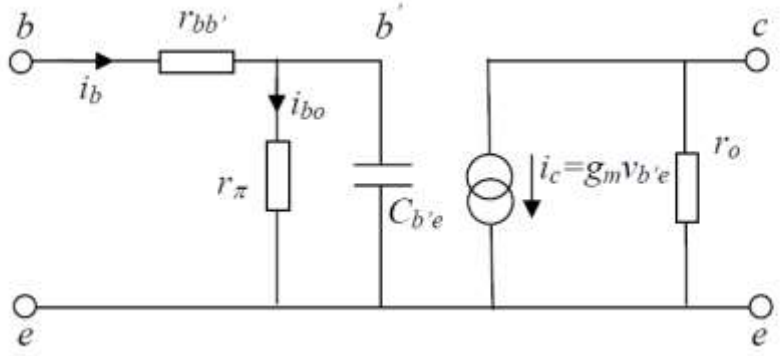

Figure 1: Small signal circuit diagram of a BJT

Provide equations which link the input and output dynamic resistances to the collector current.

An increase in r_o is often seen at high collector currents. What effect is responsible for this increase? Sketch typical output characteristics for a device which is compromised by this effect and indicate the characteristic voltage.

What is the physical origin of $r_{bb'}$ and $c_{b'e}$? How may we minimise these components? **(5)**

b. The small-signal input base current to the transistor is given by $i_b = i_{b0} + j\omega C_{b'e} V_{be}$ in the case where $r_{b'b}$ is small. Use this to derive an expression for the small signal current gain, h_{fe} as a function of ω. What simplified expressions for h_{fe} are obtained in the limits of (i) $\omega \to 0$ and (ii) $\omega \to \infty$?

What parameters influence the high speed operation of the device? How may we improve these parameters? What happens if the parameter $r_{b'b}$ cannot be assumed to be small? **(5)**

c. Explain how the HBT concept represents a major improvement over the BJT in terms of speed. What are the structural differences? How are the resistances in Figure 1 affected by these changes? **(5)**

d. InGaAs/InP HBTs are currently providing some of the highest f_T values for any transistor device. Some basic parameters for this material system are given below:

Band gaps: InP=1.34eV, InGaAs=0.74eV. Band offset- $\Delta E_C = 0.44\Delta E_g$

Electron mobility: InP=5400, InGaAs= 12500

Hole mobility: InP=200, InGaAs= 450 (all in $cm^2V^{-1}s^{-1}$)

Which material should be used for the emitter?

What are the emitter-base conduction and valence band offsets?

What is the relative ratio of the electron and hole currents at room temperature in this junction solely due to the barrier difference. **(5)**

3. **a.** Draw typical output characteristics of a MESFET for different gate voltages and indentify the linear, saturation and breakdown regions. Describe the physical origin of these three mechanisms, using diagrams if necessary. **(5)**

b. Derive an expression for the cut–off frequency of a GaAs MESFET through consideration of the a.c. input and output currents in the device. You may assume the drain current is given by: $I_D = n_s e V_{sat}$ where ($n_s e$) is the sheet charge on the gate and V_{sat} is the saturation velocity for GaAs.

Calculate the cut-off frequency for a device with a 2μm gate length. **(5)**

c. An n-channel GaAs MESFET has the following parameters:

Channel length (l)= 1μm, depth (a)= 0.5 μm. Device width (z)=25 μm. Channel doping (N_D)=2x10^{15}cm-3. Barrier potential (ϕ_{bar}) =0.8V. Channel resistivity(ρ) = 0.05Ω.m.

(i) Calculate the pinch-off voltage, V_P for this device.
(ii) Calculate the threshold voltage, V_T.
(iii) Calculate the saturated drain current at pinch-off for a gate voltage of 0.7V
(iv) Calculate the transconductance, g_m, at pinch-off. Comment on the sign of your value.

(6)

d. Sketch (i) the materials structure and (ii) the band structure of a GaAs/AlGaAs high electron mobility transistor (HEMT). Describe all the major features.

Describe how this device presents major improvements compared to a simple MESFET in terms of the transconductance (g_m) and cut-off frequency (f_T) of the device. **(4)**

4. **a.** A CMOS foundry uses a process which produces 45nm gate length MOSFETs which use 2.5nm of SiO_2 for the oxide and have an acceptor doping (N_A) of $5x10^{22}m^3$. The oxide capacitance per unit area is measured as $8x10^{-6}F.m^{-2}$. V_{FB} is measured as 0.60V and is not scaling dependent.

Calculate the threshold voltage for the device. The foundry wishes to replace this device with a scaled device of 28nm gate length. What would be the effect of this scaling on:

(i) The capacitance per unit area, C_{Ox}
(ii) The depletion width under the gate
(iii) The doping density, N_A
(iv) The overall threshold voltage V_T

It is found that the measured threshold voltage is somewhat higher than calculated and that the error is greater for the smaller device. Describe the possible mechanism that may be responsible for this? **(9)**

b. The oxide thicknesses of the MOSFET above must also scale with the device dimensions. What is the predicted value of the oxide thickness and capacitance per unit area for the 28nm gate length device?

The leakage current for field-assisted electron tunnelling across the gate oxide is known to follow the relationship

$$I_L \propto exp\left(-\mathrm{K}\phi_b^{3/2}/E\right)$$

where $m_{eff,ox}$ is the oxide electron effective mass, Φ_b is the silicon/oxide barrier height in eV (determined by the difference in electron affinity), $\epsilon_{r,ox}$ is the relative permittivity of the oxide a E is the magnitude of the electric field across the oxide in $V.m^{-1}$and K is a constant = $1x10^8$.

If the leakage current for the 45nm device is 0.7nA what is the predicted leakage current for the 28nm device? Why might this new value be unacceptable for integrated circuits?

The foundry considers the use of HfO_2 high-K oxide as a replacement for SiO_2 for the 28nm process. What value of oxide thickness should be used to maintain scaling? What value of leakage current would we now expect?

(8)

c. Why is the reduction of threshold voltage important for low power CMOS? What determines the physical lower limit for V_T?

What is meant by sub-threshold CMOS operation? What are the benefits and limitations of this approach? **(3)**

5. **a.** Calculate the following parameters for GaAs at room temperature:

(i) The electron and hole drift velocity in an electric field, E= $5x10^5$ Vm^{-1}
(ii) The electron and hole thermal velocity of holes
(iii) The electron and hole total average velocity
(iv) The mean free lifetime of electron and holes, between scattering collisions.
(v) The mean free path of electron and holes.

What would happen to the transport and value of conductivity in a GaAs MESFET if the source-drain separation is lower than the mean free path calculated in (v)?

(5)

b Draw a schematic diagram of band structure of an GaAs-AlAs n-type double barrier resonant tunnelling diode (RTD) under (i) zero bias conditions and (ii) a bias which aligns the emitter energy to that of a quantum confined state in the well.

Using the infinite well approximation, calculate the energy in eVof the two lowest lying electron states.

Assuming that there are only these two confined electron states, sketch the well, draw the output characteristics of this device.

Why might RTD devices be attractive for logic gates in the future?

(5)

c. Give an expression for the total transit time of bipolar transistor in terms of its individual components. Write the equations that link these components to the device parameters and from this write the full equation for the total transit time.

The device has capacitances C_{EB}= 3pF and C_{BC}=2pF, resistances r_E=0.1Ω and r_C=0.2Ω and has a base width of 0.2μm and a collector width of 1μm.

Calculate the cut-off frequency, f_T for emitter currents of 0.2mA, 2mA and 20mA. What is the significance of the change with collector current?

(6)

d. Describe one materials and one device approach which may offer potential for high speed electronic devices in the future. What are the prospects and present limitations with these approaches **(4)**

6. a. State of the art CMOS devices make use of the following structural or materials features

(i) Reduced gate lengths, down to around 22nm
(ii) Strained-silicon channels
(iii) High-k dielectric gate oxide
(iv) Low-k dielectric insulation for interconnects
(v) Multiple 3-dimensional gates instead of simple planar gates

For each aspect, describe the relevance of each of these technological steps, using diagrams and equations where necessary. What physical or technological limits may prevent further implementation

(8)

b. Describe the operation of floating gate flash memory, based on a Si MOSFET, with the aid of diagrams. Explain how the device can be measured to observe a digital '0' or '1' bit and how it can be erased.

A device with a 45nm gate length and a 140nm gate width and which uses a SiO_2 insulator stack with a top oxide thickness of 4nm is addressed with a read voltage of 1.2V applied to the gate. The MOSFET threshold voltage when there is no net charge on the floating gate is 0.7V. Calculate the number of electrons required on the floating gate to change the read out to a '0' bit.

(6)

c. The structure of an Si IMPATT diode is shown in figure 2 below:

0.5μm p+ ($10^{23}m^{-3}$) Cathode
1μm n ($10^{21}m^{-3}$) Avalanche Region
0.5μm n+ ($10^{23}m^{-3}$) Anode

Figure 2: Structure of a Si IMPATT diode

Sketch (i) the carrier concentration and (ii) the electric field profile of the device. What is the transit time and the oscillation frequency of this device?

Calculate the threshold electric field (E_{Th}) needed for ionisation in the avalanche region. The ionisation coefficients α and β for electrons and holes, respectively, in silicon are measured as a function of the field, E, to be:

$$\alpha(E) \approx \beta(E) \approx A.e^{-\frac{B}{E_{Th}}}$$

where A and B are measured to be 3.8×10^7 and 3×10^8 respectively.

What is the device breakdown voltage resulting from this value of E_{Th} ?

A similar structure could be used for form an avalanche photodiode. Explain briefly the function of such a device. **(6)**

USEFUL INFORMATION

Fundamental constants

Electronic charge, $q = 1.6\times10^{-19}$ C

Permittivity of free space, $\varepsilon_o = 8.85\times10^{-12}$ Fm^{-1}

Planck constant, $h = 6.63\times10^{-34}$ Js. Reduced Planck constant, $\hbar = 1.055\times10^{-34}$ Js

Boltzmann Constant, $k = 1.38x10^{-23}m^2{\cdot}kg.s^{-2}K^{-1}$

Mass of electron $=9.1x10^{-31}$Kg

Materials Data

Saturation velocity, $v_{sat} = 1\times10^5$ ms^{-1} (Si), 2×10^5 ms^{-1} (GaAs)

Conduction band density of states, $N_c = 2.86\times10^{19}$ cm^{-3} (Si), 4.71×10^{17} cm^{-3} (GaAs)

Intrinsic carrier concentration of Si, $n_i=1x10^{16}m^{-3}$

Electron diffusion coefficient = $3.9x10^{-3}$ m^2.s (Si)

	Si	GaAs	Ge	$Si0_2$	$Hf0_2$
Band Gap (eV)	1.12	1.42	0.66	9.0	6.8
Relative Permittivity, ϵ_r	11.9	12.9	16.2	3.9	25
Electron Affinity, Ψ (eV)	4.1	4.07	4.0	0.95	1.9
Density of states in the conduction band (m^{-3})	$2.8x10^{25}$	$4.4x10^{24}$	$1.05x10^{25}$	-	-
Electron Mobility ($m^2.V^{-1}s^{-1}$)	0.15	0.85	0.39	-	-
Hole Mobility ($m^2.V^{-1}s^{-1}$)	0.045	0.04	0.19	-	-
Electron Effective mass, m* (m_o)	0.26	0.068	0.12	0.55	0.11
Hole Effective mass, m* (m_o)	0.49	0.45	0.28	-	-

Useful Formulae (all symbols have their usual meaning)

NB: Not all the equations needed are presented here. You WILL have to remember or derive some basic formulae.

MESFET

$$\boldsymbol{I_D(sat) = \frac{Za}{\rho L} V_P \left[\frac{V_d}{V_p} + \frac{2}{3}\left(\frac{V_g}{V_p}\right)^{3/2} - \frac{2}{3}\right]}$$

$$\boldsymbol{V_p = \frac{qa^2 N_D}{2\varepsilon_0 \varepsilon_r}}$$

$$V_n = \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right)$$

$$v_T = \phi_{bar} - V_n - V_p$$

MOSFET

$$\boldsymbol{g_m = \frac{Z\mu C_{ox}}{L}[V_{GS} - V_T]}$$

$$\boldsymbol{I_D = \frac{Z\mu C_{ox}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]}$$

$$\boldsymbol{V_T = -|V_{FB}| + 2|V_B| + V_{Ox}}$$

$$V_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$V_{ox} = \frac{\sqrt{2q\varepsilon_r\varepsilon_0 N_A|2V_B|}}{C_{Ox}}$$

$$|V_A| = \frac{qA_C N_B w_b}{C_{BC}}$$

$$w_{dep} = \sqrt{\frac{\varepsilon_o\varepsilon_r . 2V_B}{qN_A}}$$

$$I_{Dsat} = \frac{Z\mu\varepsilon_0\varepsilon_r}{2aL}(V_G - V_T)^2$$

BIPOLAR

$$D_e = \frac{\mu_e kT}{q}$$

QUANTUM

Infinite well model $E_n = \frac{\hbar^2}{2m}\left(\frac{\pi N}{d}\right)^2$