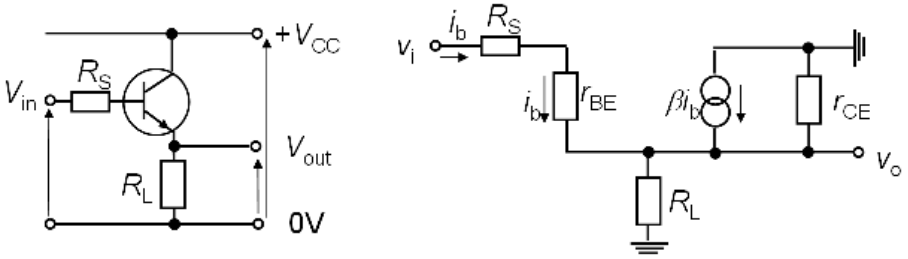
EEE331/EEE6037 exam 2013: exam questions and model solutions

1. single BJT circuits

a. Draw the small-signal equivalent circuit for an emitter follower with load resistor R_L and signal resistor R_S. Derive an expression for the voltage gain v_o/v_i, taking into account the resistance of the base-emitter junction, r_{BE}, and the resistance of the collector-emitter junction, r_{CE}. Under what conditions does the gain approximate to unity?

Solution:
The small-signal circuit is on the right. As r_{CE} looks like a connection to ground from a small signal point of view, this means it appears in parallel to the load resistor. The currents are also marked. i_b denotes the base current.



2 points

output voltage calculation: $v_o = (r_{CE} \parallel R_L)\ (\beta+1)\ i_b$
input voltage calculation: $v_i = (R_S+r_{BE})\ i_b + (r_{CE} \parallel R_L)(\beta+1)\ i_b$

3 points

Hence, the voltage gain: $v_o/v_i = [(\beta+1)\ (r_{CE} \parallel R_L)]/[R_S+r_{BE}+(\beta+1)(r_{CE} \parallel R_L)]$
Here the sign $\parallel$ stands for parallel connection of resistors according to Kirchoff's Law. For $R_S \rightarrow 0$ and $r_{BE} \rightarrow 0$ the expression converges to 1.

2 points

b. For the single stage amplifier shown in Figure 1, draw the small-signal equivalent circuit for low frequency operation. State the functions of resistors R_1 and R_2. Derive an expression for the small signal voltage gain, assuming $R_1 >> 1/g_m$. Show how the expression for the voltage gain can be simplified for large values of R_1 and R_2.

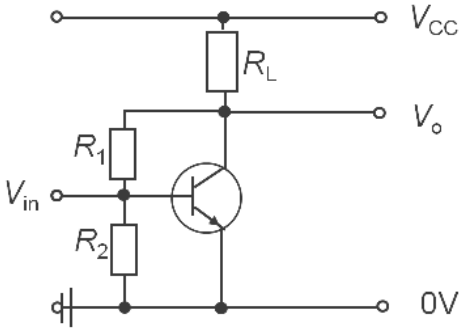
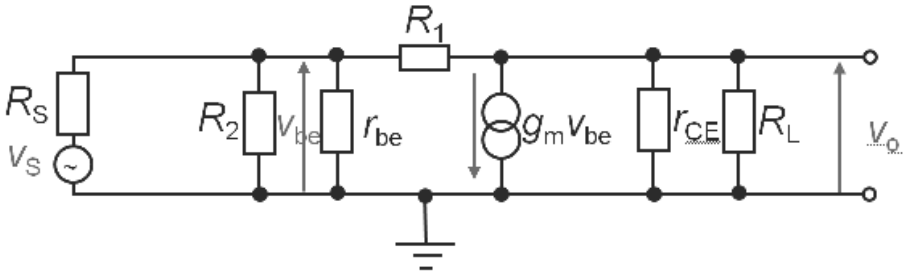


Figure 1

Solution:
The small signal equivalent circuit should look something like

2 points



2 points

where R_1 is a feedback resistor connecting input and output and R_2 a bias resistor.
Summing all currents at the output node (top right) yields:
$v_o/(R_L||r_{CE})+g_m v_{BE}+(v_o-v_{BE})/R_1=0$
Summing all currents at the input node (bottom left) yields:
$(v_S-v_{BE})/R_S+(v_o-v_{BE})/R_1-v_{BE}/R_2-v_{BE}/r_{BE}=0$
Both equations can be solved for v_{BE} and equated:
$-v_o(1/R_L+1/r_{CE}+1/R_1)/(g_m-1/R_1)=v_{BE}=(v_S/R_S+v_o/R_1)/(1/R_1+1/R_2+1/R_S+1/r_{BE})$
This can be written as (for $g_m>>1/R_1$):

3 points

$-v_o/[g_m\,(R_1||R_L||r_{CE})]\approx v_S(R_1||R_2||R_S||r_{BE})/R_S+v_o(R_1||R_2||R_S||r_{BE})/R_1$
This yields for the voltage gain
$G=v_o/v_S=-R_1/R_S\times 1/\{1+R_1/[g_m(R_1||R_L||r_{CE})(R_1||R_2||R_S||r_{BE})]\}$
For $R_L<<R_1,r_{CE}$ and $R_S<<R_1,R_2,r_{BE}$ we get

1 point

$G\approx-R_1/R_S\times 1/\{R_1/[g_m R_L\,R_S]=-g_m R_L$,
as for a standard common emitter amplifier without bias or feedback.

c. Figure 2 shows the circuit of an unbiased single stage amplifier. Identify the type of circuit and state what amplifier class it is, giving reasons for your decisions. Draw small-signal equivalent circuits for both input and output sides when the amplifier in Figure 2 operates at high frequencies. Calculate the cut-off frequency of the amplifier in Figure 2 for a transistor with emitter capacitance and base-collector capacitance of $C_E=C_{BC}=20$pF, a transconductance of $g_m=40$mS and a low-frequency current gain of $\beta_0=200$. Take the Miller effect for the capacitance between input and output into account but neglect r_{CE}.

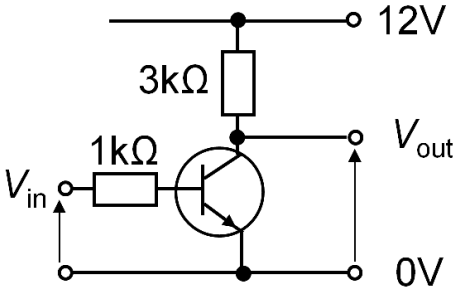
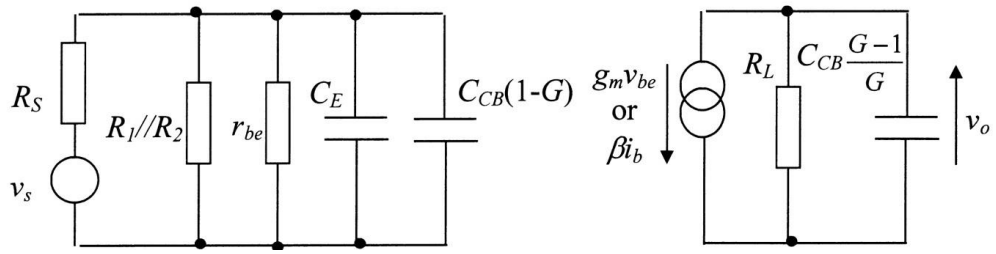


Figure 2

Solution:
The transistor is connected in common emitter mode (emitter at ground, signal at collector). The lack of a bias means it is operating as class B amplifier (only switched on some time during a voltage input cycle).

5 points

The small-signal equivalent circuit for high-frequency transfer should look like



with R_S=1kΩ, R_1=R_2=∞ (hence, negligible) and R_L=3kΩ.

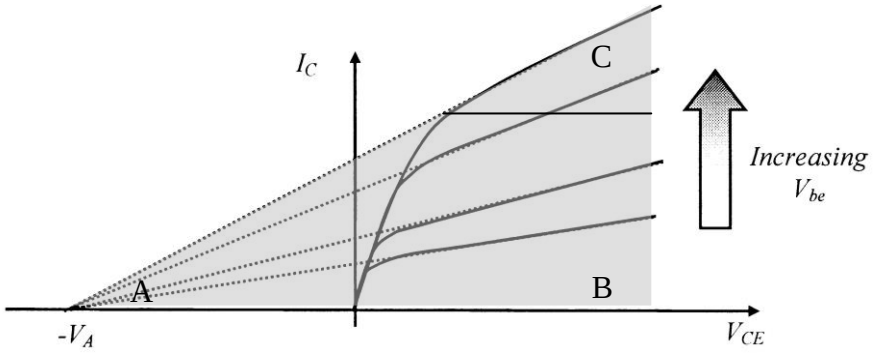
voltage gain: $G = v_o/v_i = -g_m R_L = -40\text{mS} \times 3\text{k}\Omega = -120$
capacitance increase by Miller effect: $C'_{CB} = (1-G)C_{xy} = 20\text{pF} \times 121 = 2.42\text{nF}$
(only for C_{CB} which bridges the $g_m v_{be}$ section, not C_E, as emitter is grounded)
With $r_{BE}=\beta_0/g_m=5000\Omega$ the cut-off frequency is given by the input side as
$f=\beta_0/[2\pi r_{BE} (C'_{CB}+C_E)] =g_m/\{2\pi[C_{CB}(1+g_m R_L)+C_E]\}=2.61\text{MHz}$

2. Early effect and multiple BJTs

a. Draw a set of common emitter output characteristic curves of I_C vs. V_{CE} for four significantly different values of v_{BE} and include the Early voltage V_A in your diagram. Describe the physical processes that lead to the Early effect. What would be the output resistance of a BJT without the Early effect?

6 points

Solution:



With increasing V_{BE} the effective base width is reduced. Then more carriers can transit the base per time, because of
a) reduced recombination probability and
b) increased diffusion gradient, thereby increasing collector current I_C.
In the output characteristic the result is a finite slope of the set of $I_C(V_{CE})$ curves that increases with V_{BE}. Without the Early effect the $I_C(V_{CE})$ curves would be horizontally flat in the active region, hence the output resistance (i.e. inverse of slope) would be ∞.

b. Figure 3 shows an *N*-output current mirror. Assume all transistors are matched and have finite small-signal current gain of β. Ignore the effect of finite output resistance. Calculate the ratio of the current at the collector of transistor Q_N, I_N, relative to the input current I_{ref}. Compare your result to that of a simple current mirror consisting of only two transistors Q_{ref} and Q_1 where the output is at the collector of Q_1. How many outputs (N) can the current mirror support if the individual output currents current (I_N) are to stay within 98% of the reference current (I_{ref}) and if β=200 is assumed for all transistors?

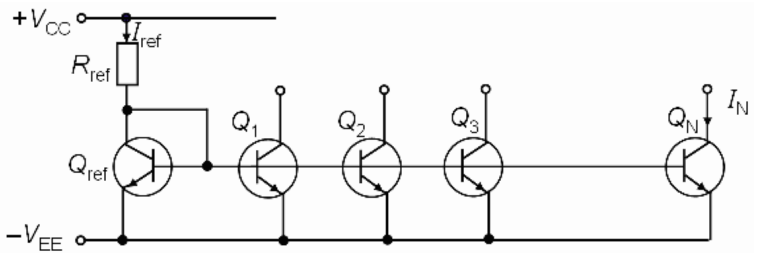


Figure 3

Solution:
At the node just below R_{ref} apply Kirchoff's Law to the sum of the currents:

5 points

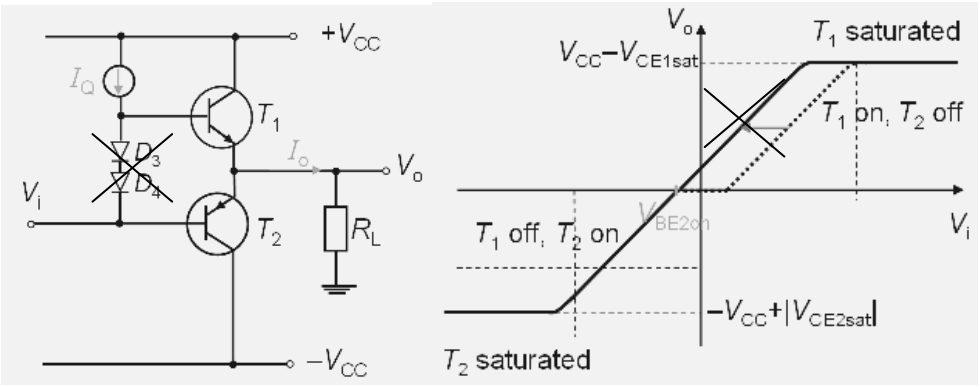
$I_{ref} = I_{C,ref}+I_{b,ref}+I_{b,1}+I_{b,2}+\ldots+I_{b,N}$

$= \beta I_b + (N+1) I_b$
$= (\beta + N + 1)\, I_b$,
because all base currents are identical (I_b) and the current gains as well (β).
At the output we just measure the collector current of transistor Q_N:
$I_o = I_{C,N} = \beta\, I_b$
The current gain thus is the ratio $I_o/I_{ref} = \beta/(\beta+N+1)$
For two transistors the circuit consists of only the reference transistor and $Q1$, hence N=1 in the above equation, which yields $I_o/I_{ref} = \beta/(\beta+2)$. This is identical to the result $1/(1+2/\beta)$ of the simple current mirror discussed in the lecture.
For $I_o/I_{ref} = \beta/(\beta+N+1)>0.98$ we get
$200/(200+N+1)>0.98$ or $N<200/0.98–201=3.08\ldots$,
i.e. a maximum of N=3 outputs can be supported.

4 points

c. Sketch the circuit for a class B push-pull amplifier configuration. Draw the voltage characteristic V_{out}/V_{in} and describe the distortion you would expect. How could the distortion be reduced by biasing to produce a class AB output stage?

Solution:



The principle of the class B output stage is an unbiased push-pull complementary pair, as shown on the left with the diodes shorted. Transistor T1 then follows the dotted line in the right diagram of the voltage characteristic. This leads to a dead band of width $2V_{BE_{on}}$, and for input signals between $-V_{BE_{on}}$ and $+V_{BE_{on}}$ there will be no output. This causes severe cross-over distortions, particularly for small signals. This is avoided in a class AB stage where T_1 is biased by $2V_{BE_{on}}$ relative to T_2 such that the dotted curve in the output characteristic shifts left as sketched and continues the straight curve from the output characteristic of T_2 without introducing any distortion of small signals.

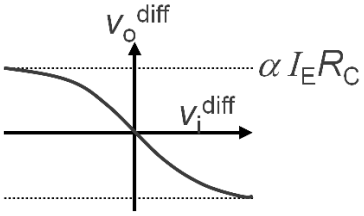
5 points

d. The output characteristic of an emitter coupled pair of BJTs can be written as

$$v_o^{diff} = \alpha\, I_E\, R_C \tanh\left[-v_i^{diff}/(2V_{to})\right].$$

Define all six parameters in this equation, sketch the curve of v_o^{diff} as function of v_i^{diff} and comment on sign, slope and range of the linear approximation.

Solution:
V_o^{diff} and v_i^{diff} are differences between output [input] voltages at the collector [base] junctions of the emitter coupled pair, a is the ratio of collector to emitter current ($\alpha = \beta/(\beta+1) \approx 1$), I_E the sum of both emitter currents, R_C the resistor between each collector and supply rail voltage, V_{to} the turn-on voltage of the BJTs.



The output characteristic of the emitter coupled pair

a) inverts the signal,
b) amplifies small signals by a factor given by the product of $\alpha I_E R_C$,
c) saturates for larger input values, where there is a trade-off between amplification factor and linear range.

3. MOSFETs

3 points

a. The square law below describes the drain current, I_D, of a MOSFET as function of gate-source voltage, V_{GS}:

$$I_D = 0.5\mu C_{ox} (W/L) (V_{GS}-V_{to})^2 (1+V_{DS}/V_A)$$

where V_{to} is a threshold voltage, V_{DS} the drain-source voltage and V_A the Early voltage. μ, C_{ox}, W and L are device parameters. Derive an expression for the mutual conductance g_m in the active region. State how drain current and over-voltage influence the mutual conductance.

Solution:
mutual conductance:
$g_m=\partial I_D/\partial V_{GS}=\mu C_{ox} W/L (V_{GS}-V_{to}) (1+V_{DS}/V_A)=2I_D/(V_{GS}-V_{to})=2I_D/V_{ov}$
To maximise the mutual conductance and thus the voltage gain in common source configuration, a MOSFET should be operated with a drain current and a small over-voltage, i.e. by a gate-source voltage just above the turn-on voltage.

6 points

b. Figure 4 shows a MOSFET circuit called centroid layout. Draw the circuit diagram corresponding to the figure, explain how the transistors are interconnected and describe the function of the circuit. What are the advantages and disadvantages of this layout compared to a simple layout using only two transistors?

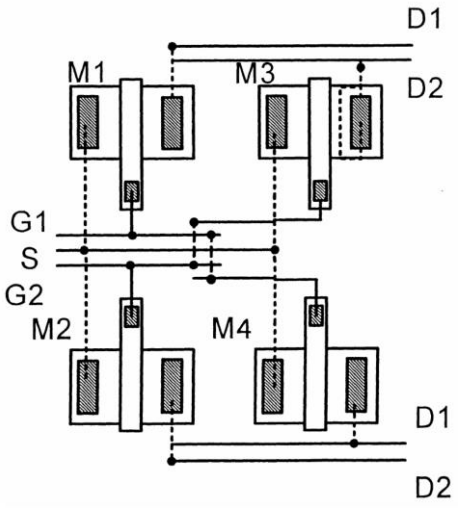
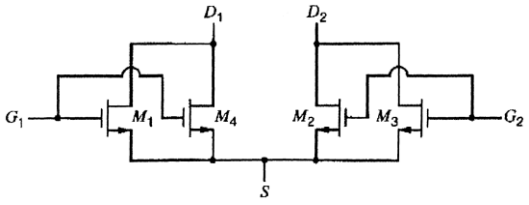


Figure 4

Solution:



Transistors M1 and M4 are connected in parallel and do exactly the same, and the same is true for M2 and M3. The circuit is a differential amplifier, as can be seen from the source electrodes connected to a common source and the differential signals being fed into opposite base electrodes. For such differential amplifiers it is important to minimise any mismatch between the two signal paths. Failure to do

this would yield non-zero offsets, thereby increasing the common-mode signal and decreasing the common mode rejection ratio (CMRR).
Replacing single transistors by pairs of transistors at opposite positions on the substrate automatically eliminates linear process gradients, such as variations of gate oxide thickness, that can be decomposed into x- and y-components. The result is a higher CMRR and lower temperature dependence of the performance. The disadvantage is the longer connection lines needed for cross-connection.

c. Describe the function of each transistor (Q_1, Q_2 and Q_3) in the circuit shown in Figure 5. Explain the advantage of combining BJTs with a MOSFET in this circuit.

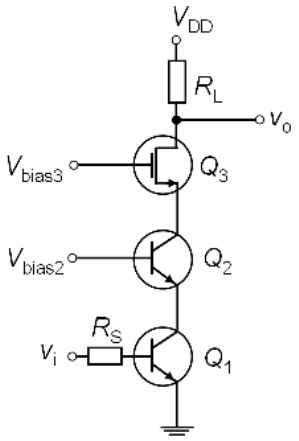


Figure 5

4 points

Solution:
This circuit is a second-level BICMOS cascode. BJT Q_1 provides a high transconductance and thereby translates the small input voltage into a large current I_C, BJT Q_2 ensures that the common emitter stage of Q_1 sees only a resistive load of $r_{BE2}<<R_L$, thereby reducing gain and Miller effect, and MOSFET Q_3 enhances the finite output resistance of the circuit by a factor A_{o3}. R_L then translates the current I_C back into a voltage signal $V_o=V_{DD}-I_C R_L$.

7 points

d. Transistor T_1 in the emitter follower of Figure 6 is biased by a quiescent current I_Q supplied by transistor T_2. What class of amplifier output stage is this? For a sinusoidal input voltage V_i, sketch the waveforms for the full range of output voltage, output current and instantaneous power as a function of time. You may neglect $V_{CE,sat}$. Derive an expression for the power conversion efficiency of this output stage amplifier.

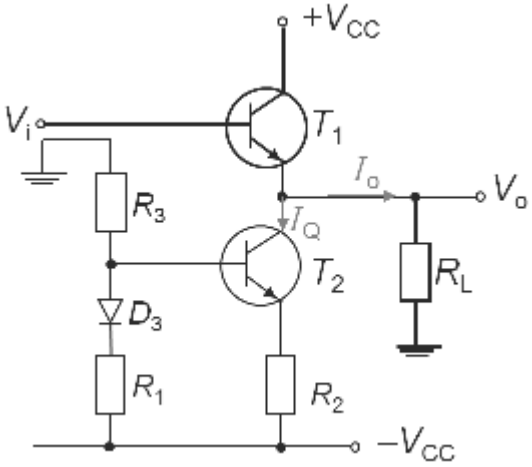
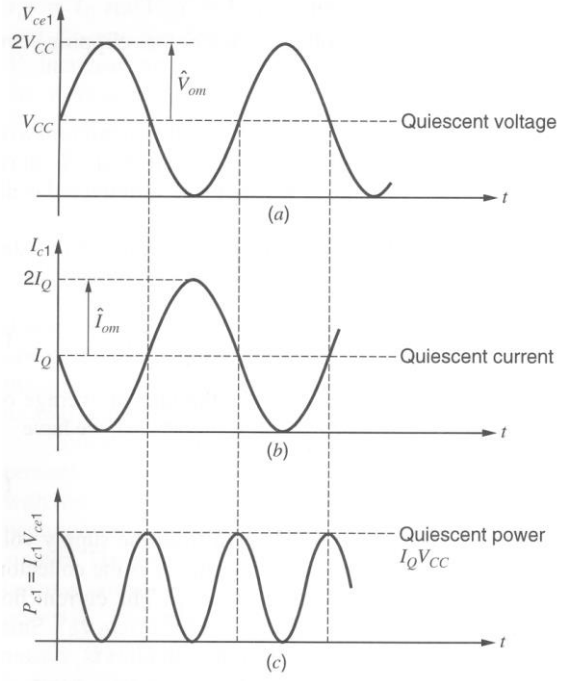


Figure 6

Solution:

Because of the biasing by a constant current source this is a class A amplifier. For the output signals we get $V_{CE1}=V_{CC}(1+\sin \omega t)$ and $I_{C1}=I_Q(1-\sin \omega t)$, which yields for the instantaneous power dissipation:

$P_{C1}=V_{CE1}I_{C1}=V_{CC}I_Q \cos^2 \omega t = ½\ V_{CC}\ I_Q\ (1+\cos 2\omega t)$



Average output power delivered to load:

$P_L=\langle V_o\rangle\langle I_o\rangle=½V_o^{max}\ I_o^{max}$ with

$V_o^{max}=V_{CC}-V_{CEsat}$

$I_o^{max}=V_o^{max}/R_L=I_Q$, hence

$P_L^{max}=½\ (V_{CC}-V_{CEsat})\ I_Q$

On the other side, the power drawn from the supply is

$P_{sup}=V_{CC}(I_o+I_Q)$ where $\langle I_o\rangle=I_Q$, hence $\langle P_{sup}\rangle=2V_{CC}\ I_Q$

The ratio is the power conversion efficiency:

$\eta= P_L^{max}/\langle P_{sup}\rangle=¼\ (1-V_{CEsat}/V_{CC}) \leq 25\%$

4. Filters

6 points

a. State what class of filter is shown in Figure 7. Using qualitative arguments, describe the frequency behaviour of the filter. Draw the leap-frog structure diagram of the filter, deriving equations for the voltages and currents of all components in your leap-frog diagram.

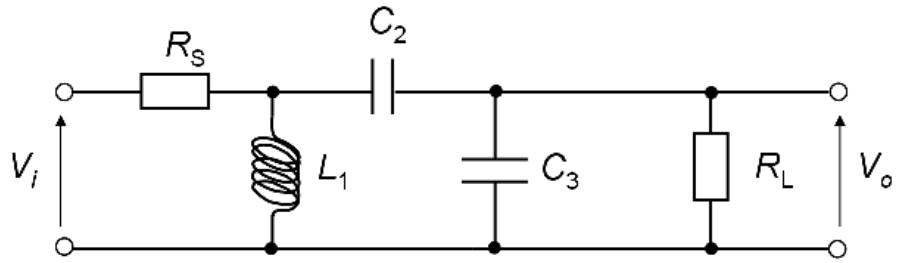
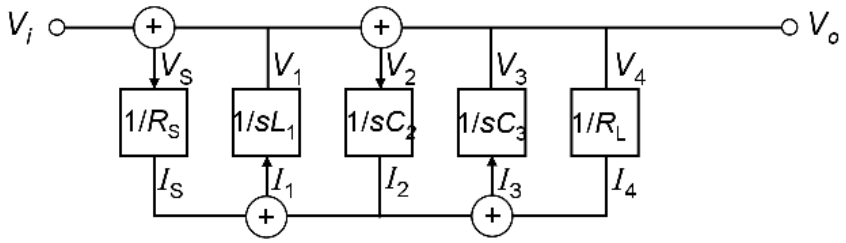


Figure 7

Solution:
The filter is a 3rd order LC band-pass filter. Its acts as band-pass because C_2 effectively blocks DC signals which L_1 then shortens to ground, while C_3 shortens high-frequency signals to ground. In both cases V_o=0. The leap-frog structure would look like the following:



With input and output resistors there are 5 components. For each of them we can write down two equations, one from Ohm's Law and one from Kirchhoff's Law. Hence, there are 10 equations to describe the interdependence of 4 voltages V_S and $V_{1\text{-}3}$ (V_i and ω are given, V_o=V_4=V_3) and six currents I_S, $I_{1\text{-}4}$ and I_L. So it is possible to calculate the output voltage V_o for any given set of V_i and ω.

(i) $V_S=I_S R_S$; $V_S=V_i-V_1$
(ii) $V_1=I_1 sL_1$; $I_1=I_S-I_2$
(iii) $V_2=I_2/(sC_2)$; $V_2=V_1-V_3$
(iv) $V_3=I_3/(sC_3)$; $I_3=I_2-I_4$
(v) $V_4=I_L R_L$; $I_L=I_4$

5 points

b. Determine the transfer function of the circuit shown in Figure 8. Write down expressions for its zeros and poles. What classification of filter is it? Compare the pole frequency to the time constant of the RC network.

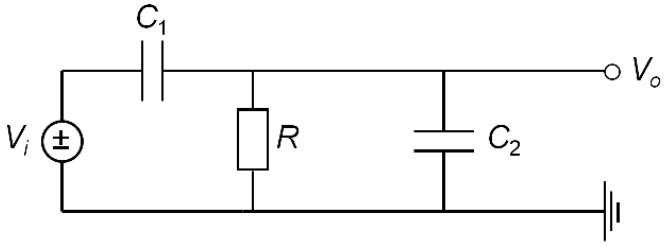


Figure 8

Solution:
The transf function is defined as the ratio of output to input voltage, i.e. $T(s) = V_o(s)/V_i(s)$
With complex impedances Z and admittances $Y=1/Z$ we get for current I:
$T(s) = Z_o(s)\, I / [Z_i(s)\, I] = Y_i(s)/\, Y_o(s)$
The admittance for short circuited output is simply: $Y_i = sC_1$, as both C_2 and R appear short circuited.
The admittance for short circuited input is: $Y_o = sC_1+sC_2+1/R$, as all components appear in parallel connection.
Thus we get:
$T(s) = sC_1 /[sC_1+sC_2+1/R] = sRC_1 / [1+sR(C_1+C_2)]$
This function is a first-order network. It acts as band-pass filter with a zero for $s=0$ and converges to $\lim_{s\to\infty} T(s)=C_1/(C_1+C_2)$. It has one pole $-\omega_0$ at the pole frequency $\omega_0 = 1/[R(C_1+C_2)]$. This is the inverse of the time constant $\tau = RC_{eff}$ for two capacitors C_1 and C_2 in parallel connection ($C_{eff}=C_1+C_2$).

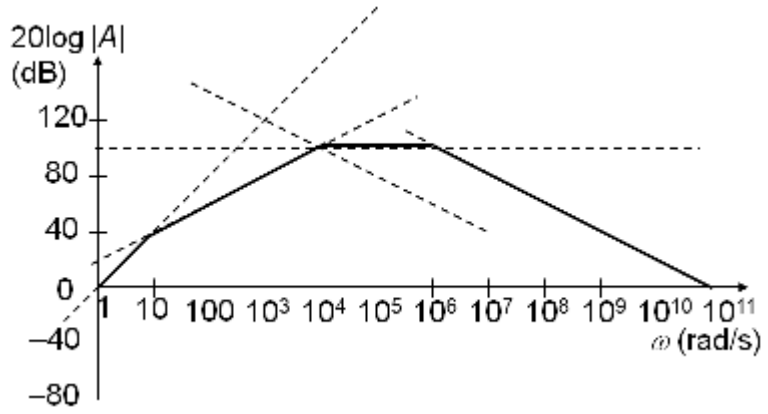
6 points

c. For the transfer function below write down the location of the poles and zeros and sketch the magnitude of the Bode plot:

$$T(s) = \frac{10s^2}{(1+s/10^1)\ (1+s/10^4)\ (1+s/10^6)}$$

Name the order and the classification of filter. What is the transition frequency of unity gain?

Solution:
zeros: $s=0$ and $s=\infty$
poles: $s=-10^1$, $s=-10^4$ and $s=-10^6$
The Bode plot can be obtained from the multiplicative superposition of four curves for
(i) $T(s)=10s^2$, which is a straight line through (1rad/s, 0db) of slope +40dB/decade.
(ii) $T(s)=1/(1+s/10^1)$ gives two asymptotes intersecting at $\omega=10^1$.
(iii)$T(s)=1/(1+s/10^4)$ gives two asymptotes intersecting at $\omega=10^4$.
(iii)$T(s)=1/(1+s/10^6)$ gives two asymptotes intersecting at $\omega=10^6$.
This is a 3rd order band-pass filter. The transition frequency is $f_t=\omega_t/(2\pi)$=15.9GHz.



3 points

d. Explain the principle stages within a typical three-stage operational amplifier. Name all three basic stages, explain their function and briefly discuss possible methods of implementation.

Solution:
A typical 3-stage operational amplifier consists of

i) a differential input stage for high differential gain and good CMRR
ii) an intermediate stage with high voltage gain, either as differential pair or emitter (source) follower cascode
iii) an output stage in push-pull configuration with low output impedance and high output current (high current gain)