Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2009-2010 (2 hours)

Advanced Computer Architectures 4

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. A processing pipeline consists of 4 functional blocks, *A*, *B*, *C*, and *D* (implementing functions $f_A(\bullet)\ldots f_D(\bullet)$) that appear, schematically, as shown in **Figure 1**.

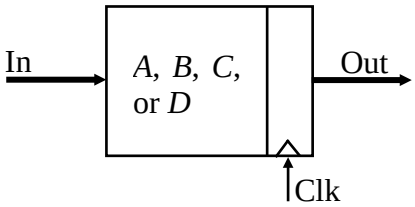

Figure 1: Functional Block

A sequence of data, *x*, is passed through the pipeline producing an output *y* such that $y_i = f_D(f_C(f_B(f_D(f_B(f_A(x_i))))))$.

a. Draw a schematic diagram for the processing pipeline (you will need to use 2:1 multiplexers as well as *only* one instance of each functional block). **(6)**

b. For the sequence of operations above:

i) Draw the reservation table. **(4)**

ii) What is the throughput of the processing pipeline (in datum/clock cycle)? **(2)**

iii) What is the latency of the processing pipeline (in clock cycles)? **(2)**

c. You recognise that adding a single register can improve the throughput of the processing pipeline.

i) Show how your schematic can be modified, in this way, to improve the throughput. **(3)**

ii) Draw the reservation table for the revised schematic. **(2)**

iii) What is the improved throughput of the processing pipeline (in datum/clock cycle)? **(1)**

2. a. i) Draw a schematic diagram for the Processing Element (PE) of a typical SIMD array processor. **(4)**

ii) Comment on the organisation of the local storage that the PE accesses (i.e. single/dual port memory, registers) and the effect that this organisation can have on performance. **(4)**

b. An *n*x*n* SIMD processor supports a flag, *F*, that allows conditional execution of instructions across the array and supports the following set of instructions:

```
IN x   a      ; copies the data from the x (=N,S,E,W) input into address a
BCAST  a      ; broadcast the data from address a to the N,S,E, and W outputs
CMP    a, #N  ; compares the data in address a with the constant N and sets
              ; the flag, F, to 1 if they are equal, 0 otherwise
INCC   a      ; increment the data in address a but only if F=1
CLR    a      ; clear the data in address a
ADD    a,b    ; add the data in address a to the data in address b
MOVE   a,b    ; copy the data in address a to the data in address b
```

An *n*x*n* image, *f*, is mapped onto the array such that *f*(*x*,*y*) is in memory location 0 of PE_{xy}. The image contains only 0s and 1s. Write a program that will detect the occurrence of patterns in the image as shown in **Figure 2**:

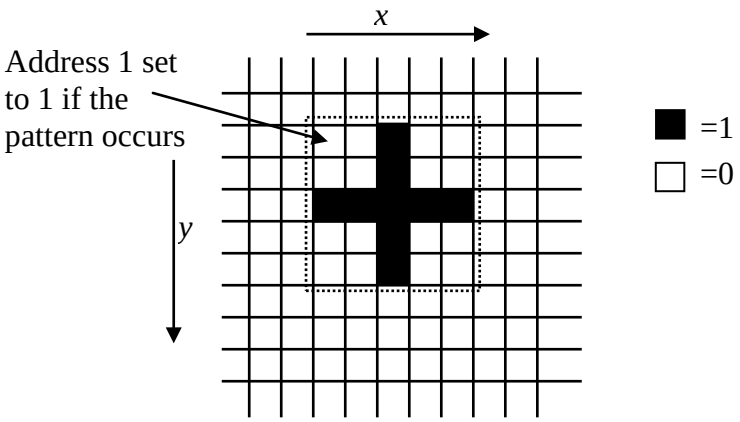

Figure 2: Pattern in Image

such that, if the exact pattern, as shown within the dotted square in **Figure 2** occurs in the image, *f*, then the data in address 1 of the PE at the top left hand corner of the dotted square will be set to 1 otherwise it will be set to 0. Clearly, the pattern could occur anywhere in the *n*x*n* image and the program should detect all instances (ignoring boundary effects).

Hint: what does the pattern look like if you add up the data along each row and along each column? **(12)**

3. **a.** State Flynn's Taxonomy and give an example for each part of the taxonomy. **(4)**

b. Amdahl's Rule is:

$$speedup = \frac{1}{1-\alpha+\frac{\alpha}{N}}$$

i) Explain what this means, identifying the meaning of the terms. **(2)**

ii) Show how Amdahl's Rule can be extended to deal with situations where the use of parallelism is more complicated. **(2)**

c. A processor farm consists of N+1 identical processors networked together. One of the processors (the master) receives blocks of data from outside the system, each of which must be processed equivalently. The processor takes an incoming block of data, once it has been input, and splits it between the N processors (workers) actually doing the work. When a worker processor has finished processing its part of the data block, it sends the result to a master processor that is responsible for assembling and outputting the results before getting the next input block.

Tests show that the time taken to:

- Receive a block of data at the input is 100μs
- Distribute a part of the block of data to or from a worker takes negligible time
- Process one part of the block of data in a worker is 1500/Nμs
- Output a result for each block is 30μs

Restate this problem as in Amdahl's Rule, stating any assumptions that you make. **(4)**

Estimate the best value for N if:

i) 6000 blocks per second have to be processed **(2)**

ii) *cost/benefit* is the metric used. **(2)**

How might you change the system's architecture to improve performance? **(4)**

4. **a.** Describe the organisation of typical memory hierarchy for a leading-edge desk-top processor system giving the general characteristics of each part of the hierarchy. **(4)**

b. **i)** What are the problems/issues involved in constructing a mapping scheme to map virtual to physical memory addresses? **(5)**

ii) Describe a practical mapping scheme to help overcome these problems. **(3)**

c. Increasingly, leading-edge systems consist of multiple processing *cores* that share a common memory system. Describe the problems that this gives rise to and how these problems can be resolved (your answer should cover coherency, contention, and bandwidth). **(8)**

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