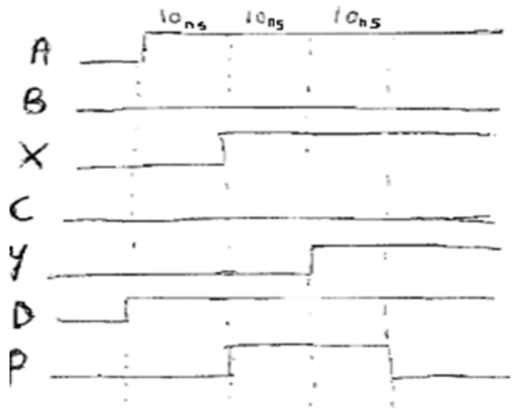
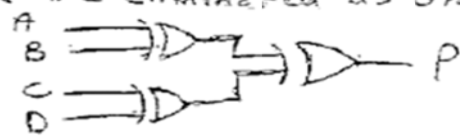
1.

XOR gates give 'odd' function. Output is '1' when there is an odd number of '1's on ABCD. ∴ the output will indicate odd parity. Maximum delay = $10+10+10 = 30ns$ $f_{max} = \frac{1}{30ns} = 33.3MHz$



P should remain at '0' as '0000' and '1001' are both even parity. It is seen that there is a static-'0' hazard on the output. It can be eliminated as shown.



Delays are now equal.

2.

(a) See lecture notes } bookwork

(b) see lecture notes

(c) $S_o = (A \oplus B) \oplus C_i$

$C_o = AB + C_i(A+B)$

when $B = \phi$, $S_o = A \oplus C_i$

$C_o = C_i A$

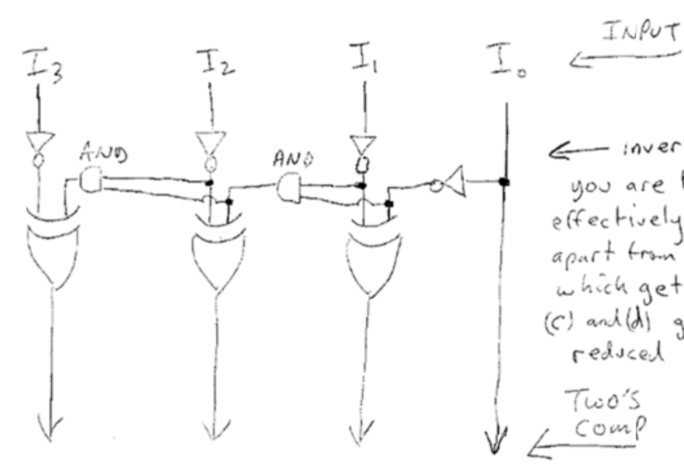
(d) $B=1$, $C_i=0$

$S_o = \bar{A}$, $C_o = A$

$(A \oplus 0 = A, A \oplus 1 = \bar{A})$

(e) invert all bits and add 1

(f)



invert all bits. you are then effectively adding '0' apart from the LSB which gets '1'. Par (c) and (d) give the reduced adder circuit.

3. In a Moore type machine, the outputs depend on only the present state. They may be the state itself or decoded from the state. In a Mealy type machine, the outputs are a function of the state and current inputs.

4. In binary encoding, *n* bits can be used to represent 2^n states. In one-hot encoding, one bit is required for each state. When in a certain state, one bit is active or *hot*. This could be the output of a flip-flop where *n* flip-flops would be required to represent *n* states.

5.

$\frac{1}{50ns} = 20 MHZ$ Use the 80MHZ signal to clock a 2 bit counter. Q_1 will be at 20MHZ