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The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2007-2008 (3 hours)

Semiconducting Materials: Preparation to Device Processing 6

Answer **THREE** questions from **SECTION A** and **TWO** questions from **SECTION B**. **No marks will be awarded for solutions to additional questions in either section.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

SECTION A: Answer **THREE** questions out of **FOUR**

1. a. Provide a list of the seven crystal systems. **(3)**

b Explain how the Miller index of a lattice plane in crystalline Si is defined. **(2)**

c. A semiconductor with the diamond cubic structure has a lattice parameter of $a_0 = 0.5522$nm. Calculate the spacings of the following planes: (110), (111), (113) and (422). Give values in nanometres to four decimal places accuracy. **(4)**

d. For a diamond cubic crystal, deduce which of the following pairs of planes are perpendicular to one another: (113) and $(12\bar{1})$

(114) and $(1\bar{1}0)$

(114) and $(0\bar{1}0)$ **(3)**

e. By use of a band diagram, explain the difference between donor and acceptor impurities in Si. **(4)**

f. Using a simple lattice diagram of an edge dislocation, explain quantitatively what is meant by the term 'Burgers vector'. In the diamond cubic lattice, what are the Burgers vectors of a perfect dislocation, a Frank partial dislocation and a Shockley partial dislocation. **(4)**

2. a. Describe the overall features of the Metal-Organic Chemical Vapour Deposition (MOCVD) technique used for epitaxial semiconductor layer growth. Include an outline of the local processes that control deposition upon the substrate surface. What precursors are typically used in the growth of III-V compound semiconductors, upon what basis are the precursors chosen and how is p- and n-type doping carried out? **(12)**

b. What is a heteroepitaxial pseudomorphic layer? Give diagrams of two such layers with built-in strain opposite to one another. How and under what conditions does such a pseudomorphic layer relax: consider separately the low misfit and high misfit regimes? **(8)**

3. **a.** Ion implantation is the key process used for introducing dopants into Si ICs: state the reasons why this is so. Describe the implantation equipment used for the process on a fabrication line. Also describe, in general terms, the way implanted ions travel through the Si semiconductor lattice and lose energy along the way. Outline the phenomenon of ion channelling: state whether this is a wanted or unwanted process during ion implantation for IC fabrication and clearly explain your answer. **(10)**

b. Describe the difference in Si disorder produced by the implantation of either low- to moderate- doses of light ions (eg B^+ ions) or high doses of heavy ions (eg Sb^+ ions). During IC processing, ion implanted layers require annealing treatment. Explain why this is so: what differences would be expected after rapid thermal annealing of the two different types of initial layer disorder referred to above. **(5)**

c. An (001) Si wafer is implanted with Ge^+ ions to produce a surface amorphous layer which is 1.5×10^{-5} cm in thickness. After subsequent implantation with a low dose of boron ions, the amorphous layer is recrystallised epitaxially at 650°C Calculate how long the epitaxial regrowth of this layer will take. (The activation energy for the regrowth process is 2.76eV, the pre-exponential factor (v_0) is 3.68×10^8 cm/s and Boltzmann's constant (k) is 8.617×10^{-5} eV/K). **(5)**

4. **a.** Outline briefly the main operating advantages and disadvantages of circuits produced using CMOS IC technology on the one hand and bipolar IC technology on the other **(3)**

b. With the assumption that a p-type substrate wafer is used, describe with the aid of diagrams the **basic** sequence of processing steps that can be employed to fabricate CMOS circuits with adjacent p- and n-channel MOS devices. **(11)**

c. A stage in the fabrication of a particular transistor requires the formation of an n-type tub in an initial p-type wafer. An implant of As^+ is first carried out using 12 keV ions to give a shallow As-containing layer. The impurity is then driven in by a 30min anneal at 1150°C. Calculate the characteristic diffusion length of the impurity as a result of this anneal. The diffusion pre-exponential factor (D_0) may be taken to be $12 cm^2/sec$, with an activation energy for diffusion of 4.05eV: Boltzmann's constant (k) is 8.61×10^{-5}eV/K. **(6)**

SECTION B: Answer **TWO** questions out of **THREE**

5. Scanning Probe Microscopy (SPM) allows the highly detailed study of surfaces. Give a detailed description of the fundamantal and practical aspects of the following two SPM techniques, giving examples of the areas of semiconductor application.

a. Atomic Force Microscopy **(10)**

b. Scanning Tunnelling Microscopy **(10)**

6. a. The scanning electron microscope (SEM) is widely used by IC manufacturers for assessing processed semiconducting materials. Describe, with the aid of a suitable diagram, the complete general structure and basic functions of the SEM. **(8)**

b. Describe the five major imaging modes of the SEM, including consideration of any special instrumentation required and the types of information that are produced. **(12)**

7. a. Outline the way in which Secondary Ion Mass Spectrometry can be used for the depth profiling of impurities in semiconductors. Give the principle of the technique, describe using diagrams the main types of spectrometer, discuss the factors that govern the choice of the incident ions and indicate what limits the depth resolution achieved. **(12)**

b. Describe in detail the two main techniques employed in IC production to etch dielectric films. Explain with the aid of diagrams the advantages and disadvantages of the two techniques. **(8)**

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