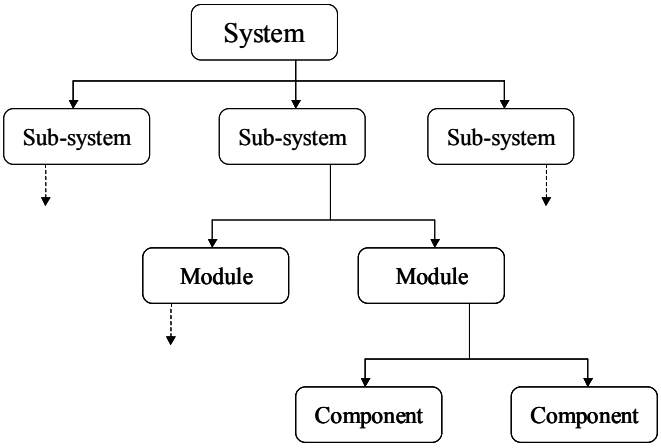
Answers to EEE115 examination Spring 2006

Question 1

a.



System

System or system specification is the top-level of our hierarchy. At this level the system is described only in a terms of its external behaviour. Details about the internal behaviour of the system are left to the subsequent levels.

Sub-system

Sub-systems represent divisions in the functionality/requirements of the overall system. Often, sub-system definitions directly relate to the system specification statements.

Modules

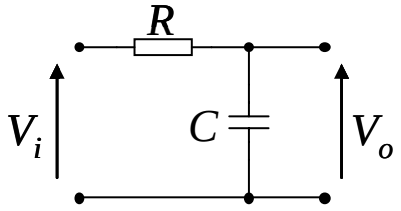
Modules are high-level functional blocks required to construct a sub-system.

Component

Components are the lowest level building blocks for the system. Electronic components and programming language functions fall into this category.

b.

Abstraction is the process of filtering out certain details about a system (sub-system or element) to obtain a more generic description of the system's behaviour. This means an engineer can benefit by transferring knowledge gained in analysing one system to other similar systems even though their final usage may be completely different.



$$\frac{V_o}{V_i} = \frac{1/j\omega C}{R + 1/j\omega C} = \frac{1}{1 + j\omega CR}$$

Identifying the corner frequency $\omega_c = \frac{1}{CR}$ one can develop the normalised response,

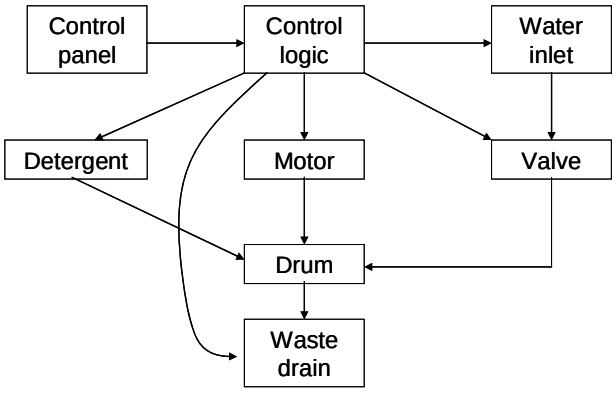
$$\frac{V_o}{V_i} = \frac{1}{1 + j\omega/\omega_c}$$

We now have a generic expression for a low-pass filter in terms of a corner frequency. No information about its implementation is given thus it is suitable for analysis independently.

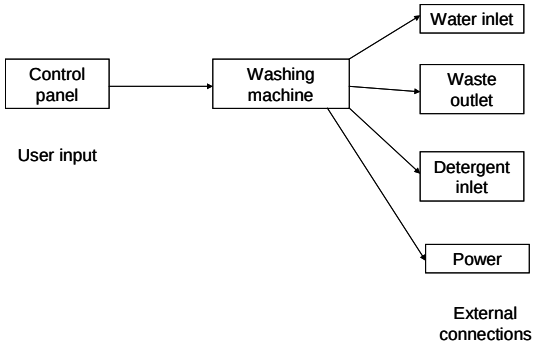
c.

i)
Components of a washing machine:
Drum, Motor, Control panel, water inlet connection and valve, detergent container, waste outlet and valve, controller.

ii)
As a designer I would partition according to control tasks



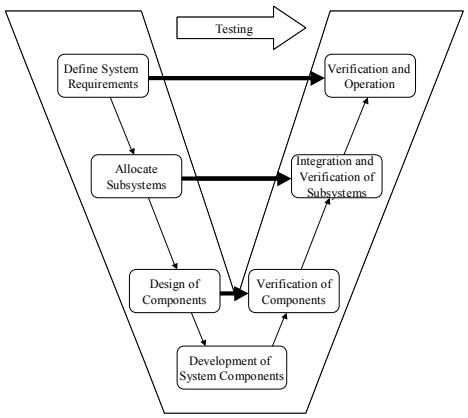
iii)
As user guide writer I would partition according to function and input output connections.



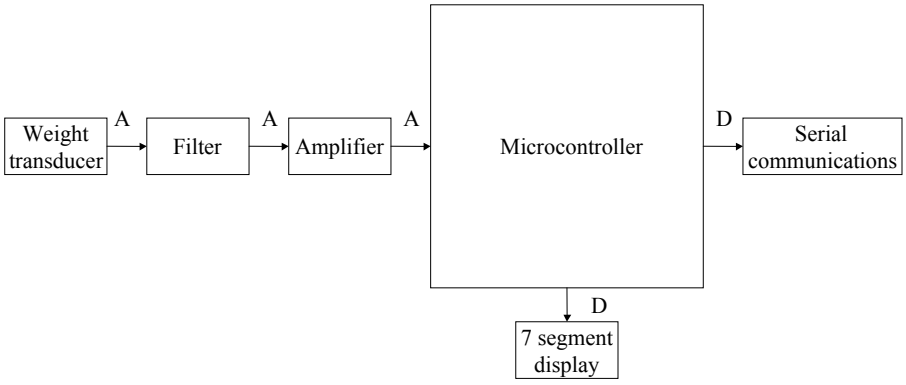
d.
Here, the design process is modelled as two distinctive sections, a "Decomposition and Definition Sequence" and "Integration and Verification Sequence", related together through testing.

Decomposition and Definition Sequence
- The system requirements are set down and analysed.
- Subsystems and functions are defined.
- Low-level component and subsystems are designed.

Integration and Verification Sequence
- Functionality of the low-level components verified.
- Verification of higher-level sub-systems.
- Verification of full system and deployment.



Question 2
a.

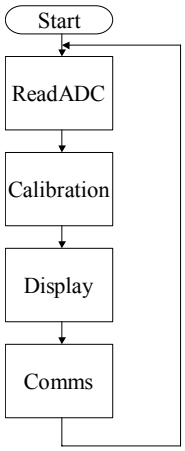


A- analogue
D – digital

b. Functions microcontroller needs to perform

1. Read ADC
2. Perform calibration/measurement correction
3. Send weight to display

4. Send weight via series communications



c. Maximum transducer output is 20mV.
Maximum voltage required by ADC is 2.5V

There gain required is 2.5/0.02=125

Circuit should be a non-inverting amplifier.

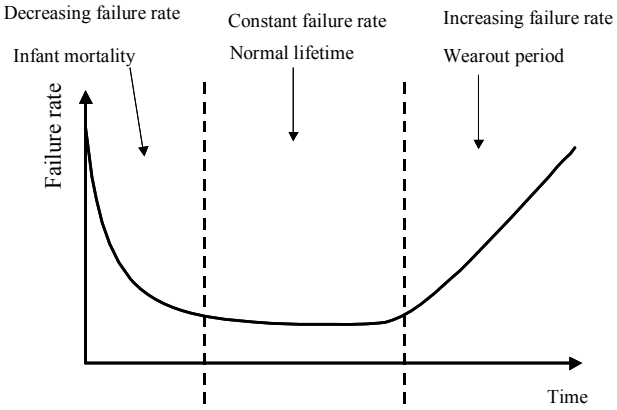
d.

- ADC is 14-bits provides a maximum output of 16383 taking zero into account.
- $2FFF_{hex}$ is 12287.
- Ratio of ADC value to maximum ADC is 12287/16384=0.75
- Therefore transducer voltage is 0.75×20mV=15mV.
- The weight required to produce this voltage is 15×10=150kg.

e. Because the unit is being subjected to high-frequency noise the input signal must be low-pass filtered before it is converted into digital. By correct choice of low-pass filter the high-frequency noise can be attenuated to such a level that it does not pose a problem due to aliasing. The signal could also be digitally filtered but it must be filtered in analogue first to ensure aliasing does not occur.

Question 3

a.



When systems are manufactured and released on sale they often exhibit a failure rate distribution similar in shape to the bath tub curve. The bath tub curve is divided into 3 sections:

1) Infant mortality – when a system/product is first built a number of these often fail. This can be due to defective components or problems that have arisen during manufacturing. When releasing a product one must ensure that one's customers do not buy products that suffer a high mortality rate.
2) Normal lifetime – this is where the product failure rate has reached a constant level. This is the normal operating time of a product.
3) Wearout period – as the product ages components being to wear, placing an excessive burden on other parts of the system. Eventually a component will fail, possibly resulting in complete product failure.

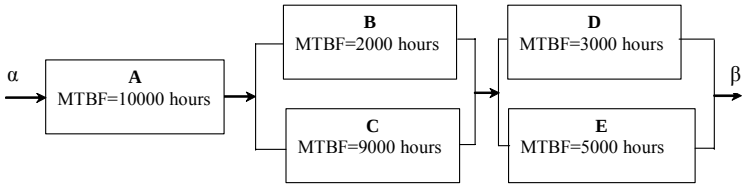
b.

Mean-time-between-failure is the average time it takes a system to fail. It is defined mathematically as:

$$MTBF = \frac{\text{No. of operating hours}}{\text{No. of failures}}$$

MTBF is only valid for a constant failure rate (i.e. the normal lifetime portion of the bath tub curve).

c. Reliability for 1500 hours of operation.



$$R(t) = e^{-\frac{t}{M}} = e^{-\lambda t}$$

R_A=0.8607, R_B=0.4724, R_C=0.8465, R_D=0.6065, R_E=0.7408

R_{p1} is the parallel branch B and C, R_{p2} is E and E

$R_{p1}=R_B+R_C- R_B\times R_C=0.4724+0.8465-0.4724\times0.8465=0.9190$
$R_{p2}=R_D+R_E- R_D\times R_E=0.6065+0.7408-0.6065\times0.7408=0.8980$

$R_{tot}=R_A\times R_{p1}\times R_{p2}=0.8607\times0.9190\times0.8980=0.7103$

d.

Reliability if MTBF of A is now 12000 hours, an additional sub-system system, called F, is placed in parallel with system E with a MTBF of 6000 hours and a further sub-system, called G, with a MTBF of 8000 hours is connected between the points α and β?

R_A= 0.8825, R_F= 0.7788, R_G=0.8290

Now $R_{p3}=1-(1-R_D)(1-R_E)(1- R_F)=1-(1-0.6065)(1-0.7408)(1-0.7788)=0.9774$

$R_{tot1}=R_A\times R_{p1}\times R_{p3}=0.8825\times0.9190\times0.9774=0.7927$
Finally,
$R_{tot}=1-(1-R_{tot1})(1-R_G)=0.9646$

e.
Component de-rating

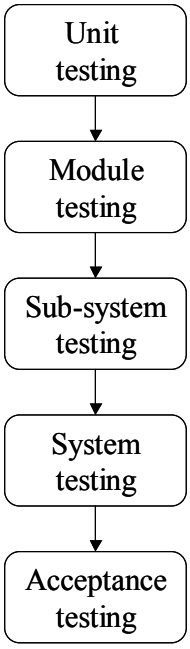
Component manufacturers provide the designer with all manner of design data relating to their components. For example, a transistor datasheet provides information above maximum current, voltage and power dissipation rating. If these ratings are exceeded during operation then it is more likely that the component will fail. It has been shown experimentally that a component's lifetime is reduced the closer it operates to its maximum ratings. The reason for this is that many failure mechanisms have a failure rate proportional to Arrhenius equation, $e^{-\frac{Ea}{kT}}$, that is used to describe many processes that occur is chemistry and physics. The Arrhenius equation states that a reaction rate is proportional to an activation energy *Ea*, some physical constant *k* (such as Boltzmann's constant = $8.62\text{x}10^{-5}\text{eVK}^{-1}$) and absolute temperature *T*.

Designers can take advantage of this phenomenon and de-rate their components to achieve greater reliability. They do this by operating component at lower voltage, current and temperature levels.

Question 4

a.

To ensure that every aspect of the design has been tested in some way the V.V.T. phase must be related to the structure/hierarchy of the implementation phase. Systems are designed from the top-down (from a concept to many components – see partitioning and decomposition) but they are built/implemented from the bottom-up (modules built using components, sub-systems from modules, whole system from the sub-systems). Thus, applying V.V.T. inline with implementation allows errors or omissions to be more easily identified and the subsequent corrections to be incorporated within the design. The V.V.T. process, therefore, proceeds in stages where testing is carried out incrementally in conjunction with system implementation to test every element of the design at successive stages of assembly. While in any particular case the hierarchy has its own form, it will trace the following general pattern in which the testing process consists of five stages.



1. Unit testing - Individual components are tested to ensure that they operate correctly. Unit testing treats each component as a stand-alone entity that does not need other components during the testing process.
2. Module testing - A module is a collection of dependent components. A module encapsulates related components so can be tested without other system modules.
3. Sub-system testing - This phase involves testing collections of modules which have been integrated into sub-systems. Sub-systems may be independently designed and implemented, and the most common problems which arise in large systems are sub-system interface mismatches. The sub-system test process should concentrate on the detection of interface errors by rigorously exercising these interfaces.
4. System testing - The sub-systems are integrated to make up the entire system. The testing process is concerned with finding errors which normally result from unanticipated interactions between sub-systems and components. It is

also concerned with validating that the system meets its functional and non-functional requirements.

5. Acceptance testing - This is the final stage in the testing process before the system is accepted for operational use. It involves testing the system with data supplied by the customer (or his agent such as the marketing department) rather than simulated data developed as part of the testing process. Acceptance testing often reveals errors and omissions in the system requirements definition. The requirements may not reflect the actual facilities and performance required by the user and testing may demonstrate that the system does not exhibit the anticipated performance and functionality.

b.

As the number of inputs to a logic gate increases, so does the number of tests required to ensure it is operating correctly. For example, with 2 inputs 4 tests can fully characterise the system. If a gate had 24 inputs over 16 million tests would be required. If a chip contained many 24 input gates it is not unforeseeable that a billion tests would be required. This problem is known as "the combinatorial explosion".

If we are to avoid incomprehensively large systems (w.r.t. testing) we need to reduce the complexity to a reasonable level. One of the easiest ways to do this is to segment the circuit into small components that can be tested individually. So we need to partition the circuit in order to avoid having very large numbers of inputs and/or outputs. As an aside, it is worth remembering that this technique is just a manifestation of the general principle of "divide and conquer".

c.

i)

The stuck-at fault model assumes that any failure in a unit can be modelled by saying the output of the unit is "stuck-at" a particular logic value (0 or 1). In the SAF model we assume that the effect of the physical fault (whatever it may be) is to create only two kinds of logical fault: a stuck-at-1 fault (abbreviated to SA1 or s@1) and a stuck-at-0 fault (SAO or s@0).

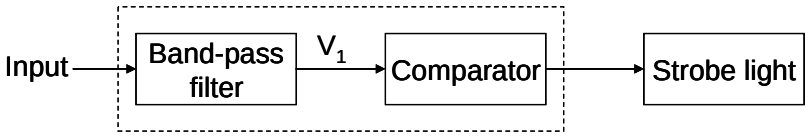
ii)

In fault simulation we place faults on a node, or on an input of a circuit, or on an output of a circuit. The circuit is then simulated to see what happens in a design when we deliberately introduce faults. In a production test there is only limited access to the circuit. To test a circuit we must devise a series of sets of input patterns that will detect any faults that there are in the circuit. A stimulus is the application of one such set of inputs (a test vector) to the inputs of the circuit.

A fault simulation mimics the behaviour of the production test. The fault simulator deliberately introduces all possible faults into our circuit, one at a time, to see if the test program will find them. As each fault is inserted, the fault simulator runs our test program. If the fault simulation shows that the outputs of the faulty circuit are different from the outputs of a good circuit at any time, then we have a detected fault; otherwise we have an undetected fault. This allows us to generate a set of test vectors that can be used to test a circuit during production.

d.

Although not stated, students should draw a block diagram of the system to identify system inputs and outputs and internal signals.



One should test the band-pass filter and comparator independently to ensure they are work and then combine to test the overall system.

Band-pass filter:
1. Test frequency response to ensure filter is operating correctly.
2. Test at differing signal levels to ensure linearity.

Comparator:
1. Test with DC input voltage to ensure correct switching thresholds.
2. Test with AC to ensure correct switching at high-frequencies.

Combined system:
Combine system and test with known input source, for example a signal generator with known frequency content. This ensures system is working as predicted.