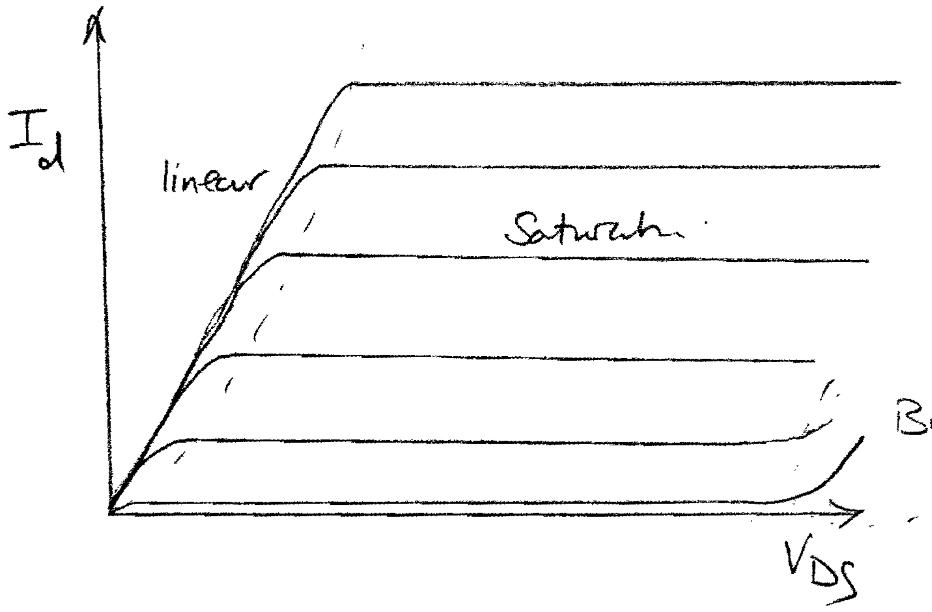
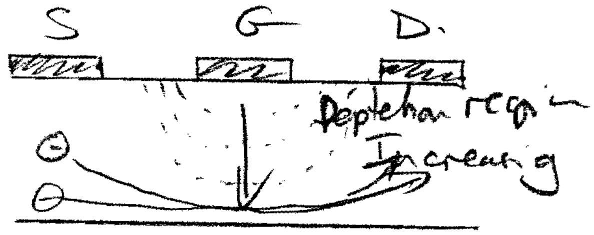
1a.



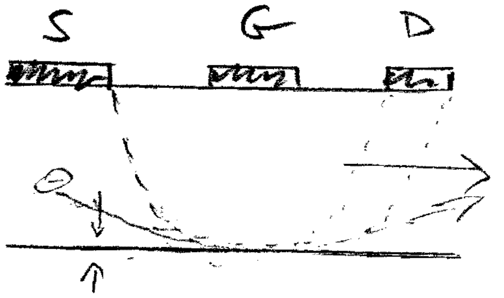
2 1

In the linear region the width of the depletion region is extended by the application of the gate voltage. It acts like a variable resistor on the drain. I_D is approx linear with V_D when $V_{DS} >> V_G$.



1

In the saturation region the device approaches pinch-off. The depletion region extends almost fully through the material whilst also being dragged towards the drain due to the higher V_{DS} values

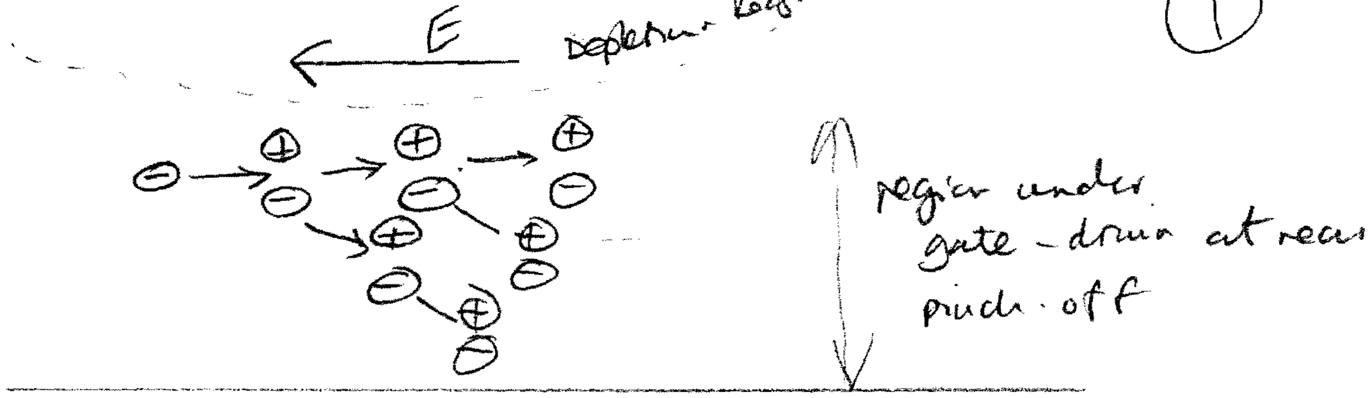


1

fixed thin remaining channel – High field due to V_{DS}. Electrons travel through fixed channel at saturation velocity – I_D constant.

1a Breakdown - increase in drain current at high -ve V_G and V_{DS}. Due to the high E field now developing between the gate and the drain. Eventually this reaches the impact ionisation threshold. Current is then multiplied through the creation of extra e-h pairs

1



1b.

Input ac current $= I_{GS}$.

$$I_{GS} = V_g / Z_g \qquad Z_g = \frac{C_g}{\omega} = 2\pi f C_G$$

so $I_{GS} = 2\pi f C_g V_g$

Output ac.

$$I_{DS} = g_m V_G$$ by definition of transconductance

Current gain $= \frac{\text{output}}{\text{input}} = 1$ when $f \to f_T$

So $\frac{g_m V_G}{2\pi \underbrace{f}_{=f_T} C_G V_G} = 1$ $\qquad f_T = \frac{g_m}{2\pi C_G}$ (3)

$g_m = \frac{\delta I_D}{\delta V_G}$ $\qquad I_D = (n_s q) V_{sat}$

sheet charge.

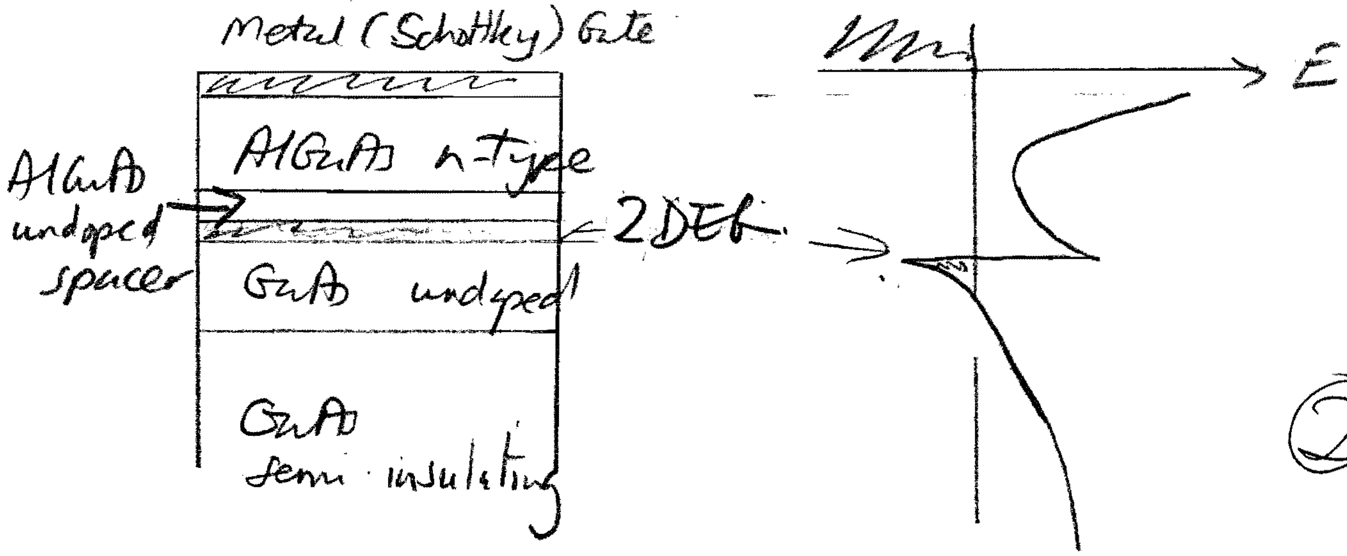
So $g_m = \frac{\delta (n_s q)}{\delta V_G} V_{sat} = \frac{C_G}{L} V_{sat}$ Gate width

$f_T = \frac{\cancel{C_G}}{L} V_{sat} \frac{1}{2\pi \cancel{C_G}} = \frac{V_{sat}}{2\pi L}$

$V_{sat} = 2\times10^5$ m sec^{-1}. $\quad L = 20\mu m$

$f_T = 1.6\times10^9 = 1.6$ GHz (3)

1c) ~~1B~~ HEMT



(2)

Charge flows from wide gap AlGaAs into narrow gap GaAs producing a thin channel of high density electrons at the interface - 2D electron gas.

Main advantages.

Seperation of electrons from ionised impurities, resulting in increased mobility due to the absence of ionised impurity scattering.

Channel can be positioned close to the gate and has a fixed high sheet charge

g_m and f_T improved due to mobility increase

g_m increased by proximity to gate

g_m - more constant with V_G

2

$$g_{MES} / g_{HEMT} = \frac{W \cdot \mu N_{MES}}{W \mu N_{HEMT}}$$

$$\frac{\cancel{5000 \times 10^{-4}} \times 0.3 \times 5 \times \cancel{10^{22}}}{\cancel{3600 \times 10^{-4}}\ 0.9 \times 2 \times \cancel{10^{22}}} = 1.39$$

g_m for MESFET is 1.39x higher. 2

f_T $\quad E = V/L \quad v = \mu E = \frac{\mu V}{L} \quad \tau = \frac{L}{v} = \frac{L^2}{\mu V}$

Transit

$$f_T = \frac{1}{2\pi\tau}$$

$$f_{T\,MES} / f_{T\,HEM} = \frac{\mu_{MES}}{\mu_{HEMT}}$$

$\frac{v}{2\pi L}$

f_T of HEMT is 3x Higher! 2

Similar g_m values (MESFET slightly high)
Much better f_T for HEMT.

2

For breakdown

$M_n \to \infty \qquad 1 - \frac{1}{M_n} \to 1.$

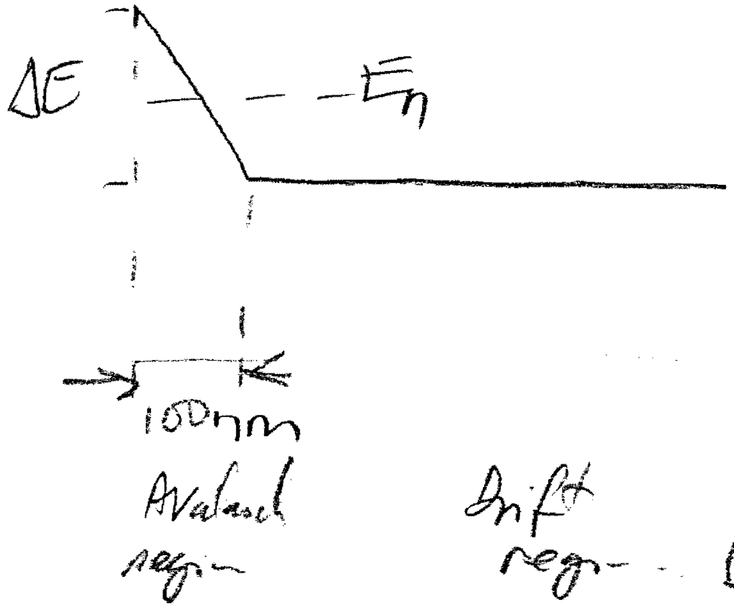
$\alpha W = 1$

$\alpha(E) = 3.8\times10^{7} \exp\left(-\frac{3\times10^{6}}{E_n}\right) m^{-1} = \frac{1}{W}$

$E_n = \frac{3\times10^{6}}{\ln[3.8\times10^{7}\times100\times10^{-9}]} = 2.25\times10^{6}$ V/m

(2)

This is the average field in the avalache region



$\Delta E \approx \frac{eh}{\varepsilon} dx$

$\frac{1.6\times10^{-19}\times5\times10^{21}\times100\times10^{-9}}{1.17\times10^{-10}}$

$\Delta E \quad 6.83\times10^{5}$ V/m

Breakdown Voltage - Area under curve

$E_n \times 100nm + \left(E_n - \frac{\Delta E}{2}\right) \times 800nm$

$0.225 + 1.522 = 1.752V$

(2)

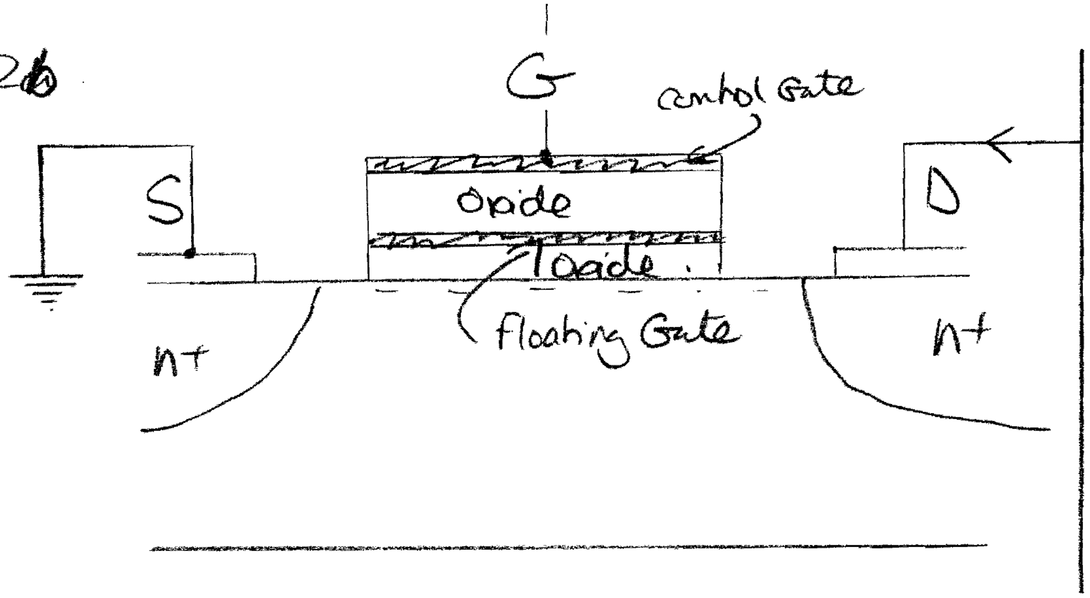
frequency

$V_{sat} = \frac{d}{\tau}$

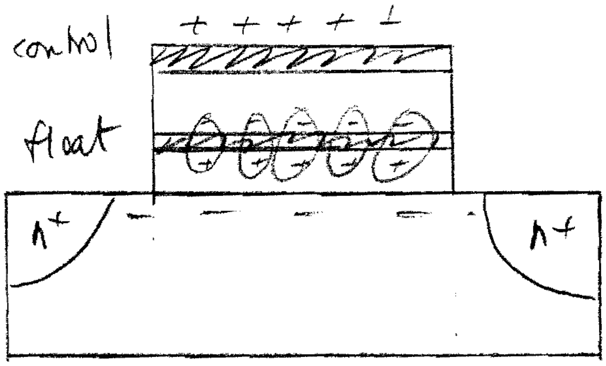
$f = \frac{1}{\tau} = \frac{V_{sat}}{d} = \frac{1.1\times10^{5}}{800\times10^{-9}} = 1.375\times10^{11}$ (2)

137GHz

2b



Flash memory (floating gate) MOSFET with two gates one of polysilicon, and surrounded by oxide. This floating gate is 'written' by placing charge on the upper control gate.

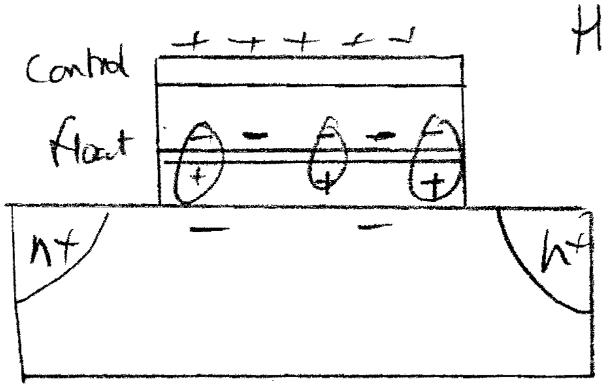


Normal FET operation

No net charge on floating gate (just polarisation charge)

V_T low.

2



HV pulse applied to word line - sufficient to bend bands and allow tunnelling to the floating gate

Trapped charge on floating gate (long lifetime)

Results in reduced charge in channel. 2

V_T high

Device read by applying a gate voltage sufficient large to overcome V_T low, but not V_T high, → will then either be low or high when read. 2

The device is erased when a large negative voltage pulse is applied sufficiently large to bend the bands and allow electrons to tunnel out of the floating gate. 1

Read voltage is 1.5V, V_T with no charge is 1.0V. so $V_{gs} > V_T$ in this case. We will need V_T with charge on the gate to be at least 1.5V (will accept slightly higher)

$\Delta V_T \left(\substack{\text{charge} \\ \text{ON - OFF}} \right) \doteq 0.5V$

simple electrostatics $\Delta V_T = \dfrac{\Delta Q_{float}}{C_{ox(top)}}$ $\Delta Q_f = C_{ox,tp} \Delta V_T$

$\Delta n_f = \dfrac{C_{ox} \cdot \Delta V_T}{e}$ $C_{ox} = \varepsilon \varepsilon_0 \dfrac{A}{d}$

$C_{ox} = \dfrac{3.9 \times 8.85 \times 10^{-12} \times (100 \times 10^{-9})^2}{20 \times 10^{-9}}$

$C_{ox} = 1.726 \times 10^{-17}$

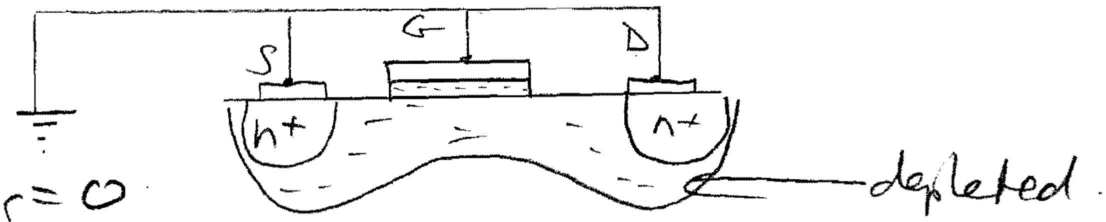
$\Delta n_f = \dfrac{1.726 \times 10^{-17}}{1.6 \times 10^{-19}} \cdot 0.5 = 54.$ 3

Very small nos of electrons involved

3a

(i)

$V_{GS}=V_{DS}=0$

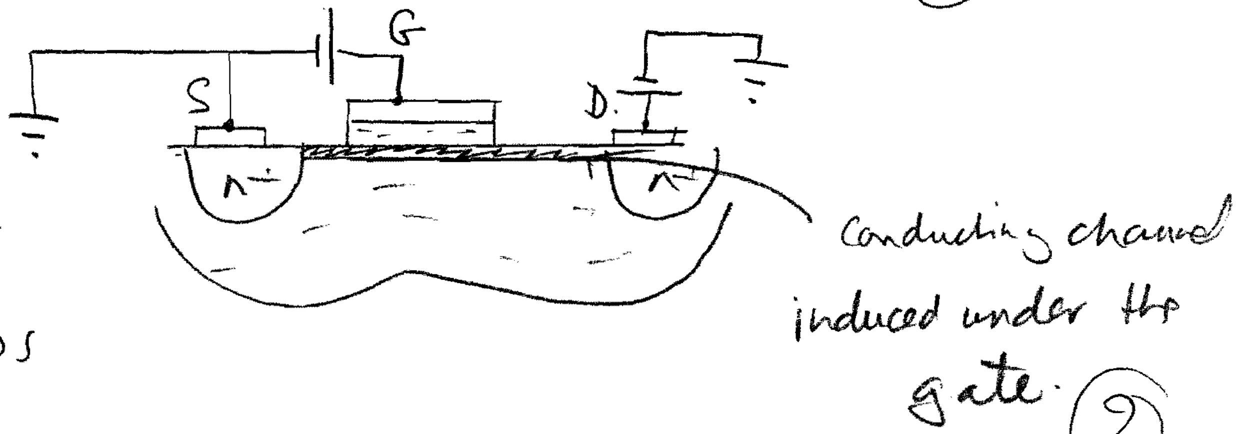


2

(ii)

$V_{GS}>V_T$

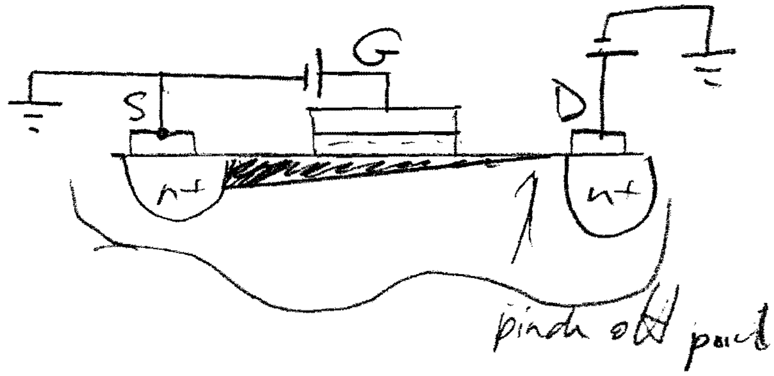
$V_{GS}\gg V_{DS}$



2

(iii)

$V_{DS}=V_{GS}-V_T$

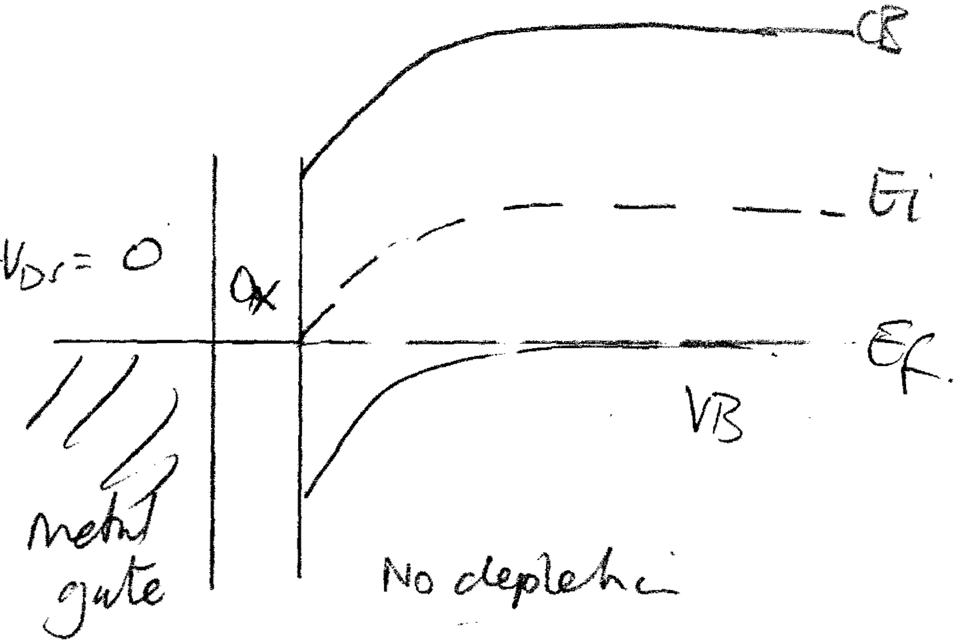


2

3b,

(i)

$V_{GS}-V_{DS}=0$



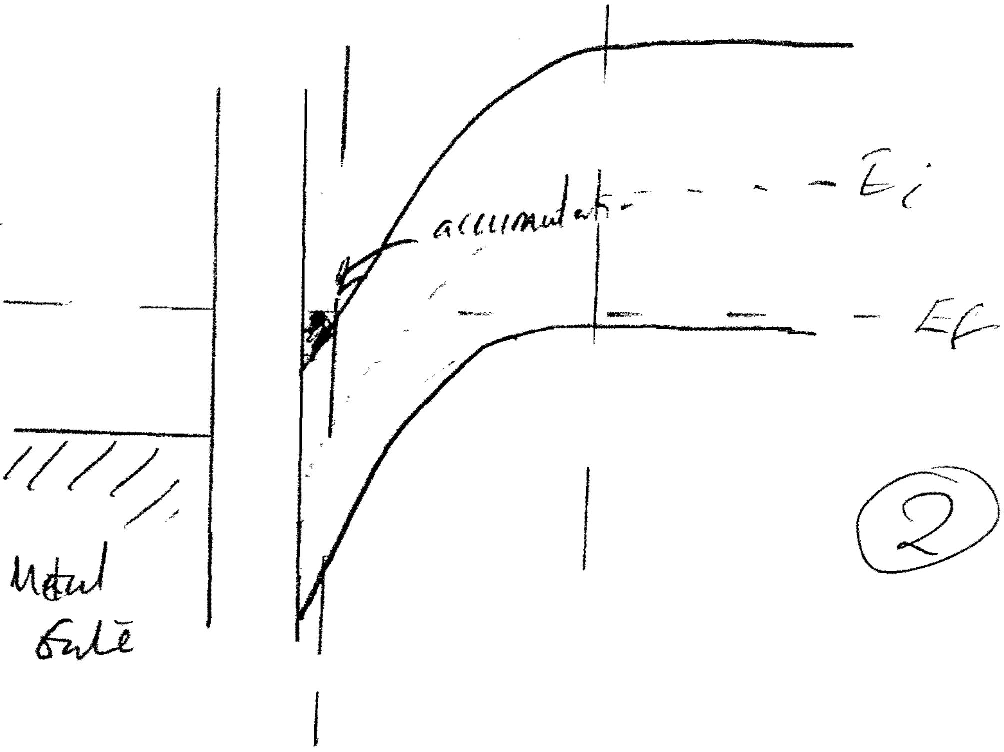
2

SD cont

(ii)

$V_{GS} > V_T$

$V_{GS} \gg V_{DS}$



(2)

3c Drain current 150μA at 1.5V Value at 2.0V + at 3.0V

$$I_D = \frac{Z\mu C_{ox}}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS}$$

1mm, 200nm

$$I_{D1} - I_{D2} = \frac{Z\mu C_{ox}}{L}\left[V_{GS1} - V_{GS2}\right] V_{DS} = 0.2V$$

$$= \frac{Z\mu C_{ox}}{L}[0.5V]\,0.2 \text{ in case 1}$$

$$= \frac{Z\mu C_{ox}}{L}[1.5V]\,0.2 \text{ in case 2.}$$

Cut!

$C = 1\times10^{-6}\,Fm^{-2}$ $\mu = 0.06\,m^2V^{-1}s^{-1}$.

$$\frac{Z\mu C_{ox}}{L} = \frac{1\times\cancel{10^{-3}}\times6\times10^{-2}\times1\times\cancel{10^{-6}}}{200\times\cancel{10^{-9}}} = 3\times10^{-4}.$$

3c cont

~~ΔI_D (case 1) $= 3\times10^{-4} \times 0.5 \times 0.2 = 30\mu A$~~

~~ΔI_D (case 2) $= 3\times10^{-4} \times 1.5 \times 0.2 = 90\mu A$~~

~~at 2V $I_D = 150+30 = 180\mu A$~~

~~3V $I_D = 150+90 = 240\mu A$~~

cut! too long!

3d) $C_{ox} = 1.8\times10^{-11}\ F.m^{-2}$ $\chi_{Si} = 4.1$ $\chi_{SiO_2} = 0.95$

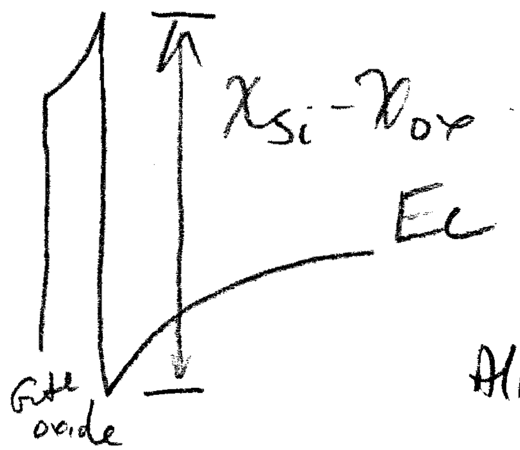
$C_{ox} = \frac{\varepsilon_r \varepsilon_o}{t_{ox}}$ $\frac{\varepsilon_r}{t_{ox}} = \frac{C_{ox}}{\varepsilon_o} = 2.nm^{-1}$ ($t_{ox} = 1.95nm$)

1 Required to double this $\Rightarrow 4nm^{-1}$

Oxide A $\frac{\varepsilon_r}{t_{ox}} = 4nm^{-1}$ $t_{ox} = \frac{\varepsilon_r}{4} = 2nm$ 1

Oxide B $t_{ox} = \frac{\varepsilon_r}{4} = \frac{16}{4}$ $t_{ox} = 4nm$ 1

Barrier height



Oxide A 1

$\chi_{Si} - \chi_A = 4.1 - 1 = 3eV$

Almost same as SiO_2

Oxide B 1

$\chi_{Si} - \chi_B = 4.1 - 3.7 = 0.4V$

Almost no barrier for oxide B 1

The greater thickness of oxide B would be advantageous in terms of lower leakage and better yield. However the barrier height is only 0.4eV. This is insufficient and will result in a strong tunnelling current.

Oxide A is more suitable - a doubling of the capacitance with similar t_{ox} and barrier height to Si/SiO2.

4

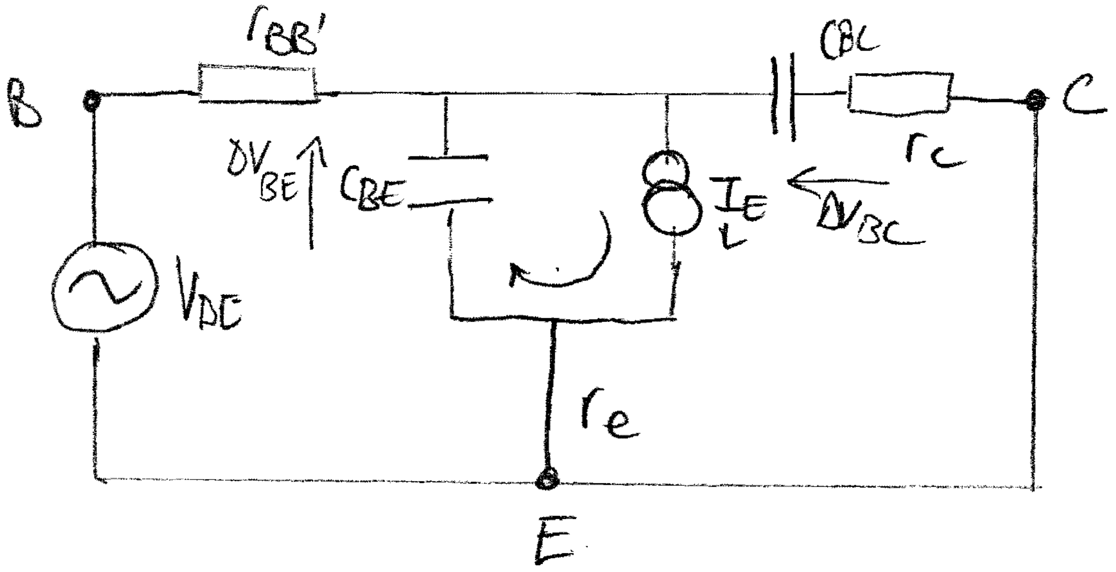
4\.
a) $f_T = \frac{1}{2\pi \tau_{EC}}$ $\tau_{EC} = \tau_{BE} + \tau_{BC} + \tau_B + \tau_C$

capacitive/charging

τ_{BE} – Time required to charge the base-emitter junction capacitance – to allow carrier injection

τ_{BC} – Time required to charge base-collector junction to allow carriers to flow through the device

~~2a~~ 1



2

τ_{BE} dependent on C_{BE} – charged by the diode current I_E.

$$\tau_{BE} \simeq \frac{dQ_{BE}}{dI_E} \simeq C_{BE}\frac{dV_{BE}}{dI_E}$$

differentiate diode eqn (should be known)

$$\simeq \frac{kT}{qI_E} C_{BE}$$

Reduce τ_{BE} – increase I_E or reduce C_{BE} (reduce doping in emitter)

τ_{BC} is related to C_{BC} charging time. 2

V_{BC} is responsible for charging C_{BC} - an amount ΔV_{BC}. Kirchoff's Law (or otherwise) (collector loop)

$$\Delta V_{BC} = \Delta V_{BE} + \Delta I_c (r_e + r_c)$$

$$\tau_{BC} = \frac{d Q_{BC}}{d I_c} = C_{BC} \frac{d V_{BC}}{d I_c}.$$

Substituting for ΔV_{BC}.

$$= C_{BC}\left(\frac{dV_{BE}}{dI_c} + r_e + r_c\right)$$ 2

Improve τ_{BC}

- reduce parasitics r_e, r_c
- increase collector current I_c. 2
- reduce C_{BC}.

b) HBT - uses a heterojunction - different emitter + base materials

HBT advantages. | Limits the back injection of holes into the emitter

(i) EB heterojunction

- hole inj. suppressed. Higher inj efficiency → higher gain

Base may now be doped v. high

materials $\underset{E}{Si}/\underset{B}{SiGe}$, $GaAs/AlGaAs$, $\underset{E}{InP}/\underset{B}{InGaAs}$

(ii) Higher base doping can now be used.

- reduced $r_{BB'}C_{BC}$ delay time. → increased f_T

(iii) Can reduce emitter doping.

3 ~~one per~~ advantage → reduced C_{BE} → reduced τ_{BE} → increased f_T.

(IV) Lower band gap base generally means higher mobility material eg: InGaAs in GaAs based HBT's.

3 - one per correctly argued advantage

c. (i) Switching voltage

Reduce power dissipation – allow higher speeds + higher packing density.

Has reduced from ~5V to ~1.05V over many years primarily due to materials processing improvements.

Physical limitation interface charges and unintentional doping in the channel contributing to a finite V_T.

Voltage must be $\gg V_T$.

Ultimate limit if V_T reduced → ~100mV. Needs to be $\geqslant 4kT$. logic swing for on and off state to be distinguishable.

Also limited by fluctuations in V_T due to the random position of dopands/impurities. 2

(ii) Gate dielectric thickness

Need a high C_g or at least to maintain it whilst scaling other factors.

I_D, g_m etc are $\propto \frac{1}{d_{ox}}$. 2

Dielectric thickness has been continually reduced until leakage due to QM tunneling has limited

... scaling. typically this is now ~ ...
Uniformity problems leading to low yield also an issue.

(iii) Gate material

SiO2 reached its limits some time ago.

Using 'high-k' oxides Hf_2O_3. to increase capacitance.

Can also back-off on thin dielectric thickness

Other high k under investigation. 2

(iv) Gate Length

Reductions in the gate length have given major improvements → g_m, I_D, f_T etc all scale well. Now very close to the limits of optical lithography (EUV) at ~20-30nm.

Could use E-beam lithography, but limits - relatively slow + expensive. Or x-ray methods, but not yet fully developed.

Ballistic transport comes in at < 20nm.

Ultimate limit QM tunnelling between Source + Drain - independent of gate 2

~~(v) Interconnects~~

~~Trend has been to smaller tracks, higher densities~~

~~→ Increased resistance, mutual inductance + capacitive coupling to devices.~~

~~Using copper after development of Damascene process~~

cut