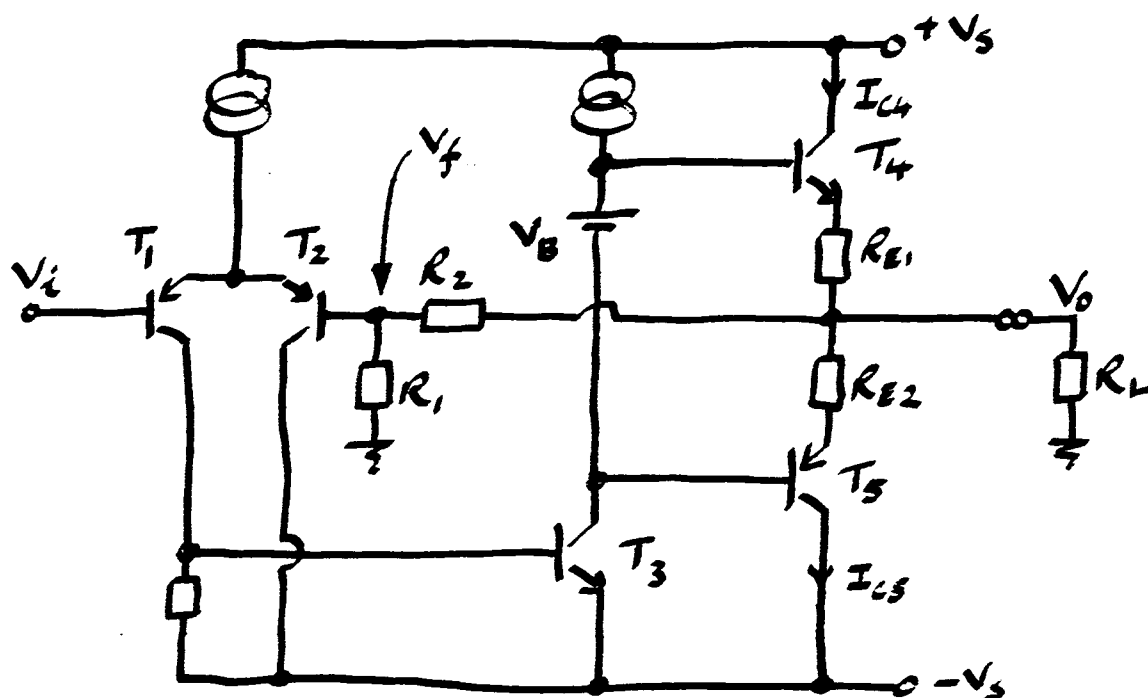


# Power Amplifiers

- typical circuit topology .....



- $T_1$  &  $T_2$  form a "differential amplifier" or "long tailed pair". It behaves like the differential input of an op-amp ( $V_i \equiv v^+$  and  $V_f \equiv v^-$ ) and as in the case of the op-amp, because the open loop amplifier gain is high,  $V_i \approx V_f$ . The gain of this first stage is typically between 2 and 10 V/V.
- $T_3$  is a common emitter voltage gain stage. A high voltage gain is obtained by providing  $T_3$  with a high impedance collector load, hence the current source in the collector circuit. The gain of this stage is typically between 5000 and 20000 V/V.
- $V_B$  is a floating voltage source which interacts with the base-emitter junctions of  $T_4$  &  $T_5$ , and their associated resistors  $R_{E1}$  &  $R_{E2}$ , to control the bias current through the output stage, and hence control crossover effects.
- $T_4$  &  $T_5$  are output emitter followers.  $T_4$  does the work (ie supplies the current) on positive output half cycles whilst  $T_5$  deals with the negative half cycles. In this way, the load is driven by a low output impedance in both polarities of output voltage.

The bias control circuit in a little more detail is ....

$V_B$  is set by a circuit known as a " $V_{BE}$  multiplier" - a very common arrangement in both power amplifier and op-amp output stage biasing.

$T_6$  always conducts so  $V_{BE6}$  will be more or less constant

$$\therefore I_{R4} = \frac{V_{BE6}}{R_4}$$

and  $I_{R3} \approx I_{R4}$  if  $I_{B6}$  is negligible

$$\therefore V_{R3} = I_{R3} R_3 = I_{R4} R_3 = \frac{V_{BE6}}{R_4} \cdot R_3$$

$$\text{and } V_B = V_{R3} + V_{R4} = \frac{V_{BE6} R_3}{R_4} + V_{BE6} = V_{BE6} \left[ \frac{R_3 + R_4}{R_4} \right]$$

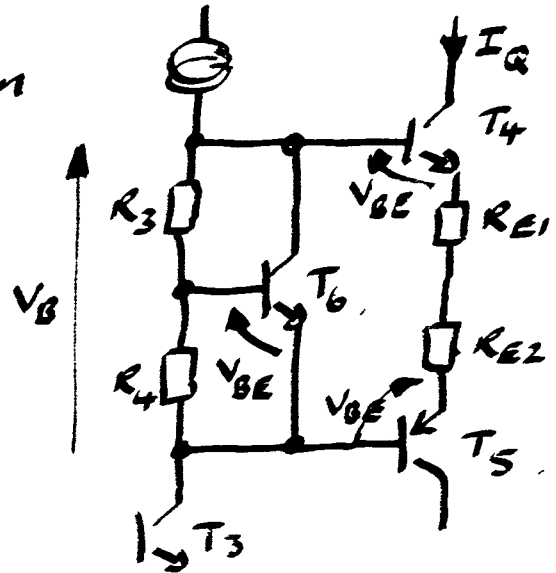
this is the factor that multiplies  $V_{BE6}$

The quiescent output current,  $I_Q$  is controlled by  $R_{E1} + R_{E2}$  since the voltage across  $R_{E1} + R_{E2}$  is controlled by  $V_B$  .....

$$\begin{aligned} V_B &= V_{BE4} + I_Q R_{E1} + I_Q R_{E2} + V_{BE5} \\ &= I_Q (R_{E1} + R_{E2}) + 2V_{BE} \end{aligned}$$

$$\text{or } I_Q = \frac{V_B - 2V_{BE}}{R_{E1} + R_{E2}} = \text{"Quiescent" or "no signal" bias current through the output stage.}$$

Note that if the transistors heated up,  $I_Q$  would tend to increase since  $V_B - 2V_{BE}$  would increase. If  $R_{E1}$  and  $R_{E2}$  do not exist, the value of  $I_Q$  is uncontrolled and increases in temperature lead to increases in  $I_Q$  which lead to further increases in temperature ..... and so on. The process is known as "thermal runaway" and is usually destructive.



The presence of  $R_{E1} + R_{E2}$  limit thermal runaway to manageable proportions by their negative feedback action and the effects of temperature changes on  $I_Q$  can be almost eliminated by making sure that  $V_{BE6}$  (the  $V_{BE}$  that controls  $V_B$ ) accurately tracks  $V_{BE4}$  and  $V_{BE5}$  in temperature.

## Amplifier Classes

An amplifier with a circuit shape as shown on page ① is often referred to as "push pull" or "double ended". Single ended amplifiers were used in the days of valves but are almost unheard of in transistor circuitry. The following comments apply to push-pull amplifiers unless otherwise stated.....

The class of amplifier describes either the way it is biased or the way it works. There are four main classes:-

Class A	} These three describe different output stage bias conditions for the output circuit of page 1.
Class B	
Class C	
Class D	This is a completely different type of amplifier.

Class A, Both output devices are biased so that they are active throughout a signal cycle.

- Very good linearity
- Very poor efficiency.

Class B The output devices are never on together and never off together - ie top transistor does the +ve half cycles and bottom transistor the -ve ones.

- good linearity
- good efficiency

Class C, The output transistors are both off for most of a signal cycle.

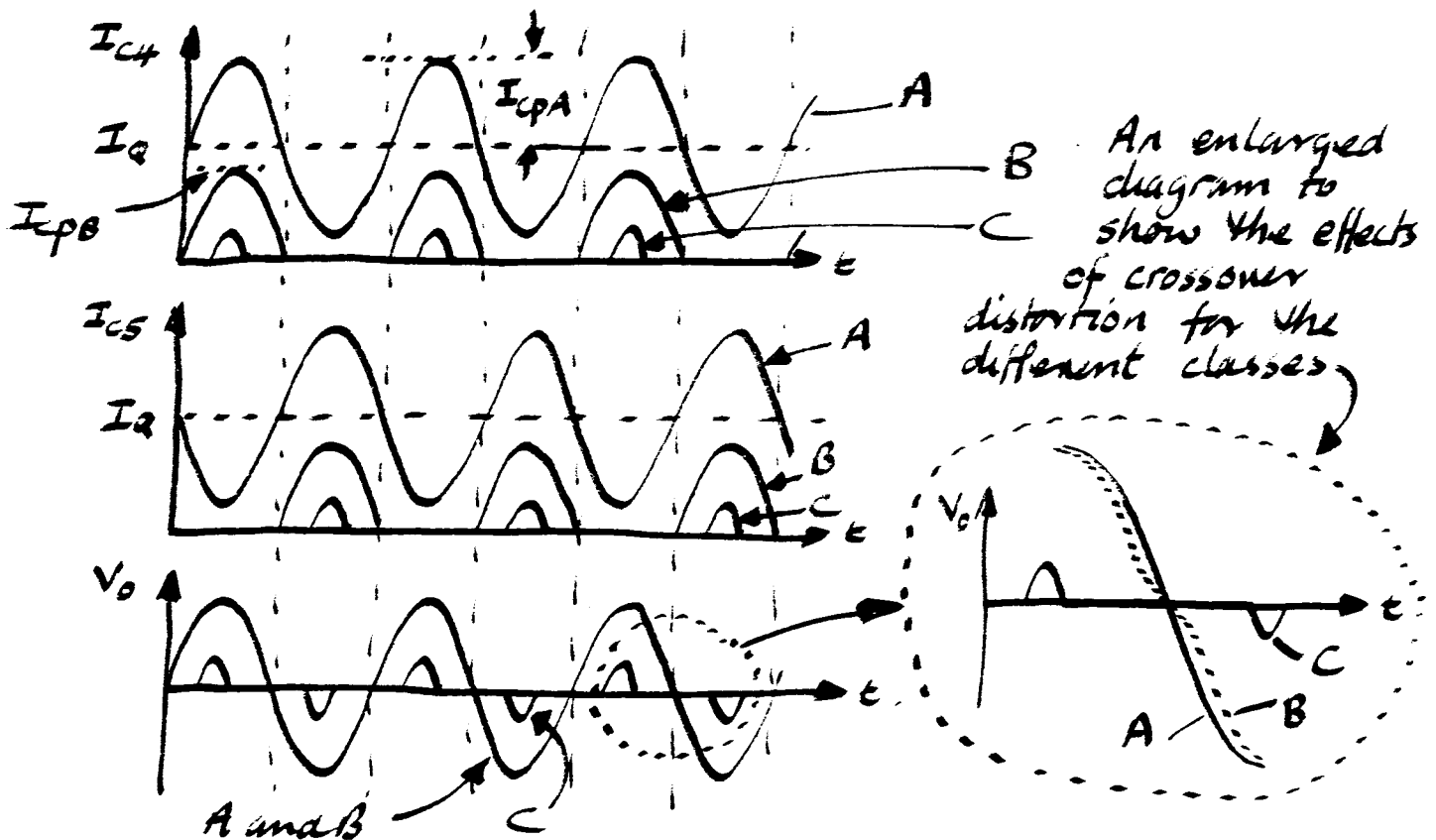
- poor linearity because of extreme crossover distortion
- excellent efficiency
- only useful for RF circuits.

Class D. This is a completely different approach to amplification involving switching transistors and pulse width modulation.

- reasonable linearity
- excellent efficiency.

There are also a number of intermediate classes between A and B which have various ranges of input signal for which both transistors conduct. Such intermediate classes (usually called AB) operate at Class A for low level signals and approach Class B for large amplitude signals.

The collector currents and output voltage for the three amplifier classes A, B and C are ....



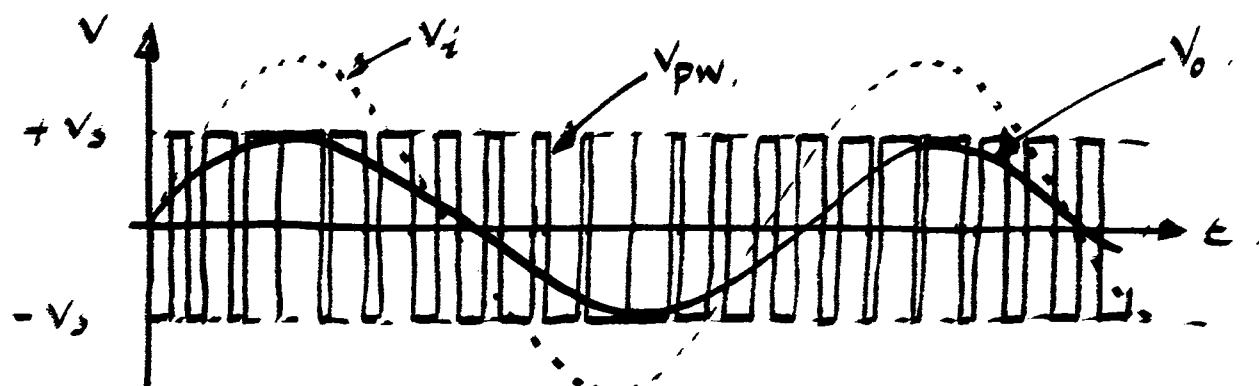
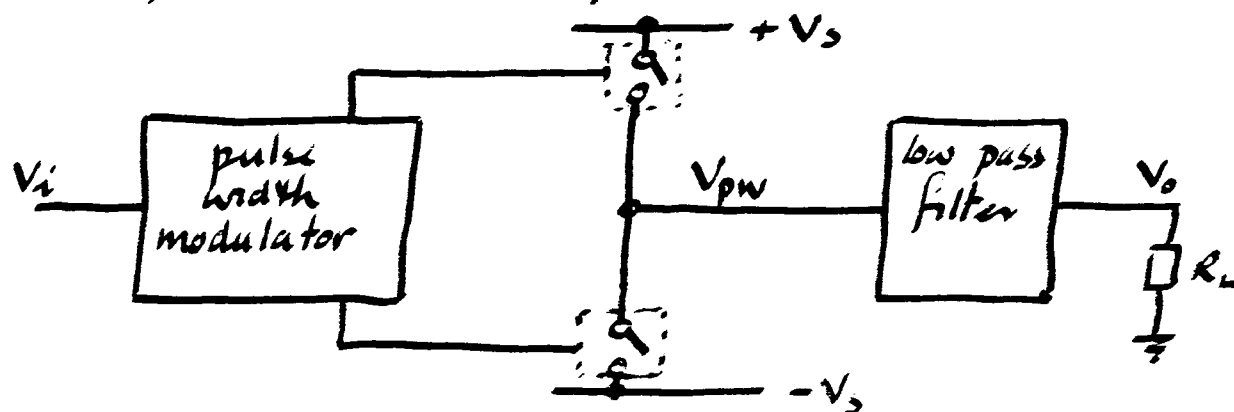
$$I_{Lpk} \text{ for A} = 2 \times I_{CPA} \quad \therefore V_{OAp} = 2 I_{CPA} \cdot R_L$$

$$I_{Lpk} \text{ for B} = I_{CPB} \quad \therefore V_{OBp} = I_{CPB} \cdot R_L$$

$$I_{Lpk} \text{ for C} = I_{CP} \quad \therefore V_{Ocp} = I_{CP} \cdot R_L$$

Crossover distortion is the non-linearity caused when conduction transfers from the top transistor to the bottom or vice versa.

Class D works by switching between the power supplies at a frequency that is high compared to the maximum frequency of interest. The ratio of high time to low time is varied (pulse width modulation) to vary the average voltage reaching the load.....

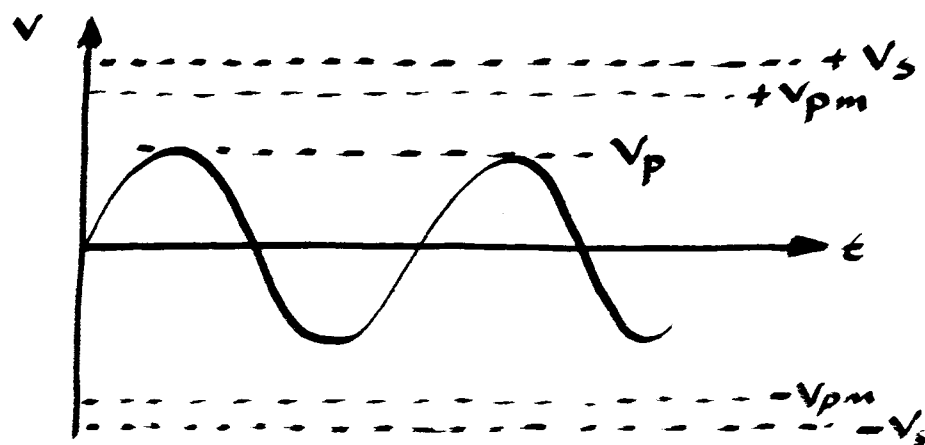


Note:  $V_i$  is not drawn to scale - usually  $V_i \ll V_s$ .

This type of amplifier is very efficient because the output transistors are either on (ie large  $I_c$  but small voltage drop) or off (ie large voltage drop but small  $I_c$ ) so the  $VI$  product for the output devices is always small.

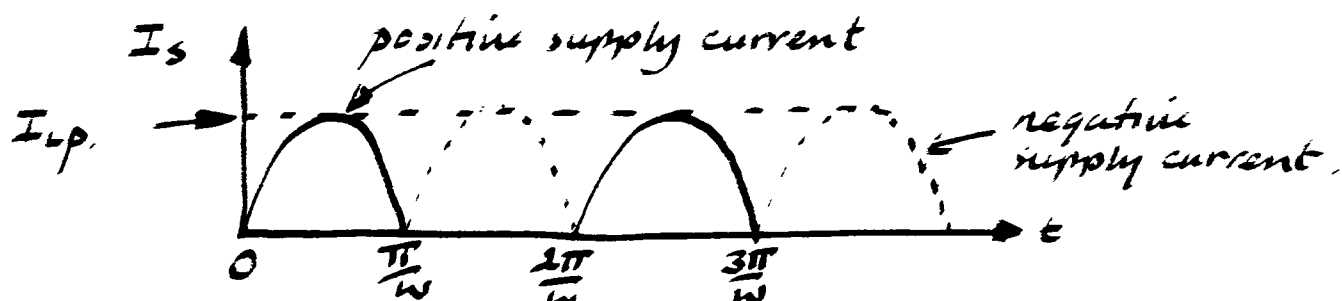
## Power Dissipation in Class B Amplifiers.

- Class B commonest - usually with a very small  $I_Q$  (making it class A for very small signals). The  $I_Q$  is usually sufficiently small to have a negligible effect on power dissipation in the output devices.



$V_s$  = supply voltage

$V_{pm}$  = max value of peak load voltage that the amplifier can support. Sometimes  $V_{pm} \approx V_s$ .



To find power dissipated in  $T_4$  .....

$$V_{C4} = V_s$$

$$V_{E4} \approx V_L = V_p \sin \omega t$$

$\therefore$  voltage drop across  $T_4$  is

$$V_{CE4} = V_{C4} - V_{E4} = V_s - V_p \sin \omega t$$

$I_{C4}$  = positive supply current

$$= I_{Lp} \sin \omega t \quad \text{for } t = 0 \text{ to } \frac{\pi}{\omega}$$

$$= 0 \quad \text{for } t = \frac{\pi}{\omega} \text{ to } \frac{2\pi}{\omega}$$

$$P_D = \frac{1}{T} \int_0^T V(t) I(t) dt \quad \text{--- (1)}$$

$$= \frac{1}{2\pi/\omega} \int_0^{\pi/\omega} (V_s - V_p \sin \omega t) (I_{Lp} \sin \omega t) dt$$

note that the integral is performed over 0 to  $\pi/\omega$ . Between  $\pi/\omega$  and  $2\pi/\omega$ ,  $I(t) = 0$  so it is pointless to integrate that bit..... but the averaging is still over a cycle, hence the  $1/\pi\omega$  before the integral.

$$I_{Lp} = V_p / R_L$$

$$\begin{aligned} \text{so } P_D &= \frac{\omega}{2\pi} \int_0^{\pi/\omega} (V_s - V_p \sin \omega t) \left( \frac{V_p}{R_L} \sin \omega t \right) dt \\ &= \frac{\omega}{2\pi} \int_0^{\pi/\omega} \frac{V_s V_p \sin \omega t}{R_L} dt - \frac{\omega}{2\pi} \int_0^{\pi/\omega} \frac{V_p^2}{R_L} \sin^2 \omega t dt \\ &= \frac{V_s V_p}{\pi R_L} - \frac{V_p^2}{4 R_L} \quad \text{--- (2)} \end{aligned}$$

This is the difference between a linear and a quadratic term and so will have a maximum value somewhere.....

$$\frac{dP_D}{dV_p} = \frac{V_s}{\pi R_L} - \frac{2V_p}{4R_L} = 0 \text{ for max}$$

$$\text{ie } P_D \text{ max when } V_p = \frac{2V_s}{\pi}$$

$\therefore$  max  $P_D$  is ....

$$\begin{aligned} P_{Dm} &= V_s \left( \frac{2V_s}{\pi} \right) \frac{1}{\pi R_L} - \left( \frac{2V_s}{\pi} \right)^2 \frac{1}{4R_L} = \frac{2V_s^2}{\pi^2 R_L} - \frac{4V_s^2}{4\pi^2 R_L} \\ &= \underline{\underline{\frac{V_s^2}{\pi^2 R_L}}} \end{aligned}$$

Note that this is the power dissipated per transistor because the  $V(t)$  and  $I(t)$  used to evaluate it related to one transistor.

The power dissipated in  $T_5$  is the same as that dissipated in  $T_4$  because of the symmetry of the circuit, i.e. the waveforms across + through the transistors are identical except for a phase shift. Note that the idea of r.m.s. is inappropriate in this sort of power calculation.

### An alternative way of finding $P_D$

The previous derivation of dissipated power was based on the power integral of equation (1), the classical way of calculating power dissipation. An alternative is to use arguments based on energy conservation.....

$$\text{Power in} = \text{Power out}$$

↑  
Total power supplied  
by the supplies  $\pm V_S$

↙  
Power Dissipated plus  
power delivered to load.

$$\text{i.e. } P_S = P_D + P_L$$

$$\begin{aligned} P_S &= \frac{1}{T} \int_0^T V(t) I(t) dt \\ &= V_S \cdot \frac{1}{T} \int_0^{T_0} I(t) dt \\ &= V_S \cdot I_{AVE} \end{aligned}$$

$$= V_S I_P / \pi$$

$$= \frac{V_S V_P}{\pi R_L} \text{ per supply}$$

and since there are two supplies...

$$P_S = \frac{2V_S V_P}{\pi R_L}$$

$$\begin{aligned} P_L &= \frac{V_{r.m.s.}^2}{R_L} \\ &= \frac{V_P^2}{2R_L} \end{aligned}$$

Note that r.m.s. can be used here because the waveform is sinusoidal and the load is a linear resistor.

$$\text{hence } \frac{2V_S V_P}{\pi R_L} = P_D + \frac{V_P^2}{2R_L}$$

$$\text{or } P_D = \frac{2V_S V_P}{\pi R_L} - \frac{V_P^2}{2R_L}$$



This is the same as equation (2) in the previous derivation except that  $P_D$  is now the total dissipation — hardly surprising since  $P_S$  is the total power supplied and  $P_L$  is the total load power.

Proceeding as before gives :-

$$P_{om} = \frac{2V_s^2}{\pi^2 R_L} \text{ for both devices}$$

(ie  $V_s^2 / \pi^2 R_L$  per device).

- NOTES - Max dissipation does not necessarily occur at max power output.
- These relationships are different for different waveshapes
  - Heatsink requirements must be specified on basis of maximum power dissipation.

### Choosing a value for $V_s$ .

Supply voltage  $V_s$  depends on :

- required maximum output power
- load resistance
- waveform of interest (eg sinusoid, triangle, etc)
- minimum voltage difference between  $V_s$  and the maximum peak output voltage,  $V_{pm}$ .

If  $V_s$  is bigger than it needs to be, energy will be wasted.

Let maximum load power required =  $P_{Lm}$   
 Load resistance =  $R_L$   
 ( $V_s - V_{pm}$ ) =  $V_{DIFF}$   
 waveshape = sinusoid

$$P_{Lm} = \frac{V_{r.m.s. \max}^2}{R_L} = \frac{V_{pm}^2}{2R_L}$$

$$\therefore V_{pm} = \pm \sqrt{2R_L P_{Lm}}$$

$$\therefore V_s = \pm \left[ \sqrt{2R_L P_{Lm}} + V_{DIFF} \right]$$

$\approx \pm \sqrt{2R_L P_{Lm}}$  if  $V_{DIFF} = 0$ , ie if the output devices work normally to  $V_{CE} = 0$ .

Defining the peak and average current that the supply must be capable of delivering.

The supply current,  $I_s$ , is a half wave rectified version of the load current for each supply as shown on page 6.

The largest peak current  $I_{Lpm}$  is given by Ohm's law as

$$I_{Lpm} = \frac{V_{pm}}{R_L} \approx \frac{V_s}{R_L} \text{ if } V_{DIFF} = 0$$

The average value of a half wave rectified sinusoid with an amplitude  $I_{Lpm}$  is:

$$I_{AVE} = \frac{I_{Lpm}}{\pi} = \frac{V_{pm}}{\pi R_L} \approx \frac{V_s}{\pi R_L} \text{ if } V_{DIFF} = 0.$$

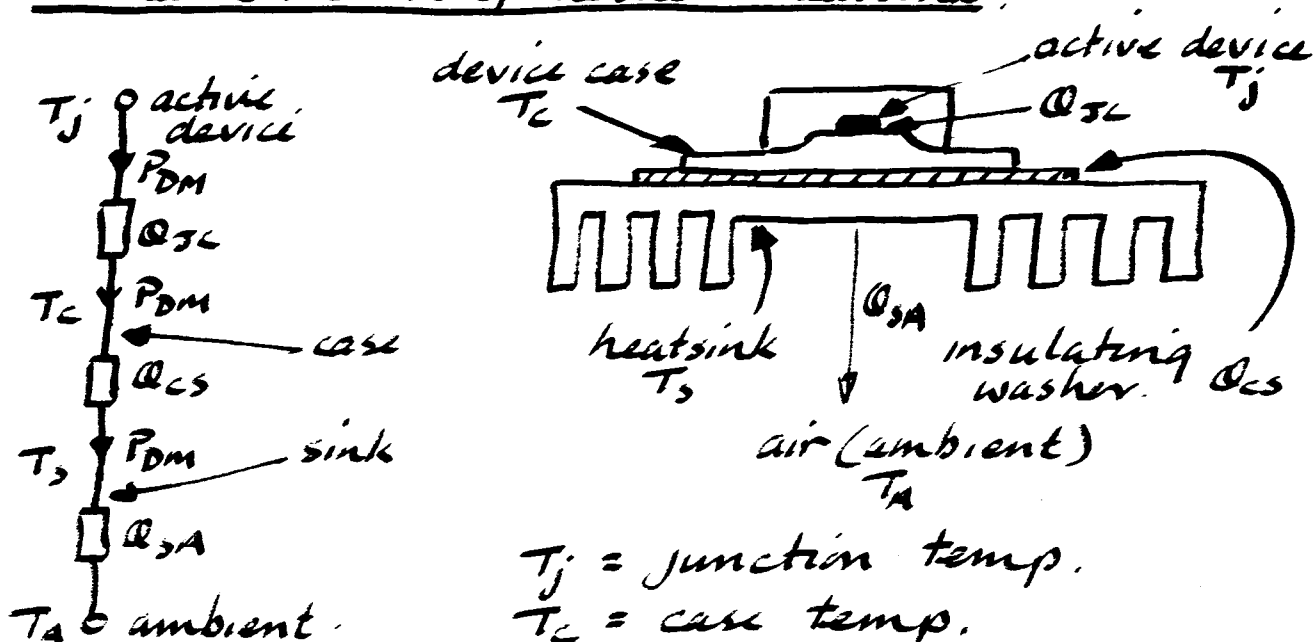
WARNING You need to think carefully for a particular application about which of the peak or the average value is the appropriate one to use. eg if the amplifier works down to dc (0Hz),  $I_{AVE}$  is equal to  $I_{Lpm}$  under some circumstances.

Removing the dissipated thermal energy

- done using a heatsink
- air cooled by convection, forced air (fan) cooled, water cooled, etc depending on amount of power to be removed.
- heatsinks specified by "thermal resistance" which has the units  $^{\circ}\text{C}/\text{W}$

- ie if you know how many watts are passing through a thermal resistance you can easily work out the temperature difference across it.

### Thermal Structure of device + heatsink.



$T_J$  = junction temp.  
 $T_C$  = case temp.  
 $T_S$  = sink temp.  
 $T_A$  = ambient temp.

$Q_{JC}$  = junction to case thermal resistance  
 $Q_{CS}$  = case to sink thermal resistance  
 $Q_{SA}$  = sink to air (ambient) therm. res.

The relationships are intuitive and straightforward:

$$T_S = P_{DM} Q_{SA} + T_A$$

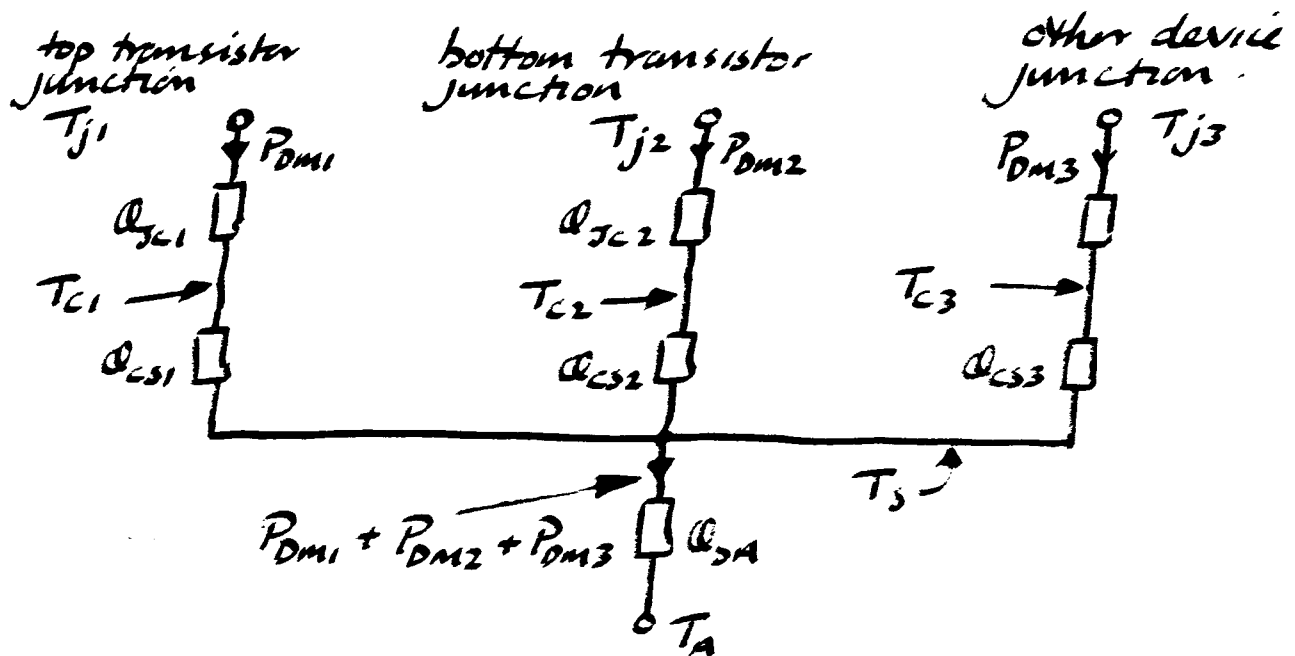
$$T_C = P_{DM} Q_{CS} + T_S = P_{DM} Q_{CS} + P_{DM} Q_{SA} + T_A$$

$$\begin{aligned}
 T_J &= P_{DM} Q_{JC} + T_C = P_{DM} Q_{JC} + P_{DM} Q_{CS} + T_S \\
 &= P_{DM} Q_{JC} + P_{DM} Q_{CS} + P_{DM} Q_{SA} + T_A
 \end{aligned}$$

You must use  $P_{DM}$ , the maximum power dissipation, and  $T_A$  must be the maximum expected ambient temperature.  
 The limits are usually  $T_J$  (typically  $120^\circ\text{C}$  to  $150^\circ\text{C}$  - figure given in manufacturers data) and  $T_S$ . The limit on  $T_S$  is simply to prevent overheating of components near

the heatsink and to prevent burn injuries to operators. (many devices are happy at  $100^{\circ}\text{C}$ , humans, regrettably, are not!)

If there are two (or more) devices mounted on the same heatsink, just extend the model



If  $T_1 = T_2$  are the output stage of a power amplifier,  $P_{DM1} = P_{DM2}$ .

**NOTE** An IC amplifier effectually has one junction in thermal terms;  $T_j$  is actually the silicon chip temperature. All the power dissipated in the output stage passes through the IC's  $\theta_{jc}$  and  $\theta_{cs}$ .

This thermal model works reasonably well for most low and medium frequency devices — transistors, rectifiers, thyristors, triacs, IGBTs, power resistors and many more.