1.(a) The economic decision as to whether a chip should be implemented as a PLD, gate array, cell-based or full custom will depend on the size of the market for that chip. Sketch a graph showing price per chip versus market volume to compare the relative costs of these implementations. Briefly explain why the different implementations have different relative costs at different market volumes. [8 marks]

(b) In each of the following situations you are called in as a consultant to advise on which ASIC technology would be most appropriate. In each case produce a reasoned argument leading to appropriate advice. Note that the best solution may not always be clear, in which case you should narrow down the possibilities as much as possible and make it clear what extra information you would require before you could make a firm decision. *[note that the supporting arguments are critical here - a simple statement that specifies a technology without argument will not receive high marks. However, the arguments should be specific to the given situations, not a simple repetition of those presented in section (a). The purpose of these questions is to show that you can apply the ideas from section (a) to realistic situations]* [12 marks]

(i) A small company makes digital electronic systems to pre-process data from sensors on the control surfaces of commercial airliners. Traditionally they have implemented their designs on conventional PCBs using commercially available ICs. However, they now have evidence that their commercial competitors are reverse engineering their products and stealing their designs. Another consultant has suggested using an ASIC to implement their next product to protect their design. Unfortunately the consultant's report does not say why this will work. Briefly discuss whether this is a good idea. If they choose to try this approach, what type of ASIC do you advise them to use?

(ii) A large electronics company has developed a new type of video telephone. The data compression is much higher than previous types allowing high quality communication down a conventional telephone line. However, the compression requires a large amount of electronics working at fairly high speed. they are considering whether to implement this electronics on an ASIC. The marketing division believes that the potential market is huge but expects competitors to launch similar products in about 12-18 months. Until then this product will have a monopoly. What technological and commercial issues are critical and what approach would you recommend?

(iii) A large chemical factory has been forced to temporarily cease production following the failure of its safety inspection. Another consultant has designed electronics to remedy the safety problems, but its implementation in discreet components is too slow to satisfy the safety inspectors. The quoted performance of available PLDs is marginal on speed. What will you recommend? Take care to give as many supporting arguments for your recommendation as possible.

2. (a) (i) When analysing a VLSI circuit for test purposes, it is usual to make an assumption about the **types** of fault that might be present. What is this assumption and why is it necessary? [2 marks]

(ii) Figure 2a shows a simple circuit. List all the possible states that might be considered by fault simulation based on only the assumption in part(i) [3 marks]
(iii) In practice it is also usual to make an assumption about the **number** of faults present. State this assumption and explain why it is justifiable. Make a new list of the states that fault simulation must consider for the circuit in figure 2a based on both the assumption in part (i) and this new assumption. [3 marks]
(iv) Thus give generalised relations for the number of states that must be considered for a circuit with N lines both with and without making the assumption in part (iii) [2 marks]

(b) The following tests, ABC=000 and ABC=111 are applied to the circuit shown in figure 2b. Using a fault matrix analysis determine what possible faults this would fail to detect. *[Note that this must be done by a fault matrix approach and you must show your working. Answers based on path sensitisation arguments or those that fail to show their working will receive no marks]* [10 marks]

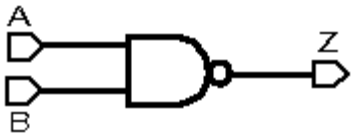

Figure 2a

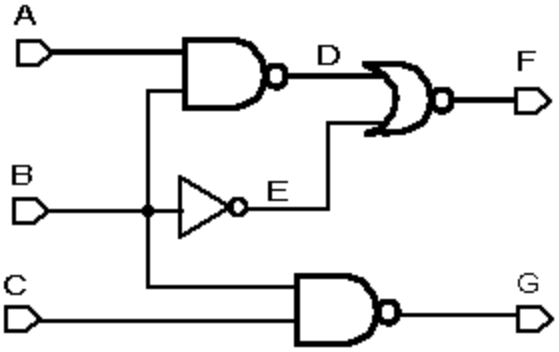

Figure 2b

3. Figure 3 shows a (to scale) plan view of a small VLSI chip with V_{dd}=5V. The gate length is 1μm. For simplicity, this has been designed with all dimensions being an integer number of microns.

(a) Draw the circuit diagram that is implemented by this chip [6 marks]

(b) Initially the inputs are set at AB=00. They are then switched to 01 and then 10. Calculate the total energy dissipated as the result of these two switching events. You may

use the information for this process provided in Table 3. *[Hint: take into account any relevant capacitances, where these might include those associated with the input and output lines.]* [10 marks]

(c) In fact, this circuit is very poorly designed and for many combinations of inputs has serious timing hazards, leading to glitches. What would the consequence of such glitches be for the power dissipation? [4 marks]

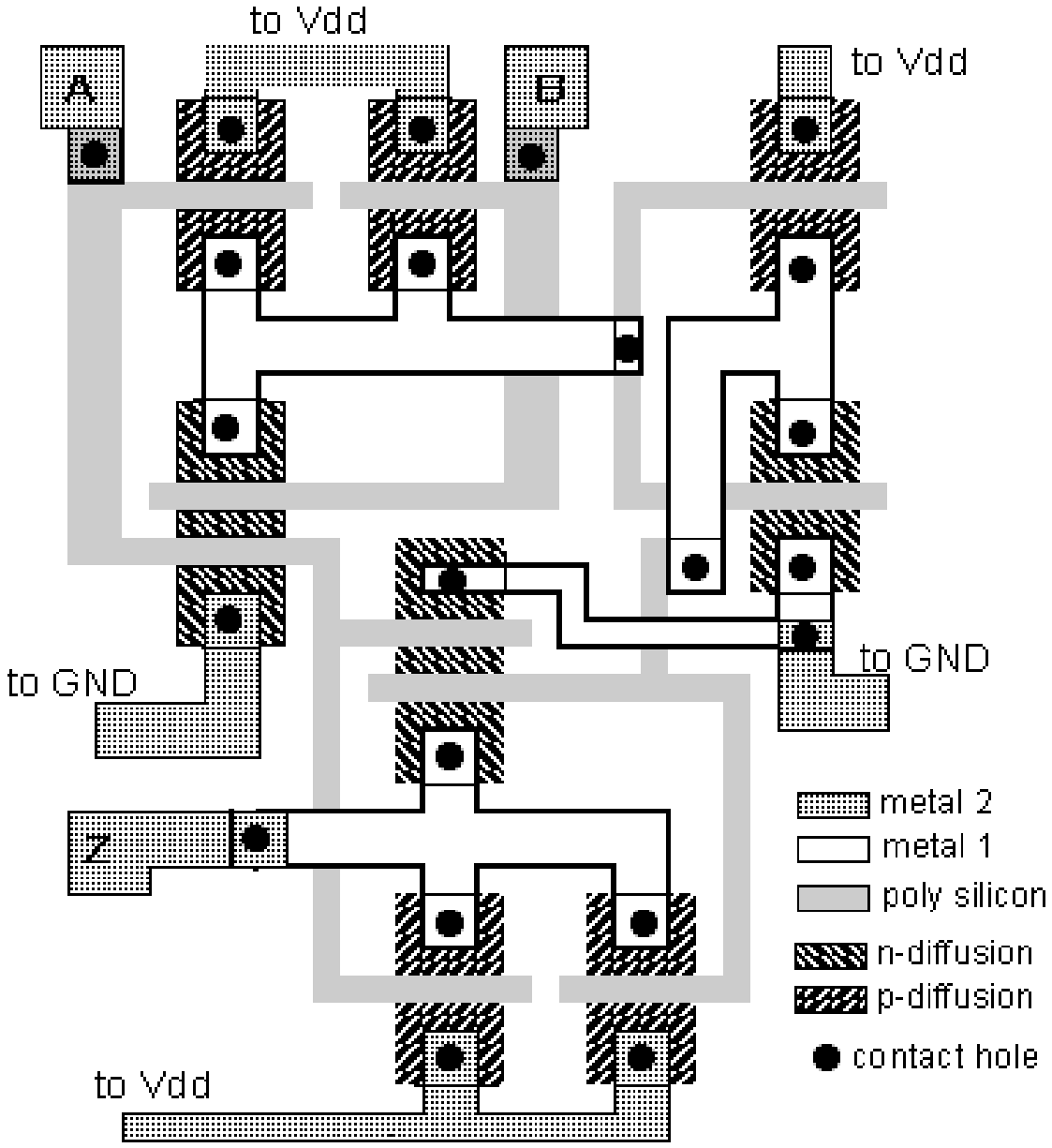

Figure 3

	Value	Comments
Cr1	$1x10^{-4}$ pF/μm^2	Routing in metal 1
Cr2	negligible	Routing in metal 2
C_{poly}	$5x10^{-4}$ pF/μm^2	Routing in poly silicon
Cg	$5x10^{-4}$ pF/μm^2	gate capacitance
Cjap	negligible	junction area capacitance (p-diffusion)
Cjan	negligible	junction area capacitance (n-diffusion)
Cjpp	negligible	junction periphery capacitance (p-diffusion)
Cjpn	negligible	junction periphery capacitance (n-diffusion)

Table 3

4. The current of the p-channel MOSFET is given by $I_{ds} = -\beta\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^2}{2}\right]$ if $V_{gs} - V_t < V_{ds} < 0$ and $I_{ds} = -\frac{\beta}{2}\left[\left(V_{gs} - V_t\right)^2\right]$ if $V_{ds} < V_{gs} - V_t < 0$. The current for the n-transistor is given by equivalent equations with appropriate sign changes. Consider a CMOS inverter with the following characteristics:
β for the n-channel transistor is 3 times larger than that for the p-channel transistor; V_{dd}=5V; V_{tn}=1V; V_{tp}=-1V.

(a) If we define a voltage V_{inv} such that if the input voltage to the inverter $V_{in}=V_{inv}$ then the output voltage $V_{out}=V_{inv}$, what is the value of V_{inv} for this inverter. *[Hint: remember that a square root has both a positive and negative solution, e.g √4=2 or –2]*
[6 marks]

(b) If the input voltage is 2V, will the n-channel transistor be in the linear or saturation region of its characteristics? Similarly, under the same conditions, will the p-channel transistor be in the linear or saturation region of its characteristics? In both cases, justify your answers. [4 marks]

(c) Calculate the value of V_{out} when V_{in}=2V. [10 marks]