Examination Feedback for EEE6206 – Power Semiconductor Devices
Spring Semester 2014-15

Feedback for EEE6206 Session: 2014-2015

Feedback: Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

General Comments:

Majority of marks were achieved on basic semiconductor device descriptions and simple calculations. Some complex phenomena, such as thermal runaway was seem to score well. Some candidates seemed to incorrectly use given formulas and failed to observe simple changes in dimensions such as microns to cm etc. The BJT breakdown equation seems to have posed problems were they failed to iterate the formulae to find the breakdown voltage at the critical electric field strength. In general, questions which required drawing band diagrams and electrical characteristics scored well, indicating the value of taught material whereas analytical questions seemed to have made some of the candidates to struggle.

Question 1:

This was on basic understanding of semiconductors. 18 candidates attempted this question, majority scored well. Thermal runaway and the definition of Fermi level were answered quite well. Generally calculation was attempted and correct answers obtained. In some cases intrinsic carrier concentration incorrectly answered.

Question 2:

16 candidates attempted this question. Most students answered q2a correctly, with some confused by terminologies used in describing technology (punch through & non punch through). Some innovative solutions were offered on how the junctions are formed; epi and implant + diffusion. Reasons why shallow n+ junctions are required (SOA) was answered incorrectly by almost all. In most cases, correct equations were selected, but, incorrect values used. Most were unclear about the differences between SiC and Si pn junctions.

Question 3:

15 candidates attempted this question. Generally most candidates drew the Schottky barrier energy diagram correctly and used this to describe the on-state behavior. On state characteristics were generally correct, some candidates were confused with soft switching characteristics of Schottky diode. Part C was generally answered correctly albeit the equivalent circuit was not given.

Question 4:

9 candidates attempted this question. Some correctly drew the IV characteristics of a BJT. Majority incorrectly identified the differences between open base breakdown and maximum breakdown voltages. Candidates did not score well on 4c, and no attempt to iterate the equation was made. The majority of student failed to implement the equation given in the question. Some correctly drew the IV curve of a thyristor, which shows some understanding of the subject matter.

Question 5:

10 candidates attempted this question. MOS structure correctly drawn. Some candidates failed to calculate threshold voltage and correctly answer question 5c. Vth calculated correctly, sometimes incorrect variable used in formulae. Generally cross-section were correctly drawn.

Question 6:

4 candidates attempted question. Differences between Power MOSFET and IGBT correctly identified as well as the differences between IGBT technologies. Latch up and minimization of this was not answered correctly as with the influence of gate resistance upon switching performance. Cross-sections on device technologies were generally correct.