Comments on EEE310/6036 Examination – June 2006

General

There was an issue raised by a number of students near the beginning of the examination concerning the quality of printing on Figure 1 (a representation of a CMOS layout). Better copies of this diagram were provided as quickly as possible. Having looked at the printed exam paper (which we do not see until the examination, unfortunately), it is certainly true that the keys for n+ and p+ diffusions were not at all clear. However, the new copies provided were more than sufficient.

In the main, the questions were reasonably well answered. However, some of the individual answers that I read did cause me to question whether I had managed to convey certain points during the course. Fortunately, there were sufficient answers that obtained close to full marks to identify that this was not generally the case.

Question 1

It is not clear whether the problem with the printing put people off answering this question (only about half of the cohort did so). This is unfortunate, because, in the main, those who did so did well.

In part a) I was surprised at how easily people coped with converting the layout into a transistor level circuit. In particular, double-gate FETs were used in the layout and whilst a few people seemed to have to think about this, they seemed to come to the right conclusion. Clearly, those who came up with the circuit had a good idea of translating it into a logical function – which is pleasing.

Part b) was less well answered – people tended to know that this is where the transistors were formed but the formation of the active area (where a thick field oxide is not grown but, instead, only a thin gate oxide layer) was only mentioned by a few people.

People tended to view the V_{DD} and V_{SS} placement in part c) as a means of keeping the nets apart – which is axiomatic in any circuit – wires that are electrically distinct must not be connected. Fewer people mentioned the formation of a well-gridded power supply to cut down IR drops and the ease of forming rows of cells in a cell-based layout process.

Question 2

This question was relatively well answered.

In part a) the diagrams for a transistor-level implementation of a latch were somewhat varied. In some cases people had a vague idea of the topology of the inverters and TGs but were a bit flummoxed as to how they connected together. In some cases, when drawing the master-slave arrangement, people showed edge-triggered device not level sensitive latched.

In part b) most people did well although, again, some of the schematics were a bit weird. For example, a NAND gate has more than one input and to show two signals converging on the same, single input pin is wrong. In sub-section iii) there were a number of people who insisted on providing an analysis for the way in which buffers increase in size – despite the fact that the question specifically says that this is not necessary.

In part c) most people could state the expression although fewer could delineate the terms. Sub-part ii) caused difficulties for people although, in essence, it is straightforward. Some people did not divide upsets/sec by $f_{clk}f_{data}$ to find p_u and **using this value** substitute it into an expression $(1-(1-p_u)^8)$. That is, $(1-p_u)^8$ is the probability of no error across 8 bits. Fewer

people, still, recognised that because p_u is so small your calculator will not cope. However, to first order, the expansion of $(1-p_u)^8$ is $1-8p_u$ + terms. So the answer is $8p_uf_{clk}f_{data}$.

Question 3

In part a) some people gave incorrect or incomplete answers. Mistaking the conditions that I explicitly identify in the lecture with the nature of the networks e.g. naturally inverting, p network – pull up, etc.

Part b) was generally answered well. Although a few people obviously got confused with the inversions necessary to find the function and started adding inverters to the output of the network!

Part c) was less well answered. Many people knew that it was a consequence of large V_{BB} for transistors at the top of a chain but only a few people bothered to identify when it gave rise to a problem. That is, when top transistor on but others below it are off but switching on.

Question 4

This question was the least well answered of the questions.

In part a) some people identified (some of) the major steps but fewer showed where the iterations came in. Other people gave details of the process of making an IC – which was not asked for.

Part b) gave rise to a range of answers – which is OK as long as the decisions are backed up by evidence. In my mind, the clear pointers are short time to market, largish market with some risk for a device of modest size and performance. I would choose FPGA as a loss-leader to get in the market and follow it up by migrating to a MGA/CBIC dependent on take-up. Some people tried to factor in the cost of building an IC fab. I've got to ask – why? IC design houses will typically buy ICs from IC manufacturers – they seldom do it themselves. Particularly, not for one modest ASIC design!