EEE336 Problem Sheet 5 – NJP (Sample Exam Questions)

Questions generally start with some bookwork to help to get you off the ground. In theory, you should be able to pass the exam just by knowing your notes! This is followed by a part where you may have to do some engineering calculations, some design, or maybe some extended bookwork. The final part is known as the *sting in the tail* and is meant to be harder than the rest of the question. It may be a more difficult aspect of something that you have seen or a completely new situation which you should be able to tackle if you know the course well.

1. **a.** What are the fundamental differences between computers with the von Neumann architecture and those with a Harvard architecture? What are the advantages and disadvantages of both architectures? In what specific application area is the Harvard architecture commonly used? **(8)**

b. What do you understand by the term *recursion* when applied to a procedure call? **(2)**

Sketch the pseudo-code for a recursive evaluation of x^n where n is a positive integer. Illustrate the operation of this code for the evaluation of x^3 by means of a call tree, tracing the calling of each recursive instance of the subroutine. **(6)**

c. In most processors, each of the possible register-to-register moves have a distinct op code; for example, the op code for A→ B is distinct from the op code for B→A, etc. Explain why this approach is adopted rather than use a single op code for a register-to-register move and then specifying the source and destination registers as operands. **(4)**

2. **a.** Outline the process whereby two floating point numbers are added together. **(4)**

b. Calculate 1111_2 divided by 100_2 by non-restoring division. The data values must all be held in byte wide storage locations **(8)**

c. In the context of procedure calling, what are the differences between passing parameters by value and by reference? What are the comparative advantages and disadvantages of both methods? **(8)**

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3. **a.** Sketch a possible hardware implementation of a serial shift-and-add multiplier (using a parallel adder) for multiplying two n-bit numbers. Carefully describe the initial circuit conditions. **(5)**

For the more general case of multiplying an m-bit multiplicand by an n-bit multiplier, how long will it take to generate the product? **(2)**

Outline the operation of a serial shift-and-add multiplier with reference to the multiplication of two unsigned integers, 110_2 by 101_2 using a table to show the states of the circuit at each stage. **(5)**

b. Using the example of 110_2 multiplied by 011_2 (where 110_2 is the multiplicand and 011_2 is the multiplier) describe how basic shift-and-add multiplication can be extended to handle multiplication of a signed multiplicand by an unsigned multiplier **(4)**

c. Rather than forming partial products by successively left-shifting the multiplicand, an alternative implementation for a shift-and-add multiplier is to right-shift the accumulated partial product after each stage. What are the advantages of this method? **(4)**