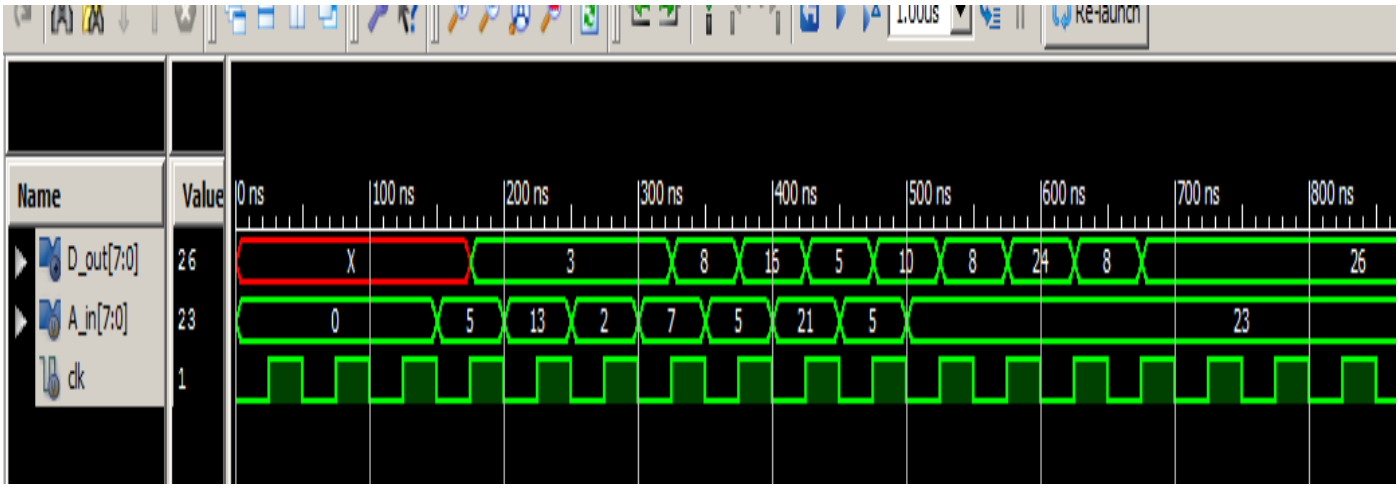
EEE339/336 Solution Sheet 1 - NJP

1. a) 100100001 b) 11010110
2. a) 01011011 + 10111010 = 00010101 b) 01101011 + 11010101 = 01000000
3. A&B = 00010100, A|B = 11110111, A^B = 11100011, &A = 0, |A = 1 , ^A = 0
4. **wire** – net data type, used for connections in Verilog designs, does not store any data, must be driven, default type
   reg – variable data type, used as a storage element, stores value between assignments, holds its value until a new assignment is made
5. **initial** procedure – executes once only, never repeats, single-pass behaviour
   always procedure – cyclic behaviour, executes whenever there is an event on its sensitivity list
6. **blocking assignment** (=) – evaluated and assigned in a single step, execution flow in the procedure is blocked until the assignment is completed, statement must be executed before the execution of the statements that follow
   nonblocking assignment (<=) two stage evaluation, right hand side evaluated immediately, assignment to left hand side is delayed until other evaluations in the current time step are completed, flow not blocked, allows several register assignments to be made in the same time step, no dependence on the ordering of statements
7. The nonblocking model gives the correct behaviour. Nonblocking assignments correctly model the registers as the update does not happen until the end of the simulation step.
   The blocking assignments each complete before the next is executed so the data at A ripples through to the output during a single simulation step.

Nonblocking – output samples appear after 4 rising clock edges



Blocking assignment – data appears on next rising edge