EEE225 Problem Sheet 1 Solutions - NJP

1.

rise time approx 3.5ns
fall time approx 2.5ns

remember to use the 10% and 90% points

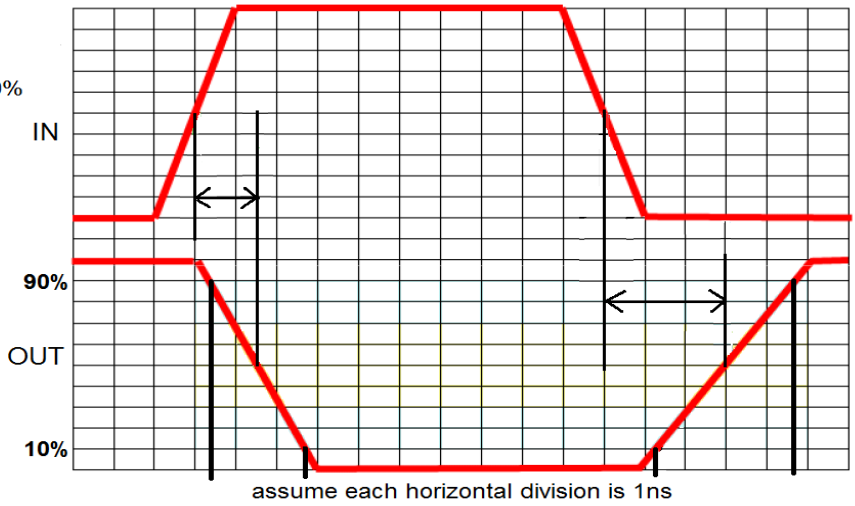
for the propagation delay, use the 50% points

t_{phl} = 1.5ns

t_{plh} = 3 ns

$tp = \frac{1.5 + 3}{2}$

= 2.25ns

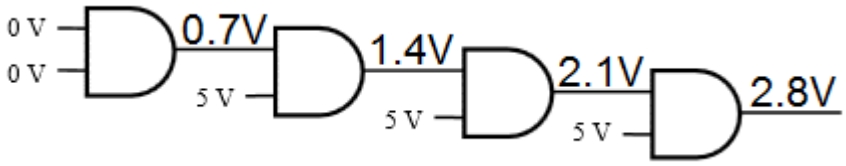


Note: Rise time and fall time here relate to the output response.

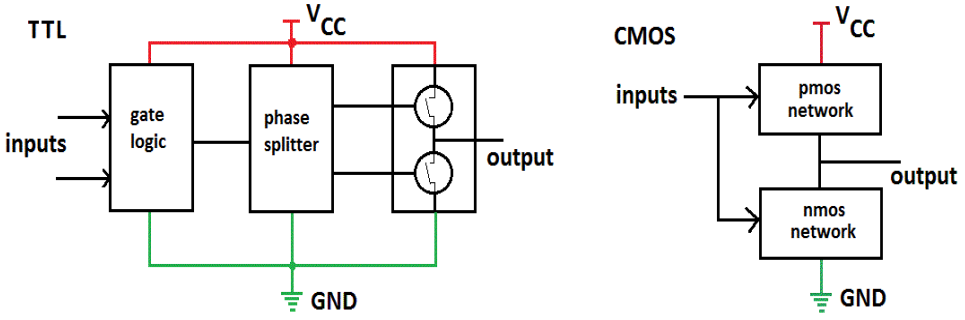
2. See notes for pulse shape. Ringing is an unwanted oscillation of the pulse which happens in response to a sudden change. It is caused by resonance due to parasitic capacitances and inductances in the circuit.

3. LV-A has lowest leakage current Icc = 20µA hence lowest static power dissipation.

4. The circuit has failed because the output voltage for the last two gates is in the forbidden area and hence the logic level is undefined.



5.



Turn Over

TTL – the first structural block implements the required logic. The second block is a phase splitter which is required to drive the final block which is a totem-pole output stage. In contrast, a CMOS logic gate consists of a pmos pull-up network to the positive supply rail and an nmos pull down network to ground.

6. In the case of TTL the gate logic consists of a multi-emitter transistor and the number of emitter connections would be increased from two to four. In the case of CMOS, an additional transistor in both the pull-up and pull-down network would be required for each extra input.

7.

original

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

modified

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Original circuit implements $F = \overline{A}.\overline{BC}$

Modified circuit uses a diode logic AND gate to replace the input which was originally pulled high with the AND of B and C.

$$F = \overline{\overline{ABC}.\overline{BC}}$$
$$= (\overline{A} + \overline{B} + \overline{C})(\overline{B} + \overline{C})$$
$$= \overline{A}\overline{B} + \overline{A}\overline{C} + \overline{B}\overline{B} + \overline{B}\overline{C} + \overline{B}\overline{C} + \overline{C}\overline{C}$$
$$= \overline{A}\overline{B} + \overline{A}\overline{C} + \overline{B} + \overline{B}\overline{C} + \overline{C}$$
$$= \overline{B}(\overline{A} + 1) + \overline{C}(\overline{A} + \overline{B} + 1)$$
$$= \overline{B} + \overline{C}$$
$$= \overline{\overline{B} + \overline{C}}$$
$$= \overline{BC}$$

If Bodge It Circuits Inc. had trusted to Boolean algebra, they would have discovered that the required functionality reduced to the NAND of B and C. They could have simply taken the output from NAND2 at no extra cost in components.