1. Multiply the two unsigned binary numbers: 1011 x 1010 using the basic school (shift-and-add) multiplication method. Trace through the operation of the serial multiplier circuit described in the lecture for this. Form a table representing the state of the circuit at every time interval just before the edge of the clock.

Time Step	Contents of 2n-bit wide multiplicand shift register	Multiplier shift register	Output of adder	Contents of 2n-bit wide accumulator register
1	…	…	…	…

   Identify the corresponding states in the hand calculation above and the hardware implementation.

2. With reference to the product of two 3-bit numbers, show that basic shift-and-add multiplication does not work for 2s-complement numbers. (Hint: Consider the weightings associated with the digits of a 2s-complement number.

   i) Can you suggest a modification to the basic shift-and-add method that would make it work with negative multiplicands?
   ii) Can you suggest a modification to give the correct answer for negative multipliers?

3. Trace through the operation of the serial divider circuit described in the lecture for 010111 ÷ 0110. Form a table representing the state of the circuit at every time interval just before the edge of the clock.

Time Step	Contents of dividend register	Contents of divisor shift register	Output of subtractor	Input to quotient shift register
1	…	…	…	…

   Identify the corresponding states in the hand calculation above and the hardware implementation.

4. Divide 1010 by 0101 using restoring division. (Set your result out as a table)

5. Calculate 1101 ÷ 110 by non-restoring division. The data values must all be held in byte wide storage locations. Tabulate each of the calculation steps.

6. Using non-restoring division, sketch a circuit to perform combinatorial division on two 3-digit binary numbers. Comment on the speed of operation of this circuit as the width of the operands increases.

7. Prove that the 2s-complement of the 2s-complement of x is equal to x.