Sequential Logic Design

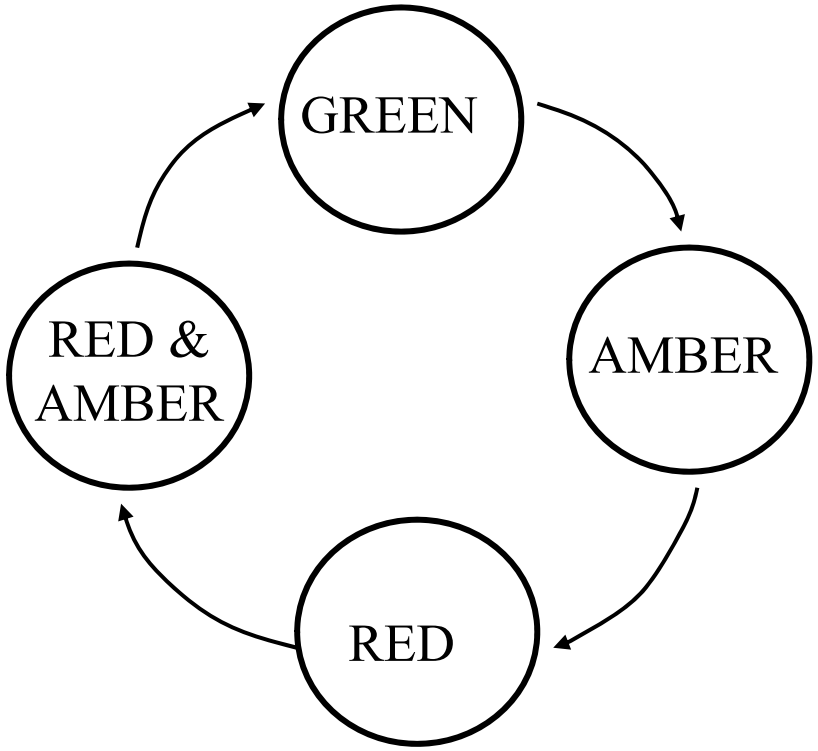
- System States
- State Diagrams & Transition Tables
- Sequential Circuit Analysis
- Sequential Circuit Design

System States

The state diagram shows a traffic light sequence with four states.

The states are represented by circles and the transitions between the states by directed arrows.

For a synchronous system, movement between states will happen when an active edge from a free running clock is applied.



Sequential Circuit States

- At any point in time, a sequential circuit can be said to be in a certain **state**.
- The state is defined by the outputs of the flip-flops in the sequential circuit.
- In a synchronous sequential circuit, movement between states only occurs in response to a clock edge.
- A state diagram can be used to graphically show the progression from one state to the next.
- The state is represented by a circle and the transitions between states are represented by directed lines joining one state to the next.

State Diagrams

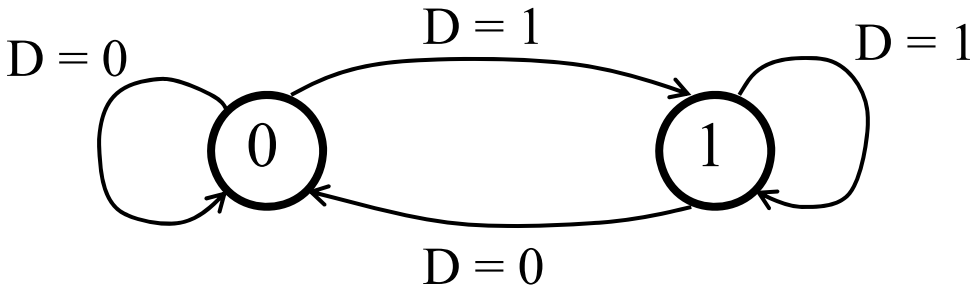
The state of a single flip-flop is one of the two stable conditions that the output can take (**0** or **1**).

A state diagram can be used to graphically show the progression from one state to the next. The state is represented by a circle and the transitions between states are represented by directed lines joining one state to the next.

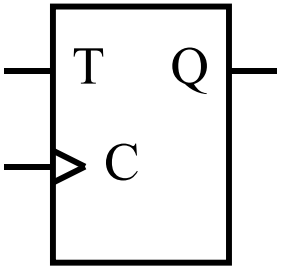
Consider the D-Type flip-flop:

D	$Q_{(next)}$
0	0
1	1

$Q_{(next)} = D$

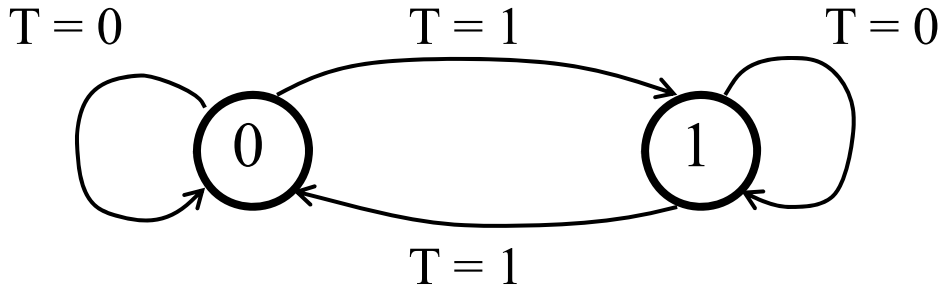


T-Type Flip-Flop

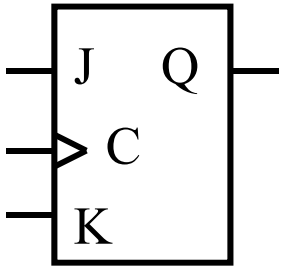


T	$Q_{(next)}$	
0	Q	← unchanged
1	$\overline{Q}$	← Toggle

$$Q_{(next)} = T.\overline{Q} + \overline{T}.Q$$

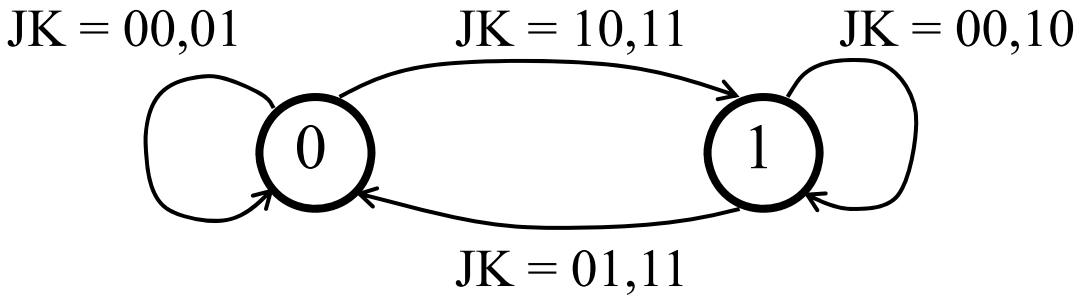


JK Flip-Flop



J	K	$Q_{(next)}$	
0	0	Q	← unchanged
0	1	0	← reset
1	0	1	← set
1	1	$\overline{Q}$	← Toggle

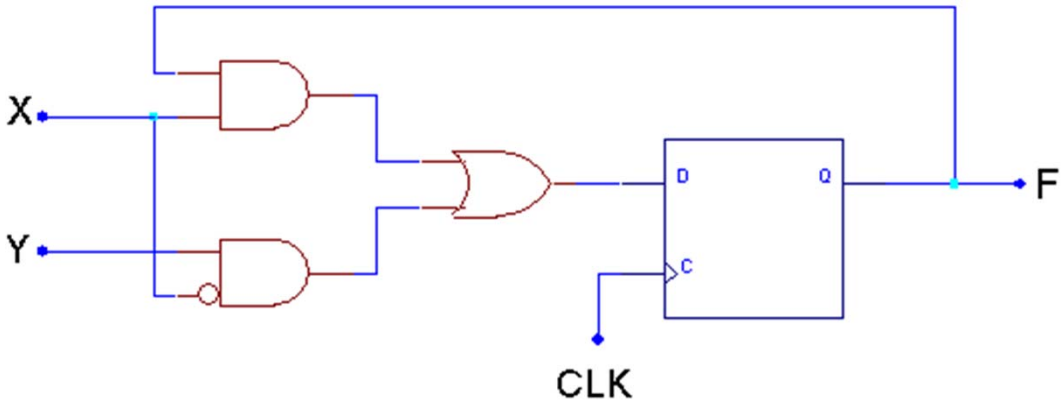
$$Q_{(next)} = J\overline{Q} + \overline{K}Q$$



Analysis of Clocked Sequential Circuits

The output of a clocked sequential circuit depends upon its inputs and the state of the flip-flops. Its behaviour can be described by a state equation (sometimes called transition equation). Consider the circuit below.

The next state of F, one clock edge later, is denoted by $F(t + 1)$.



$$F(t + 1) = F(t).X(t) + Y(t).\overline{X}(t)$$

The right hand side is the Boolean expression that will make the next state equal to '1'. It is usual to omit the designation (t) giving:

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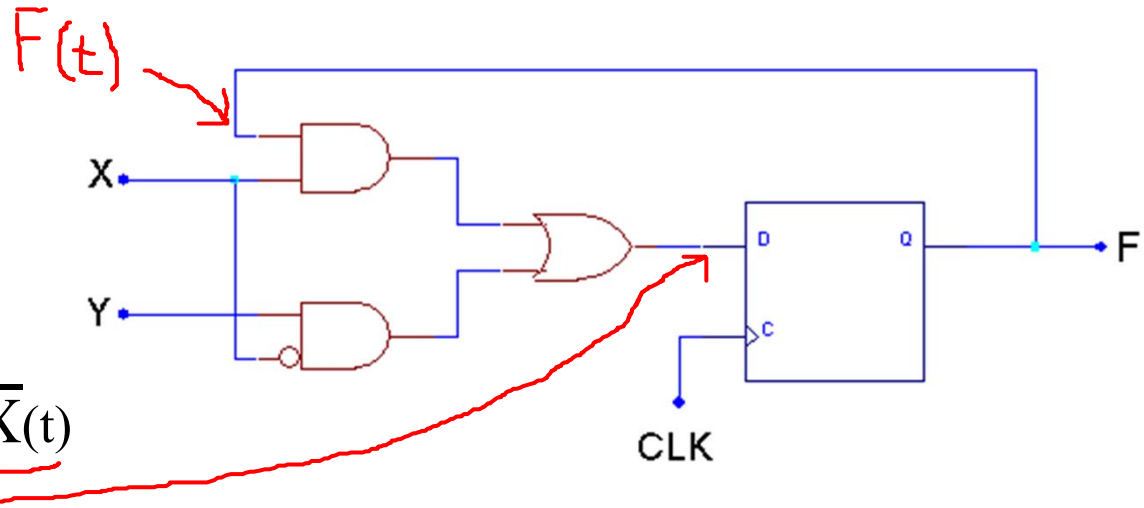

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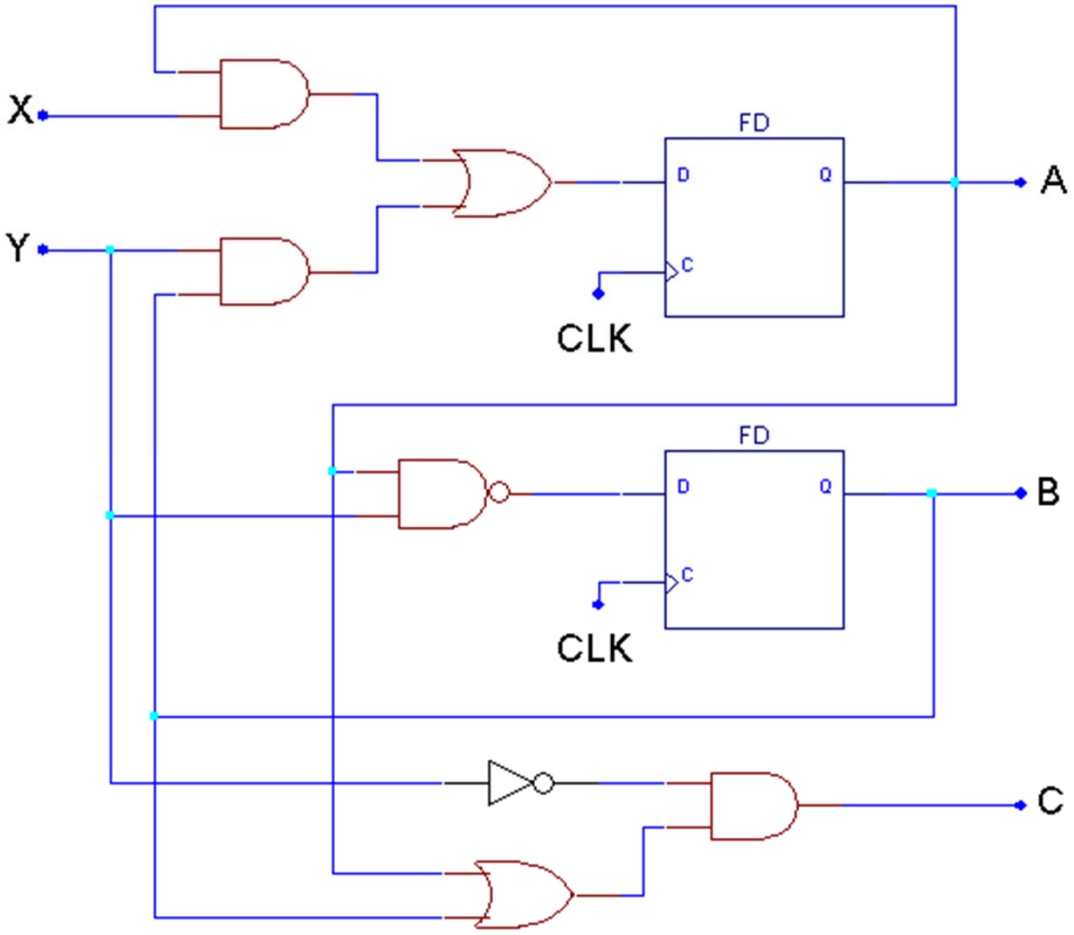
Write down state equations for A,B,C.

Remember $Q_{(next)} = D$



$A_{(t+1)} =$

$B_{(t+1)} =$

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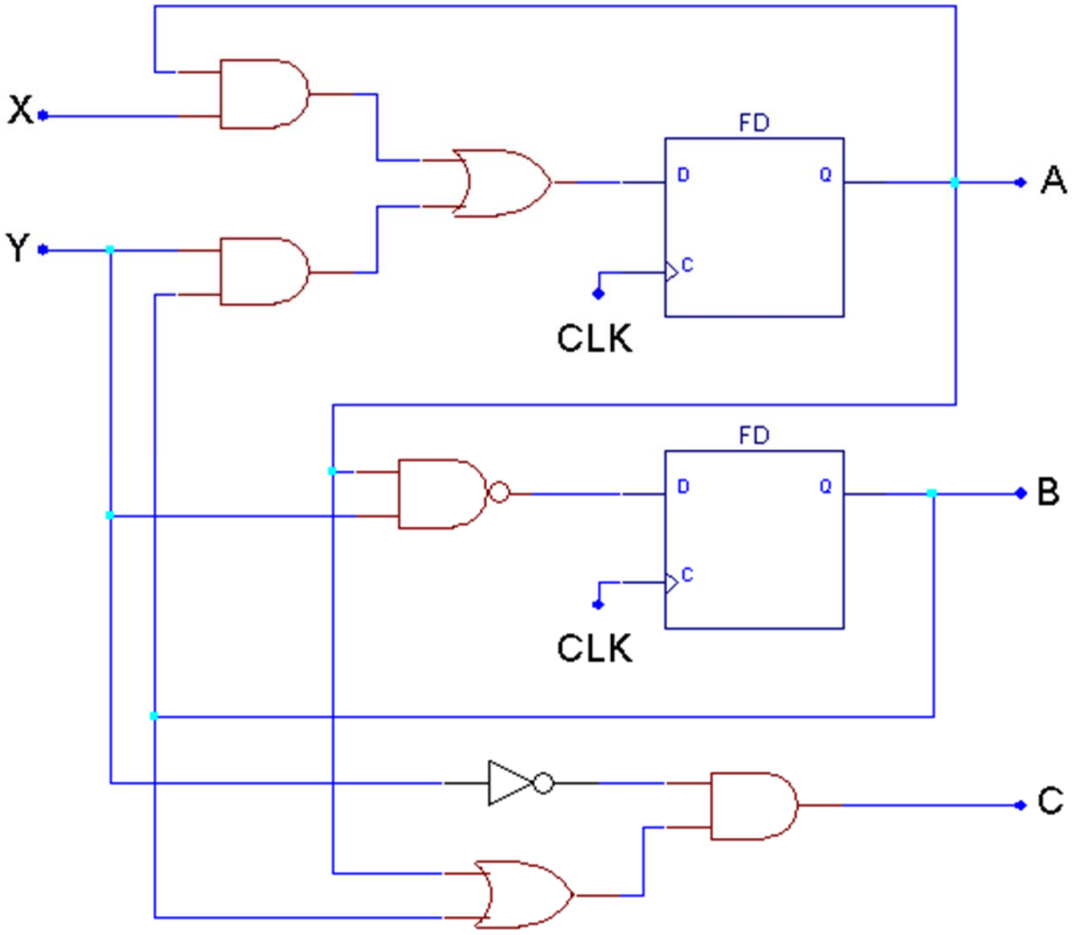

$$A_{(t+1)} = A.X + Y.B$$

$$B_{(t+1)} = \overline{A.Y}$$

$$C = \overline{Y}.(A + B)$$

State Tables

The time sequence of inputs, outputs and flip-flop states can be represented by a state table (sometimes called state transition table).

$$F(t+1) = FX + \overline{X}Y$$

A sequential circuit with m flip-flops and n inputs needs 2^{m+n} rows in the state transition table.

A state table is a truth table that takes into account the time dependant nature of a synchronous sequential circuit.

Present State	Input	Next State
F	X Y	$F_{(t+1)}$
0	0 0	0
0	0 1	1
0	1 0	0
0	1 1	0
1	0 0	0
1	0 1	1
1	1 0	1
1	1 1	1

Sequential Circuit Design

A synchronous sequential circuit is required with two inputs **D**, **E** and one output **Q**. The output will be unchanged when the enable signal E is '0' and will take the value of the D input when E = '1'.

First, produce the state table:

present state Q	Inputs E	Inputs D	next state $Q_{(t+1)}$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
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Then solve for Q(t+1):

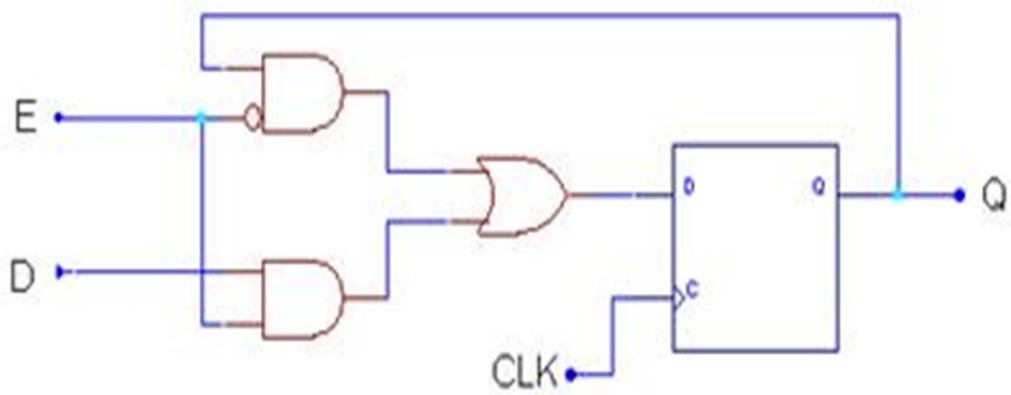
$$Q(t+1) = \overline{Q}ED + Q\overline{E}\,\overline{D} + Q\overline{E}D + QED$$

$$Q(t+1) = Q\overline{E}(\overline{D} + D) + ED(\overline{Q} + Q)$$

$$Q(t+1) = Q\overline{E} + ED$$

State Equation: $Q(t+1) = Q\overline{E} + ED$

The state equation gives the combinational logic that is required as the input to the D-type flip-flop. This will then give the required next state after the next active clock edge.



In this example, we have produced a D-type flip-flop with enable. The logic circuit is that for a 2-to-1 multiplexer. The enable line **E** selects between keeping the same state when **E = 0** or clocking in a new value for D when **E = 1**.

Summary

- Sequential circuit outputs depend upon current and previous inputs.
- Changes in synchronous sequential circuits happen on active clock edges.
- There are three types of flip-flop : D-type, T-type and JK
- D-Type flip flops are generally used for sequential design.