Data Provided: List of reliability models

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2009-2010 (2 hours)

Reliability and Failure 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. The failure data from a group of 10,000 MOS capacitors is shown in figure 1.1. The data can be fitted using a Weibull model with the constant β = 0.5 as shown in figure 1.1.

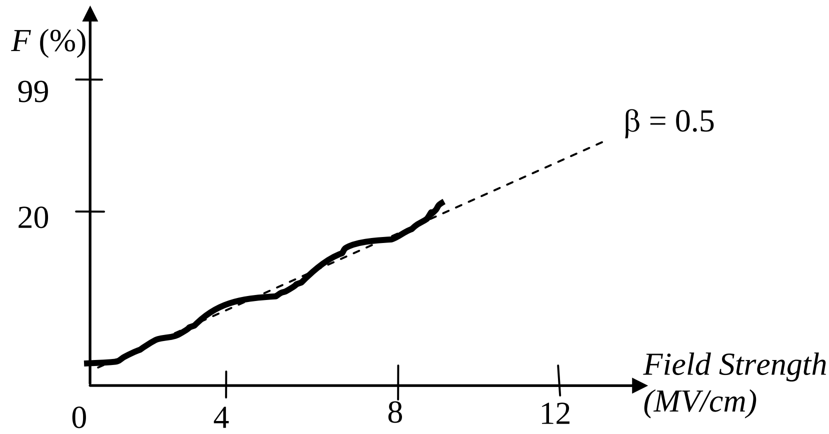


Figure 1.1

i) Discuss the failure trend and suggest a possible cause of these failures. **(3)**

ii) Propose and explain two prevention methods for the failure mechanism suggested in part a(i). **(4)**

1. **b.**

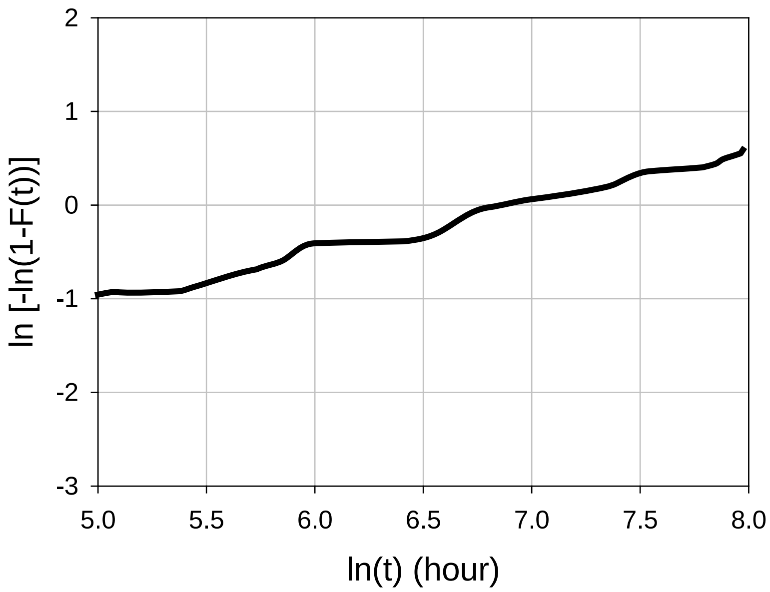


Figure 1.2

A reliability test on a group of MOSFETs at 100^{o}C yielded the failure data shown in figure 1.2.

i) Recommend an appropriate model for these devices and work out the model parameters. **(4)**

ii) Estimate the time when 60% of the devices will fail. **(2)**

iii) Obtain the failure rate at 150 hours, 500 hours, 800 hours and 1200 hours. **(4)**

iv) Using your answers from part b(iii) sketch and label the failure rate as a functioin of failure time. Suggest a possible cause of failure in these devices. **(3)**

2. **a.** Al is commonly used to form ohmic contacts on Si devices. However the Al-Si contacts are generally prone to failure at high temperature. Explain why. **(5)**

b. i) Pure Al interconnects deposited on Si devices show higher electromigration failure than alloyed interconnects based on Al-Cu(4wt%)-Si(1.7wt%). Discuss the benefits and disadvantages of adding Cu and Si in the metallization scheme. **(5)**

ii) In an electromigration failure test the data was analysed using a lognormal distribution. It was found that for pure Al, t_{50} = 85 hours and σ = 0.32, while for Al-Cu-Si t_{50} = 5600 hours and σ = 0.22. Sketch and label the failure probability on the lognormal graph paper provided. **(4)**

iii) Estimate the times when 80% of Al and Al-Cu-Si interconnects will fail. **(2)**

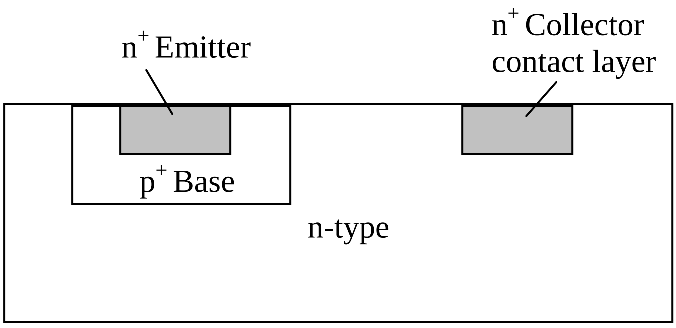
c. Suggest four measures to minimise electromigration failure. **(4)**

3. **a.** Sketch a schematic diagram of a scanning acoustic microscope (SAM) and explain how it works. **(6)**

b. A range of frequencies can be used to detect failure mechanisms in ICs. Discuss the characteristics of SAM when used at (i) low frequencies (<100 MHz) and (ii) high frequencies (>100 MHz). **(4)**

c. Give an example of failure mechanism that can be detected using each of the frequency bands in part (b). **(2)**

d. Consider a planar diffused Silicon bipolar junction transistor shown in figure 3.1. The emitter and collector were contaminated by Cu during the fabrication stages.



i) Suggest an appropriate technique to analyse these contaminants. Explain how the technique you suggested works.

ii) Identify two 2 limitations of the technique suggested in part d(i) and list one reliability issue introduced by Cu contamination. **(8)**

4. **a.** Describe 2 physical mechanisms that degrade Si MOSFETs and GaAs MESFETs under radiation of high energy particles. **(7)**

b. i) What is meant by a Single Event Upset (SEU) in digital electronics? **(2)**

ii) One hundred FPGAs were tested for soft errors in different locations and at different elevations in Albuquerque, New Mexico and on White Mountain, California. The test yielded mean time to event (MTTE) of 38,000 hours and 7500 hours at Albuquerque and White Mountain respectively. Explain the reason for the significantly smaller MTTE obtained on White Mountain. **(2)**

iii) Discuss how reduction in device dimensions will affect SEU. **(4)**

c. Identify the 2 main sources of the high energy particles. **(2)**

d. Outline 3 methods to reduce SEU. **(3)**

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