SOLNS 2002

Electronic Devices

[redacted]

1

1. Bookwork: This should be straightforward for most students.
Electrons have a random thermal motion. Since they move in random directions, any point where the density changes with distance will experience a net flux away from the high concentration region towards the lower concentration region. This is because the concentration from which the concentration originates determines the magnitude of the flux. A diffusion current will flow which tends to equalise any non-uniformities 1 [4 marks]

Since the net flux is proportional to the concentration difference between to the two regions, it follows that the diffusion current density is proportional to the gradient of concentration. 2
i.e.

$$J_{diff} \propto e\frac{dn}{dx} \quad 2$$

[3 marks]

The electronic charge is included to convert from particle flux to charge flow. 2
The constant of proportionality is the diffusion coefficient, D. [2 marks]

Since the temperature, T, increases the random thermal motion $D \propto T$ 2
The ease of movement of the random motion must be determined by the mobility, μ. 2
Thus,

$$D \propto \mu T \quad 1$$

[3 marks]

Bipolar transistor: More demanding bookwork,
The excess minority electrons in an npn bipolar will diffuse towards the collector where the concentration is zero. As they diffuse they will tend to recombine with the majority holes in the base. For good gain, nearly all the injected electrons are required to reach the collector. [4 marks]

1 injection
1 diff → coll
1 recomb
1

Problem: If there is no recombination the concentration profile of electrons across the base is linear.
The electron concentration at the emitter end (x=0) is 2e22. At the collector end (x=3e-6) n=0.
Thus dn/dx=2e22/3e-6=6.67e27 m-4
D is given as 0.008 so J=eD dn/dx = 1.6e-19 . 0.008 . 6.67e27 = 8.53e6 Am-2 [4 marks]

2. Bookwork: Should be straightforward for reasonably able students

A parallel plate capacitor has two conducting metal plates separated by a region of dielectric material. The depletion region of a pn junction is also a dielectric. It is insulating because it is depleted of free carriers and separates two conducting regions (n and p type). The only difference is that a pn junction has a space charge inside the depletion region which replaces the charge normally found on the capacitor plates.

dielectric

~~plates~~ ?

2

In both cases $C = \dfrac{\varepsilon A}{d}$ 1 [6 marks]

As the reverse bias increases the depletion depth increases to support the higher voltage

$d \propto \dfrac{1}{V^{1/2}}$ Hence from the above $C \propto \dfrac{1}{V^{1/2}}$ [2 marks]

Calculation: This first calculation is very simple provided the students understood the above. I expect most diligent students to be capable of this.

$C = \dfrac{\varepsilon A}{d}$ =1.4e-10 * 0.25e-6 / 3e-6 =1.17e-11 F = 11.7pF [4 marks]

The second part of the calculation is more demanding and I expect this to stretch all but the most able students

$$C \propto \frac{1}{V^{1/2}} = \frac{C'}{V^{1/2}}$$

$$C' = CV^{1/2} = 10e-12 * 4^{1/2} \Rightarrow 2e-11$$ 3

at the new voltage V=4.5

Therefore

$$C = \frac{2e-11}{4.5^{1/2}} = 9.43pF$$

i.e. the capacitance reduces by 0.57pF [6 marks]

This demands synthesis of ideas and is therefore demanding for first year students:

Since d is smaller for higher doping, the capacitance can be increased by increasing the doping density in either or both sides of the junction.

[2 marks]

3 This is standard bookwork.

For a good mark a student should include

JFET

The JFET comprises a current path from S to D whose width is controlled by a depletion region formed by the gate region of opposite type. Carriers are driven from S to D by Vds. As Vds increases a potential drop along the channel gradually increases the reverse bias of the gate (at the D end of the channel) gradually increasing the depletion region width restricting the channel. Eventually the channel is pinched off and the drain current saturates. Increasing the gate voltage causes pinch off to occur at lower voltages since the channel is already partially depleted. [5 marks]

MOSFET

Without a gate bias the channel does not conduct since we have effectively back to back diodes. However a positive bias (assuming an n-channel MOSFET) depletes the positive charges under the gate by repelling the holes. Eventually the positive charge is so large that electrons flow in from the S and D to under the gate to form a channel. The amount of charge in the channel (and therefore the current) is modulated by the gate bias. [5 marks]

JFET
1) Carriers S → D by Vds
2) Controlled by depletion width
3) V_{gs} controls depth
4) ~~Pinch off~~. Depletion dep on V
5) pinch off.

MOSFET
~~Start~~ How induced channel. 2
Amount of channel charge ~~...~~ by Vgs
No current without channel. 1
High input impedance 1

Derivation:

Resistance of the channel $R = \dfrac{\rho . l}{bW}$

$\therefore \dfrac{1}{R} \propto b$ where R is the resistance with a gate bias and

$\dfrac{1}{R_0} \propto a$ where R0 is the resistance with no gate bias

The ratio of these two will therefore be given by

$$\frac{R_0}{R} = \frac{G}{G_0} \frac{b}{a} = 1 - \left(\frac{V_g}{V_p}\right)^{\frac{1}{2}}$$

also

$$I_d = GV_d \quad \text{(Ohm's Law)}$$

$$I_d = G_0 \left[1 - \left(\frac{V_g}{V_p}\right)^{\frac{1}{2}}\right] V_d$$

[5 marks]

Problem:

$$G_0 = \frac{1}{500}$$

$$\therefore \frac{G}{G_0} = \frac{500}{1000} = 1 - \left(\frac{2}{V_p}\right)^{\frac{1}{2}}$$

$$\Rightarrow V_p = 8V$$

Now to calculate I under the given condition

$$I_d = \frac{1}{500}\left[1 - \left(\frac{3}{8}\right)^{\frac{1}{2}}\right] 10 = 7.75mA$$

[5 marks]

Q 4 (cont.)

At reverse bias $I = I_0 = 10\,\mu A = 10^{-5}\,A$

$\therefore$ diode equation $I = 10^{-5}\left(\exp\frac{eV}{kT} - 1\right)$

$$= 5\times10^{-2}$$

$$\Longrightarrow \quad V = \frac{kT}{e}\ln(5001)$$

$$= \frac{293\times1.38\times10^{-23}}{1.6\times10^{-19}} \times 8.52$$

$$= \underline{0.215\,V}$$ 4

Use $R = \frac{\rho l}{A} = \frac{l}{\sigma A}$ (given on question paper)

p side $\quad R_p = \frac{10^{-3}}{2\times10^{3}\times0.5\times10^{-6}} = 1\,\Omega$ 2

n side $\quad R_n = \frac{10^{-3}}{5\times10^{2}\times0.5\times10^{-6}} = 4\,\Omega$ 2

Voltage dropped across these resistors

$$= 50\,mA \times 5\,\Omega = 0.25\,V$$

$\therefore$ Total terminal voltage $= 0.25 + 0.215$

$$= \underline{0.465\,V}$$ 4

n_i^2 term in equation (2) relates to the bond strength

2

24.

From equation (2) first term is the hole current and second term is the electron current contribution. 2

Since both these components are multiplied by $\left(\exp \frac{eV}{kT} - 1\right)$ ratio is given by

$$\frac{J_e}{J_h} = \frac{D_e}{L_e N_a} \cdot \frac{L_h N_d}{D_h} \qquad 2$$

to further reduce these $D_{e,h} \propto \mu_{e,h}$

also $L_h \approx L_e$

$$\therefore \frac{J_e}{J_h} \approx \frac{\mu_e}{\mu_h} \cdot \frac{N_d}{N_a} = \frac{\sigma_n}{\sigma_p} \quad \text{(ratios of conductivities}$$

2

$\sigma_n = n e \mu_e$

$\sigma_p = p e \mu_h$)

This ratio is important in the emitter/base junction of a bipolar transistor. Since electrons injected into the base of an npn transistor contribute solely to the collector current and reverse injection of holes from the base 2 contributes to the base current and the latter has to be reduced by doping up the emitter with respect to the base.