Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2006-2007 (2 hours)

Integrated Circuit Technology 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

1. a. State the electronic configuration of the Si atom. For the Si crystal lattice, give the Si orbital hybridisation, outline the nature of the Si-Si bonds and briefly describe the energetics of bond formation. **(4)**

b. The lattice parameter of a crystalline semiconductor with the diamond cubic structure is $a_0 = 0.5522$nm. Calculate the spacings of the following planes: (002), (112), (212) and (114). Give values in nanometres to four decimal places accuracy. **(4)**

c. Calculate the angles between the following pairs of planes in the diamond cubic lattice:

(001) and (011)

(111) and (112) **(3)**

d. By the use of diagrams, explain the differences between an intrinsic stacking fault, an extrinsic stacking fault and a twin in the diamond cubic lattice. **(3)**

e. With the aid of a diagram, show the dislocations which exist in a tilt grain boundary: what character do these dislocations have? Name two other types of grain boundary which can be found in the diamond cubic lattice: do either of these exhibit a single type of dislocation and, if so, what is this? **(3)**

f. Metal interconnect tracks are to be fabricated on an oxide surface. Before patterning is carried out, the sheet resistance of the metal is measured to be 0.4Ω/□. Calculate the resistance of final tracks that are 3mm long and have widths of 1 and 5μm. **(3)**

2. **a.** Describe the apparatus and processes required for the chemical vapour deposition of epitaxial Si. Indicate the way in which the deposited material is doped and comment on factors that affect layer quality: include diagrams of the apparatus and of the range of deposition chamber designs. **(10)**

b A Si epitaxial layer is grown by CVD upon a Si substrate at a temperature of 1100°C. If the layer growth rate is 0.4μm/min and the substrate is heavily doped with boron, deduce by calculation whether autodoping of the layer would be expected to be a problem. You may assume that the activation energy for boron diffusion (E_A) is 3.46eV, the boron diffusion pre-exponential factor (D_0) is 0.76cm^2/s and Boltzmann's constant (k) is 8.62x10^{-5}eV/K. **(6)**

c. If epitaxial Si is deposited upon sapphire, rather than upon Si itself, how does the layer grow and what structural differences would you expect to find in the grown layer? What is the possible use of Si layers on sapphire? **(3)**

d. What modification must be made to the deposition conditions for Si on Si in order to give (i) polycrystalline Si and (ii) amorphous Si? **(1)**

3. **a.** Describe, with the aid of suitable diagrams, the processing sequence that can be used to fabricate a basic n-p-n bipolar transistor. Explain fabrication constraints or special conditions associated with any buried conducting layer, epitaxy that may be necessary, the base width and contact, together with the emitter region and contact. **(14)**

b. The first stage in a transistor fabrication requires the formation of an n-type tub in the p-type wafer. A shallow implant of As is first carried out using 10 keV ions. The impurity is then driven in by a 30min anneal at 1200°C. Calculate the characteristic diffusion length of the impurity as a result of this anneal. The diffusion pre-exponential factor (D_0) may be taken to be 12cm^2/sec, with an activation energy for diffusion of 4.05eV: Boltzmann's constant (k) is 8.61x10^{-5}eV/K. **(6)**

4. **a** Describe the processes by which Si can be thermally oxidised and outline the reaction kinetics in terms of rate-limiting steps. List the factors that can adversely affect the gate oxide integrity of a MOSFET. How can potential metal contamination be controlled during Si oxidation and what is the nature of the defects which form in the Si if such contamination is present. **(12)**

b. Describe the processes by which Si oxide and nitride can be deposited. Note the advantages and disadvantages of the different methods. **(8)**

AGC / PAH