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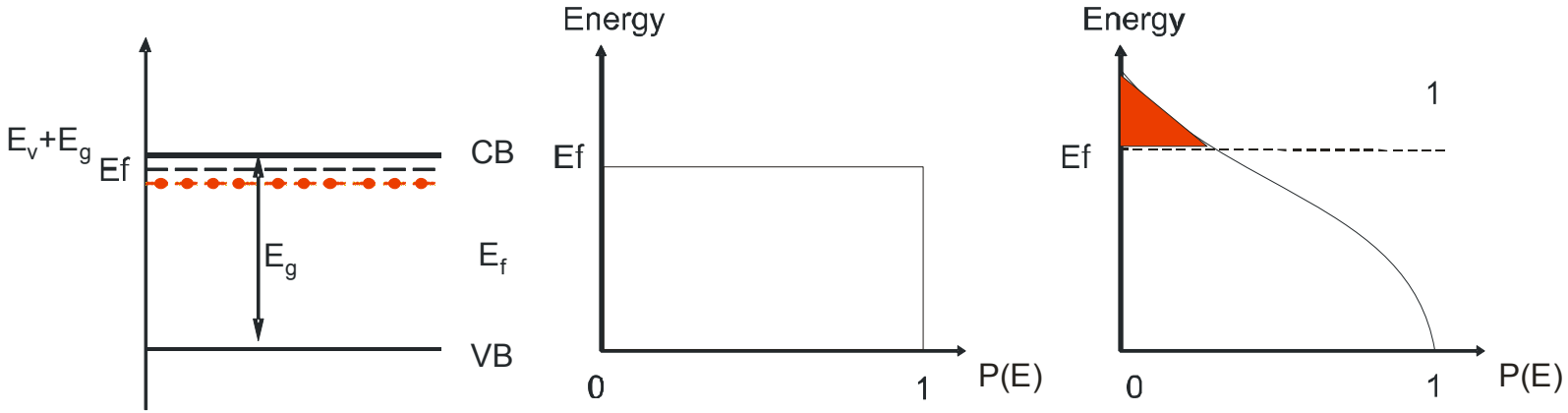
Energy bands & Occupation

Position of the Fermi Level in Doped Semiconductors

Intrinsic semiconductor E_f is mid-gap, Eg/2 because $n=p=n_i$

n-type material is characterised by n(C.B.) >> p(V.B.)
$n=10^{22}$ m-3 $p=10^{10}$m-3

Some CB states are full, only a few VB states are empty. Since E_f is the probability of occupation this is accounted for by E_f moving up to bottom of C.B.



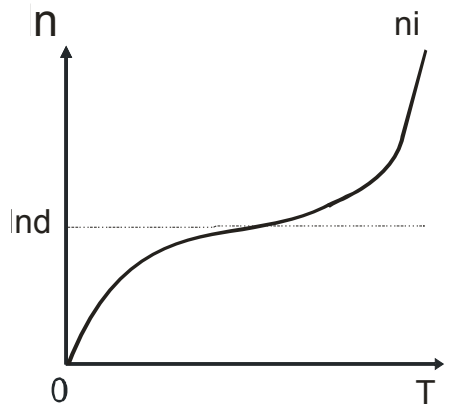
T=0K T=300K

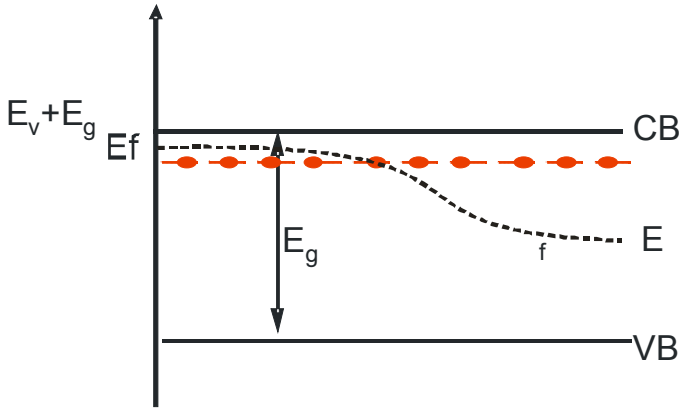
At T=0K, possibility of V.B. electron crossing Eg is negligible. As T ↑ from 0K, first electrons to reach C.B. come from donor levels, - so behaves like intrinsic semiconductor with gap reduced to Ei and E_f located at the middle of this gap.

Energy bands & Occupation

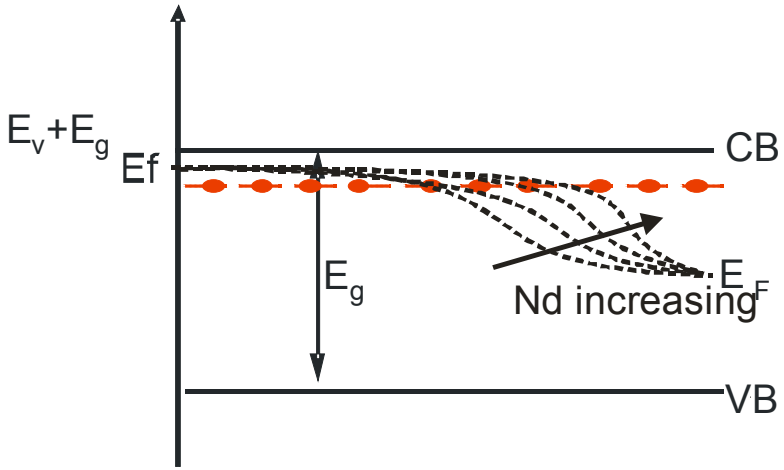
At high T (>300ºC), intrinsic carriers come in to play.
Then n = N_d + 'intrinsic' electrons.This is significant when kT>>E_g

Intrinsic carriers become more dominant, as T ↑ E_f moves to mid-gap.





As Nd ↑ , 'intrinsic' behaviour sets in at higher temperatures



Precise position of E_f is by calculation.

σ_i can be higher than σ_n at very high temperatures, so not true extrinsic behaviour.

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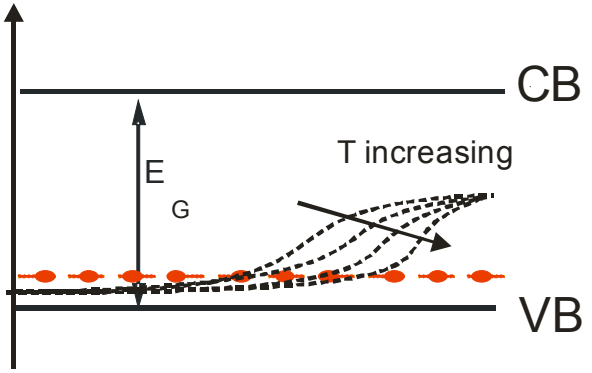
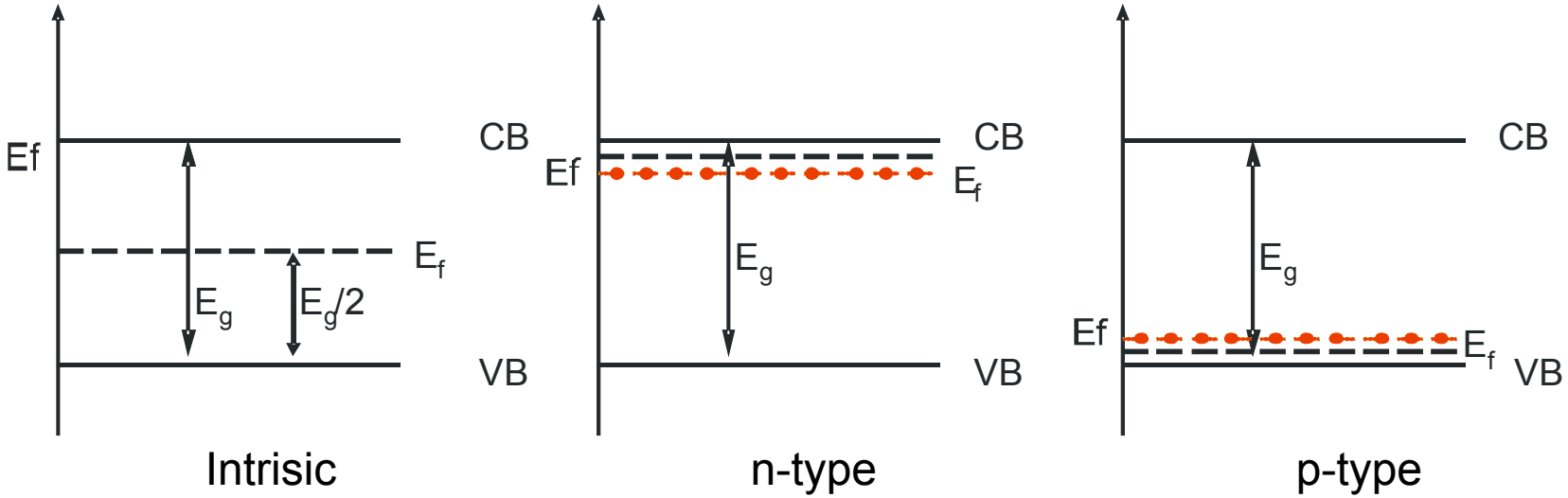
Energy bands & Occupation

P-type

By similar arguments, EF well below mid-gap and near V.B., only moving towards $E_g/2$ at very high temperature.



Summary



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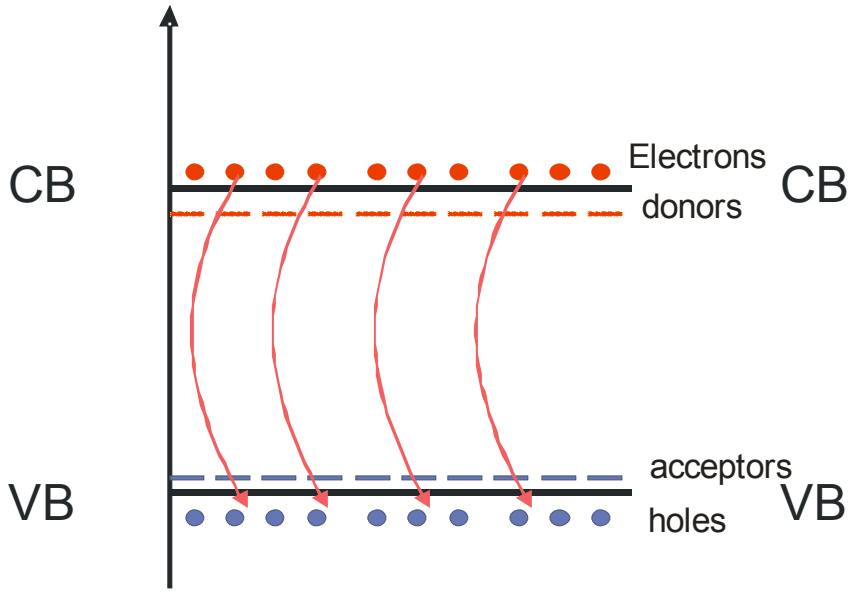
Energy bands & Occupation

Compensation Doping

Occurs when semiconductor is doped with *both* acceptors and donors

Compensation occurs when the extra electrons provided by donors fall into vacancies (or holes) created by acceptors, so if we put N_d donors= N_a acceptors into the silicon, no extra electrons or holes are produced



Why is this important?

Semiconductor wafers are normally doped one type. How to make a device?

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Energy bands & Occupation

Consider two of the simplest types of device:
planar diode, planar transistor

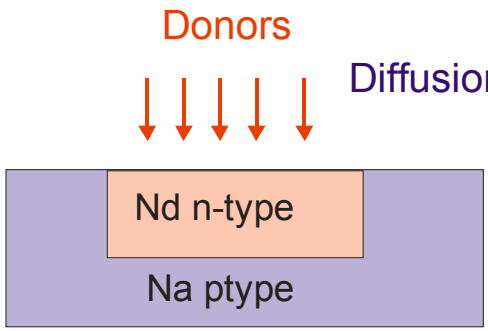
Starting point is a piece of p-type Silicon

These are semiconductors containing N_d and N_a – need to know σ for device design.

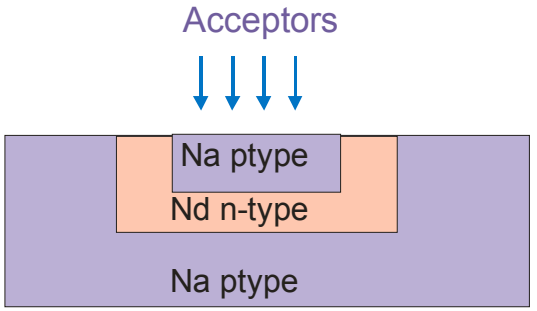
e.g. Si doped with $10^{21} m^{-3}$ acceptors (N_a)
Then doped with 10^{22} m^{-3} donors (N_d).

All the initial10^{21} holes from acceptors **recombine** with 10^{21} electrons from donors, leaving the material

n-type 10^{22} - 10^{21} = 9x 10^{21} m^{-3} – still a high concentration.



Planar diode



P-n-p transistor

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Energy bands & Occupation

Net density n(9. 10^{21}) < Nd (10^{22}) because of the presence of acceptors – called **compensation**.

Therefore magnitude of |Nd-Na| determines net carrier density and the sign (+ or -) gives the majority carrier type.

$N_d > N_a$ – n-type **$N_a > N_d$ – p-type**

General Case

acceptors	N_a	N_d	donors
electrons	n	p	holes

For electrical neutrality, assuming that T is such that dopants are completely ionised:
negative charge = positive charge

$n + Na = p + Nd$ (3)

Always $np = ni^2$ (4)

Using (3) in (4) $n + (N_a - N_d) = ni^2/n$ `$n^2 + (N_a - N_d)n - ni^2 = 0$

$$n = \frac{(N_d - N_a) \pm \sqrt{(N_d - N_a)^2 + 4n_i^{\,2}}}{2}$$

$$n = \frac{(N_d - N_a)}{2} + \frac{(N_d - N_a)}{2}\sqrt{1 + \left(\frac{2n_i}{(N_d - N_a)}\right)^2}$$

carriers from dopants intrinsic carriers

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Energy bands & Occupation

For p-type level, use eqn. (4)

$p = n_i^2/n$

can always use this relationship – especially when $n_i \sim (N_d - N_a)$

Case 1: Extrinsic (doped) material

$(N_d - N_a) >> n_i$ e.g. $10^{22} - 10^{21} >> 10^{16} m^{-3}$

2nd term under $\sqrt{}$ $\rightarrow 1$, and

$$n \approx \frac{(N_d - N_a)}{2} + \frac{(N_d - N_a)\sqrt{1}}{2} = N_d - N_a$$

$$p = \frac{n_i^2}{n} = \frac{n_i^2}{N_d - N_a}$$

e.g. n=9. 10^{21} m^{-3}, p ≈ 10^{22} m^{-3}

If $N_a > N_d$,

p = $N_a - N_d$ AND $n = \frac{n_i^2}{N_a - N_d}$

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Energy bands & Occupation

Case 2: Near Intrinsic Semiconductor

made by doping extrinsic material with just sufficient opposite type dopant to fully compensate and hence produce a net carrier concentration.

Nearly zero e &h from dopants of near zero – carriers then nearly all come from e-h pairs from intrinsic process.

i.e. $n_i >> |N_d - N_a|$ '1' is negligible in 2nd term under √

$$n \approx \frac{(N_d - N_a)}{2} + \frac{(N_d - N_a)\sqrt{\left(\frac{2n_i}{(N_d - N_a)}\right)^2}}{2}$$

$$n \approx \frac{(N_d - N_a)}{2} + n_i \approx n_i = p$$

Practically it is difficult to get the dopants to cancel exactly to get this condition

e.g. if $10^{22}m^{-3}$ donors and want to make it intrinsic (~10^{16}m-3), we need to add acceptors of 1.000001 x $10^{22}m^{-3}$ – nearly impossible to control to this accuracy!

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Junction Diode

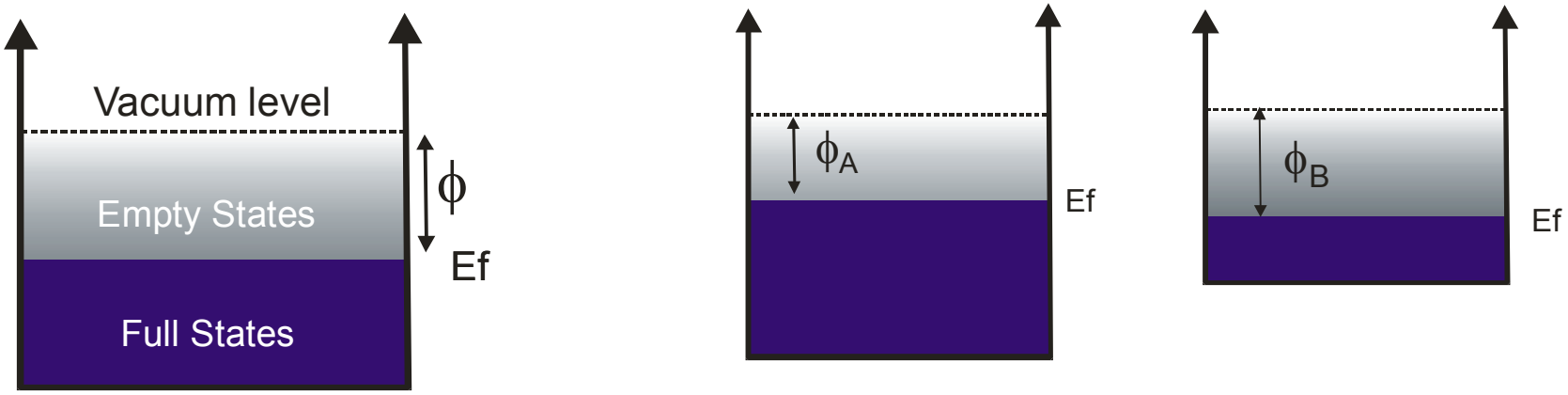
The simplest semiconductor device (but also the basis for the transistor)

Consider the junction in equilibrium (no bias).

In classical electrostatics, 2 bodies in equilibrium have *same* potential – **NOT** true for semiconductor junctions.

For electronic equilibrium, no net current flows – this requires a contact potential to exist between the 2 parts. e.g. p-n junction, V_o

Consider joining two different pieces of material.



Φ= work function –height of the potential energy barrier at material surface.

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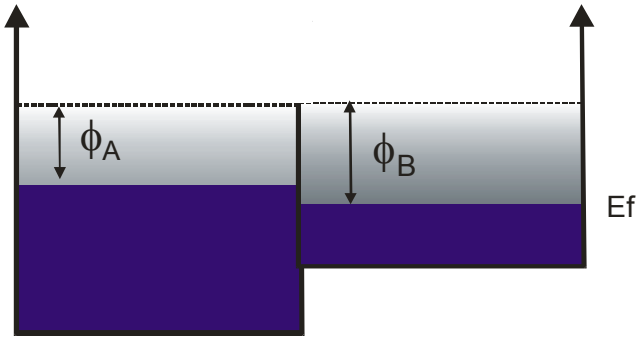
Junction Diode

immediately after contact

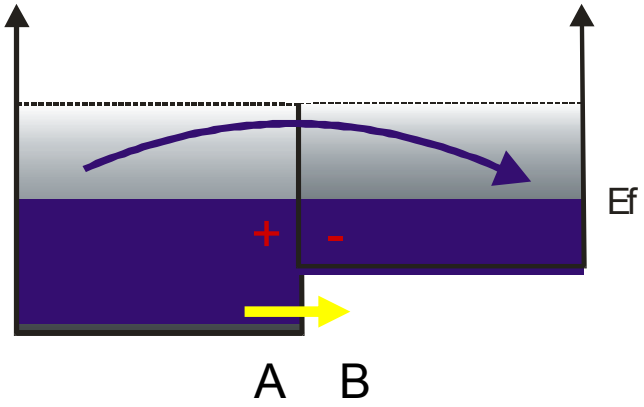


electron flow from material A (higher Fermi energy level) to material B

In equilibrium

No current will flow since the probability of electrons having a particular energy is the same on each side (*E_F and T same on each side)*

$$P(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}$$



E-field from built-in potential.

E_F is continuous and aligned across the junction. But a contact or built-in potential, V_o, exists to ensure no net flow of electrons.

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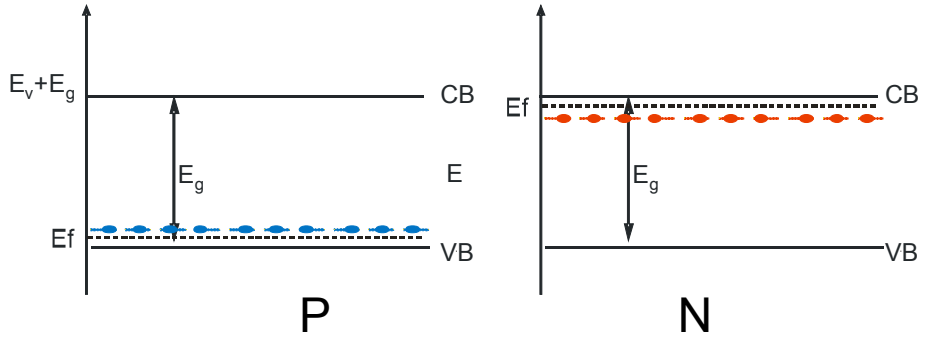
Junction Diode

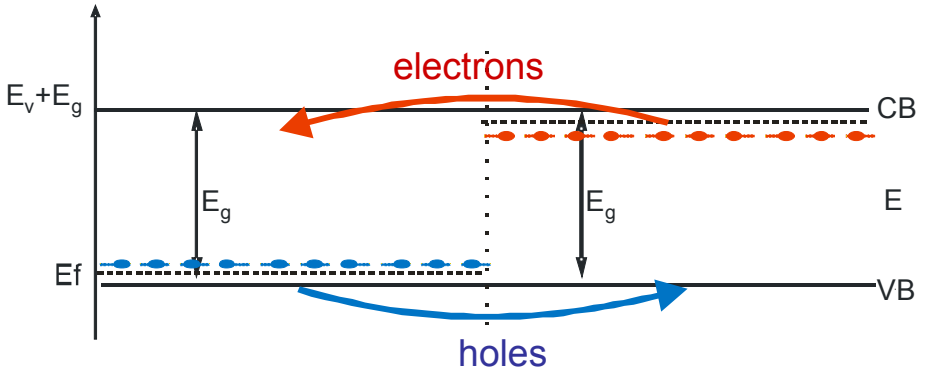
P-N Junction in Equilibrium

Bring ‘p’ and ‘n’ semiconductors together to form a junction

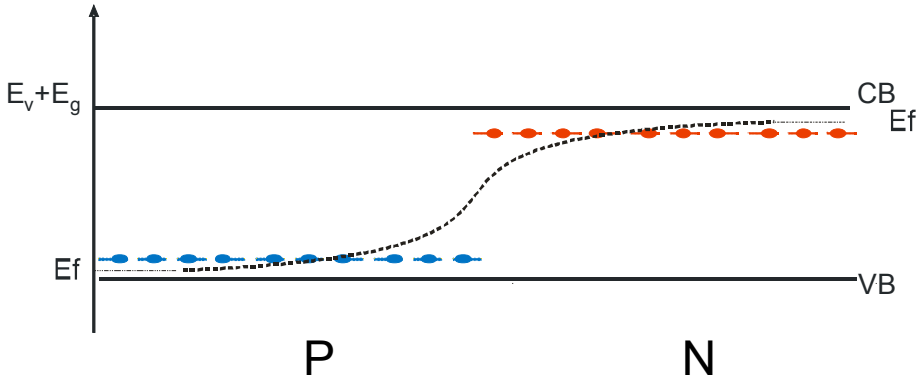


At the point of contact

Majority carriers flow across the junction into empty states opposite (diffusion).



After contact



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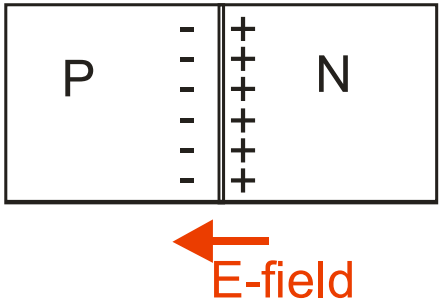
Junction Diode

As carriers diffuse across, an electric field is created across the junction which eventually balances the flow of carriers. A built in potential, Vo, appears across the junction



In equilibrium

At equilibrium net current = 0. Hence drift current flow due to the electric field opposes diffusion current flow.

i.e. diffusion current = drift current.

E builds up until net current is zero at equilibrium.

$$E = -\frac{dV}{dx}$$

Holes have left the p-region leaving behind fixed negative acceptor charge – **p-levels rise.**

Electrons have left n-region leaving behind fixed positive donor charge – **n levels fall.**

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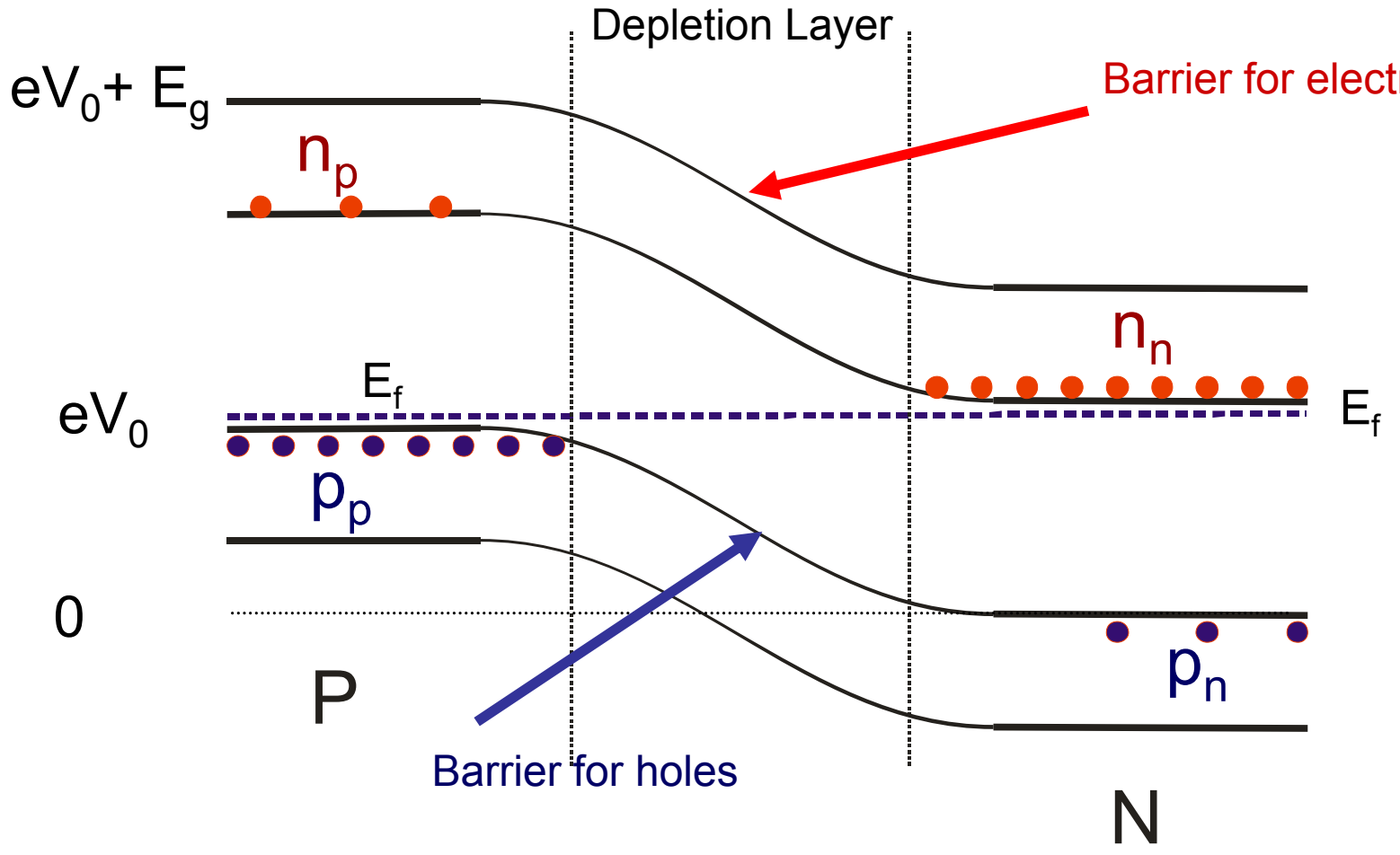
Junction Diode

But C.B., V.B.& E_F are fixed, so alignment only possible if all levels in p-type move relative to those in n-type. Each side of junction takes up a different potential, V_o.



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Junction Diode

The flow of carriers into the opposite side of the junction leaves a charge behind. This so called space charge (fixed charge) produces the electric field.

A barrier of height eV_o forms due to this electric field which brings the junction into equilibrium and prevents further current flow.

Number of electrons in CB of n-region, $n \propto P(E_g)$

$$n_p \propto \frac{1}{1 + \exp\left(\frac{E_g + eV_o - E_F}{kT}\right)} \propto \exp - \left(\frac{E_g + eV_o - E_F}{kT}\right)$$

Number of the electrons in CB of p-region, $n_p \propto (E_g + eV_o)$

$$n_n \propto \frac{1}{1 + \exp\left(\frac{E_g - E_F}{kT}\right)} \propto \exp - \left(\frac{E_g - E_F}{kT}\right)$$

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Junction Diode

Divide the two expressions:

$$\frac{n_n}{n_p} = \exp\left(\frac{eV_o}{kT}\right)$$

$$V_o = \frac{kT}{e}\log_e\left(\frac{n_n}{n_p}\right)$$

Remember that np = n_i^2, and therefore $p_p n_p = p_n n_n = n_i^2$

$$n_p = \frac{n_i^2}{p_p}$$

If all carriers are ionized $n_n \approx N_d$ and $p_p \approx N_a$, so by substitution

$$V_o = \frac{kT}{e}\log_e\left(\frac{N_d N_a}{n_i^2}\right)$$

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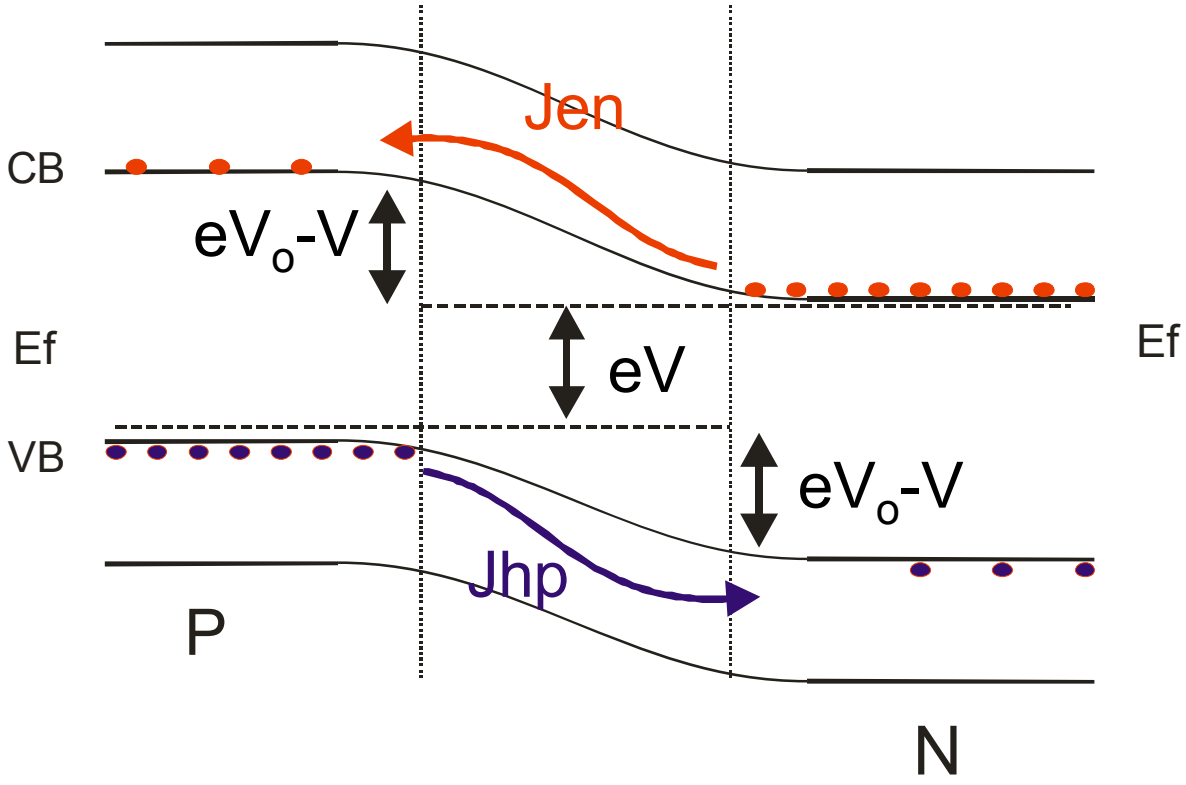
Junction Diode

p-n with different bias conditions

No bias, I=0 due to potential barrier (in equilibrium)

Forward bias

With forward bias, V, the barrier height is efficiently reduced to $e(V_o - V)$. Immediately after bias is applied, energy bands tilt – majority carriers diffuse- current flows (diffusion ≠ drift)



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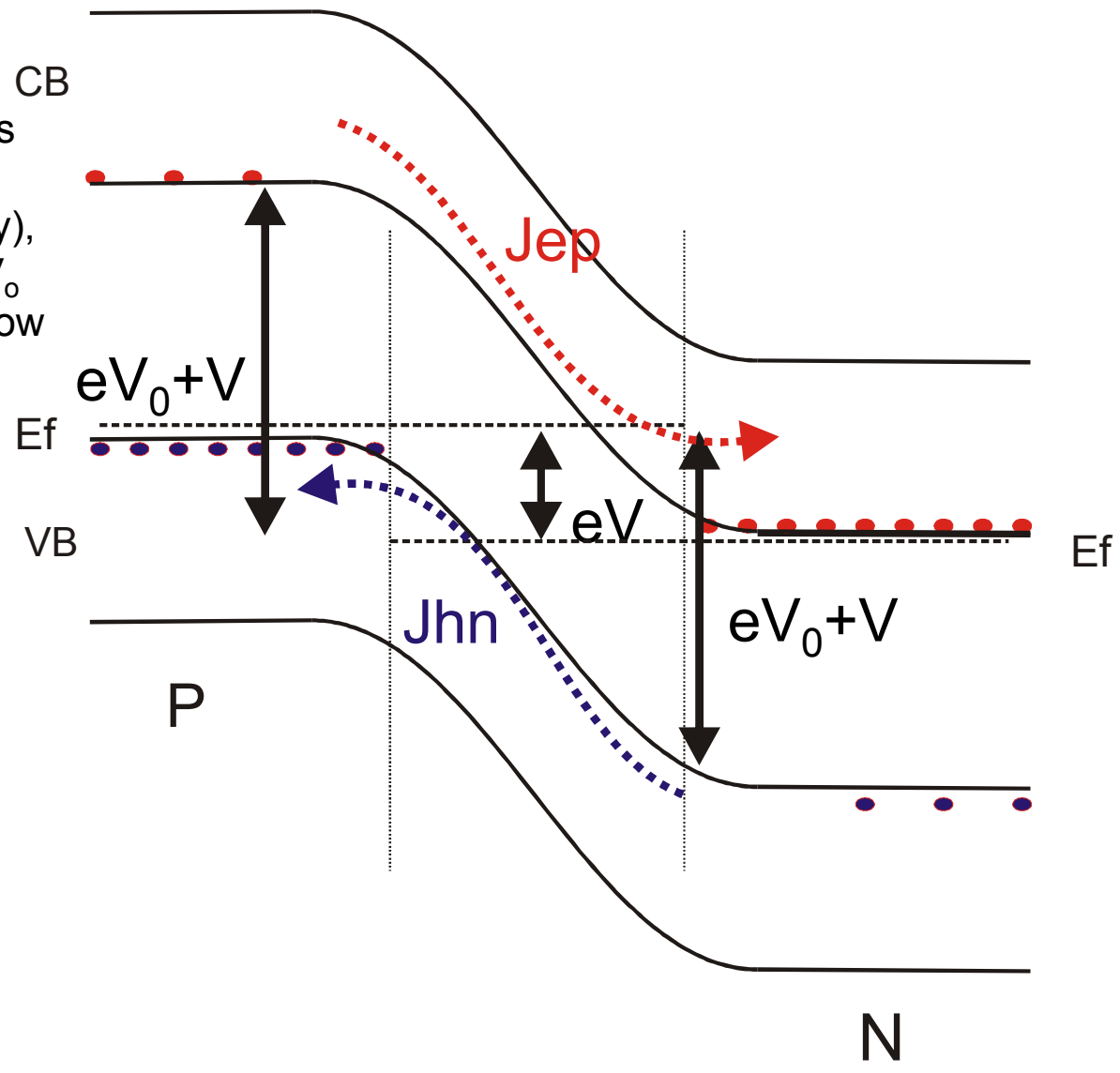
Junction Diode

In steady state, carriers flow from the contacts (external circuit) to restore equilibrium away from junction. V appears across depletion layer (fewer carriers so lowers conductivity), lowering barrier height to e((V_o – V). Large majority current flow

<u>Reverse bias</u>

In steady state, barrier height is increased, e(Vo + V). No majority carriers flow because of increased barrier height (i.e. diffusion → zero).



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Junction Diode

Very small electron current flows from p $\rightarrow$ n due to minority electrons, which are swept across by E-field (i.e. fall down potential hill). Similarly for minority holes flow. The small saturation current which does flow is Io which is independent of V – it depends primarily on temperature.

This leads to the diode (rectifier) equation: $$I = I_o \left[\exp\left(\frac{eV}{kT} \right) - 1 \right]$$

4 components of current flow in a p-n semiconductor junction.

Majority hole current from p, Jhp. Minority hole current from n, Jhn

Minority electron current from p, Jep. Majority electron current from n, Jen

Reverse bias –majority current cannot flow - get minority Jep and Jhn as shown – they arise from thermal generation of e-h pairs in or near the depletion region. – depends on temperature.

Zero bias –

When V=0, $J_{hp} = J_{hn}$ and $J_{ep} = J_{en}$, **i.e. no current**

Forward bias with V>0,

$J_{hp} = J_{hn} \exp\left(\frac{eV}{kT} \right)$ (hole flow)

$J_{en} = J_{ep} \exp\left(\frac{eV}{kT} \right)$ (electron flow)

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Junction Diode

Net hole current, $J_h = J_{hp} - J_{hn} = J_{hn} \left[\exp\left(\frac{eV}{kT}\right) - 1\right]$

Net electron current, $J_e = J_{en} - J_{ep} = J_{ep} \left[\exp\left(\frac{eV}{kT}\right) - 1\right]$

Total diode current is

$$J = J_h + J_e = J_o \left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

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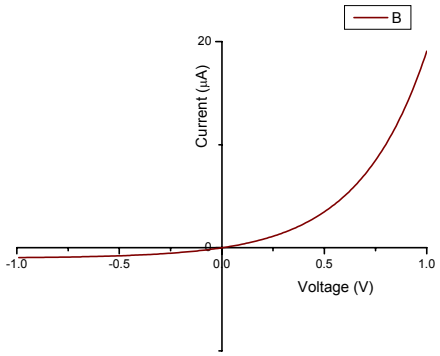
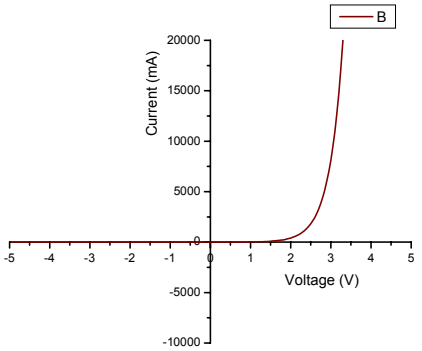
Junction Diode

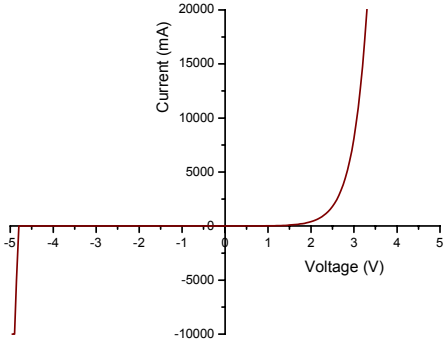
Ideal Diode Equation

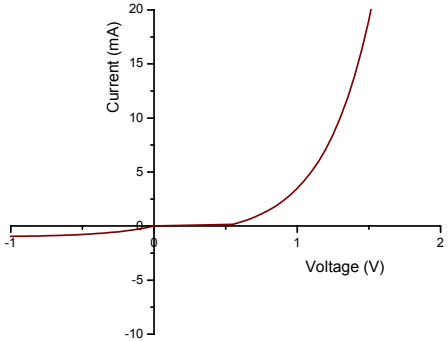
$$J = J_o \left[\exp\left(\frac{eV}{kT} \right) - 1 \right]$$





Deviation from Ideality





Reverse (avalanche) breakdown

Offset (or turn-on) voltage

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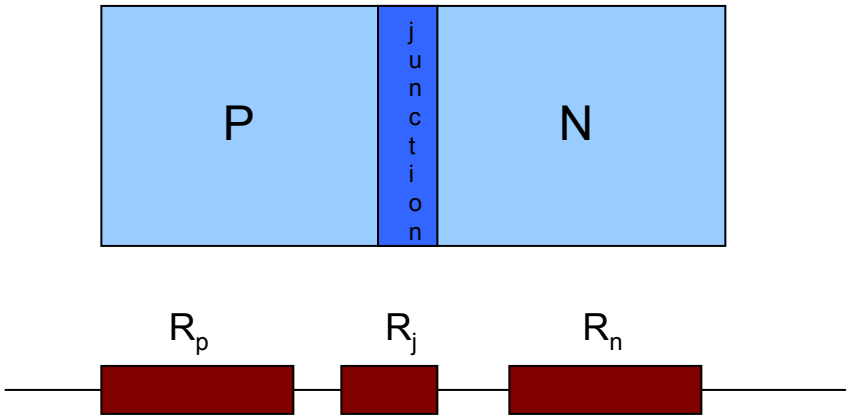
Junction Diode

- **Avalanche Breakdown**

Avalanche breakdown is a current multiplication process that occurs only in strong electric fields. Under high reverse bias voltage the electric field across the narrow junction region can become large enough to ionise (strip electrons) from semicondcutor atoms. Field strengths used in semiconductor devices that exploit the avalanche effect are often in the 20–40 MV/m range. In devices that exploit the avalanche effect, the electric field is normally kept just below the threshold at which avalanche breakdown is possible, resulting in a current that is highly dependent on the generation of free electrons. In avalanche photodiodes, for example, incoming light is used to generate these free electrons.

- **Voltage drop (Turn-on voltage)**

Regions of the p-n diode which are not part of the junction can add resistance and cause a voltage drop. Therefore the diode is not seen to ‘turn-on’ until a certain voltage is reached. Values can range from 0.8V for Si up to 2-3V for a GaN LED.



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Junction Diode