Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE339 Digital Engineering

Answer **FIVE QUESTIONS** comprising **AT LEAST TWO** each from **part A** and **part B. No marks will be awarded for solutions to a sixth question, or if you answer more than three questions from parts A or B.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Part A

A1. **a.** Describe what is meant by *cache memory* in a microprocessor. Briefly explain what you understand by the terms *direct mapping*, *fully associative mapping* and *set associative mapping* in the context of cache memory. **(8)**

b. Perform the calculation of $1111_2 \div 110_2$ (decimal 15 divided by 6) by restoring division. Show each step of the calculation using 8-bit binary arithmetic. You must start the process by left shifting the divisor by three places (multiplication by 2^3) in order to model a process whereby any four bit positive integer could be divided by any three bit positive integer. **(6)**

c. An Intel 8086 processor has a 16-bit address bus and 16-bit data registers. However, it is still able to address 1Mb of memory. Explain how this is achieved, clearly describing how the address is generated. **(6)**

A2. **a.** Explain the operation of a serial multiplication circuit using shift-and-add multiplication. Be sure to carefully describe the initial circuit state. **(5)**

b. Describe the different circuit states (just before each rising clock edge) for the case of multiplying the two unsigned 4-bit binary numbers, 1010 x 0110; set out your answer as a table. **(6)**

c. Explain why basic shift-and-add multiplication does not work for multiplying 2s-complement numbers. **(6)**

d. For n-bit wide multiplicands and multipliers, what determines the maximum speed of operation of the serial multiplication circuit as n becomes moderate to large? **(3)**

A3. **a.** Describe the implementation of a stack in a microprocessor. In particular, how is a stack managed and manipulated? **(4)**

b. How can a stack be used for passing parameters (arguments) to a function or procedure? **(4)**

c. A finite state machine is required which can generate a Fibonacci sequence. This is a sequence of numbers that follow the pattern:

0, 1, 1, 2, 3, 5, 8, 13, 21, 34 ……

The number in position ***i*** of the sequence is given by adding the previous two numbers:

fib(i) =

0, if i = 0

1, if i = 1

fib(i-1) + fib(i – 2), if i > 1

This component will be part of a larger system, which will supply a signal ***start*** which indicates the start of an operation and ***i*** which indicates how many numbers in the sequence to generate. The component should output the sequence itself and a signal ***done*** should go high for one cycle when the sequence is complete.

Draw an ASMD (Algorithmic State Machine with Datapath) chart for this component, clearly describing the purpose of any states that you use. **(12)**

A4. **a.** With reference to the Verilog Hardware Description Language, describe with the aid of a timing diagram, what you understand by:

i) Inertial Delay

ii) Transport Delay **(6)**

b. Draw a truth table for the circuit described by the following Verilog code.

```
module mycircuit (output reg [3:0] y, input [1:0] a);
integer i;
always @ (*)
  for (i = 0; i <= 3; i = i + 1)
    if  (a == i)
      y[i] = 1;
    else
      y[i] = 0;
endmodule
```

Describe a use for this circuit. **(4)**

c. Explain the function of a Barrel Shifter. Show with the aid of a suitable diagram, how a 4-bit barrel shifter could be implemented using only combinatorial multiplexers. **(6)**

d. What are the advantages of implementing a shift register in a microprocessor CPU with combinatorial logic as opposed to sequential logic based upon D-Type flip-flops. **(4)**

Part B

B1. a. i) In the context of a discrete-time system, explain the concepts of causality, stability, linearity and time invariance. (6 marks)

ii) A sequence is said to be the eigenfunction of a linear time invariant (LTI) system, when given such a sequence at its input, its output is a simple scaled version of the same sequence. Determine whether the sequence $x[n]=4^n$ is the eigenfunction of an LTI system. Explain your answer. (4 marks)

(10)

b. i) Determine whether the following two signals are periodic. If the signal is periodic, state its period: (4 marks)

1) $x[n] = e^{j2n\pi/3}$ 2) $x[n] = \cos(n\pi/\sqrt{2})$

ii) Suppose the above two sequences are obtained by sampling two continuous-time signals, respectively. What extra information do you need to recover the original continuous-time signal? (3 marks)

iii) Draw the block diagram of an ideal system for recovering the original continuous-time signals. (3 marks) **(10)**

B2. a. Given the spectral coefficients of a filter, *H(k)*, which are symmetrical about *k*=0, the original impulse response *h*[n], can be reconstituted using the following equation, where *N* is the total number of coefficients:

$$h[n] = \frac{1}{N}\sum_{k=-(N-1)/2}^{(N-1)/2} H(k)e^{j2\pi nk/N} = \frac{1}{N}\left(H(0) + 2\sum_{k=1}^{(N-1)/2} H(k)\cos(2\pi nk/N)\right)$$

From this you are going to design a lowpass FIR filter with *N=5* coefficients with a passband range of *0.5*kHz at a sampling frequency f_s*=2*kHz.

i) Use the frequency sampling method to calculate the FIR filter coefficients. (4 marks)

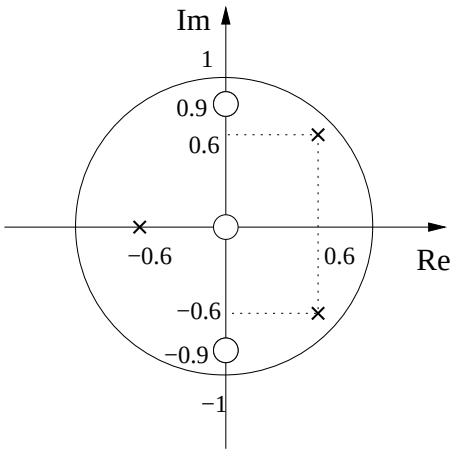
ii) Sketch the structure of the filter using unit-delay elements. (2 marks)

iii) Derive the linear constant coefficient difference equation of the filter. (2 marks)

(8)

b. For a causal stable LTI system to also have a causal stable inverse, what kind of characteristics should such a system possess? Explain your answer. **(6)**

c. i) Derive the transfer function (z-transform) for a causal IIR filter which has the z-plane pole-zero plot shown in the following figure, where there are 3 poles and 3 zeros. Specify its region of convergence. (4 marks)



ii) Find the transfer function (z-transform) of its inverse system and specify its region of convergence. (2 marks)

(6)

B3. a. Calculate the Discrete Fourier Transform (DFT) of the discrete series x[n]={1, 2, 2, 1}.

(4)

b. Consider a sequence $x_1[n]$ whose length is L points (nonzero for n=0, 1, …, L-1) and a sequence $x_2[n]$ whose length is P (nonzero for n=0, 1, …, P-1). A linear convolution of these two sequences will generate a third sequence $x_3[n]$. Describe the process involved in calculating this linear convolution using DFT.

(6)

c. A lowpass digital filter is to be designed for a digital signal processing system and the first-order analogue filter given in the following equation is used as a prototype, where ω_b is the filter cutoff frequency.

$$H(s) = \frac{\omega_b}{s + \omega_b}$$

i. Design the digital filter using the Impulse Invariant method if ω_b=50rad/sec and the filter is implemented at a sampling frequency of 80Hz. (5 marks)

ii. Given the same sampling frequency of 80 Hz, design the digital filter using the Bilinear Transform method and make sure that the resultant digital filter has a normalised cutoff frequency corresponding to 50rad/sec. (5 marks)

(10)

B4. **a.** What is the output y[n] of an LTI system with impulse response h[n], n=-∞, …, 0, …, +∞, given the sinusoidal input x[n]=Acos(Ω_0n+φ)? How about if h[n] is real-valued?

(8)

b. The impulse response of a causal LTI system can be described by the following equation:

$$h[n] = \left(\frac{1}{2}\right)^n \quad \text{for} \quad n \geq 0$$

i) Obtain the linear constant coefficient difference equation describing its behaviour and draw a block diagram of the system. (4 marks)

ii) Find its frequency response and then calculate its output given the following input sequence: (4 marks)

$$x[n]=10+2\sin(n\pi/2)$$

(8)

c. Give a comparison between IIR and FIR filters in terms of their relative advantages and disadvantages. **(4)**

WL/NJP/JR