Exam Feedback: EEE204 January 2008

General Comments: A reasonable attempt at EEE204 very few people scored very low marks. As last year, and, sadly, every year, many marks were lost because of silly numerical errors and whilst each error only loses one mark, some of you were totting up quite a few that you could ill afford. The two main problems that some of you have are disorganisation and explanation. These are perennial problems so the comments that follow were also in last year's feedback comments. Some of you presented very messy work that was hard (in some cases impossible) to interpret and in a few cases you confused yourselves by failing to take an ordered approach to your questions. If you are doing an analysis, you need to draw a circuit diagram – how else can I credit correct formulation of equations describing the circuit? You need to explain briefly (three or four words is usually enough) what you are doing so that I can follow your thinking – if I just see a set of numbers or equations you leave me in a position of having to guess whether or not you are intentionally doing the right thing.

Q1: The example of figure 1 was the same as one in the *RC* problem sheet and although most of you managed to derive the transfer function, a few people got stuck - it was easy to see who had practiced doing *R-C* circuit problems. About 50% of you recognised that hf gain was a capacitive divider but half of that 50% got the divider expression wrong. Most of you recognised that lf gain was zero. Several incorrect attempts gave answers like "lf gain = R_1" - this cannot be right for a dimensionless ratio V_o/V_i. In part (iii) I got a range of sketch qualities ranging from really good to meaningless squiggle - you do need to take care with sketches, I should not have to use my imagination to decide whether or not you know what you are doing. In part (iv) you either had to say lf gain (resistive divider) must equal hf gain (capacitive divider) or recognise that $C_1R = C_2R_1$ to remove frequency dependence from the circuit gain. Alternatively you could re-analyse the circuit with the extra component and find the condition that made pole and zero cancel out - a laborious alternative just for 2 marks. In part b(i) it was evident that some of you have not been saying $\tau = 1/\omega_0$ before bed every night and quite a few people neglected to multiply the Hz by 2π before inverting it to get τ. I was disappointed by your attempts at (b) (ii). Most people assumed they were dealing with a sinusoid (which they weren't) and of those who read the question and dealt with a step, most forgot that it was the size of step at the output that mattered. Only one person worked out (by differentiation) the maximum rate of change of an exponential - shame on the rest of you!

Q2. Part (i) tested your ability to identify the major features of the transfer function given, most attempts were reasonable although a few people thought it was a band pass response (which it wasn't) and some thought it was digital! Part (ii) asked you to interpret the transfer function given to identify k, ω_n and q. Most people managed k and ω_n but about 30% of the qs were wrong. The q problems, for the most part, lay in algebraic errors in the substitution of ω_n into $1/(\omega_n q) = C_2(R_1+R_2)$ - I remember warning you about these dangers in lectures. A few made errors such as $C_2\Big/\sqrt{C_2} = 1\Big/\sqrt{C_2^3}$! The easy check here was that q should be dimensionless. One or two people interpreted part (ii) as "derive the transfer function" - which they did but it was not asked for so there were no marks for it. Few people had a serious go at part (iii) although one person used a method quite different from the one I used in the notes but equally valid - well done that person! Part (iv) was spoiled in many cases by a lack of organisation on the part of the doers. Most recognised which relationships were needed but many didn't write things out in an ordered way and as a result they confused themselves and made careless errors. The majority forgot that 4 kHz needs multiplying by 2π in order to change it into ω.

Q3: This question was attempted well – 90% of you managed the first two parts without problems. Those who had problems made similar mistakes to last year - very disorganised and forgetting to square the potential dividers operating on the various noise power sources. In part (b)(i) most people worked out the resistance that would give a noise voltage that was 10% of v_n when the question said 10% of noise power. Thus you should have worked out the mean squared value of v_n and then found the resistance that would generate a mean squared noise voltage that was 10% of this value. You also needed to use the non-inverting amplifier gain, $(R_1+R_2)/R_1$, as some of you did. Many of you wrote down the non-inverting gain as $R_1/(R_1+R_2) = 50$ - it cannot be true! You must learn to look at what you write down and check for impossible statements. Depending on the errors you made, I got resistor values between $10^{-12}\Omega$ and $10^{27}\Omega$ and only two people commented that their values looked a bit strange - very worrying. (There was also an element of this in **Q2** part (iv) where some of the capacitors had values of millions of Farads - again with no comment!) I gave some credit for those who indicated that they realised their answer was silly but took a dim view of those who didn't.

Q4: A relatively small fraction of you attempted question 4 but most of you that did attempt it made good attempts. Most answers to part (i) got full marks although some people lost a mark because they failed to show that P_L was the same as P_{DISS} at the maximum P_{DISS} condition. In parts (ii) and (iii) most answers were correct but one or two of you used the maximum P_{DISS} relationship of part (i) to calculate the required V_{CC}. This gives the wrong V_{CC} because maximum P_{DISS} occurs at a lower V_{LP} than that at maximum load power. Part (iv) was done well by some and less well by others. In part (iv) some people obviously thought about where the power was flowing and applied their knowledge appropriately while others tried to fit the information given to fragments of equation that they recalled and consequently ended in a mess. Part (v) was answered correctly by a couple of people but quite a few attempts were thinking along the right lines. With an 8Ω inductive load the peak *V* and peak *I* would be the same as for the resistive load but no power would be dissipated in the inductor so all the supply power would be dissipated in the output transistors. Since average supply current is proportional to peak load current, maximum P_{DISS} with an inductive load occurs at maximum I_{LP} ($=V_{CC}/Z_L$).