Direct Digital Synthesis (DDS)

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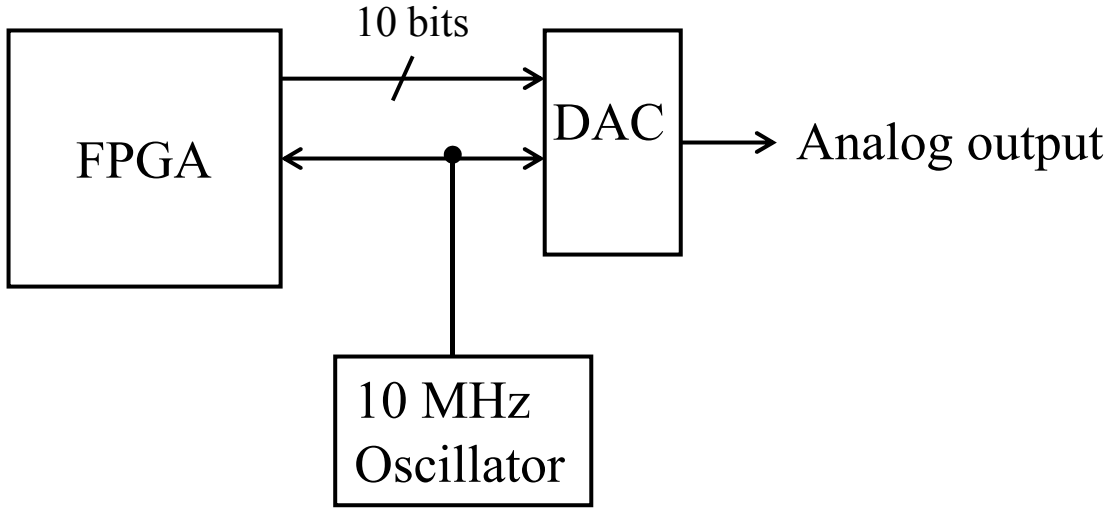
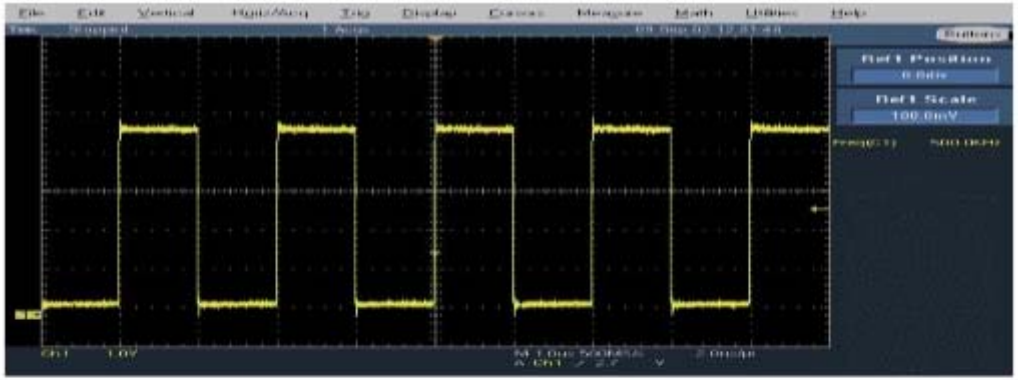
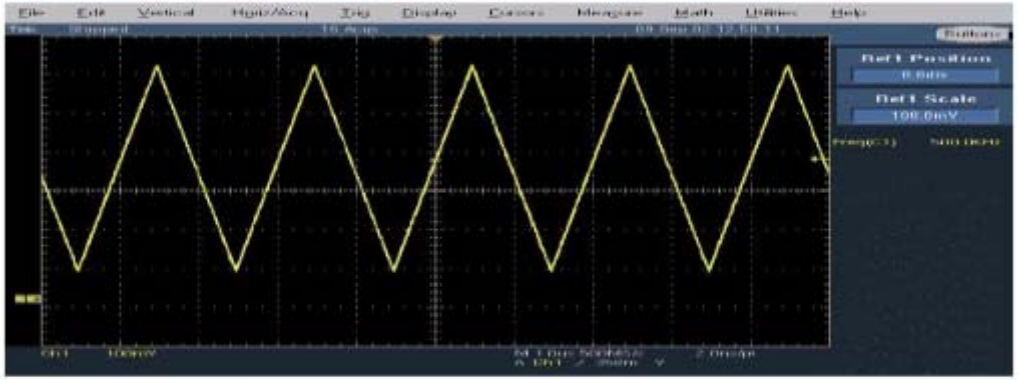
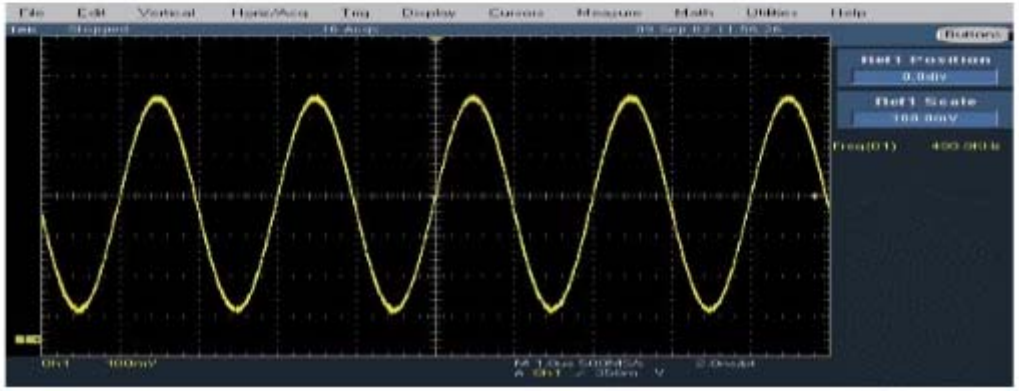
- Method to produce an analog waveform
- Generate time varying signal in digital form
- Convert to analog form using Digital-to-Analog Converter (DAC)
- Fast switching between output frequencies
- Fine frequency resolution
- Operation over a broad spectrum of frequencies









```
module DDS_Square (DAC_clk, DAC_data);
  input DAC_clk;
  output [9:0] DAC_data;
  reg [15:0] cnt;
  always @(posedge DAC_clk) cnt <= cnt + 16'h1;
  wire cnt_tap = cnt[5];
  assign DAC_data = {10{cnt_tap}};
endmodule
```

Create a 16 bit register for a binary counter

Take one bit out of the counter

Duplicate it 10 times to create the 10-bits DAC value

Using the 6^{th} bit to generate the output:

Let the counter clock = 10 MHz

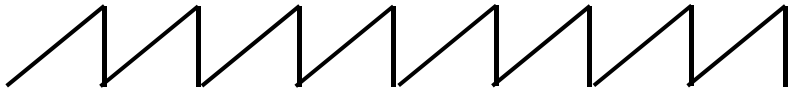
Then 6^{th} bit toggles at 10MHz / 2^6 = 156.25 KHz

DAC output is a 156.25 KHz square wave

Amplitude is maximum value

156.25 KHz

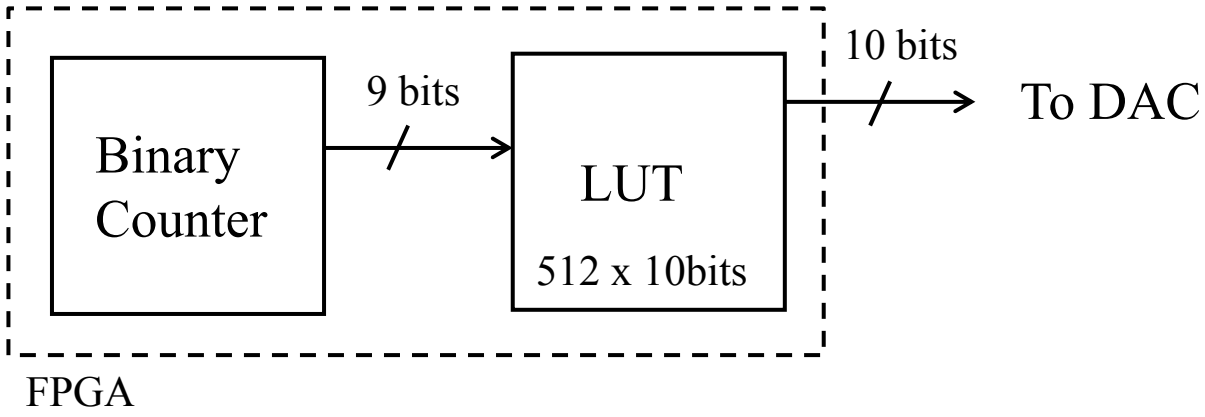
```
module DDS_SawTooth (DAC_clk, DAC_data);
  input DAC_clk;
  output [9:0] DAC_data;
  reg [15:0] cnt;
  always @(posedge DAC_clk) cnt <= cnt + 16'h1;
  assign DAC_data = cnt[9:0];
endmodule
```



```
module DDS_Triangle (DAC_clk, DAC_data);
  input DAC_clk;
  output [9:0] DAC_data;
  reg [15:0] cnt;
  always @(posedge DAC_clk) cnt <= cnt + 16'h1;
  assign DAC_data = cnt[10] ? ~cnt[9:0] : cnt[9:0];
endmodule
```

Arbitrary signals

Use a LUT (lookup table) to hold the shape of the analog signal that we want to generate. The most common shape to generate is a sine wave.



On an FPGA, the LUT would typically be implemented as blockram and would be instantiated as shown:

```
wire [9:0] LUT_output;

blockram512x10bits
  DDS_LUT(
      .rdclock(clk),
      .rdaddress(cnt[8:0]),
      .q(LUT_output)
);
```

The size of the LUT can be reduce by exploiting the symmetry of a sine wave.

$$\sin(\theta) = \sin(\pi - \theta)$$

```
wire [9:0] LUT_output;

blockram512x10bits
   DDS_LUT(
      .rdclock(clk),
      .rdaddress (cnt[9] ? ~cnt[8:0] : cnt[8:0]),
      .q(LUT_output)
);
```

The direction of reading the LUT has been reversed after a half-period.

Thus LUT appears to be 1024 x 10 bits instead of 512 x 10 bits.
A second symmetry can be exploited to make it appear 2048 x 10 bits.

```
wire [7:0] LUT_output;

blockram16x8bits
DDS_LUT(
.rdclock(clk),
.rdaddress (cnt[3] ? ~cnt[2:0] : cnt[2:0]),
.q(LUT_output)
);
```