Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2008-2009 (2 hours)

Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **Figure 1** shows a simplified layout of a logic circuit, with the inputs (A, B, C, D) and output (Y) labelled:

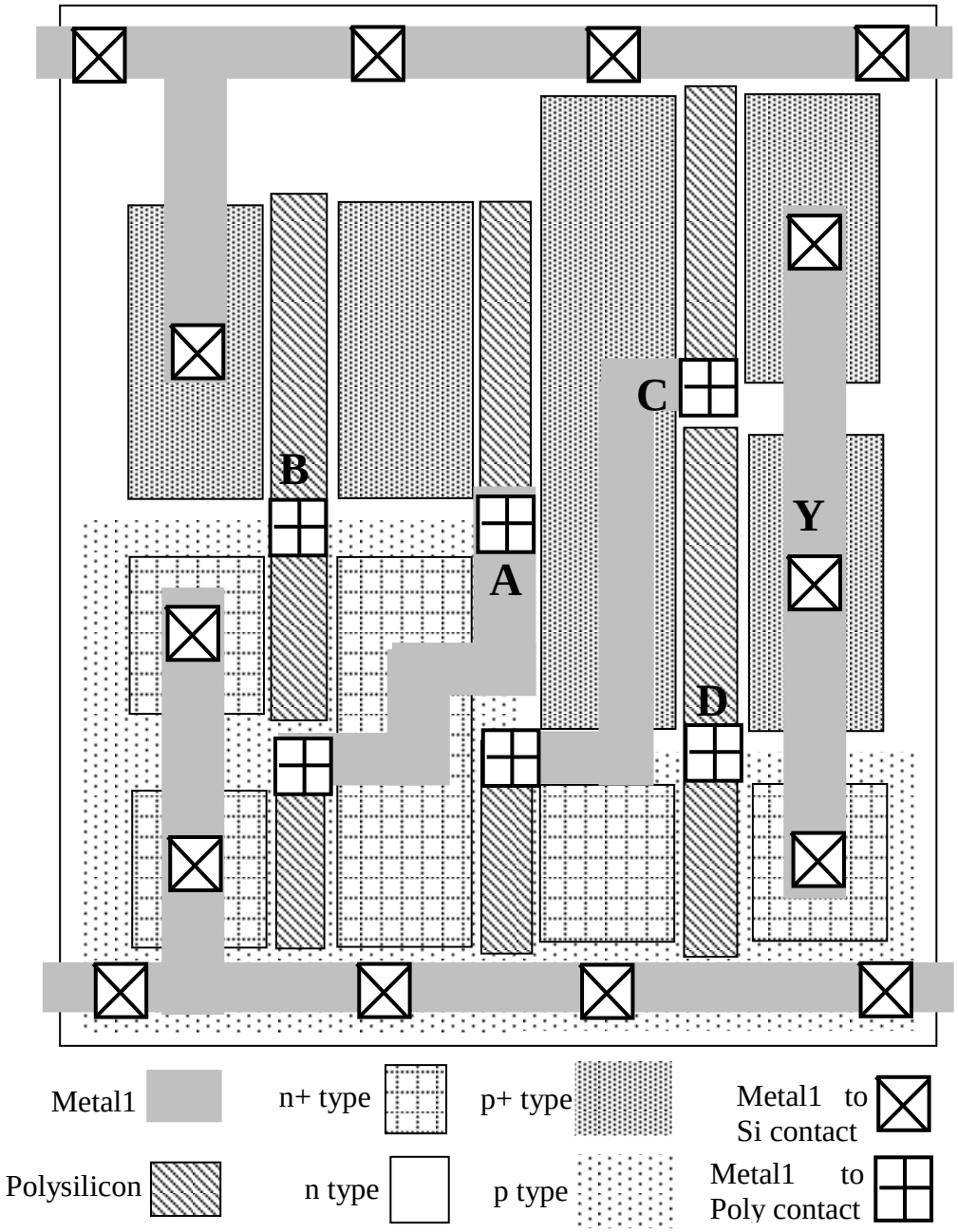

Figure 1: Circuit Layout

a. Draw a circuit diagram that is an *accurate* representation of the layout in **Figure 1**. **(8)**

b. Write down the logical function of the circuit. **(4)**

c. There are rows of four contacts along the top and bottom of the cell connecting the power supply lines to the underlying silicon. What is their function and why are there so many contacts? **(4)**

d. What can you say about the mobilities of electrons and holes from looking at the layout? **(4)**

2. A logic circuit is shown in **Figure 2**.

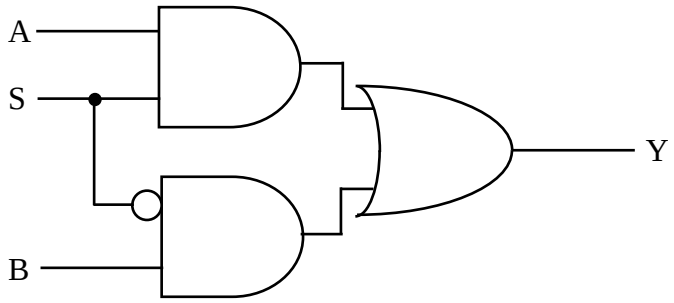

Figure 2: Logic Circuit

a. Convert the logic circuit into a standard-CMOS transistor-level circuit. **(8)**

b. Size the transistors (as a multiple of a minimum-sized *n*-type FET) for a minimum sized logic circuit, stating any assumptions that you make. **(6)**

c. Estimate the capacitance associated with each of the inputs and wires within the circuit (you can neglect the interconnect capacitance), given that the gate capacitance of a minimum-sized *n*-type FET is 1fF. **(4)**

d. Can you give the more *common* or standard name given to the type of circuit shown in **Figure 2.** **(2)**

3. **a.** For the two FETs shown in **Figure 3**, write down the equations for I_{DSN} and I_{DSP} in the saturated mode of operation (using the usual terms and ignoring channel length modulation).

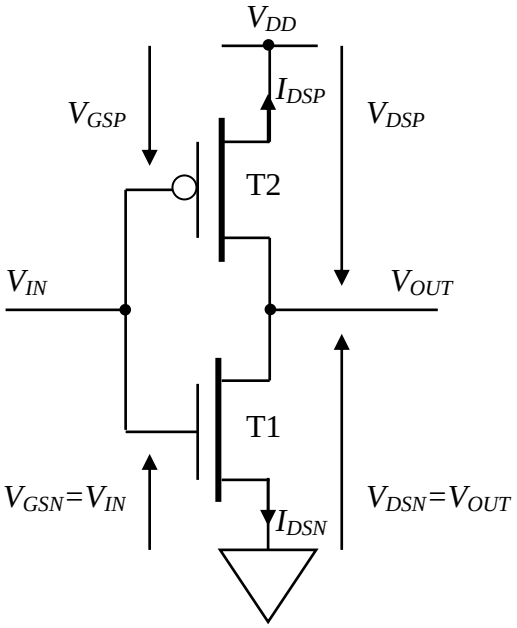

Figure 3: CMOS Inverter **(4)**

b. Show that the value of the input voltage, $V_{IN|switch}$, when the output of the inverter in **Figure 3** switches is identified by the following equation:

$$V_{IN|switch} = \frac{V_{DD} - V_T\left(1 - \sqrt{\frac{\beta_N}{\beta_P}}\right)}{\left(1 + \sqrt{\frac{\beta_N}{\beta_P}}\right)}$$

where β_N and β_N have their usual definitions and the threshold voltages of the FETs is such that $V_T = V_{TN} = -V_{TP}$. **(8)**

c. What would the *normal* value of the switching voltage be and how is this achieved practically? **(2)**

d. Are there any circumstances in which you might want to alter the switching voltage, how might this be achieved, and what are the limitations likely to be. **(6)**

4. **a.** Show how a rising-edge-triggered master-slave D-type Flip-flop can be constructed from two basic latches. Ensure that you describe how the pair of latches behave. **(6)**

b. **i)** Draw a schematic to show how you can construct a clock generator that will produce a clock signal and its inverse, which do not overlap in the low state. **(4)**

ii) Why is it important, in some types of design, to have two clocks that do not *overlap*? **(2)**

c. **i)** What is a clock tree and why is it so important for the synchronous design methodology? **(4)**

ii) Show how a clock tree might be constructed **(2)**

iii) What is metastability? **(2)**

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