EEE105 2006-7 Examination Paper -- Solutions

1.a. [Bookwork]

The answer here should indicate that the LED is a p-n junction. As it is a diode the device should exhibit an exponential rise in current with voltage due to the exponential rise in carrier diffusion across the junction as the forward bias increases, reducing opposing drift current term given by the built-in field. Very good students may also note that at high currents, to get the most light output from the LED, the resistive losses will play a role and consequently a linear rise in current with voltage may eventually be expected. Light is produced by the electron-hole pairs recombining, i.e. from electrons falling from the conduction band to valence band. The rate of recombination is equivalent to the current, therefore the light output should rise linearly with increasing current.

1.b. [Problem – varying degrees of difficulty for the different parts]

i) ***External Efficiency is essentially a new concept to the students, but a clear definition is given. The problem really resolves around interpreting the facts given correctly, which should be fairly easy.***

We need to calculate the number of photons emitted per unit time:

The energy of one photon is given by: $E = hc/\lambda$, which is a given equation on the front of the paper.

As λ =530 nm, we have $E = 3.75 \times 10^{-19}\,\mathrm{J}$ (or 2.35 eV)

Optical power is 40 mW, thus the number of photons emitter per second is

$$n_{photon} = \frac{4 \times 10^{-2}}{3.75 \times 10^{-19}} = 1.07 \times 10^{17}\,\mathrm{s}^{-1}$$

The number of recombination events per second is simply given by the number of electrons injected into the device: $n_{recomb} = \dfrac{I}{q} = \dfrac{3.5 \times 10^{-1}}{1.6 \times 10^{-19}} = 2.19 \times 10^{18}\,\mathrm{s}^{-1}$

Thus the external efficiency is given by $\eta_{ext} = \dfrac{n_{photon}}{n_{recomb}} = 4.9 \times 10^{-2}$ or 4.9%

ii) ***The wall plug efficiency again is defined and should be trivial:***

We are told that the wall plug efficiency is Power out divided by power in. Hence:

$$\eta_{wallplug} = \frac{OptPwr}{IV} = \frac{4 \times 10^{-2}\,\mathrm{W}}{3.5 \times 10^{-1}\,\mathrm{A} \bullet 3.4\mathrm{V}} = 3.4 \times 10^{-2} \text{ or } 3.4\%$$

iii) ***The last part requires some understanding and is essentially hidden***

The difference is that the external efficiency considers only the conversion of current into optical emission, and pays no attention to voltage drops in other parts of the device, other than that across the junction. There are resistive losses at the contacts and in the p- and n- layers that lead to additional voltage drops which reduce the wall plug efficiency compared to that of the external efficiency of the device.

1.c. [Hidden]

This is a variant on a theme explored in last year's examination that was done poorly. Ga is a group III element and N is a group V element thus across each pair of atoms we have eight shared outer electrons – as for silicon. If we replace a Ga atom with group II magnesium then there is one less electron in the bonding state and we will have a hole that can move around the lattice. If we replace a Ga atom with Si then there will be an additional electron provided to the crystal that will not be required for bonding and this will be able to move into the conduction band and hence move freely around the GaN crystal.

2.a. [Bookwork]

In a metal, or conductor carriers are freely moving around the material due to their thermal energy, which translates into kinetic energy. There is no barrier to overcome for the outermost electrons to

leave their host atoms and hence there is a high density of free carriers in the material giving a low resistivity.
In a semiconductor the electrons are tied up in chemical bonds, but some electrons can escape due to thermal energy at room temperature giving some conductivity both due to free electrons and also holes due to the gaps in the electron population in the bonds. Normally the density of free carriers is quite low, but it can be increase by doping.
In an insulator the electrons are not free to move as there are tied up in the chemical bonds of the material. The energy required to lift electrons out of the bonds however is very much greater than the thermal energy and as a result there are very very few free carriers in the material, giving its insulating properties.

2.b. [Bookwork]

The splitting of the question into three is more to assist students to answer all the points in one general topic in this case and an overall model answer is given here:
An intrinsic semiconductor is one in which all the free carriers are created through thermal generation, whereas in an extrinsic semiconductor the density of free carriers is modified by doping the material with a suitable impurity. In an intrinsic semiconductor the density of carriers is quite low and there will be equal numbers of electrons and holes. In an extrinsic semiconductor the density of carriers is usually many orders of magnitude higher than that of intrinsic material and, depending on the dopant used the density of one carrier type will massively dominate over the other.

2.c. [Applied Bookwork - fairly obscure]

Variant of a question asked about copper last year. As temperature increases the carrier concentration in the doped Si will remain the same, being defined by the donor density. However, the mobility of the material must decrease due to the increased amount of scattering caused by to the increased amount of vibrations (phonons) in the Si Crystal. As the mobility decreases and the carrier concentration remains the same so the resistivity of the material must increase.

2.d. [Problem]

This problem is similar to a two mark question last year and hence should be fairly easy]
In order to solve this problem we need to calculate the resistivity of the Si at 50^0C, an increase of 30^0C.
The resistivity will increase by an amount $\alpha \bullet \delta T = 5.2\times10^{-7} \bullet 30 = 1.56\times10^{-5}\,\Omega\text{m}$
Thus the new resistivity will be $(1.563+0.156)\times10^{-4} = 1.719\times10^{-4}\,\Omega\text{m}$

2.e. [Hidden]

This question has some similarities to a question I asked last year that was generally not well done. The difficulty in it though it a little different.
We are given an equation describing the variation of temperature in the rod. We also know from 2(d) the relationship between temperature and resistance.
The equation for temperature is: $T(x) = 20 + 400x - 1000x^2$ which can also be written as $T(x) = T(0) + \delta T(x)$ and from 2.d. we know the resistivity at x=0 to be $\rho(0) = 1.563\times10^{-4}\,\Omega\text{m}$

Now we can also write $\rho(x) = \rho(0) + \delta\rho(x)$ and as $\frac{d\rho}{dT} = \alpha$ we can therefore say that $\delta\rho(x) = \alpha \cdot \delta T(x)$.
Substituting gives
$\delta\rho(x) = 2.8\times10^{-4}x - 5.2\times10^{-4}x^2$, hence
$\rho(x) = 1.563\times10^{-4} + 2.8\times10^{-4}x - 5.2\times10^{-4}x^2$

Now resistance is normally calculated by $R = \frac{\rho l}{A}$, and for a variable resistivity (due to temperature variation) we need to effectively sum all the resistances in small lengths of the rod to get the overall resistance. This means we must replace $\rho \cdot l$ term with the integration of the resistivity function with x, over the limits of the length of the silicon rod:

$$R = \frac{1}{A}\int_0^l \rho(x)dx = \frac{1}{A}\int_0^{0.1}\left(1.563\times10^{-4} + 2.8\times10^{-4}x - 5.2\times10^{-4}x^2\right)dx$$

$$R = \frac{1}{A}\left[1.563\times10^{-4}x + 1.4\times10^{-4}x^2 - 1.7\times10^{-4}x^3\right]_0^{0.1} = \frac{1}{1\times10^{-6}}\left(1.563\times10^{-5} + 1.4\times10^{-6} - 1.7\times10^{-7}\right)$$

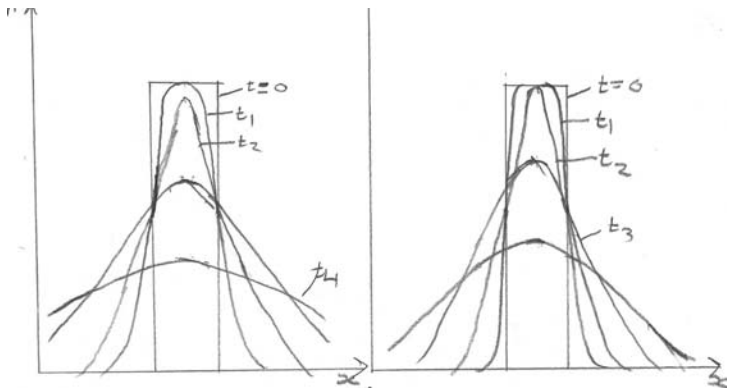
$$R = 16.9\Omega$$

3.a. [Applied Bookwork]

This part tests students understanding of three concepts in a way that requires them to think a little as this is one of the most fundamental parts of the course and fairly simple this should be easy.
In the figures below the behaviour of the electrons is on the left and the holes on the right in each case. As specified in the exam question the direction of the electric field is from right to left.

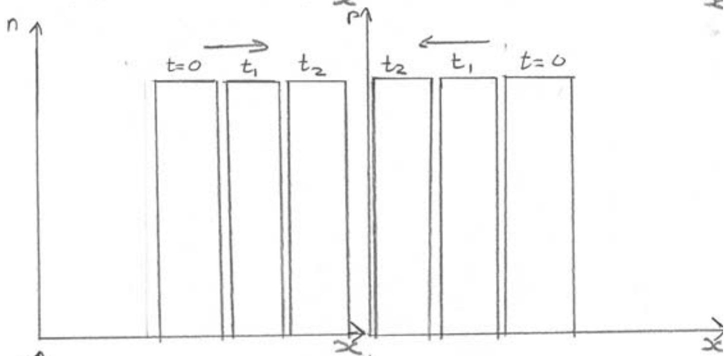
i) *Diffusion*

Diffusion will cause the electrons and holes to spread out to both sides equally with time as indicated below. Good students may point out that there may be some difference in the rate of diffusion of the electrons compared to that of the holes depending on the relative carrier mobilities. As there is no recombination the area under the curve should remain the same with time and the number of carriers does not change.



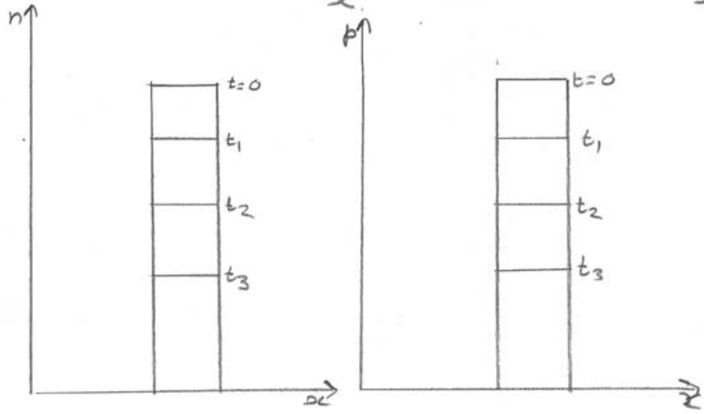
ii) *Drift*

Drift will move the electrons to the right in the opposite direction to the field, while holes will move to the left with the electric field. In the absence of Diffusion we would expect the carrier profile to remain unchanged.



iii) *Recombination*

As electrons and holes recombine the number of both the electrons and holes will decrease by equal amounts. Thus the concentration will decrease. The overall shape of the profile will remain unchanged and it will not move with respect to x as there is no diffusion or drift involved.



3.b. [Bookwork - Bit more advanced]

The base transport factor is a measure of the fraction of minority carriers injected from the emitter into the base that reach the collector. Ideally the value should be as near to one as we can make it. In this situation the concentration profile of minority carriers in the base will be a linear decrease from the injected value on the emitter side to essentially zero on the collector side of the base.

3.c. [Hidden - Problem leads directly on from 3.b.]

Assuming as indicated above that the base transport factor is one. Then the electron concentration, n in what must be an npn device will be a linear decrease, meaning dn/dx is a constant.

If we know dn/dx the we can substitute in the equation for the diffusion current to get the current density in the collector, using $J = qD_e \, dn/dx$, as the current density in the collector must equal that in the base if the base transport factor=1.

As the function is linear $dn/dx = \dfrac{n_{ee} - n_{ce}}{l}$ where n_{ee} is the density of excess electrons at the emitter end of the base, n_{ce} is the density at the collector end of the base (=0) and l is the base length.

Hence, $dn/dx = \dfrac{n_{ee} - n_{ce}}{l} = \dfrac{1\times10^{21}}{2\times10^{-6}} = 5\times10^{26}\,\mathrm{m^{-4}}$

Using the given equation for the diffusion constant (Einstein relation): $D_e = \dfrac{kT}{q}\mu_e$ and the given value for the electron mobility in Si we get: $D_e = \dfrac{1.38\times10^{-23}\cdot 300}{1.60\times10^{-19}}\cdot 0.12 = 3.11\times10^{-3}$ assuming the device is operating at room temperature.

The collector current density, will be: $J = 1.60\times10^{-19}\cdot 3.11\times10^{-3}\cdot 5\times10^{26} = 2.49\times10^{5}\,\mathrm{Am^{-2}}$

4.a. [Simple Problem]

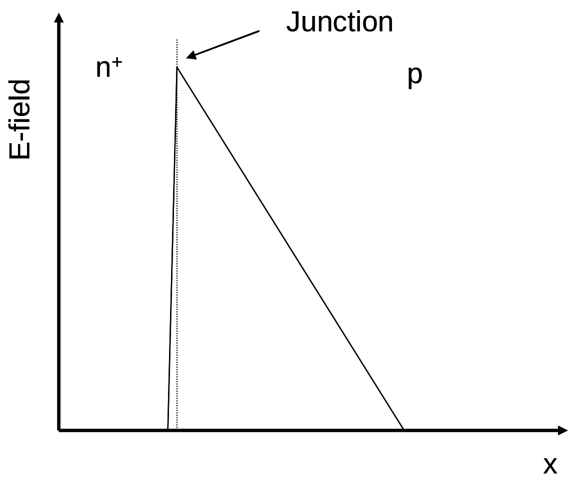
The equation for depletion region is given on the front – for a p^+-n junction. All students need to do is substitute the values in the question and those given in the question. A key point is remembering that we have an n^+-p junction in this case.

$$d_j = \left(\frac{2\varepsilon_o\varepsilon_r V_j}{qN_a}\right)^{1/2} = \left(\frac{2\cdot 8.85\times10^{-12}\cdot 12\cdot 0.7}{1.60\times10^{-19}\cdot 3\times10^{22}}\right)^{1/2} = 1.76\times10^{-7}\,\mathrm{m}$$

4.b. [Applied Bookwork]

The sketch should look something like the figure:

The E-field comes from the exposed donor and acceptor ion charges after the electrons and holes near the junction have recombined. As the donor ions are positive the field in this region will be positive and vice-versa



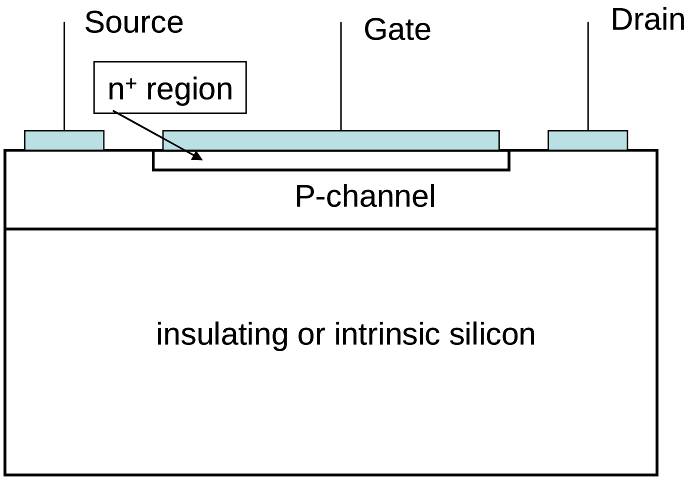
4.c. [Fairly Obscure Bookwork]

Breakdown is where the current rises rapidly with voltage once some critical value of reverse bias is exceeded. In avalanche breakdown the current rise is caused by the electrons and holes in the depletion region being accelerated by the field sufficiently that their kinetic energy is high enough to cause another electron to leave its bond when it interacts with it. This effect snowballs hence leading to the name avalanche.

4.d. [Applied Bookwork, and problem]

i) ***JFET structure***

This should be fairly easy bookwork. The device should look as follows. It must be a planar device it is specified to be prepared on an insulating piece of Si.



ii) ***Maximum channel thickness***

This is a problem that should be not too difficult as it basically reapplies the equation in the first part of this question, but involves recognition of the need to do so from the device knowledge.
In any JFET in order to be able to use it usefully we need to be able to pinch the channel off. Thus the maximum channel thickness will be given by the value of the depletion region thickness when the maximum possible voltage is applied. This is 60V as we must remain below the breakdown voltage.

$$d_j = \left(\frac{2\varepsilon_o\varepsilon_r V_j}{qN_a}\right)^{1/2} = \left(\frac{2\cdot 8.85\times10^{-12}\cdot 12\cdot 60}{1.60\times10^{-19}\cdot 3\times10^{22}}\right)^{1/2} = 1.6\times10^{-6}\,\mathrm{m}$$