EEE119 Digital System Engineering – Digital Logic Revision

1. (i) X(X'+ Y) = XX' + XY= 0 + XY = XY
   (ii) X + X'Y = (X + X')(X + Y) = 1.(X + Y) = (X + Y)

2. (X + Y + Z)' = X'Y'Z'
   (XYZ)' = X' + Y' +Z'

XYZ	X + Y + Z	(X + Y + Z)'	X'	Y'	Z'	X'Y'Z'
000	0	1	1	1	1	1
001	1	0	1	1	0	0
010	1	0	1	0	1	0
011	1	0	1	0	0	0
100	1	0	0	1	1	0
101	1	0	0	1	0	0
110	1	0	0	0	1	0
111	1	0	0	0	0	0

   From the truth table it can be seen that (X + Y + Z)' = X'Y'Z' , the duality principle confirms that (XYZ)' = X' + Y' +Z' as it is the dual of the first law.

3. F = X'Z' + YZ

XYZ	X'Z'	YZ	F
000	1	0	1
001	0	0	0
010	1	0	1
011	0	1	1
100	0	0	0
101	0	0	0
110	0	0	0
111	0	1	1

   F' = X'Y'Z + XY'Z' + XY'Z + XYZ'
   F = (X'Y'Z + XY'Z' + XY'Z + XYZ')'
   F = (X + Y + Z')(X' + Y + Z)(X' + Y + Z')(X' + Y' + Z)

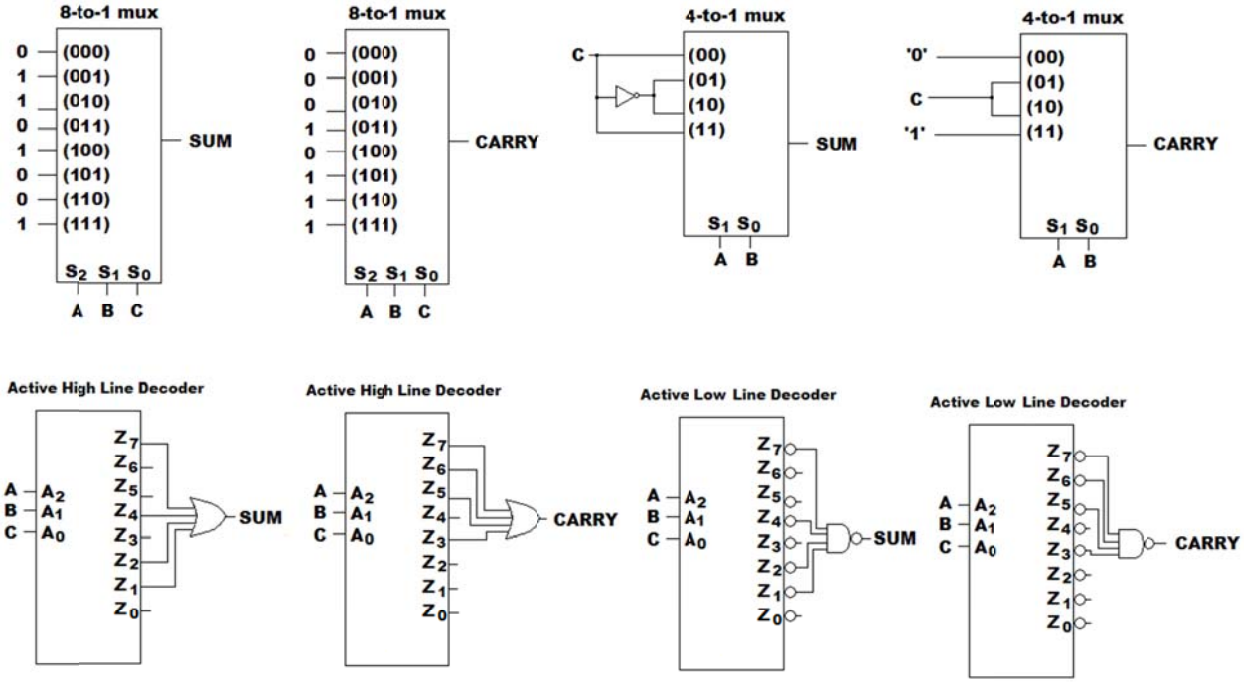
4. (i) 10100000 (ii) 10111101 (iii) 00011101 (iv) 11100010 (v) 01010011 (vi) 01001110

5. F = A'B + AB'

   Complement, F' = (A'B + AB')' = (A'B)'(AB')' = (A + B')(A' + B)
   Dual, F = (A' + B)(A + B') , hence equal.
   (Remember, AND is commutative)

6.

ABC	SUM	CARRY
000	0	0
001	1	0
010	1	0
011	0	1
100	1	0
101	0	1
110	0	1
111	1	1

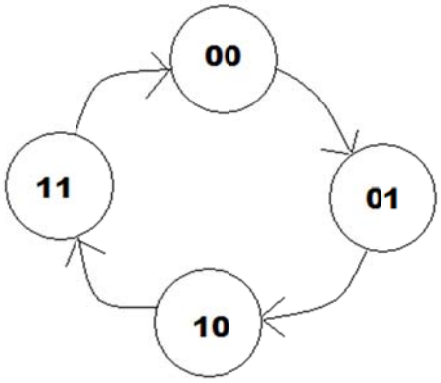


7. Perform the following calculations using 8-bit binary:

(i) 17 + 49 > 00010001 + 00110001 = 01000010
(ii) 57 – 23 > 00111001 – 00010111 = 00100010
(iii) 37 – 41 > 00100101 – 00101001 = 11111100 (twos complement for -4)

8. Design a sequential circuit which implements the two bit binary count sequence 00,01,10,11,00 etc

state diagram



state table

present state Q_1 Q_0	next state Q_1' Q_0'
0 0	0 1
0 1	1 0
1 0	1 1
1 1	0 0

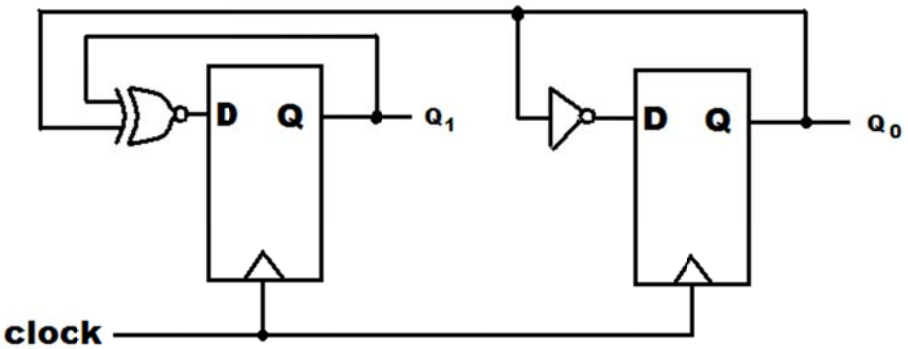
state equations

$$Q_0' = \overline{Q_0}$$

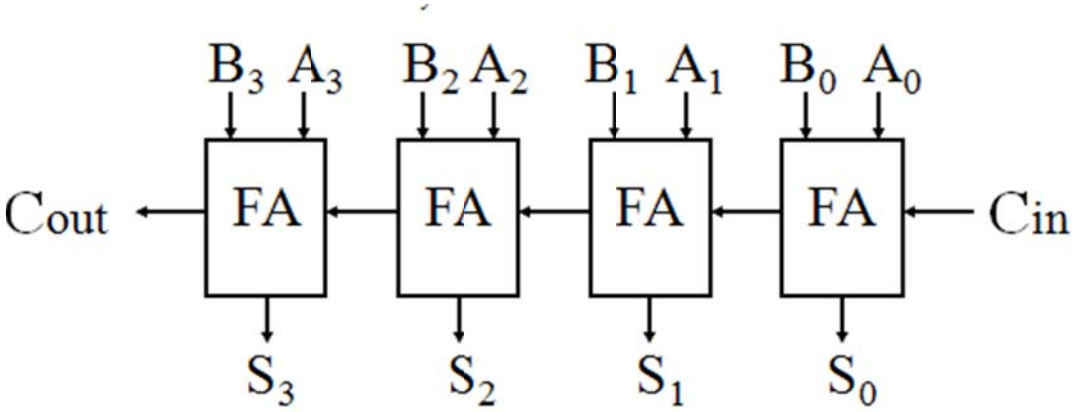
$$Q_1' = \overline{Q_1}Q_0 + Q_1\overline{Q_0}$$

$$= Q_1 \oplus Q_0$$

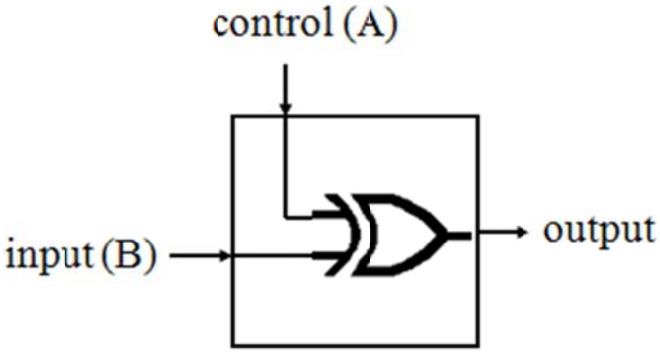
circuit diagram



9.



10.



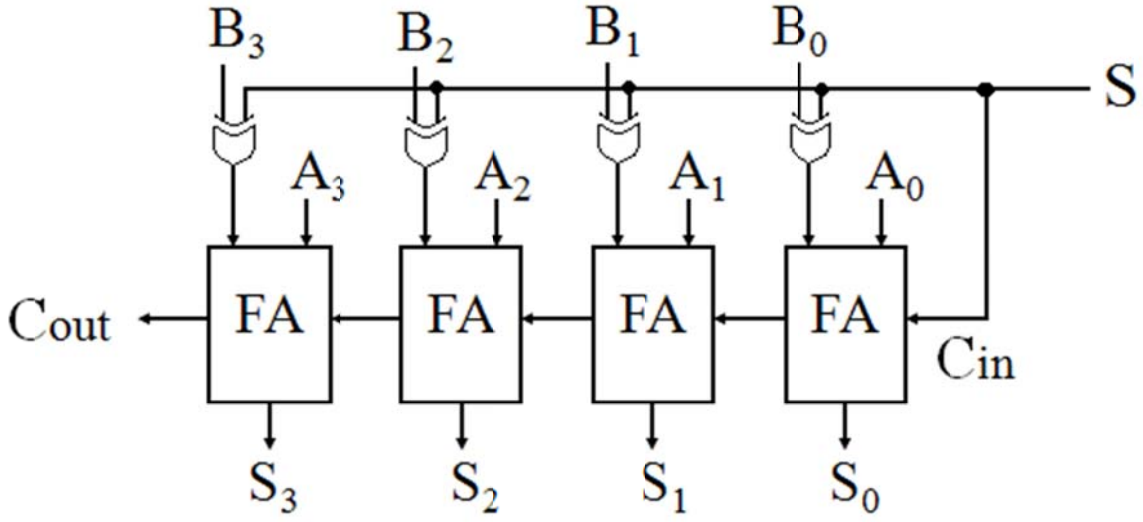
When the control line (A) is ‘0’ the input (B) is passed , when it is ‘1’ the input is inverted.

To produce the twos complement in hardware, invert all of the bits and add ‘1’.

For the add/subtract circuit, use the control line S to control the inverters and provide the ‘1’ to be added in.

When S = ‘1’, B will be inverted and 1 added in via the carry in, to form the twos complement of B, hence B will be subtracted from A.

When S = ‘0’, B will be passed straight to the adders and the carry in will be ‘0’, hence B will be added to A.



11. 01010111 > 01111100, 01011000 > 01110100 Remember that the MSB is the same in binary and Grey code. Four bits change in the consecutive binary sequence but only one bit changes between Grey codes as expected.