DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 1999-2000 (2 hours)

INTRODUCTION TO VLSI DESIGN

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

additional materials: 1 piece linear graph paper
figure 4(b)

1. You work for a chip supply company. One of your successful products is currently implemented as a gate array. Your sales department estimates the chip's market will exist for another two years and expects sales to continue at the current 30,000 chips per year for that period. Your manager wants to know whether it would be financially beneficial to convert to a cell based (standard-cell) implementation. Produce an argument to determine whether this is likely to be worthwhile. The information below is available. Not all of this is relevant and some vital numerical information is missing. In producing your argument, make it clear what numerical information is missing, but make sensible estimates for the relevant values in order to come to a conclusion.

   Note that it is important that you develop your argument clearly and logically in order to be awarded high marks

   (20)

   The cell based fabrication process requires 15 photolithography masks.
   The gate array process requires 6 design specific photolithography masks
   A typical photolithography mask costs 1600Euros
   The chip fabrication process you use is based on 6 inch (15cm) diameter wafers, where each costs 290Euros to process.
   The current implementation uses 75% of the cells on a 8x8mm gate array.
   The chip is already incorporated within several of your customers' products. Any change in package would require the customers to rework their PCBs, so this is not acceptable.
   1Euro ≈ £0.65

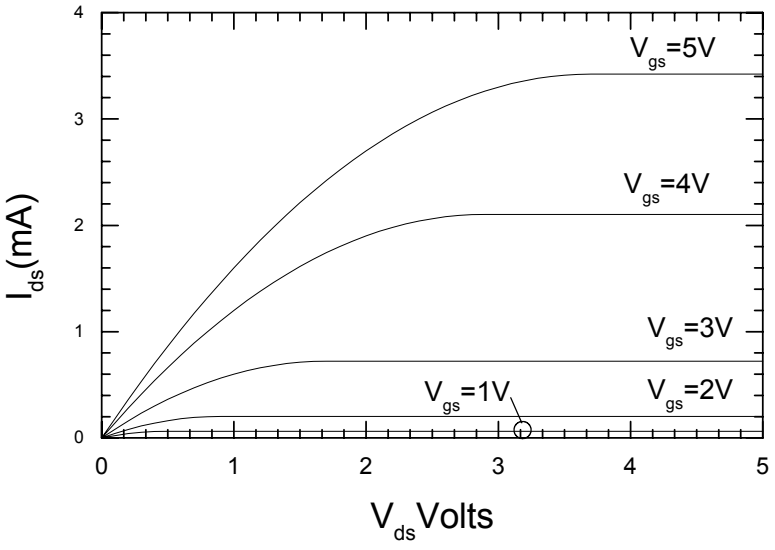
2. Figure 2 shows the measured characteristics of an n-channel and a p-channel MOSFET. Draw appropriate graphs to estimate the threshold voltages and values of β for these two devices.

   (8)

Consider an inverter made by connecting these two devices together in an appropriate manner with a supply voltage of 5V. Consider the situation where an input voltage is applied to the inverter such that the output voltage is equal to the input voltage. Show that in this condition both the MOSFETs are in saturation.

(4)

Estimate the value of this input voltage. **(8)**



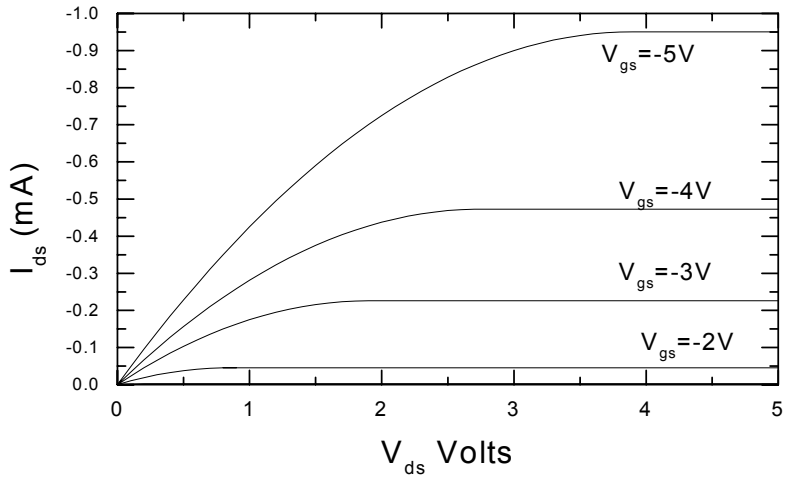


Figure 2

3. In the context of the testing of VLSI circuits, what is meant by the term "fault cover"? Explain why this is important.

(5)

Figure 3 shows a small circuit, where A,B and C are inputs and X and Y are outputs. How many tests would be required to carry out an exhaustive test of this circuit if we make no assumptions about the type and number of faults?

(4)

Demonstrate by developing a subset of the fault matrix that the set of tests ABC=000,111,001, 011,010 can provide 100% fault cover if we make the usual assumption of single stuck-at type faults (include the possibility that the input and output lines could be faulty).

(7)

Show that this is not the minimum set of tests that can provide 100% fault *cover (it is not required that you identify the minimum set of tests)* **(4)**

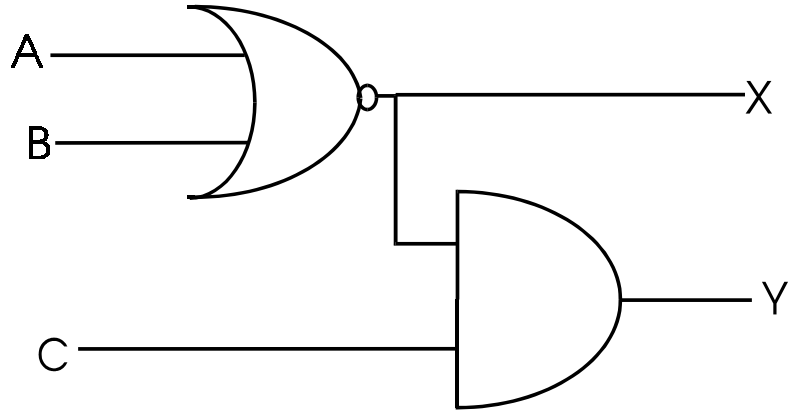


Figure 3

4. (a) Figure 4 (a) shows a tri-state output cell for a CMOS circuit. Explain how this works and why it is preferable to designs involving pass transistors.

(6)

(b) In a particular example of this type of cell, the output transistors are designed such that when "enable" is on the cell can drive a load capacitance of 100nF with rise and fall times of 2nS and 1nS respectively. What must the minimum width of the p-channel transistor be? You may use any of the information below that is relevant. **(8)**

ε for silicon dioxide = $2x10^{-11}$ F/m
oxide thickness in this oxide process is 10nm
Vdd=5V
Threshold voltage for the p-channel transistor is -1V
minimum gate length is 0.5μm
hole mobility = $0.04m^2/Vs$

(c) Figure 4(b) is supplied as additional material and shows a stick figure of the structure of one cell of a gate array. Onto this figure draw the metal tracks (in level 2 metal) that need to be added to implement this cell as a two input NAND gate.

(6)

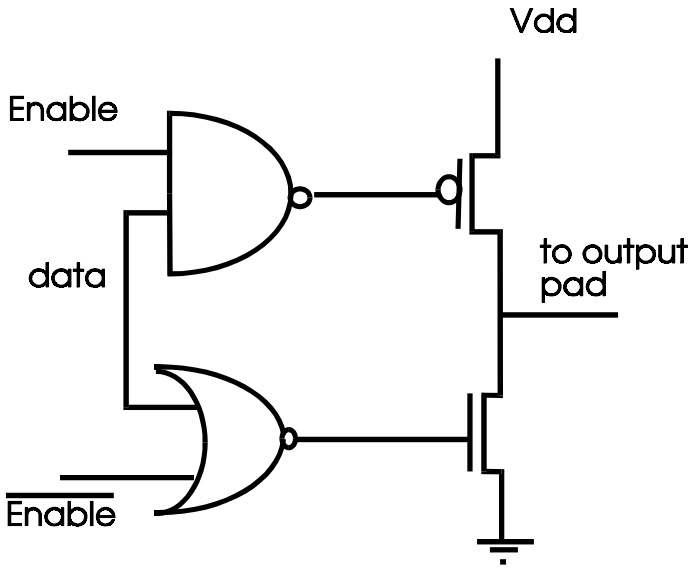


Figure 4 (a)

END OF QUESTION PAPER