The University Of Sheffield.

Electronic & Electrical Engineering.

EEE339 DIGITAL ENGINEERING

Credits: 20

Course Description including Aims

The aim of this module is to provide students with a fundamental understanding of synchronous digital systems. This is done in conjunction with the Verilog Hardware Description Language (HDL) and particular emphasis is placed on the architecture and organisation of a basic microprocessor. This module also considers digital signal processing.

1. To introduce the Verilog HDL and gain a working knowledge of its application to the modeling, simulation and synthesis of digital systems.
2. To develop a solid understanding of synchronous digital systems with an awareness of performance limitations and implementation issues.
3. To obtain detailed knowledge of the architecture and organisation of a basic microprocessor and its peripheral interfaces.
4. To introduce fundamental ideas of digital signal processing (DSP), its limitations and its advantages.
5. To give the student a working knowledge of basic DSP operations, as well as a solid theoretical understanding of their behaviour.
6. To make the student aware of the options available when constructing a DSP system.

Outline Syllabus

Verilog HDL: syntax, simulation, synthesis, digital building blocks, finite state machines. **Microprocessors:** Instruction Set Architecture (ISA), functional behaviour, internal organisation. **Peripherals:** memory hierarchy, memory cycles, Direct Memory Access (DMA). **Operations:** arithmetic, floating point representation, addressing modes, stacks, interrupts. **Processor Architecture:** ALU, registers, data path design, RISC, CISC. **Processor Control:** Hardwired, microprogrammed. **Microcontrollers & DSP:** Architecture, practical examples. **Discrete-time**: signals and systems, z-transform, sampling of continuous-time signals, discrete-time Fourier transform (DTFT), transform analysis of linear time-invariant (LTI) systems, structures for discrete-time systems, discrete Fourier transform (DFT), fast Fourier transform (FFT). **Filters**: finite impulse response (FIR) filter design techniques: window method and frequency sampling method, infinite impulse response (IIR) filter design techniques: impulse invariance method and bilinear transform method.

Time Allocation

48 lectures, 24 hours of other material.

Recommended Previous Courses

EEE119, EEE224, EEE225.

Assessment

3 hour examination, answer 5 questions out of 8

Recommended Books

Mano & Kime	Logic and Computer Design Fundamentals, 4/E	Prentice-Hall
Gajski, D D	Principles of Digital Design	Prentice-Hall
Ciletti, M D	Advanced Digital Design with the Verilog HDL 2/E	Prentice-Hall
Floyd, T L	Digital Fundamentals	Prentice-Hall
Ifeachor & Jervis	*Digital Signal Processing - A practical approach*	(Addison-Wesley)
Proakis & Manolakis	*Digital Signal Processing - Principles, algorithms and applications, second edition*	(Macmillan student edition)
Meddins, B	*Introduction to digital signal processing*	(Newnes)
Mulgrew, Grant and Thompson	Digital signal processing : concepts and applications	(Palgrave Macmillan)
Oppenheim and Schafer	Discrete-time Signal Processing	(Prentice Hall)

Objectives

On completion of this module successful students will be able to

1. Analyse a synchronous digital system described schematically or in Verilog.
2. Design a small synchronous digital system.
3. Be aware of implementation issues and factors that limit performance.
4. Understand and explain the basic structure and operation of a digital computer.
5. Identify and describe the functional requirements of a (micro) processor and peripherals.
6. Understand and explain the internal organisation of different types of processors.
7. Understand the necessary changes of choosing a digital solution when processing signals.
8. Understand and exploit the relationship between the time and frequency domain representations of linear time-invariant (LTI) discrete-time systems and the signals passing through them.
9. Design simple FIR and IIR filters to satisfy desired performance specifications.
10. Demonstrate a broad knowledge of well-known digital signal processing tools.

Detailed Syllabus

lecture	topic
1	**Verilog:** Concepts, hierarchy, structure, behavior
2	**Verilog:** Types, syntax, synthesisable subset
3	**Verilog:** Event driven simulation, test benches
4	**Verilog:** Fundamental digital building blocks
5	**Verilog:** Register Transfer Level (RTL)design, Finite State Machines (FSM)
6	**Implementation**: ASIC, FPGA architectures, design methodology
7	**Computer Arithmetic:** Data representation, addition, subtraction
8	**Computer Arithmetic:** Serial & Parallel multiplication, Booth's algorithm
9	**Computer Arithmetic:** Restoring and non-restoring division algorithms
10	**Computer Arithmetic:** Floating point unit
11	**Memory:** Classification and organisation, SRAM, DRAM, performance
12	**Microprocessor:** Instruction Set Architecture (ISA)
13	**Microprocessor:** Datapath elements
14	**Microprocessor:** Control, microcoding

15 **Microprocessor:** Pipelining and performance
16 **Microprocessor:** Stack architectures
17 **Microprocessor:** Interrupts
18 **Microprocessor:** Direct Memory Access (DMA)
19 **Microprocessor:** Architectural alternatives, RISC, CISC
20 **Microcontroller:** Architectures, peripherals
21 **Digital Signal Processor:** Architecture, practical example using convolution
22 **Direct Digital Synthesis (DDS):** Look up tables
23 **Introduction to DSP**, what it is, why we use it.
24 **Basic discrete-time signals/sequences and operations**: unit sample sequence, unit step sequence, exponential sequence, sinusoidal sequence, differences between discrete-time and continuous-time complex exponential or sinusoidal sequences (frequency range, periodicity).
25 **Discrete-time systems**: ideal delay system, moving average system, memoryless system, linear system, time-invariant/shift-invariant system, causal system, stable system.
26 **Linear time-invariant (LTI) system**: impulse response of an LTI system, convolution, why an LTI system is completely characterized by its impulse response, properties, FIR system, IIR system.
27 Linear constant-coefficient difference (LCCD) equations, frequency-domain representation of discrete-time signals and systems, frequency response of an LTI system, sinusoidal response of an LTI system.
28 **Discrete-time fourier transform** (DTFT), properties of DTFT, DTFT and the frequency response of an LTI system.
29 **Z-transform**, its relationship with DTFT, region of convergence (ROC), pole-zero plot.
30 Properties of ROC, inverse z-transform (inspection method, power series expansion).
31 Properties of z-transform (focused on its application to convolution of sequences in time-domain).
32 **Sampling of continuous-time signals**, periodic sampling, Nyquist sampling theorem, reconstruction of the continuous-time signal, discrete-time processing of continuous-time signals, and continuous-time processing of discrete-time signals.
33 **Transform analysis of LTI systems**: frequency response of an LTI system (ideal frequency-selective filters, phase distortion and delay), system functions for systems characterized by LCCD equations (stability and causality, inverse systems).
34 **Impulse response** for rational system functions, frequency response for rational system functions, frequency response of a single zero or pole, frequency response of multiple poles and/or zeros.
35 **Structures for discrete-time systems**: block diagram representation of LCCD equations (addition of two sequences, multiplication of a sequence by a constant, unit delay), direct form I and direct form II implementation of an LTI system.
36 **Discrete Fourier transform (DFT)**: DFT defined on finite duration sequences, DFT as sampling of the DTFT, properties of the DFT.
37 **Circular convolution**, linear convolution using the DFT for two finite-length sequences, implementing LTI systems using the DFT (overlap-add method).
38 **Fast Fourier transform (FFT)**: decimation-in-time algorithm for sequence length being the power of two, summary of Fourier-related transformations (complex Fourier series, Fourier transform (for continuous signals), DTFT, DFT).
39 **Design of IIR filters I**: filter design specifications (passband, stopband, transition band), impulse invariance method,
40 **Design of IIR filters II**: bilinear transform method, comparison of the bilinear transform method with the impulse invariance method, IIR filter design for highpass and bandpass filters.
41 **Design of FIR filters I**: linear phase shift characteristic, Gibbs phenomenon, window method.
42 Design of FIR filters II:, frequency sampling method, relative advantages and disadvantages of FIR/IIR filters:
43 **Review Lecture 1**

UK-SPEC/IET Learning Outcomes

Outcome Code	Supporting Statement
SM1p / SM1m	Fundamental ideas of digital signal processing and related math, sampling process/theory, digital systems vs. analogue systems. (assessed by examination)
SM2p/SM2m	Data representation is covered including number systems and codes. Integer and floating point numbers are examined. Algorithms for computer arithmetic and digital signal processing are developed. Boolean algebra is used throughout to analyse and design digital components. Convolution, LCCD equations, z-transforms and Fourier-related transforms, and their application to FIR/IIR filter design problems. (assessed by examination)
SM5m	Algorithms for multiplication and division are examined. Hardware solutions are developed and trade-offs considered. Floating point arithmetic is examined and limitations considered. Verilog models of digital functional blocks are developed. The relationship between the constructs used in the Verilog model and the synthesised circuit are examined. Implementation of mathematical functions using look up tables is examined.
EA1p/EA1m	Design flow and methodology for digital systems, using a hardware description language, is examined. Principles for the correct use of Verilog for synthesis are established. Synchronous design techniques are encouraged throughout. Simulation using Verilog models is examined in detail. Fourier analysis for the filtering operation and the sampling process, and analysis of the frequency response of LTI systems; comparison and critical analysis of different FIR/IIR design methods. (assessed by examination)
EA2m/EA2p	Circuit performance is examined (speed/area/power). Algorithms for computer arithmetic are developed and analysed to investigate performance. Alternative microprocessor architectures are considered and compared for performance.
EA3p/EA3m	Design of FIR/IIR filters, draw frequency response of filters using MATLAB. (assessed by examination)
EA4m/EA4p	A top down approach is applied to the examination of computer architectures. Lower level components are developed and integrated to form a microprocessor.
D4p/D4m	Advances in computer architectures and arithmetic have involved creativity to overcome problems. This is highlighted throughout the course.
EP2p/EP2m	Electronic Design Automation (EDA) tools: Verilog modelling, simulation and synthesis are examined in detail. FPGAs are considered for implementation.
EP4p/EP4m	Use of data sheets for memory and microprocessors. Review of instruction set for microprocessor.