Data Provided: None

EEE310

The University of Sheffield

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2001-2002 (2 hours)

Introduction to VLSI

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. Show that a simple expression for the *dynamic* power dissipation of a CMOS circuit due to switched capacitance is:

$$P_{sw-cap} = \alpha C_{load} V_{DD}^{\ 2} f$$

(ensure that you define the meaning of each of the terms) **(4)**

Identify and comment briefly on the other two major sources of power dissipation in a CMOS circuit. **(4)**

An IC, with a supply voltage of 1.8V, contains the equivalent of 5 million 2-input minimum-sized NAND gates and a minimum-sized *n*MOSFET in the circuit has a gate length of 0.18μm and a gate width of 0.4μm. The ratio of electron to hole mobility is 2:1 and the gate oxide ($Si0_2$, ε=3.45x10^{-11}F/m) thickness is 10nm. It is calculated that the total length of the interconnect between the gates over the surface of the IC is 1000m and the average width/height of the interconnect is 0.5μm/0.8μm. The permittivity of the dielectric around the interconnect is 4x10^{-11}F/m and the average spacing around each conductor is 0.5μm. Functional simulations show that each interconnect toggles with a probability of 0.125 in any clock cycle and the IC runs at a clock frequency of 600MHz. Furthermore, circuit simulations indicate that power dissipation due to switched capacitance accounts for 80% of the total power dissipated by the IC.

Estimate the power dissipation of the IC. **(12)**

2. Discuss the factors that affect the manufacturing cost of a packaged ASIC and, where appropriate, quote expressions that model these factors. Show how these factors are combined to yield the overall cost. **(4)**

Time-to-market is a critical in the introduction of an ASIC to the market – explain, simply, why this is the case? **(4)**

How is the semiconductor industry seeking to minimise the time-to-market and what factors make this difficult? **(4)**

A design company is designing an 1M transistor ASIC and is faced with a number of options for designing and manufacturing the ASIC – each of which has the characteristics shown in Table 2.

Designer cost = \$0.5M / person / year

Device Type	Manufacturing NRE (\$)	Cost Per Part (\$)	Minimum Order Quantity	Designer Productivity T/p/y
FPGA	0	1000	1	218400
MGA	50000	10	20000	136500
CBIC	200000	5	50000	91000

Table 2

Find the volume of production at which it would be better to switch from FPGA to MGA and from MGA to CBIC and find the overall cost per ASIC at these volumes of production. **(6)**

Calculate the best, overall cost per ASIC if the volume of production is 1 million devices. **(2)**

3. Derive an expression for the value of the input voltage to an inverter at which the input voltage is equal to the output voltage (using the standard equations and terms that link V_{GS}, V_{DS}, and I_{DS}). **(3)**

What will the value of this input voltage be if V_{TP}=-V_{TN} and if the transistors are sized such that β_P=β_P? **(1)**

What is metastability and what is its effect on a circuit? **(2)**

The effect of metastability is characterised by $upsets/s = T_0 e^{-\frac{t_r}{t_c}} f_{clk} f_{data}$ Explain what the terms mean and from where they arise. **(2)**

Explain how the effect of metastability can be reduced and how this is achieved in practice. **(2)**

An IC in a system simply samples an external 8-bit data bus to read data that is asynchronous to the clock of the IC. The clock frequency of the IC is 50MHz and the effective frequency of the data is 23MHz. T_0=5ns, and t_c=1.5ns: Calculate the *upsets per second*. **(2)**

It is noticed that this value is far too high. The designer also notes that 10000 such systems must be deployed and that only one failure every five days (due to metastability) across the systems deployed can be tolerated. What would the design of a metastable-resistant sampler be that would meet this requirement? **(8)**

4. A logic gate is to be designed to implement the function:

$$Y = \overline{A.(B+C)}$$

Show how a standard CMOS circuit would be designed to implement this function. You should draw a schematic of the circuit and your answer must consider the sizing of transistors. **(8)**

Estimate the switching time of the unloaded output of this gate.
(μ_E=0.08m^2/Vs, μ_H=0.04m^2/Vs, t_{OX}=10nm, W_{min}=1μm, L_{min}=0.25μm, ε=3.45x10^{-11}F/m, V_{DD}=3.3V, V_{TN}=-V_{TP}=0.6V) **(6)**

A logic gate produces an output signal that must drive a large capacitance, C_{load}, but, obviously, a small gate will suffer large rise/fall times and delays. How can this delay be minimised. **(6)**