The University Of Sheffield.

Electronic & Electrical Engineering.

EEE160 First Year Laboratory

Individual Constructional Project

1: Background

During last semester's FYGER competition, you will have observed at first hand the problems that can occur due to the wire leads becoming entangled. To overcome this problem a "wireless" communication system that uses modulated infra-red (IR) signals is being developed. The system under development consists of three parts

1. a circuit capable of transmitting a coded infra-red signal
2. a circuit to receive and demodulate the coded infra-red signal
3. a decoder circuit to extract the required information from the demodulated signal

Before integrating the new system into FYGER, we must be sure that a high proportion of first year students can build a working system.

Your task, therefore, is to build the second of these parts, to check that it works, and to comment on its suitability for implementation with FYGER next academic year. Constructive criticism of the design and suggestions for improvements would be welcome. There are a number of questions in italics in various parts of this text - they are issues that you should consider. Your tutor may probe the depth of a selection of your considerations on these issues.

2: Aims and Objectives

The aim of this project is to give you experience in understanding, building, testing and, if necessary, fault-finding a circuit of significant complexity. You will gain experience in recognising and handling electronic components, soldering, test and measurement of your circuit performance, managing your time effectively, collecting and interpreting information, using your engineering knowledge in some design tasks and producing written and oral reports for your tutor.

3: Project Timetable

In the laboratory timetable, already circulated, there are dark and light shaded afternoon slots. You should attend all the dark shaded afternoons timetabled for your laboratory group unless you have agreed with a demonstrator that you have completed the work you have to do. The light shaded afternoons are available for you to work on the project if you need extra time and if space is available. Note

- the laboratory closes at 5.00pm - which means you will be asked to begin to clear up a few minutes before 5.00pm.
- **no afternoons other than those timetabled will normally be available!**
- the level of technical supervision available during the shaded afternoons may vary and may be completely absent during lightly shaded slots.

- The space available for project work, i.e. benches not in use for other experiments, is limited. Priority will be given to groups with a dark shaded timetable slot; others will be accommodated on a first come first served basis.

If you have prior constructional experience **and** do what preparation you can before you come to the lab, you could probably build and test this system in two to three afternoons. Our experience is, however, that it is more sensible for you, even if you consider yourself an expert, to plan spending at least four afternoons on your project. If you have no previous experience with this type of project, plan on using all the time available. You should always plan to leave time to deal with unexpected problems.

4: Preparation

Before coming to the laboratory to start your project, there are some issues that you can deal with.

4.1 Getting a feel for the circuit: Look at the circuit diagram and see if you can work out what the various stages are supposed to do – concentrate particularly on the receiver circuit, figure 2. The notes in **Section 5** should help you, although they are not supposed to be detailed system descriptions. It is not initially necessary to understand what every single component does, although your curiosity should drive you to find out the purpose of most of the components by the end of the project. To start with, try and identify the individual functional blocks in the design.

4.2 Choosing a carrier frequency: Next, you need to decide on the sub-carrier frequency of your system. The IR frequency ($\approx 300 \times 10^{12}$Hz) is the carrier in this system. Your information is carried on a much lower frequency - a sub-carrier lying somewhere between 40kHz and 100kHz - which modulates the IR carrier and which is itself modulated by the digital code. When used with FYGER, each group must be allocated its own significantly different frequency - *can you think of any reasons why?* - so you should choose the appropriate frequency from the table below:-

First letter of surname or family name	FREQ	C_{12}	C_{15}
A to B	41kHz	680pF	680pF
C to G	50kHz	470pF	2.2nF
H to L	60kHz	330pF	1.5nF
M to Q	71kHz	470pF	1.5nF
R to T	79kHz	390pF	1.5nF
W to Z	88kHz	330pF	1.5nF

4.3 Find required L: For the receiver circuit (figure 2), work out the value of inductance needed in parallel with the C_{12} and C_{15} value given in the table to give the resonant frequency allocated to you. The values from which you can choose are 2.2mH, 2.7mH, 3.3mH, 4.7mH, 10mH, and 22mH, all with a tolerance of ± 5%.

4.4 Defining the q factor: For the receiver circuit (figure 2), work out the value of R_9, R_{15} and R_{16} that will give a -3dB bandwidth of 7.5kHz in each resonant circuit. The resistors, R_{15} and R_{16}, should be of equal value in order to set up the proper bias for T_5 and T_6. R_{15} and R_{16} appear to be in parallel with each other and with the resonant combination C_{15} L_2 from a signal point of view so the R you calculate to get the required q must be modified appropriately to get a value for R_{15} and R_{16}. Choose a suitable resistor from the E12 "preferred value" series, these values being 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8 and 8.2, multiplied by an appropriate factor of 10.

4.5 Predicting behaviour: Plot a graph of |gain| in dB (ie., 20log|gain|) against log frequency - a graph known as the amplitude response - that you would expect from each resonant circuit, and for the two circuits in series, assuming a voltage input applied at the test point TP1. Plot your responses over the frequency range 10kHz to 400kHz. You then have a theoretical ideal against which to compare your real circuit. If you prefer you can produce the plot with the aid of a computer. The gains of the first and second stages are very approximately given by:

$$gain\,of\ \ first\ stage \approx 2.0x10^{-3} R_9 . \frac{jf\,/(f_0 q)}{1-(f\,/\,f_0)^2 + jf\,/(f_0 q)} \qquad (4.1)$$

$$gain\,of\ \ second\ stage \approx 4.5x10^{-3} R_{15}\,//\,R_{16} . \frac{jf\,/(f_0 q)}{1-(f\,/\,f_0)^2 + jf\,/(f_0 q)} \qquad (4.2)$$

The constant before the resistor in the gain expression is dependent on the parameters of the particular transistors used and may deviate markedly from the value given, particularly for the second stage. The frequency dependent part is the same in both cases; f is frequency variable in Hz, f_0 is the resonant frequency in Hz, q is quality factor and j is the normal j operator used in complex number expressions. Remember that if you have two circuits in series, you can get the overall gain in dB by adding the gain of the first circuit in dB to the gain of the second circuit in dB.

If you have access to a circuit simulation package you can try simulating the circuit behaviour as well.

5: The circuits

The system consists of three circuit boards, the transmitter, the receiver and the decoder. Figures 1, 2 and 3 show the circuit diagrams for these sections. Figures 1 and 3, the transmitter and decoder, have been built by us for you and a number of these are available to you for test purposes – more is said about these in the "encoder" description in section 5.1.4 below. Even though you are not constructing these circuits, your tutor might be interested to learn how they work so you should be prepared to explain their operation. Figure 2 is the circuit diagram of the receiver you are to build and test.

The following notes give guidance as to how the modules work, but you are expected to read around the subject to improve your understanding. Any questions included here are to aid your thinking. It is not intended that you should necessarily specifically address these during the assessment.

5.1: Transmitter

5.1.1 Oscillator: The oscillator, consisting of U_1D and its associated circuitry, is based on a standard *RC* circuit using an inverting Schmitt trigger. Its operation is described in most text books (look for index entries like "astable multivibrator", "square wave generator" and "relaxation oscillator") although the description might be centred around an op-amp version of a Schmitt trigger rather than a logic circuit.

5.1.2 Divide-by-2 circuit: This standard flip-flop circuit, centred around U_2, divides the oscillator frequency by 2. U_2 is a dual D-type flip-flop circuit but only one half is used. *What advantages might be gained by dividing the signal by 2?.*

5.1.3 Infra-Red LED Driver: The purpose of this circuit is to convert the output voltage of the oscillator into an oscillating current through the IR LED. Those of you who study EEE118 will already have some understanding of how the LED works. For those of you who don't, the LED is like any other light bulb in so far as a bigger current through it leads to more light production -

within reason, of course! *What current will flow through the LED when the transistor is "on"? Can you see any light coming out? If not, why not?*

DO NOT POINT THE IR LED DIRECTLY INTO YOUR EYES AT SHORT RANGE

5.1.4 Encoder circuit: this is a commercial IC chip that sends an encoded version of an 8-bit address unique to your transmitter, plus four data bits. Twelve sets of transmitter and decoder units have been constructed by us. Each set is capable of operating at any of the six operating frequencies, adjustment being made by turning the frequency adjustment knob. Twelve different codes have been used for these twelve transmitter/decoder sets so it is vital that you choose a matching transmitter and decoder. The match is determined by two factors:

(a) a coloured disc (six colours) in the frequency control knob of the transmitter and a matching disc on the decoder

(b) the colour of the power on led (2 colours) which must be the same on transmitter and decoder.

5.2: Receiver

5.2.1 Photodiode Receiver and amplifier: The photodiode, D_1, is reverse biased. Changes in the reverse current in the photodiode caused by the incident light are fed via C_6 into the amplifier. Both amplification stages are examples of "cascode" amplifiers- *see what you can find out about cascode amplifiers*. The first stage, T_1, T_2 and their associated circuitry, is a "folded" cascode amplifier circuit and the second stage, T_3 and T_4, is a normal cascode amplifier using a junction field effect transistor as the amplifying element. Both these circuit shapes have a number of desirable characteristics and are frequently used inside operational amplifiers. Both reduce the Miller effect which is always a potential problem in medium to high frequency amplifiers. *See what you can find out about the Miller effect - a book is less likely to give you a misleading idea about Miller effect than the web.*

5.2.2 Resonant Filters: Two resonant *LC* filters are used in this design. One forms the load circuit for the folded cascode amplifier and the other forms the load for the normal cascode pair. The signal equivalent circuit of a cascode amplifier output is a current source in parallel with a large resistance (plus some components of secondary importance that give rise to problems like the Miller effect) so a parallel resonant circuit is the appropriate form for the load. It is important that the resonant frequency of each circuit is the same as the transmitter frequency. *Why are these filters necessary? Have you plotted the expected frequency response of your tuned amplifier?*

5.2.3 Detector: The purpose of the detector circuit is to extract the digital modulation code from the high frequency sub-carrier. (The photodiode has already separated the sub-carrier from the IR carrier.) The circuit consists of a push-pull emitter follower buffer amplifier, T_5 and T_6, followed by a diode clamp (C_{19}, D_4 and R_{18}) which is in turn followed by a peak detector (D_5, C_{20} and R_{21}). The diode clamp defines the potential at the lowest point of the waveform as one diode drop below 0V and the peak detector then provides an output that approximates to the original input signal. R_{19} limits the peak current that can flow through T_5, C_{19}, D_5 and C_{20} on a rising signal edge at TP4. The output of the peak detector can reach almost 10V under strong signal conditions so R_{20} and D_6 are included to limit the detector circuit output voltage to a safe level for the decoder chip. The correct choice of time constants for the clamp and peak detector is very important if the circuit is to achieve its goals. R_{23} protects D_6 against inadvertent connection of +12V to the output connector post.

5.3 Decoder

The decoder is a commercial 5V logic IC that matches the encoder IC used in the transmitter. To operate correctly, the 8-bit receiver address must be identical to the transmitter address. The green LED indicates a successful transmission, and the red LEDs indicate the data that has been decoded.

6: Construction and testing

6.1 Construction

Some general guidelines on circuit construction are supplied separately. Please try to follow these, as they lead to a neater job that is more likely to operate correctly first time. Your tutor will want to look at your construction during the assessment, so it is a good idea to make it as neat as possible.

The layout plans of the receiver circuitry are shown in figures 4, 5 and 6. Figure 4 is a "solder side" or "track side" view of copper patterning on the board, viewed through the circuit board from the component side. Figure 5 is a component side view of the copper patterning - in this case a ground plane - and figure 6 is a diagram showing the position of components on the board. The pin-outs of the components used can be found in manufacturers' data or distributers' catalogues. There are two particularly important points:

- Take special care with all polarised components - diodes, transistors and electrolytic capacitors - damage can be caused by connecting them into the circuit incorrectly.
- Your receiver circuit plugs into the pre-built decoder using three pins so it is vital that these pins are soldered to your board in exactly the right place and point in the right direction. They should be soldered in place before any other components are on the board. To help you achieve correct pin alignment a few jigs have been made up to keep the pins in the right position while you solder them to you board. PLEASE DO NOT USE BUILT UP DECODER UNITS TO FULFILL THIS FUNCTION because heat flow along the pins might unsolder the insides of the decoder unit!

On successful completion of the construction it is necessary to perform tests on your circuit to be sure that it behaves as expected. These tests fall into two broad categories, system tests and circuit tests.

6.2 System Tests

The system tests aim to evaluate the effectiveness of your circuit as a receiver and demodulator when used in conjunction with a transmitter and decoder - does it enable the reception of signals? - over what range is it capable of successful reception? - how immune is your receiver to signals transmitted at frequency bands adjacent to yours? You might think of other tests you could perform. When you do the system tests remember to select transmitter and decoder units with matched codes as described in section 5.1.4 above and remember to set the frequency to your allotted value - a frequency monitor facility is available on the transmitter.

6.3 Circuit Tests

The circuit tests aim to verify that the circuit is performing as it was designed to do. You can measure the gain of the first stage [$20\log(V_{TP2}/V_{TP1})$] by injecting a small sinusoidal signal into TP1 and measuring the input at TP1 and the output at TP2 as a function of frequency. You can similarly measure the gain as a function of frequency for the second stage [$20\log(V_{TP3}/V_{TP2})$] by injecting a signal at TP2 and measuring the output at TP3. These tests should be done using a sinusoidal generator, not a transmitter or decoder unit. The following hints might help you with your measurements and their interpretation:

- Use 10:1 attenuating oscilloscope probes to measure the output signals.

- Use 1:1 oscilloscope probes to measure the input signals.
- You may find it easier to measure the input signal if you divide the oscillator output voltage by some factor, say 11, using a resistive potential divider – say 100Ω and 10Ω – across its output and applying the divider output to the circuit and measuring the oscillator output. This allows you to put a very small signal into the amplifier but leaves you with a larger version of that signal to monitor. Calculating the real input signal amplitude from the measured oscillator output is straightforward.
- Measure over the same range of frequencies as you used in your estimate of gain based on equations 4.1 and 4.2. Plot your measurements on the same axes as your theoretical responses so that you (and your readers) can compare them easily.
- Check that the resonant frequency, *q* factor and gain of each stage are consistent with what you expect from your preparatory design calculations and comment on the results. Can you explain any discrepancies?

7: Assessment

THE PROJECT REPORT SUBMISSION DEADLINE IS FRIDAY 3rd May 2013

The project will be assessed in two ways.

- Your tutor will meet you in the laboratory on an agreed mutually convenient date in the week beginning 29th April. Your tutor will want to inspect your constructional work, watch you demonstrate your system in operation and ask you some questions about it. Your tutor may ask you to carry out specific measurements to illustrate the circuit operation. This session will normally last about 30 minutes and the mark will contribute 4% towards your coursework module.
- A formal report on the project. Whilst you are collecting and recording data about your circuit, bear in mind the requirement to write this report. The report should include the following:

  (i) ***Introduction.*** Here you should give the reader scene setting, contextual information by explaining in your own words what the project is about and the general organisation of the system. You should say here why each competing group must use a different frequency in the FYGER arena.

  (ii) ***Theory.*** Here you should detail the calculations leading to the choice of components you were asked to make in sections 4.3 and 4.4 together with the predicted responses you generated from equations (4.1) and (4.2).

  (iii) ***Results.*** This section should contain a brief procedural description of how you made the various measurements outlined in sections 6.2 and 6.3 that you made on the completed circuit and system, followed by a statement of the observations made and appropriate comments on the observations. In the case of response measurements, results should be presented in graphical form. Where a measured response is to be compared with a predicted one, both the measured and predicted responses should be drawn on the same set of axes so that comparison is facilitated. In all cases the results should be discussed in the context of the expectations calculated at the outset.

  (iv) ***Conclusions.*** Here you should draw together the main findings of your project work and offer some assessment of likely fitness for purpose of this system, pointing out its strengths and weaknesses. Remember that conclusions should be a concise statement of outcomes. For a report of this length, if you find yourself writing more than 200 words you are probably including inappropriate text.

(v) ***References.*** You should list here the sources you have used to help you in your execution of the project and the preparation of your report. The references should be appropriately referred to in the body of your report by their number in this list. Advice on the use of references is available on the Department's web pages under Undergraduate Teaching Resources.

The project report contributes up to 10% of your coursework mark and the approximate weightings of the various parts are as follows: **(i)** 1, **(ii)** 2, **(iii)** 3, **(iv)** 1, **(v)** 1. In addition, 2 marks are allocated to overall presentation and style; use of English, use and quality of diagrams and report formatting. Assume when writing this report that your marker is someone with a knowledge of electronics equivalent to a conscientious first year EEE student at Sheffield but with no knowledge about the project, why it is being run, what its aims are, or how it works.

A report of around 1200 to 1500 words should be sufficient to get full marks. If you find that you need fewer words than this to say what you want to say, that's fine. If on the other hand you use significantly more than 1500 words – say more in the 2000 to 2500 word region - there is a real possibility that you are writing things that do not need to be written (remember your target readership specification); unnecessary text is bad style and will be penalised! You can use as many diagrams as are necessary to aid your explanations. Always try and draw your own diagrams – it is the safest way of ensuring that the diagrams transmit the ideas you want them to.

- When your report is complete you should attach a barcode coversheet and post it in the black box outside E133. You must also send an electronic copy of the text to the plagiarism detection software service. Details of how to do this can be found on the web as follows; starting from the EEE home page (www.shef.ac.uk/eee/), select "information for staff / students" and then "EEE Teaching Resources". The first item on the list is the "JISC Plagiarism Detection Service - Student User Guide" which tells you what to do and the second item is "Departmental Policy on Referencing" which tells you the proper way to acknowledge your information sources. Take care to reference your sources properly and avoid quoting tracts of text from your sources – direct quotes are rarely appropriate in technical written English unless you are commenting critically on a particular form of words used by another author. THIS DOCUMENT IS ONE OF YOUR SOURCES!

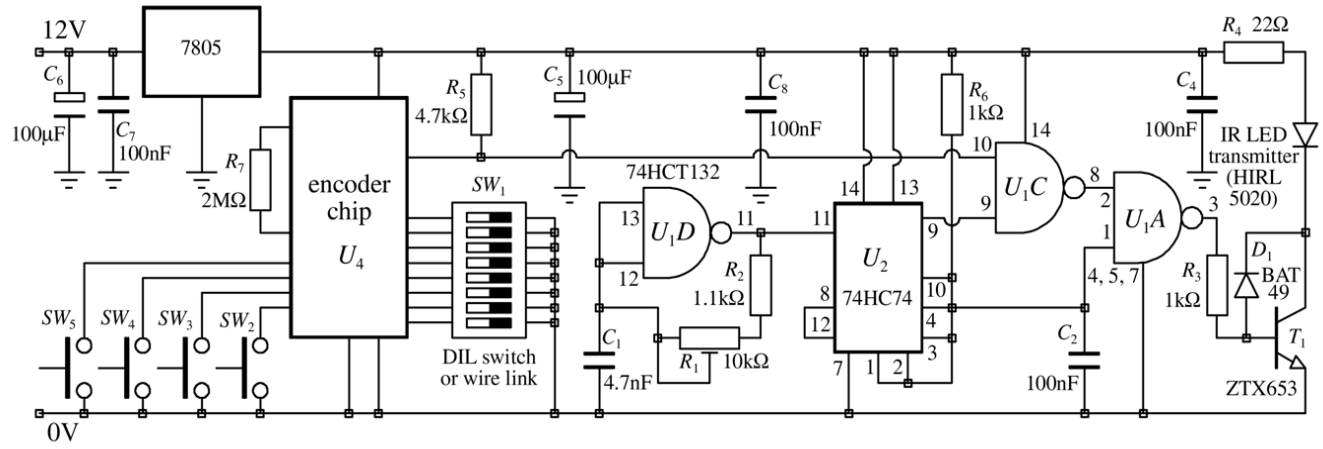
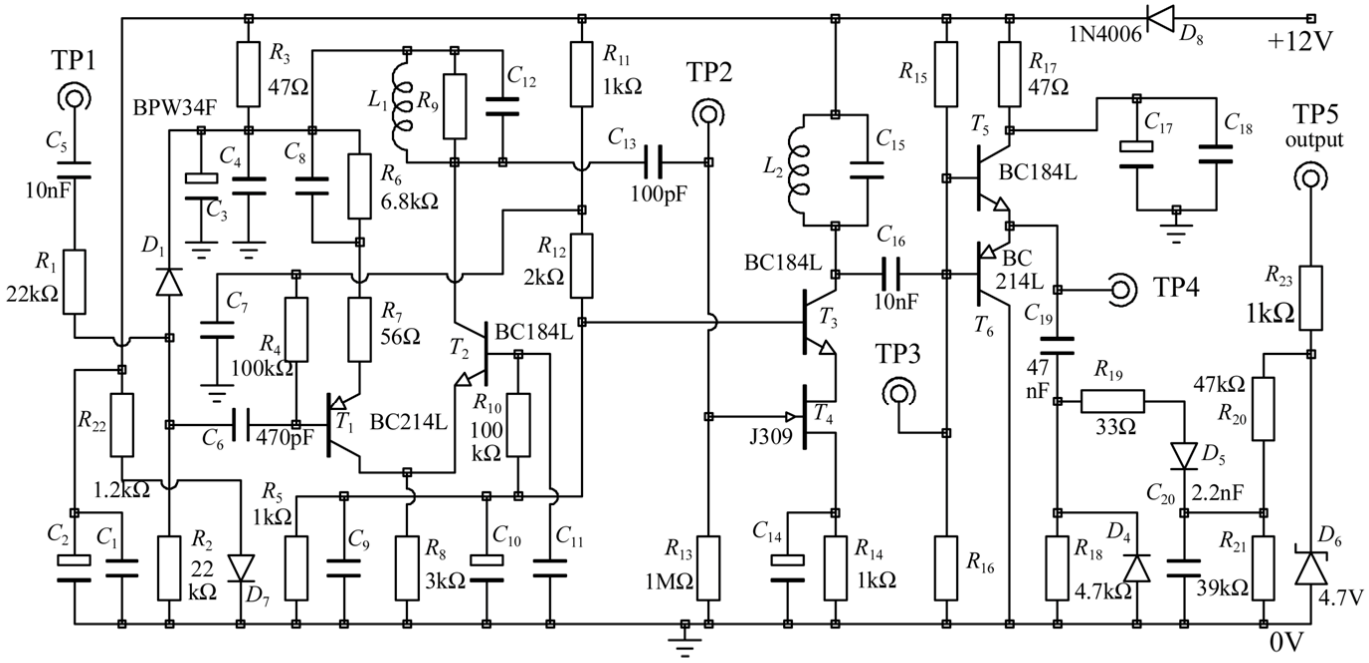


Figure 1 Encoder, Modulator and Transmitter Circuit



C_2 is 100µF 25V; C_3, C_{10}, C_{14} and C_{17} are 10µF 25V; C_1, C_4, C_7, C_8, C_9, C_{11} and C_{18} are 100nF ceramic; D_4 and D_5 are 1N4148 p-n junction diodes; D_7 is an LED.

Figure 2 The Receiver and Demodulator Circuit

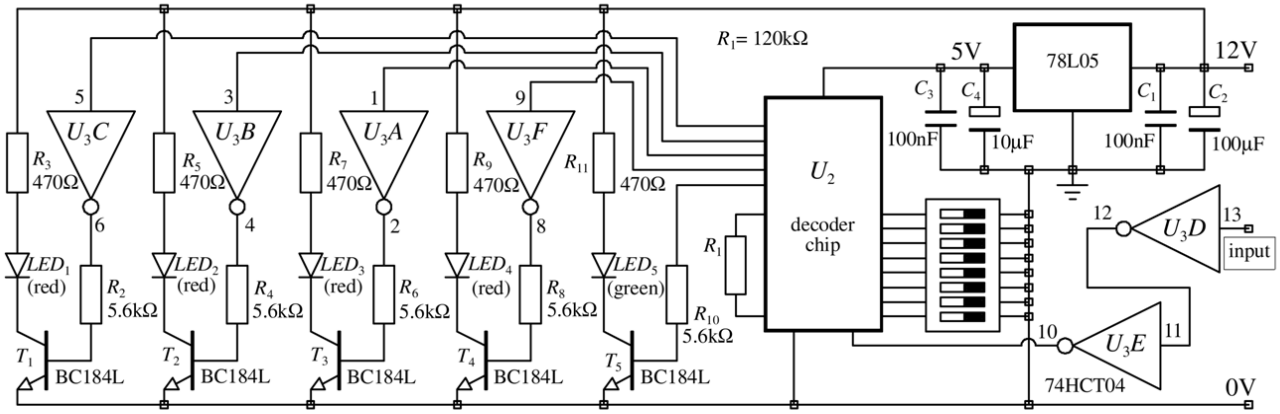


Figure 3 The Decoder Circuit

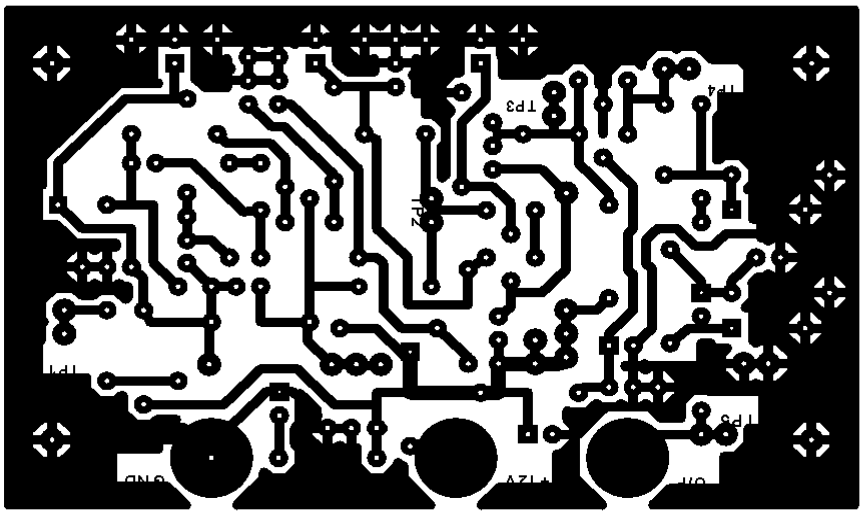


Figure 4

Track Side Receiver Layout (viewed from component side)

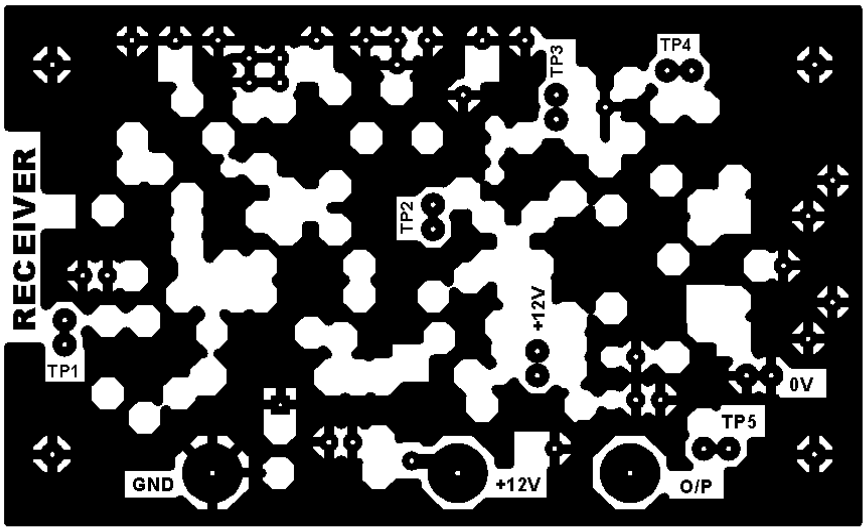


Figure 5

Component Side Receiver Layout

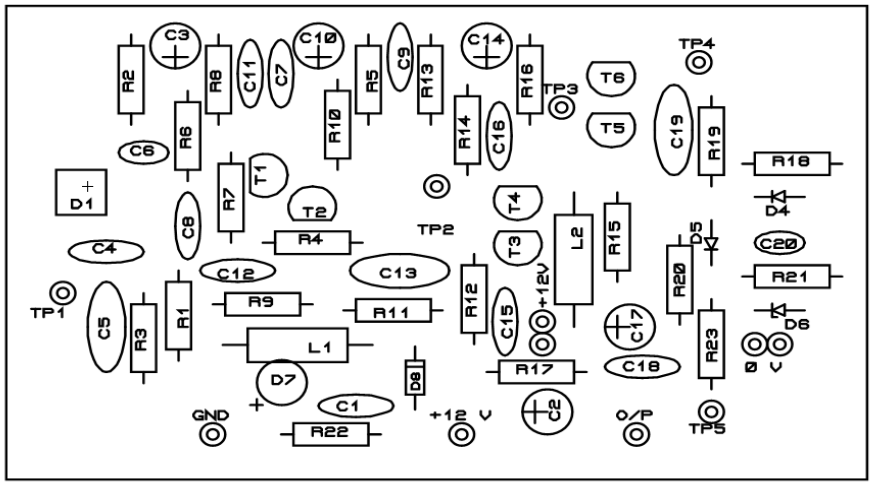


Figure 6

Receiver Component Layout

Components List

Receiver Components

R_1, R_2	22kΩ
R_3, R_{17}	47Ω
R_4, R_{10}	100kΩ
R_5, R_{11}, R_{14}, R_{23}	1kΩ
R_6	6.8kΩ
R_7	56Ω
R_8	3kΩ
R_9	????
R_{12}	2kΩ
R_{13}	1MΩ
R_{15}, R_{16}	????
R_{18}	4.7kΩ
R_{19}	33Ω
R_{20}	47kΩ
R_{21}	39kΩ
R_{22}	1.2kΩ
C_1, C_4, C_7, C_8, C_9, C_{11}, C_{18}	100nF ceramic
C_2	100µF electrolytic
C_3, C_{10}, C_{14}, C_{17}	10µF electrolytic
C_5	10nF polyester
C_6	470pF ceramic
C_{12}, C_{15}	????
C_{13}	100pF
C_{16}	10nF ceramic
C_{19}	47nF polyester
C_{20}	2.2nF polyester
D_1	BPW34F
D_4, D_5	1N4148
D_6	4.7V zener
D_7	LED
D_8	1N4006
L_1, L_2	????
T_2, T_3, T_5	BC184L
T_4	J309
T_1, T_6	BC214L

RCT February 2010