Examination Feedback for EEE6393 – Microsystem Packaging
Spring Semester 2012-13

Feedback for EEE6393 Session: 2012-2013

General Comments:

The exam scripts were, in general, very good. Q2 was the least popular and also yielded the lowest average mark.

Question 1

a) Bathtub curve, identifying and defining regions. Question answered well, majority of students correctly reproduced figure and identified regions: infant mortality, intrinsic and wear out. Few students identified the over-stressing of components as the main cause of steady state failures.

b) Burn in. Question answered well, majority of students correctly stated the purpose of burn in to reduce infant mortality and methods used to accelerate lifetime (voltage, temperature, current, humidity). Some candidates incorrectly answered that the devices are tested at extremes, i.e. maximum operating temperatures and not elevated temperatures, typically 90^{o}C for a 150^{o}C part.

c) Calculating yield via Poisson distribution. Generally answered well, candidates correctly implemented the given equation to obtain the correct results. Some confusion regarding the factorial mathematical function.

d) Calculating redundancy via Poisson distribution. Question extended the previous equation to calculate redundant units to increase redundancy above a set limit. Some confusion here; a number of candidates misunderstood the question and calculated how many wafers were required whereas others used the wafer area and calculated yield per unit area.

e) HTRB; calculating ambient temperature for a 1000hr lifetime test from thermal activation energy. Majority of candidates answered question well, reproducing Arrhenius equation, combining for two temperatures and re-arranging to calculate anneal time. Majority of mistakes made manipulating equations or using the incorrect parameters.

Question 2

a) COB versus SMT. Generally answered well, though some students confused COB (chip on board) with SOC (system on chip) – they are very different! Few students identified difficulty of rework as a disadvantage of COB.

b) Rent's rule plus track layout calculation. Most students correctly used Rent's rule to determine number of I/Os (400). From there, a number of assumptions needed to be made (track = gap, total routing length = 8 x pitch x (n-1) where n = 20), eventually leading to an answer of: track pitch = 152 µm. Many students confused the track pitch with the BGA pitch and thus derived a very wrong answer.

c) BGA materials. This question required the student to explain the sequence of materials

that constitute under-bump metallization (UBM) and also the actual solder ball and compliant underfill. It was book work, but generally not answered well.

d) Eutectic versus non-eutectic SAC solder alloys. Generally answered well, though some confusion over which solder has the lower melting point (it's the eutectic).

Question 3

a) Convective heat transfer from isothermal PCB. Many students failed to take note of the fact that the PCB was isothermal. Another common mistake was to place the 2 thermal resistances in series, whereas they were in fact in parallel.

b) Improved thermal performance for a). Add fan/heatsink. Orientate PCB vertically (not many students suggested this).

c) 2-layer PCB fabrication. Bookwork. Many students failed to mention photolithography. Waste copper could be minimized by using a build-up process, where etching is performed on thin copper layer and then tracks are made thicker by electroplating.

d) Microstrip dimensions. Oh dear, not done well at all. Many folk assumed impedance of IC tracks was 50 Ω, whereas in fact it should be calculated from: $Z = (L/C)^{½} = 80\ \Omega$. Making sensible assumptions for track thickness (1 oz/foot^2 copper = 35 µm) and track width (50-1000 µm) enables *h* to be found.

QFP package preferred because DIP package will have longer connections and, more importantly, different length connections to the pins. This will result in unequal signal propagation delays.

e) Decoupling capacitors. Used to provide instant power to IC.

Question 4

a) Comparison between 'efficiency' of IC packaging technologies. Bookwork, done well.

b) Through silicon vias (TSV) for a CMOS image sensor. Students struggled with this question. Few could explain the TSV fabrication method and even fewer explained why they helped with improving light gathering capability – namely that by using TSVs the 4 routing layers could be on the opposite side of the silicon from the photodiodes.

c) Silicon versus glass interposers. Glass cheaper than silicon, but may have different thermal expansion coefficient, hence thermal stress. Holes in glass need to be made by laser/shot blasting – Bosch process not possible.

d) Cooling of power transistor via conductive heat transfer to heat sink. Done well, though some students tried to include heat transfer through gold bond wires, which is negligible. Some answers were poor due to wildly incorrect estimates of layer thicknesses or mistaking aluminium for alumina or missing a layer.

e) Effect of diamond substrate on thermal performance of d). Some students made this far more complicated than necessary. All that needed to be done was to calculate the total thermal resistance using: $R_{total} = R_{jc} + R_{ca} = 0.1 + 1 = 1.1$ °C/W; hence: $T_{junction} = 1.1 \times 200 + 20 =$ <u>240 °C</u> – far too hot for silicon.