EEE 331 – Tutorial Sheet 1

Bookwork questions

These would normally form 40% of an examination paper.

1) a) Sketch the Hybrid-π s.s. model for a BJT.
b) Define the physical origins of each of the elements in the circuit.
c) Which elements can be ignored when the load impedance is small? (and for a bonus hard question, why?)

2) Sketch the s.s. model for a MOSFET

3) State the relationships between;
a) collector current and base-emitter voltage for a BJT
b) drain current and gate-source voltage for a MOSFET

4) Calculate the values of Z1 and Z2 in figure 2, given that the circuit in figure 2 is equivalent to that shown in figure 1. Show all of your analysis.

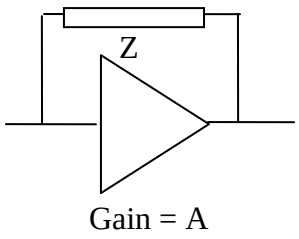

Figure 1

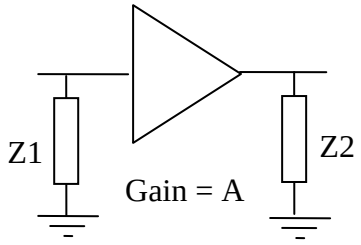

Figure 2

5) State the voltage gain in terms of BJT s.s. parameters and circuit elements for the following circuits.
a) Common-emitter
b) Common-base
c) Common-collector

6) What effect does emitter degeneration have on the output impedance of a common-emitter circuit?

7) Give one common application of a common-collector circuit, explaining why this circuit is particularly attractive for this application.

Application questions

These questions would normally form 30% of an exam paper.

8) The BJT in the high-power, single-ended output stage below obeys the relationship $I_C = 4\times10^{-31}\exp(100\times V_{be})$. Calculate the gain for the circuit, assuming that a quiescent current of 1A flows through the resistor R_e and that $i_b << i_1$.

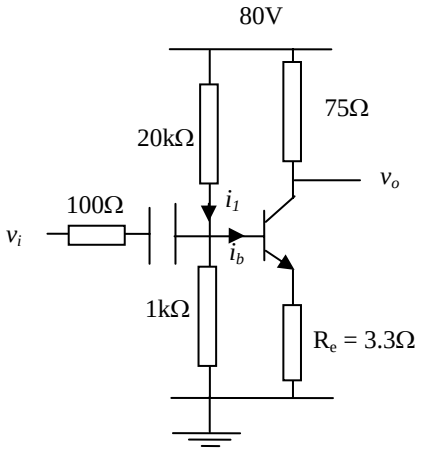

Figure 3

For a bonus difficult question, why is a two stage topology with a voltage gain stage and a push-pull output stage preferable to the circuit given above?

9) Calculate the mid-frequency gain of the circuit below. You should assume that the capacitors C1 and C2 are short circuits at the frequencies of interest that the internal capacitances of the BJT are open circuits and that r_{bb}, r_{ce}, and r_{cb} can be neglected. Also calculate the output impedance of the circuit from the small signal's point of view in the mid-frequency range.

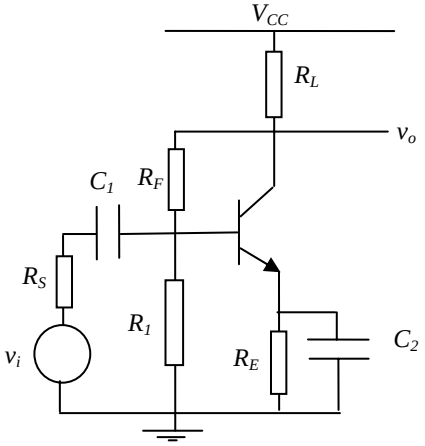

Figure 4

10) The circuit shown below in figure 5a has a voltage gain of 100. The circuit comprises a BJT with C_{CB} = 10pF which has $V_{be\ on}$ = 0.7V and $V_{ce\ on}$ = 1V. The waveform generator is programmed to give an output of the type shown in figure 5b. Plot a graph of the rate of change of v_o as a function of t. How could one increase the slew rate of the following?

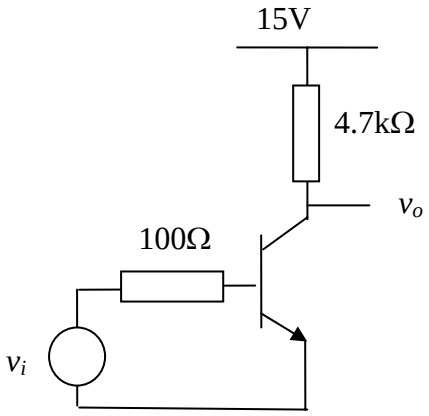

Figure 5a

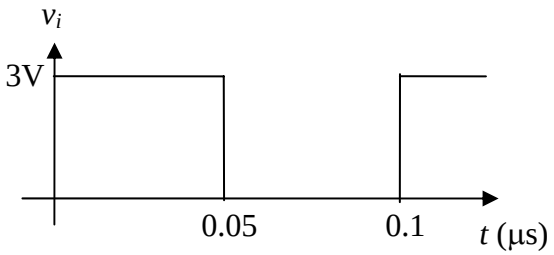

Figure 5b

Difficult questions

Usually constitute roughly 30% of the paper.

11) Explain why MOSFETs are rarely used as transistors in voltage gain stages if BJTs are available.

12) Explain (i.e. do not use equations) why including emitter degenerating resistors reduces the gain of a common-emitter amplifier.

    Emitter degeneration is used commonly to better define the bias for a BJT. Sketch a circuit diagram showing how a common-emitter gain stage with emitter degeneration can be modified so that a s.s. does not incur this gain penalty.

13) Explain the difference between the Miller effect and slew rate limiting.

14) Why are additional capacitors sometimes included between base and collector in voltage gain sections of power amplifiers?