The University Of Sheffield.

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DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (2.0 hours)

EEE6214 Packaging and Reliability of Microsystems

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. One of the first stages in the packaging of an integrated circuit (IC) is the separation ('singulation') of individual ICs from the completely processed semiconductor wafer.

Describe the standard method that is used to perform this operation.

What are the limitations of this method? (4)

b. What new techniques are starting to be used for die singulation and what improvements do they offer? (2)

c. Some electrical testing normally precedes singulation? Why and how is it done? (2)

d. A microprocessor is packaged in a ball grid array (BGA) package with 900 pads arranged in square array at a pitch of 1 mm.

Suggest the specification (e.g. line width, vias, number of layers, etc.) for a printed circuit board that would enable signals to be routed to all balls on the package. (5)

e. The semiconductor industry is finding it increasingly difficult to maintain Moore's Law. One possible 'fix' is to stack multiple ICs vertically within the same package – a '3d MCM'.

i) Explain why temperature control is so challenging in 3d MCMs and suggest a plausible innovative solution for removing the heat. (4)

ii) What advantages do 3d MCMs have over system in package (SIP) and system on chip (SOC) solutions? (3)

2. a. Describe the wave soldering process for the assembly of a simple electronic system. (4)

b. Wave soldering has largely been replaced by reflow soldering for the assembly of compact electronic systems (e.g. mobile phone). However, even for these compact systems there are some components that may still be connected to the

printed circuit board (PCB) by wave soldering. Which components are still connected in this way and why? (2)

c. Solder balls in a ball grid array are used to connect a silicon chip to an epoxy/glass substrate. Describe with the aid of a sketch what happens to the shape of a single ball near the edge of the assembly when it cools from the bonding temperature to room temperature.

What implications does this shape change have for the lifetime of the assembly and what could be done to mitigate it? (4)

d. A dual inline package (DIP) is soldered to a printed circuit board (PCB) which is in turn mounted on a large metal chassis. The DIP has 20 tinned copper leads which make direct thermal contact between the active silicon and the PCB. Each lead is 5 mm long and has a cross-sectional area of 0.5 mm^2. The PCB has a thermal resistance to the chassis of 10 °C/W.

i) What is the maximum power that a *safety-critical silicon* IC inside this DIP package can dissipate? State any assumptions that you make. (2)

ii) Can the same DIP package be used to house a *consumer grade silicon* IC that dissipate 12 W? Explain your answer. (2)

Note: thermal conductivity copper k_{Cu} = 390 W /m °C

e. The DIP package in **d.** is modified so that it can accommodate a *silicon carbide* IC and carry a heat sink and cooling fan. It remains connected to the same PCB using the same leads. Part of the DIP modification involved thinning the top insulation layer. This results in a much-reduced thermal resistance between the silicon and the top of the package of 5 °C/W.

i) Draw a sketch of the thermal resistor network that describes this compete scenario. (2)

ii) What is the maximum thermal resistance of a heat sink/fan combination that would enable a 35 W *silicon carbide* IC to be housed in the same DIP package? (3)

iii) What would be the effect on performance if the same system were operated at high altitude? (1)

3 **a.** High-energy particles, such as alpha particles, x-rays and gamma-rays, can cause radiation damage in electronic and optoelectronic components. Explain how such damage may occur and what affects might be observed in the following:

i) Si MOSFET (2)

ii) Optical fibre (2)

iii) Photodiode (2)

b. Electro-migration describes the migration of metal atoms in a conductor through which large currents flow. Sketch and briefly describe what happens at the following locations in a conductor track:

i) Bond between Au and Al (2)

ii) Step over an oxide aperture (2)

c. Black's equation describes the relationship between mean time to failure (MTTF) of a semiconductor and both current density and temperature.

i) Write down Black's equation and define each term in the equation. (2)

ii) Draw a schematic plot of the MTTF as a function of current density, labelling important features of the plot. (2)

iii) Under what conditions does the current density exponent, $n = 2$? (1)

iv) An experiment was conducted to determine the MTTF of Al conductor tracks at a temperature of 30 °C and an operating current density of 2×10^5 A cm^{-2}. The temperature was raised to 100 °C and the operating current density increased to 4×10^5 A cm^{-2}. A MTTF of 2000 hours was estimated, with an activation energy, E_a = 0.5 eV. Calculate the acceleration factor provided by this thermal and electrical overstressing and use your answer to predict the number of years you expect the conductor tracks to last. State any assumptions made and use Black's constant, $B = 1$ and $k = 8.617\times10^{-5}$eV K^{-1}. (5)

4. **a.** Describe the most appropriate characterisation method for investigation of the following degradation processes of components in plastic encapsulated packages. Your answer should justify use of your chosen method in contrast to possible alternative methods. When making your choice you should consider the amount of sample preparation that is required.

i) Gold wire displacement in package (3)

ii) Intermetallic formation under ball bonds (3)

iii) Popcorn cracking (3)

b. A laser diode packaged in a hermetically sealed butterfly package has failed. Starting with simple optical inspection, sketch a possible process flow for detection and characterisation of the unknown defect responsible for the failure. (3)

c. The careful analysis of a printed circuit board (PCB) fabrication line has revealed the following statistics:

- 2% of the as-received copper foils are defective
- 1% of the as-received glass/epoxy prepreg layers are defective
- the lamination process has a yield of 85%

If a panel consists of 2 layers of copper plus 8 layers of prepreg, what is the yield of defect-free panels? (3)

d. The dust in the lithography room leads to a further reduction in yield. The dust has been measured to generate an average defect density D_0 = 0.1 mm^{-2}. If the copper tracks on the PCBs have a minimum pitch of 1 mm, what percentage of the panels will be experience a defect-free lithographic process? You may assume that the functional yield (*FY*) can be modelled by the Murphy model:

$$FY = \frac{1 - e^{-2A_c D_0}}{2A_c D_0}$$

where A_c = critical area on the PCB (mm^2). (5)

GLW / KG