The University Of Sheffield.

Data Provided: None

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

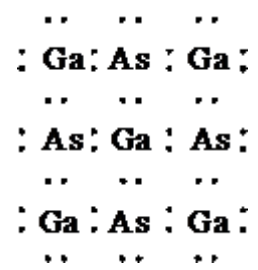
Spring Semester 2014-15 (2 hours)

Principles of Semiconductor Device Technology

Answer **THREE** questions. **No marks will be awarded for a solution to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The number given after each section of a question indicates the relative weighting of that section.**

TURN OVER

1. a. Consider the two-dimensional representation of the semiconductor GaAs shown below:



If Si atoms are inserted as dopants and exclusively replace Ga atoms in the lattice, will the Si-doped GaAs material be n-type or p-type? What if the Si atoms exclusively replace As atoms? Explain.

What is an anti-site defect? Give an example. Name two diffusion mechanisms mediated by point defects.

(5)

b. With the aid of simple diagrams, state the close packed plane stacking sequences corresponding to intrinsic and extrinsic stacking faults in the diamond cubic lattice. By means of a diagram show how the Burgers vector of the intrinsic fault may be calculated.

(5)

c. Explain using a diagram how the Miller index of a lattice plane in crystalline silicon is defined.

Deduce which of the following planes in a cubic crystal are perpendicular to one another.

(121) and $(1\bar{1}\,1)$

$(\bar{1}10)$ and $(1\bar{1}3)$ and

$(\bar{1}00)$ and $(0\bar{1}3)$

d. Given that the lattice constant of Si is 5.43Å, calculate the areal density of atoms (number of atoms/cm^2) on each of the following planes: (100), (110), and (111). Given that the direction that has the most number of covalent bonds is the best for hole conduction, which plane would you expect to be best for p-channel MOSFET performance?

(5)

(5)

2. **a.** A (non-compensated) p-type silicon sample is maintained at room temperature. When an electric field with a strength of 1000 V/cm is applied to the sample, the hole drift velocity is 3.5×10^5 cm/sec.

i) What is effective mobility μ_p of a hole in this sample?

ii) What is the average scattering time τ between events given the hole conductivity effective mass m_p^* is $0.39m_0$ where m_0 = 9.11 x 10^{-31} kg $\mu_p = q\tau / m_p^*$, q=1.6x10^{-19} C. (Note: 1 kg cm^2/V s/C = 10^{-4} sec) **(6)**

b Name 2 key generic differences between the techniques: (i) Molecular Beam Epitaxy (MBE) and (ii) Metal Organic Chemical Vapour Deposition (MOCVD) employed for the growth of III-V compound semiconductors. **(3)**

c Explain with the aid of a diagram how metal tracks can be formed using the lift-off process. **(6)**

d Sketch the energy-band diagrams of an ideal silicon MOS capacitor with p-type doping for the following bias conditions:

i) accumulation
ii) depletion
iii) flatband
iv) strong inversion

(5)

In each diagram please indicate the Fermi level and the intrinsic level in the semiconductor. How is the threshold voltage defined with respect to these levels and band bending ?

3 **a** State any 2 of 3 key attributes of ion implantation that make it the key process for introducing dopants into ICs. In an ion implanter comment on the following a) method of production of dopant b). Role of the bending magnet c) calibration of dose.
What is meant by "range" and "projected range".
Outline the phenomenon of ion channelling: Name two methods to prevent channeling. **(5)**

b. Si+ ion implantation into an (001) Si wafer produces an amorphous layer 1.5 x 10^{-5} cm in thickness. Calculate how long the epitaxial regrowth of this layer will take at 600°C. (The activation energy for the regrowth process is 2.76eV, the pre-exponential factor (v0) is 3.68 x 10^8 cm/s and Boltzmann'sconstant (k) is 8.617 x 10^{-5} eV/K). **(5)**

c State what is meant by dry and wet oxidation. Explain with the help of diagram and necessary flux equations, the reaction kinetics of an oxidation process. How is it possible to modify the reaction rates of oxidation? **(6)**

d Explain what is meant by Liquid Encapsulation Czochralski technique (LEC). **(4)**

4. **a** Explain with the aid of a diagram of the energy band potential in the source and channel regions, the main reason for the subthreshold leakage of an MOS transistor. What is the maximum limit of the inverse subthreshold slope ? **(5)**

b Explain diagrammatically a CMOS process. Write a statement explaining what is meant by (i) LOCOS and why is it needed. (ii) Field threshold adjust implant and why it is needed. (iii) Self aligned process. **(10)**

c Explain using diagrams where necessary the working of a tunnel FET device. Indicate the tunnelling mechanism using band diagrams in the off and on-state. **(5)**