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EEE6212 Lecture 19
“p-n junctions and diodes”

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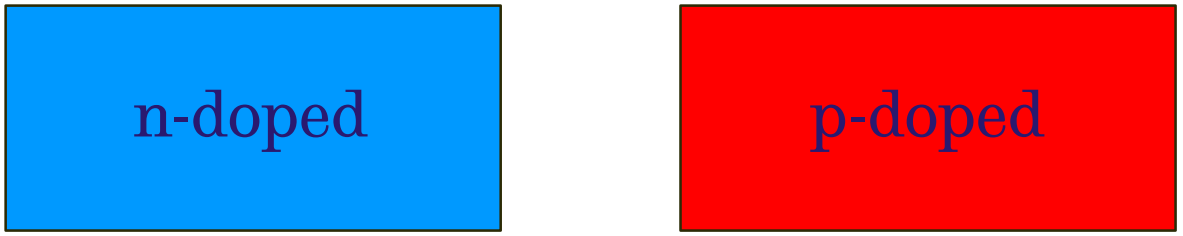
Outline

- Formation of a p-n junction
- Solution of Poisson's equation for a p-n junction
- Built in electric field and bias
- Electrical operation under forward/reverse bias
- Diode characteristics
- Types of diode: rectifiers, LEDs, Zener diodes, APDs
- Principle of bipolar junction transitors (BJTs)

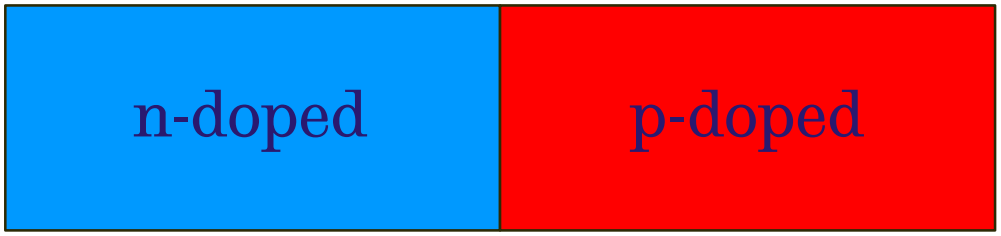
Formation of a p-n junction

Take two isolated blocks of n and p type semiconductor

Each block has a constant doping level throughout



Bring them together – there is now a non-uniform carrier concentration at the junction between the two…

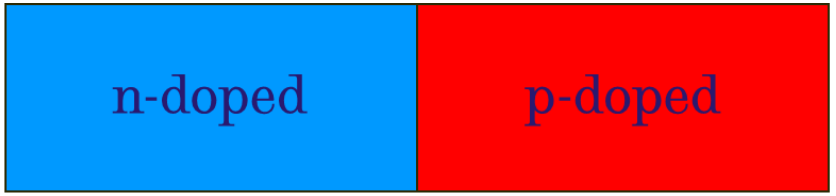


What happens?

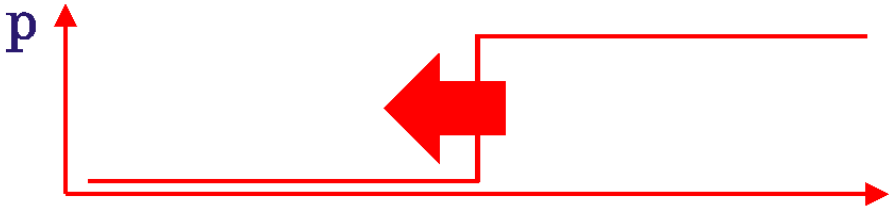
Carrier Diffusion

(t=0 at connection)

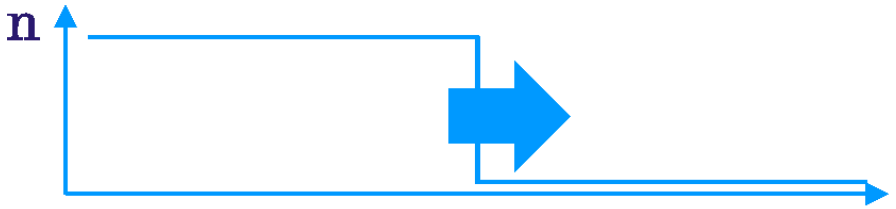
Holes diffuse from the p-type material into the n-type material where the are minority carriers and recombine with electrons



The holes leave behind ionised (-ve) acceptors in the p-region



Electrons from the n-type region diffuse in the opposite direction recombining with holes



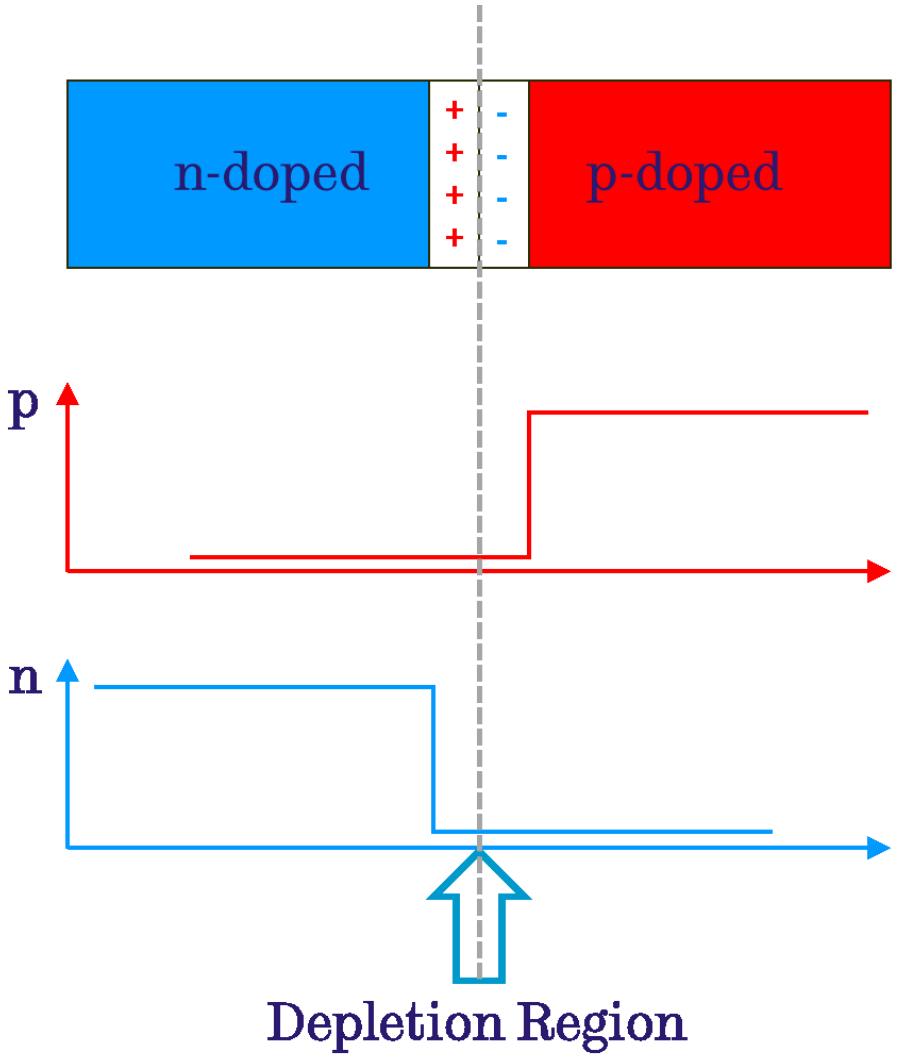
➔ Depletion of free carriers at the junction

Have electron diffusion current from left to right (conventional current flow from right to left)

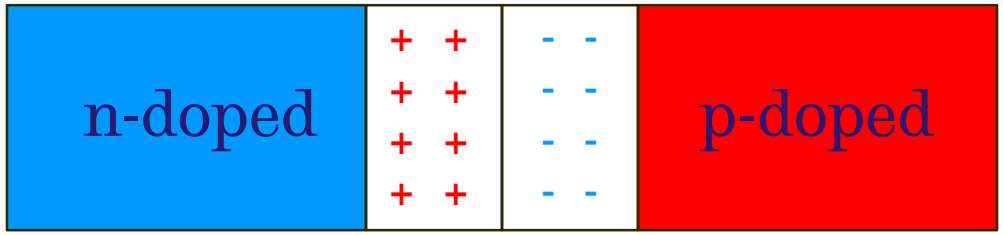
Have hole diffusion current from right to left (conventional current flow from right to left)

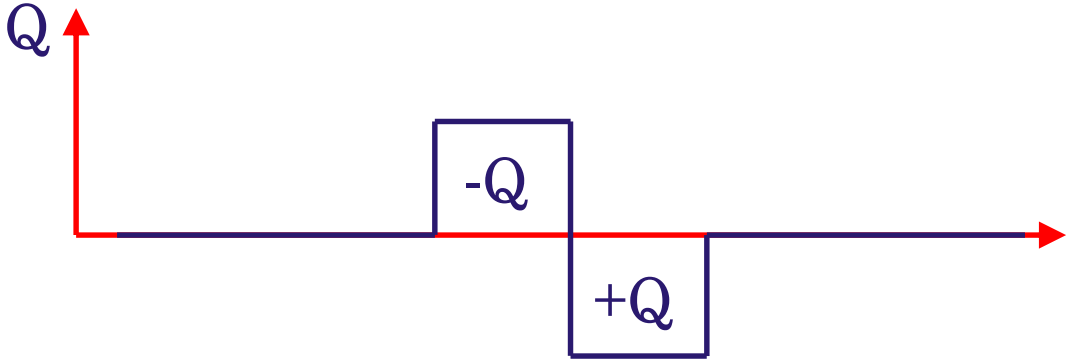
At equilibrium there must be no net current so an E-field is generated

Gives a potential difference V_0 between the n and p regions



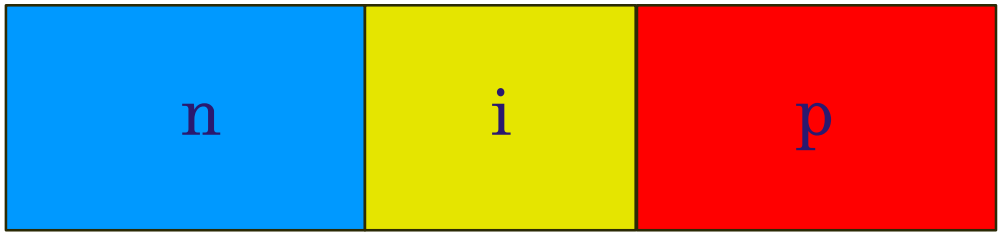
Ionised dopants create a local charge density (space charge)





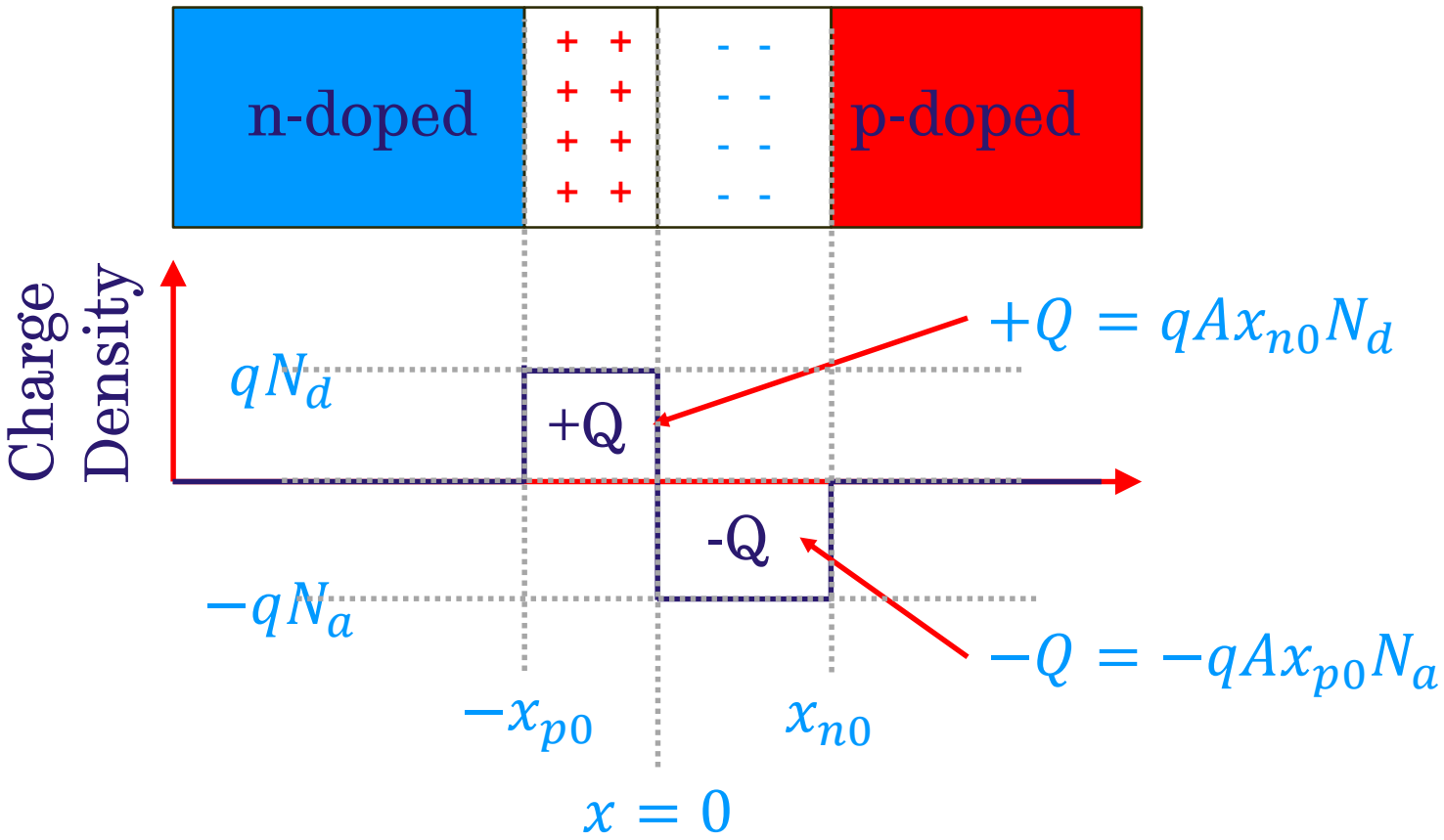
Within the depletion region there are no free carriers any more

Therefore the depletion region is intrinsic and does not conduct

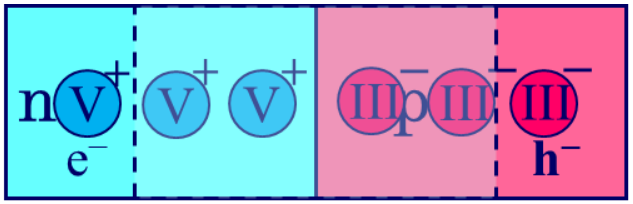


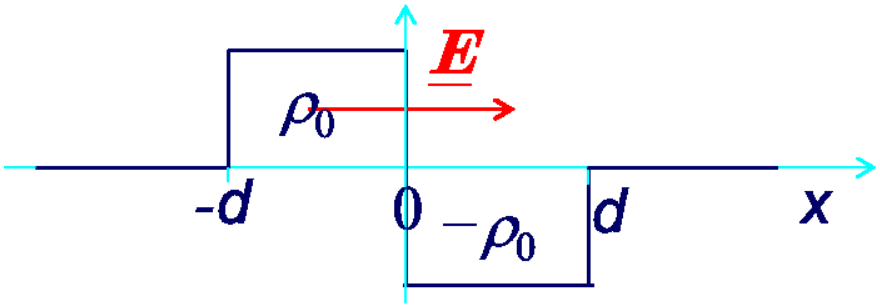
Space charge at a Junction

Assume a rod with cross sectional area A and doping densities of N_d and N_a for the donors and acceptors respectively. The depletion widths for the n and p type regions are x_{n0} and x_{p0}



Poisson equation for p-n junction





Consider step function of charge density

$$\rho = \begin{cases} +\rho_0, & -d < x < 0 \\ -\rho_0, & 0 < x < d \end{cases}$$

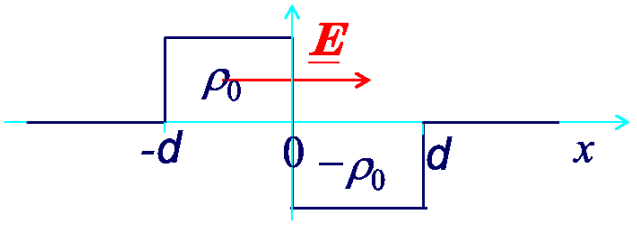
Solve Poisson Equation

$$\nabla^2 V = div\,(grad\,V) = -div\,E = -\frac{\rho}{\epsilon}$$

In 1D this becomes

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon}$$

Left hand side



Solving for the left hand side (n-type material)

$$\frac{d^2V}{dx^2} = -\rho/\epsilon$$

Double integration yields an equation with three constants

$$V(x) = c_1x^2 + c_2x + c_3$$

Then

$$-E(x) = \frac{dV}{dX} = 2c_1x + c_2$$

and

$$\frac{d^2V}{dx^2} = 2c_1 \Rightarrow c_1 = -\frac{\rho_0}{2\epsilon}$$

Boundary conditions

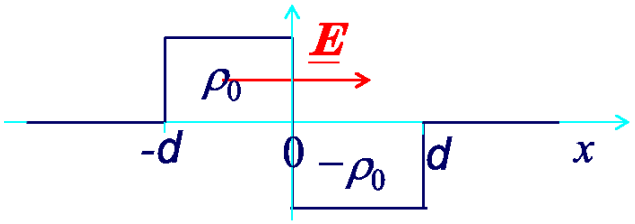
$$V(0) = 0 \Rightarrow c_3 = 0$$

$$E(-d) = 0 \Rightarrow -2c_1(-d) - c_2 = 0 \Rightarrow c_2 = -\frac{\rho_0 d}{\epsilon}$$

$$\Rightarrow V(x < 0) = -\frac{\rho_0}{2\epsilon}(x^2 + 2dx)$$

Right hand side

Solving for the right hand side (p-type material)



$$\frac{d^2V}{dx^2} = +\rho/\epsilon$$

Double integration yields an equation with three constants

$$V(x) = c_1x^2 + c_2x + c_3$$

Then

$$-E(x) = \frac{dV}{dX} = 2c_1x + c_2$$

and

$$\frac{d^2V}{dx^2} = 2c_1 \Rightarrow c_1 = +\frac{\rho_0}{2\epsilon}$$

Boundary conditions

$$V(0) = 0 \Rightarrow c_3 = 0$$

$$E(+d) = 0 \Rightarrow -2c_1(+d) - c_2 = 0 \Rightarrow c_2 = -\frac{\rho_0 d}{\epsilon}$$

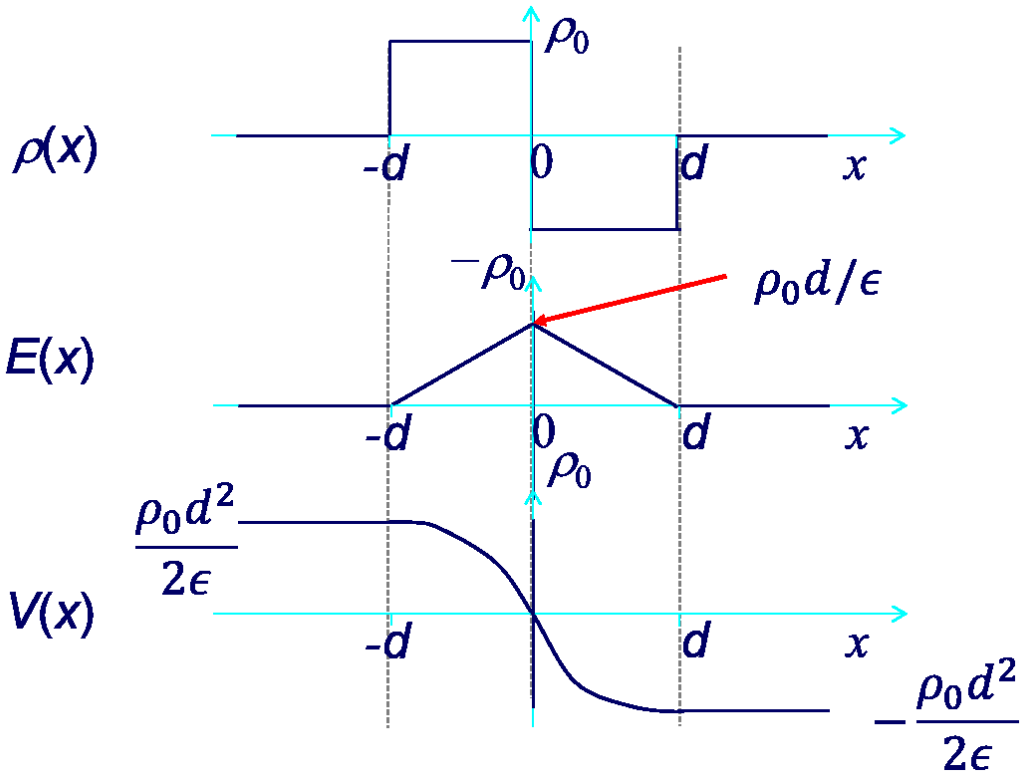
$$\Rightarrow V(x > 0) = +\frac{\rho_0}{2\epsilon}(x^2 - 2dx)$$

Combine solutions

$$V(x<0) = -\frac{\rho_0}{2\epsilon}(x^2 + 2dx), \qquad V(-d) = \frac{\rho_0 d^2}{2\epsilon}$$

$$V(x>0) = +\frac{\rho_0}{2\epsilon}(x^2 - 2dx), \qquad V(+d) = -\frac{\rho_0 d^2}{2\epsilon}$$

Plot functions vs x direction



Built-in potential and electric field

Some typical numbers

Silicon: $\epsilon_r = 11$, doping of 1ppm, 2/3rd of dopants activated, $d = 90nm$

$$\rho_0 = \frac{2}{3} \times 10^{-6} \times ne = \frac{2}{3} \times 10^{-6} \times \frac{8}{a^3} = 5335 \frac{C}{m^3}$$

$$\epsilon = \epsilon_0 \epsilon_r = 8.8542 \times 10^{-12} \frac{As}{Vm} \times 11$$

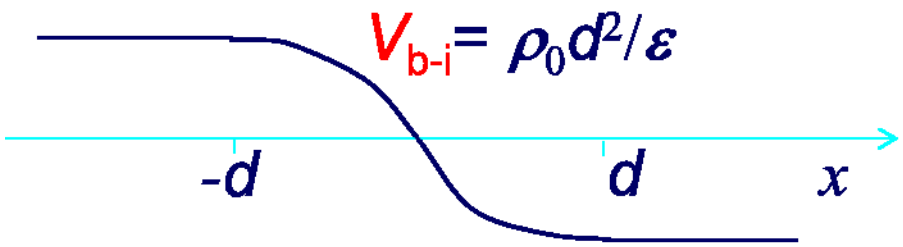
$$E_{max} = \frac{\rho_0 d}{\epsilon} = 5.5 \times 10^6 \, V/m$$ ⟸ This is quite large

$$V_{b-i} = V(-d) - V(d) = \frac{\rho_0 d^2}{\epsilon} = 0.55V$$

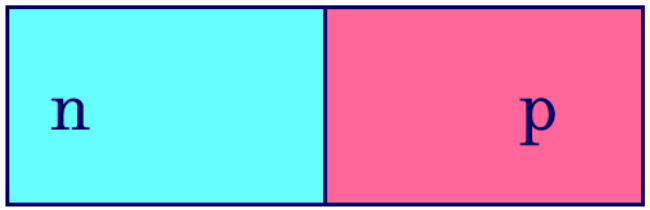
This is the built in potential across the p-n junction

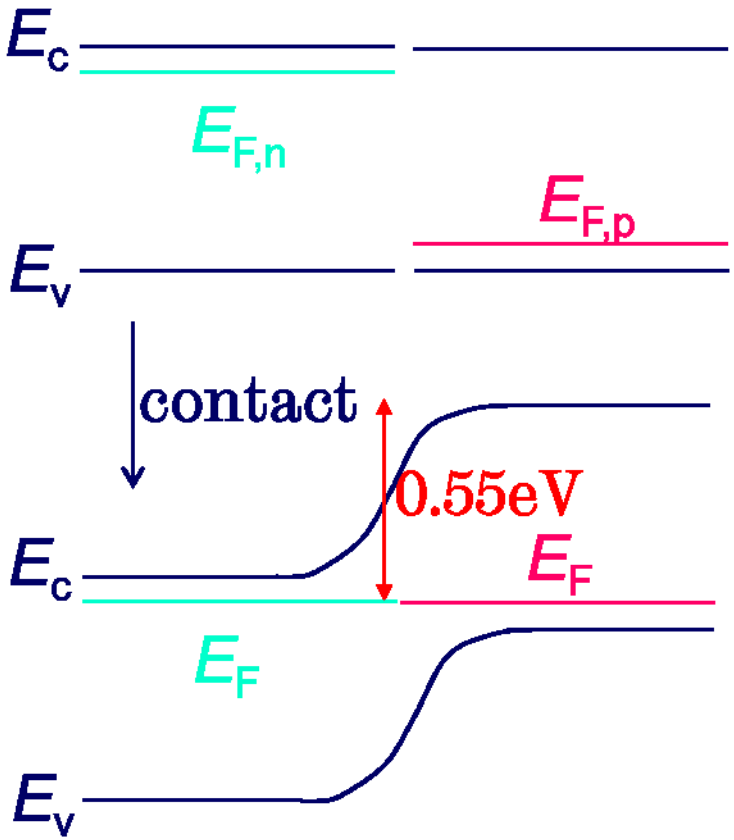
For the diode to conduct the applied voltage (bias) needs to at least compensate this built in potential

Built-in potential and Fermi Level



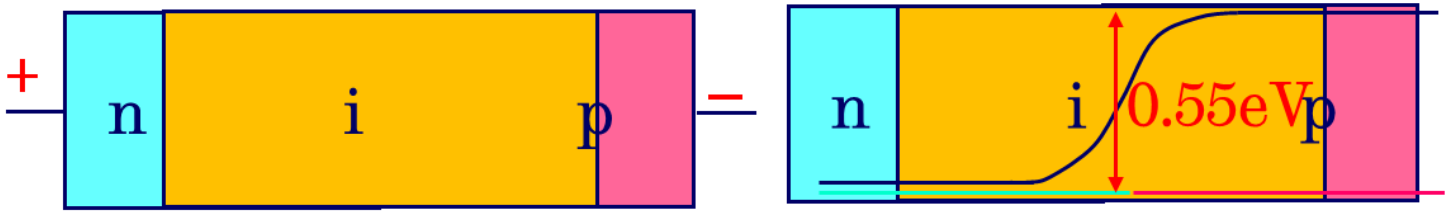
pot. energy of electrons: $-eV_{b\text{-}i}$





Qualitative Diode Behaviour

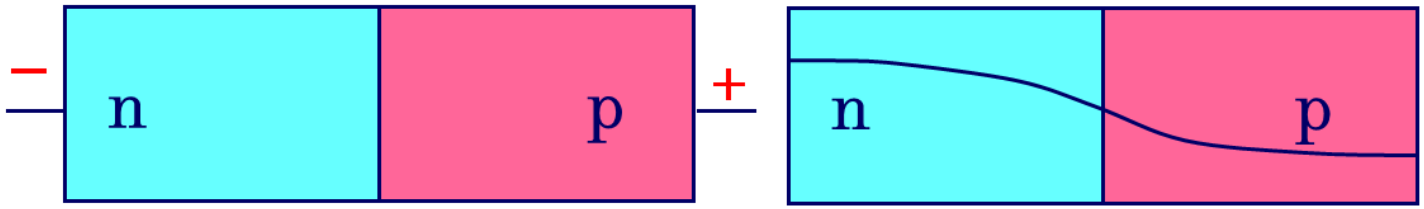
reverse bias: diode blocks



depletion region expands

$V_{bias} < V_{b\text{-}I}$ or even enhances $V_{b\text{-}i}$

forward bias: diode conducts



depletion region shrinks and finally vanishes

$V_{bias} > V_{b\text{-}I}$ counter-acts $V_{b\text{-}i}$

Quantitative Diode Behaviour

thermodynamic calculation of built-in potential: consider current densities due to both drift and diffusion on both sides:

$$J_n^{total}(x) = J_n^{drift} + J_n^{diffusion} = q\mu_e E_x n + qD_n \frac{dn}{dx}$$

$$J_p^{total}(x) = J_p^{drift} + J_p^{diffusion} = q\mu_h E_x p - qD_p \frac{dp}{dx}$$

in equilibrium, there is no charge motion any more: $J_h^{total} = J_e^{total} = 0$

$$E_x = -\frac{D_n}{\mu_e n}\frac{dn}{dx}, \qquad E_x = +\frac{D_p}{\mu_h p}\frac{dp}{dx}$$

$$V_{b-i} = -\int E_x dx = -\int -\frac{D_n}{\mu_e n}\frac{dn}{dx}dx = \frac{D_n}{\mu_e}\int \frac{1}{n}dn$$

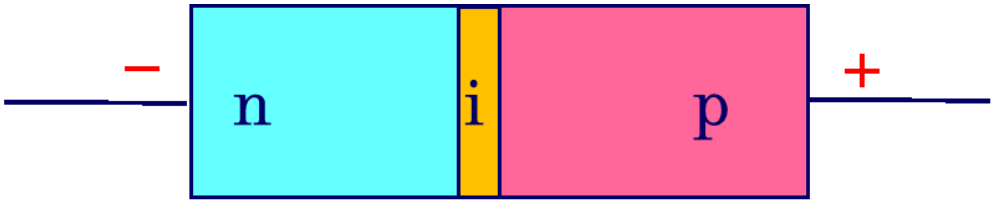
$$= (D_n/\mu_e)\ln(n_n/n_p), \qquad (n_n = N_d, n_p = n_i^2/N_a)$$

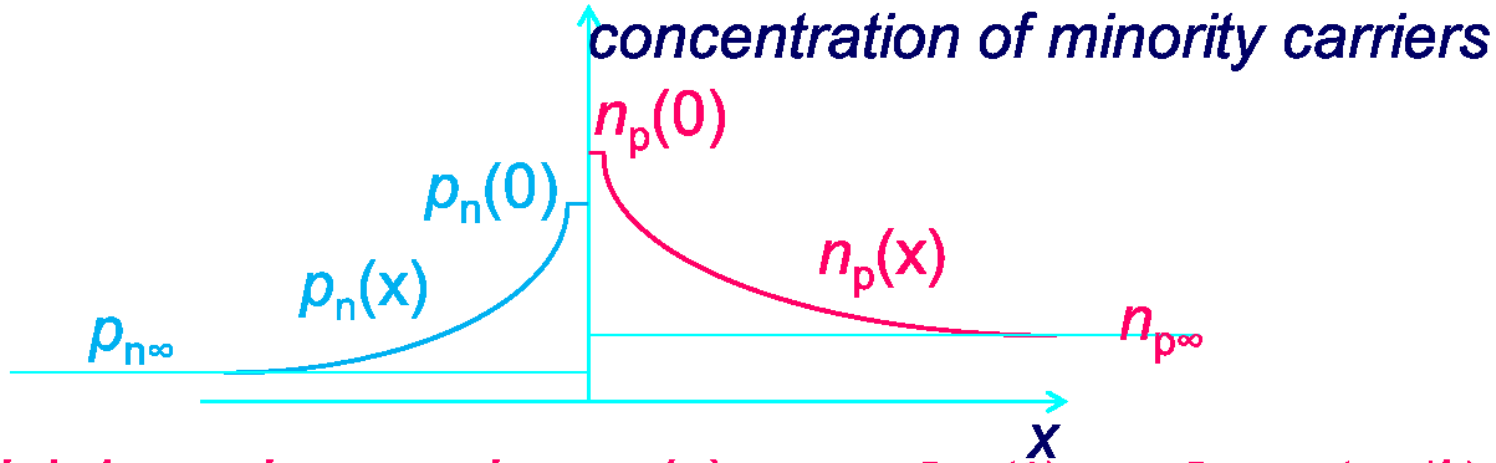
$$\approx (kT/e)\ln\left(N_d N_a/n_i^2\right)$$

For silicon with N_A=N_D=5*10^{15} cm^{-3}, n_i=p_i≈10^{10} cm^{-3}, room temp.:

$V_{b\text{-}i}$≈0.026V ln (25*10^{10}) ≈ 0.68V

Diode Characteristics





exponential decay in p–region: $n_p(x)=n_{p\infty} + [n_p(0)-n_{p\infty}] \exp(-x/L)$

exponential decay in n–region: $p_n(x)=p_{n\infty} + [p_n(0)-p_{n\infty}] \exp(x/L)$

approximations: applied voltage (bias)drops almost exclusively across depletion region and Maxwell-Boltzmann distribution

$n_n/n_p = p_p/p_n = \exp[eV_{b\text{-}i}/(kT)]$ is valid

Diode Characteristics

exponential decay in p-region: $n_p(x)=n_{p\infty}+[n_p(0)-n_{p\infty}]\exp(-x/L_n)$

exponential decay in n-region: $p_n(x)=p_{n\infty}+[p_n(0)-p_{n\infty}]\exp(x/L_p)$

approximations: applied voltage (bias)drops almost exclusively across depletion region and Maxwell-Boltzmann distribution

$n_n/n_p = p_p/p_n = \exp[eV_{b\text{-}i}/(kT)]$ is valid

-> $n_n = n_p \exp[eV_{b\text{-}i}/(kT)] \approx n_p(0)\exp(-x/L)\exp[eV_{b\text{-}i}/(kT)]$

$\approx n_p(0)\exp[e(V_{b\text{-}i}-V_d)/(kT)]$ where V_d is the applied bias

-> diffusion currents in depletion region:

$j_n|_{x=0} = eD_n\,\partial n_p/\partial x|_{x=0} = eD_n\,n_p(0)/L_n\,[\exp(eV_d/(kT)-1]$

$j_p|_{x=0} = -eD_p\,\partial p_n/\partial x|_{x=0} = eD_p\,p_n(0)/L_p\,[\exp(eV_d/(kT)-1]$

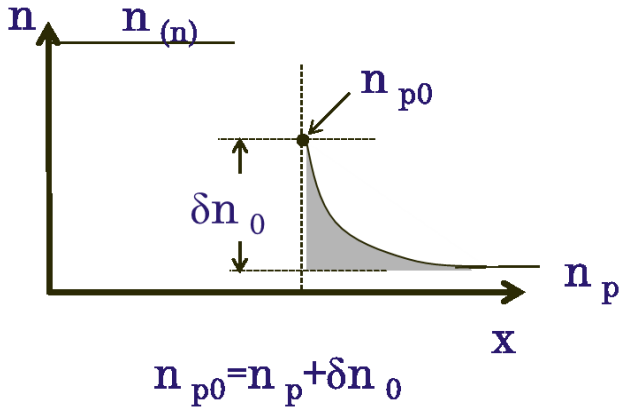
-> total diode current through area A is $I_d=A(j_n+j_p)$, hence

$I_d=I_S[\exp(eV_d/(kT)-1]$ where $I_S=eA[D_p\,p_n(0)/L_p+D_n\,n_p(0)/L_n]$

Diode Characteristics

$$V_{b-i} = (kT/e)\ln(n_n/n_p)$$
$$n_{p0} = n_p + \delta n_0$$

$$n_n = n_p \exp\left(\frac{eV_{b-i}}{kT}\right) \quad *$$



Modify to include applied potential, we get this in terms of n_{p0}

$$n_n = n_{p0} \exp\left(\frac{e(V_{b-i} - V_d)}{kT}\right)$$

$$\delta n_0 = n_{p0} - n_p$$

$$\delta n_0 = \frac{n_n}{\exp\left(\frac{e(V_{b-i}-V_d)}{kT}\right)} - \frac{n_n}{\exp\left(\frac{eV_{b-i}}{kT}\right)} = \frac{\exp\left(\frac{eV_d}{kT}\right) n_n}{\exp\left(\frac{eV_{b-i}}{kT}\right)} - \frac{n_n}{\exp\left(\frac{eV_{b-i}}{kT}\right)}$$

But from *

$$\delta n_0 = n_p\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right), \qquad similarly\ for\ holes \quad \delta p_0 = p_n\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$

Diode Characteristics

Diffusion currents in the depletion region

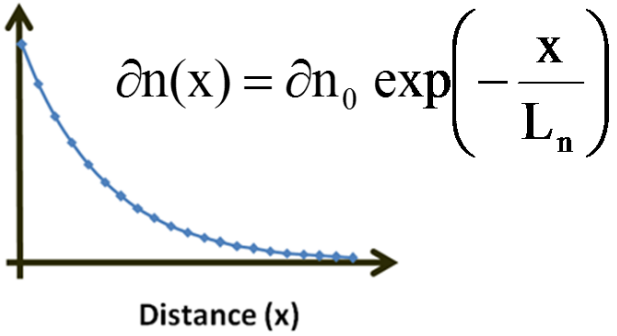
$$j_n(x=0) = eD_n \frac{\partial n_p}{\partial x}(x=0)$$

$$j_p(x=0) = -eD_p \frac{\partial p_n}{\partial x}(x=0)$$

$$\delta n_0 = n_p\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$

$$j_n = eD_n \frac{n_p(0)}{L_n}\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$

$$j_p = eD_p \frac{p_n(0)}{L_p}\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$



Total diode current through area A is $I_d = A(j_n + j_p)$

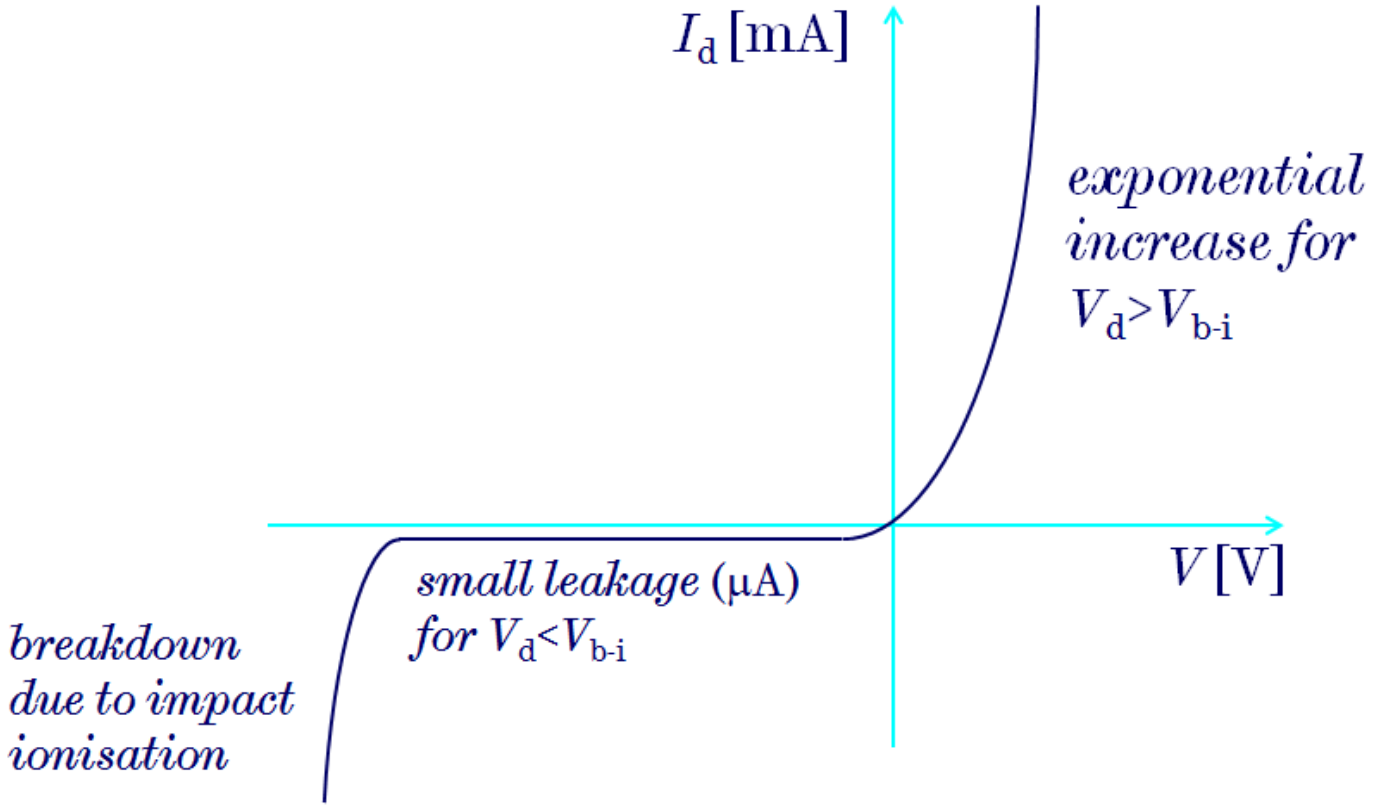
Hence $$I_d = I_s\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$

Where $$I_s = eA\left[\frac{D_p p_n(0)}{L_p} + \frac{D_n n_p(0)}{L_n}\right]$$

Diode Characteristics

$$I_d = I_s\left(\exp\left(\frac{eV_d}{kT}\right) - 1\right)$$

Is known as Shockley's diode equation



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Types of diode and applications

rectifying diode: blocks for $V<V_{b\text{-}i}$ and conducts for $V>V_{b\text{-}i}$

biasing diode: yields voltage drop of $V_{b\text{-}l}$ (~0.6V for silicon)

LEDs: light-emitting diodes when a direct band-gap semiconductor pn-junction is forward biased with $eV>E_g$ so electrons and holes are injected from opposite ends and recombine near the contact area, creating photons (light)

Zener diodes: reverse biased, yield constant voltage drop independent of current flow

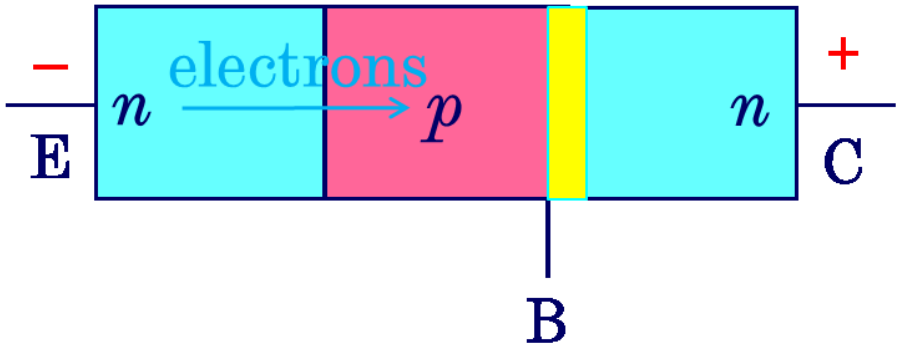
APDs: avalanche photodiodes are operated under very strong reverse bias (so normally only leakage current); if a high-energy photon or X-ray strikes, it produces e-h pairs that can be separated in the field and due to their high energy produce an avalanche of further charge carriers (-> high current pulse)

And of course Solar Cells, Lasers etc. rely on diode behaviour too!

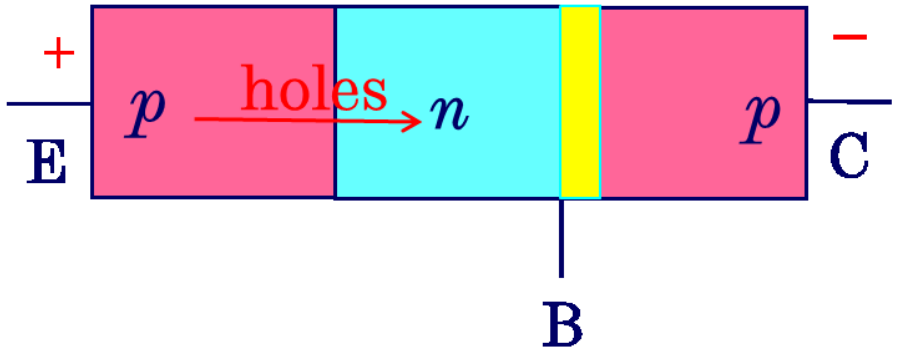
Principle of Bipolar Junction Transistor (BJT)

principle: connect 2 diodes with same doping back-to-back so you get a 3-terminal device and operate one diode just under forward bias (base-emitter, BE) and the other under reverse bias (base-collector, BC)

npn: V_{BE}~0.7V, V_{CB}>>1V



pnp: V_{BE}~–0.7V, V_{CB}<< –1V



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EEE6212 Lecture 20 “Transistors”

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Outline

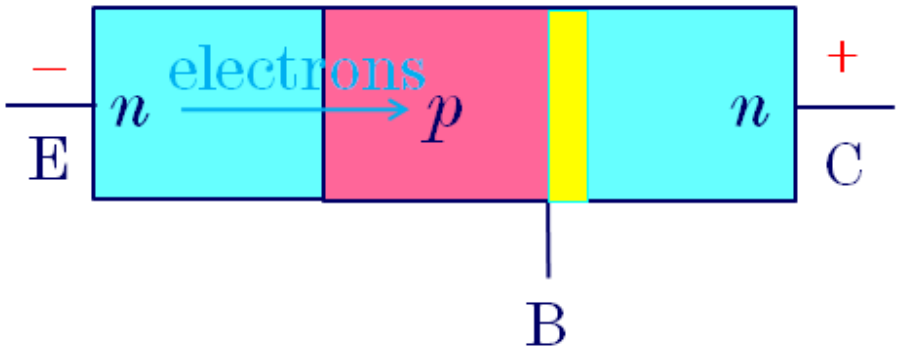
- principle of bipolar junction transistors (BJTs)
- transconductance
- transistor families
- BJT properties
- MOSFET design and properties
- multigate MOSFET devices

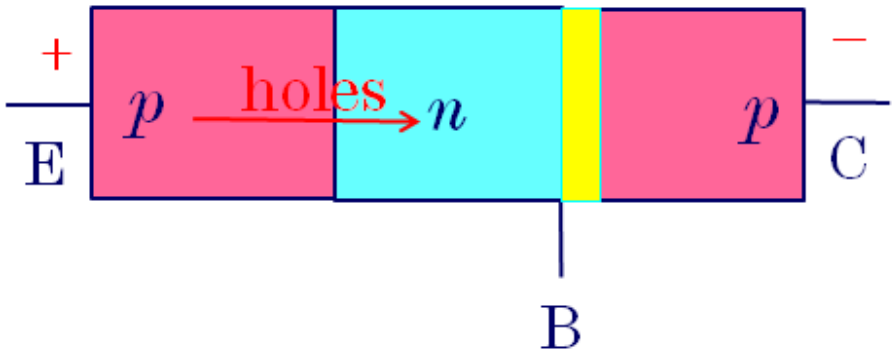
Principle of Bipolar Junction Transistor (BJT)

principle: connect 2 diodes with same doping back-to-back so you get a 3-terminal device and operate one diode (just) under forward bias (base-emitter, BE) and the other under reverse bias (base-collector, BC)

npn: V_{BE}~0.7V, V_{CB}>>1V

pnp: V_{BE}~–0.7V, V_{CB}<< –1V





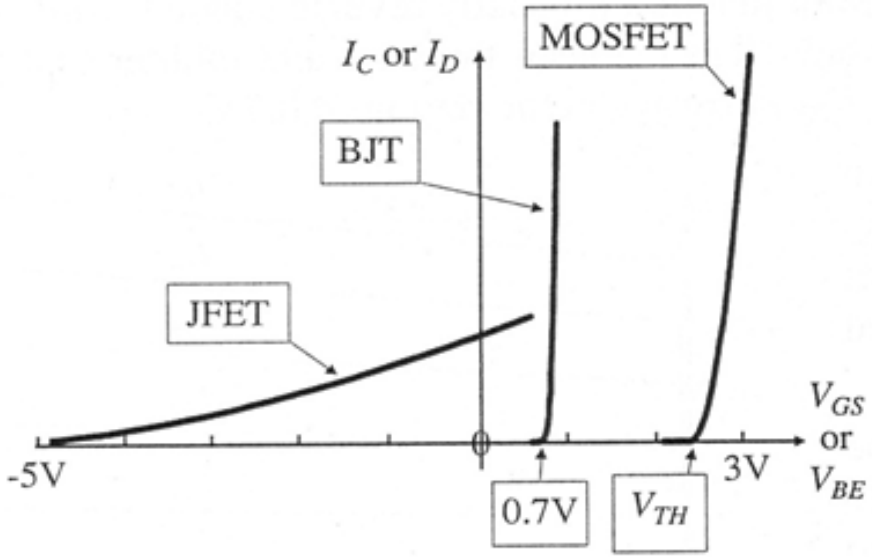
General Transistor Behaviour

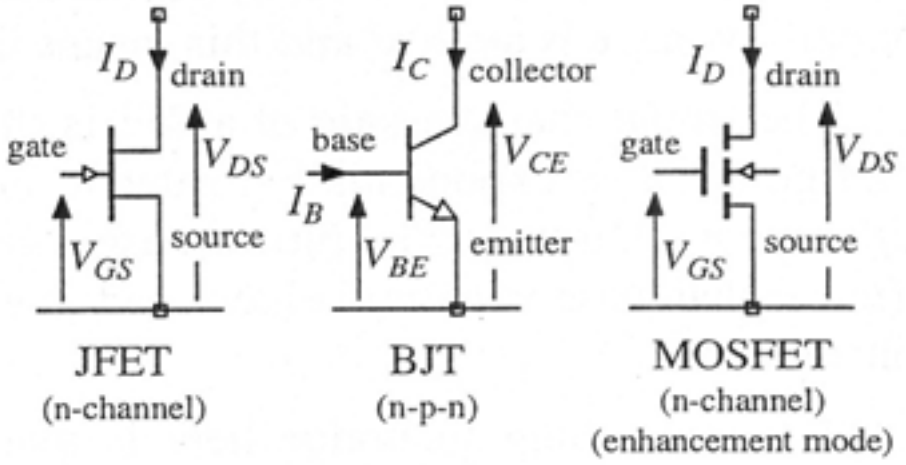
Transconductance is the relationship between :

input control voltage (V_{BE} for a BJT; V_{GS} for a FET) and

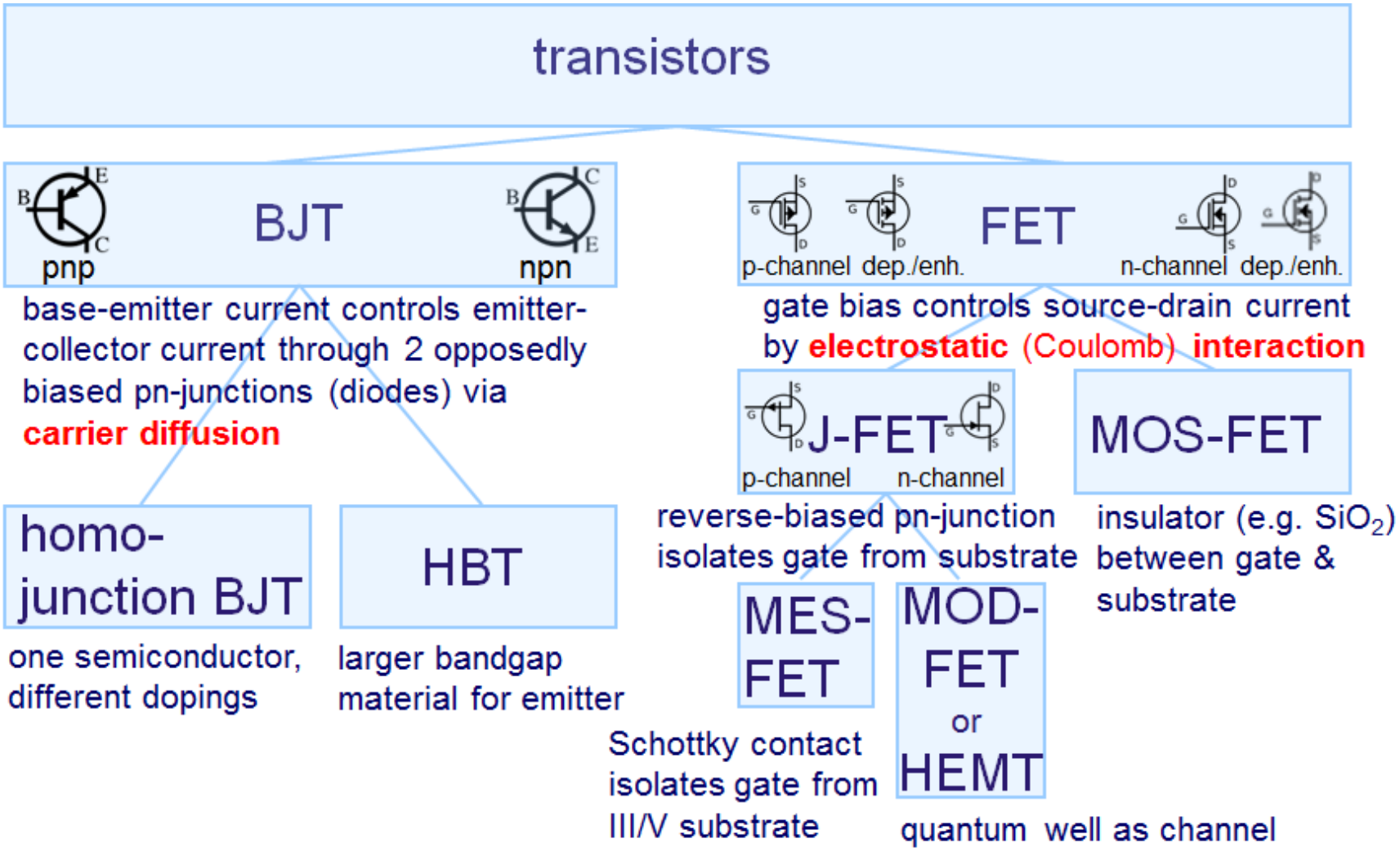
output (controlled) current (I_C for BJT, I_D for FET).

These curves are similar in shape for all transistor types, with a rapid current increase after some threshold is reached. The slope of these curves is called mutual conductance, g_m, or transconductance.





Transistor Families



Can keep subdividing the transistor family based on differences….

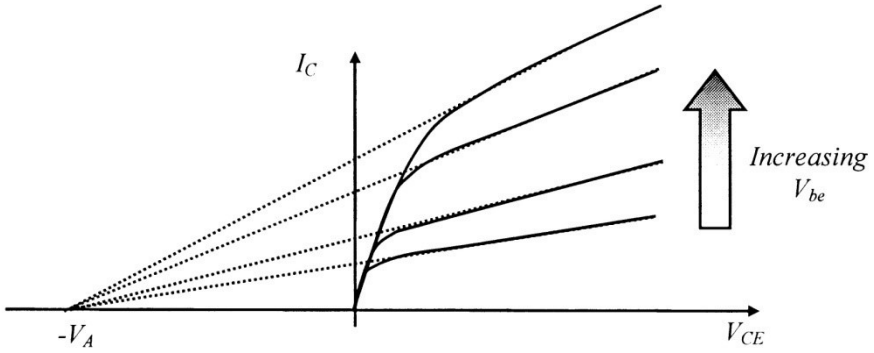
Important BJT relationships

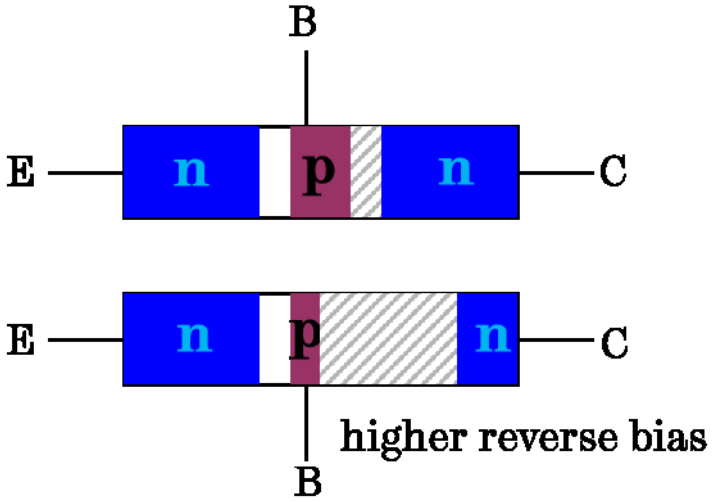
Parameter	Relationship
β	small signal current gain through r_{be} $\quad \beta = \frac{dI_c}{dI_b}$
g_m	transconductance, defined as $g_m = \frac{dI_c}{dV_{be}}$ (with $V_{ce} = const$)
	From $I_c = I_{c_0} \exp\left[\left(\frac{qV_{be}}{kT}\right) - 1\right] \approx I_{c_0} \exp\left[\frac{qV_{be}}{KT}\right]$ then in forward bias
	$g_m = \frac{q}{KT} I_c \exp\left[\frac{qV_{be}}{kT}\right] \approx \frac{qI_{c_0}}{kT}$, if $h_{FE} \gg 1$
r_{be}	small signal input impedance, defined as
	$r_{be} = \frac{dV_{be}}{dI_{be}}$ (with $V_{ce} = const$)
	From $g_m = \frac{dI_c}{dV_{be}} = \frac{dI_c}{dI_b} \times \frac{dI_b}{dV_{be}} = \frac{\beta}{r_{be}}$ we directly get $r_{be} = \frac{\beta}{g_m}$

Note that in small signal terms $r_{be} = v_{be}/i_b$ hence also $\beta i_b = g_m b_{be}$

This means that the BJT can be considered as a current or voltage amplifier

The Early Effect



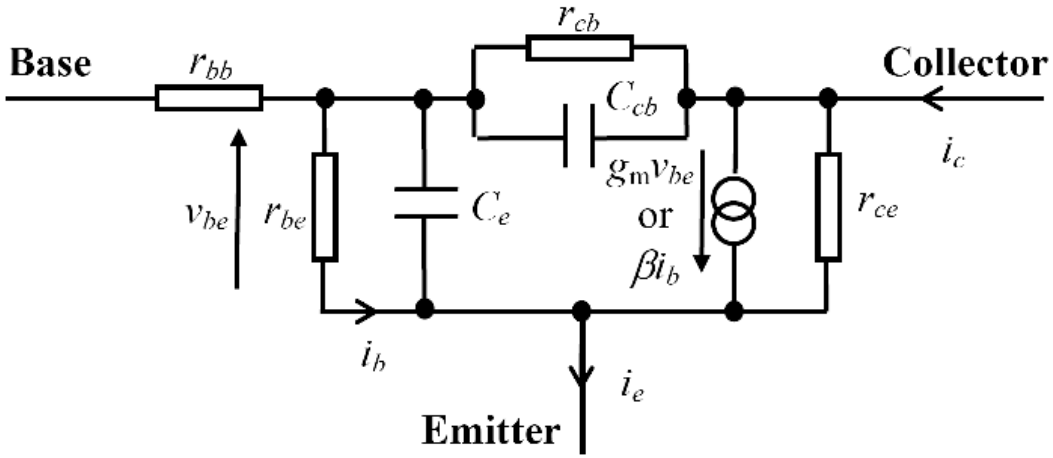


The base-collector depletion region (hatched area) increases with increasing base-collector voltage V_{cb}. The base width shrinks correspondingly. Then more carriers (e^- in the case on an npn-BJT) transit the base because

1) The time for crossing the narrower base decreases and more charge carriers can transit the base without undergoing recombination (hence I_c increases)
2) The charge gradient across the base increases, hence also I_e increases

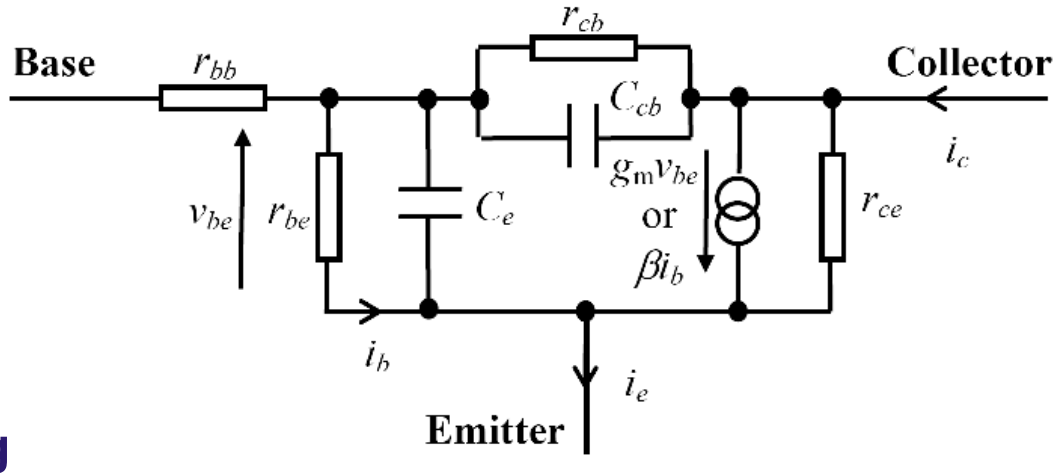
The result of a larger net current gain α is a finite slope on the output characteristic, corresponding to a smaller output impedance, r_0. This is bad if one wants to construct a current source which ideally would have $r_0 \to \infty$ so that any voltage change across the BJT would not cause any change in the output current (all ideal curves would be horizontal). So, if the transistor has a high impedance load, such as a current source, then we need to **model the Early effect of reduced base width by including serial resistors r_{ce} (and sometimes also r_{cb}).**

Small signal circuit model of a BJT



Symbol	Meaning
r_{bb}	base spreading resistance = series resistance between pacckge wire and active part of semiconductor; can be ignored in many cases; typically $0.5\Omega < r_{bb} < 50\Omega$
r_{be}	base incremental resistance of base-emitter junction ($\propto 1/I_b$); inverse gradient of $I_b(V_{be})$
r_{bc}	feedback resistance modelling the Early effect ($\propto 1/I_c$); may be ignored for analytical purposes **unless the transistor has a high impedance load**
r_{ce}	models the small slope of output characteristic, mostly due to the Early effect ($\propto 1/I_c$); may also be ignored **unless transistor has a high impedance load**
C_{cb}	base-collector depletion capacitance ($\propto V_{cb}$)
C_e	emitter diffusion capacitance that models the transient behaviour of charge crossing the pn-junction
b	small signal current gain for the current through r_{be}
g_m	transconductance which operates on the voltage across r_{be}

BJT cut-off frequency



Param.	Meaning
C_e	emitter diffusion capacitance can be determined from measurements of the transition frequency f_t which is the intrinsic, no-load, figure of merit of the speed for a BJT

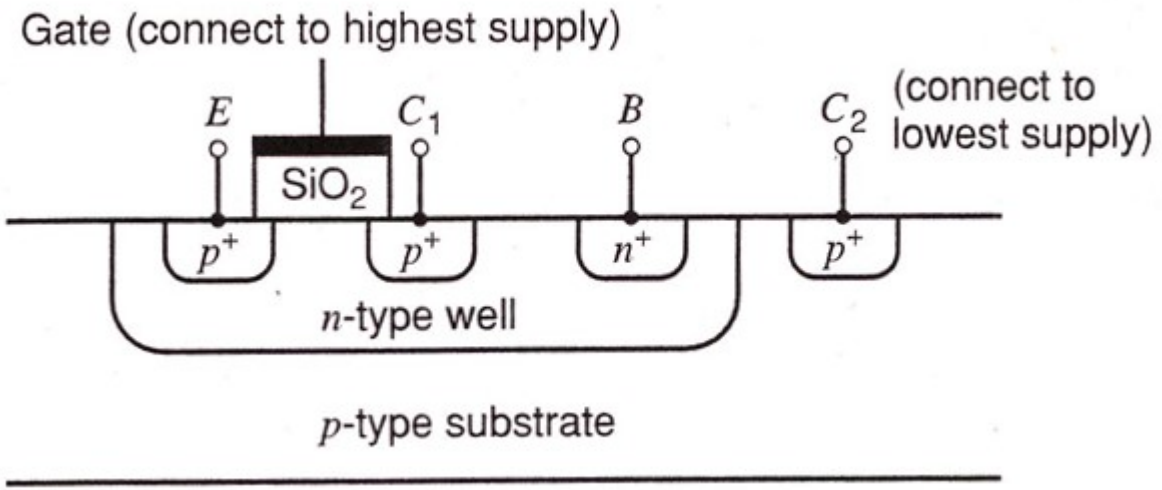
$$f_t = \frac{g_m}{2\pi(C_e + C_{cb})} \approx \frac{g_m}{2\pi C_e}, \qquad if\ C_e \gg C_{cb}$$

Deduction: Consider frequency $f = \omega/2\pi$ of a resonant circuit with R_{eff}, C_{eff} when all the energy is alternately stored in R_{eff} and in C_{eff} so that $R_{eff} = 1/\omega C_{eff}$.

This gives $\omega = 1/(R_{eff}C_{eff})$. Here $i_e = 0$ if the voltage $v_{be} = i_b r_{be}$ corresponds to the voltage drop across $C_{eff} = C_e + C_{cb}$ (as they are in parallel) where a larger current βi_b flows.

Setting $r_{be} i_b = \beta i_b/(\omega C_{eff})$ with $r_{be} = \beta/g_m$ gives the above

BJT design in CMOS technology



If collector C_1 is incorporated into the well, then a lateral pnp-BJT is formed by $E - B - C_1$ where the additional MOSFET gate ensures reverse biasing (i.e. corresponding source drain contacts operate in the cut-off region

BUT

A biased substrate forms the collector of a parasitic vertical pnp-BJT formed by $E - B - C_2$ for some electrons diffusing out of the n-well

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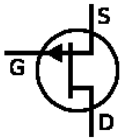
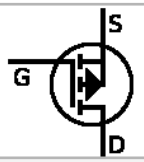
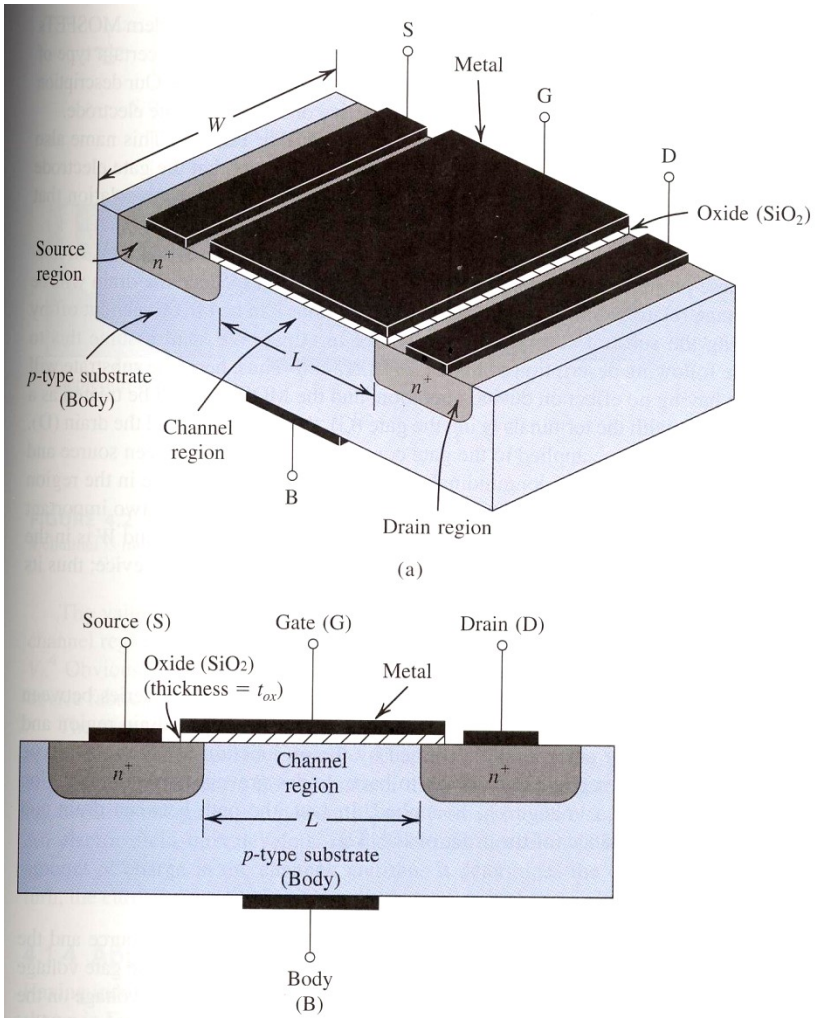
Comparison of transistor types BJT vs. JFET vs. MOSFET

Criterion	BJT 	JFET 	MOSFET 
Principle	**Diffusion** through one forward and one reverse biased diode (depletion region)	Reverse-biased pn-junction isolates gate from substrate	Gate bias controls source-drain current by **electrostatic** interaction across insulating gate
Input current	$i_B = i_C/\beta$ (μA)	Small	$i_G \approx 0$ (pA)
Input impedance	Low	High	Very high
I/V transfer character.	Exponential (exact)	Modified square law	Square law (approx.)
Transconductance	High	Medium	Low
Carrier type	Minority	Minority (depletion mode)	Majority
Radiation resistance	Low	?	High
Zero-offset of $I_c(V_{ce})$ or $I_{DS}(V_{DS})$	Yes	?	None
Gate-channel breakdown	-	Partly reversible	Irreversible = Destructive
Applications	Audio amplifiers Phototransistors	High power radio transmitters, low noise differential amplifiers	Switches Charge measurement devices

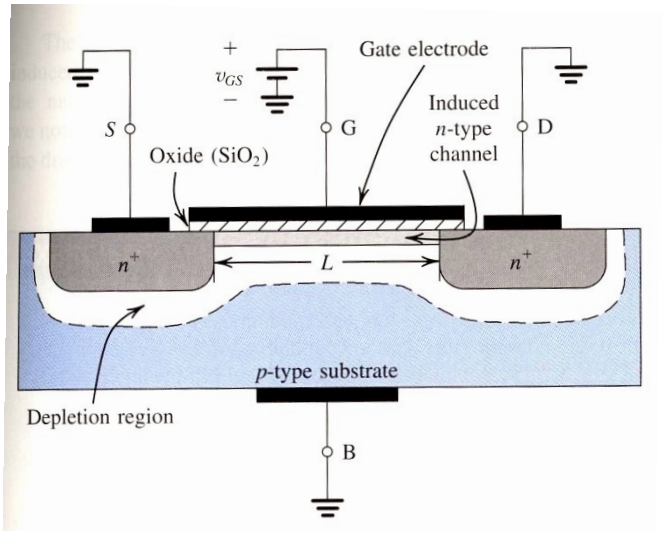
MOSFET design in CMOS technology



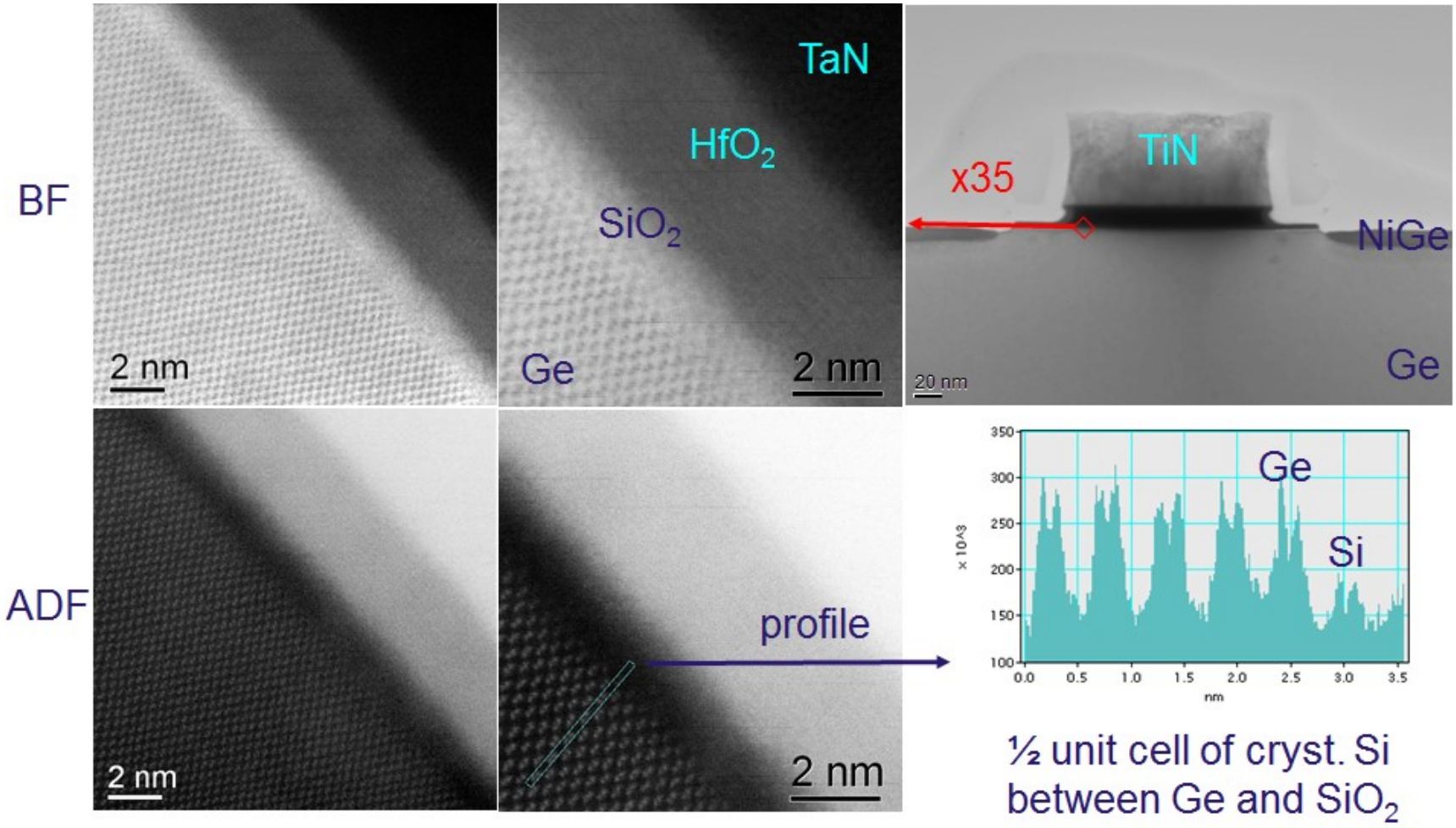
Left: Enhancement type n-MOSFET

Bottom Left: cross section

Bottom Right: n-channel for positive gate biases

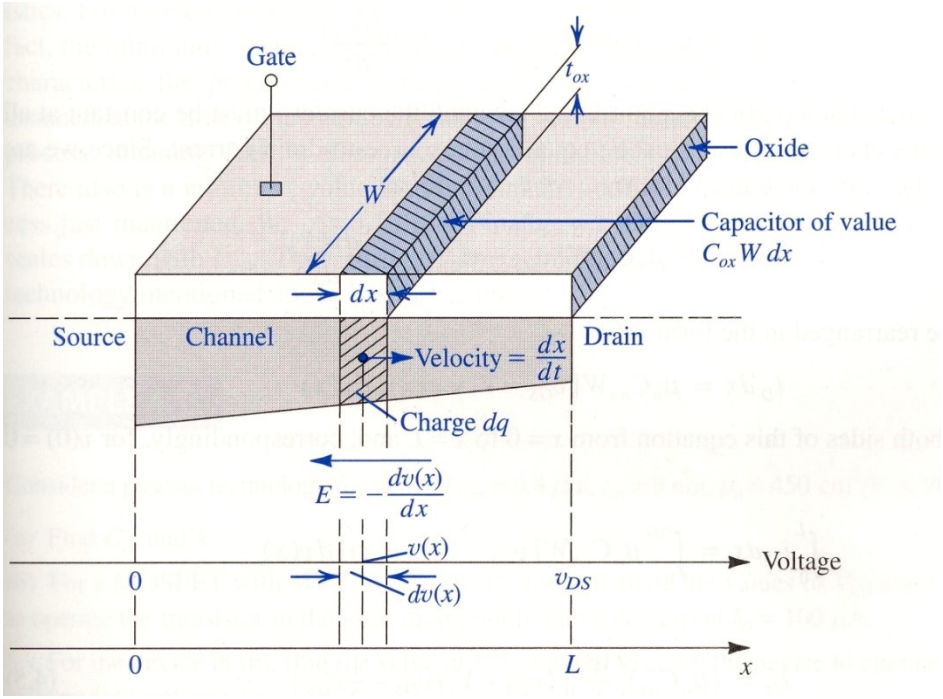


MOSFETs at atomic resolution



Annular Dark Field (ADF) and Bright Field (BF) images in a Scanning Transmission Electron Microscope

MOSFET output characteristic



Capacitance of gate oxide per unit area

$$C_{ox} = \epsilon_{SiO_2}\epsilon_0/t_{ox}$$

Capacitance of an infinitesimal strip of gate at a distance x from source contact $C_{ox}Wdx$

Effective voltage here

$$V = V_{GS} - V_{to} - v(x)$$

Charge in infinitesimal strip of n-channel:

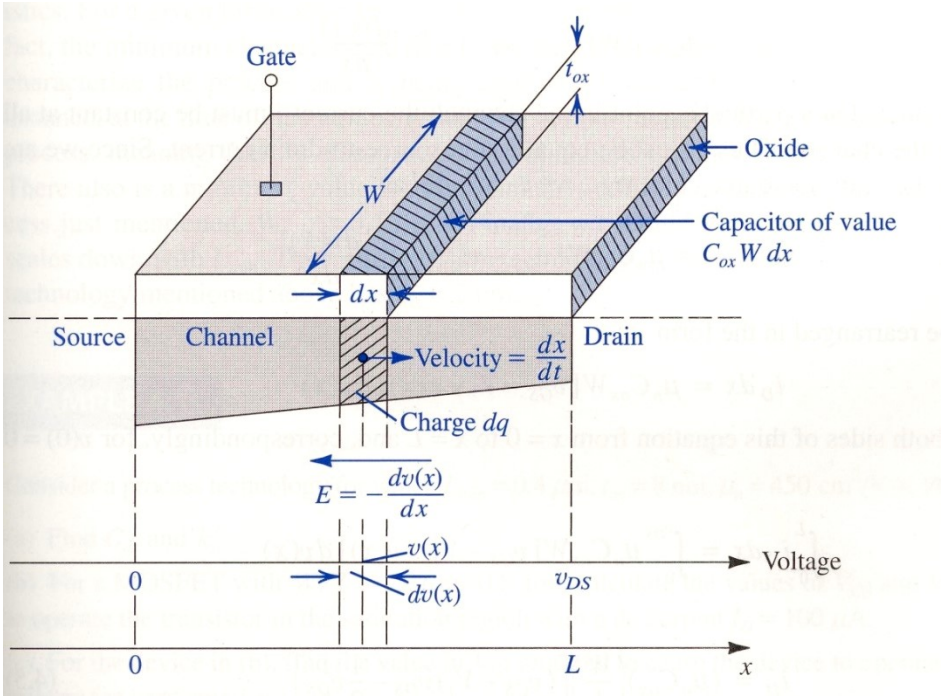
$$dq = -C_{ox}Wdx[V_{GS} - V_{to} - v(x)]$$

Electric field at this point

$$E(x) = -\frac{dv(x)}{dx}$$

This causes the charge dq to drift towards the drain …

MOSFET output characteristic



This causes the charge dq to drift towards the drain with a velocity given by the mobility of the electrons μ_n

$$\frac{dx}{dt} = -\mu_n E(x) = \frac{\mu_n dv(x)}{dx}$$

Resulting drift current

$$i = \frac{dq}{dt} = \frac{dq}{dx} \times \frac{dx}{dt}$$

$$= -\mu_n C_{ox} W [V_{GS} - V_{to} - v(x)] \frac{dv(x)}{dx}$$

Drain-source current

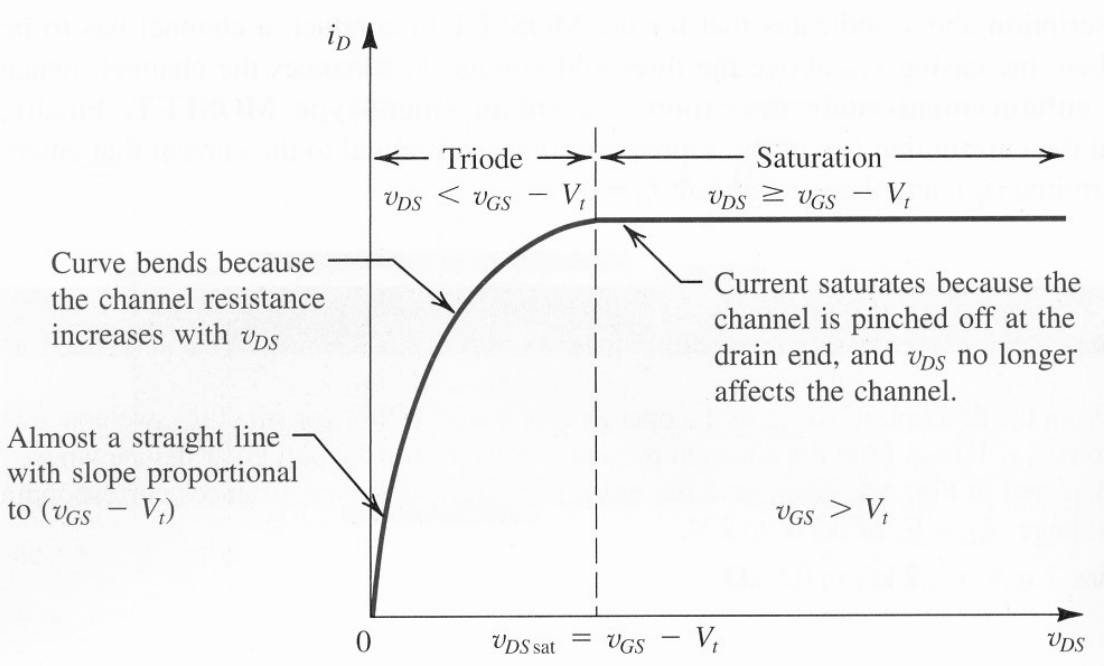
$$i_D = -i = \int_0^L i_D dx$$

Where $v(0) = 0\ at\ x = 0$
and $v(L) = V_{DS}\ at\ x = L$

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{to})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

MOSFET output characteristic (modes)

General form $$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{to})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$



Triode Region: $V_{DS} < V_{OV}$

$$i_D \approx \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{to})V_{DS}$$

Saturation Region: $V_{DS} \geq V_{OV}$

$$i_D \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{to})^2$$

Overdrive Voltage V_{OV}

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Derivation of MOSFET transconductance

In the saturation region

$$i_D \approx \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{to})^2$$

Differentiating yields transconductance

$$g_m = \frac{di_D}{dV_{GS}} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{to}) = \frac{2i_D}{V_{OV}}$$

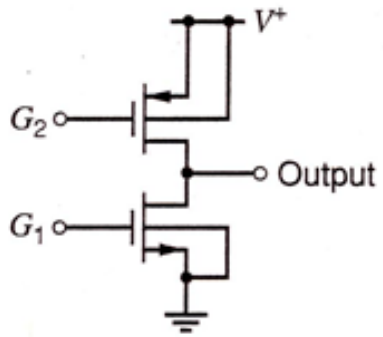
Is lower than for BJTs, as i_D is usually up to a few Amps,

whilst $V_{OV} = V_{GS} - V_{to} = 0.2 - 0.5V$

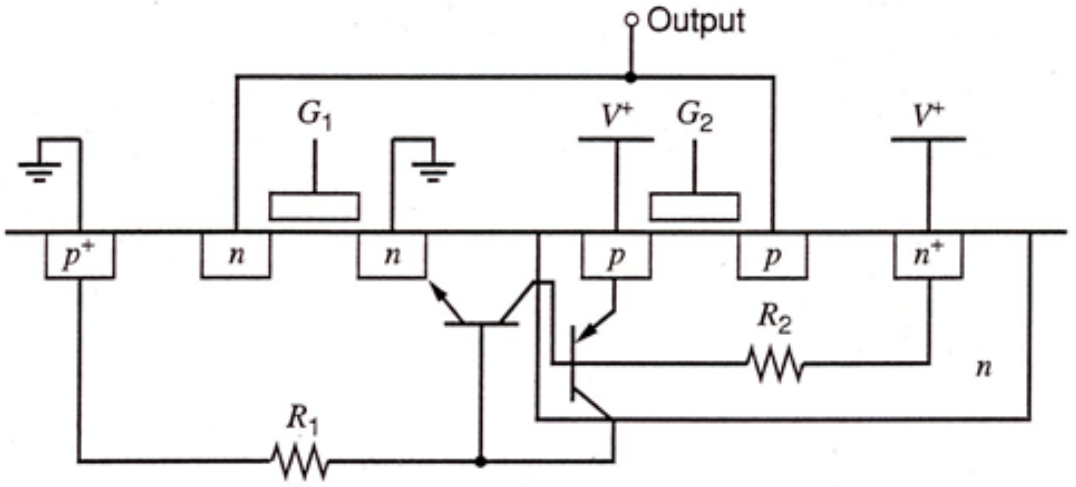
Hence use the ratio $\frac{i_D}{V_{OV}}$ as an operation design parameter

Latchup in CMOS technology

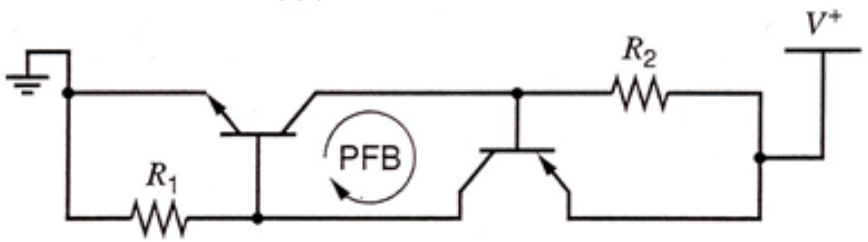
typical n-channel and p-channel MOSFET device pair involves several pn-junctions to impleme (e.g. as inverter)



formation of two parasitic BJTs by the n-well MOSFETs, a lateral npn a vertical pnp BJT

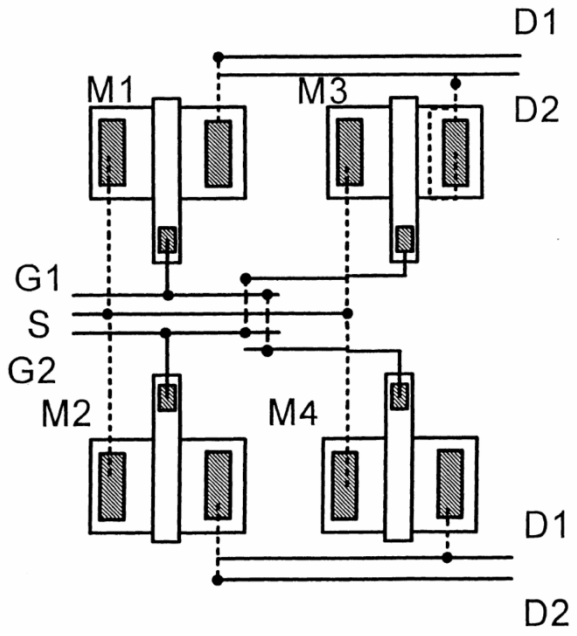


positive feedback occurs if the BJTs enter the active region, have $\beta > 1$ and start to conduct This can destroy the circuit.



Example of a typical MOSFET circuit: centroid layout

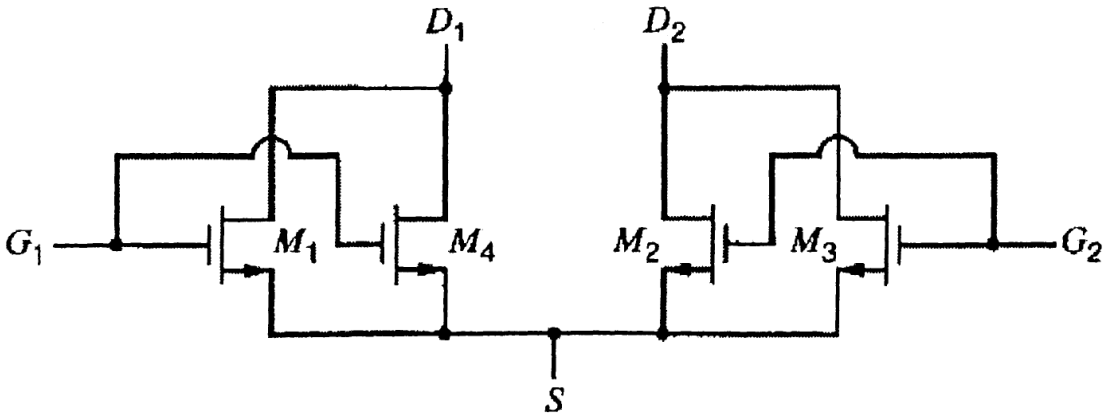
The circuit is a differential amplifier, as the source electrodes are connected to a common current source and the diff. signals are fed into opposite base electrodes.



Problem: diff. amplifiers are very sensitive to any mismatch between the two signal paths, which would increase the common-mode and decrease the diff. mode signal

Solution: replace single transistors by pairs of transistors at opposite positions on the substrate to eliminate linear process gradients, such as variations of t_{ox}, that can be decomposed into x- and y- components.

Disadvantage: longer lines for cross-connection



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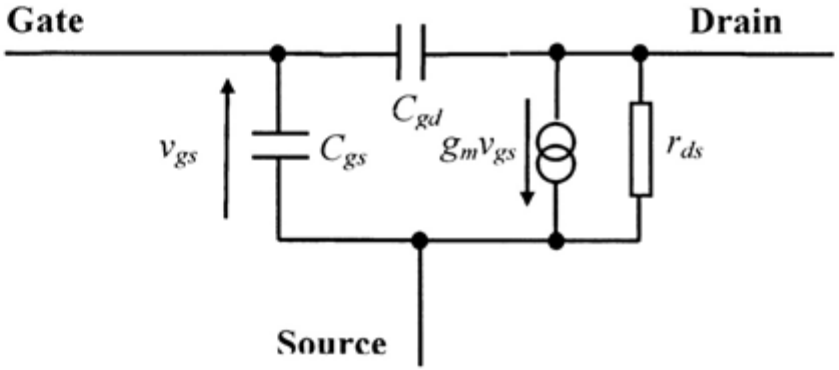
Body or Substrate effect in MOSFETs

problem: substrate acts as 4th terminal (called body) which results in another pn-junction between the induced channel and the substrate

substrate is usually common to many MOSFETs within a device and connected to most negative [positive] supply voltage in NMOS [PMOS], hence resulting reverse bias V_{SB} between source and body (in NMOS)

This will affect device operation by widening the depletion region and reducing the channel depth, so that V_{GS} has to be increased to maintain constant operation conditions and keep i_D constant.

Small signal circuit model of a MOSFET

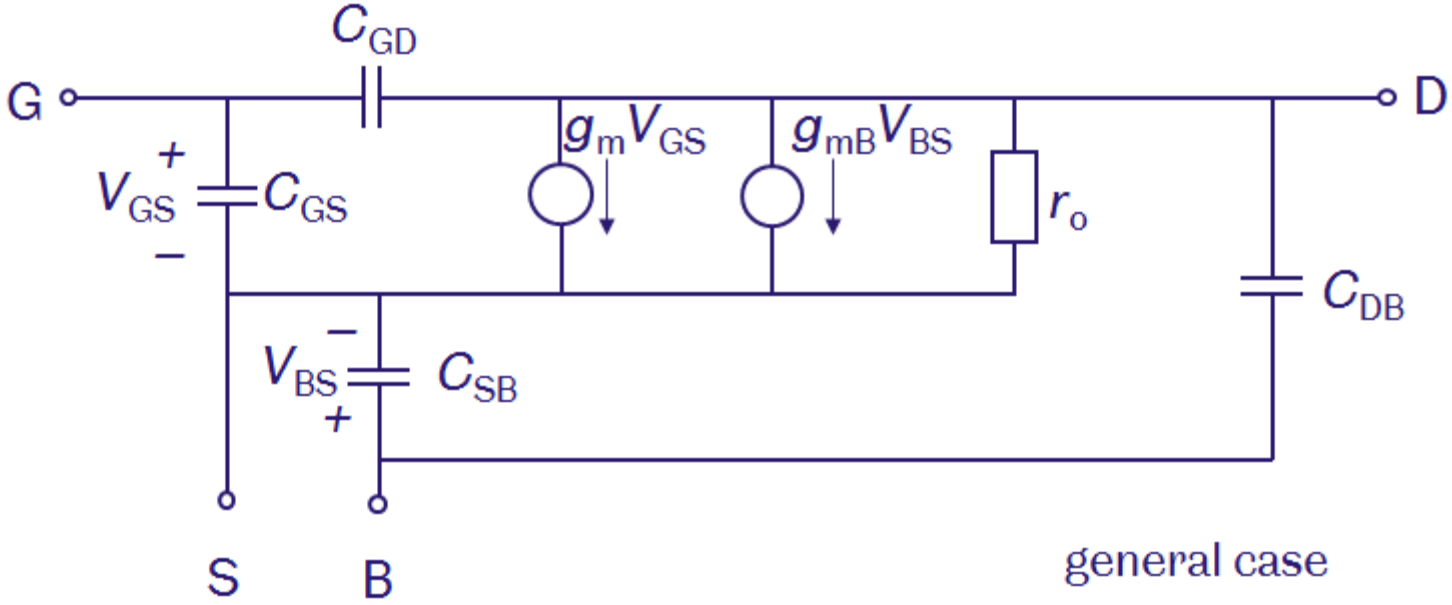


NB: Occasionally, you may also see a substrate on a MOSFET small signal circuit diagram as the substrate can act like an extra gate. Usually the substrate is connected to $-V_{dd}$. This needs to be taken into account only if there is ripple on V_{dd}.

symbol	meaning
C_{gs}	capacitance between gate and source contact
C_{gd}	capacitance between gate and drain contact
V_{gs}	voltage between gate and source
V_{thresh}	threshold voltage that must be applied to the gate-source connection to create a conducting channel (enhancement mode MOSFET), typically a few volts
r_{ds}	apparent resistance of the conducting channel between source and drain. As V_{ds} is increased above V_{thresh} the conducting channel changes shape (shortens) and I_d then depends on V_{ds} in the saturation region ($V_{ds} > V_{gs} - V_{thresh}$ = '**overdrive voltage**').
I_d	**drain current:** $I_d = \frac{1}{2}\,\mu C_{ox}\, W/L\, (V_{gs}-V_{thresh})^2\, (1+\lambda V_{ds})$, if $V_{ds} > V_{gs} - V_{thresh} > 0$ where μ is charge-carrier mobility, C_{ox} the gate oxide capacitance per unit area, W the gate width, L the gate length and λ the channel-length modulation parameter
g_m	**transconductance** of the MOSFET device: $g_m = 2\, I_d / (V_{gs}-V_{thresh})$
f_t	**transition frequency:** $f_t \approx g_m/(2\pi C_{gs})$

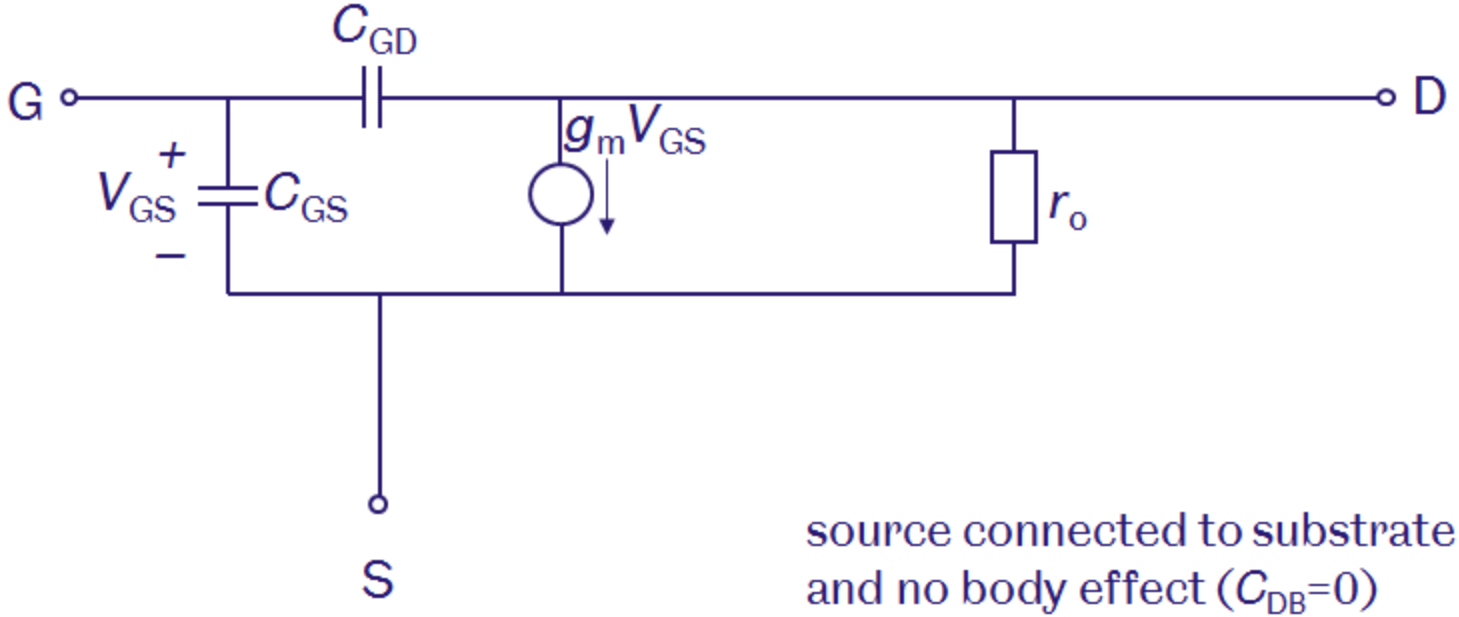
Gate capacitance and high frequency behaviour

Hybrid-π model for small high-frequency signals of MOSFET



general case

Hybrid-π model for small high-frequency signals of MOSFET



source connected to substrate ($V_{BS}=0$)
and no body effect ($C_{DB}=0$)

inject test current at gate: $i_i = j\omega(C_{GS}+C_{GD})V_{GS}$

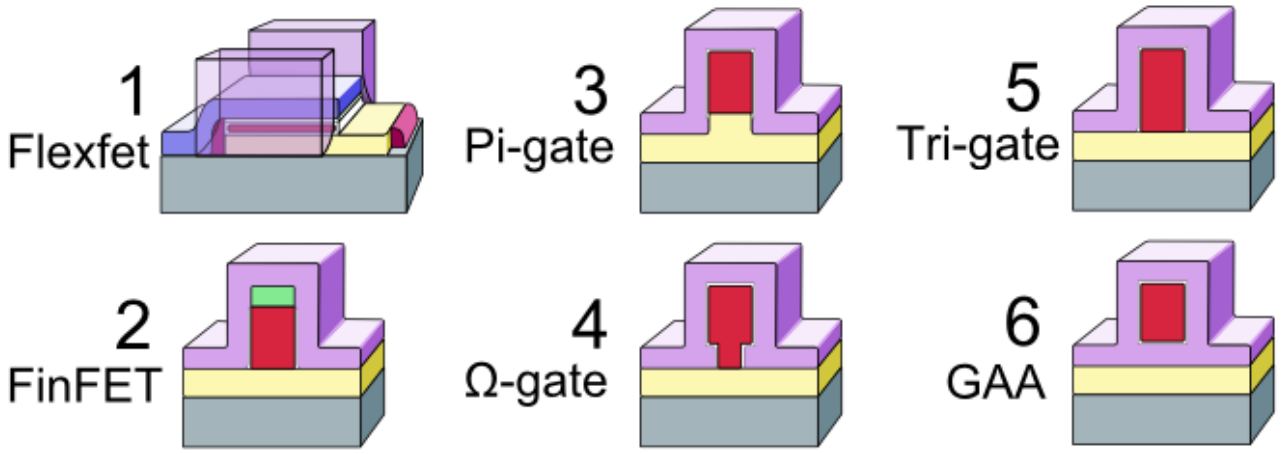
output current at drain: $i_o = g_m V_{GS} - j\omega C_{GD} V_{GS} \approx g_m V_{GS}$

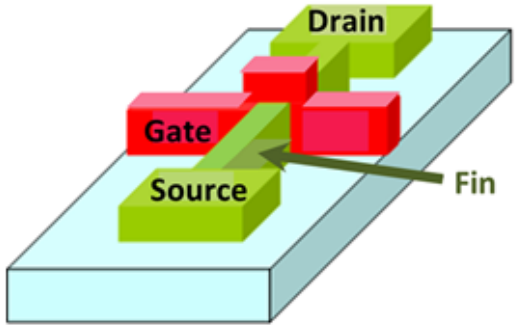
short-circuit current gain: $i_o/i_i \approx g_m/[j\omega(C_{GS}+C_{GD})]$

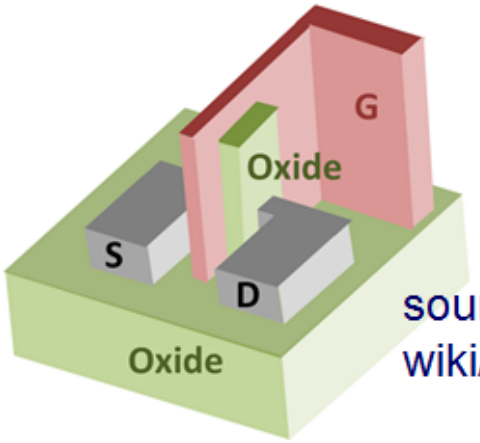
unity gain at frequency $f_T = g_m/[2\pi(C_{GS}+C_{GD})] = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$

Multigate MOSFET devices

basic idea: wrap channel by gate extension in 3D to get better electrical control and lower leakage current; presently at 16nm gate length
problem: non-planar design is more difficult to make







source:http://en.wikipedia.org/wiki/Multigate_device

