Examination Feedback for EEE310/6036 – Introduction to VLSI
Spring Semester 2011-12

General Comments:

A mixed set of attempts, some marred by simple lack of knowledge.

Question 1:

This question was generally very-well answered. Most people could generate the pull-up network quite well (although there were a few attempts that were hopelessly wrong). Additionally, there are still a few people who got confused about the method and attempted to put an inverter on the end of the circuit (they weren't penalized for this as long as they got the right pull-up network). Similarly, people found the function of the circuit quite readily and could, in the main, size the transistors. Where people lost marks was in section iv): they could tell me that the substrate connection of each nFET is connected to 0V but omitted to tell me that this was because the FETs are in a common area of p-type material (substrate or well).

Question 2:

The question was uniformly badly done. In part a) not too many people could tell me that non-overlapping clocks prevented overlap between the transparent phases in master-slave FFs. Very few people, clearly, had read the handout on DLLs that I circulated in part b) and, consequently, very few marks were picked up. In part c), nobody noticed that with a clock frequency of 350MHz in the sending domain, that the data frequency is 175MHz (a data signal from a FF, for example, can have a maximum frequency that is half the clock frequency). In some cases, people used the equation to calculate what the observation time should be, completely ignoring the fact that it is related to the clock frequency of the receiving domain. Moving on from this, again, nobody could work out that to get fewer than 10-9upsets/second requires the observation time to be increased by adding creating a chain of three FFs. It is almost as though I did not go through this in the lectures (which, of course, I did). Clearly, having not done well on parts i) and ii), it is not likely that people scored in part iii). In this case, what I really wanted was a comment about a signal taking 3 clock cycles at 1.2GHz to move to the other domain and then a clock cycle delay at 350MHz to move back to the first domain again creating quite long round-trip time.

Question 3:

The first part, relating to the derivation of the dynamic power dissipation is book work and, disappointingly, some people had trouble with this – omitting steps and not giving adequate explanations.

In part b) people tended not to describe what happens with scaling and some people did not consider the various terms in eq 3.1.

In the power dissipation calculation, the major problems were:
Not considering the sizing of the transistors;
Double counting of capacitances;
Not considering the drain capacitances;
Not including alpha. In this regard, a lot of people used a value of alpha at the input to calculate the probability of a change at the output. All well and good, but just saying that you assumes that alpha=0.1, for example, was sufficient.

Question 4:

Whilst a lot of people identified the function and could draw the schematic, a lot of people omitted the substrate connections. However, some people drew the most fantastic schematics involving any number of transistors and then popped an inverter on the end!

The ratio of μ_E to μ_H is 2:1. However, nobody seemed to notice that the p+ source/drains of the pFETs are circa 4x the width of the n+ source/drains of the nFETs because the two pFETs are in series and should be 2x the width of the nFETs for this reason leaving the additional 2x explicable by the ratio of mobilities.

Again, nobody gave an adequate description of the self-aligned gate process where source and drain regions are implanted with the polysilicon, forming the gate, in place so that the gate gets doped similarly to the source and drain regions and the polysilicon gate acts as a mask keeping the region below it as it was originally doped.