Solutions to EEE6213 Principles of Semiconductor Device technology: 2014-15.

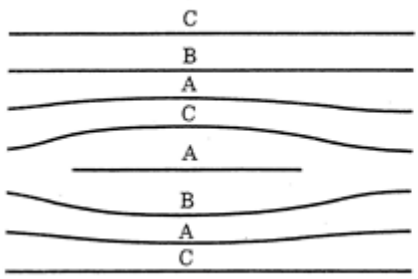
1a: If Si atoms replace Ga atoms within the GaAs lattice, the material will be **n-type** because Si has one more valence electron than Ga (which has three valence electrons). This "extra" valence electron can easily escape the Si atom to become a conduction electron. (The Si atom becomes positively ionized, as a result.) (1)

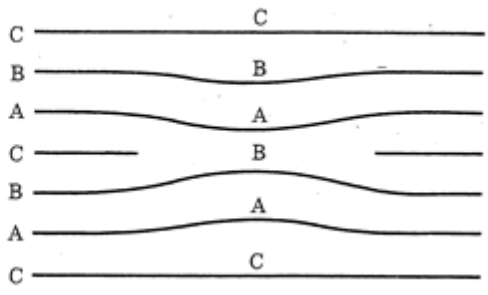
If Si atoms replace As atoms within the GaAs lattice, the material will be **p-type** because Si has one less valence electron than As (which has five valence electrons). An electron from a nearby covalent bond can easily move to the Si atom to fill its outmost electron shell, creating a hole. (The Si atom becomes negatively ionized, as a result.) (1)

An antisite defect is As taking the place of Ga and vice versa. (1)

Two diffusion mechanisms: any one of vacancy (frank-turnbull), interstitial, interstitialcy (kickout). (2)

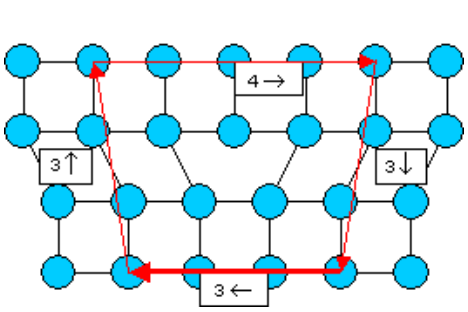
b) Two types of stacking faults, intrinsic and extrinsic.

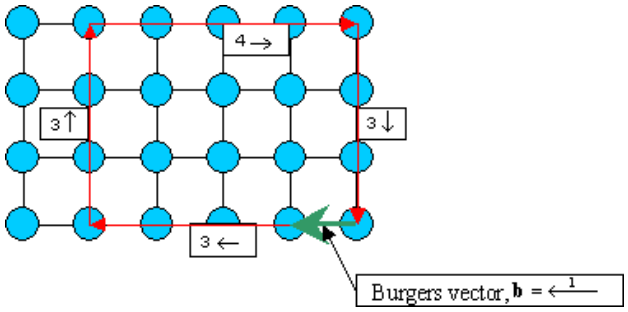




(1)

EXTRINSIC: CBACABAC (1) INTRINSIC: CBABAC. (1)





(1)

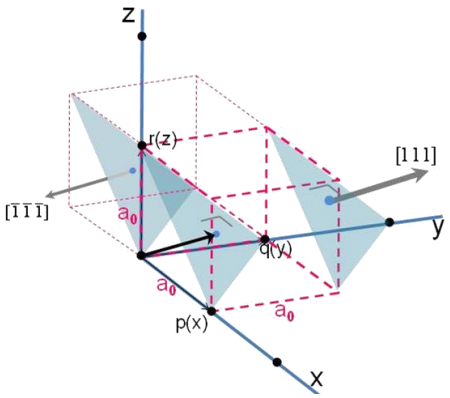
Trace around the end of the dislocation plane to form a closed loop. Record the number of lattice vectors travelled along each side of the loop. (Numbers in the boxes shown here).

In a perfect lattice, trace out the same path, moving the same number of lattice vectors along each direction as before. This loop will not be complete and the closure failure is the Burgess

vector. (1)

c) Miller indices relate to an x,y,z, coordinate system along the edges of the unit cell

A plane intersects these coordinates at three points: **p(x), q(y)** and **r(z)**
The Miller indices of the plane are h = 1/p, k = 1/q and l = 1/r
h,k and **l** must be multiplied up to integers. See diagram below. (1)

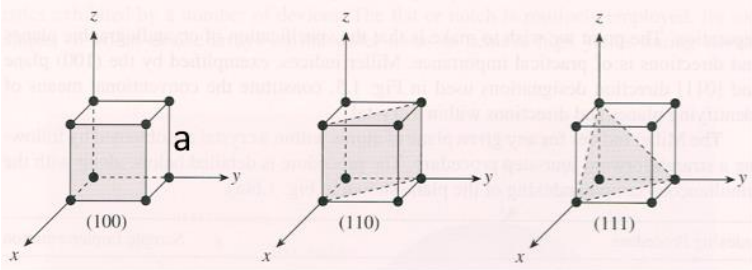


(1)

c. If two planes are at right angles, the dot product is zero.
Angle between planes $(h_1k_1l_1)$ and $(h_2k_2l_2)$ is given by
$\cos^{-1}[(h_1h_2 + k_1k_2 + l_1l_2)/\sqrt{((h_{12} + k_{12} + l_{12})(h_{22} + k_{22} + l_{22}))}]$

Since
$[121]\cdot[1\bar{1}1] = 0$ then (121) is perpendicular to $(1\bar{1}1)$
$[\bar{1}10]\cdot[1\bar{1}3] = 1$ then $(\bar{1}10)$ is not perpendicular to $(1\bar{1}3)$
$[\bar{1}00]\cdot[0\bar{1}3] = 0$ then $(\bar{1}00)$ is perpendicular to $(0\bar{1}3)$ (3)

1.d: The lattice constant of Si, a, is 5.43 Å. We have to calculate the number of atoms per unit area (cm^2) on the (100), (110) and (111) planes:



First, let's find the unit-cell area of these planes.

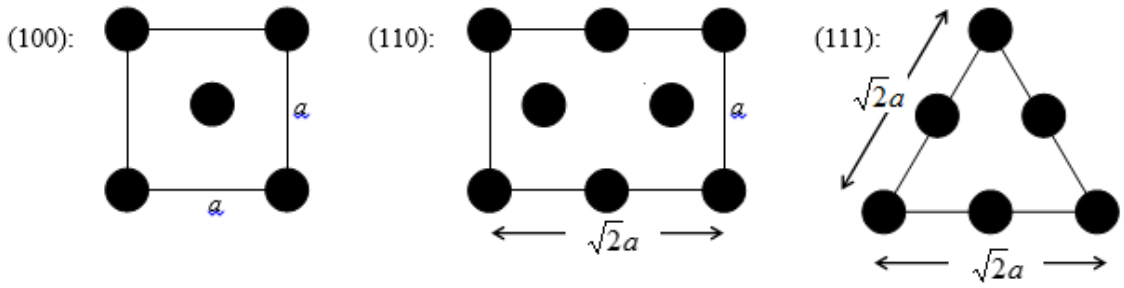
The area of the square region of the (100) plane within the unit cell is $A_{100}=a \times a = a^2$

The area of the rectangular region of the (110) plane within the unit cell is $A_{110} = a \times \sqrt{2}a = \sqrt{2}a^2$

The area of the triangular region of the (111) plane within the unit cell is

$$A_{111} = \frac{1}{2} \times \sqrt{2}a \times \frac{\sqrt{3}}{\sqrt{2}} a = \frac{\sqrt{3}}{\sqrt{2}} a^2$$

Next we need to determine how many atoms lie on each of these planes within the unit cell.



(1)

For the (100) plane, there are 4 atoms at the 4 corners and one atom in the middle. One fourth of each corner atom is enclosed within the unit cell, and middle atom is entirely within the unit cell, so the number of atoms on the (100) plane within the unit cell is $N_{100} = 4 \times (1/4) + 1 \times 1 = 2$.

For the (110) plane, there are $N_{110} = 4 \times (1/4) + 2 \times (1/2) + 2 \times 1 = 4$ atoms within the unit cell.

For the (111) plane there are $N_{111} = 3 \times (1/6) + 3 \times (1/2) = 2$ atoms within the unit cell.

Atomic density on the (100) plane = $N_{100} / A_{100} = 2/a^2 = 6.78\times10^{14}$ atoms/cm^2 **(1)**

Atomic density on the (110) plane = $N_{110} / A_{110} = 4/\sqrt{2}\, a^2 = 9.59\times10^{14}$ atoms/cm^2 **(1)**

Atomic density on the (111) plane = $N_{111} / A_{111} = 2/(\sqrt{3}/2)\, a^2 = 7.83\times10^{14}$ atoms/cm^2 **(1)**

The (110) plane has the highest atomic density and hence is best for p-channel MOSFET performance. **(1)**

2a) i Since hole drift velocity $v_{dr} = \mu_p . E_p$ $\mu_p = v_{dp} / E = 3.5\times10^5/1000 = 350$ cm^2/Vs. (3)

(ii)Since $\mu_p = q\tau / m_p^*$ where τ is the average time between scattering events and m_p^* is the hole conductivity effective mass,

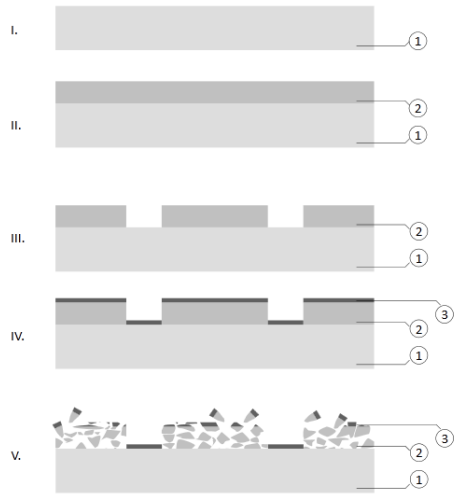
$$\tau = 350 * 0.39 * 9.11x10^{-31} * 10^{-4} / 1.6x10^{-19} = 7.7719x10^{-14} \text{ secs.}$$ (3)

2b) While there may be specific device and materials issues in certain cases, we can identify at least two key generic differences between the techniques

- MBE layers can be grown at *lower temperatures* than for MOCVD
- MBE is not limited by precursor decomposition kinetics

- MOCVD employs a *simpler technology* than MBE
- MOCVD does not require advanced DRV technology
- but, MOCVD does need substantial toxic gas handling facilities. (3)

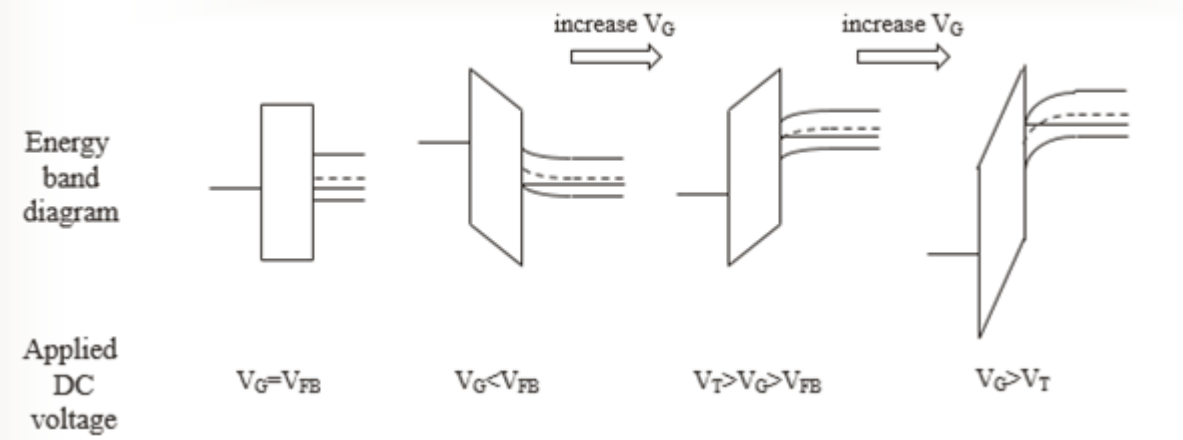
2c)



(4)

The lift off technique consists of depositing a PhotoResist (2) on a substrate (1), the PR is developed to show regions where the metal (3) is required. Metal is deposited on the entire wafer, and the PR is etched off, taking metal on the top along with it. This only leaves the metal in the desired locations. (2)

2d.



(5, 1 each diagram)

Threshold voltage is defined as the voltage where the band bending at the surface equals the difference between the intrinsic level and the fermi level in the bulk. (1)

3a.

Ion implantation is employed because it offers *advantages* over simple dopant diffusion into a semiconductor: in particular it gives

very accurately controlled doping concentrations

tightly controlled depth distributions

high reproducibility. *(1)*

Ion Implantation Apparatus

i)The dopant is initially produced in the form of a gas (from a cylinder) or a vapour (from a heated solid or liquid) The gas or vapour is ionised by an electron beam to give ***positive ions.*** ***(1)***

ii) The ***bending magnet*** provides ***mass analysis*** for e.g. isotope separation. Ions of the selected mass emerge through a resolving aperture and are ***accelerated*** further to the desired energy. (1)

iii)the ion dose can be ***calibrated*** by use of a Faraday cage monitor (1)

Range and Projected Range. An ion passing through a lattice traverses a total path length (R) called the range

However, the important parameter is the mean distance that ions of a given type travel normal to the surface: the projected range (R_p) (1)

Channeling: ions incident along a low index crystallographic direction channel down the lattice holes making correlated glancing collisions they penetrate larger distances by such channeling.

Channeling is prevented by preamorphisation dose or tilting the wafer along a non crystallographic direction. ***(1)***

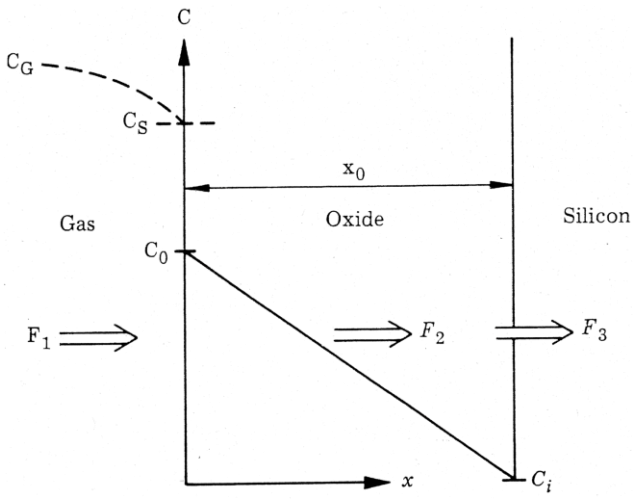
3b). Calculation of time for layer regrowth:
i) velocity = v0[exp(-EA/kT)]
= 3.68×10^{8} [exp(-2.76/8.61x10^{-5}x873)]
= $3.68 \times 10^{8} \times 1.130 \times 10^{-16}$ cm/s
= 4.28×10^{-8}cm/s
ii) time required to regrow 1.5×10^{-5}cm:
= $1.5 \times 10^{-5} / 4.28 \times 10^{-8}$s
= 350s (5)

3c. oxidation with dry oxygen gas (dry oxidation)

$$Si + O_2 = Si0_2$$ (1)

oxidation with steam (wet oxidation) - a faster process

$$Si + 2H_2O = Si0_2 + 2H_2$$ (1)



(1)

The reaction kinetics involves ***three steps*** in the oxidation process; the oxidising species is ***transported*** from the bulk of the gas to the oxide/ gas interface

flux = h_G (C_G - C_S) [h_G is mass transfer coefficient]

The oxidising species diffuses across the oxide layer already present

flux = D (C_o - C_i)/Xo [D is the diffusivity in oxide]

The oxidising species reacts with the **Si** at the oxide/**Si** interface

flux = $k_s C_j$ [ks is reaction rate constant]. (2)

High concentrations of **B** or **P** in the **Si** cause both the linear and parabolic reaction rates to *increase,* probably by different mechanisms

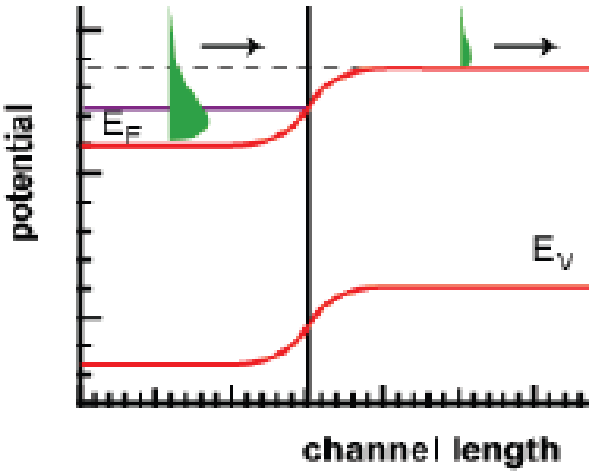
Presence of **HCl** (giving **Cl_2** by reaction **$2HCl + 1/2O_2 = H_2O + Cl_2$**) also *increases* the reaction rates (1)

Q3d. ThE LEC technique is used for III-V compounds. Standard CZ method cannot be used due to high vapour pressure of GrV. In practice, a layer of molten boric oxide (B_2O_3) is floated across the top of the melt in the crucible (typically BN).This seals the melt against loss of Group V material.

It is still necessary to carry out the procedure in a pressure vessel in order to apply a high pressure of gas to balance the Group V vapour pressure under the boric oxide.

But this can now be done in an **inert gas** such as argon (much safer)! (4)

Q4a.In subthreshold region: Diffusion limited current. $D_n=\mu_n V_{thermal}$.Tail end of Boltzmann Distribution can overcome the source barrier (1)



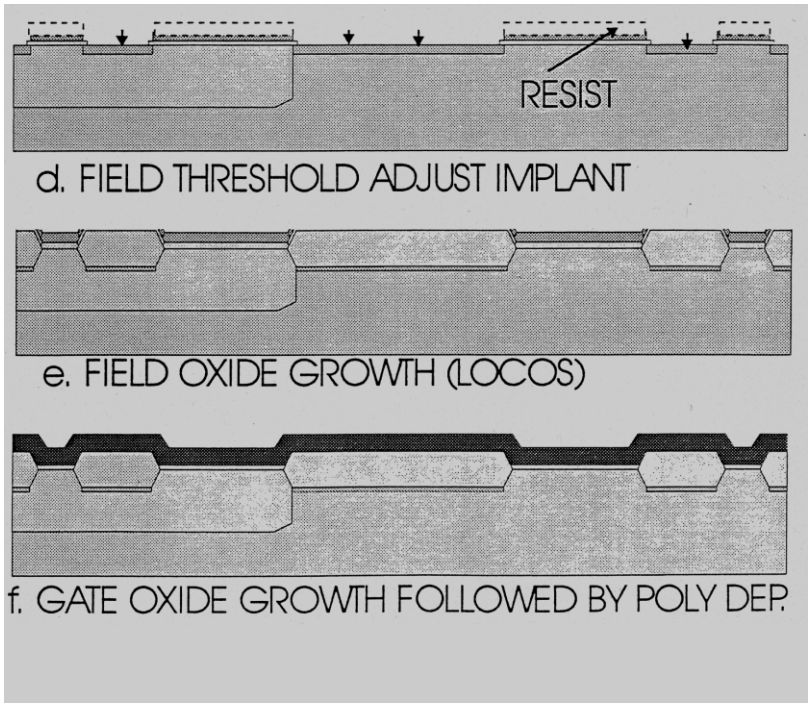
(1)

$$Smin = \frac{kT}{q} ln10$$

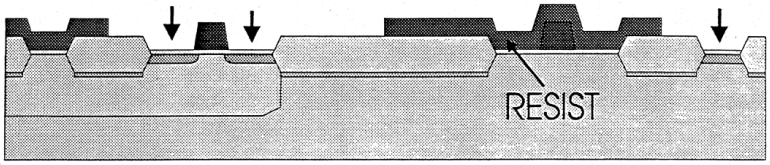
(optional)

S=60mV/decade (1)

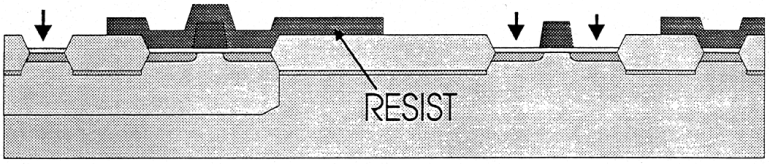
Q4b. Conventional CMOS process as outlined.



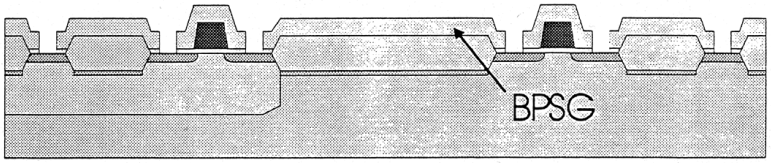
g. POLY PATTERNING & ETCHING



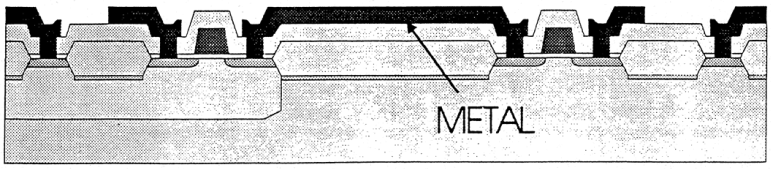
h. RESIST MASK FOR P+ SOURCE & DRAIN IMPLANT



i. RESIST MASK FOR N+ SOURCE & DRAIN IMPLANT



j. .BPSG DEPOSITION & CONTACT WINDOW ETCH



k. METAL DEPOSITION AND ETCH

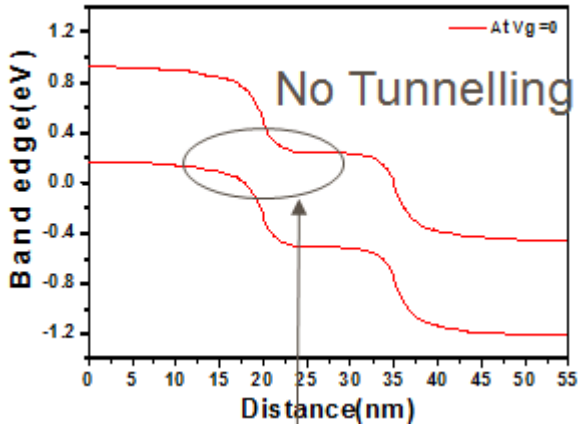
N Well implant and drive in; Oxide/nitride masking layers for LOCOS; oxide nitride patterning, field threshold adjust implant, field oxide growth (locos);gate oxide growth and poly deposition ;poly patterning and etching;resist mask and p+ source and drain implants (B),resist mask and n+ source and drain implants (As);BPSG deposition and contact window mask and etch, metal deposition and etch.

(i) LOCOS thick oxidation layer for isolation.
(ii) Threshold adjust field implant to raise the threshold of parasitic MOS devices, across the field oxide, so that they will not become active during IC operation
(iii) Self aligned process: Source/drain implanted to gate as mask, no additional mask.

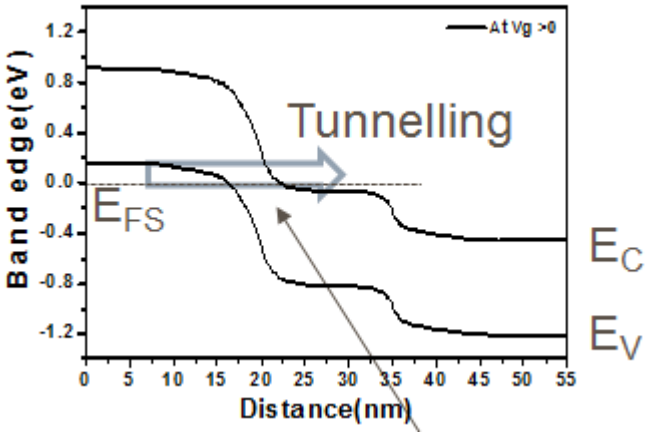
(10)- ***of which 3 marks for getting the sequence correct, 3 marks for diagrams and 4 for content, 1 each question right.***

Q4d. In a Tunnel FET the n+ drain is converted to a p+. Device operates in the subthreshold region via tunnelling current between the source and drain. Channel conduction band is forced

below the source valence band in the on state facilitating direct tunnelling as per the band diagrams shown below. (3)



OFF state. (1)



ON state. (1)