Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2009-2010 (2 hours)

Introduction to VLSI Design 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. The three-input CMOS logic circuit shown in **Figure 1** is incomplete:

i) Draw *both* of the possible complete circuits that could be formed by adding transistors (you cannot cut any of the existing wires); **(8)**

ii) Write down their logical functions; **(6)**

iii) Size the transistors for each of the circuits (as multiples of the width of a minimum-size N-type FET) assuming a minimum sized gates (using the normal assumptions). **(6)**

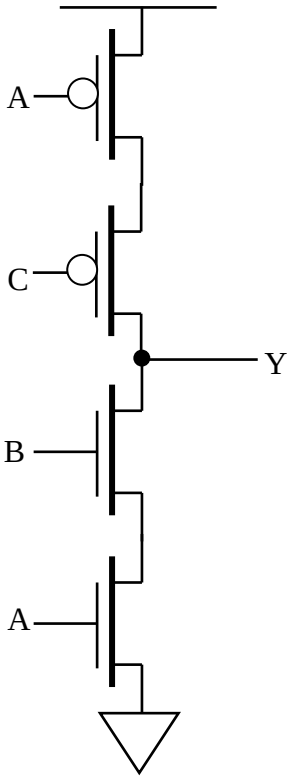

Figure 1: Incomplete Logic Circuit

2. **a.** Distinguish between static and dynamic power dissipation in circuits. **(4)**

b. One of the major sources of dynamic power dissipation in CMOS circuits is due to switched capacitance.

i) Develop an expression to show what the power dissipated in a CMOS circuit due to switched capacitance should be (ensure that you define all terms and state assumptions). **(4)**

ii) Why has reducing the power supply voltage traditionally been the best way to reduce power consumption in CMOS circuits and why is this not likely to be the case in the future? **(2)**

c. A 2-input standard-CMOS, minimum-sized NAND gate is part of a clocked circuit and has the following attributes:

- Gate capacitance of minimum-sized *n*-FET = 2fF;
- The inputs are essentially independent of each other and each *changes state* with a probability of 0.25 at each rising edge of the clock;
- The system clock is 1GHz;
- The power supply voltage is 1.2V;
- The output of the gate drives a 10fF load.

Estimate the power dissipation associated with the NAND gate. **(10)**

3. **a.** **i)** As ICs are scaled down in size what is the particular problem that interconnect presents? **(4)**

ii) How is the problem due to interconnect normally managed? **(4)**

b. Why might a logic gate within an IC be required to drive a large capacitance? **(2)**

c. How is driving a large capacitance in an IC normally accomplished? **(6)**

d. A signal, inside an IC, is to be used to optimally drive a load of 18pF (i.e. with minimum delay). You know that a minimum-sized inverting buffer has an input capacitance of 6fF and an area 0.2μm x 1.5μm. Design a set of inverting buffers to drive this load. You need to identify the width of the intermediate buffers as a multiple of the width of the minimum-sized inverting buffer and the area occupied by the set of buffers. **(4)**

4. The circuit shown in **Figure 4** is not a standard CMOS circuit but is from a logic family called Domino Logic.

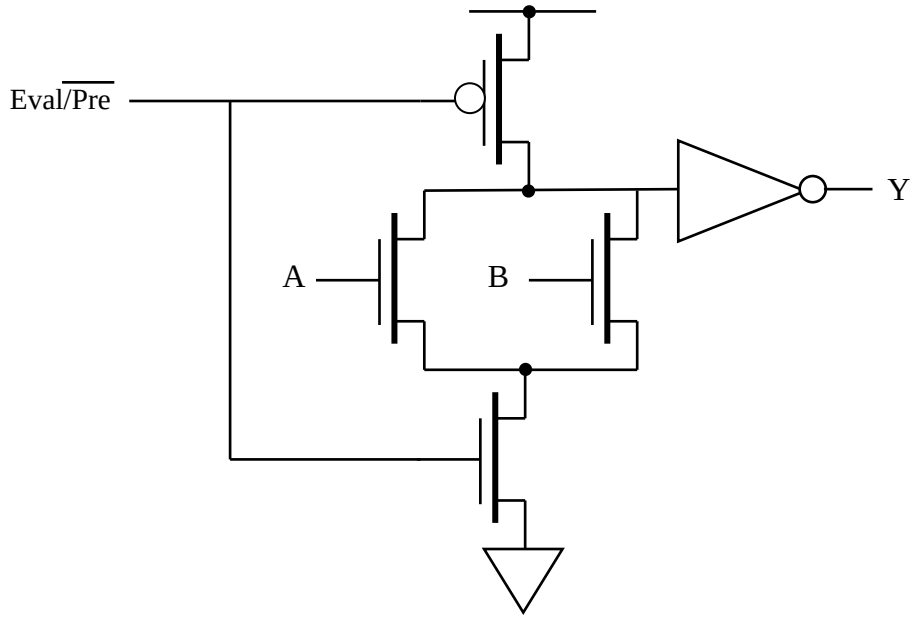

Figure 4: Domino Logic Circuit

The logical output is only valid (the *evaluated* value) when the Eval/$\overline{\text{Pre}}$ input is 1 (Evaluate) and the Eval/$\overline{\text{Pre}}$ input must go low (Precharge) between evaluations. You can assume that the A and B inputs are driven from the outputs of other Domino Logic circuits (which will behave similarly) – all of which share a common Eval/$\overline{\text{Pre}}$ signal.

a. **i)** How can you tell that this is not a standard CMOS circuit? **(2)**

ii) What happens to Y during the Precharge period? **(2)**

iii) What does this, in turn, mean about the behaviour of circuit node at the input of the inverter? **(4)**

b. The Pre/$\overline{\text{Eval}}$ input is driven by a regular, clock-like signal, draw waveforms showing the behaviour of the circuit for various *evaluated* values of A and B. Hence determine the function of the circuit in terms of the *evaluated* values of A and B.

(8)

c. What happens when a number of these circuits (with a common Eval/$\overline{\text{Pre}}$ signal) are cascaded together (*Hint: why is the logic family called Domino Logic*). **(4)**

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