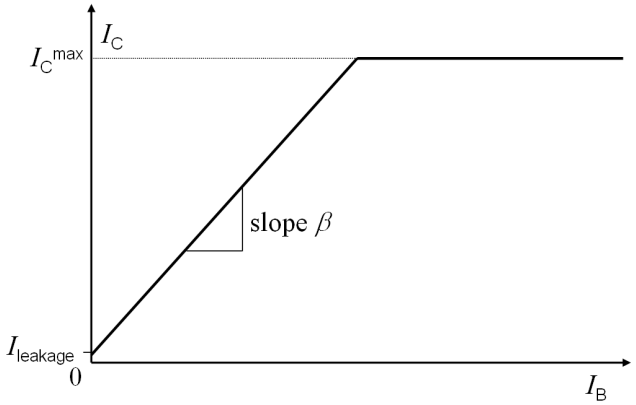
EEE331/6037 exam 2011: exam questions and model solutions

1. single BJT circuits

5 points

a. Sketch the behaviour of collector current versus base current for a bipolar junction transistor (BJT) in common emitter configuration, taking into account both leakage and clipping. Explain the difference between small signal current gain (β) and large signal current gain (h_{FE}) and state when they are identical.

Solution:
The plot of collector current I_C vs. base current I_B is approximately linear over a wide range.
The slope is the small signal current gain $\beta = i_C/i_B = \partial I_C/\partial I_B$.
The offset on the vertical axis (I_C) is the leakage current I_C^{min}, which is usually small, say ≤1μA. For very large base currents I_B, the leakage current may reach a maximum I_C^{max}, at which point the full supply voltage will drop over the resistance connected to the collector. Increasing I_B further will just cut (clip) the output signal, leading to distortion. So the output is a linear function up to that point.
The large signal current gain, h_{FE}, is the ratio of peak currents $h_{FE}=I_C^m/I_B^m$ at any point in the linear range, min<m<max.
When the leakage current is negligible and the I_C (I_B) curve is linear then we have a proportionality and $\beta=h_{FE}$. If leakage is relevant, then $h_{FE}>\beta$ by some small amount. If clipping is reached, h_{FE} decreases but remains finite, while $\beta\approx 0$.



4 points

b. Using the standard Ebers-Moll equation for the collector current of a BJT, derive an expression for its transconductance for given collector current. Comment on its temperature dependence: will it go up or down with temperature, and how much will its relative change be if the BJT heats up from room temperature (20°C) to 80°C?

Solution:
Ebers-Moll equation for collector current: $I_C=I_0\{\exp[qV_{BE}/(kT)]-1\}$
Transconductance is obtained by simple differentiation:
$g_m=\partial I_C/\partial V_{BE}= q/(kT)\, I_0 \exp[qV_{BE}/(kT)] = qI_C/(kT) \propto T^{-1}$
Hence, g_m will decrease with temperature, from room temperature (293K) to 80°C (353K) by about 17% if I_C=constant (i.e. V_{BE}/kT is assumed to be kept constant).

8 points

c. (i) Name the transistor circuit shown in Figure 1.
(ii) Explain the functions of all resistors and capacitors marked.
(iii) Calculate the voltage gain.
(iv) Draw a small signal equivalent circuit that would be appropriate for high-frequency signals. Neglect emitter capacitance but take the Miller effect into account.
(v) Calculate approximate transition frequencies for input and output side.
(vi) Which will dominate for large voltage gains?

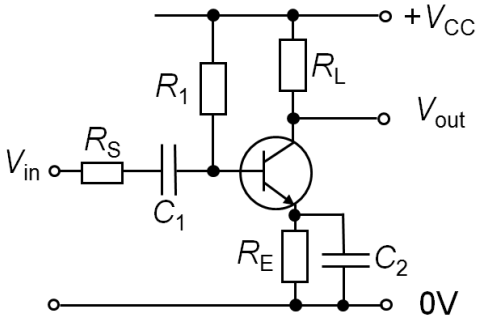
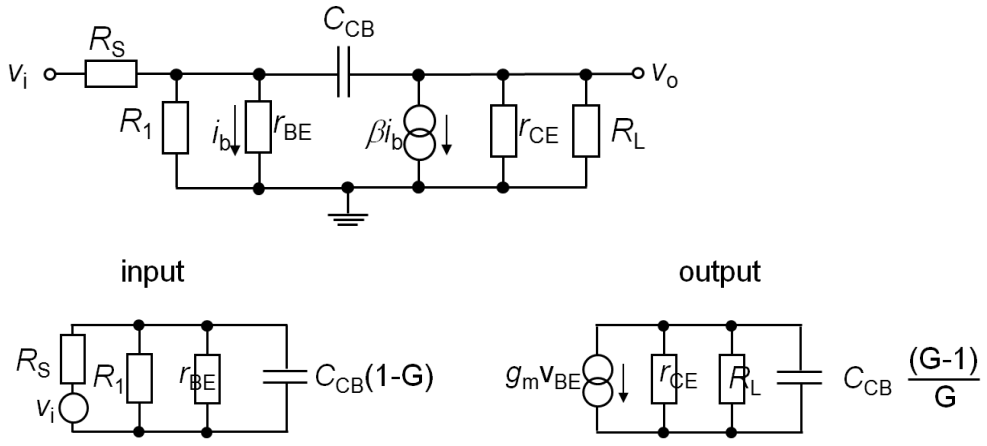


Figure 1

Solution:
(i) This is a common emitter setup with emitter generation.
(ii) R_S is a signal resistor to limit current into the base, R_1 a bias resistor, R_E provides emitter generation and R_L serves as load. C_1 couples the signal in, blocking DC and thus retaining the bias, C_2 shortens R_E for high frequency signals.
(iii)
This is actually a tricky part, as it will depend on a number of approximations.
The approximate small signal voltage gain for a simple common emitter without any signal degeneration (R_E=0), bias (R_1=∞), signal resistor (R_S=0) and C_1 or C_2 is
$G = v_o/v_i = -g_m v_{BE} R_L/v_{BE} = -g_m R_L$
This answer would have been OK if all implicit approximations have been properly stated!
With all these additional resistors (but still without C_1 & C_2) it gets much messier:
$v_o = -\beta i_B [R_L || (R_E+r_{CE}))$
For v_i you can either conisder a voltage divider where
$v_i=v_{BE}\{R_S+[R_1 || (R_E+r_{BE})]\}/[R_1 || (R_E+r_{BE})]$
or consider the potential v_b at the point between C_1,R_1 and the transistor base:
$v_b = i_B r_{BE}+(\beta+1)i_B R_E$
where the base current splits into a horizontal component i_x towards the input and i_y towards R_1 and the supply rail:
$i_B=i_x+i_y$ where $i_x=(v_{in}-v_b)/R_S$ and $i_y=v_b/R_1$.
Inserrtig both into the above and using $v_{BE}=i_b r_{BE}$ gives
$i_B=[v_{in}-v_{BE}-(\beta+1)i_B R_E]/R_S+[v_{BE}+(\beta+1)i_B R_E]/R_1$
This can be solved for $v_i=i_B R_S+[v_{BE}+(\beta+1)i_B R_E][1-R_S/R_1]$, thus
$G = v_o/v_i = -\beta i_B [R_L || (R_E+r_{CE})) / \{i_B R_S+[v_{BE}+(\beta+1)i_B R_E][1-R_S/R_1]$.
(iv)
A small signal circuit for high frequency signals can omit C_1 and C_2 as they are effectively short-cut, but needs to consider C_{CB}, which connects both input and output side and therefore is Miller-magnified on the input side.



(v)
The transition frequencies are thus given by
$f_{t,in}=1/\{2\pi\,[R_S+(R_1||\,r_{BE})][C_{CB}(1-G)]\}$ and
$f_{t,out}=1/\{2\pi\,(R_L||\,r_{CE})\,[C_{CB}(G-1)/G]\}$
(vi)
For large negative values of G we get $f_{t,in}<<f_{t,out}$, so the input side is limiting the transfer at high frequencies.

3 points

d. Explain the different bias settings of class B and class C amplifiers using appropriate diagrams. Compare qualitatively the differences with respect to distortion, sensitivity, maximum voltage swing at input and power consumption.

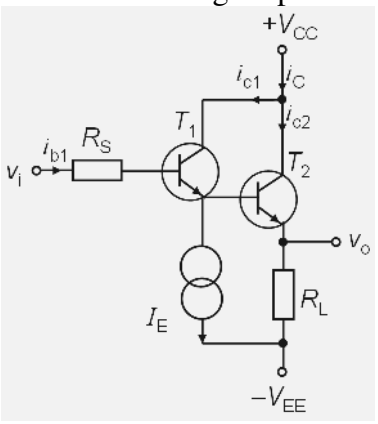
Solution:
Class B is unbiased and only switches on if base voltage > v_{BEon} whereas class C is reverse-biased so that it will only switch on for voltage pulses $>v_{BEon}+|\,v_{bias}\,|$. Class C will thus have very strong distortion, will stay switched off for small input voltages and thus be very insensitive, but it can cope with a larger maximum voltage swing at the input without going into saturation and also consumes very little energy (as it mostly remains switched off).

2. Multiple BJT circuits

5 points

a. Sketch the circuit for a Darlington pair of two different transistors T_1 and T_2 with signal resistor R_S at T_1 and load resistor R_L at T_2. Determine the voltage gain under the approximation that both small signal current gains β_1 and β_2 are >>1. Explain which of the transistors influences the voltage gain more strongly.

Solution:
Sketch of Darlington pair:



Consider for a base current I_B flowing into T1 the output/input voltages at short circuited inputs/outputs. The base current is amplified by a factor (β_1+1) at the emitter of T1 and by another factor (β_2+1) at the emitter of T2. Hence:

$v_o=(\beta_1+1)(\beta_2+1)i_B R_L$

$v_i= R_S i_B + (\beta_1+1)i_B r_{BE1} + (\beta_1+1)(\beta_2+1) (r_{BE2}+R_L) i_B$

The voltage gain then is the ratio

$v_o/v_i=(\beta_1+1)(\beta_2+1)R_L / [R_S + (\beta_1+1) r_{BE1} + (\beta_1+1)(\beta_2+1) (r_{BE2}+R_L)]$

$=R_L / [R_L+ r_{BE2} + r_{BE1}/(\beta_2+1) +R_S/\{(\beta_1+1)(\beta_2+1)\}]$

$\approx R_L / [R_L+ r_{BE2}]$

for β_1, β_2 >>1.

So, only the base-emitter resistance of the second transistor T2 is relevant.

6 points

b. (i) Calculate for the Wilson current mirror shown in Figure 2 the ratio of output to input current for the general case that all three transistors have different small signal current gains of β_i, i=1,2,3. Assume the base currents to transistors T_1 and T_2 at point B are equal. Neglect the Early effect.

(ii) Which transistor has the least effect on the current ratio and why?

(iii) Show that for that case that all transistors are identical ($\beta_1=\beta_2=\beta_3=\beta$) and β>>1 the result approximates to $1/(1+2/\beta^2)$.

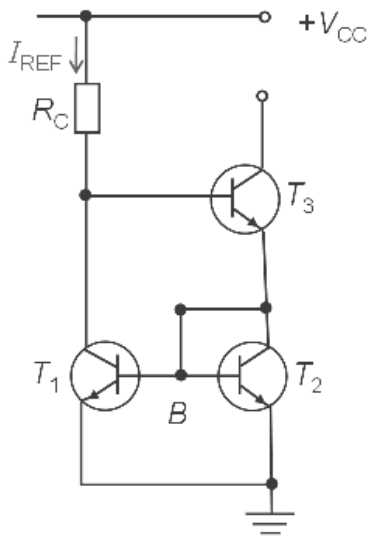


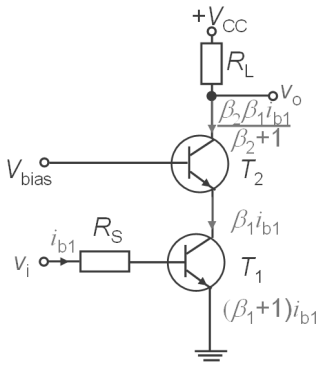
Figure 2

Solution:
If the small signal current gains are different, then, starting at the midpoint between T1 and T2, the base currents into T_1 and T_2 are I_B. Hence, $2I_B$ flows to the midpoint of T2 and T3 where it unites with the collector current from T2, $\beta_2 I_B$, to flow into the emitter of T3. T3 then transfers the fraction $\beta_3/(\beta_3+1)$ of this sum to its collector, which acts as output, so:
(i) $I_{out}=(2I_B+\beta_2 I_B)\beta_3/(\beta_3+1)$
The input is the sum of the collector current of T1, $\beta_1 I_B$, and the base current transferred from T3, which is $(2I_B+\beta_2 I_B)/(\beta_3+1)$, hence:
(ii) $I_{in}= \beta_1 I_B+(2I_B+\beta_2 I_B)/(\beta_3+1)$
The ratio is thus
(iii) $I_{out}/I_{in}=[(2+\beta_2)\beta_3/(\beta_3+1)]/[(\beta_1+(2+\beta_2)/(\beta_3+1)]=(\beta_2\beta_3+2\beta_3)/(\beta_1\beta_3+\beta_1+\beta_2+2)$
From this we can conclude:
(iv) β_3 is the only parameter that shows up in the products dominating both numerator and denominator; so that a change of β_3 almost cancels out. Hence, T3 is least critical.
(v) This is clear as T_1 is directly connected to the input, so a change of β_1 by some % reduces I_{in} via the first term in (i) by an almost similar fraction. T_3 is directly connected to the output, but only passes the current from T_2 through its emitter to its collector.
(vi) For $\beta_1=\beta_2=\beta_3=\beta$ we get
$I_{out}/I_{in}=(\beta^2+2\beta)/(\beta^2+2\beta+2)=1/[1+2/(\beta(\beta+2))]\approx 1/(1+2/\beta^2)$
where the approximation is for $\beta>>1$.

3 points

c. Sketch the circuit for a cascode pair with BJTs, including input and output voltage connections. Derive the small signal expression for its current gain and compare this to a single BJT in common emitter configuration.

Solution:



R_S in the sketch was not required. The output current is:
$i_o=i_{C2}=\beta_2\beta_1 i_{b1}/(\beta_2+1)\approx\beta_1 i_{b1}$, hence current gain:
$i_o/i_{b1}=\beta_2\beta_1/(\beta_2+1)\approx\beta_1$ is rather small and very similar to that of T_1 alone.

6 points

d. Identify the type, function and configuration of the BJTs in figure 3, state the classes of both amplifiers and draw a sketch of their characteristics. Which will have the smoother transfer characteristic?

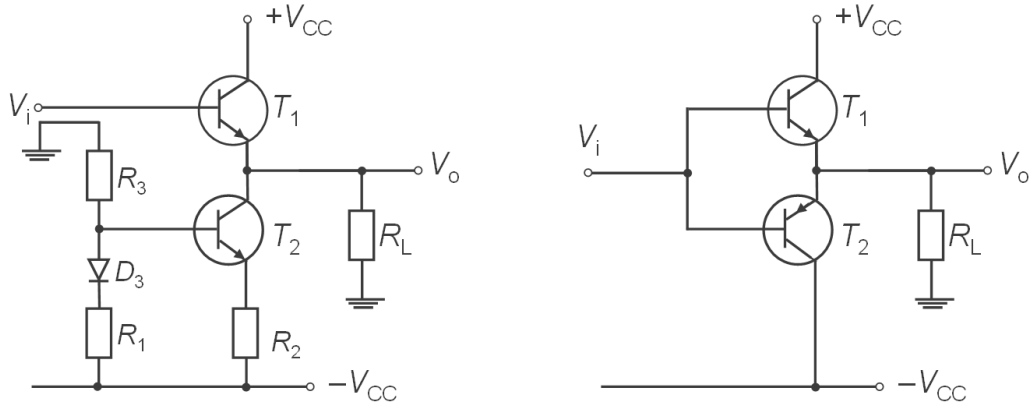
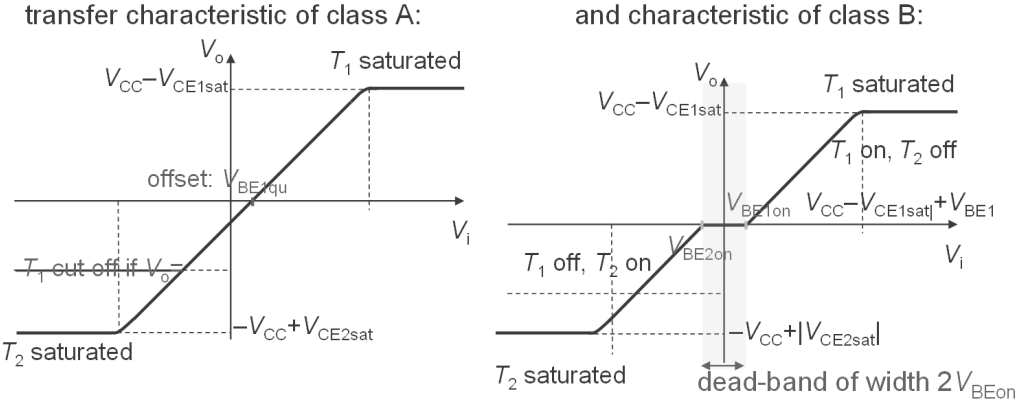


Figure 3

Solution:
The left cicuit shows two identical (npn) BJTs, with T_1 in emitter follower configuration and T_2 supplying the quiescent current for biasing. The pair is a typical class A output stage. The right circuit shows a complementary pair (one pnp and one npn BJT) in push-pull configuration. Because of the lack of any bias, this is a class B output stage. The output characteristic curves look like this:



Obviously, class A (left) has the better transfer characteristic, class B suffers from severe cross-over distortions due to the dead band of width $2V_{BEon}$. V_{CEsat} labels are not required.

3. MOSFETs

6 points

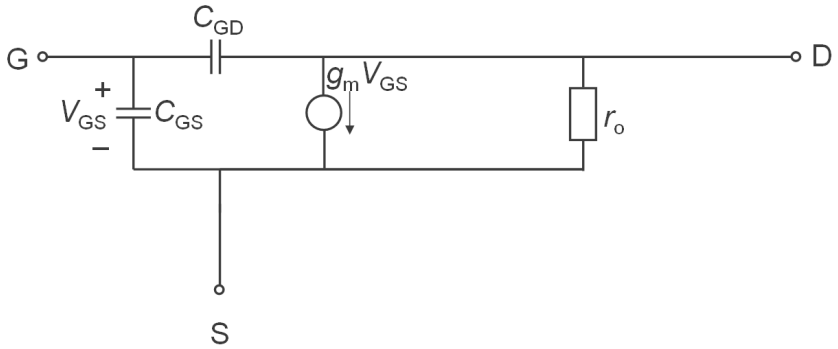
a. (i) Sketch the small-signal hybrid-π equivalent model of a metal-oxide-semiconductor field effect transistor (MOSFET). Neglect all body or substrate effects.

(ii) Derive an expression for the small signal current gain, assuming for the transconductance $g_m >> \omega C_{GD}$. Use the standard square-model for the drain current and the definition of the transconductance to express the transconductance in terms of drain current i_D and overvoltage V_{ov}.

(iii) Inserting this into the expression for the transition frequency f_t (where gain is unity), show that the result is $f_t = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$.

(iv) What does this mean for the physical design of improved MOSFETs?

solution:



Injecting a test current at the gate: $i_{in} = j\omega(C_{GS}+C_{GD})V_{GS}$

results in an output current at the drain of: $i_{out} = g_m V_{GS} - j\omega C_{GD} V_{GS} \approx g_m V_{GS}$

This gives a short-circuit current gain of: $i_{out} / i_{in} = g_m / [j\omega(C_{GS}+C_{GD})]$

Square-model for drain current: $i_D = \text{const.}\ (V_{GS}-V_{to})^2$

Definition of transconductance: $g_m = \partial i_D/\partial V_{GS} = 2i_D/(V_{GS}-V_{to}) = 2i_D/V_{ov}$

Definition of transition frequency: $f_t = \omega_{|i|\,out=|i|\,in}/(2\pi) = g_m/[2\pi(C_{GS}+C_{GD})]$

Inserting above expression for g_m: $f_t = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$

So, for an improved high-frequency transfer behaviour, we need

i) large drain current i_D

ii) small overdrive voltage V_{ov}

iii) small total capacitances of C_{GS} and C_{GD}

4 points

b. The square law model for the drain current of a MOSFET in the saturation region states $i_D = \frac{1}{2}\,\mu\, C_{ox}\, W/L\, (V_{GS}-V_{to})^2$ where μ is the carrier mobility, C_{ox} the specific oxide capacity per oxide area and W and L are the width and the length of the transistor channel, respectively.

(i) Considering the MOSFET as a plate capacitor of area $A=WL$, calculate the drain current density.

(ii) Explain for given materials which design parameters for the MOSFET layout are important to achieve a high drain current density.

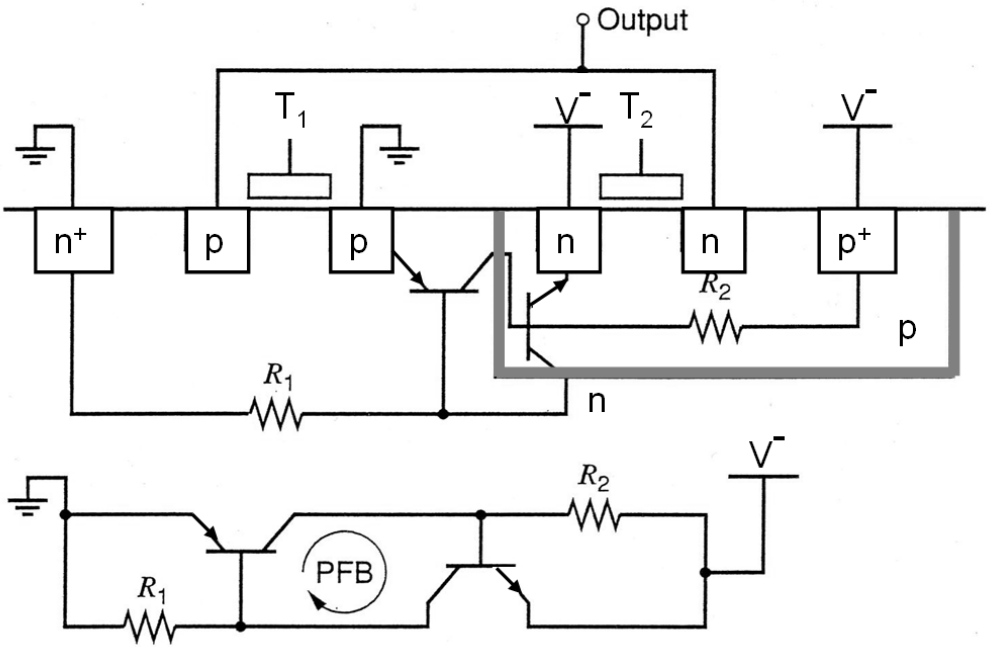
(iii) If you take into account that you cannot increase V_{GS} significantly without risking breakdown due to high electric fields across the gate oxide, which is the most important design parameter?

Solution:
The MOSFET gate works like a plate capacitor whose capacitance is given by $C=\varepsilon_0\varepsilon A/t$ where ε_0 = electric field constant, ε = relative dielectric constant, A = area and t = distance between electrodes (= oxide thickness). This means $C_{ox}=C/A=\varepsilon_0\varepsilon/t$ and hence we get: $i_D = ½\ \varepsilon_0\ \varepsilon\ \mu W\ (V_{GS}-V_{to})^2/(tL)$
This gives for the current density: $j_D = i_D/A = ½\ \varepsilon_0\ \varepsilon\ \mu\ (V_{GS}-V_{to})^2/(tL^2)$
ε, μ and V_{to} are materials properties to be assumed fix.
V_{GS} is limited by gate oxide break-down as stated in the text. So j_D can only be maximised by design by reducing the product (tL^2) in the denominator, where the channel length L has the strongest influence: the transistor has to be made shorter.

7 points

c. Sketch the phenomenon of latch-up for a complementary pair of a p-channel MOSFET T_1 and an n-channel MOSFET T_2 that are fabricated on the same n-doped substrate. Explain what latch-up is, why it occurs and what the consequences can be. Explain the benefit of a dielectric with low dielectric constant to encapsulate T_2.

Solution:
To make the n-channel MOSFET a p-doped region needs to be created first into which the n-doped source and drain regions can then be fabricated. This means a number of p- and n-doped regions co-exist next to each other that can interact. In particular, two parasitic BJTs will be formed at the boundary of the two MOSFETs, a lateral pnp BJT (between drain of p-channel, n-substrate and p-region encapsulating the n-channel MOSFET) and a vertical npn (between the source of the n-channel MOSFET, its p-channel surrounding and the n-substrate=body). These can interact and create a positive feedback where one BJT drives the other. If they enter the active region and start to conduct, the resulting high current will heat up and destroy the circuit.



Including a high-k dielectric to encapsulate T_2 (thick grey line) will effectively isolate T_1 and T_2, creating almost infinite resistance, and so reduce the damaging

currents, and it will also minimise the capacitance of the plate capacitor formed by p- and n-doped regions either side.

3 points

d. Consider an active loaded MOSFET differential amplifier with two matched transistors T_1 and T_2 with the following technical specifications: W/L=200, μC_{ox}=0.2mA/V^2, V_{SS}=12V, I=0.4mA, R_{SS}=20kΩ. Calculate overdrive voltage V_{ov}, conductance G_m, output resistance R_0, differential mode gain A_{dm}, common mode gain A_{cm} and common mode rejection ratio (CMRR) in dB.

Solution:
The total current flowing consists of the sum of both drain currents, i.e. $I=i_{D1}+i_{D2}=2\langle i_D\rangle$ where the brackets denote time averaging and the individual currents at drains 1[2] are given by $i_{D1[2]} = I/2 \pm I/V_{ov}\, v_i^{diff}/2$.
The overdrive voltage is $V_{ov} = [I/(\mu C_{ox}\, W/L)]^{½} = 0.1\text{V}$.
The conductance thus is $G_m = I/V_{ov}$ =0.4mA/0.1V = 4mA/V.
The output resistance is $R_o = V_{SS}/I$ = 12V/0.4mA = 30kΩ.
The differential mode gain is $A_d = G_m R_o$ = 4mA/V × 30kΩ = 120.
The common mode gain is $A_{cm} = 1/(2G_m R_{SS})$ = 0.00625
The CMRR is then = A_d/A_{cm} = 19200, which corresponds to 85.7dB.

4. Filters

6 points

a. Name the order and type of filter shown in Figure 4. Justify qualitatively its frequency behaviour. Derive its corresponding leap-frog structure. Write down the equations for all components.

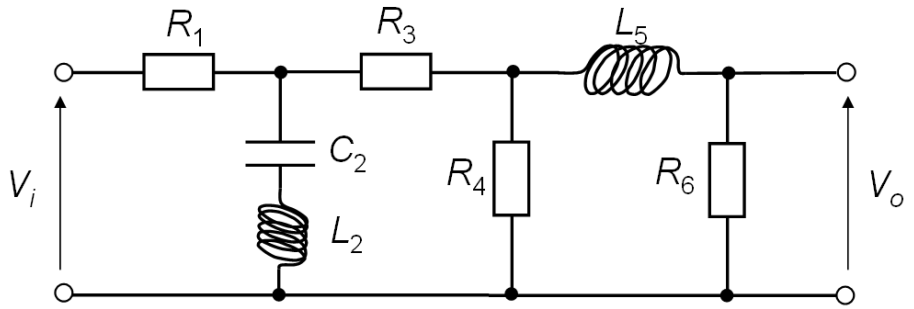
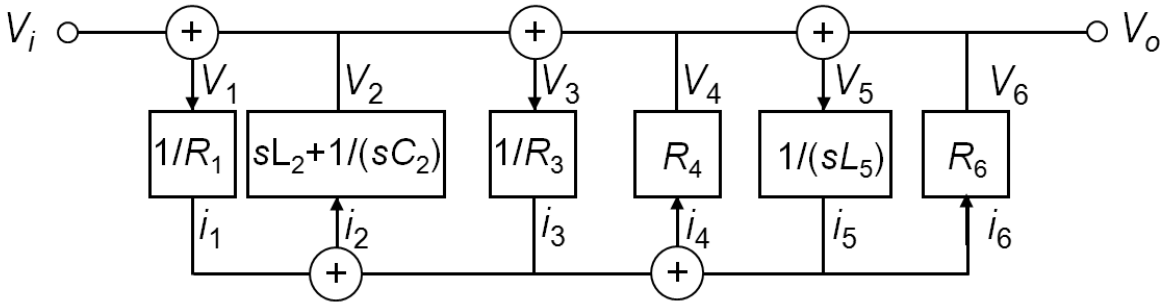


Figure 4

Solution:
The filter is a 3rd order LC low pass filter. It acts as low pass because C_2 effectively blocks DC signals which R_1, R_3 and L_5 then transfer to the output, while high-frequency signals are blocked by L_2 and L_5 and then transfer to ground via the ohmic resistances. Medium frequencies in-between can pass L_5 and the L_2C_2 combination and are thus partly shortened to ground, partly transferred. Another way of explanation would be that the left part (R_1, C_2 and L_2) forms a classical 2nd order band stop and the right part (L_5, R_6) a typical 1st order low-pass filter. The multiplication of both results in a skewed low pass filter.
The leap-frog structure would look like the following:



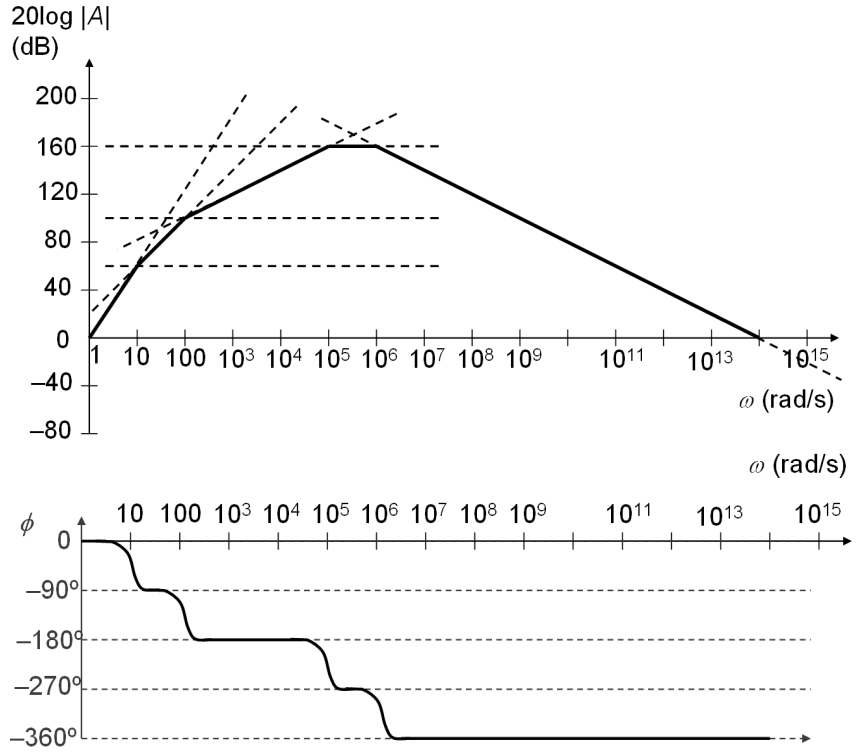
With input and output resistors there are 6 components, if C_2 and L_2 are considered together. For each of them we can write down two equations, one from Ohm's Law and one from Kirchhoff's Law. Hence, there are 12 equations to describe the interdependence of 6 voltages $V_{1\text{-}6}$ (V_i and $s=j\omega$ are given) and six currents $I_{1\text{-}6}$. So it is possible to calculate step by step the output voltage $V_o=V_6$ for any given set of V_i and ω.
(i) $I_1=V_1/R_1$; $V_1=V_2-V_i$
(ii) $V_2=I_2\,[sL_2+1/(sC_2)]$; $I_2=I_3-I_1$
(iii) $I_3=V_3/R_3$; $V_3=V_4-V_2$
(iv) $V_4=I_4R_4$; $I_4=I_5-I_3$
(v) $I_5=V_5/(sL_5)$; $V_5=V_6-V_4$
(vi) $V_6=I_6R_6$; $I_6=I_5$

8 points

b. Find the zeros and poles and sketch the Bode plot of the magnitude and phase of the transfer function $T(s) = s^3/[(1+s/10)(1+s/10^2)(1+s/10^5)(1+s/10^6)]$. Name the

order and the type of the filter. What is the transition frequency of unity gain? Considering both gain and phase margins, state over which frequency range this transfer function would be stable and whether it would be a good high-frequency amplifier.

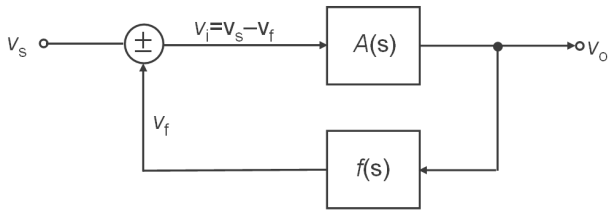
Solution:
zeros: s=0 and s=∞
poles: s=−10, s= -10^2, s= -10^5 and s= -10^6
The Bode plot of the amplitude can be obtained from the multiplicative superposition of four curves for
(i) $T(s)$= s^3, which is a straight line through (1rad/s, 0db) with a steep slope of +60dB/decade.
(ii) $T(s)$=1/(1+s/10^1) gives a line of slope −20dB/decade intersecting at ω=10, thereby reducing the slope from ω=10 onwards to +40dB/decade.
(iii)$T(s)$=1/(1+s/10^2) gives a line of slope −20dB/decade intersecting at ω=10^2, thereby reducing the slope from ω=10^2 onwards to +20dB/decade.
(iv)$T(s)$=1/(1+s/10^5) gives a line of slope −20dB/decade intersecting at ω=10^5, eliminating the slope from ω=10^5 onwards.
(v) $T(s)$=1/(1+s/10^6) gives a line of slope −20dB/decade intersecting at ω=10^6, The gain thus approaches unity at ω=10^{14}.
This is a 4th order band-pass filter.
The transition frequency with unity gain is f_t=10^{14} s^{-1}/(2π)= 15.9 THz.
Stability means both, a significant gain margin (A>10dB) and a significant phase margin (ϕ>−180°+45°), so that the amplifier does not produce noise and does not become instable due to feedback. The latter criterion is here only valid for very low frequencies, below f=16Hz, so this amplifier would be highly instable at high frequencies.



6 points

c. Sketch a block diagram of a non-inverting voltage amplifier with frequency-dependent amplification factor $A(s)$ and feedback $F(s)$. Calculate
(i) the loop gain,
(ii) the voltage gain,
(iii) the de-sensitivity factor.
Show from this for a single-pole amplifier with mid-band gain A_m, where $A(s)=A_m / (1+s/\omega_t)$ for a pole frequency ω_t and frequency-independent feedback F that the product of gain and bandwidth is constant. Explain this using a simple Bode plot.

Solution:



signal: v_s
input: $v_i=v_s-v_f$
output: $v_o=A(s)\,v_i$
feedback: $v_f=f(s)v_o$
loop gain: Af
total gain: $A/(1+Af)$

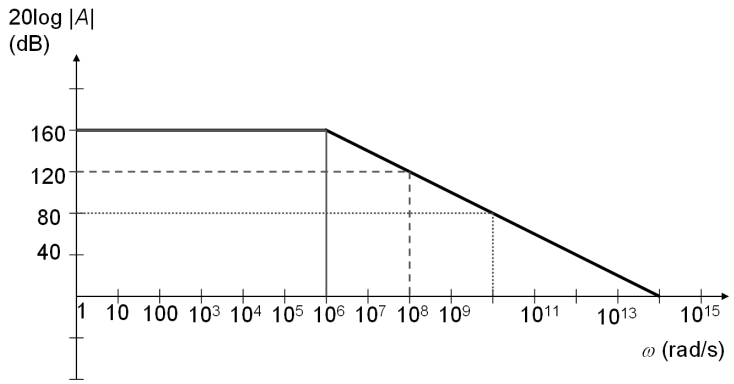
where $f=F$=feedback

(i) The loop gain is defined as the product $A(s)F(s)$.
(ii) The total voltage gain is $G=v_o/v_s$ where $v_s=v_i+v_f=v_o/A+v_oF=v_o(1+AF)/A$, hence $G=A/(1+AF)$
(iii) From above: $dG/dA=[1+AF-A(F+A\,dF/dA)]/(1+AF)^2=1/(1+AF)^2$ for const. F, hence $dG/G= 1/(1+AF)\,dA/A$ where the factor in the denominator is the de-sensitivity factor, which describes how much relative change in total gain G one gets for a given relative chance of the amplification factor A.

For $A(s)=A_m / (1+s/\omega_t)$ insertion into (ii) yields

$$G(s)=A(s)/[1+A(s)F]$$
$$=A_m/\{[1+s/\omega_t]\,[1+FA_m/(1+s/\omega_t)]\}$$
$$=A_m/[1+s/\omega_t+FA_m]$$
$$=A_m/[1+FA_m]\times 1/\{1+s/[\omega_t(1+FA_m)]\}$$

The gain in the first term is reduced by a factor of $(1+AF)$, while the new pole frequency is multiplied by the same factor, i.e. the product of gain and bandwidth stays constant. In the graph this means the 3 rectangles (solid, dashed, dotted) all cover the same area. Reducing the gain by e.g. 40dB (i.e. a factor 100) extends the bandwidth by a factor of 100.


20log |A|
(dB)
160
120
80
40
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^11
10^13
10^15
ω (rad/s)