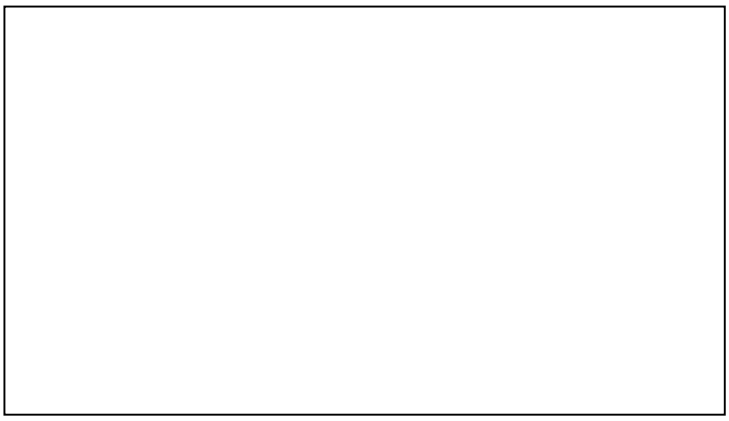
EEE105 - Electronic Devices
Lecture 18

Depletion Mode MOSFET

In the last lecture the operation of a so-called enhancement mode MOSFET was described, where a channel is created, and its conductance enhanced by application of a positive bias on the gate (to form an n-channel). It is possible to also fabricate an n-channel MOSFET with a pre-existing channel.

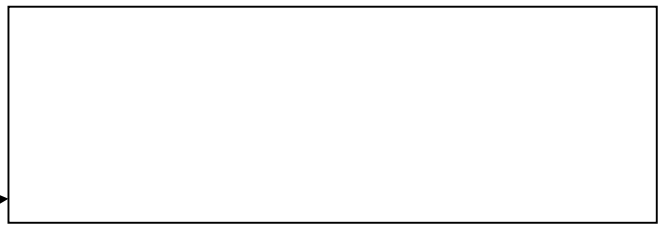
In this case we diffuse in the two n^+ contact regions for the source and drain, but then also diffuse in another thin n-type region between them before creating the insulating oxide and placing the metal contacts on the device.



As the drain voltage is increased the channel will again become triangular in shape and the current will saturate when pinch-off of the channel is achieved near the drain end of the device.

In this case we can apply a negative bias to the gate to ***deplete*** the electrons out of the channel and hence reduce the channel conductance. Thus a negative gate bias is required to reduce conduction from a *"normally-on"* state.

The circuit symbol for the depletion mode MOSFET is:



MOSFET Circuit Properties.

The circuit properties of the MOSFET are very similar to those for a JFET. For example the transconductance is identical and is given by the equation:

The equivalent circuit is also identical. However it should be noted that since the gate is insulated from the channel, the input impedance is extremely high thus the two input resistances will be very large.

FET as an electronic switch

In a switch we want a device to have two states: OPEN and CLOSED

When a switch is open we want the voltage drop to be and the current flow to be

When a switch is closed we want the voltage drop to be and the current flow to be

A common application for the MOSFET is its use as a switch in digital integrated circuits. When the channel conducts freely we have the "on-state" and when it does not conduct the device will be in an "off-state" The state is controlled by the gate bias. The operating points will be as indicated in the figure (one could imagine them being at either end of a load line.)

A key point in any digital circuit is to minimise the power dissipated as this will:

Now the power dissipated will be given by

Thus for the switch we want the voltage drop to be as small as possible in the on-state and the current flow to be a small as possible in the off-state.

In reality most of the heat is produced as transistors switch from the on to the off state. During the switching usually both the current and voltage are significant and hence heat is produced. The more switching operations we perform per second the more heat that will be produced and hence the hotter the transistors in our integrated circuit will be.

Up until now we have discussed only n-channel MOSFETs. It is equally easy to create p-channel MOSFETS, where holes, rather than electrons transport the charge from the source to the drain.

The circuit symbols for p–channel MOSFETs are the same as for n-channel ones, except that the central arrow will point out of the device rather than into it.

Both n-channel and p-channel devices are combined in so-called Complementary MOS (or CMOS) circuits. CMOS has a major benefit in that the power dissipation is very low.

The Bipolar Junction Transistor (BJT)

(CAL: Bjt(a), Bjt(b), Bjt(c))

The bipolar junction is in essence two back-to-back p-n junctions, separated by a very ***THIN*** common region.

npn device (more common)

pnp device

In reality BJTs can be fabricated in a planar geometry. The p- and n-type regions are formed by diffusing or implanting the dopant atoms into the Silicon.

(In diffusion the semiconductor is hearted up in an atmosphere of the dopant atom, whilst in implantation a beam of dopant ions is accelerated into the semiconductor.)

Let us consider the following transistor circuit:

Planar Structure

In this circuit the Base-Emitter junction is

Biased

(this bias voltage is called V_{be})

The Collector Base junction is

biased

(this bias voltage is called V_{cb})

In this npn transistor electrons are injected through the forward biased junction into the base.

The electrons then diffuse across the base towards the collector. However as the diffuse some will electrons will be lost due to

Now let us say that the n-type carrier concentration in the emitter is much higher than the p-type carrier concentration in the base. That is $N_d(\text{emitter}) >> N_a(\text{base})$.

From our discussion of electron and hole currents for a p-n junction we therefore will have the situation in the base-emitter junction that the electron current will be ***much*** ***than*** the hole current due to the equation:

We always design the transistor such that we have almost all the base-emitter current in the form of electrons injected into the base, with as few holes as possible injected from the base into the emitter.

Next, we next need to consider what happens to the electrons in the base. Consider first a:

a. Thick Base "Transistor"

If the base is thick then the electrons will behave in exactly the same way as for an ordinary p-n junction diode:

Electrons will diffuse into the p-type base and recombine as they go. There will be the usual decay with distance into the p-type material characterised by the minority carrier diffusion length.

Few if any of the excess electrons injected into the base reach the reverse biased collector-base junction and hence only a small leakage current will appear at the collector.

In this situation the current appearing at the base terminal of the device (*the base current*), I_B, will be large and the current appearing at the collector terminal (*the collector current*), $I_C \approx 0$.

In this device it is important to note that the width of the base, $W_B >> L_e$

This arrangement is not useful as a transistor.

Next time we will see how, if we make the base much thinner how a transistor characteristic can be produced.

Key Points to Remember:

1. As well as an enhancement mode MOSFET we can also create a device with a pre-existing channel, which then can be reduced by applying a bias to the gate.
    a. This is called a DEPLETION mode MOSFET
2. The equivalent circuit for a MOSFET is identical to a JFET. Usually the input resistances are extremely large though.
3. Transistors can be operated as electrical switches where the input voltage can control if the output current is large or (nearly) zero.
4. One can have both n-channel and p-channel MOSFETS, CMOS is a way to combine these to provide switching with very low power consumption
5. The BJT consists of an emitter and collector of one type, with a base of semiconductor material of the opposite type.
6. We need emitter-base junction to be designed to give injection of minority carriers into the base under forward bias.
7. For a transistor effect we cannot have a base that is very thick.