The University Of Sheffield.

Data Provided:

Boltzmann constant (k_B) = 1.38×10^{-23} m^2 kg s^{-2} K^{-1}

Electronic charge = 1.602×10^{-19} C

Thermal Conductivity: k_{epoxy} = 0.5 $W.m^{-1}.K^{-1}$,

k_{SiN} = $65W.m^{-1}.K^{-1}$, $k_{aluminium}$ = $216W.m^{-1}.K^{-1}$

Permittivity of free space (μ_o)=8.85×10^{-12} m^{-3} kg^{-1} s^4 A^2

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2007-2008 (2 hours)

Microsystem Packaging 6

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Describe the methods of (a) wire bonding, (b) tape automated bonding, and (c) flip chip technology for the connection of circuits to a substrate or direct to a chip package. What are the advantages and disadvantages of these techniques? **(5)**

b. The Intel 80286 microprocessor (made in 1995) had 10^5 gates and operated at 8 MHz. Ten years later the first Intel Pentium (80586) processors had $5x10^6$ gates and operated at 100 MHz.

(i) Assuming Rents rule, with the rent exponent =0.6 and the rent multiplier =0.2, calculate the possible number of I/O terminals for these two packages.

(ii) The 80286 used a plastic leaded chip carrier (PLCC) package, whilst the 80586 used a ceramic pin grid array (PGA) package. The package area is 2 x 2 cm in each case. Estimate the average pin separation for the two types of package.

(iii) Explain the advantages of the PGA and why the material of the package had to be changed.

(iv) The latest Intel Core 2 Quad processors are multichip modules consisting of 2 individual die each with 2 processors. Describe what is meant by a multichip module and why it is used instead of individual packaged processors.

(6)

c. Explain the origins of simultaneous switching noise and crosstalk. Describe how these two issues in electromagnetic interference may be minimised by appropriate packaging design. **(5)**

d. One of the major sources of parasitic impedance introduced by a package is the mutual inductance between leads. The mutual inductance (M) of two conductors is given by:

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{d}+\sqrt{1+\left(\frac{l}{d}\right)^2}\right)-\left(\sqrt{1+\left(\frac{d}{l}\right)^2}\right)+\left(\frac{d}{l}\right)\right]$$

Where l is the conductor length and d the distance between conductors.

(i) A typical Quad flat pack (QFP) package has leads of 6mm length with a separation of 1.2mm. Calculate the mutual inductance between two leads.

(ii) What other sources of parasitic inductance could be introduced by the packaging?

(iii) Describe one modern package which effectively deals with the problem of mutual impedance between leads. **(4)**

2. a. Explain why thermal management is important for packaged integrated circuits. What is responsible for the heat generation? Describe the problems which could result if the temperature is not managed? **(4)**

b. Under typical operating conditions an integrated circuit of dimensions 5 mm x 5 mm, dissipates 25 W. The IC is epoxy mounted to a 3 mm thick silicon nitride substrate, which is then epoxy mounted to a 10 mm thick aluminium heat sink. The epoxy is spread to a thickness of 100 μm.

The maximum allowable on-chip temperature is 90 ^{o}C. Assuming linear heat conduction, what is the maximum allowable temperature on top of the heat sink? What methods could be employed to keep this temperature below the limit? **(6)**

c. Integrated circuits show an average failure rate as a function of time which is typical of semiconductor devices.

(i) Draw a graph of the average failure rate versus time and describe its three main regions.

(ii) Describe the process of ‘burn in’, which could be applied to these devices. What advantages might this have for the manufacturer? **(4)**

d. (i) Describe what is meant by the 'accelerated testing' of semiconductor devices and why is it performed?

(ii) Which typical environmental stresses may we wish to accelerate?

(iii) Describe two common industry standard tests. Briefly describe their measurement conditions. What are they designed to reveal?

(iv) A semiconductor laser device should achieve at least $1x10^5$ hours of reliable operation at its 20 ^oC operating temperature. However only 1000 hours are realistically available for testing. Assuming the failure mechanisms are known to be due to a thermally activated process with a rate of failure given by;

$$R = R_0 \exp(-E_a / k_B T),$$

where R is the rate of failure, E_a the activation energy, k_B is Boltzmann's constant and T the temperature. Assuming that E_a = 0.5 eV, at what temperature should the accelerated testing be performed? **(6)**

3. a. Describe the soldering method by which surface mount components are attached to the top surface of a printed circuit board (PCB). **(8)**

b. The packing density can be increased by mounting components on both side of the PCB. What are the limitations of this approach and how could they be overcome? **(3)**

c. An extra assembly step usually follows the soldering of ball grid array (BGA) packages onto the PCB. Describe this step and explain its purpose. **(3)**

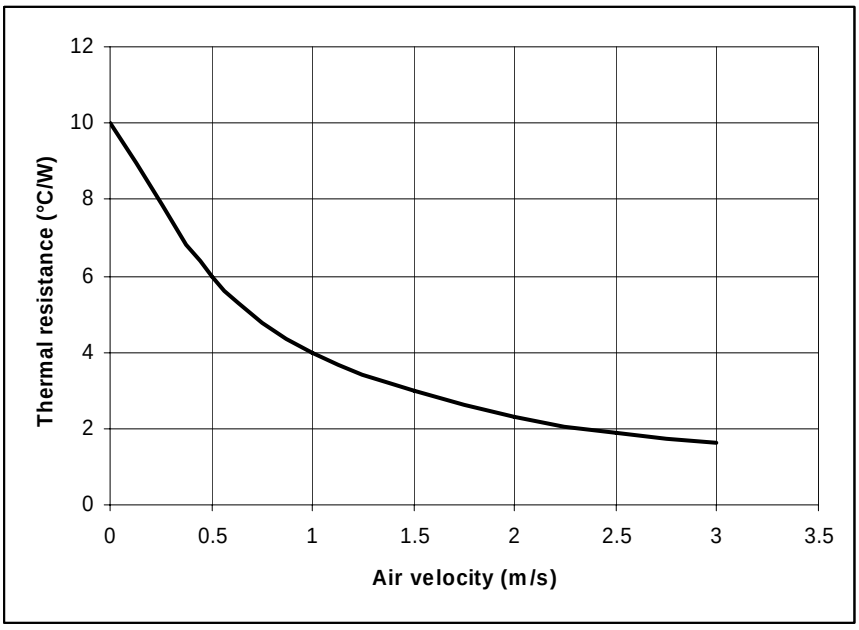
d. The tin-lead solder that was used in electronics manufacture had a eutectic composition, whereas the many different 'SAC' alloys that have replaced it are typically not of a eutectic composition. Discuss the issues relating to this switch, with special regard to the manufacturing process and subsequent product reliability. **(6)**

4. a. An electronic system includes two BGA packaged devices - a high speed microprocessor and a video-co-processor. They are connected via a 32-bit data bus. Describe how the PCB placement and routing could be optimised for these two devices with respect to thermal and electrical performance. **(5)**

b. The PCB for this system will typically require many layers. Discuss the distribution of power, ground and signal tracks between these layers. **(4)**

c. The BGA package has a thermal resistance of 0.3 °C/W and the video co-processor dissipates 8 W. What thermal resistance heat sink should be used to maintain the junction temperature of the device below 125 °C? State any assumptions made. **(4)**

d. The microprocessor dissipates 45 W and is mounted with a heat sink cooled by a fan. Using the graph below determine the air velocity necessary to keep the chip within a safe working temperature range.



Thermal performance of an air-cooled heat sink

(4)

e. Describe the alternative cooling strategies that might be employed if it were desired to implement the electronic system described above as a portable (i.e. low power) item. **(3)**

GLW-MH / NLS