Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (2.0 hours)

EEE335 Integrated Electronics

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

You may require the following:

The Shichman-Hodges model:

In the *triode* region:

$$I_D = K_n \frac{W}{L}\left(V_{OV} - \frac{V_{DS}}{2}\right)V_{DS}$$

In the *saturation* region:

$$I_{D0} = K_n \frac{W}{L}\frac{{V_{OV}}^2}{2}$$

In the *ohmic* region:

$$I_D \approx K_n \frac{W}{L} V_{OV} V_{DS}$$

Regardless of the region:

$$I_S = I_D$$

$I_G = 0$

Channel length modulation:

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

The overdrive voltage:

For an NMOS device: $V_{GS} = V_{TO} + V_{OV}$

For a PMOS device: $V_{GS} = -(|V_{TO}| + |V_{OV}|)$

MOSFET output resistance:

$$r_o = \frac{1}{\lambda I_{D0}}$$

MOSFET transconductance:

$$g_m = K_{n,p} \frac{W}{L} V_{OV}$$

Metastability:

$p_u = T_0 e^{-\frac{t_r}{t_c}}$ upsets/clock/data

1. The *pull-down* network for a digital CMOS gate is as shown in **Figure 1**:

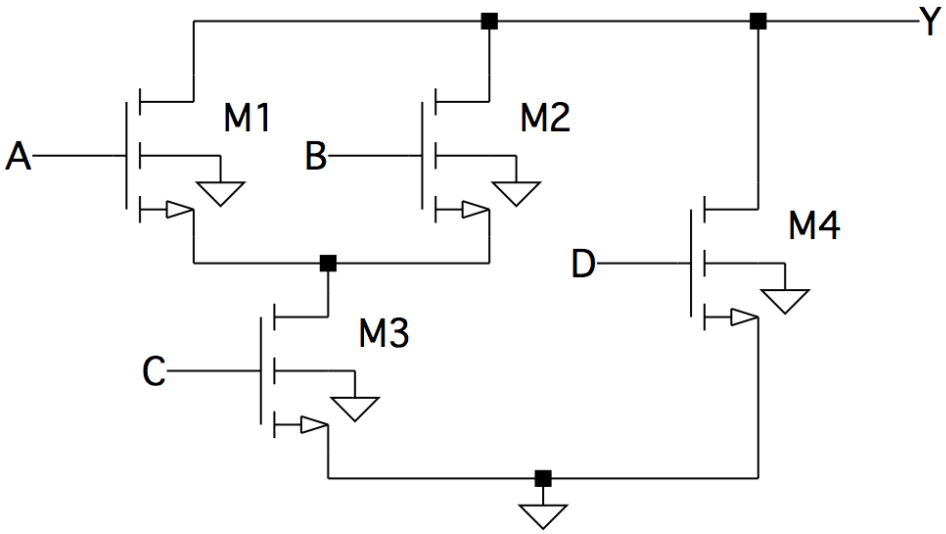

Figure 1: Pull-Down Network

a. Draw the corresponding *pull-up* network for the gate in **Figure 1**. **(4)**

b. Derive an expression for **Y** in terms of **A**, **B**, **C**, and **D**. **(4)**

c. Size the transistors **M1**…**M4**, assuming that the gate is *minimum-sized*. State any assumptions made. **(4)**

d. What is the justification for connecting all of the substrate connections for **M1**…**M4** to the negative supply rail? What problem can this, potentially, cause? **(4)**

e. If circuit in **Figure 1** were used in an environment where the output of the circuit, **Y**, could sometimes *under-shoot* (that is, a voltage at the output could be below the negative supply rail), the consequence could be that one or more of the transistors in the circuit could be damaged. Describe how this could happen and what might be done to prevent this problem. **(4)**

2. **a.** How is a *master-slave* D-type flip-flop organised. Draw a transistor-level schematic, identifying the function of each part. **(4)**

b. What is the constraint on the clock used for a *master-slave* D-type flip-flop? Draw a schematic for a non-overlapping clock generator. **(4)**

c. One of the problems that can occur with a flip-flop is *metastability*. What is *metastability* and what is the solution to minimise its occurrence. **(2)**

d. A system consists of two separate clock domains (D1, and D2). Data from D1 is being transferred to D2, as shown in Figure 2.

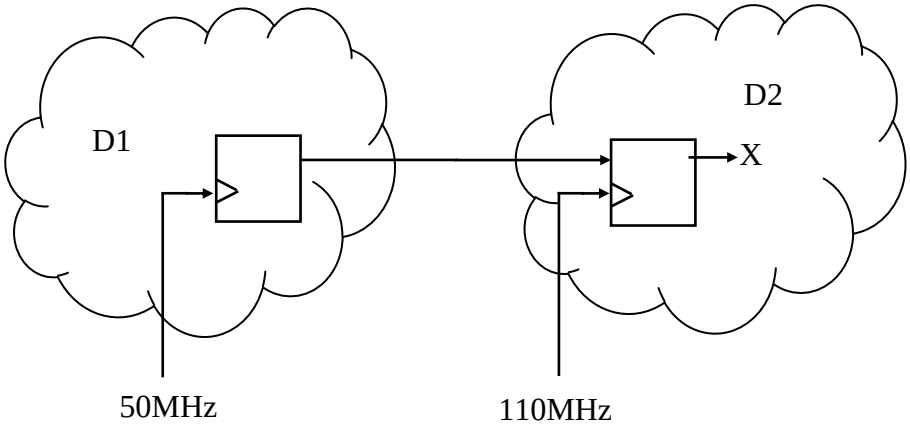

Figure 2: Transfer of Signal Between Clock Domains

i) You know that, for the fabrication process in which the components are implemented, $T_0=t_c=0.5$ns. Show that you would expect to see approximately 0.0175 *upsets/second* at point X. Please ensure that you justify your choice of t_r. **(4)**

ii) Is 0.0175 *upsets/second* at point X a reasonable result? If not, then why? **(2)**

iii) You decide that you need the number of *upsets/second* at point X to be fewer than $2.5\text{x}10^{-10}$. How would you design the receiving circuit in D2 to meet this requirement? **(4)**

3. a. Give a brief description of the following terms:

i) Overdrive voltage,
ii) Transconductance,
iii) Channel length modulation. **(3)**

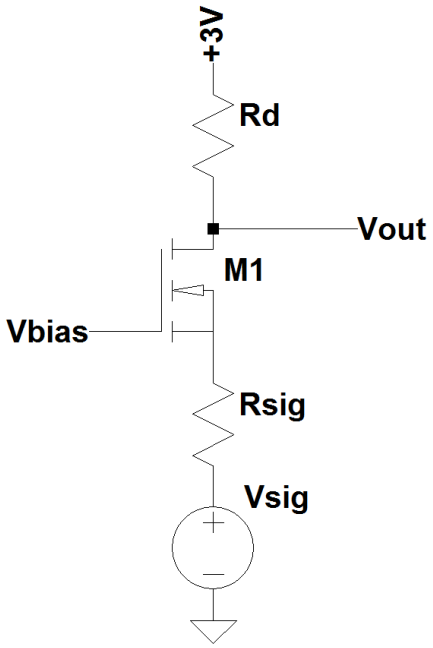

Figure 1: A SPICE model of a common gate amplifier.

b. **Figure 1** shows a SPICE model for a common gate amplifier. The MOSFET in the circuit, labelled M1, has the following parameters:

V_{TO}=0.6V, K_n=100μA/V^2, W/L = 8μm/1μm, λ=0.05V^{-1}.

The amplifier is to be biased at a drain current I_{D0}=150μA.

i) Calculate the overdrive voltage, V_{OV}, the transconductance, g_m, and the output resistance, r_o, of transistor M1. **(3)**
ii) Draw the small signal model of this circuit. Use the 'T' model for transistor M1 and include the effects of channel length modulation – you may ignore parasitic capacitances. **(5)**
iii) By ignoring the effects of channel length modulation, derive an expression for the gain of the amplifier, showing your working. Calculate this gain if the signal source V_{sig} has an output resistance, R_{sig} of 5kΩ and the drain resistor, R_d, is 50kΩ. **(3)**

c. For implementation on an IC, the drain resistor in **Figure 1** can be replaced by a PMOS current mirror active load.

i) Redraw **Figure 1** to show how you would implement this current mirror, showing where an external resistor would be connected to realise the reference current for the mirror. **(4)**
ii) If the PMOS transistors used in your mirror have a channel length modulation parameter λ=0.025V^{-1}, determine the gain of your redesigned amplifier (you may again ignore channel modulation effects for transistor M1 in this calculation). The bias current remains the same at 150μA. **(2)**

4.

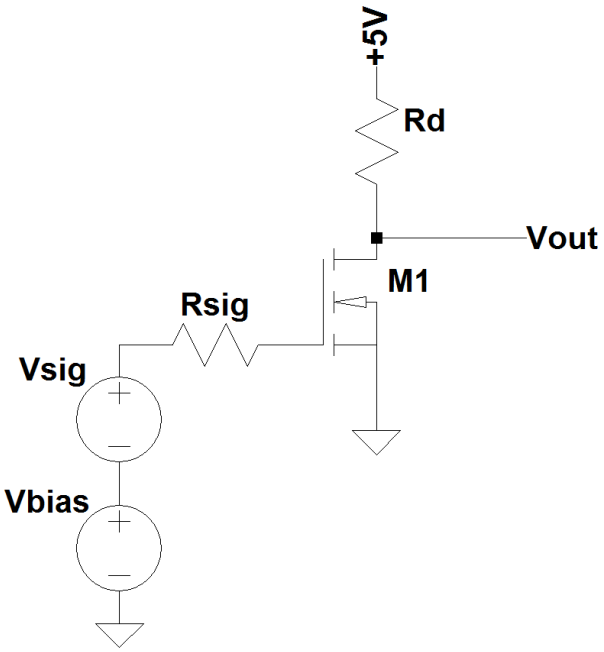

Figure 2: A SPICE model of a common source amplifier.

Figure 2 shows a common source amplifier. The amplifier operates with a transconductance of g_m=1.5mS. The parasitic gate-source and gate-drain capacitances are: C_{gs}=C_{ds}=10fF.

a. The bias voltage, V_{bias}, in **Figure 2** could be realised using a potential divider. Explain why this is not the ideal solution and give an example of a situation where it may cause a problem. Suggest an alternative method that could be used to bias the amplifier. **(5)**

b.

i) Draw the small signal model of the amplifier in **Figure 2**. Use the 'π' model for transistor M1 and include the dominant parasitic capacitances in your drawing. **(5)**

ii) The amplifier has a drain resistance R_d=5kΩ. Use this value and your small signal model to calculate the midband gain of the amplifier. Explain any assumptions you make in this calculation. **(3)**

iii) Calculate the two Miller capacitances for this amplifier and describe where they would appear in your small signal model (e.g. 'between the drain and source of M1', 'between the source of M1 and ground' or similar). **(3)**

iv) Calculate an approximate upper cutoff frequency for the amplifier when a source is connected whose output resistance, R_{sig}, is 100kΩ. State any assumptions made. **(4)**

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