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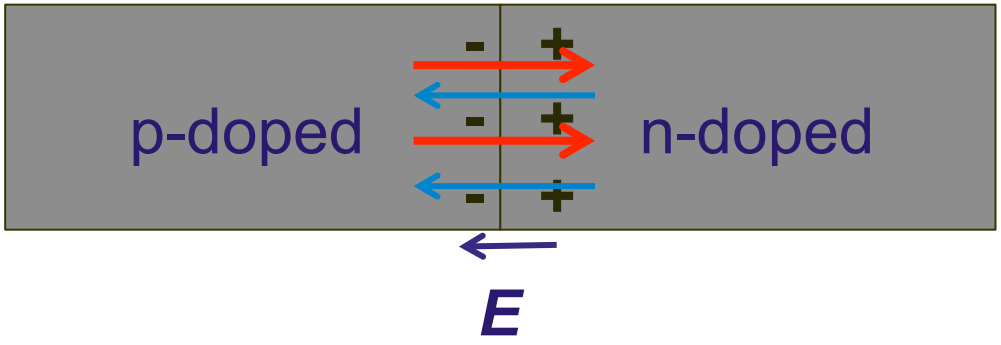
Lecture 19 (Review)

- p-n Junction (diode)
- JFET
- MOSFET
- Bipolar Transistor

PN Junction



J must be zero….

- Diffusion will occur (holes as red arrows – L to R, electrons as blue arrows – R to L)
- Fixed dopant atoms near the interface form a ‘space charge’
- An electric field must be generated to oppose the diffusion and create a drift current which is equal and opposite to the diffusion current i.e. net $J = 0$ – note that the built-in field direction opposes both electron and hole diffusion current
- This electric field will appear as a built-in potential, V_0, within the junction
- Here we will calculate the magnitude of V_0 and see what factors influence it….

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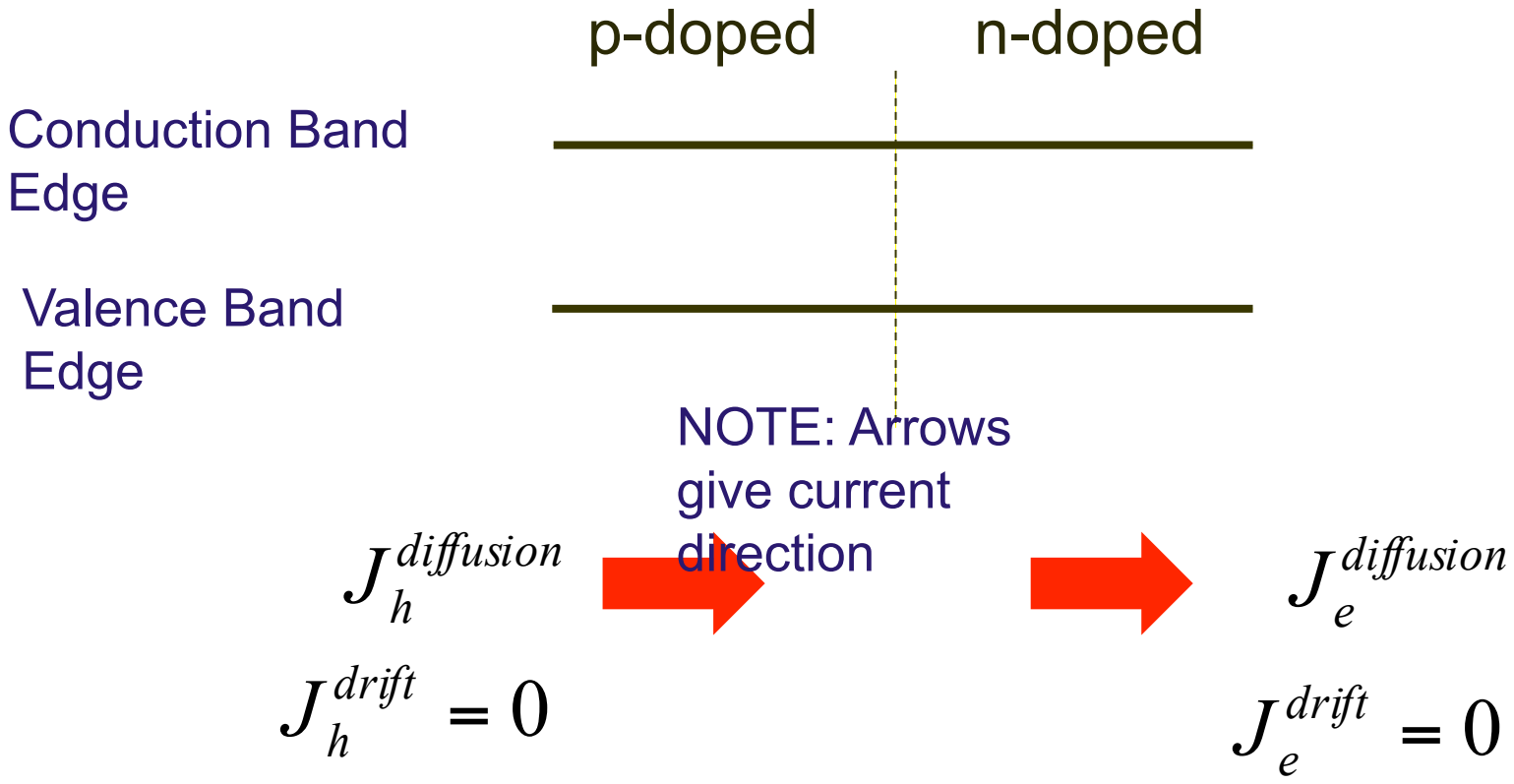
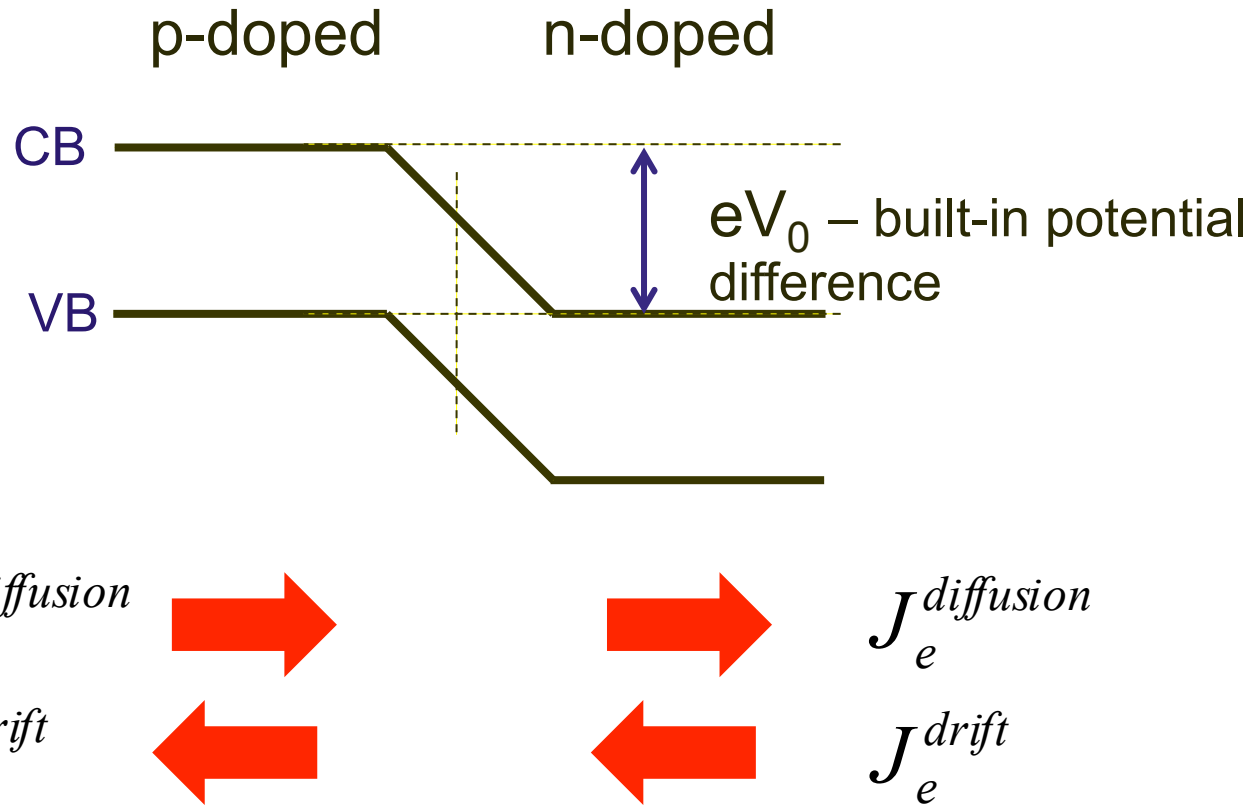
PN Junction - no internal field yet



Built-in Field at the Junction

Built-in field is established to exactly balance the drift and diffusion currents ($J = 0$)



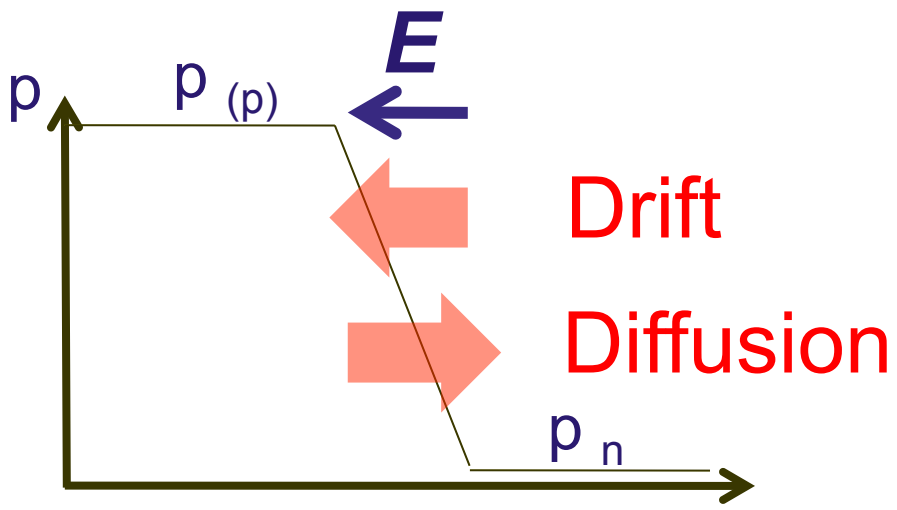
V_0 - consider holes

From discussion on drift and diffusion

$$J_h^{total}(x) = J_h^{drift} + J_h^{diffusion} = q\mu_h E_x p - qD_h \frac{dp}{dx} = 0$$

Rearranging

$$E_x = \frac{D_h}{\mu_h p} \cdot \frac{dp}{dx}$$



Built-in potential V_0

$$\Rightarrow \quad V_0 = \frac{k_B T}{e} ln\left(\frac{p_p n_n}{n_i^{\,2}} \right)$$

All terms are known, or can be calculated

T= Temperature
p_p = acceptor doping density
n_n = donor doping density
n_i= intrinsic carrier density

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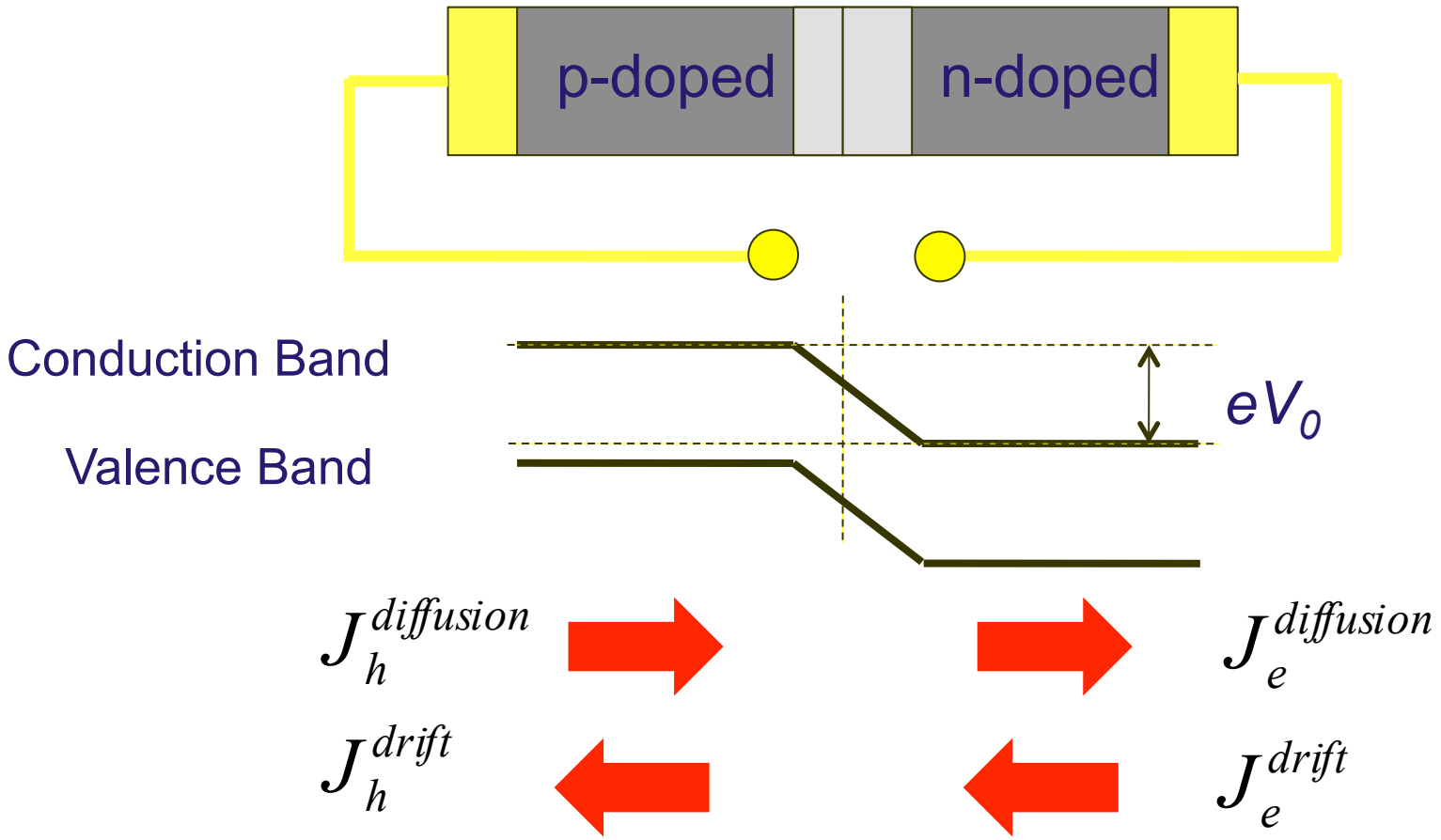
Zero External Applied Voltage



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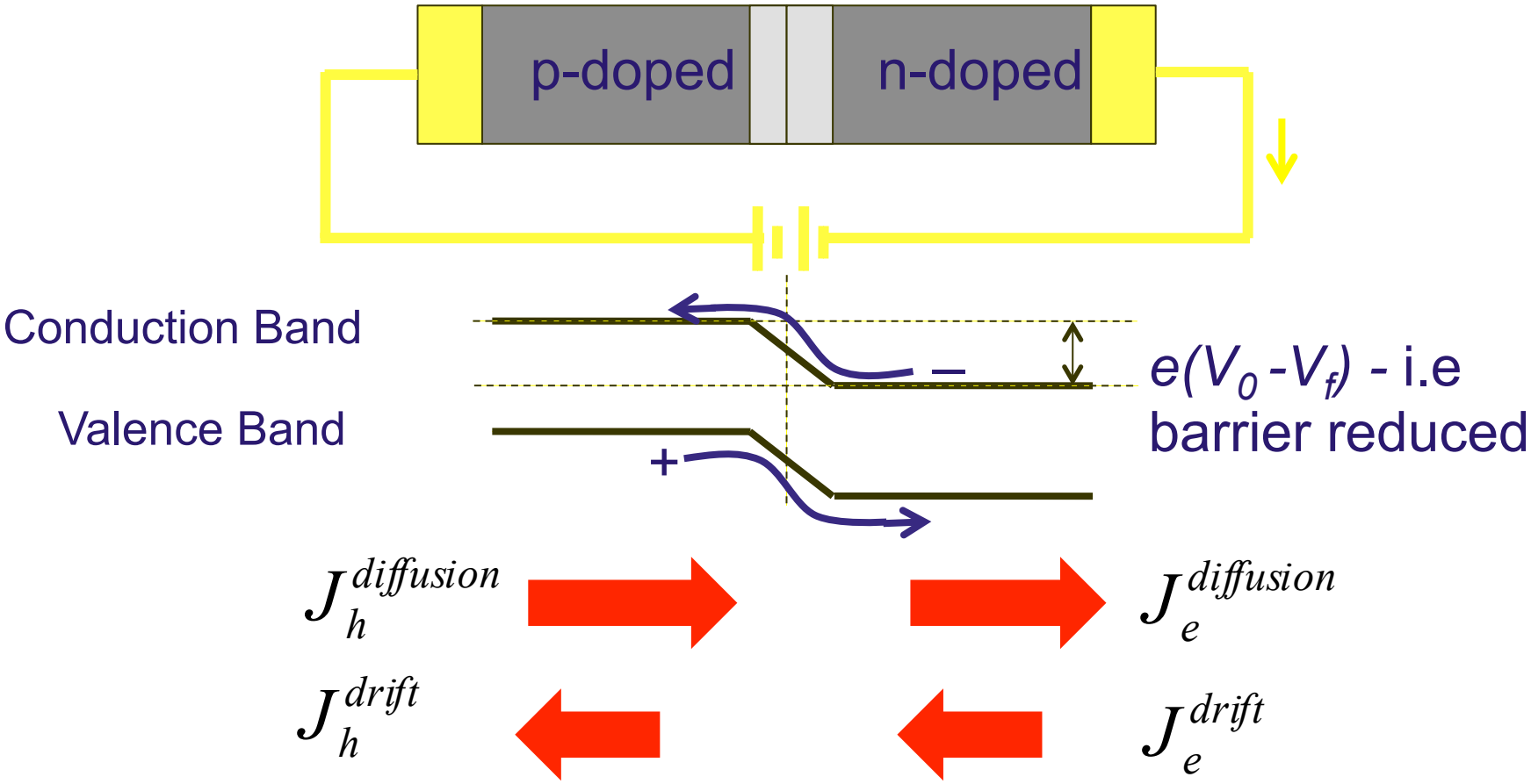
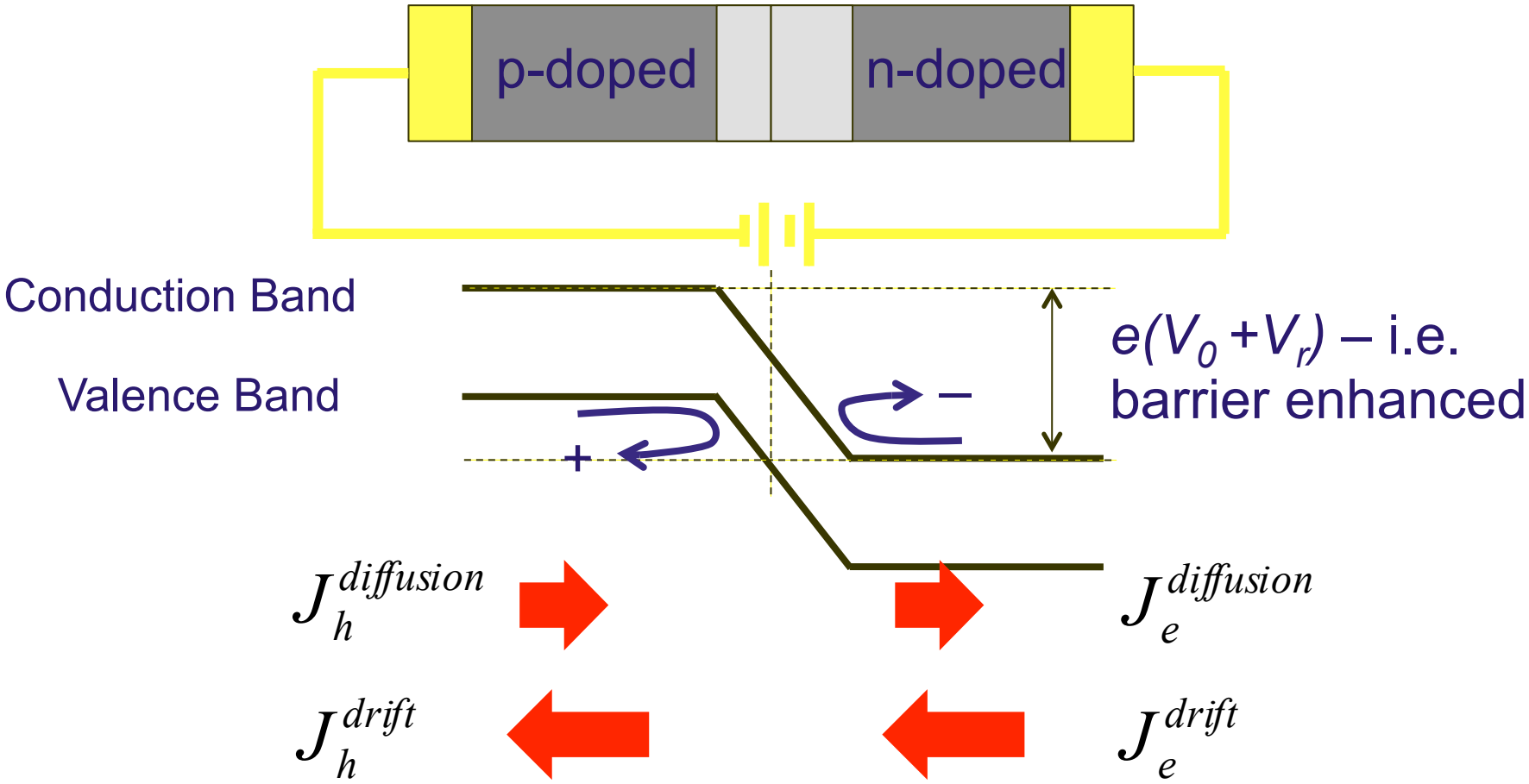
Forward Bias, V_f



Reverse Bias, V_r



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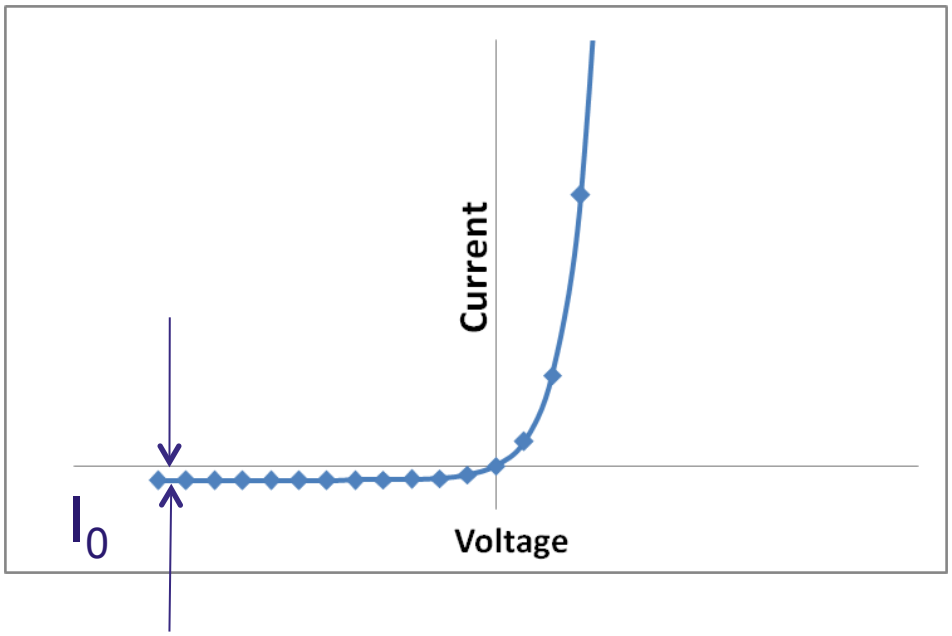
Can be + or - to reflect forward and reverse bias

Diode Equation

$$I = I_0\left[exp\left(\frac{eV}{k_BT}\right) - 1\right]$$



- Exponential increase in I with $V = V_f$
- For reverse bias $V \rightarrow -V >> k_BT$ (large and negative)
  $I \rightarrow I_0$
- I_0 is the (reverse) saturation current

In terms of current density, J

$$J = J_0\left[exp\left(\frac{eV}{k_BT}\right) - 1\right]$$

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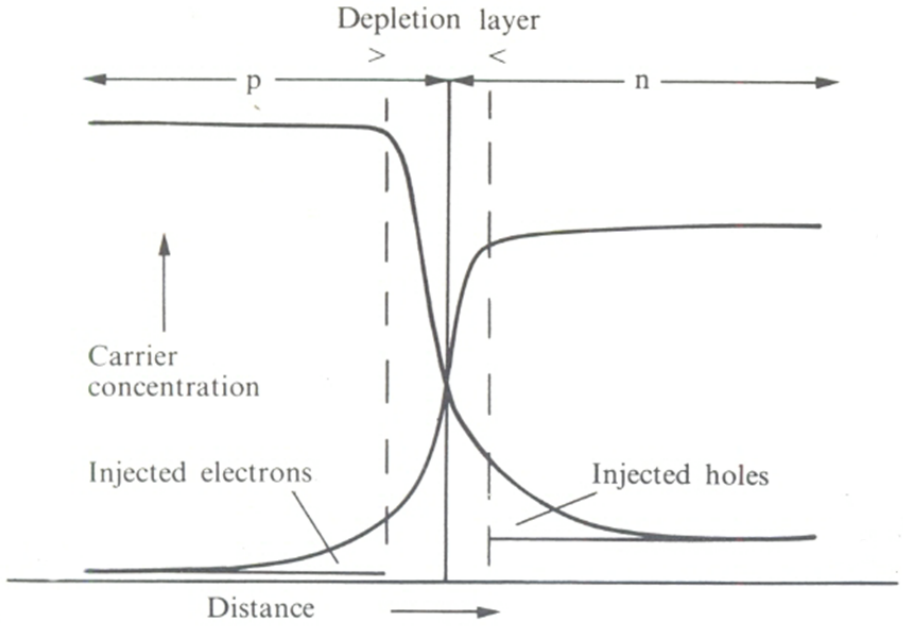
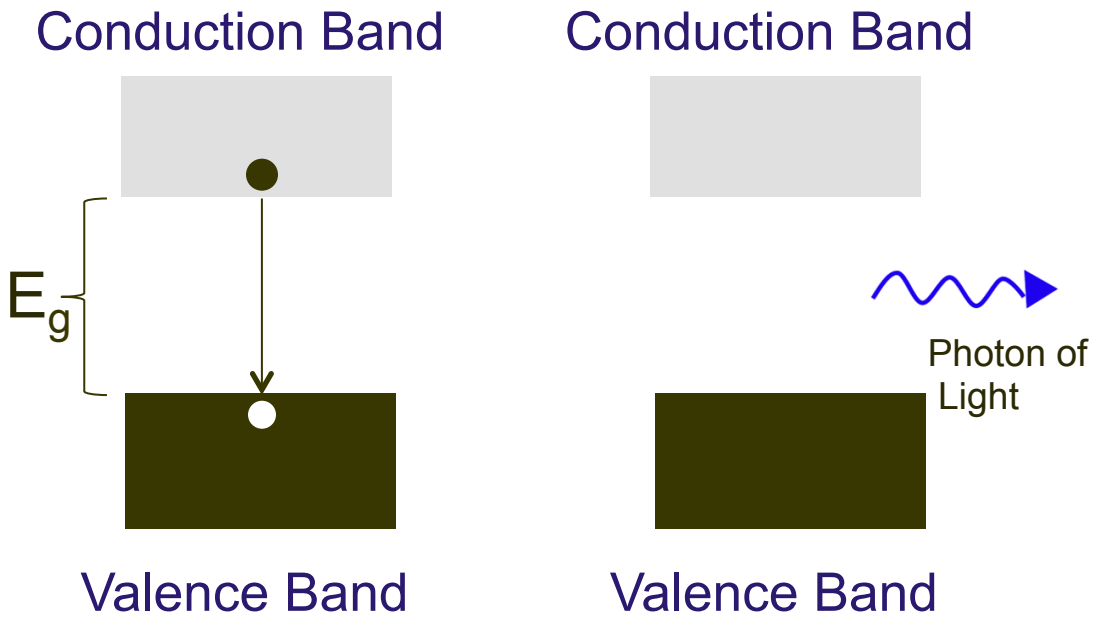
Light Emitting Diode



- In forward bias we can get a high concentration of electrons and holes in the same place controlled by the bias we apply
- In this region the electrons and holes can recombine liberating energy
- The most useful form of this energy is photons of light

Making coloured light - Energy and Wavelength



- Electrons recombine with holes across the band gap
- The electron ‘gives up’ its excess energy to return to the valence band
- This excess energy is equal to the band-gap of the semiconductor and is emitted as a photon
- Some semiconductors do this efficiently (e.g. GaAs, InP, GaN) others are innefficient and liberate their energy as heat rather than light (e.g. Si, Ge)

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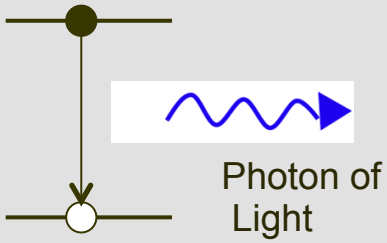
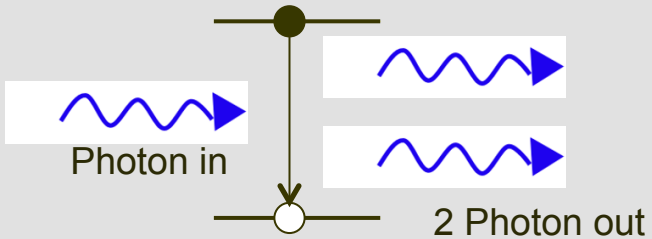
Spontaneous Emission and Stimulated emission

Spontaneous Emission



Random relaxation of an electron leads to emission of 1 photon

Stimulated Emission



One photon interacting with electron stimulates relaxation and two photons emerge

LED emits light through **Spontaneous Emission** process

Laser emits light through **Stimulated Emission** process

Each emitted photon can stimulate further emission:
1 -> 2 -> 4 ->8…
Hence a single photons is **amplified** in this process

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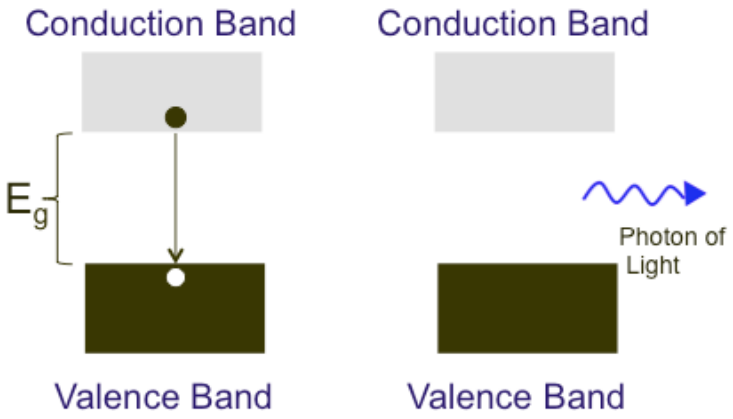
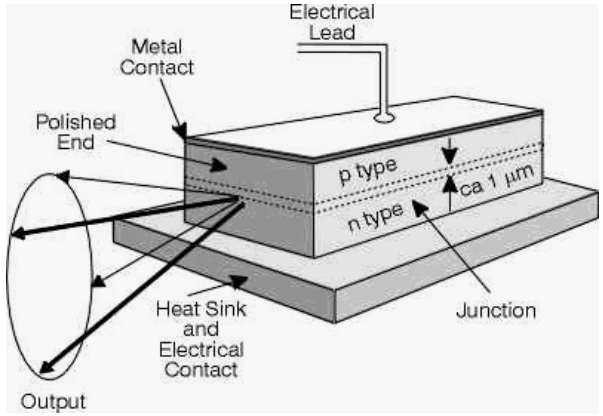
Semiconductor Laser





- In a semiconductor laser, the emission is between the bands
- In order to allow the photons to interact with as many atoms (electons) as possible a **feedback** mechanism is used. This consists of two mirrors surrounding the pn junction and reflecting light back in to the laser
- In a semiconductor the mirror is usually formed by the cleaved or polished edge of the laser chip
- Lasers emit a beam of light because only light travelling between the mirrors is amplified

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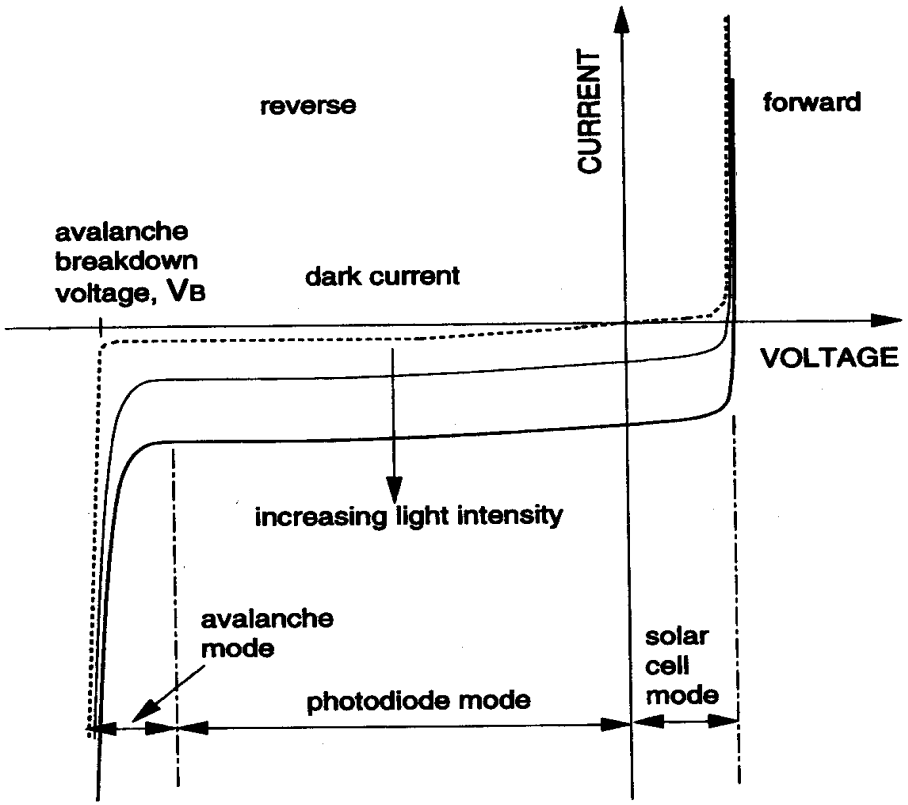
Detectors and Solar Cells



- In reverse bias, a PN junction can act as a detector for light.
- Minority carriers are generated in the depletion region if the energy of absorbed photons is larger than the band gap.
- The reverse bias field sweeps these carriers into the p and n- regions and this can be detected as a current in an external circuit
- In a Solar cell current and voltage (and hence power) are generated due to the effect of the internal electric field in the junction

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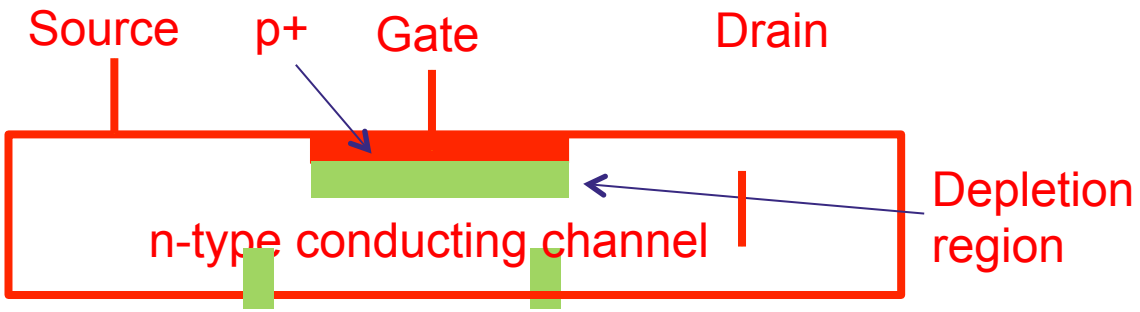
JFET – Planar Structure



$$W = \left[\frac{2\varepsilon(V_0 - V_f)}{q} \left(\frac{N_a + N_d}{N_a N_d} \right) \right]^{1/2}$$

- Width of depletion in a PN junction is controlled by applied voltage
- All contacts on surface (easier to make)
- Varying the gate voltage varies the cross-sectional area of the n-type channel under the gate and hence its resistance
- In this structure only the channel under the gate is modulated
- Transistor action allows drain current to be controlled by the gate voltage
- The JFET is known as a **unipolar** device i.e. uses only one type of carrier – the illustration is for an n-channel device – a p-channel device with n^+ gate regions is possible but get reduced performance due the lower mobility of holes

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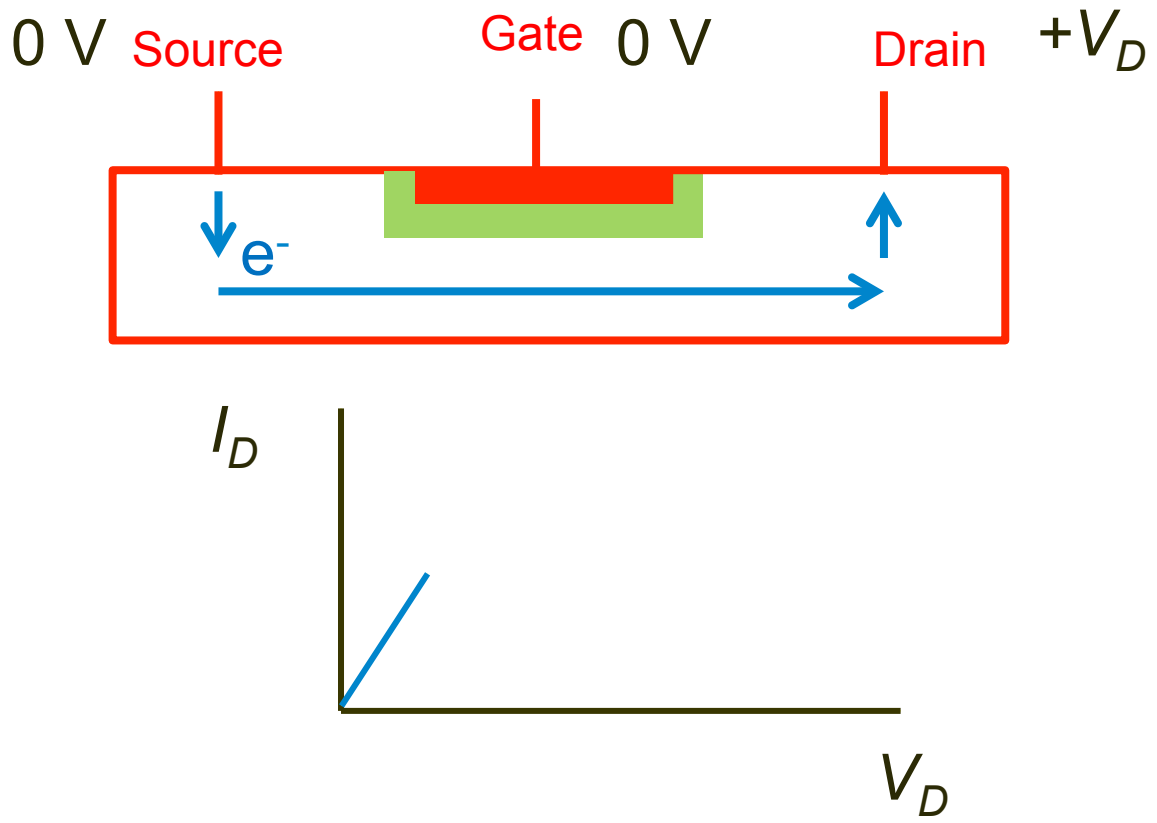
JFET – Output Characteristics



Zero gate voltage – small voltage between source and drain gives electron drift and hence drain current – behaves as a resistor.

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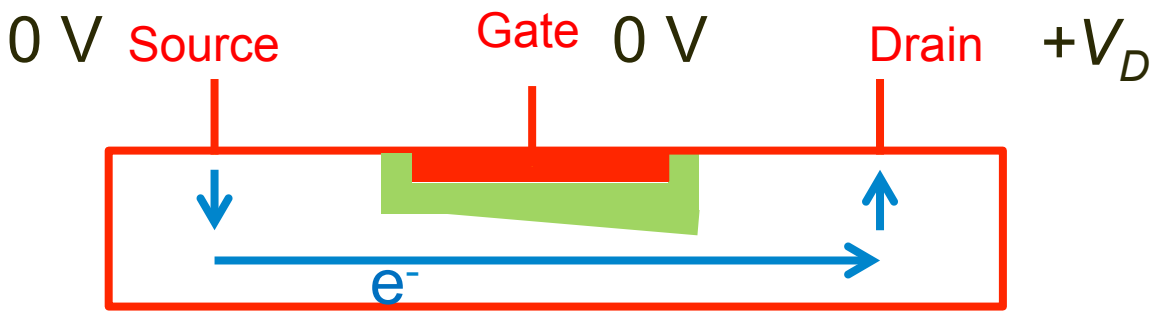
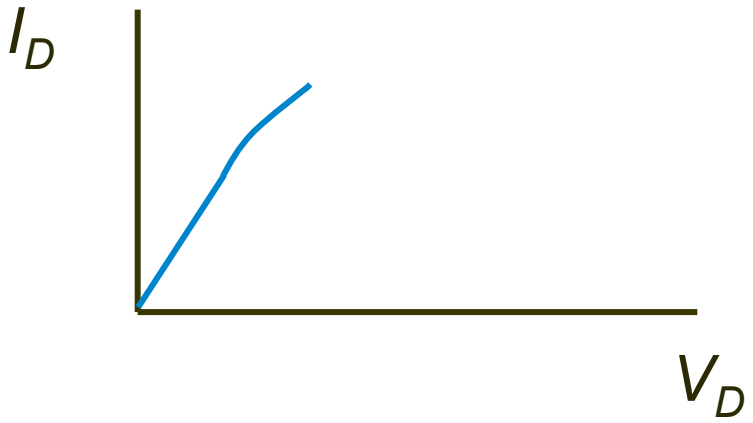
JFET – Output Characteristics





Zero gate voltage - as V_D and I_D increases further, the positive voltage at the drain increases the p^+n junction reverse bias at the drain end – increasing the depletion width there and so constricting the channel. As the resistance of the constricted channel is higher (reduced slope) – *I/V* plot is no longer linear.

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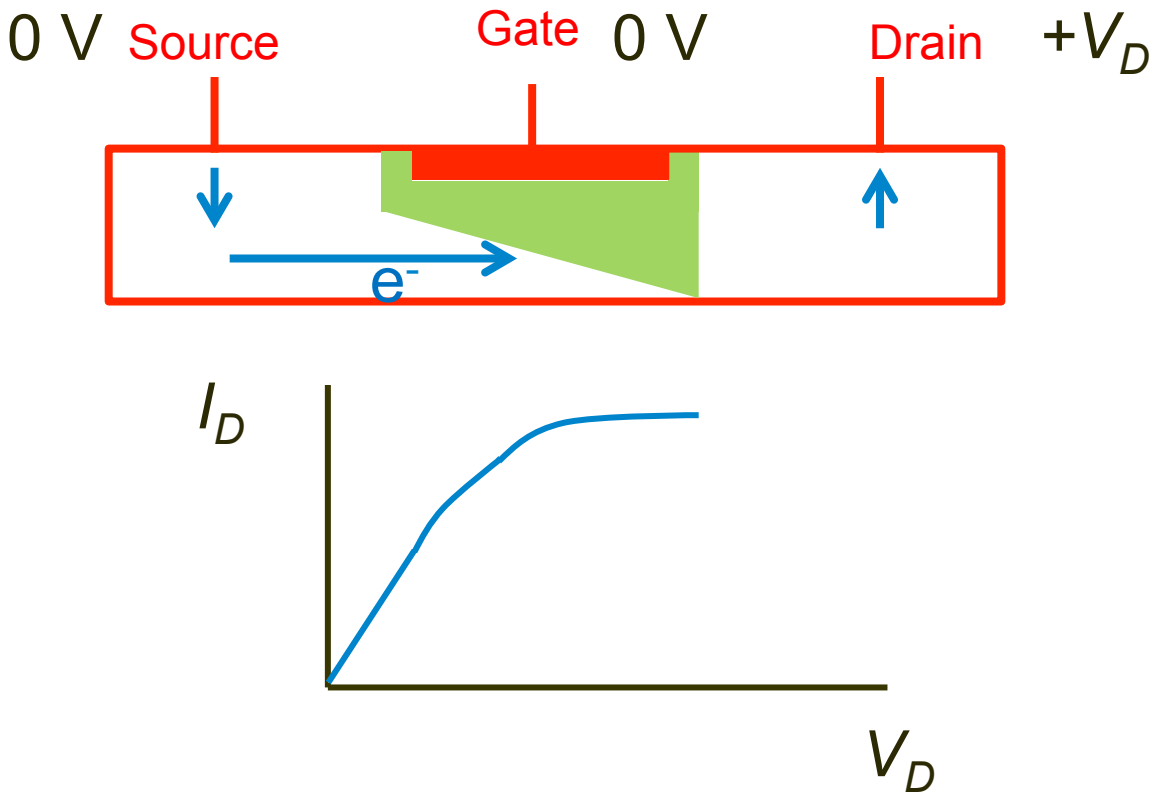
JFET – Output Characteristics



At higher V_D the depletion region closes the channel completely (called **pinch-off**) – the current I_D cannot increase with increasing V_D and it saturates (why does I_D not drop to zero?)

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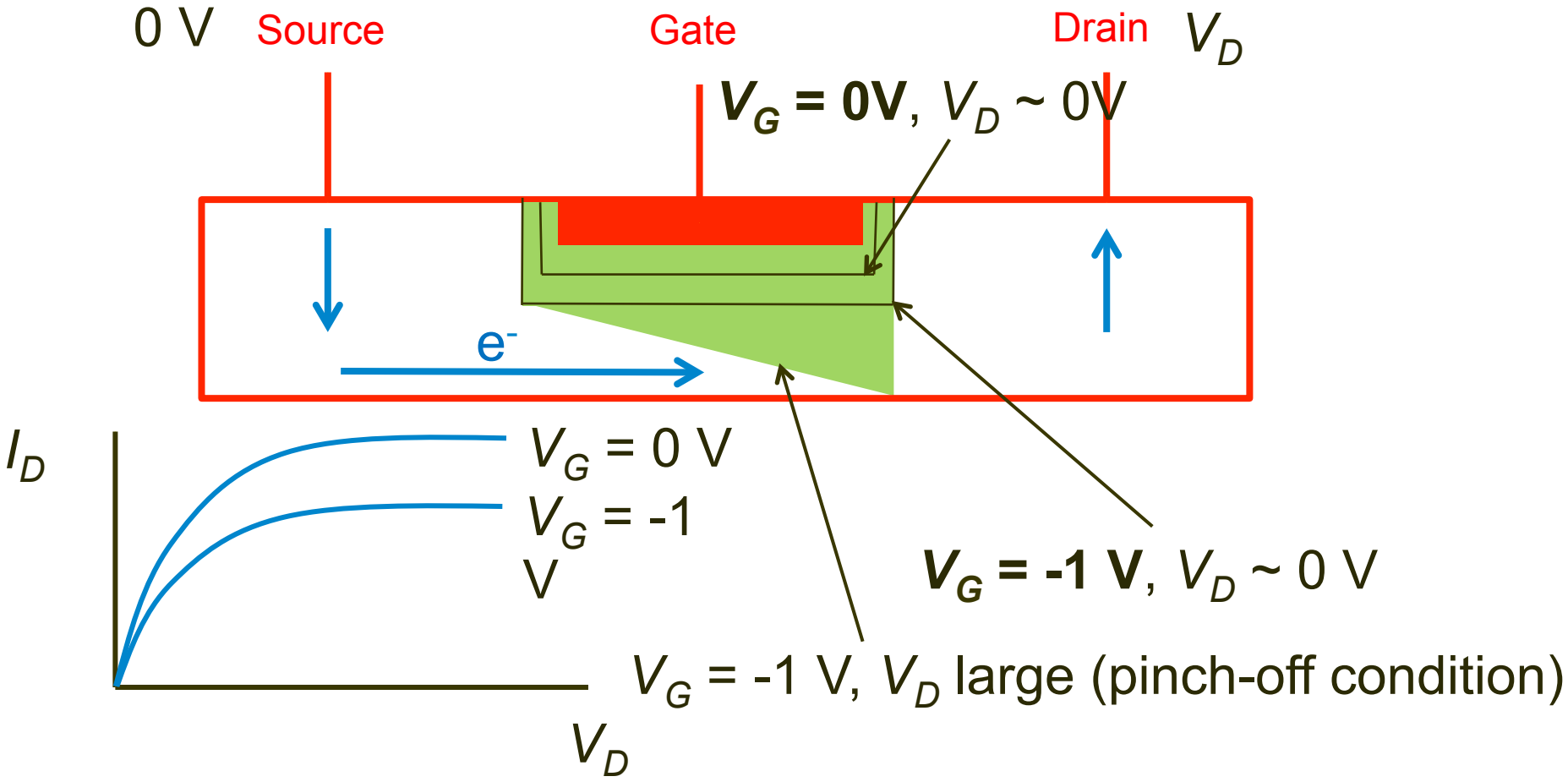
JFET – Effect of Gate Bias



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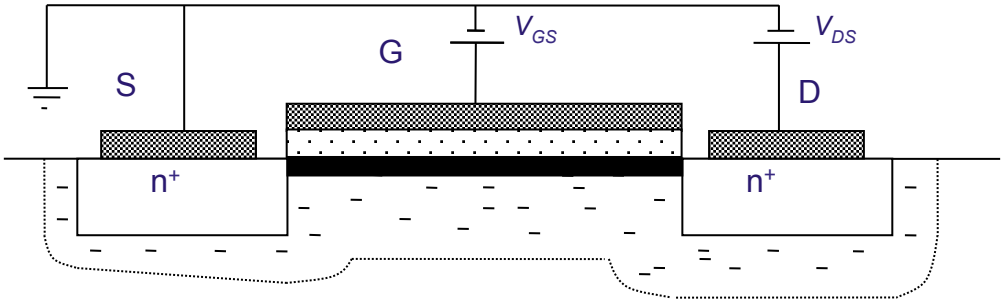
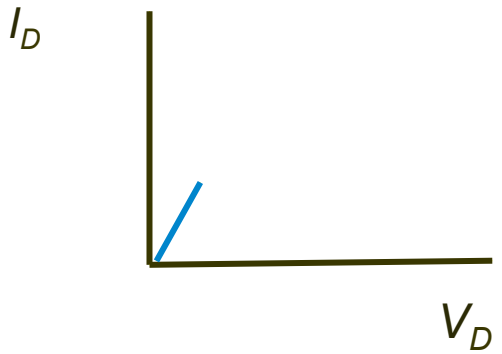
MOSFET - operation

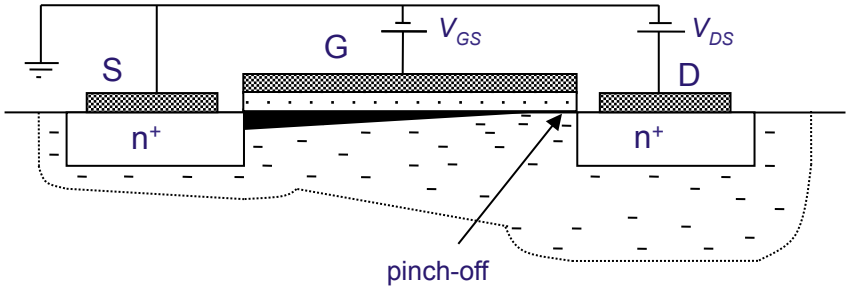


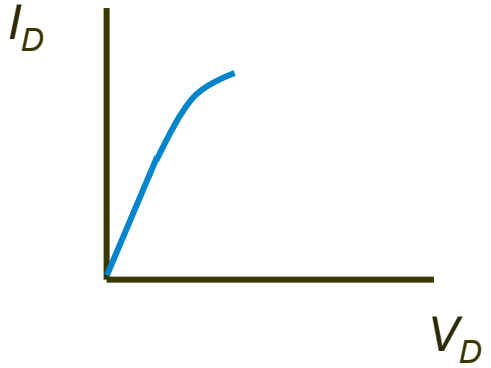


$V_D << V_G > V_T$ (linear region)

- As more positive charge is placed on the gate, depletion into the p-type region increases
- Eventually, as $V_G \cong V_T$ (called the threshold voltage), uncovering further negative fixed acceptors in the depletion region is not enough to balance the positive charge on the gate and electrons are formed under the gate (inversion layer) from the source and drain
- The source and drain are now connected by the mobile electron channel and the device conducts

MOSFET - operation





$\boldsymbol{V_D \cong V_G - V_T}$ (pinch-off condition)

- *As* $V_D - V_G$ approaches V_T, the net voltage between the gate and the drain at the drain end of the channel falls below V_T and the channel 'pinches-off' at the drain end where the channel potential is most positive

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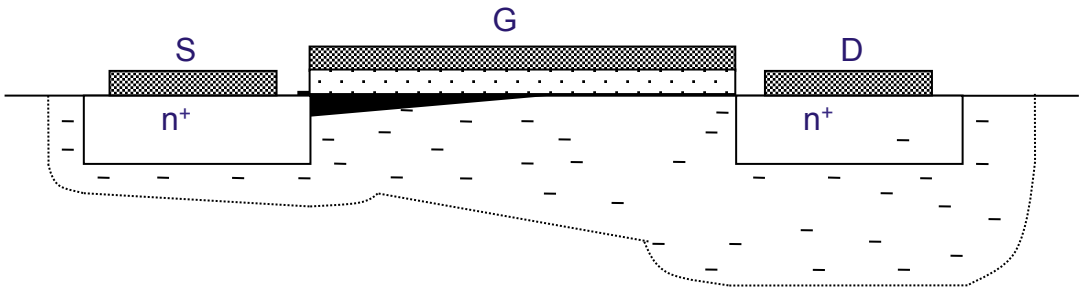
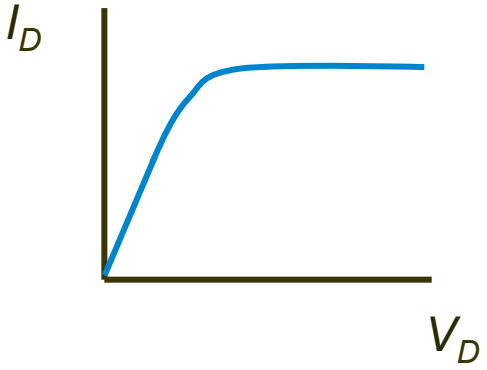
MOSFET - operation

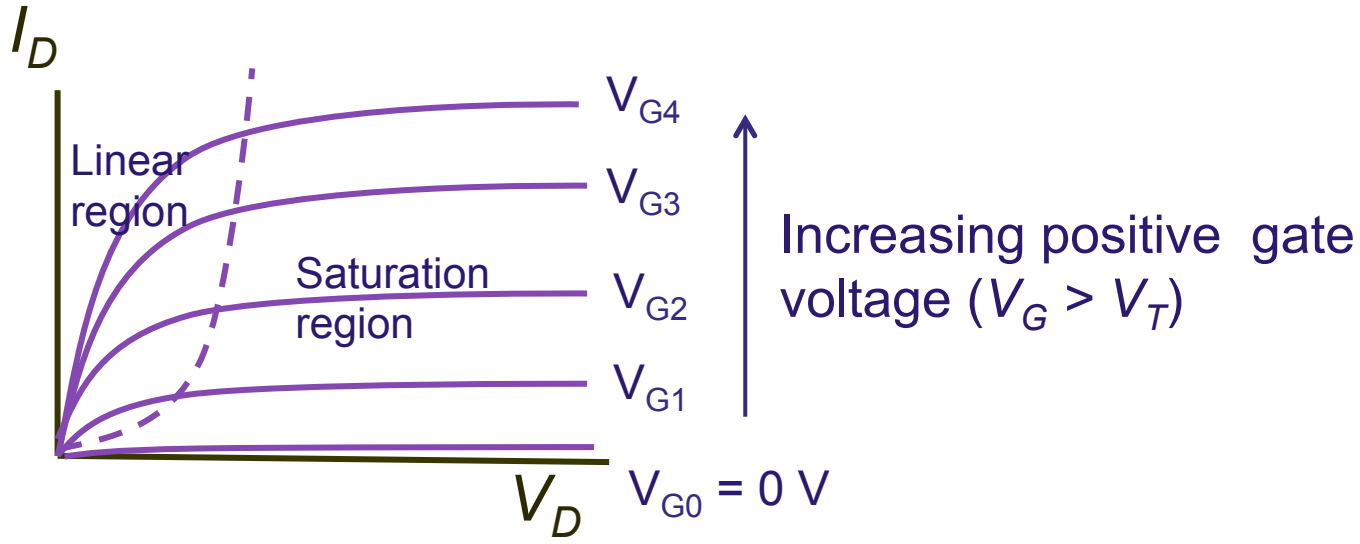




$V_D - V_G > V_T$ (saturation region)

- Further increases in V_D causes the pinch-off region to move towards the source
- I_D remains constant (saturation region)

MOSFET - Characteristics



- Similar shape to JFET but positive gate bias increases I_D
- **Enhancement mode** or **normally-off** device i.e. applying the gate bias increases or enhances the channel conductance and it does not conduct (is 'off') without a gate bias
- p-channel MOSFET possible by reversing the n and p regions and using a negative gate bias to induce conduction

Transconductance $g_m = \Delta I_D / \Delta V_G$ - measure of amplification

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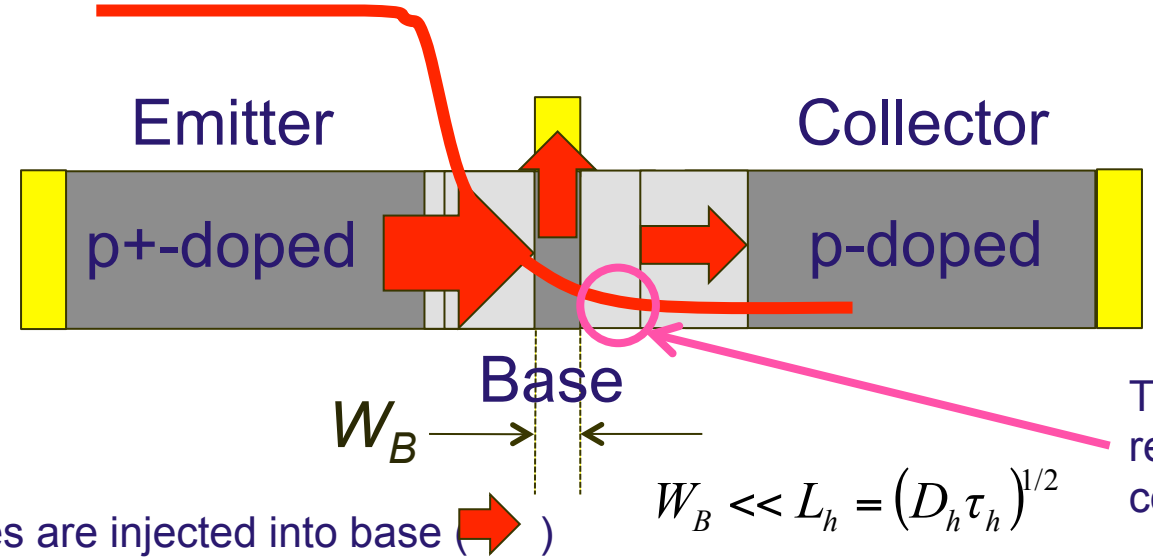
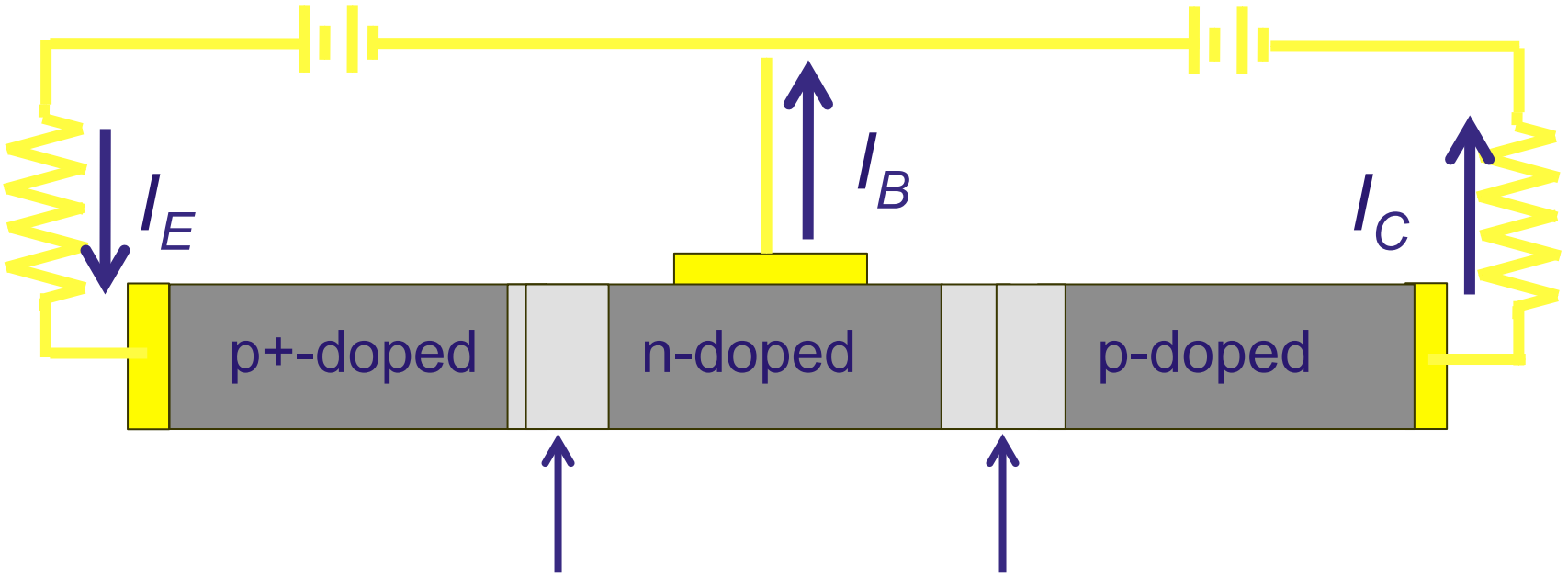
Bipolar Transistor (pnp)

Emitter-base junction diode forward biased, base-collector junction diode reverse biased



- Holes are injected into base ( )
- Some recombine with the majority electrons in the n-type base
- Electrons from the base contact flow in (conventional current flows out) to replace electrons lost by recombination
- Remaining holes diffuse to the base-collector depletion region before they recombine and are pulled into the collector region by the built-in electric field there
- These holes appear as current in the collector terminal
- The emitter-base bias therefore controls the collector current – transistor action

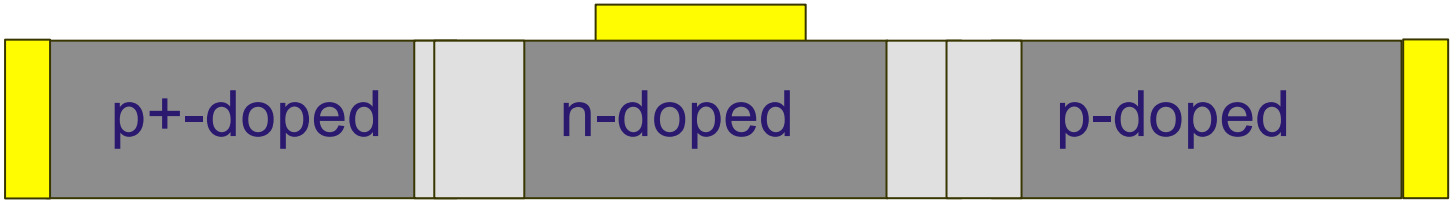
Bias

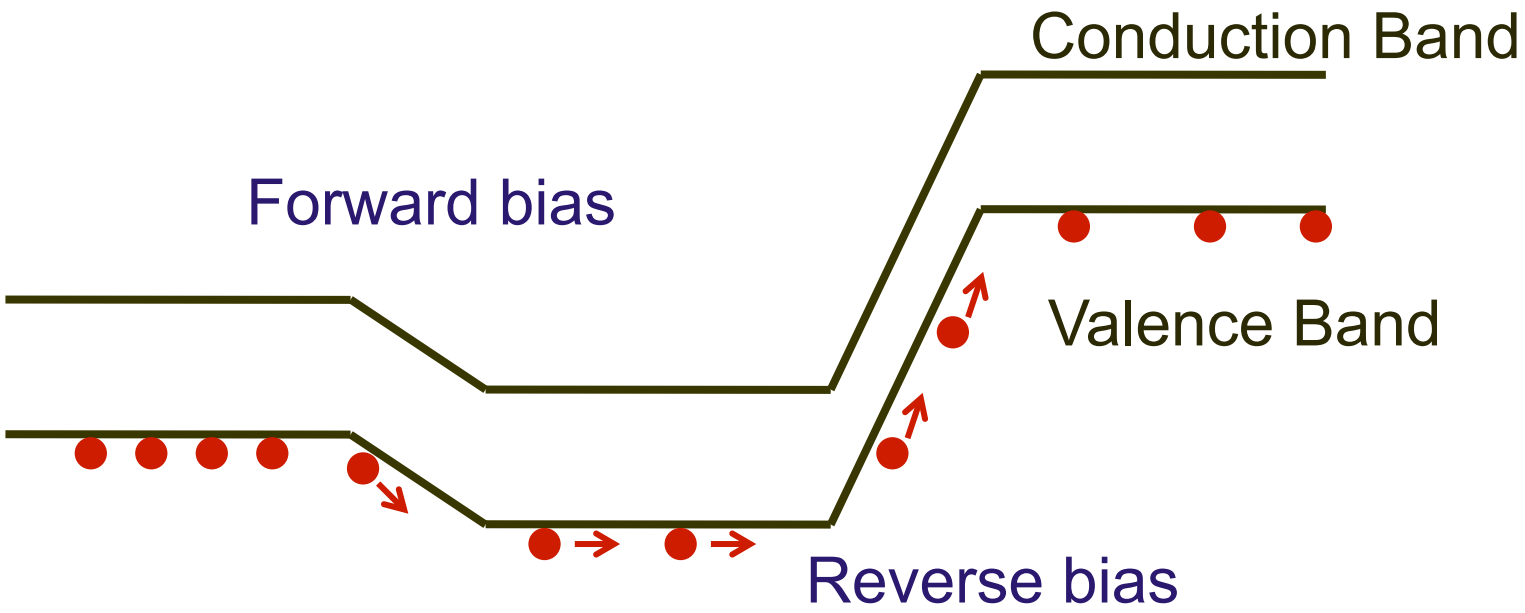


E-B forward biased diode – hole injector since p-doping >> n-doping.

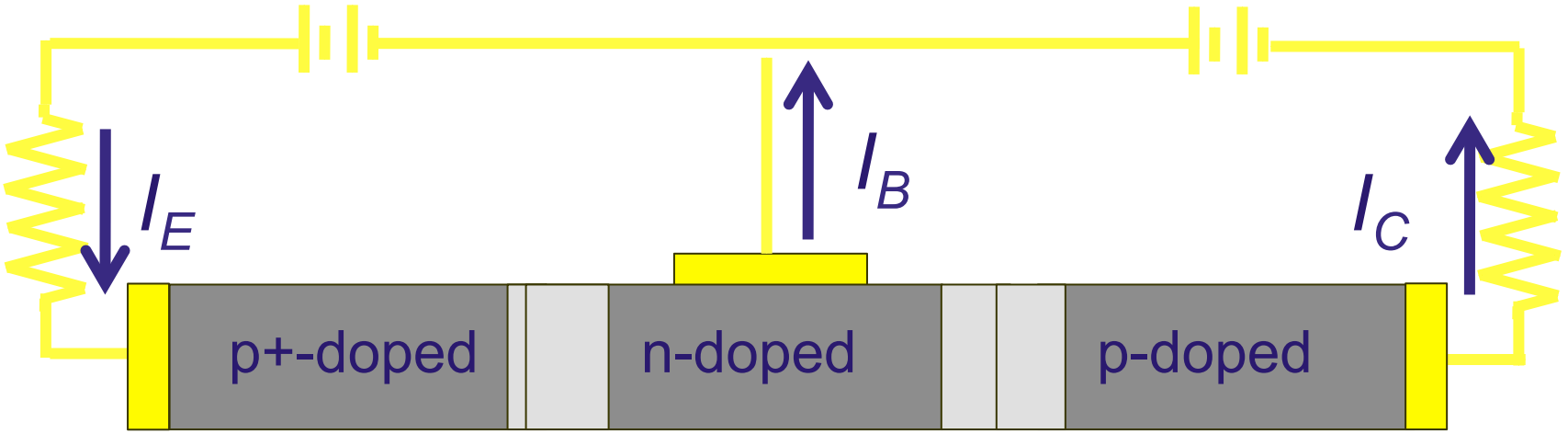
B-C reverse biased – small current unless holes make it to the B-C depletion region.

Operational Bias – p+-n-p





Currents



- For a high-gain transistor $I_E \approx I_C$ and $I_B \approx 0$, current gain $\beta = I_C / I_B$
- If all the current through the emitter-base is hole current and the base width is small there is no or very little recombination in the base

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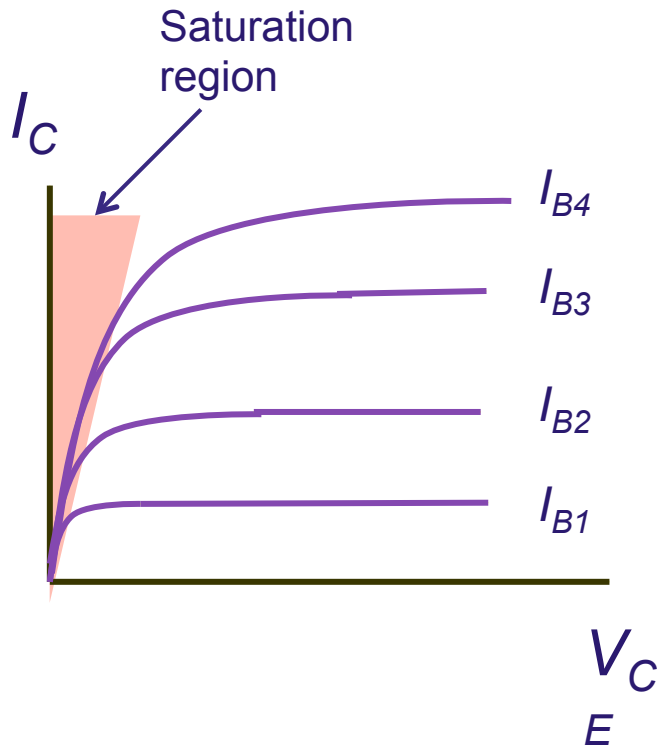
Characteristics (common emitter connection)

$$V_{CE} = V_{CB} + V_{BE}$$



- Saturation region (note: different from FET!) – both junctions in forward bias and $V_{CB} \approx V_{BE}$ and V_{CE} small

- Remainder of region is "normal operation" where emitter-base forward biased and base-collector reverse biased

$$\Delta I_C = \beta \Delta I_B$$