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The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2012-13 (3.0 hours)

EEE118 Electronic Devices & Circuits 1

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

You may require the following:

Electronic charge, e $=1.6\times10^{-19}$C

Permittivity of free space, $\varepsilon_0 = 8.85\times10^{-12}\ \mathrm{Fm^{-1}}$

Boltzmann's constant, k $=1.38\times10^{-23}\ \mathrm{JK^{-1}}$

Planck's constant, h $= 6.6\times10^{-34}$ Js

Energy of a photon $=hc/\lambda$

Poisson's Equation $\dfrac{d^2V}{dx^2} = -\dfrac{ne}{\varepsilon}$

$$E = -\frac{dV}{dx}$$

$$W = \left[\frac{2\varepsilon V_o}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

$$J = eD\frac{dn}{dx}$$

$$J_0 = \frac{eL_e n_p}{\tau_e} + \frac{eL_h p_n}{\tau_h} \quad and \quad J = J_0\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

$$n_p p_p = n_n p_n = n_i^2$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \gamma B$$

$$\partial p = \partial p_0 \exp\left(\frac{-x}{L_h}\right)$$

$$L = \sqrt{D\tau}$$

Resistivity $\rho = \dfrac{1}{ne\mu}$

$$C = \frac{\varepsilon A}{d}$$

$$D = \frac{kT}{e}\mu$$

Resistance $R = \rho L/A$

For silicon: relative permittivity $\varepsilon_r = 12$ built-in voltage = 0.7 V

electron mobility = 0.07 m^2/Vs hole mobility = 0.045 m^2/Vs

band gap = 1.12 eV

1. This question is about diodes and some common circuits that contain diodes.

a. The diode in figure 1a has a forward voltage drop of 0.7V but is otherwise ideal.

For the circuit of figure 1a,

i) Determine the conduction state of the diode. (2)

ii) If the diode is conducting, find the forward conduction current through the diode. However, if the diode is reverse biased, find the reverse voltage across the diode. (3)

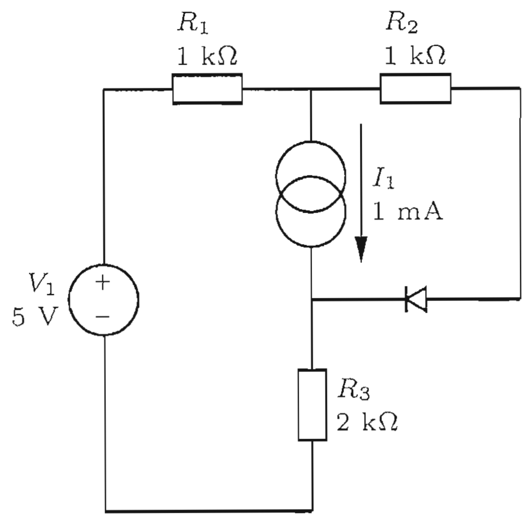

Figure 1a

b. If the current source is replaced by a variable current source, what value of current will cause the diode to be on the point of conduction? (4)

c. **i)** Briefly describe the operation of the circuit in figure 1b assuming that the time constant $R_1 \cdot C_1$ is much greater than period of the input signal.

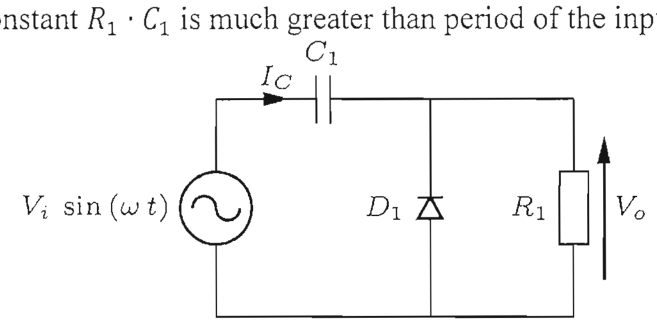

Figure 1b (5)

ii) Sketch, on separate labelled axes, the input voltage V_i, the output voltage V_o, the capacitor current, I_c. (4)

d. Combine the circuit from section 1c with a peak detector to form a voltage multiplier.

i) Sketch the voltage multiplier circuit diagram and label the components. (2)

ii) Assuming the peak detector has a sinusoidal input, sketch, on separate labelled axes, the peak detector input voltage, the peak detector output voltage and the capacitor current. (4)

iii) Write on your graph any significant time constants in terms of the component labels. (1)

2. **a.** Explain what is meant by the saturation regime for a bipolar junction transistor in terms of the bias conditions for each junction. What are the junction bias conditions for 'normal' operation where the transistor exhibits gain.

(6)

b. Figure 2 shows the output characteristics of a bipolar transistor.

(i) Sketch this characteristic on your script and indicate on that the regions corresponding to the saturation and normal regimes.

(ii) What is the minimum collector-emitter bias necessary to achieve full gain at 2 mA collector current?

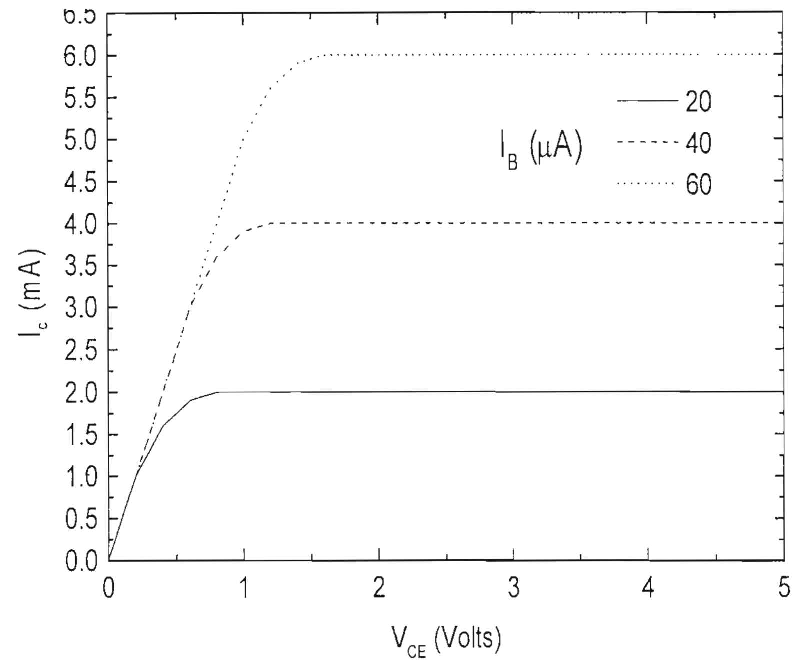

Figure 2

(4)

c. From the characteristic in figure 2 determine the common emitter current gain of this device in the normal operating regime.

(3)

d. The base transport factor B of a bipolar transistor can be related to base length by:

$$B = 1 - \frac{1}{2}\left(\frac{l_b}{L_e}\right)^2$$

Where l_b in the base length and L_e is the minority carrier diffusion length. Using equations given at the beginning of this paper and given that the emitter injection efficiency of this device is 0.997 and the minority carrier diffusion length in the base is 1.5 μm, calculate the base length, l_b to achieve a transistor gain of 100.

(8)

e. For the transistor in section (d) above, an error in the fabrication resulted in an emitter injection efficiency of 0.992 instead of 0.997. What is the resultant gain assuming that the base transport factor, B, is unaffected?

(4)

3. This question is about transistors both as switches and amplifiers.

a. Figure 3a shows a transistor switching circuit. Using the information provided in the diagram find,

i) the load current (1)

ii) the power dissipated in the load (1)

iii) the power dissipate in the switch (1)

iv) the range of possible base currents (2)

v) the maximum base resistance, R_B (1)

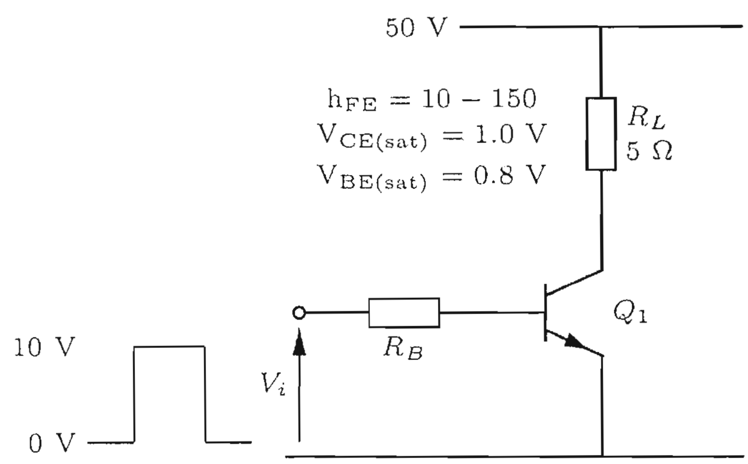

Figure 3a

b. The load resistance, R_L, in figure 3a is replaced by an electro-mechanical relay. The relay can be modelled by a series combination of inductance and resistance, where R = 15 Ω and L = 80 mH.

i) Sketch a circuit diagram showing the new switching circuit. (1)

ii) Calculate the inductor current just after the switch opens. (1)

iii) Calculate the energy stored in the inductor assuming the transistor has been switched on of a long time. (1)

iv) Add to your diagram any components required to prevent damage to the transistor. (2)

c. The design of the amplifier in figure 3b is incomplete, the collector current has already been chosen, and it is 2 mA. The voltage dropped across R_E is 1.3 V.

The maximum possible undistorted voltage swing at the output is required.

Using the information provided find numerical values for R_1, R_2, R_E and R_L. Assume that the transistor V_{BE} is 0.7 V in the forward active region and that the base current is negligible. State all other assumptions clearly. (9)

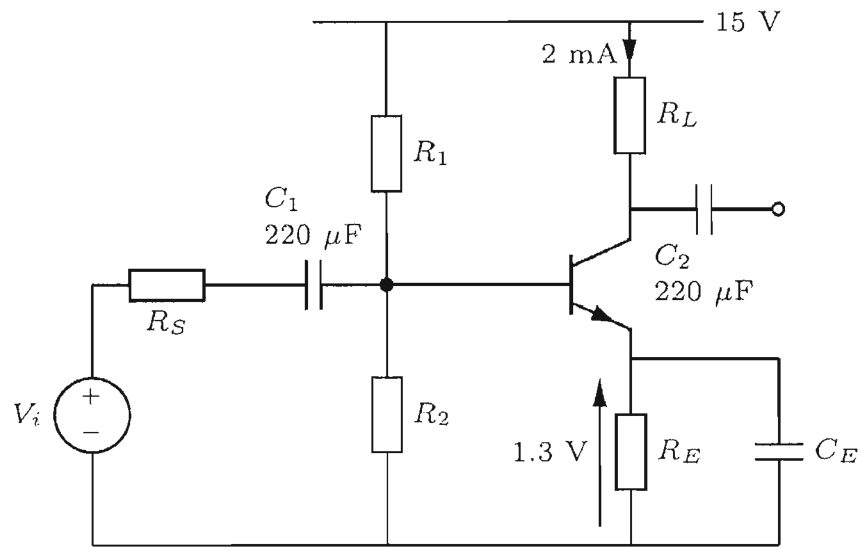

Figure 3b

d. Using a small signal equivalent circuit, find algebraically the small signal voltage gain for the amplifier in figure 3b. It is acceptable to use // to represent components which appear in parallel. **(5)**

4. a. (i) Briefly describe the difference between conductors and insulators from a free carrier point of view.
(ii) Describe the motion of individual electrons in a uniformly doped semiconductor at room temperature, with no electric field present. **(5)**

b. Explain briefly what is meant by "drift" and "diffusion" of charge carriers in a conductor and the conditions under which these occur. **(4)**

c. A copper wire of length 1 m has a resistivity of 1.8×10^{-8} Ωm at 300 K and a cross-sectional area of 1.5 mm^2. Calculate the resistance of the wire. **(3)**

d. The resistivity of copper increases with temperature. Briefly explain why this is the case. **(3)**

e. It is found that the increase in resistivity with temperature for copper is defined by an amount α, where $\alpha = 4 \times 10^{-11}$ $\Omega m K^{-1}$. Noting that the resistance of a given wire will increase at the same rate, calculate the change in resistance of the copper wire described in part (c) if the temperature is increased from 300 K to 620 K. You may assume that any increase in the length or cross-sectional area of the copper wire due to the thermal expansion can be neglected in this case. **(6)**

f. Contrary to the case with copper in section (d) above, the resistivity of a particular intrinsic semiconductor is shown to decrease with increasing temperature. Explain why this is so. **(4)**

5. **a.** Using diagrams where necessary, describe how a potential barrier forms at the junction between the p- and n-type materials in a diode, explaining clearly the formation of the so-called "depletion region".

(8)

b. The total depletion region thickness for a n-p junction, W, is given by

$$W = \left[\frac{2\varepsilon V_o}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

(i) Show how this can be simplified for the case of a 'one-sided' n^+-p junction where $N_d >> N_a$.

(ii) Explain why the depletion region is mainly on one side of the junction and identify which side.

(6)

c. Show how the above equation can be modified to give the depletion region width of a p-n junction under reverse bias.

(3)

d. A p-channel planar Junction Field Effect Transistor (JFET) fabricated from Si has the following parameters:

n-type gate doping, $n = 1\times10^{26}\ m^{-3}$
p-type channel doping, $p = 1\times10^{22}\ m^{-3}$
channel thickness, $a = 0.8\ \mu m$
gate width, $w = 10\ \mu m$
gate length, $l = 1\ \mu m$

Calculate the gate bias required in order to pinch-off the channel completely (pinch-off voltage), allowing no current flow though the device. State all assumptions you make. (5)

e. For certain applications, so-called III-V semiconductors, such as gallium arsenide (GaAs), can be preferred to Si for FETs because of their higher electron mobility. Briefly explain why this will result in higher performance. (3)

6. a. i) Draw the circuit symbol for an operational amplifier (opamp) and label,
   a. the inverting input
   b. the non-inverting input
   c. the output (3)

ii) Give typical values for the,
   a. input impedance
   b. output impedance
   c. open loop gain (3)

iii) State the opamp equation and define the terms. (2)

b.

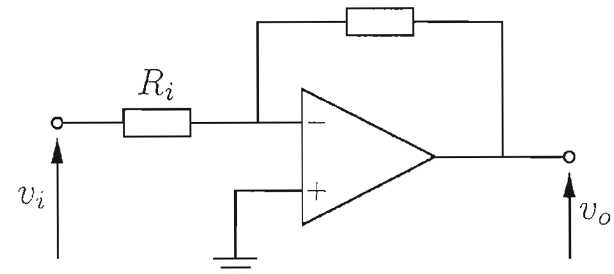

Figure 6a

i) Identify the opamp circuit in figure 6a. (1)

ii) Find an expression for $\frac{v_o}{v_i}$ assuming $A_v \to \infty$. (3)

iii) Show that $\frac{v_o}{v_i} = \frac{-R_f}{R_i + \frac{1}{A_v}[R_i + R_f]}$ assuming A_v is finite. (5)

c. The opamp circuit in figure 6b is part of a process control system.

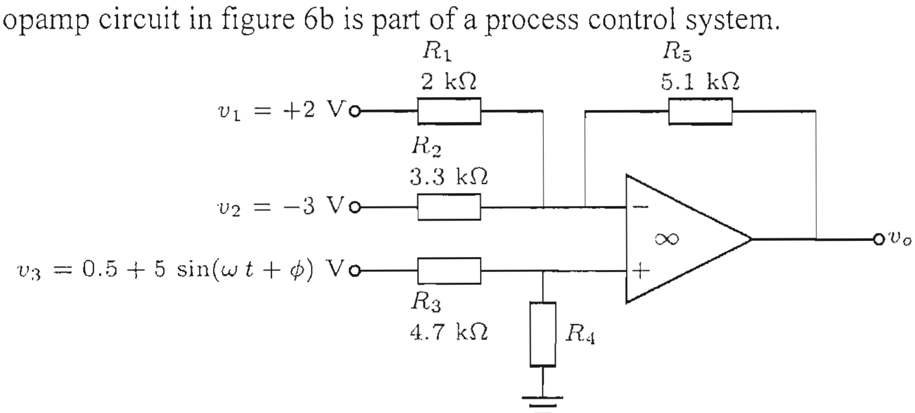

Figure 6b

i) With the inputs shown in the diagram a DC output of 0 V is required. Find the resistance R_4 which fulfils this condition. (5)

ii) Assuming R_4 is 1 kΩ, find the output voltage amplitude and phase due to the AC input. (3)

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