EEE 331 – Tutorial Answers 2

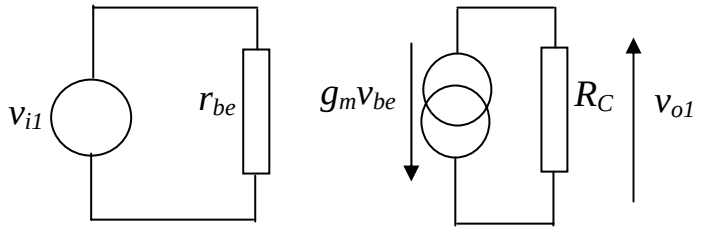
Bookwork questions

1) The current gain for a Darlington transistor is β^2 and β for the Cascode connection.

2) Cascode circuits are useful for high-speed voltage-gain applications owing to the reduced Miller effect when compared to common emitter amplifiers. The circuit is also useful as a level shifter.

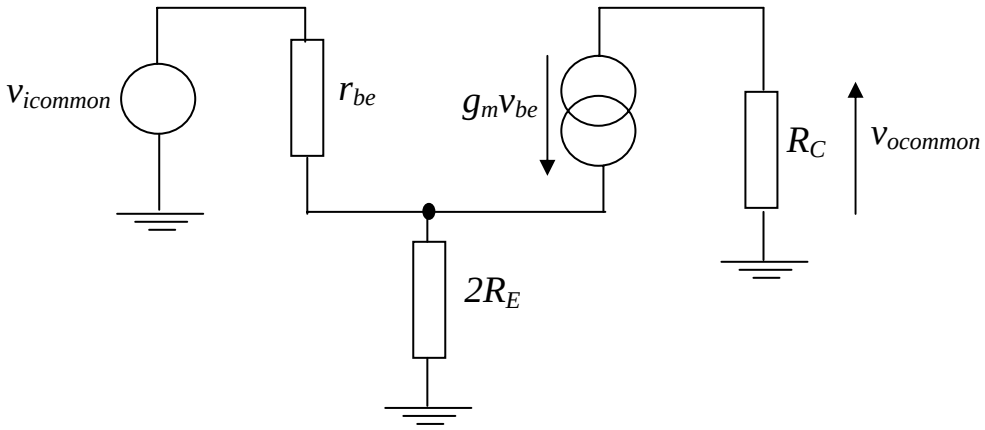
3) $v_i = v_{i1} - v_{i2}$ and $v_o = v_{o1} - v_{o2}$.

4) The differential mode half circuit is,



from which we can derive the differential mode gain as $A_{dm} = \dfrac{v_{odiff}}{v_{idiff}} = -g_m R_C$.

Whilst the common mode half circuit is,

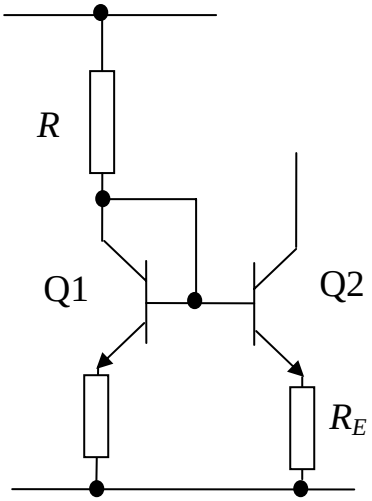


and the corresponding gain is

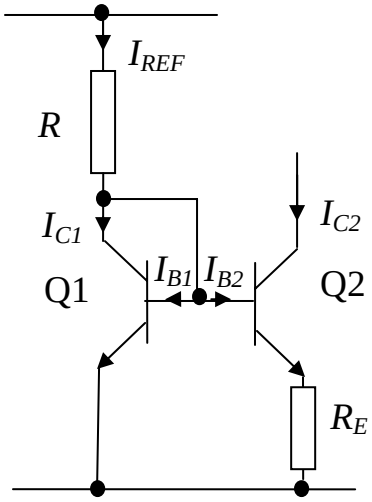
$$A_{cm} = \frac{v_{oc}}{v_{ic}} = \frac{-\beta R_C}{r_{be} + 2R_E(\beta + 1)} = \frac{-g_m R_C}{1 + 2g_m R_E\left(1 + \dfrac{1}{\beta}\right)}.$$

Thus the CMRR, $\frac{A_{dm}}{A_{cm}} = 1 + 2g_m R_E \left(1 + \frac{1}{\beta}\right)$

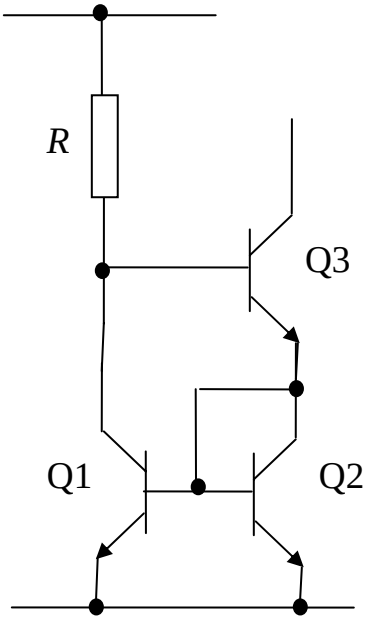
5) The emitter degenerated current source



Wildar current source



Wilson current source



All

All of the above circuits offer improved output impedance compared to the standard current source topology.

6) $$\frac{I_{REF}}{1+\frac{2}{\beta}} = I_{C2}$$

7) Factors we might have to consider when designing an output stage include, but are not limited to;
- Deliver a certain amount of power into a load.
- Distortion the transmitted signal as little as possible.
- Have a low output impedance to ensure that the output voltage is relatively unaffected by the load.
- Low quiescent power consumption.
- Should not be a major limitation to the frequency response of the IC.

Application questions

8) The question tells us that we should assume all of the things that were assumed in the notes when deriving the common mode and differential mode half circuits, and so we can use the results obtained using them.

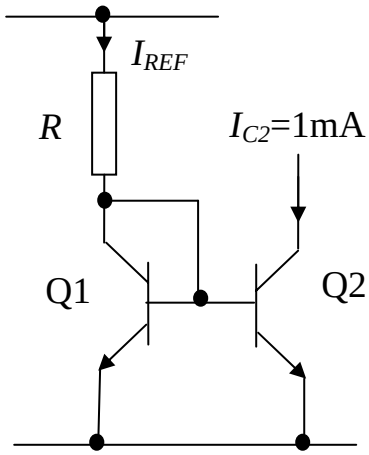
$$A_{dm} = -g_m R_C = -1000 \times 100k\Omega = -10^8 V/V$$

and

$$A_{cm} = \frac{-g_m R_C}{1+2g_m R_E\left(1+\frac{1}{\beta}\right)} = \frac{-1000 \times 100k\Omega}{1+2\times 1000\times 10M\Omega\left(1+\frac{1}{100}\right)} = -4.95\times 10^{-3} V/V$$

Hence CMRR = $\underline{2.02\times 10^{10}}$

9) We have a number of topologies available to us, so the first job is to try to decide which one is appropriate. A simple transistor current source would have an output impedance of V_A/I_C = 100/1mA = 100kΩ (think about the definition of early voltage if this doesn't make sense to you). Hence a simple current source will provide the correct impedance.



Personally I would use the simple current source, since it is capable of providing the desired impedance and also has a large output voltage swing ($V_{CC} - V_{CE\ on}$ = 4V), whereas the other more advanced topologies have a limited output swing. Indeed the Wilson source can only give a swing of $V_{CC} - 2V_{CE\ on}$ = 3V, and so does not meet our specification. The Wildar could fulfil the requirements, but you would need to design it to ensure that we could obtain > 3.5V swing.

All that remains is to choose *R* to obtain the correct output current. Since the question has told us we have high β transistors, the output current is as follows…

$$I_o = I_{c2} = \frac{V_{CC} - V_{CEon1}}{R}$$

$$\therefore R = \frac{5V - 1V}{1mA} = 4k\Omega$$

10) The output impedance of both of the individual output transistors is V_A/I_C. So first we must calculate the current each transistor is supplying. As each transistor has the same base voltage, each transistor will conduct the same amount of current. Taking the left hand side of the circuit….

$$I_o = \frac{V_{CC} - V_{CEon1}}{R} = 1.4mA$$

Each transistor conducts 1.4mA (incidentally making the total output current 2.8mA), making the output impedance of each transistor 100V/1.4mA=71kΩ. As the two output transistors are in parallel, then the total output impedance is 35.5kΩ.

The next part of the question asks us to calculate the output current for a variety of output voltages. The appropriate formula from the notes is as follows.

$$\frac{I_{C2}}{I_{C1}} = \frac{1+\frac{V_{CE2}}{V_A}}{1+\frac{V_{CE1}}{V_A}}$$

We know that I_{C1} = 1.4mA, V_{CE1} = 1V and V_{CE2} = 1, 3 or 5V and V_A = 100V.

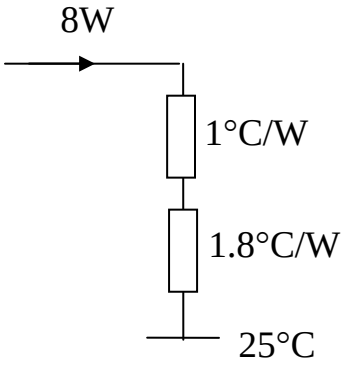
Hence $I_{C2} = \frac{1.4mA(1+1/100)}{(1+1/100)} = 1.4mA$ when V_o = 1V

$I_{C2} = \frac{1.4mA(1+3/100)}{(1+1/100)} = 1.43mA$ when V_o = 3V

$I_{C2} = \frac{1.4mA(1+5/100)}{(1+1/100)} = 1.46mA$ when V_o = 5V

Remember that we have another, identical output transistor Q3 also providing current. Hence the output currents are 2.8mA, 2.86mA and 2.92mA when V_o = 1, 3 and 5V respectively.

11) The equivalent circuit is as follows,

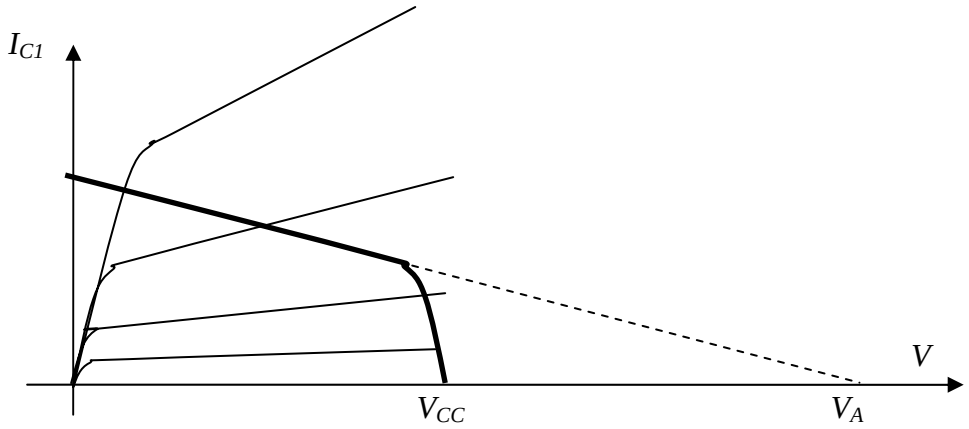


since both transistors contribute 4W of heat flow. The temperature of the BJTs is 47.4°C (note that the junction temperature, i.e. the active part of the BJT, is likely to be much hotter).

Difficult questions

12) $V_{bias} > 2V_{be\ on}$ since we need to ensure that the quiescent current is always greater than the current required to turn both transistors on. Hence the bias voltage must be greater than that required to turn both of the transistors on.

13) The output characteristic of Q1 is shown by the faint lines and the load line provided by Q2 is a thick line on the diagram below.



We now replace Q2 (and associated Q3) with a resistor. Our aim is to match the slope of the output characteristic of Q2 and the degree of I_c. Since the resistor obeys Ohm's law, it is fairly straightforward to determine the new supply voltage of the system as V_A, simply by definition of V_A. *Remember that V_A is the voltage for which the asymptote of the transistor output characteristic reaches zero current.*

14) The first thing to do is to decide on what the supply voltage is and then go from there.

We're given that 8W of power are dissipated into the load,

$$P = 8W = \frac{V_{RMS}^{\ 2}}{R_L} = \frac{V_{peak}^{\ 2}}{2R_L}.$$
$$\therefore V_{peak} = \sqrt{16R_L} = 11.3V$$

And $V_{CE\ ON}$ = 1V. So if the circuit has been properly designed, then the supply voltage should be just bigger than 11.3V+1V=12.3V. The question tells us that the minimum voltage is used here, so V_{CC} = 12.3V.

Now we know what the supply voltage is, the rest is relatively easy. We need to decide what level of current we will allow to flow through the output stage, we shall assume 100mW will be sufficient to safeguard the transistors (obviously we're making

assumptions here - other answers are admissible if you justify them).

Hence, $I_{S/C} = P_{S/C} / V_{S/C} = 100mA$.

Therefore, to get the transistor $Q_{S/C}$ to turn on at this current level we require R_E = 0.7V/100mA = 7Ω.