Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE118 Electronic Devices & Circuits 1

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

You may require the following:

Electronic charge, $e = 1.6\times10^{-19}$C

Permittivity of free space, $\varepsilon_0 = 8.85\times10^{-12}$ Fm^{-1}

Boltzmann's constant, $k = 1.38\times10^{-23}$ JK^{-1}

Planck's constant, $h = 6.6\times10^{-34}$ Js

Energy of a photon $= hc/\lambda$

Poisson's Equation $\dfrac{d^2V}{dx^2} = -\dfrac{ne}{\varepsilon}$

$$E = -\frac{dV}{dx}$$

$$W = \left[\frac{2\varepsilon V_o}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)\right]^{1/2}$$

$$J = eD\frac{dn}{dx}$$

$$J_0 = \frac{eL_e n_p}{\tau_e} + \frac{eL_h p_n}{\tau_h} \quad and \quad J = J_0\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

$n_p p_p = n_n p_n = n_i^2$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \gamma B$$

$$\partial p = \partial p_0 \exp\left(\frac{-x}{L_h}\right)$$

$$L = \sqrt{D\tau}$$

$$\sigma = ne\mu_e + pe\mu_h \qquad \rho = \frac{1}{\sigma}$$

$$C = \frac{\varepsilon A}{d}$$

$$D = \frac{kT}{e}\mu$$

Resistance $R = \rho L/A$

$v = \mu E$

For silicon: relative permittivity $\varepsilon_r = 12$ built-in voltage = 0.7 V

electron mobility = 0.07 m^2/Vs hole mobility = 0.045 m^2/Vs

band gap = 1.12 eV

1. This question is about diodes and some common circuits that contain diodes.

a. Figure 1a shows a peak detector circuit. The peak detector is driven by a sinusoidal input of much higher frequency than the time constant $R_1 \cdot C_1$, and has been running for a long time.

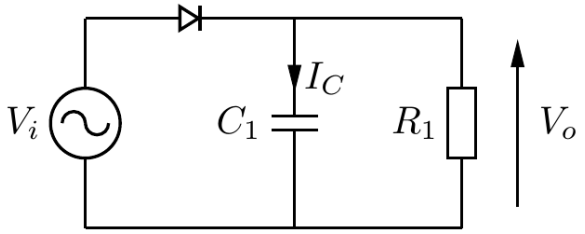

Figure 1a

i) On a single graph sketch, V_i, I_C and V_o over at least one full cycle of the sinusoidal input. **(6)**

ii) Describe the operation of the circuit over one full cycle. *Hint: Pay particular attention to the conduction state of the diode, the direction of current flow in the capacitor.* **(4)**

b. A peak detector can be connected to another circuit and the two combine to form a new circuit which acts as a voltage multiplier.

i) Sketch the circuit diagram of the voltage multiplier and label the components. **(3)**

ii) Name the additional circuit and indicate the components associated with it on the sketch. **(1)**

c. The circuit of figure 1b consists initially of R_1 and C_1. Sketch the V_o you would expect to observe in response to the 0V to 15V pulse input shown. The pulse width is 200 μs. Include on your sketch both the leading and trailing edge responses of the input pulse and label all time constants and peak voltages. **(4)**

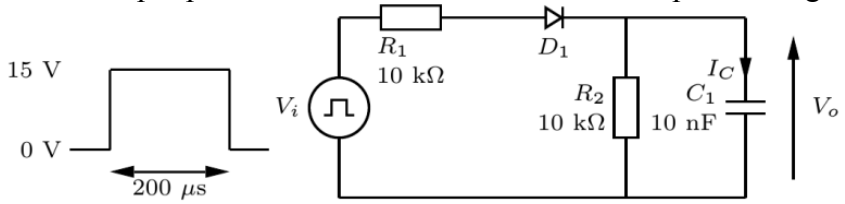

Figure 1b

d. A resistor, R_2 and an ideal diode, D_1 are now added to the circuit to form figure 1b. Sketch the I_C that you would expect to observe in response to the input shown in figure 1b. Label your sketch with peak values and time constants. **(6)**

2. **a.** Carefully sketch the I/V characteristic of a p-n junction diode showing both the forward and reverse bias and paying attention to the region around zero bias. Identify the reverse leakage current and the forward dynamic resistance in terms of the I/V slope at any particular bias. **(4)**

How does this resistance vary with forward bias? **(2)**

b. A silicon p-n diode forms the emitter-base junction of a p-n-p bipolar transistor and is doped as follows:

$p = 7x10^{25}\ m^{-3}, \quad n = 7x10^{23}\ m^{-3}$

Calculate the emitter injection efficiency. Assume that the current due to each carrier is proportional to the conductivity of the semiconductor from where it originates. **(4)**

Calculate the current gain if the base transport factor, $B = 1$. **(2)**

c. Describe the main contributing mechanism which results in the small reverse leakage current in a p-n junction? **(3)**

Would you expect the reverse biased leakage current to increase or decrease:

i. when using a semiconductor with an increased bandgap or bond strength? **(2)**

ii. at a lower diode temperature? **(2)**

d. The reverse leakage current in a p-n junction at room temperature is 1×10^{-6} A. What applied forward junction voltage will give a current of 1×10^{-2} A? In your calculation assume that the exponential term in the diode equation is >> 1. **(4)**

The actual measured voltage across the diode terminals required to give this current is 25 mV higher than the value calculated above. Explain why this happens? **(2)**

3. This question is about transistors both as switches and amplifiers.

a. Using the information provided in figure 3a find,

i) the load current, I_L, when the transistor has been on for a long time. **(1)**

ii) the energy stored in the inductor assuming the transistor has been switched on for a long time. **(1)**

iii) the power dissipated in the load when the switch is on. **(1)**

iv) the power dissipated in the switch when the switch is on. **(1)**

v) I_D, I_L and I_S immediately after the switch turns off. **(3)**

vi) V_{DS} immediately after the switch turns off. **(2)**

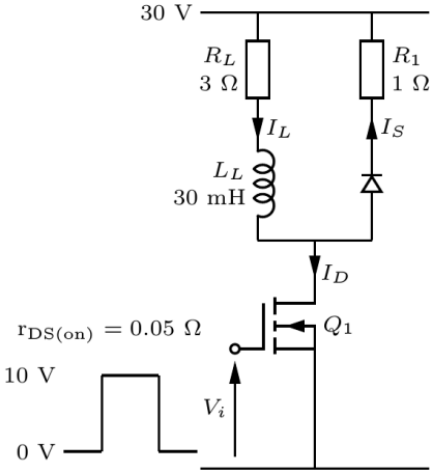

Figure 3a

b. **i)** For the amplifier in figure 3b calculate the quiescent value of V_B, V_C, I_C and the small signal parameters g_m and r_{be}. Assume that the transistor V_{BE} is 0.7 V in the forward active region and β = 700. State any other assumptions clearly. **(5)**

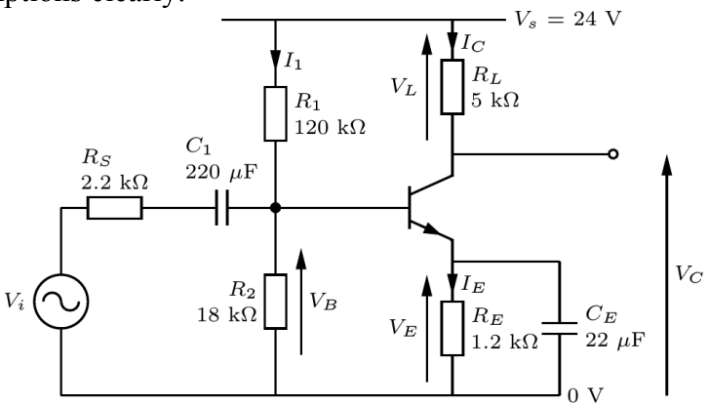

Figure 3b

ii) Sketch a graph showing V_C, V_B, V_E, the power supply voltage and the reference (0 V) over several cycles of the sine wave input siganal. Assume that the amplifier is being driven to the point of 'clipping', where the peak to peak AC voltage swing on the collector, V_C, is as large as possible without significant distortion. **(4)**

iii) Calculate the quiescent V_C for this amplifier which will maximise the possible collector voltage signal swing. **(2)**

c. **i)** Draw a small signal equivalent circuit for the amplifier in figure 3b. **(4)**

ii) Evaluate the input resistance in the 'mid-band' i.e. where all of the capacitors are short circuit. *Hint: R_S is the source resistance and does not form part of the input resistance.* **(1)**

4. **a.** i. Using sketches briefly describe the operation of the n-channel JFET and n-channel MOSFET planar devices. You should highlight the main differences between the two, including how the gate bias controls the drain current in each case. **(14)**

ii. Identify the 'on' and 'off' gate bias conditions for each when operated as a switch. **(4)**

b. i. Using data and equations from page 1 calculate the time it takes for an electron to travel underneath a 1 μm long gate in an n-channel Si MOSFET. You should assume a lateral electric field of 5×10^6 Vm^{-1} under the gate region. **(4)**

ii. Why is this delay time important when designing high frequency or fast switching MOSFETs? **(3)**

5. **a.** Boron (group 3) is used to dope a piece of silicon semiconductor to a concentration of 1 x 10^{24} m^{-3}. Explain on an atomic scale why this results in p-type material with a hole produced for every boron atom introduced into the lattice. **(6)**

b. Will the hole concentration change significantly as the temperature is increased by 50 ^{o}C above room temperature? Under the same temperature increase will the fractional change in charge carriers be higher for intrinsic (undoped) material? Justify your answers. **(4)**

c. Calculate the concentration of minority electrons in this material (n_i =1 x 10^{16} m^{-3} for silicon at room temperature). **(3)**

d. What is the conductivity resulting from this doping? **(3)**

e. Compare this with the conductivity component due to the minority electrons **(3)**

f. Calculate the resistance between opposite faces of a cube of 1 mm edge dimension made from this doped silicon. **(3)**

g. What is the resistance between the end faces of a cube where the edge dimension is doubled? **(3)**

6. **a.** Draw the circuit symbol for an opamp and label,

i) The inverting input. **(1)**

ii) The non-inverting input. **(1)**

iii) The output. **(1)**

iv) The power supplies. **(2)**

b. Draw an opamp circuit containing a "virtual earth". Describe the term and explain how it is maintained. **(6)**

c. The circuit in figure 6a is a transimpedance amplifier.

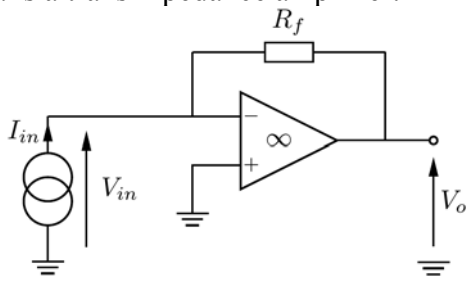

Figure 6a

i) What function does the transimpedance amplifier perform? **(1)**

ii) Derive an expression for $\frac{V_o}{I_{in}}$ assuming A_v is infinite. **(3)**

iii) The input resistance is given by $\frac{V_{in}}{I_{in}}$. Show that $R_{in} = \frac{R_f}{A_v}$ when A_v is finite **(5)**

d. **i)** Show that V_o in figure 6b is given by $V_o = V_2 - V_1$ **(4)**

ii) Suggest a suitable name for this circuit **(1)**

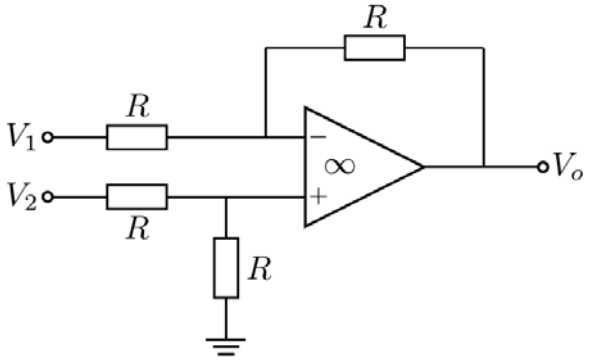

Figure 6b

PAH / JEG/JPRD