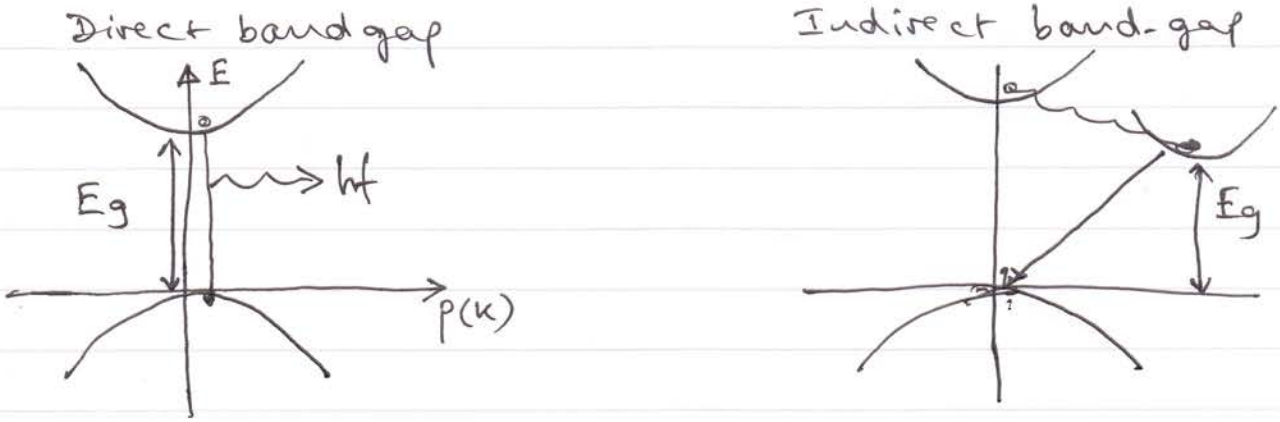
EEE225 Semester 2 2017 Semiconductors

Q7: 4 out of the following:

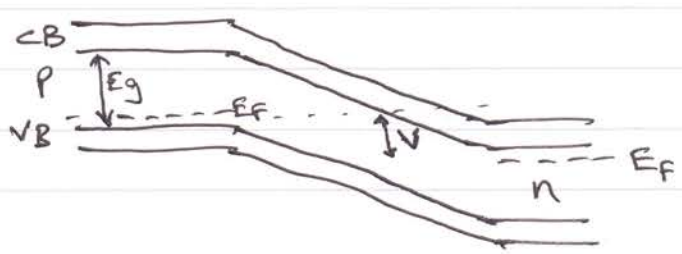
High bandwidth
Low attenuation
Light weight
No EM interference
Immune to tapping / secure
No cross-talk
Cheap
Physically tough (4)

Q8:



Direct band gap - recombination occurs at $p(k) = 0$ so photons emitted. In indirect band-gap, a phonon event is involved before an electron in the conduction band can recombine with a hole. No photon is emitted. (4)

Q11(i)



V is the difference between Fermi levels of the p and n-type regions. (6)

EEE 225 Semester 2, 2017

Q1(iii) Resistivity of intrinsic Si = $5\times10^{3}\ \Omega m$

$$\sigma = \frac{1}{5\times10^{3}} = 1.6\times10^{-19}(0.12+0.05)n_i$$

From this, $n_i = 7.3\times10^{15}\ m^{-3}$

When doped n-type conductivity increases 10^4 times

$$\sigma_n = \frac{10^4}{5\times10^{3}} = 1.6\times10^{-19}\times 0.12\times n \quad \text{(can ignore holes)}$$

From this, $n = 10^{20}\ m^{-3} = N_d$

To change this n-type to p-type we need to dope to a level $> 10^{20}\ m^{-3}$ (ignore intrinsic carriers) (6)

To make it p-type, you need to dope with acceptors. (1)

iv) $\sigma_p = 10\sigma_n = \frac{10^{5}}{5\times10^{3}} = 1.6\times10^{-19}(0.05)p$ (ignoring electrons contribution to σ_p)

From this, $p = 2.5\times10^{21}\ m^{-3} \simeq N_A$

Electron concentration here $= \frac{n_i^2}{p} = \frac{(7.3\times10^{15})^2}{2.5\times10^{21}}$

$= 2.25\times10^{10}\ m^{-3}$ (5)

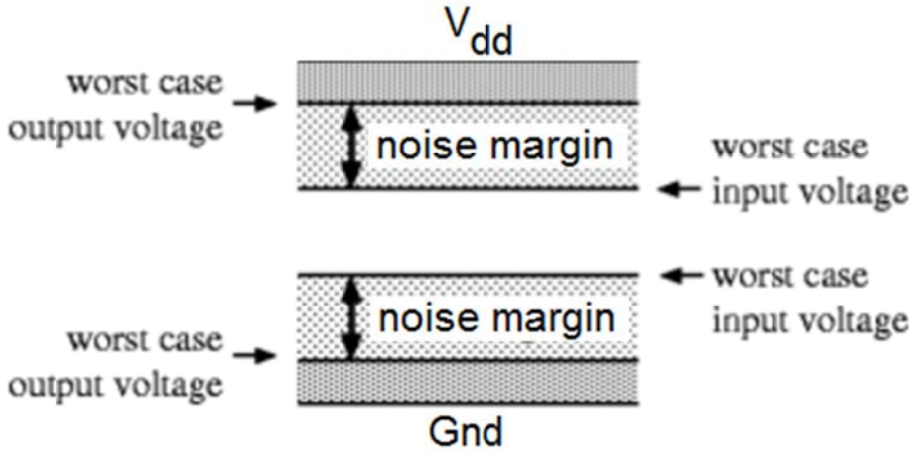
v) Longest wavelength = $1.24/1.1 = 1.127\ \mu m$

Longer wavelengths have an energy less than the bandgap so will not create e-h pairs. (2)

EEE225 Analogue and Digital Electronics 16/17 Digital Solutions

1. **Fan-out**: the maximum number of standard loads that can be connected to the output of a logic gate without degrading its normal operation. **(2)**

Noise Margin: the level of noise that can be tolerated on an output before it is not recognized as a valid logic level by an input. The HIGH and LOW level noise margins can be calculated from the voltages indicated in the diagram below. **(2)**

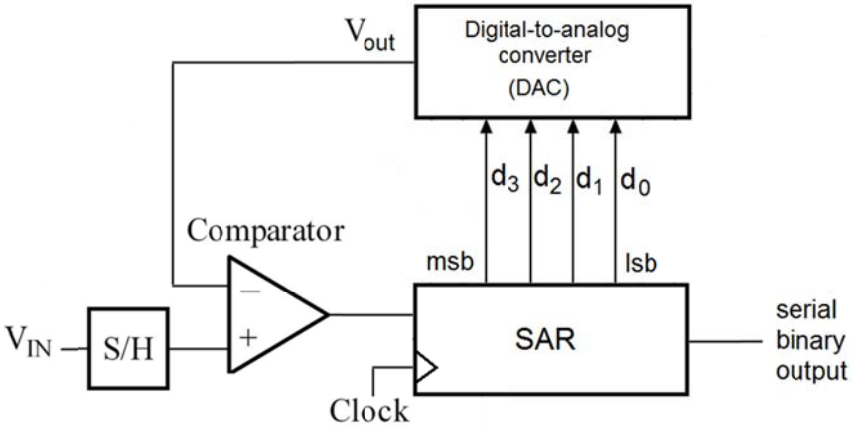


2. **a.** Both inputs LOW; both diodes are reverse biased and hence cut-off, the output Q will thus be LOW. The cases where one or both inputs are 5V; at least one of the diodes will be forward biased and conducting with a forward volt drop of about 0.7V giving about 4.3V at the output.

A B	A.B
0 0	LOW
0 1	HIGH
1 0	HIGH
1 1	HIGH

This is the OR function. **(4)**

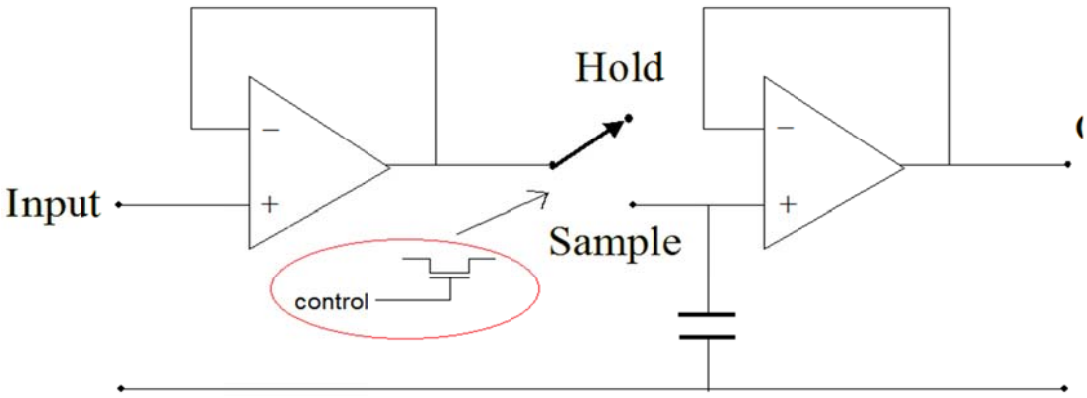
3. a.



Starting with the msb, each input to the DAC is set to a '1' one at a time in decreasing order of significance. For each setting, the DAC produces an output V_{out} which is compared with the input voltage V_{in}. If $V_{out} > V_{in}$ the comparator will give a high output and the set bit in the register is retained. When all bits have been tried, the conversion is complete. **(4)**

9. a. Aliasing is an effect which occurs in a sampled system where frequencies higher than the Nyquist frequency are present. An alias is an unwanted frequency that is not part of the original waveform. **(3)**

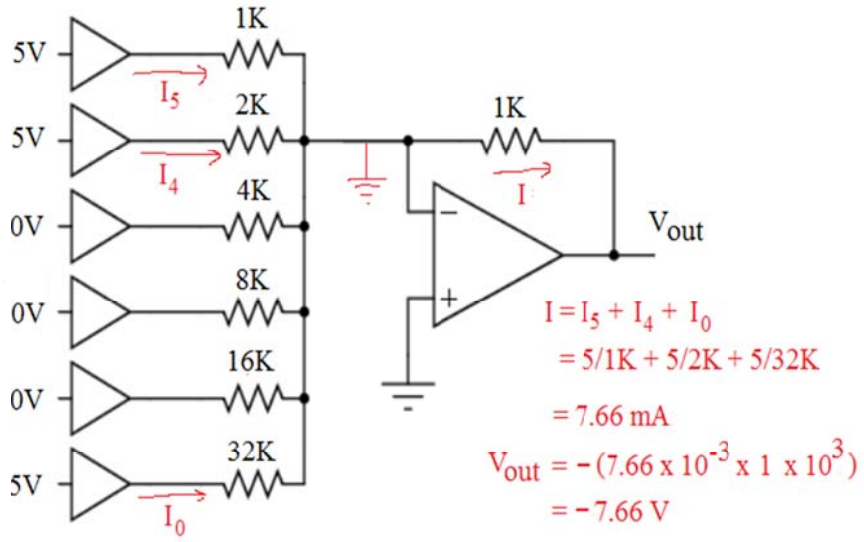
9.



An anti-alias filter is required to restrict the signal bandwidth to satisfy the sampling theorem. The input from the anti-alias filter is buffered by a op-amp configured as a unity-gain voltage follower. The sampled value must be held constant until the next sample occurs in order for the ADC to have sufficient time to convert the sample to the digital format. The voltage will be held on the capacitor until the next pulse due to the high input impedance of the buffer before the output. **(5)**

b. The resistor network has values that are inversely proportional to the binary weightings of the inputs. There is practically no current flowing into the inverting input of the op-amp which is a virtual ground (0V). Thus, the sum of the input currents will flow through the op-amp feedback resistor and hence the output **(4)**

voltage will be proportional to the sum of the binary weights.



correct currents **(1)**, correct value for I **(1)**, correct Vout **(1)**, negative **(1)** **(4)**

(4)

The disadvantage of this method is the number of different resistor values required. For say, a 12 bit converter, 12 resistors in the range R to 2048R would be required. Tolerance required would be 1 part in 4095 (0.0244%). It is difficult to mass produce these resistors within the required tolerance.

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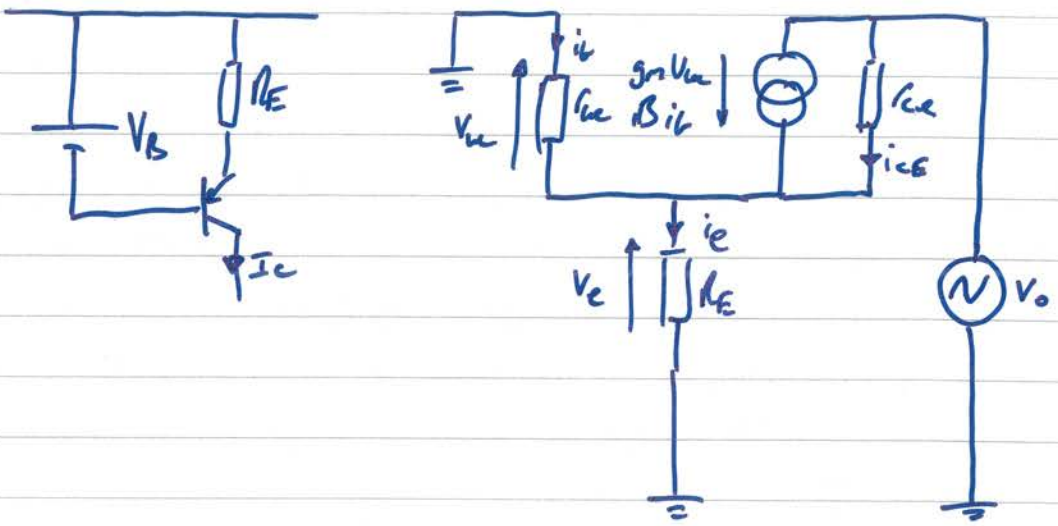
4a



1 FOR DIAG.

SUM CURRENTS AT THE EMITTER:

$$i_b + g_m V_{be} + i_{ce} = i_e$$

$$\frac{V_{be}}{r_{be}} + g_m V_{be} + \frac{V_o - V_e}{r_{ce}} = \frac{V_e}{R_E}$$

BUT $V_e = -V_{be}$ SO ELIMINATE V_e ...

$$-\frac{V_o}{r_{ce}} = V_{be}\left[\frac{1}{r_{ce}} + g_m + \frac{1}{r_{be}} + \frac{1}{R_E}\right] \quad (1)$$

(1)

SUM CURRENTS AT THE OUTPUT NODE.

$$i_o = g_m V_{be} + i_{ce}$$

$$i_o = g_m V_{be} + \frac{V_o - V_e}{r_{ce}}$$

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AGAIN $V_e = -V_{be}$, COLLECT IN V_{be}:

$$V_{be} = \frac{i_o - \frac{v_o}{r_{ce}}}{\frac{1}{r_{ce}} + g_m} \qquad (2)$$

(2) → (1):

$$\frac{v_o}{i_o} = r_{ce}\left[\frac{\frac{1}{r_{be}} + g_m + \frac{1}{r_{ce}} + \frac{1}{R_E}}{\frac{1}{r_{be}} + \frac{1}{R_E}}\right]$$

$$= r_{ce}\left[1 + \frac{g_m + \frac{1}{r_{ce}}}{\frac{1}{r_{be}} + \frac{1}{R_E}}\right] \qquad (1)$$

$g_m \gg \frac{1}{r_{ce}}$ SO:

$$r_o \simeq r_{ce}\left[1 + g_m (r_{be} /\!/ R_E)\right] \qquad (1)$$

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Q6

THIS IS A NEW STYLE OF QUESTION, BUT IT IS FAMILIAR TERRITORY IN TERMS OF THE OPAMP AS A FIRST ORDER SYSTEM.

THE QUESTION IS CONSIDERABLY EASIER THAN IT APPEARS!

$$A_V = A_0 \cdot \frac{1}{1+s\tau} \qquad (s = j\omega)$$ (1)

AT DC; $\omega = 0$... SO NO NEED TO WORRY ABOUT ALL THE FREQUENCY DEPENDANCE STUFF. AT $\omega = 0$ $A_V = A_0$! (1) FOR MENTAL "LEAP"

$$\frac{V_o}{V_i} = G = \frac{1}{\frac{1}{A_V} + \frac{R_2}{R_1 + R_2}}$$

ISOLATE FOR A_V:

$$A_V = -\frac{G(R_1 + R_2)}{GR_2 - R_1 - R_2}$$ (1)

$$= \frac{-496(250\text{K} + 500)}{496 \cdot 500 - 250\text{K} - 500}$$

$$= \underline{\underline{49699.2}} \simeq 50 \times 10^3$$ (1)

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Q5

a) SINCE THE GAIN IS GIVEN IN LOG (dB) WE CAN JUST ADD THEM.

$$A = 25\,dB + 15\,dB$$
$$= 40\,dB.$$

(1)

b) NOISE FACTOR IS LINEAR VERSION OF NOISE FIGURE...

NOISE FIGURE, $NF = 10\log(F)$ IF F IS THE NOISE FACTOR. SO.

$$F = 10^{NF/10}$$

$NF = 4.5dB \rightarrow F = 2.82.$

$NF = 7\,dB \rightarrow F = 5.01$

(1) BOTH

c) THE NOISE FACTOR OF A CASCADE OF TWO MATCHED AMPLIFIERS WITH INDIVIDUAL GAINS AND NOISE FACTORS A_{p1}, F_1 AND A_{p2}, F_2 IS:

(1)

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{A_{p1}} = 2.82 + \frac{4.01}{316.2}$$

$$= 2.83$$

$$NF_{TOTAL} = 10\log(2.83) = 4.52\,dB.$$

(1)

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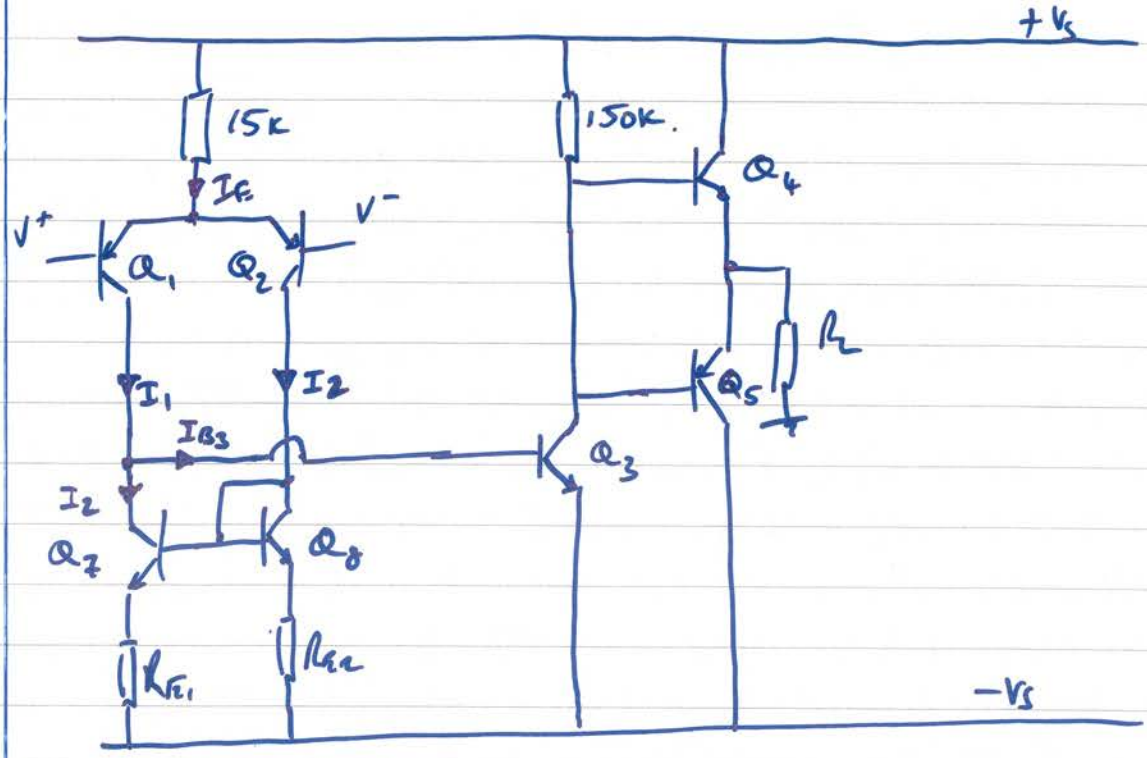
10 a i) THE MIRROR CIRCUIT CAN BE ADDED TO THE OPAMP IN FIGURE 10.



(3)

R_{E1} & R_{E2} OPTIONAL FOR THE MARK.

- SUPPOSE Q_1'S BASE IS SLIGHTLY POSITIVE W.R.T. Q_2'S BASE... BY AN AMOUNT ΔV (1)
- THEREFORE I_1 WILL BE REDUCED BY ΔI

$$I_1 = I_{E/2} - \Delta I.$$ (1)

- BY SIMILAR LOGIC I_2 IS SLIGHTLY INCREASED BY ΔI

$$I_2 = I_{E/2} + \Delta I.$$ (1)

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- THE MIRROR TRIES TO MAKE $I_2 \simeq I_1$ (WITH A SMALL OFFSET DUE TO $\beta \neq \infty$) (1)

- SUMMING CURRENTS AT Q7's COLLECTOR...

$$I_{B3} \simeq I_1 - I_2$$

$$\simeq \frac{I_E}{2} - \Delta I - \left(\frac{I_E}{2} + \Delta I\right)$$

$$= -2\Delta I. \quad (1)$$

- IN OTHER WORDS THE MIRROR EFFECTIVELY DOUBLES THE 'GAIN' OF THE DIFFERENTIAL AMPLIFIER COMPARED TO USING A RESISTIVE LOAD. (1)

ii)
- DOUBLES THE 'GAIN' OF THE STAGE.
- IMPROVES OUTPUT OFFSET BY REDUCING THE DC ERROR PRODUCED BY THE BIASING CURRENT OF Q_3
- TRANSISTORS TAKE UP LESS SPACE ON THE DIE.
- TRANSISTORS WILL BE MADE AS A MATTER OF COURSE. RESISTORS NEED EXTRA PROCESSING STEPS
- RESISTORS MAY HAVE TO BE LASER TRIMMED
- THE TOTAL CURRENT AVAILABLE TO CHARGE CCB OF Q_3 IS APPROXIMATELY DOUBLED SO THE SLEW RATE WILL BE IMPROVED

ANY (4)

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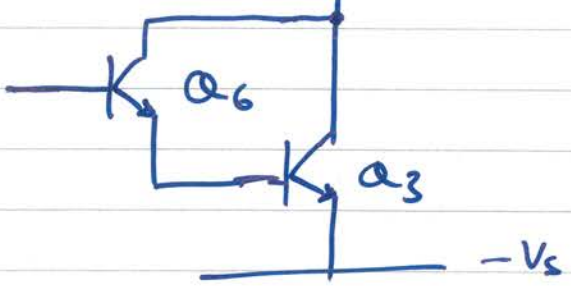
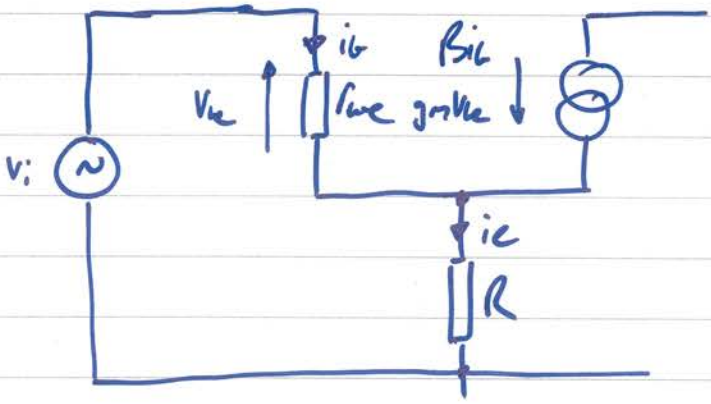
(10b) i



(1)

ii) SMALL SIGNAL MODEL:



(1)

- THE INPUT RESISTANCE OF Q_3 IS "R"...

SUM CURRENTS AT THE EMITTER.

$$i_e = i_6 + \beta i_6$$

$$\frac{V_e}{R} = \frac{V_{be}}{r_{be}} + g_m V_{be}$$

(1)

SUM VOLTAGES AROUND THE INPUT LOOP.

$$V_i = V_{be} + V_e$$

(1)

$$\frac{V_{be}}{r_{be}} + g_m V_{be} = \frac{V_i - V_e}{R}$$

(1)

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Q10bii CONTINUED...

$$V_{be} + \left(\frac{1}{r_{be}} + g_m + \frac{1}{R}\right) = V_{in}/R$$

$$i_b r_{be}\left(\frac{1}{r_{be}} + g_m + \frac{1}{R}\right) = V_{in}/R$$

$$r_i = \frac{V_b}{i_b} = \left(1 + g_m r_{be} + \frac{r_{be}}{R}\right) R \qquad (1)$$

A STANDARD EXPRESSION FOR g_m...

$$g_m = \beta / r_{be}$$

← THIS IS GIVEN ON THE EXAM SHEET

So $r_i = (R + \beta R + r_{be})$

IF $\beta >> 1$ $r_i = r_{be} + \beta R$

AND R IS INPUT RESISTANCE OF Q_3 WHICH IS r_{be_3} SO WE HAVE

$$r_i = r_{be_6} + \beta_6 \cdot r_{be_3} \qquad \text{Q.E.D} \qquad (1)$$