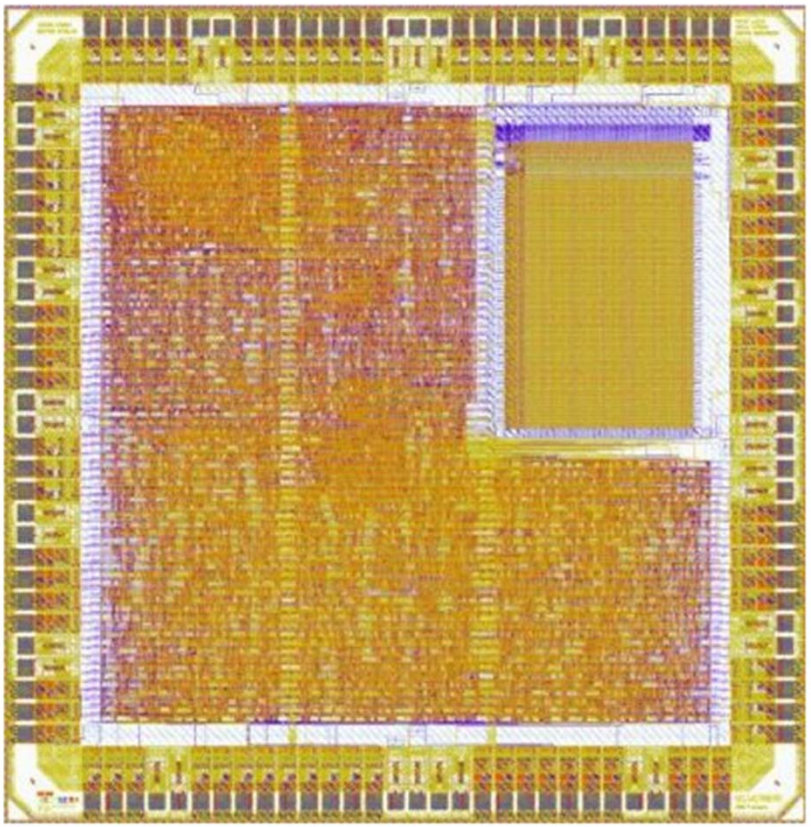
Memory Structures

- SRAM
- DRAM
- DDR Memory

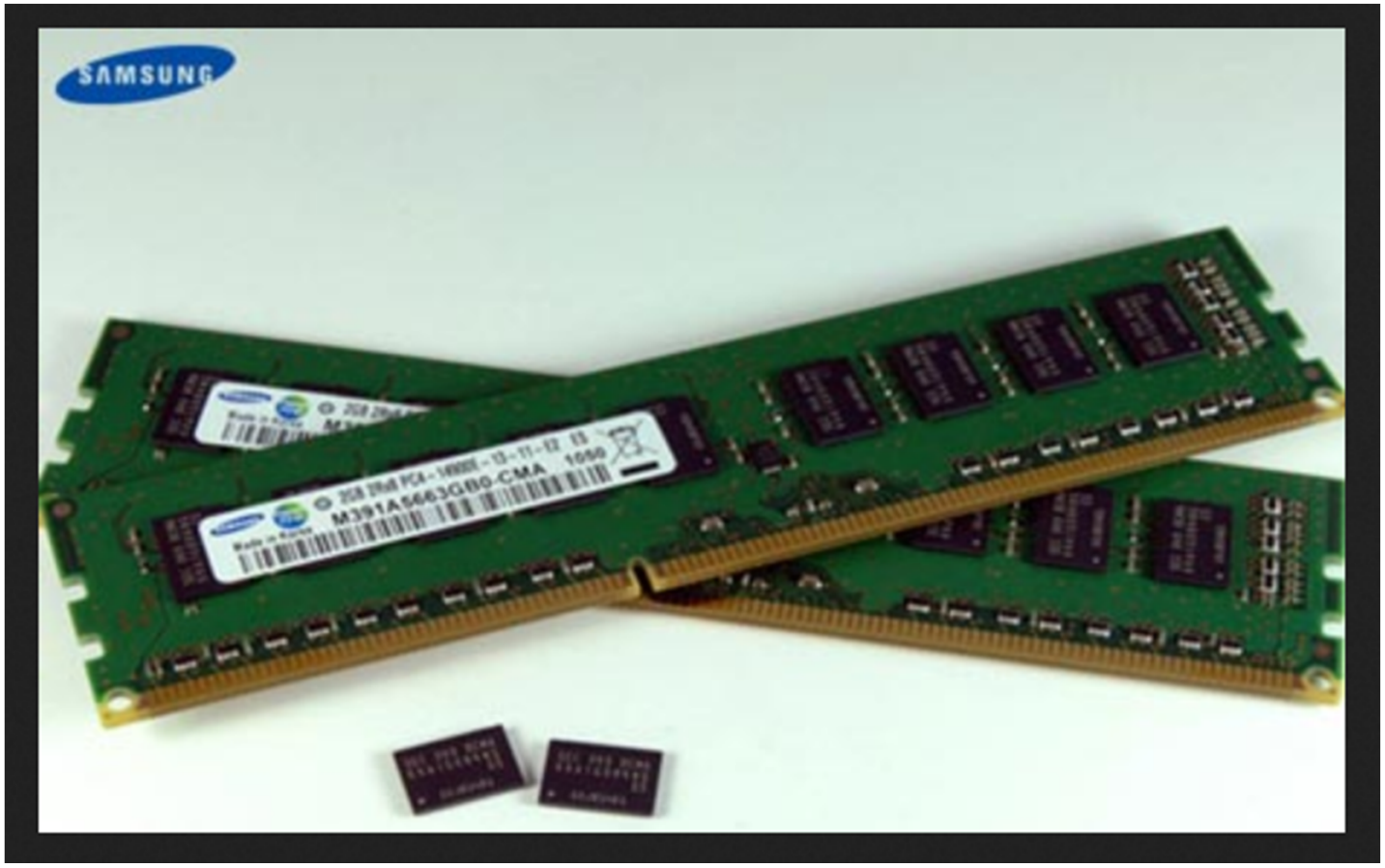
SRAM Applications

- Embedded RAM for ASICs
- Configuration Bits for FPGAs
- CPU cache memory

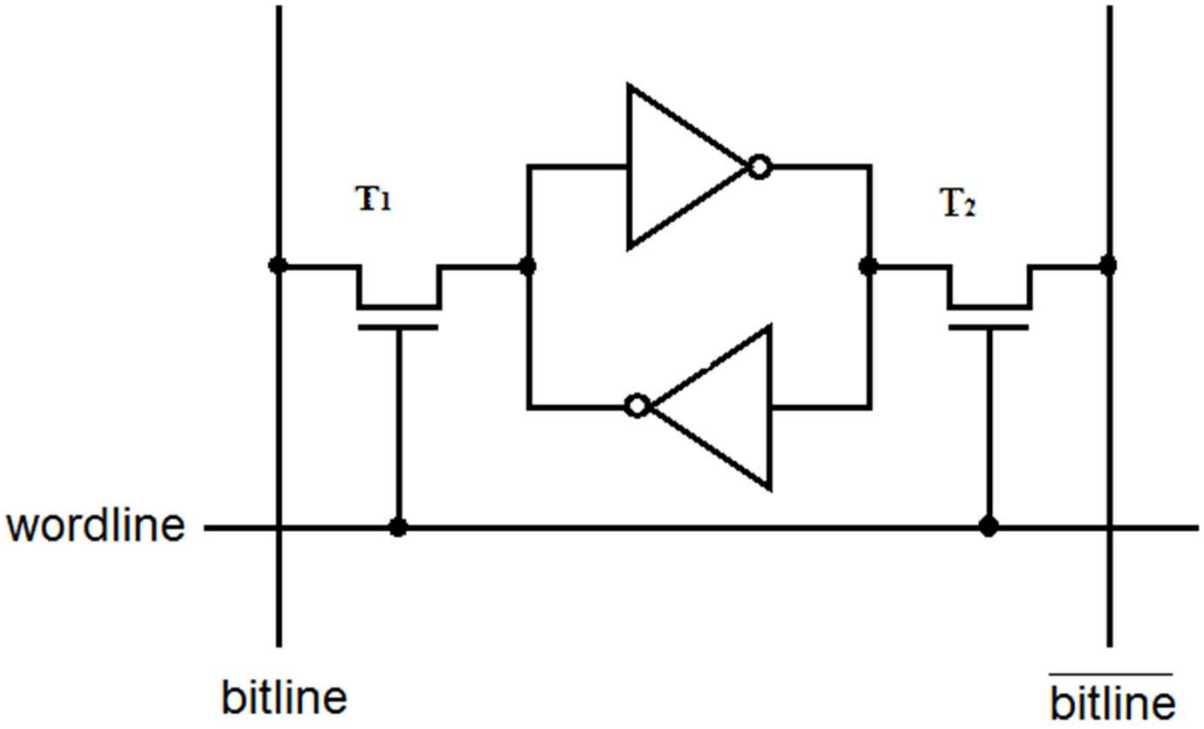


DRAM - Applications

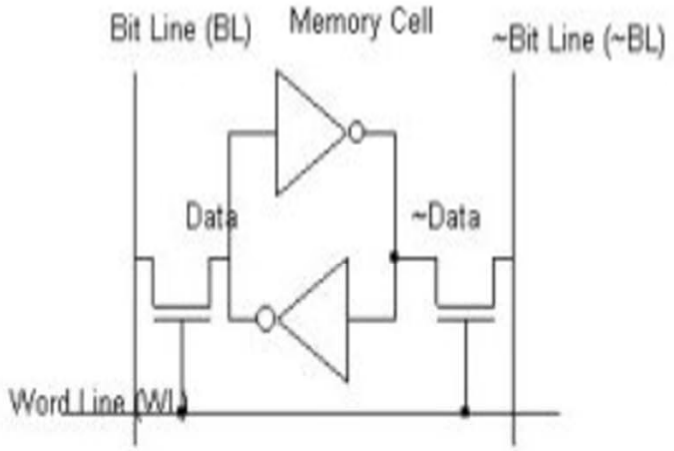
- Main memory desktops, laptops, workstations



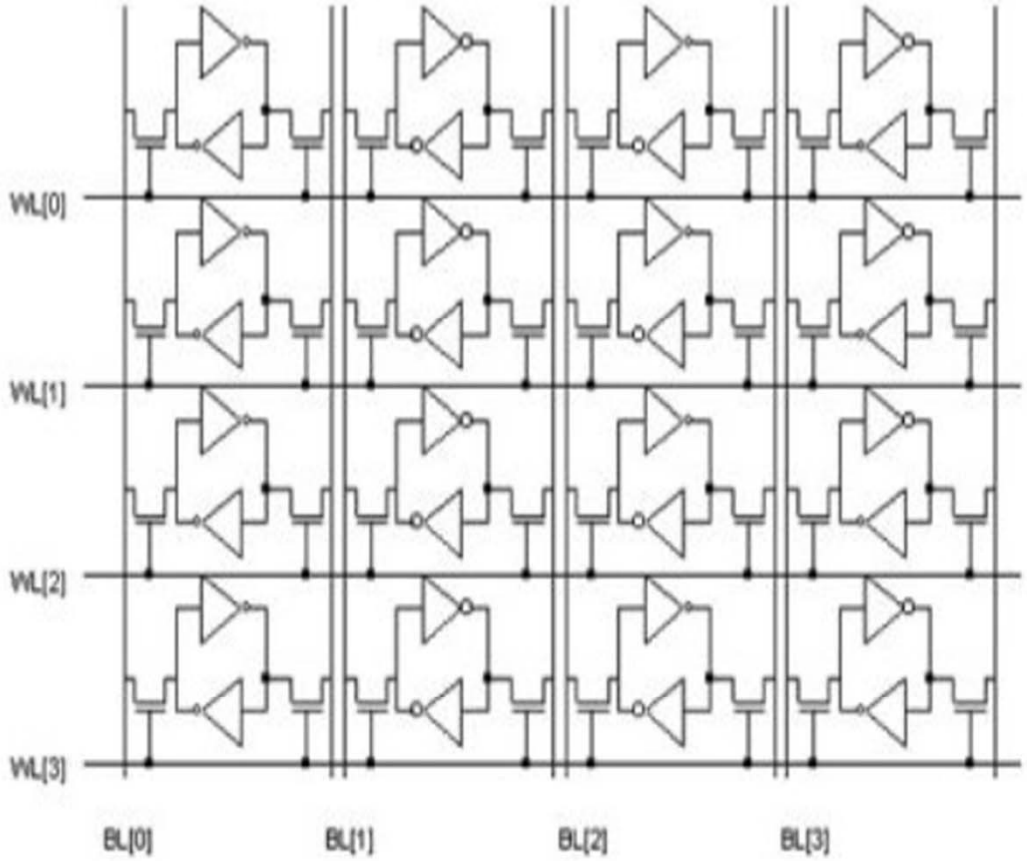
SRAM Cell



Consists of cross coupled inverters – more compact than a D-Type flip-flop.
A memory controller on the memory chip handles the complexity of writing and reading data leaving a simpler interface to the user.

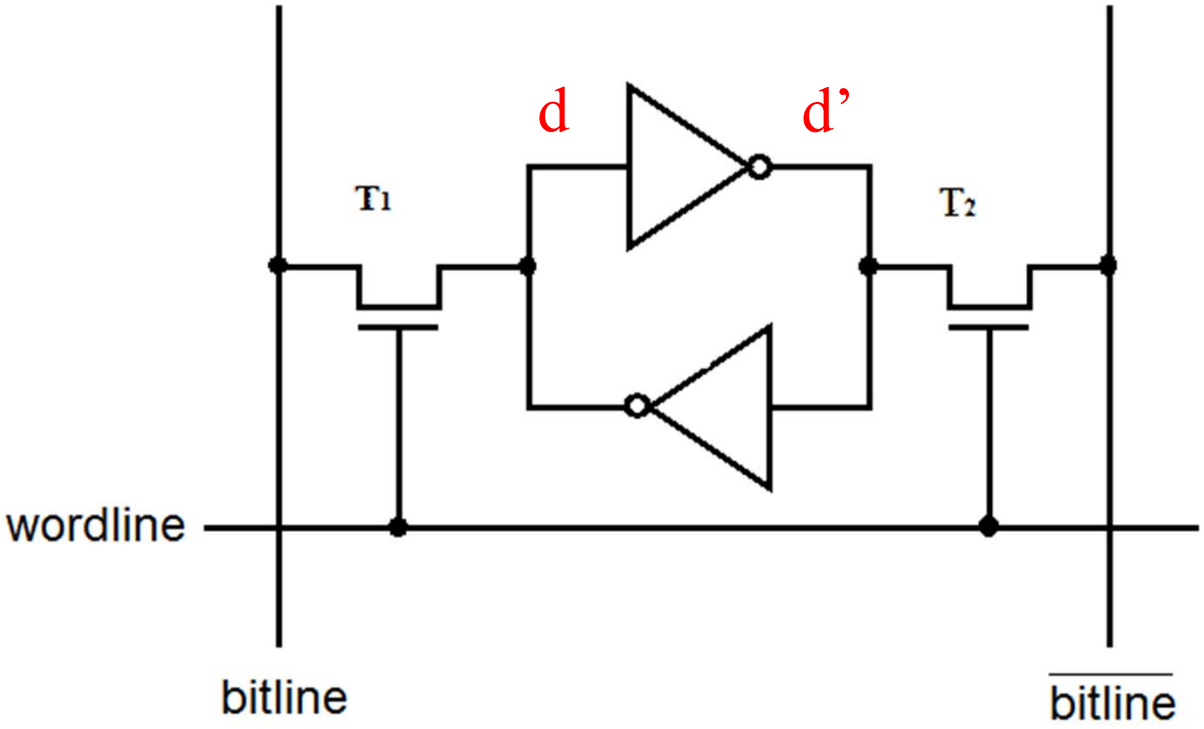


6T SRAM CELL



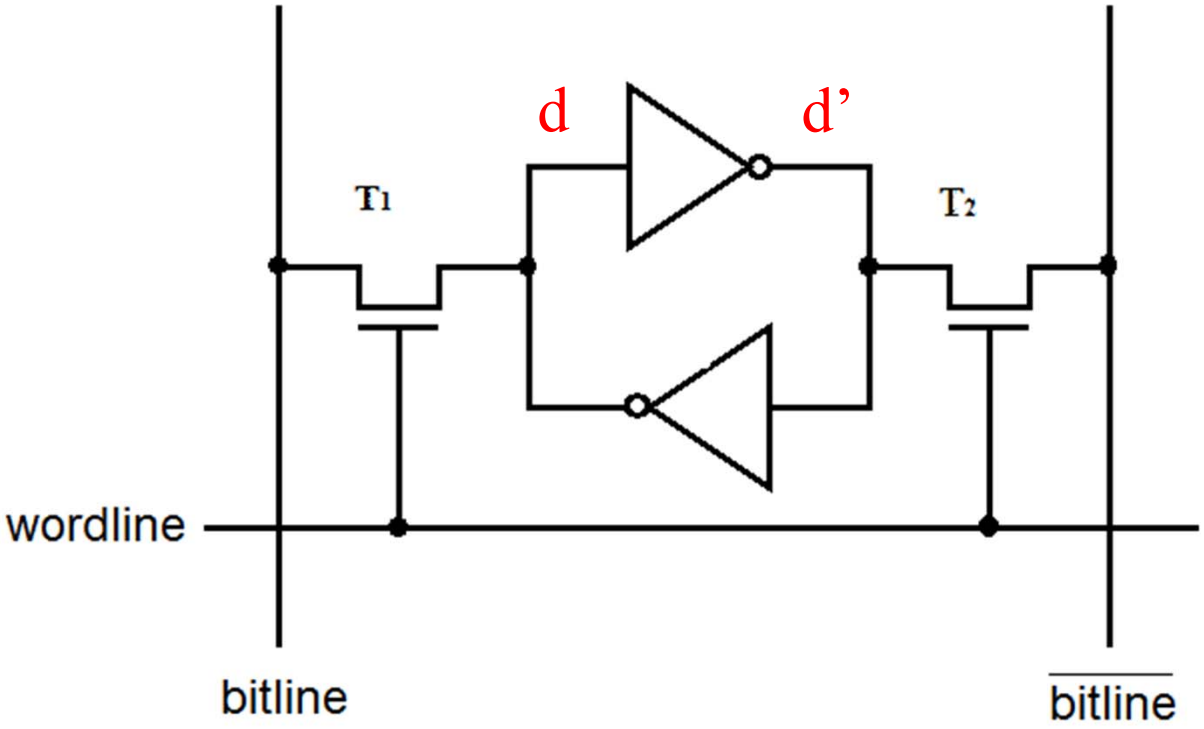
4 x 4 SRAM Memory Array

SRAM Cell WRITE

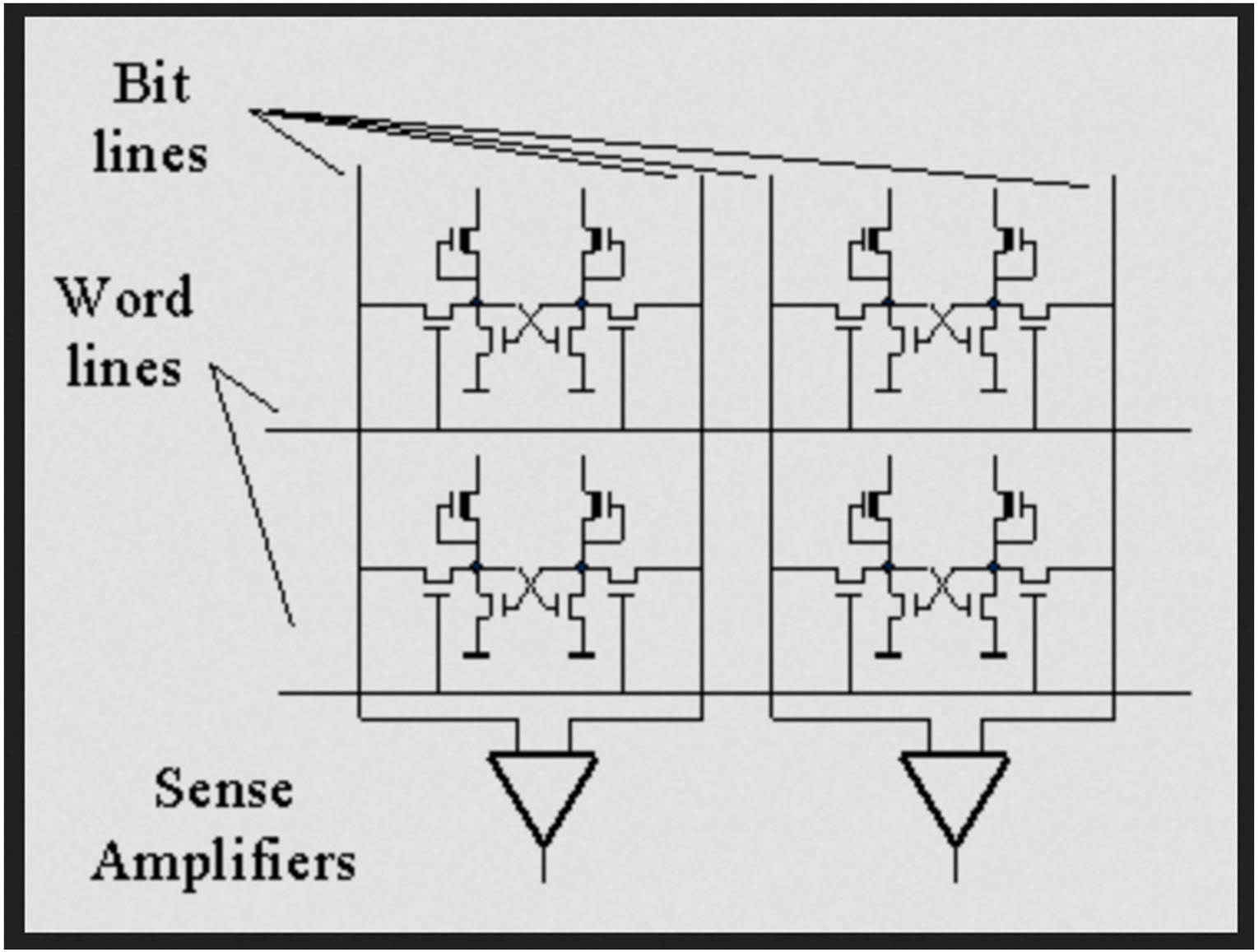


To write to the cell, *bitline* is set to the required data value and $\overline{bitline}$ is set to the complement. The controller then sets wordline = 1 which turns on transistors T1 and T2. The data values then appear in the inverter loop overwriting any previous value.

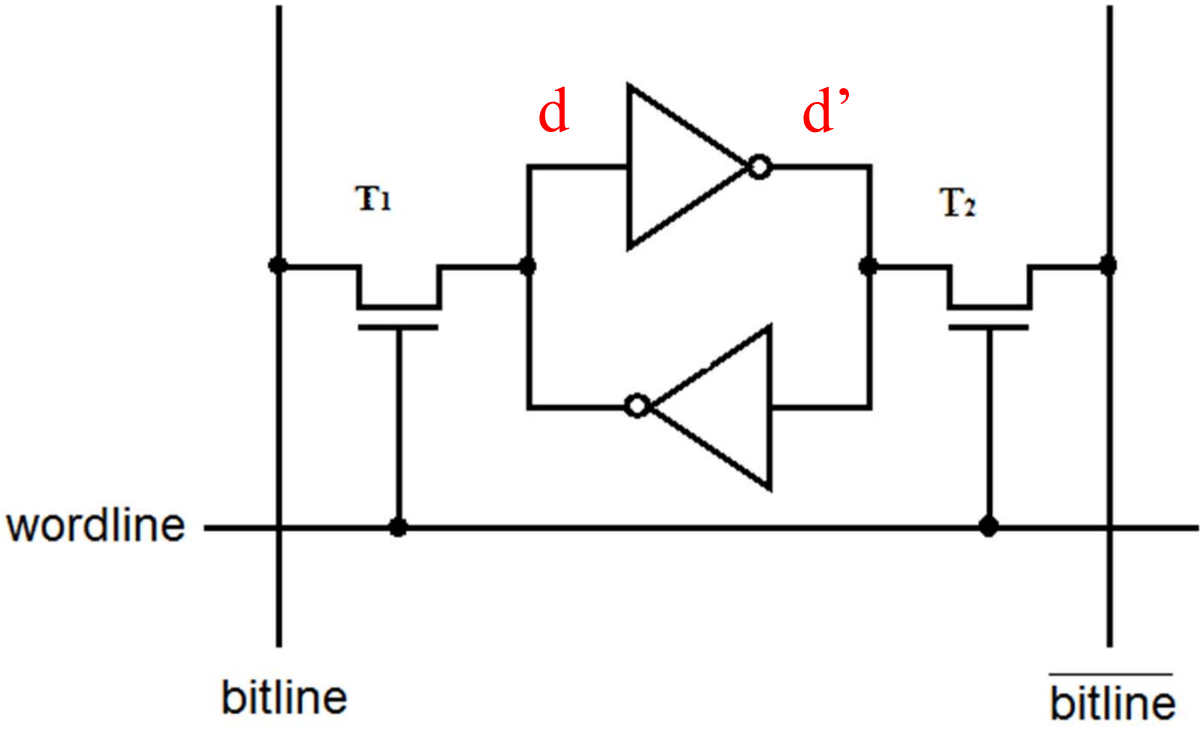
SRAM Cell READ



To read from the cell, *bitline* and $\overline{bitline}$ are both precharged to 1. Wordline is then set to 1. One of the enabled transistors will have a 0 at one end which will cause the corresponding precharged 1 to drop to a slightly lower voltage than a normal 1. Both of the bitlines are connected to a ***sense amplifier*** which can detect this variation.


Bit lines
Word lines
Sense Amplifiers

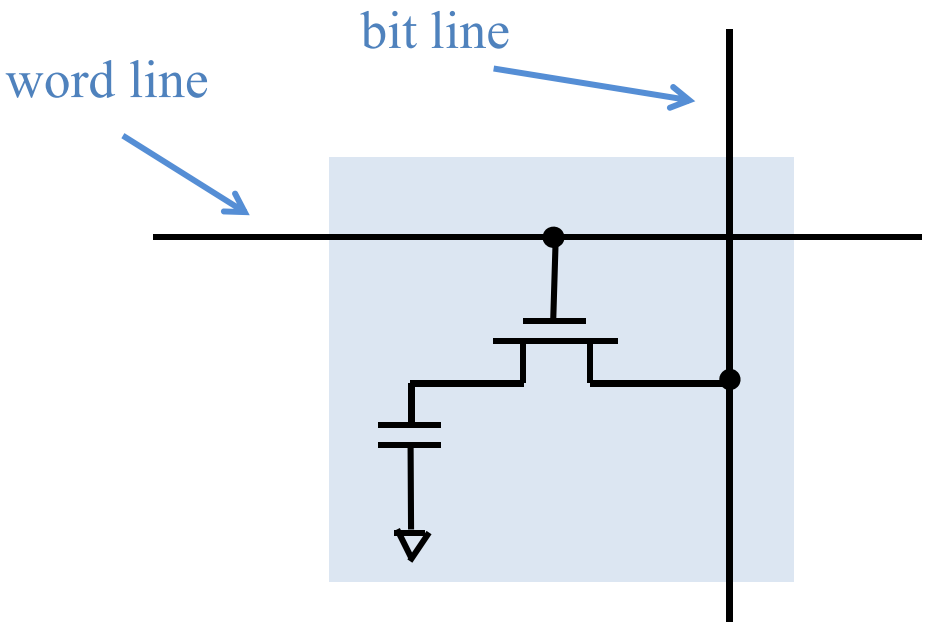
SRAM Cell READ



If the voltage on *bitline* is slightly higher than $\overline{bitline}$ then a logic 1 is stored.

If the voltage on $\overline{bitline}$ is slightly higher than *bitline* then a logic 0 is stored.

Dynamic RAM structure



1-bit DRAM cell
Information stored on small capacitor accessed through a MOS transistor

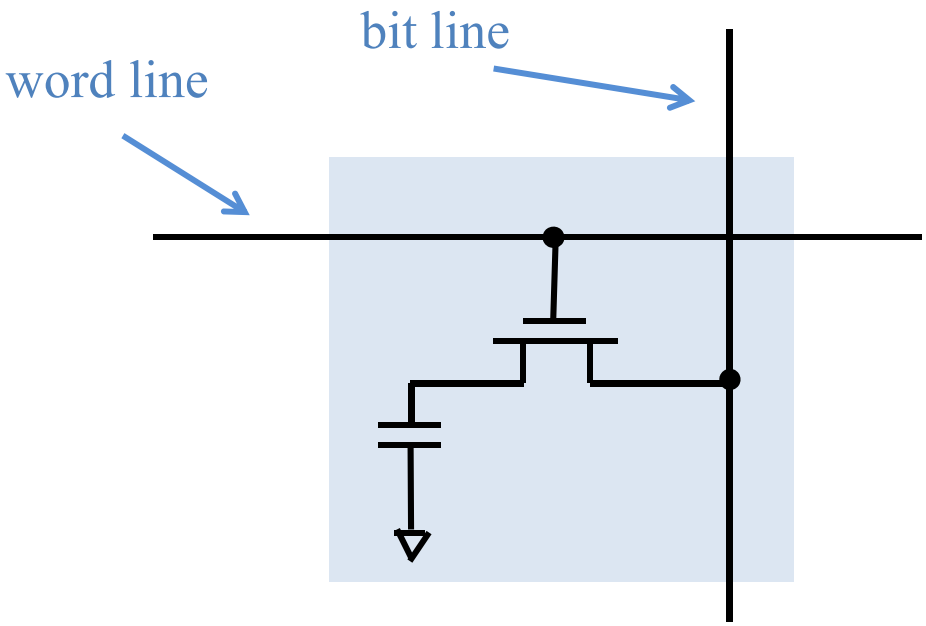
WRITE

Access by setting the word line HIGH

To store a ‘1’ access cell, set the bit line HIGH, capacitor will charge

To store a ‘0’ access cell, set the bit line LOW, capacitor will discharge

Dynamic RAM structure



1-bit DRAM cell
Information stored on small capacitor accessed through a MOS transistor

READ

Precharge bit line to a voltage halfway between HIGH and LOW

Set wordline HIGH, precharged bit line will be pulled slightly higher or lower dependent on capacitor charge. Sense amplifier detects this and recovers ‘1’ or ‘0’

DRAM – The original DRAM used in PCs was asynchronous. Once a memory access is started, it finishes a certain period of time later. It is only suitable for slower memory bus systems.

SDRAM – Synchronous DRAM is synchronized to the system clock. This allows tighter control of the timing and improved performance.

SDR SDRAM – Single data rate SDRAM can transfer one data word per clock cycle.

DDR SDRAM – Double data rate SDRAM can transfer two data word per clock cycle. It achieves this by transferring data on both the rising and falling edge of a clock cycle.

DDR4 – There have been several generations of DDR memory each having performance improvements over the previous generation. DDR4 is expected to have mass adoption by 2015.