Examination Feedback for EEE310/6036 – (Introduction to) VLSI Design
Spring Semester 2009-10

Feedback for EEE310/6036 Session: 2009-2010

General Comments:

The general level of understanding was lower than I expected. A number of people, in some cases, presented answers that were a long way off the mark.

Question_1:

This question was very well answered and *most* people seemed to understand what was happening. Two points, however: if the question says that you cannot cut any wires to add a transistor then don't do it – you can only add transistors in parallel with the existing circuitry; secondly, once you've drawn a full circuit – if the pull-up and pull-down networks do not tally then the circuit must be wrong.

Question_2:

Most people could manage the proof for the power consumption and distinguish between static and dynamic power consumption. However, fewer people could recognize that because power is quadratically dependent on V_{DD} then this must be a good approach (especially as constant scaling rules means that reducing power supply voltage is necessary when scaling). Fewer people still recognized that the fact that V_T cannot be reduced for leakage reasons is making this more problematic.

The final part was more difficult that people seemed to realize. Probability of state change at input means that α is 0.25 for the inputs. For the output the effective value of α depends on the probability of being in a state e.g. 0 and this is 0.25 for a NAND gate with random inputs and the probability of there being a state change from 0 to 1 (i.e. either input changing – with probability 0.25). So, P0→0 = 0.75*0.75 0.5625 and P0→1= 1 – 0.5625 = 0.4375. So probability of a transition will be 0.25 * 0.4375 = 0.109. Clearly, the same is true for a 1 changing to a 0. P1=0.75, and P1→0 = 0.145. Thus probability of a transition is 0.75 * 0.145 = 0.109. Based on this, α for the output is 0.0547. Each has to be dealt with separately. Some people recognized this complexity but could not deal with it.

Question_3:

Surprisingly, some people's answers to part a.i) failed to mention interconnect – despite the question asking specifically about interconnect. Delay was another BIG thing not dealt with by some people's answer. Part a.ii) was answered less well than I expected – given that it is essentially book work. Furthermore, in b) people had not been listening about what constitutes a big capacitance – anything off chip or a large capacitive structure e.g. sensor. In c) some people did not mention tapered buffers or present a proof. Some people just used a two buffer case and some people presented a proof for driving a long wire (this is a different case and this difference was made clear in the lectures).

Question_4:

Most people could articulate why the circuit in figure 4 is not CMOS. However, people who could identify that the input to the inverter is undefined when A and B are low during Eval, could not extend this to the notion that because Eval/Pre is like a clock then the value is only undefined for a short period and it keeps it's previous value due to capacitance i.e. it is dynamically defined. However, most people could recognize the overall function of the circuit even if the timing diagram was a problem. Most people did not recognize that during Pre the values A and B are also 0 because these are derived from the outputs of other domino circuits!