Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2015-16 (3.0 hours)

EEE225 Analogue and Digital Electronics

In **Part A**, answer **FIVE** questions. **No marks will be awarded for solutions to a sixth question. In Part B,** answer **all questions**. Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Physical constants:

Charge on electron:	-1.602×10^{-19} C
Free electron rest mass:	$m_0 = 9.110 \times 10^{-31}$ kg
Speed of light in vacuum:	$c = 2.998 \times 10^{8}$ ms^{-1}
Planck's constant:	$h = 6.626 \times 10^{-34}$ Js
Boltzmann's constant:	$k = 1.381 \times 10^{-23}$ JK^{-1}
Melting point of ice:	$0°\text{C} = 273.2$ K
Permittivity of free space:	$\varepsilon_0 = 8.854 \times 10^{-12}$ Fm^{-1}
Permeability of free space:	$\mu_0 = 4\pi \times 10^{-7}$ Hm^{-1}

PART A

1. **i)** Explain, with the aid of a diagram, the operation of a two-input open-drain NAND gate. **(4)**

ii) A multisource bus is required with four data inputs and enable. Show how this can be achieved using open-drain NAND gates. **(4)**

2. The following Verilog code describes a certain logic gate at the switch-level.

```
module mygate(Y, A, B, C);
input A, B, C;
output Y;
supply1 POWER;
supply0 GROUND;
wire W1, W2;
pmos t1 (W1, POWER, A);
pmos t2 (W2, W1, B);
pmos t3 (Y, W2, C);
nmos t4 (Y, GROUND, A);
nmos t5 (Y, GROUND, B);
nmos t6 (Y, GROUND, C);
endmodule
```

i) Draw a transistor-level circuit diagram for this logic gate. **(4)**

ii) Produce a truth table for all possible combinations of the inputs **A**, **B**, **C**. Hence, deduce the logic function of the gate. **(4)**

3. **i)** Explain the difference between static power consumption and dynamic power consumption in a CMOS device. In your explanation, clearly describe the three components of power dissipation in such a device. **(5)**

ii) What do you understand by the term ‘activity factor’ when related to power dissipation. **(3)**

4. The transfer function of the circuit of Figure 4a is given by:

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \cdot \frac{1 + j\omega C(R_1 + R_3)}{1 + j\omega C R_3}$$

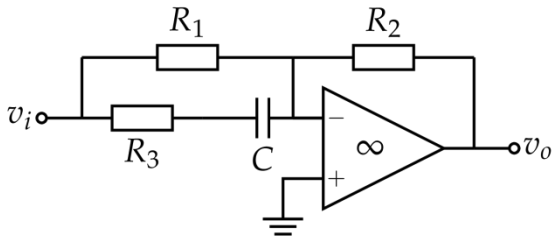

Figure 4a

a. Using the expression above, or otherwise, derive expressions for the low frequency and high frequency gain of the circuit. Briefly justify your results with arguments based on the physical behaviour of the components. **(3)**

b. The component values in the circuit are R_1 = 10 kΩ, R_2 = 20 kΩ, R_3 = 2.5 kΩ and C = l0 nF. Sketch the response of the circuit to a 0 V to 100 mV step input and label your sketch with initial and final amplitudes together with the time constant of the exponential change from one to the other. Your sketch should cover a time period of a few time constants. **(5)**

5. Describe concisely the cause of crossover distortion in class B push - pull output operational amplifiers. Use sketches to show the effects of crossover distortion on a triangular waveform, taking particular care with your representation of the crossover region. Show by sketching a circuit diagram how appropriate circuit design can largely overcome the crossover problem. **(8)**

6.

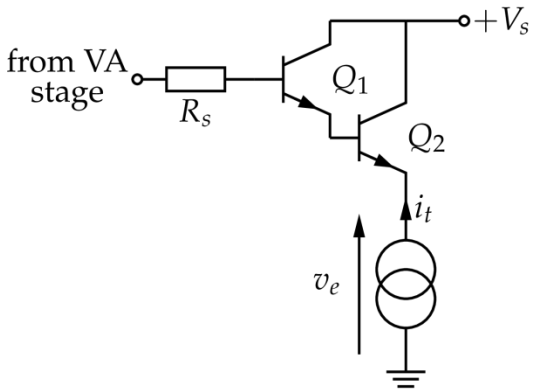

Figure 6a

The Darlington pair in Figure 6a is part of a Class B output stage of an operational amplifier. Show that the output resistance, r_o, is,

$$r_o = \frac{v_e}{i_t} = \frac{1}{g_{m2}} + \frac{\frac{1}{g_{m1}} + \frac{R_s}{\beta_1}}{\beta_2}$$

assuming $\beta_1 >> 1$ and $\beta_2 >> 1$.

g_{m1} and β_1 are small signal parameters of Q_1, g_{m2} and β_2 are small signal parameters of Q_2, v_e is the voltage on the emitter of Q2 with respect to ground and i_t is a 'test' current. *(Hint: it may be useful to draw and solve a small signal model composed of Q_2 and the resistance looking out of Q_2's base.)* **(8)**

7. Sketch a cross-sectional diagram of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST). Describe briefly how a conducting channel is formed and how it can work to amplify a signal.

Identify all the significant parts of the device in the diagram paying particular attention to the position of the gate with respect to the conducting channel. **(8)**

8. Assuming that the change in drain current with drain voltage in a MOST is given by:-

$$\frac{dI_d}{dV_d} = \frac{\mu_e C_g}{l^2}\left[V_g - V_T - V_d\right]$$

where the symbols have their usual meaning, derive expressions for:

i) the drain current in the unsaturated region,

ii) the value of drain voltage when saturation of the drain current occurs, and the value of the saturation current, and

iii) the transconductance in the saturated region. **(8)**

9. A p-n junction made of silicon (E_g = 1.1 eV), is used as a solar cell to generate power. Draw the conduction band, valence band and the Fermi-level of this p-n junction when it is open circuit with;

i) light of wavelength 1550 nm falling on its surface, and with

ii) visible wavelength light falling on its surface.

Give a brief justification for the way you have drawn these.

What is the voltage you can expect across this p-n junction in both these cases? **(8)**

PART B

10. a. Explain with the aid of a diagram the operation of a 4-bit successive-approximation Analogue-To-Digital Converter (ADC). **(6)**

A particular successive-approximation ADC uses reference values of 16 V for bit 2^3, 8 V for bit 2^2, 4 V for bit 2^1 and 2 V for bit 2^0. Determine the sequence of binary states in the register for the conversion of a constant input of 11.7 V. Explain each step. **(4)**

b. A Digital-to-Analog Converter (DAC) is required to interface a Field Programmable Gate Array to a VGA display. The circuit shown in Figure 10 is to be used for each channel.

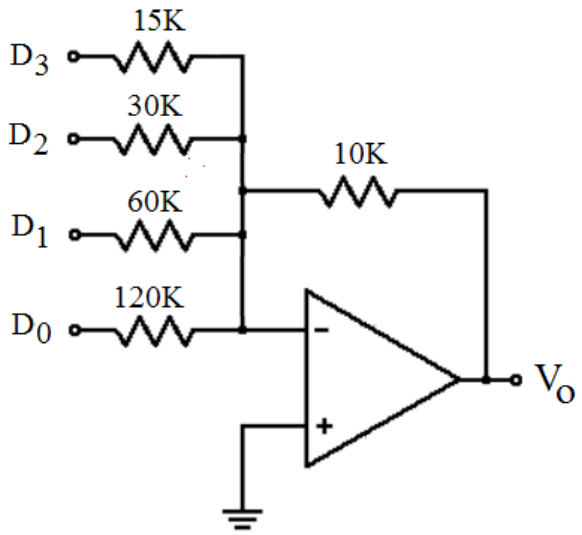

Figure 10. Weighted Binary DAC.

i) Briefly explain the operation of the circuit. **(3)**

ii) For input voltage levels of 3.0 V for logic '1', 0.0 V for logic '0' and the resistance values shown, calculate the output voltage for the input $D_3D_2D_1D_0 = 1101$. **(3)**

iii) In practice, the DAC structure shown in Figure 10 would not be used in higher resolution applications e.g. for an 8-bit converter. Explain the reason for this. **(4)**

11. a. Figure 11a shows a network consisting of noisy resistors, a noise voltage generator and a noise current generator.

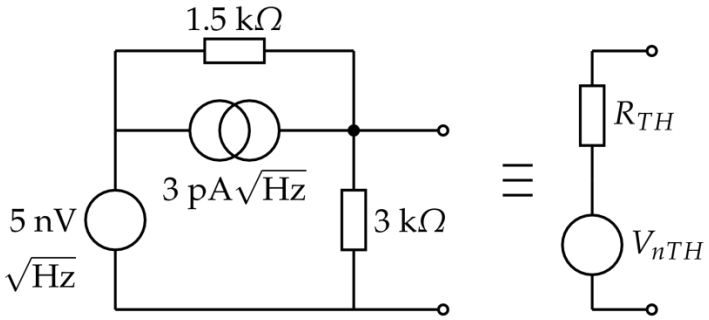

Figure 11a

Find the noise free resistance R_{Th} and the rms noise voltage V_{nTh} which form the Thevenin equivalent of the noisy network. **(10)**

b. The amplifier of Figure 11b has an equivalent input noise voltage, v_n of 15 nV $Hz^{-1/2}$, a negligible input current noise generator, and noisy resistors R_1, R_2 and R_s. The noise at the inverting input due to R_1 and R_2 is:

$$\overline{v_{nf}^2} = 4kT\frac{R_1R_2}{R_1+R_2}\ \mathrm{V^2Hz^{-1}}$$

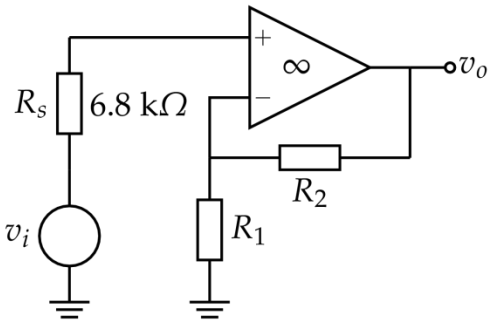

Figure 11b

i) If the noise power at the output of the amplifier due to R_1 and R_2 must not exceed 10% of that due to v_n, what are the maximum values of R_1 and R_2 that can be used to achieve an amplifier gain of 20? **(6)**

ii) A true rms voltmeter with a bandwidth of 10 kHz is connected to the amplifier output. What reading would you expect it to display with no input signal and R_1 and R_2 as calculated in part **(b) (ii)**? **(4)**

The mean square thermal noise voltage generated by a resistor R is $4kTR$ V^2 Hz^{-1} where $k = 1.38 \times 10^{-23}$ J K^{-1} and T may be taken as 300 K.

12. a. The Fermi-Dirac function is given by:-

$$P(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}$$

where the symbols have their usual meaning.

Using this, show that the built-in voltage (V_0) of a p-n junction is given by:-

$$V_0 = \frac{kT}{e} \ln\left(\frac{n_n}{n_p}\right)$$

where n_n and n_p are the electron concentrations in the n-type and p-type semiconductor respectively. **(8)**

i) Starting with a p-type silicon semiconductor (E_g = 1.1eV) doped to 2×10^{16} cm^{-3}, you create a p-n junction by diffusing in n-type dopants to a level of 1×10^{17} cm^{-3}. Given that n_i at 300K is 1×10^{10} cm^{-3}, what is the built in voltage of this junction at room temperature? **(4)**

ii) Describe qualitatively what happens to this built in voltage as the junction temperature increases to 450K and explain why. **(2)**

iii) Light from a 633 nm He-Ne laser with a 1 mW output falls on this silicon p-n junction when it is reverse biased. Assuming that it is 100% efficient in converting all of the light into current, what is the maximum current that would flow in this junction under this illumination? **(6)**

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