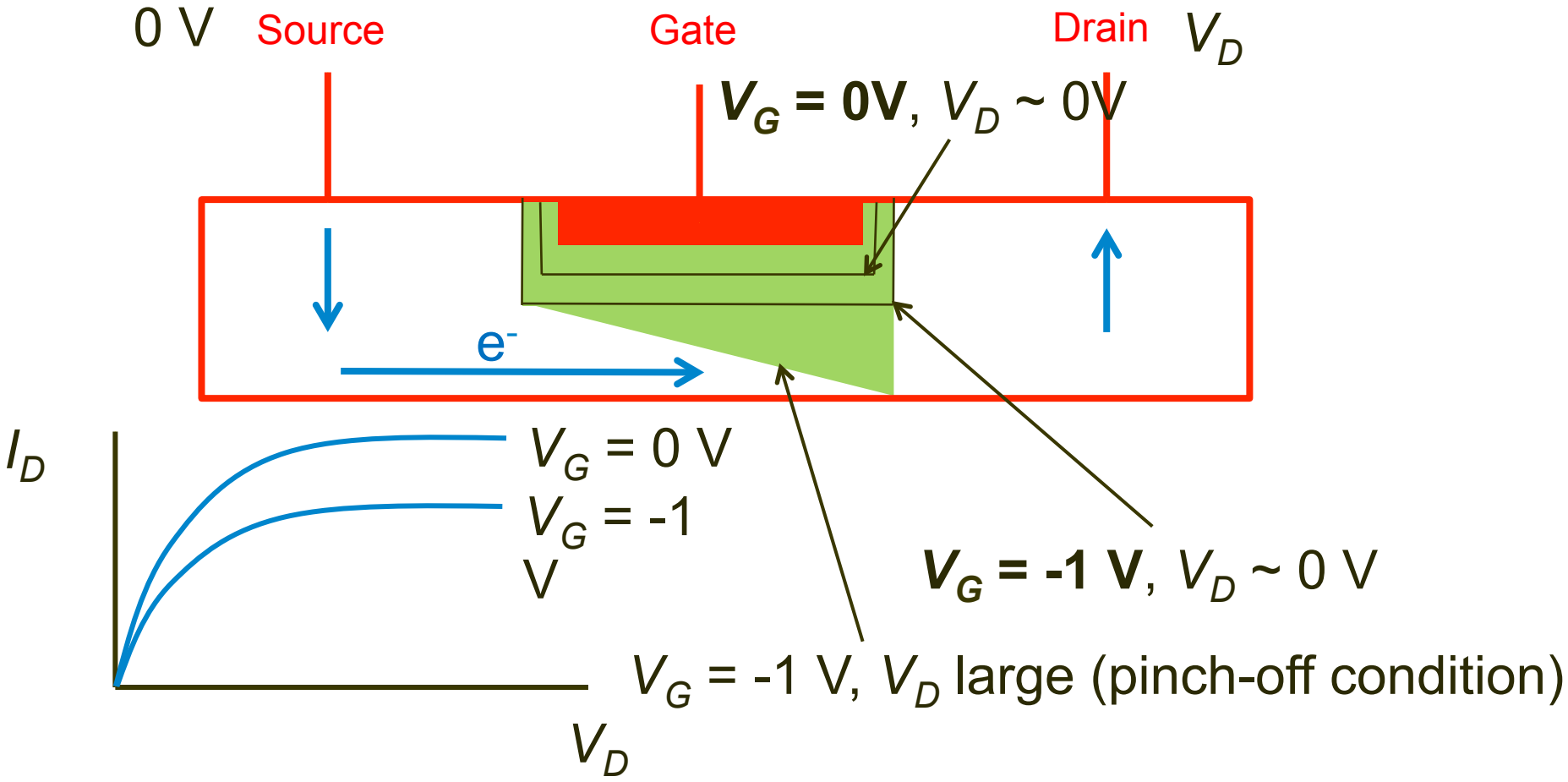
Lecture 15

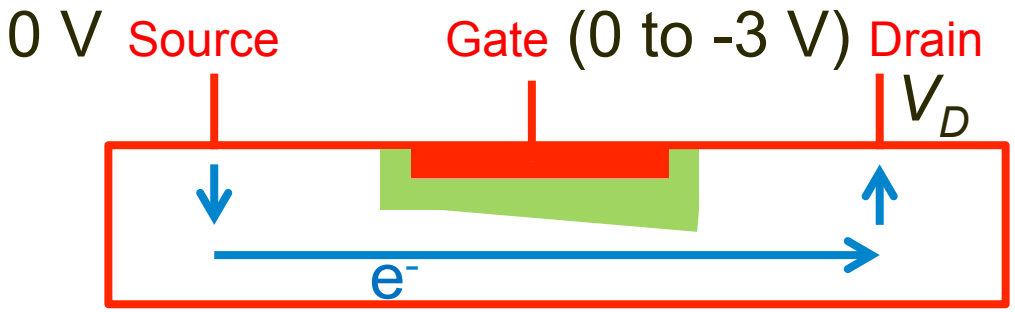
- JFET full output characteristics - explanation
- Output equations (no derivation)
- Metal oxide semiconductor field effect transistor – MOSFET

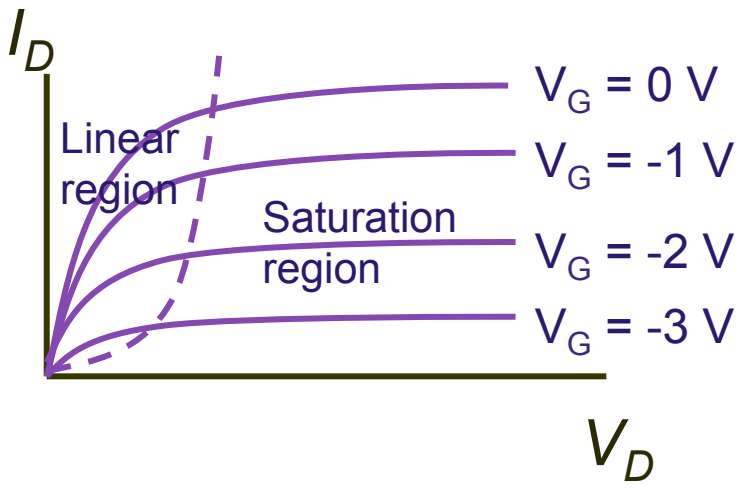
The University Of Sheffield.

JFET – Effect of Gate Bias



JFET Output Characteristics with various gate voltages



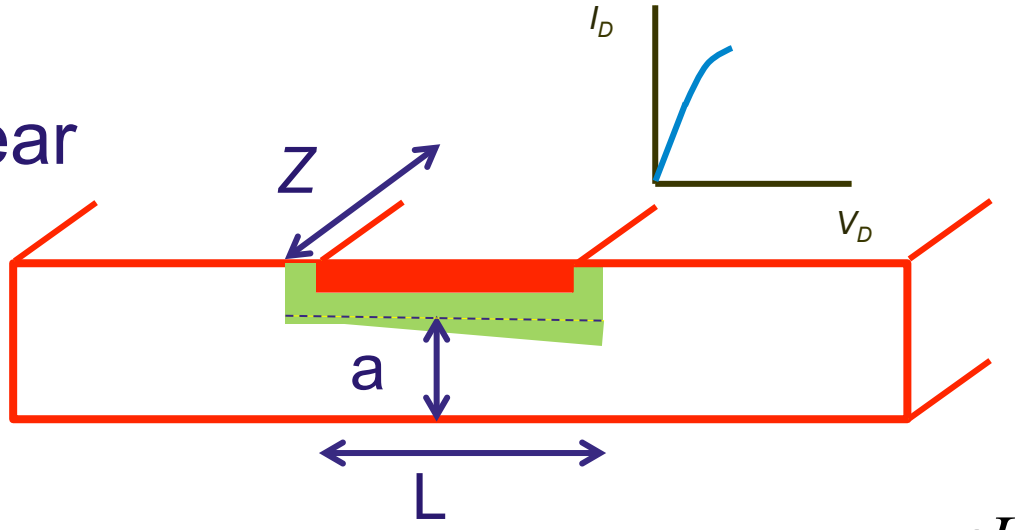


- At higher (negative) gate voltage, V_G, depletion region is already larger (constricts channel more) before V_D is applied, hence we get increased channel resistance and reduced current. Pinch-off also occurs at lower V_D
- The JFET is a **depletion mode** or **normally-on** device i.e. applying the gate bias depletes the channel, and it conducts (is 'on') without a gate bias
- Amplifier operation usually in saturation region

Transconductance $g_m = \Delta I_D / \Delta V_G$ - measure of amplification

JFET Equations (full derivation beyond scope of this course)

Below pinch-off (linear region)



At small drain bias – uniform depletion

$$I_D \alpha \frac{V_D}{R_{ch}} = \frac{ZaV_D}{\rho L} \quad \text{where } R_{ch} \text{ is the channel resistance } = \frac{\rho L}{Za}$$

At high drain bias – non uniform depletion

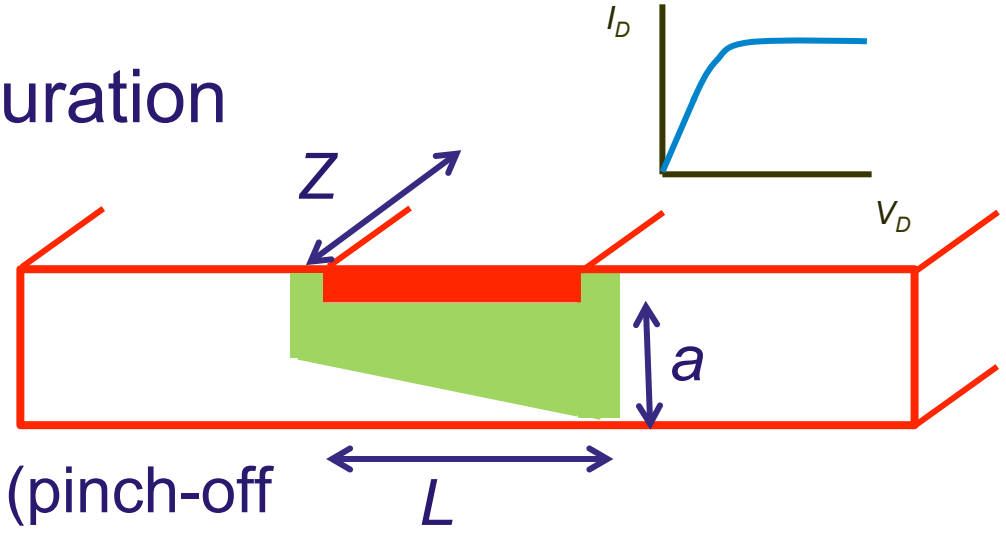
$$I_D = \frac{Za}{\rho L} V_P \left[\frac{V_D}{V_P} + \frac{2}{3}\left(\frac{V_G}{V_P}\right)^{3/2} - \frac{2}{3}\left(\frac{V_D + V_G}{V_P}\right)^{3/2} \right]$$

Takes account of non-uniform voltage and depletion region under the gate

The University Of Sheffield.

JFET Equations (derivation beyond scope of this course)

Above pinch-off (saturation region)



At pinch-off $V_G+V_D = V_P$ (pinch-off voltage) hence previous equation reduces to:

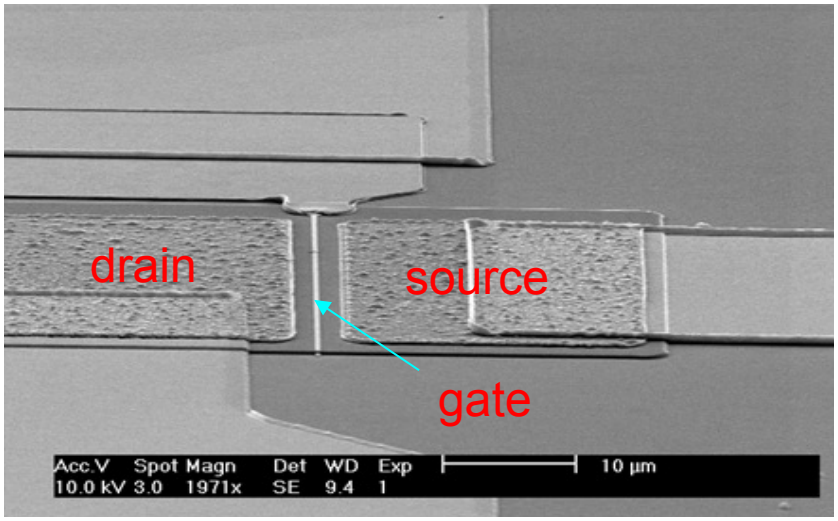
$$I_D(sat) = \frac{Za}{\rho L} V_P \left[\frac{1}{3} - \frac{V_G}{V_P} + \frac{2}{3} \left(\frac{V_G}{V_P} \right)^{3/2} \right]$$

Independent of V_D but depends on V_G

$$g_m = \frac{\partial I_D(sat)}{\partial V_G} = -\frac{Za}{\rho L} \left[1 - \left(\frac{V_G}{V_P} \right)^{1/2} \right]$$

JFET Design

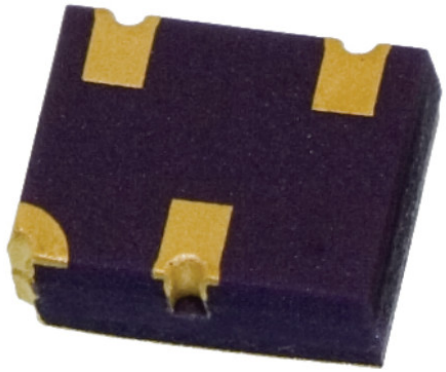
- Equations from the previous slide enable one to design a JFET device for a particular application
- High current and large transconductance mean ***small L*** and resistivity, ρ, (***high channel conductivity***) and ***large Z***
- Materials with a high electron mobility work best for these devices



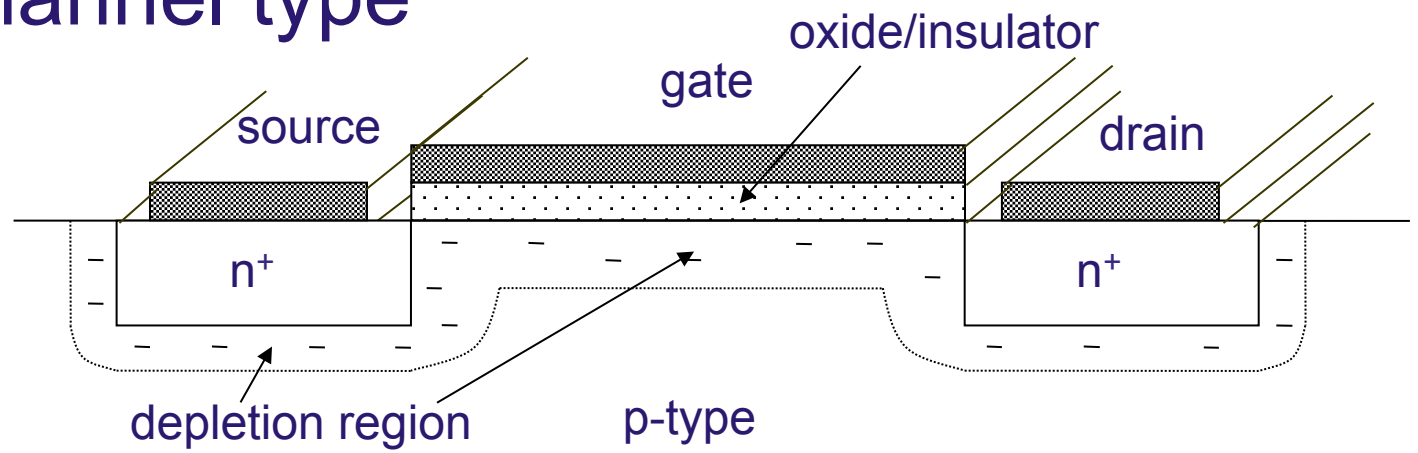
JFET Applications

Although over 40 years old, the Junction Field-Effect Transistor (JFET) is used in applications requiring low power, high input impedance (reverse biased p^+n gate) and low noise such as amplifiers, constant current sources, voltage-controlled resistors, and switches:

- Microphones
- Sensors and detectors
- Measurement instrumentation (e.g. oscilloscopes, analysers)
- Medical imaging and blood-analysis instrumentation



MOSFET (Metal Oxide Semiconductor FET) – n-channel type

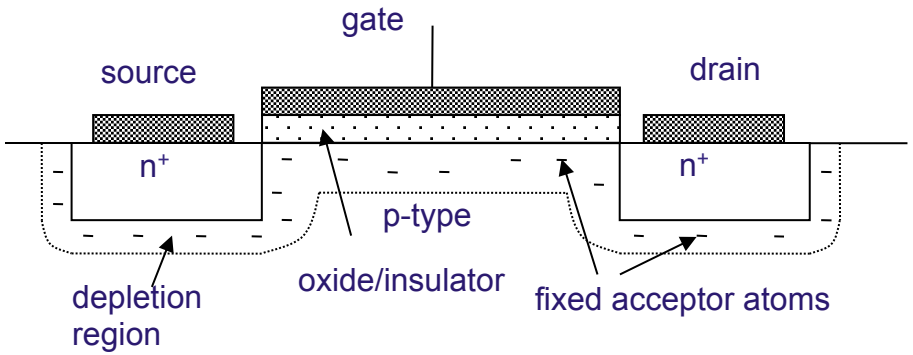


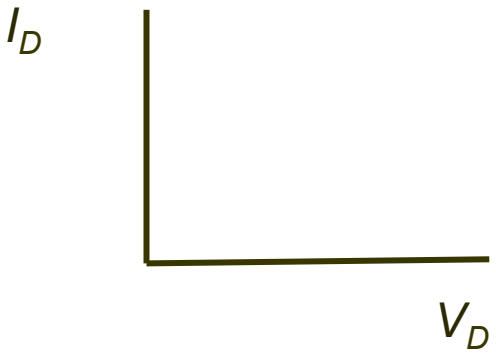
- In this case the gate is an MOS structure - does not conduct because of insulating silicon dioxide layer – behaves like a capacitor

- n^+ wells form the source and drain

- A depletion region is formed around the n+ source and drain wells since they form a pn+ junction with the p-region

MOSFET - operation





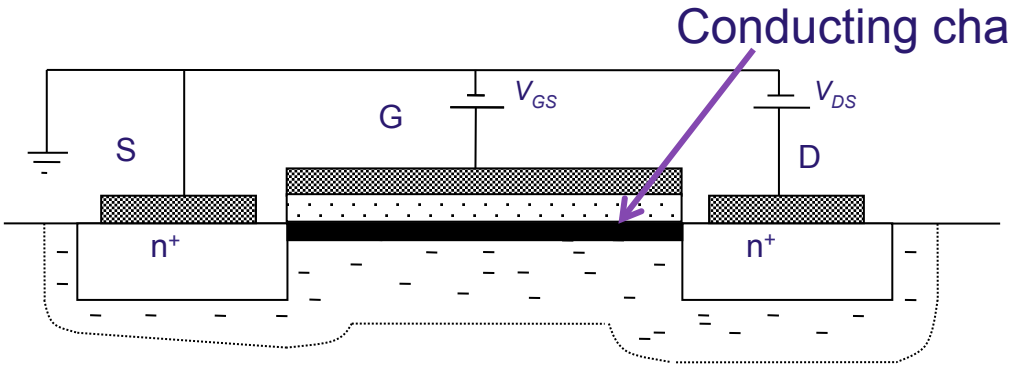
$V_G \geq 0$ (slightly positive bias) – no current

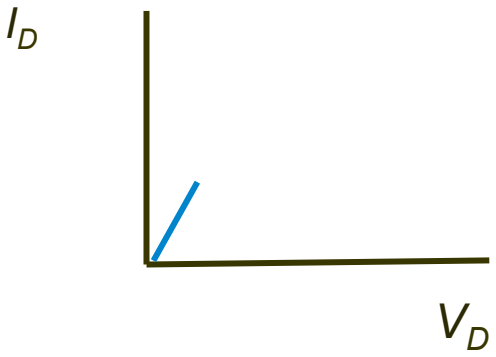
- Built-in potential at n^+p junction plus small positive gate bias induces depletion region in p-type material

- Exposed fixed negative acceptors in the depleted region under the gate balances positive charge on the gate due to positive bias (like the plates of a capacitor)

- No mobile charge between the source and drain therefore device is non-conducting

MOSFET - operation





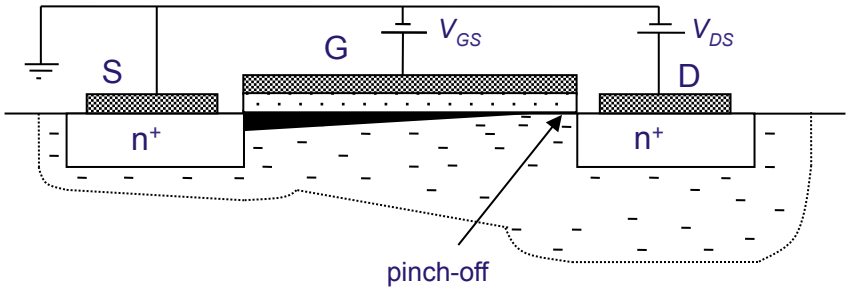
$V_D << V_G > V_T$ (linear current region)

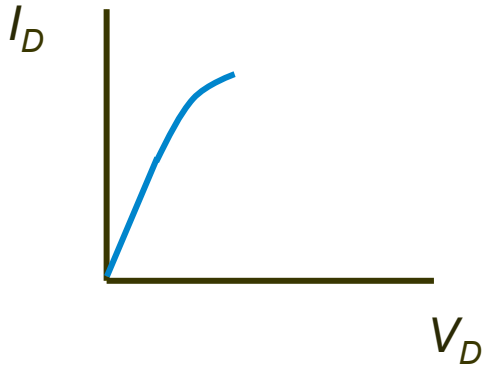
- As more positive charge is placed on the gate, depletion into the p-type region increases to balance the positive charge on the gate

- Eventually, as $V_G \cong V_T$ (called the threshold voltage), uncovering further negative fixed acceptors in the depletion region is not enough to balance the positive charge on the gate and electrons are formed under the gate (inversion layer) from the source and drain

- The source and drain are now connected by the mobile electron channel and the device conducts

MOSFET - operation

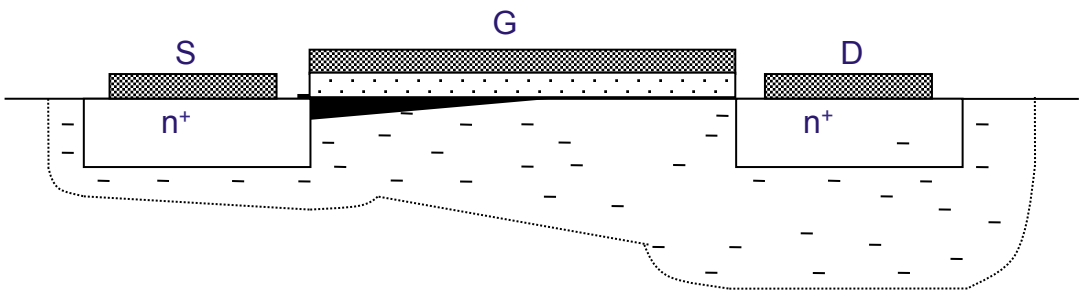


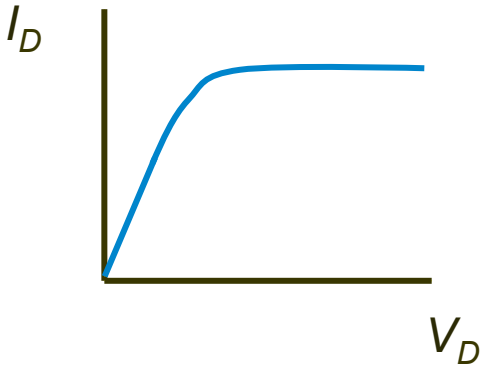


$V_D \cong V_G - V_T$ (pinch-off condition)

• *As* $V_D - V_G$ approaches V_T, the net voltage between the gate and the drain at the drain end of the channel falls below V_T and the channel 'pinches-off' at the drain end where the channel potential is most positive and the bias across the gate capacitor is least

MOSFET - operation





V_D - V_G > V_T (saturation region)

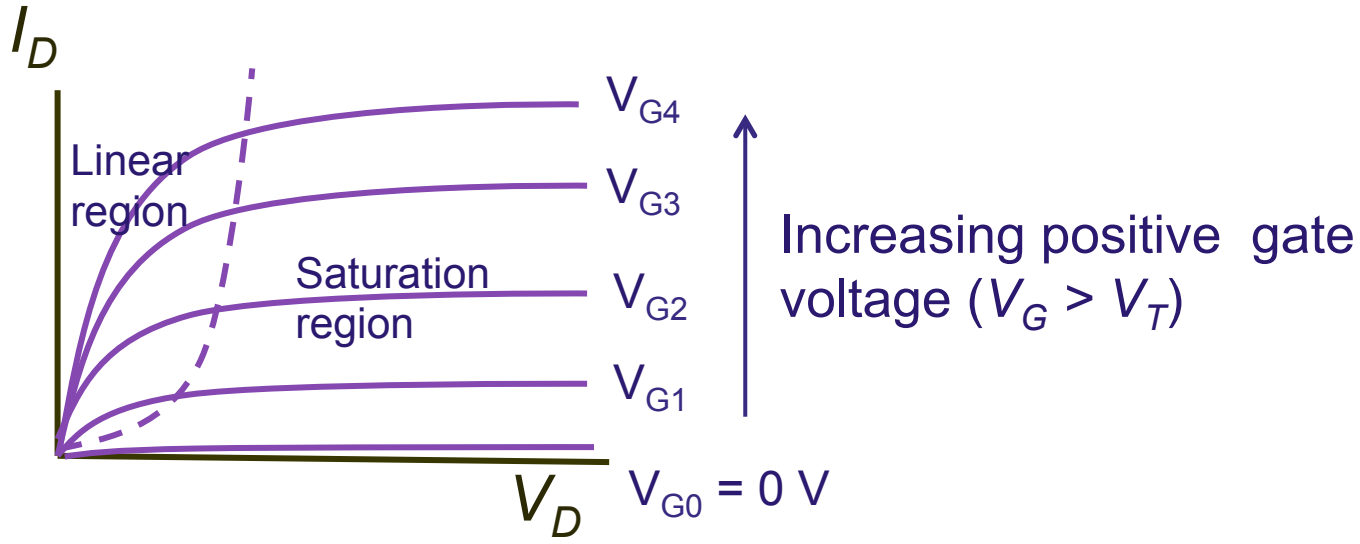
- Further increases in V_D causes the pinch-off region to move towards the source

- I_D remains constant (saturation region)

- Note: the current does not fall to zero as might be expected if the channel is pinched off near the drain (similar effect to JFET)

The University Of Sheffield.

MOSFET - Characteristics



- Similar shape to JFET but positive gate bias increases I_D
- **Enhancement mode** or **normally-off** device i.e. applying the gate bias increases or enhances the channel conductance and it does not conduct (is 'off') without a gate bias
- p-channel MOSFET possible by swapping the n and p regions and using a negative gate bias to induce conduction

Transconductance $g_m = \Delta I_D / \Delta V_G$ - measure of amplification

The University Of Sheffield.

MOSFET Equations (derivation beyond the scope of the course)

Linear region $$I_D = \frac{Z\mu}{L} C_G \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Determines the amount of charge in the channel

Saturation region $$I_D = \frac{Z\mu}{2L} C_G \left[V_{GS} - V_T \right]^2$$

Summary

- JFET drain current is controlled by the geometry of the channel in response to both the gate voltage and the drain voltage
- The JFET is a depletion mode or normally-on device
- The MOSFET has an MOS gate structure which induces a conducting channel under the gate
- The MOSFET is an enhancement or normally-off device