Comments on Introduction VLSI Design (EEE310/6036), May 2009

General

A reasonably well-attempted paper. I would judge it to be slightly easier that previous papers with a mix of book work and analysis that was appropriate.

Q1.
This question was marred by a significant mistake in Figure 1: the pull-up and pull-down networks do not match. The pull-down network is ((A+B).C.D)' whilst the pull-up network is (C'+D').A'.B'=(C.D)'.(A+B)'=(CD+A+B)'. However, given that the question asked you to produce an accurate schematic of what was in figure 1 then this was not a problem – people generally did what was asked and produced a schematic that matched the figure (invariably without showing the substrate connection). There were a few instances where people got the correct pull-down network and then inferred the correct pull-up network from it. However, there were a few cases where neither of the networks resembled the layout. Given the error in the question, I was quite lenient and where one network was used to infer the other, I marked this as though it were correct. Similarly, in part b) – where it made a difference - if you wrote down the function of the pull-up *or* pull down network then marks were awarded.

Q2.
As usual, some people had difficulty in converting the logic circuit into a transistor level circuit and a variety of solutions were offered. The answers to the sizing part of the question were generally good but the estimations of the capacitance often forgot the drain capacitance and did not consider all of the wires in the transistor circuit (not the logic diagram – the input wires to the OR gate will not exist in the transistor-level circuit!).

Q3.
Fewer people answered this question, which was quite straightforward. However, a number of people who did answer the question a) got the equations wrong (pure book work!) b) could not do the analysis for the switching voltage. This, after I specifically said in the lectures that this was one analysis that I would be prepared to put in an exam question. Most people who did this question neglected to mention that you had to take the negative root of the square term for the p equation to end up with the right result. I didn't penalize people for this but I could have done so.

Q4.
The answers to this question were marred by students not remembering basic facts presented in the lectures. The master-slave FF schematics were a collection of fanciful and erroneous diagrams. The most frequent error being that the master and slave latches were represented as being FFs. In part c) people invariably forgot to mention that clock trees are automatically generated.