Examination Feedback for EEE6393 Microsystems Packaging
Spring Semester 2010-11

# Feedback for EEE6393 Session: 2010-2011

**Feedback:** Please write simple statements about how well students addressed the exam paper in general and each individual question in particular including common problems/mistakes and areas of concern in the boxes provided below. Increase row height if necessary.

**General Comments:**

The paper produced a wide range of marks, with four candidates below the pass grade through to some exceptional scores. Most students were happier with the descriptive parts and some of the calculations suffered from mistakes and misunderstandings. Many students wrote too little in terms of justifying their answers, whilst others wrote too much; often going well outside the frame of the question. Sometimes not all of the question was answered, with many students missing the opportunity to get the odd additional mark from essentially one line comments. There was some evidence of students running out of time on the final question. There was a noticeable preference for Q3&4 (MH) over Q1&2 (GW).

**Question 1**:

Most students made a good attempt at this question. In the numerical section some made inappropriate choices for chip and package dimensions. Many missed out the need for the heat sink attachment to be flexible, to allow for the TCE mismatch. The reflow soldering process was well described, but no students specified actual temperature regimes for the different stages, instead using '$T_m$' without making it clear that they understood what it meant. None of the answers included a description of the actual equipment (IR ovens plus conveyor belt or batch oven) needed for the reflow soldering process.

**Question 2**:

The descriptions of the TSV formation process leant it self to a series of diagrams, which many students did well. However, some answers lacked detail, hence marks were dropped. The PCB design methodology was seldom described in enough detail – often being just a bullet point list without further explanation. Some students described PCB fabrication and/or BGA assembly, neither of which were asked for. The numerical section on radiative cooling was done poorly, with student not formulating the problem correctly.

**Question 3**:

The majority of students could discuss the advantages and disadvantages of a SoC/SiP fairly well, although a few left out some important statements. Most could calculate the inductances well enough, although there were a few with silly mistakes. Not many commented well on the relative values. Most suggested some improvements to methods, but there were very few comprehensive answers. Many students failed to remember how to calculate yield and either got this wrong or failed to answer at all.

**Question 4**:

Most could list the main bonding methods. Many students however failed to discuss these in any great detail. Most got the right package technology for each of the situations described, but some has very strange ideas. Many students failed to calculate the approx power dissipation of the i7 processor, but most could calculate the approx. number of pin outs OK. There were some good answers the packaging scheme, but some students went for unnecessary complexity and cost. Most could describe the purpose of accelerated testing but a few starting discussing life-cycle and burn-in which was not entirely appropriate. Most described the HAST test fine. Very few could calculate the room temperature MTTF and indeed there were some strange answers here (e.g.: fractions of a second).

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