Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2013-14 (2.0 hours)

EEE335 Integrated Electronics 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **Figure 1** shows the pull-down network for a CMOS, digital circuit.

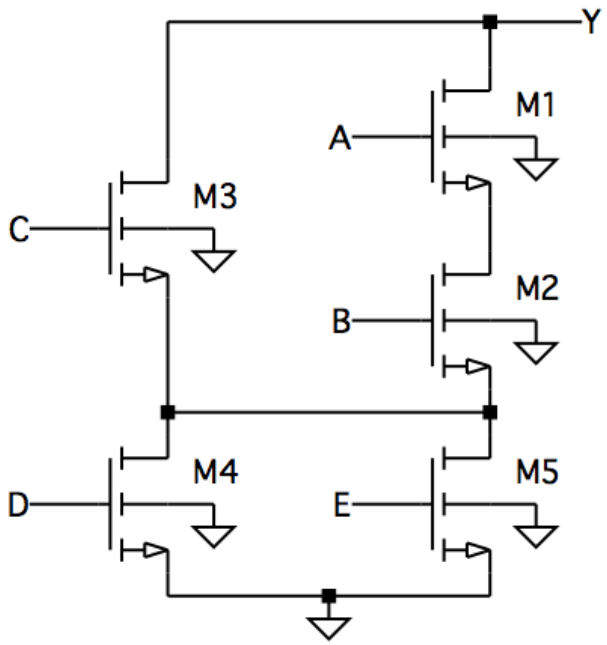


Figure 1: CMOS Pull-Down Network

a. Draw the corresponding pull-up network for this circuit (remembering to show how the substrates are connected). **(5)**

b. Determine the function, **Y**, in terms of **A**, **B**, **C**, **D**, and **E**. **(3)**

c. Size the transistors **M1**…**M5** (as multiples of the minimum width of an *n*-type FET), assuming that the gate is 'minimum-sized'. **(5)**

d. Why are all the substrates of these *n*-type FETs connected together and connected to the most negative point in the circuit? **(4)**

e. The wire connecting the drains of **M4** and **M5** is removed. What is the new function of **Y**? **(3)**

2. **a.** An IC designer has to decide how to design and fabricate an ASIC:

i) What types of fabrication technologies are available and what are their attributes? **(4)**

ii) What factors will influence the choice of technologies and the approach to design? **(4)**

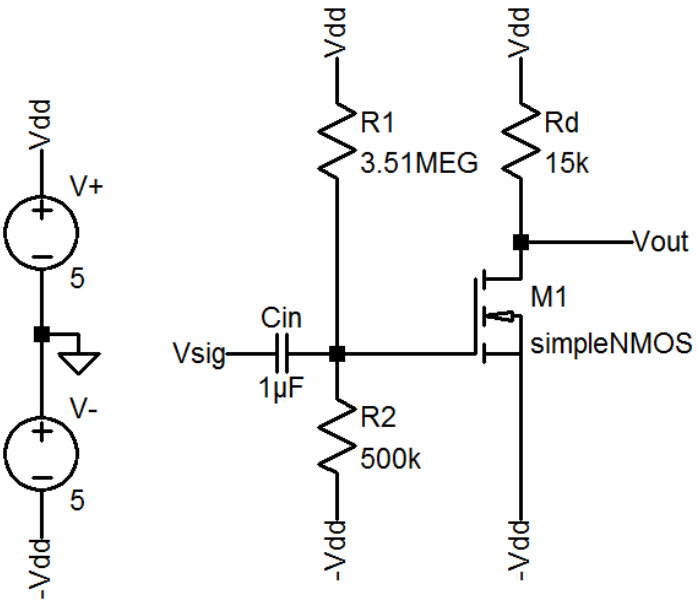
b. Currently, the design approach often adopted by designers (at an intermediate level) is termed *register-transfer level* (RTL).

i) What does RTL mean in terms of design and why is it important? **(4)**

ii) How should a clock tree be constructed to allow the implementation of a reliable design? **(4)**

c. Explain the reason why verification is important and why the time spent on verification is beginning to dominate design activity? **(4)**

3.



.model simpleNMOS nmos (kp=80u vt0=0.6 lambda=0.025 L=0.8u W=16u)

Figure 3: SPICE model of a common source amplifier.

a. **i)** Calculate the overdrive voltage, the Q-point drain current (ignoring channel modulation effects) and the transconductance of the common source amplifier shown in **Figure 3**. Show that the FET in the amplifier operates in the saturation region. **(4)**

ii) Draw the small signal π model of the amplifier including the effective resistance, r_o, of the FET. Calculate its midband gain, assuming the input signal source, **Vsig**, has an output impedance of 0Ω and ignoring channel modulation effects. **(4)**

iii) Calculate the midband gain if the signal source has an impedance of 100kΩ. **(2)**

b. The amplifier in **Figure 3** is driven by a signal source that produces a 1kHz sinusoid of 0.1V amplitude and whose output resistance is 100kΩ. Draw two sketches, one of the voltage at the gate of **M1** and one of the voltage at **Vout** in **Figure 3**. Label these sketches to show the voltage offsets and the maximum and minimum voltages of the waveforms. You can ignore channel modulation effects. **(4)**

c. **i)** Explain why the voltage divider biasing of the amplifier in **Figure 3** leads to unpredictable amplifier performance. Explain why it is not appropriate for use as part of an IC. **(3)**

ii) Biasing using a current mirror is the preferred method for IC amplifiers. Briefly explain the benefits of maximising the output resistance of a biasing current mirror. **(3)**

4. **Figure 4** shows a SPICE model of a two stage operational amplifier. The FETs in **Figure 4** have the following parameters:

K_n=200μA/V^2, K_p=150μA/V^2, $|V_{TO}|$=0.5V (for both n and p channel), λ=0.05V^{-1}, L=0.75μm.

The gain of a two stage op-amp when all transistors operate at the same overdrive voltage is given by: $A_v = 1/(\lambda V_{OV})^2$.

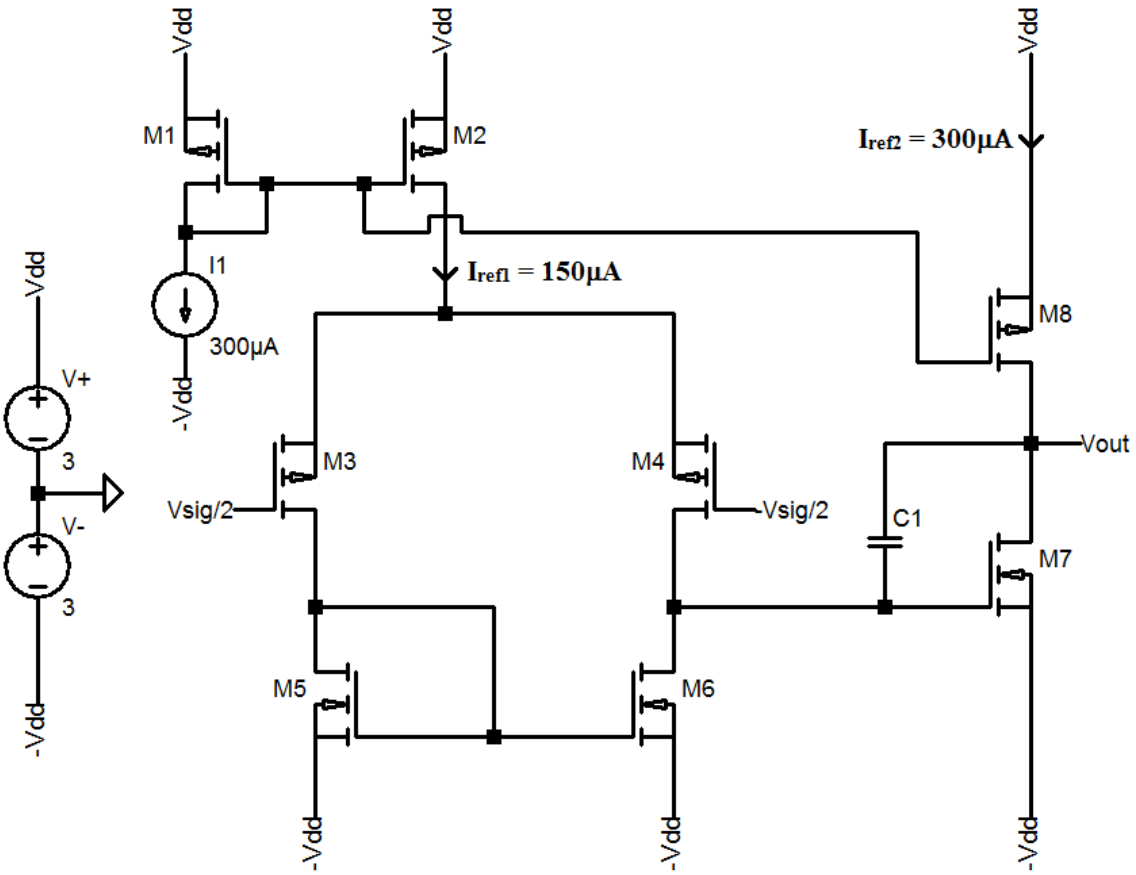


Figure 4: a two stage operational amplifier.

a. **i)** The amplifier is to be designed with a gain of 2500. Calculate the required overdrive voltage and the output resistances of FETs **M3** to **M8**. **(3)**

ii) Calculate the transconductances of the differential and the common source stages of the amplifier, and hence the gain of each stage. **(3)**

b. Derive the required channel widths for each of the FETs. **(7)**

c. Where in the circuit of **Figure 4** can a 'virtual ground' be assumed in the small signal analysis of the amplifier? (Answer in the form: gate, source or drain of FET MX.) What is the Q-point voltage at this point? **(3)**

d. When operating in saturation, the parasitic capacitances of FET **M7** are C_{GD}=0.02pF and C_{GS}=0.05pF. Use the Miller transform to derive a value for the coupling capacitor **C1** that gives an amplifier upper cutoff frequency of ~100kHz. **(4)**

NLS/AMM