Data Provided: Yes

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE6205 Power Electronic Converters

Answer **FOUR** questions. **No marks will be awarded for solutions to a fifth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** The voltage source inverter shown in figure 1.1 is modulated by Sinusoidal Pulse Width modulation. With reference to figure 1.1 and suitable voltage and current waveforms explain the effect of dead-time on voltage v_{Az}. Voltage v_{Az} is measured between terminals A and z as shown in figure 1.1.

(3)

b. For the case in a), represent the error voltage $v_{err}(t) = v_{Az\_no\_DT}(t) - v_{Az\_DT}(t)$, with an equivalent square wave. $v_{Az\_no\_DT}(t)$ and $v_{Az\_DT}(t)$ denote, respectively, the output voltage without dead-time and with dead-time inserted in turn on gate signals. The output voltage is measured between terminals A and z, as shown in figure 1.1.

(4)

c. Based on b) and using the general Fourier series expression show that the low-order harmonics in the output voltage v_{Az} are given by:

$$v_{err}(t) = \frac{4}{\pi} V_d \frac{T_d}{T_s}\left[\cos(\omega_o t - \varphi) + \frac{1}{3}\cos 3(\omega_o t - \varphi) + \frac{1}{5}cos\, 5(\omega_o t - \varphi) + \cdots\right] \quad (1.1)$$

where T_d is the dead-time, T_s is the switching period, φ is the angle by which the fundamental component of the current lags the fundamental component of the inverter phase voltage and ω_o is the angular frequency of the fundamental component of the output voltage.

(3)

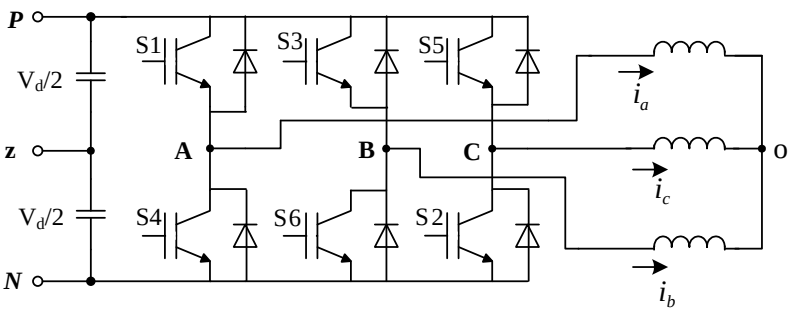

Figure 1.1 Two level voltage source inverter

d. A Voltage Source Inverter shown in figure 1.1 is modulated by Sinusoidal Pulse Width Modulation SPWM. Frequency of the modulation signal of the SPWM modulator is 400Hz. IGBT devices are switched at a frequency of 10kHz and a dead-time period of 2μs is introduced into the turn on signals. The inverter is supplied from a 600V dc source. A peak value of the current drawn by the load is 20A. The inverter is in linear mode of operation and operates at the maximum output voltage.

d.i For the case in d) and based on expression (1.1) in c) calculate a fundamental component of the output voltage v_{Az} when the load power factor is 0.866.

(4)

d.ii For the case in d) and based on expression (1.1) in c) determine under which load conditions the dead-time will have the most significant effect on the fundamental voltage.

(4)

2. **a.** For leg A of the converter shown in figure 2.1 sketch a representative waveform of the output voltage v_{AN}, select suitable gate drive signals with reference to the output voltage v_{AN} and identify available switching states.

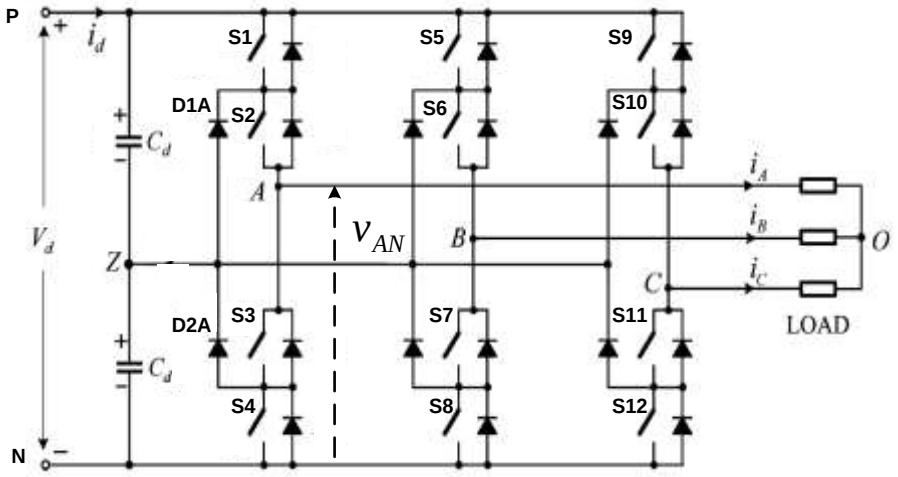

Figure 2.1 Neutral point clamped voltage source inverter

(5)

b. The inverter shown in figure 2.1 is modulated by Space Vector Modulation. Select one suitable switching state that enables power flow between the source and load and will make voltage v_{ZN} rise. For the selected switching state calculate the amplitude and position of the corresponding static space vector based on the general space vector form given by:

$$\vec{y}(t) = \frac{2}{3} \cdot (y_a(t) + y_b(t) \cdot \alpha + y_c(t) \cdot \alpha^2). \qquad (2.1)$$

(8)

c. The reference vector $\vec{V}_{ref}$ of the inverter is in Sector I as shown in figure 2.2. The inverter is modulated by Space Vector Modulation. The sampling frequency is 10 kHz and the fundamental period of the output voltage is 20ms. The reference vector $\vec{V}_{ref}$ is at the position $\theta = 30^{\circ}$, as shown in figure 2.2. Calculate the magnitude and position of the two subsequent reference vectors.

(5)

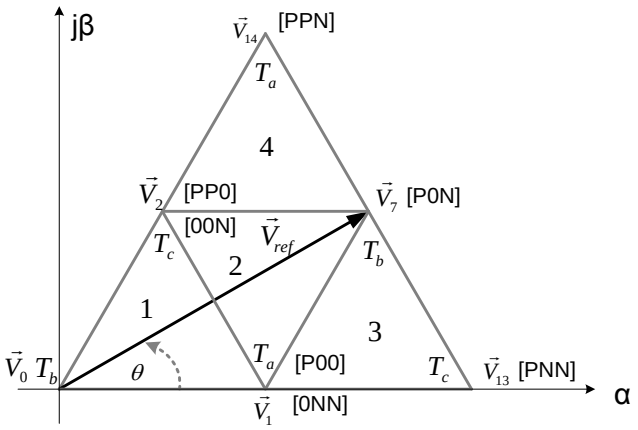

Figure 2.2 Space vector diagram

3. **a.** The Current Source Inverter CSI-fed induction motor drive shown in figure 3.1 is connected through 6-pulse SCR rectifier as a front end to the utility grid. The line-to-line voltage at the rectifier input terminals $V_{ll_{rms}}$ is 2.3kV, 50Hz (rms value). The line inductances are assumed to be zero. The dc choke L_d is sufficiently high such that the dc current is ripple-free. The losses in the system are neglected. Through the feedback control the magnitude of the dc link current is kept at a value set by its reference of 148A. The CSI is modulated by Trapezoidal Pulse Width Modulation TPWM. Show with reference to appropriate voltage waveforms that the average value of the dc-link voltage is given by

$$V_d = \frac{3}{\pi}\sqrt{2} \cdot V_{ll_{rms}} \cdot cos\alpha \quad (3.1)$$

and propose a practical solution to supply the load with 400kW. α is the firing angle of the SCRs.

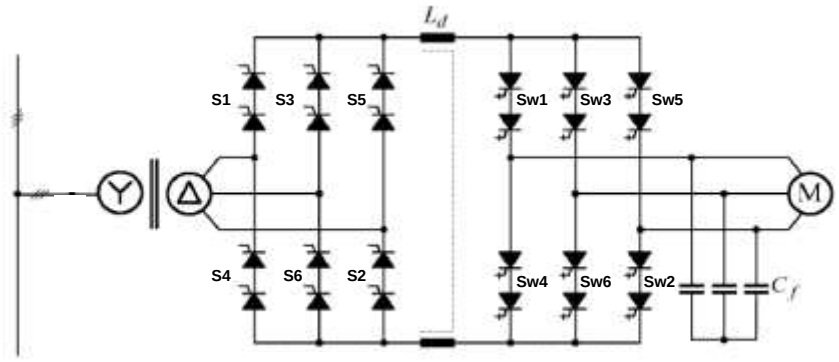

Figure 3.1 Current Source Inverter CSI-fed induction motor drive

(6)

b. With reference to suitable voltage and current waveforms determine the switching sequence and switching frequency of the SCR devices of the 6-pulse rectifier shown in figure 3.1.

(6)

c. With reference to suitable circuit diagrams explain the switching constraints of the three-phase Current-Source Inverter. Propose a practical protection solution in case of short circuit at the inverter output terminals.

(6)

4. **a.** Explain the operation of the six-step inverter shown in figure 4.1 by means of the gate-drive signals, switching sequence, switching commutations and switching frequency for one fundamental period of the output voltage.

(6)

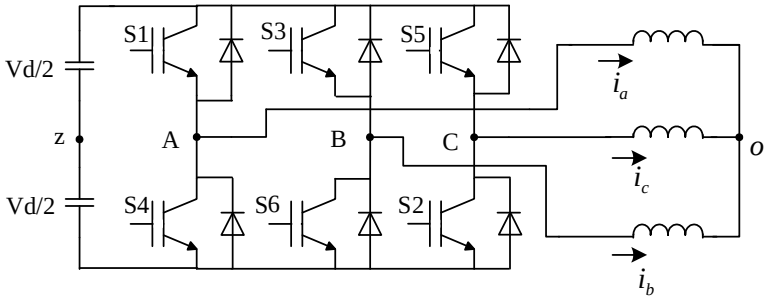

Figure 4.1 Two-level voltage source inverter

b. A six-step voltage source inverter shown in figure 4.1 supplies a 460V (rms line-to-line value), 60Hz induction motor. With reference to suitable voltage waveforms and the general Fourier series expression show that the amplitude of the fundamental output line-to-line voltage of the six-step inverter is given by:

$$V_{AB_{(1)}} = \frac{2\sqrt{3}}{\pi} V_d \qquad (4.1)$$

and select the most appropriate value of the voltage at the dc terminals of the inverter.

(6)

c. In the circuit shown in figure 4.2 an IGBT is used to switch a diode-clamped inductive load. The load is represented by a constant current source I_o. The free-wheeling diode D_f is assumed to be ideal.

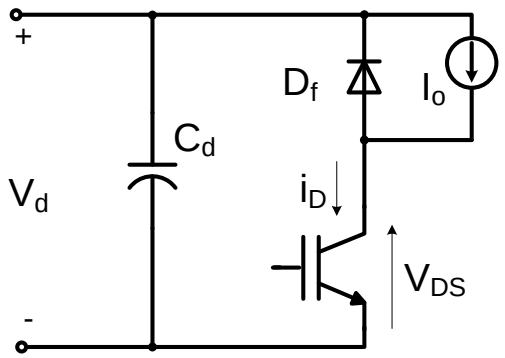

Figure 4.2 An IGBT used to switch a diode-clamped inductive load

c.i For the case in c), sketch an equivalent circuit of the circuit shown in figure 4.2 that can be used to estimate the turn on current and voltage waveforms of the IGBT.

(2)

c.ii Based on c.i), explain with reference to suitable voltage and current waveforms how $(dv_{DS}/dt)_{on}$ can be controlled by optimal design of the gate resistor.

(4)

5. **a.** The Pulse Width Modulated PWM rectifier shown in figure 5.1 is connected to the grid through the three line inductors represented by L and R in figure 5.1 and is loaded by the inverter-fed motor.

a.i For the case in a) and with reference to figure 5.1 define switching functions for legs a, b and c and based on that define rectifier phase voltages v_{ao}, v_{bo} and v_{co}. **(5)**

a.ii Based on a.i) and with reference to figure 5.1 mathematically describe the PWM rectifier in natural three-phase coordinates. **(4)**

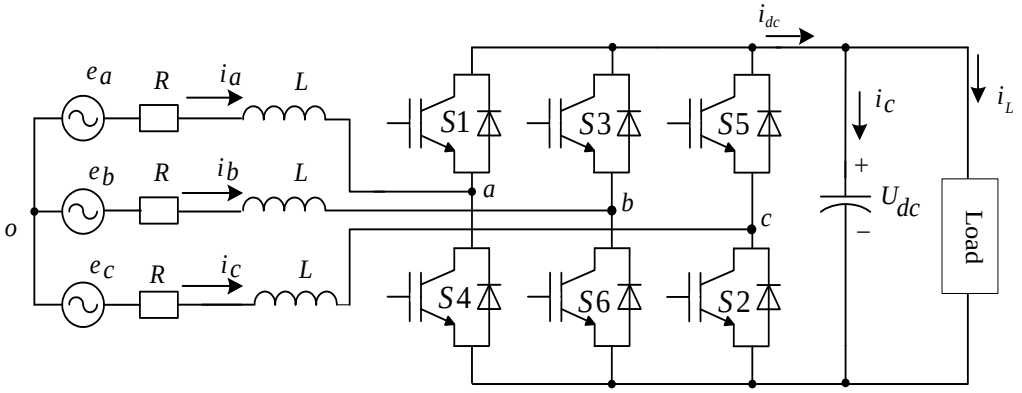

Figure 5.1 Two-level voltage source PWM rectifier

b. Represent the model developed in a) in s-domain and based on that draw a block diagram of a voltage-source PWM rectifier in natural three-phase coordinates. **(5)**

c. Select gate-drive signals for switches S1 and S4 shown in figure 5.1 considering their finite turn on and turn off times. The device switching frequency is 10 kHz, turn on time is 0.3μs and turn off time is 0.65μs. Justify your selection. **(4)**

6. **a.** The series resonant circuit, as shown in figure 6.1, is supplied by a dc source V_d and the capacitor is in parallel with a dc current I_o, which represent the load. The initial conditions for the inductor current and capacitor voltage are $i_L(t_0) = I_{L0}$ and $v_C(t_0) = V_{C0}$, respectively. With reference to figure 6.1, $i_L(t)$ and $v_c(t)$ are given by:

$$i_L(t) = I_o + (I_{L0} - I_0) \cdot cos\big(\omega_0(t - t_0)\big) + \frac{V_d - V_{C0}}{Z_o} \cdot sin\big(\omega_0(t - t_0)\big)$$

(6.1)

$$v_C(t) = V_d - (V_d - V_{C0}) \cdot cos\big(\omega_0(t - t_0)\big) + Z_0 \cdot (I_{L0} - I_0) \cdot sin\big(\omega_0(t - t_0)\big)$$

(6.2)

where ω_o is resonant frequency and Z_o is characteristic impedance of the undamped series resonant circuit. Derive the expression (6.2) given above for the capacitor voltage $v_c(t)$.

(6)

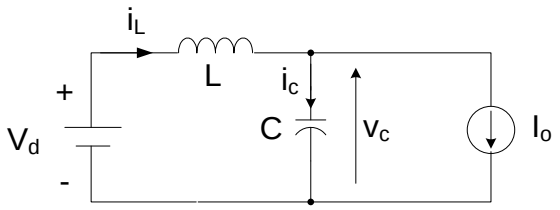

Figure 6.1 Series resonant circuit

b. A resonant dc link inverter supplied from a 200V dc source is represented by an equivalent circuit shown in figure 6.2. The inductance L and capacitance C of the resonant circuit are 0.24mH and 1μF, respectively. The current drawn by the load is constant at 200A and input current of the inductance L at the beginning of the resonant cycle is 209A. The circuit resistance has negligible effect on the voltage and current waveforms during one resonant cycle.

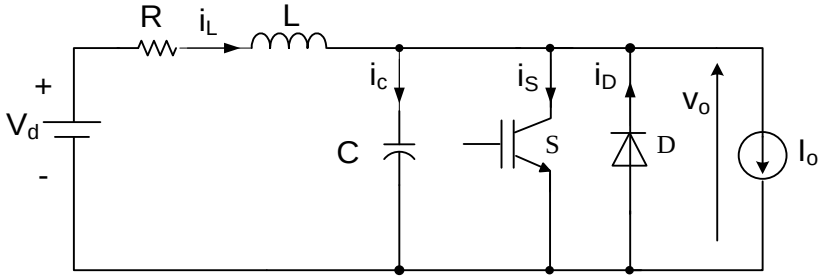

Figure 6.2 Equivalent circuit of resonant dc link inverter

b.i With reference to figure 6.2 and suitable voltage and current waveforms explain basic operational principals of the resonant dc link inverter.

(5)

b.ii Explain why switch S and diode D in the circuit shown in figure 6.2 can be removed in the practical resonant dc link inverter.

(3)

b.iii For the case in b) calculate the peak value of the current through the capacitance C using the expression (6.1) given in a).

(4)

MO/DG