Q1a) **Bookwork**

i) When the electric field in MOSFET is sufficiently high, carriers travelling from source to drain can accumulate energy to become hot carriers. This happens when the potential difference between the drain and gate is sufficiently large to cause a high electric region developing near the drain. For example in a NMOS, hot electrons can generate more electron-hole pairs via impact ionisation. The newly generated electrons and holes may also gain energy from the field to increase the population of hot carriers. These additional carriers lead to an increase in drain current and substrate current. Some of the hot electrons are also injected into the gate and are trapped at the Si-SiO_2 interface and in the gate oxide. These trapped electrons can cause a shift in the threshold voltage and reduce the transconductance. Latch-up can also occur if the substrate current is sufficiently large.

ii) This is an important reliability issue in modern ICs since the dimensions of MOSFET are reduced significantly to increase the transistor density. However the operating voltage remains constant, leading to significant increase in the electric field in MOSFETs.

Understanding

iii) Two of the following

- Reduce the electric field. Obviously this can be achieved by reducing the operating voltage. However in practice this is not ideal because of requirement to maintain some standards in operating voltages. Therefore modification of doping profiles near the drain is used to reduce the peak electric field.
- Reduce carrier trapping in the gate oxide and at the Si-SiO_2 interface. This can be achieved by careful control of the fabrication procedures, material purity and annealing cycles to reduce trap density.
- Reduce the amount of time that the device is subjected to high electric field. When possible a set of design rules that define safe operating conditions is use to ensure good circuit design that will ensure device spends minimal time at high electric field.

Q1b) **Bookwork**

i) When the applied electric field across the gate oxide approaches the breakdown field of the oxide, impact ionisation leads to generation of electron-hole pairs in the oxide. Low mobility holes are usually trapped in the oxide further increase the electric field leading to more impact ionisation events and hence higher current flowing through the oxide. The large current produces heat that damages the oxide layer.

ii) In thin oxide film with imperfections (pin holes), current tends to flow through these localised spots. This increases the heat which in turn allow more current to flow, leading to a thermal runaway that causes oxide failure/rapture at these local spots. Metal filament growth at these localised spots typically cause short circuit.

In more uniform films, the dielectric breakdown causes accumulation of charges in the gate oxide that shift the threshold voltage and reduce the gain.

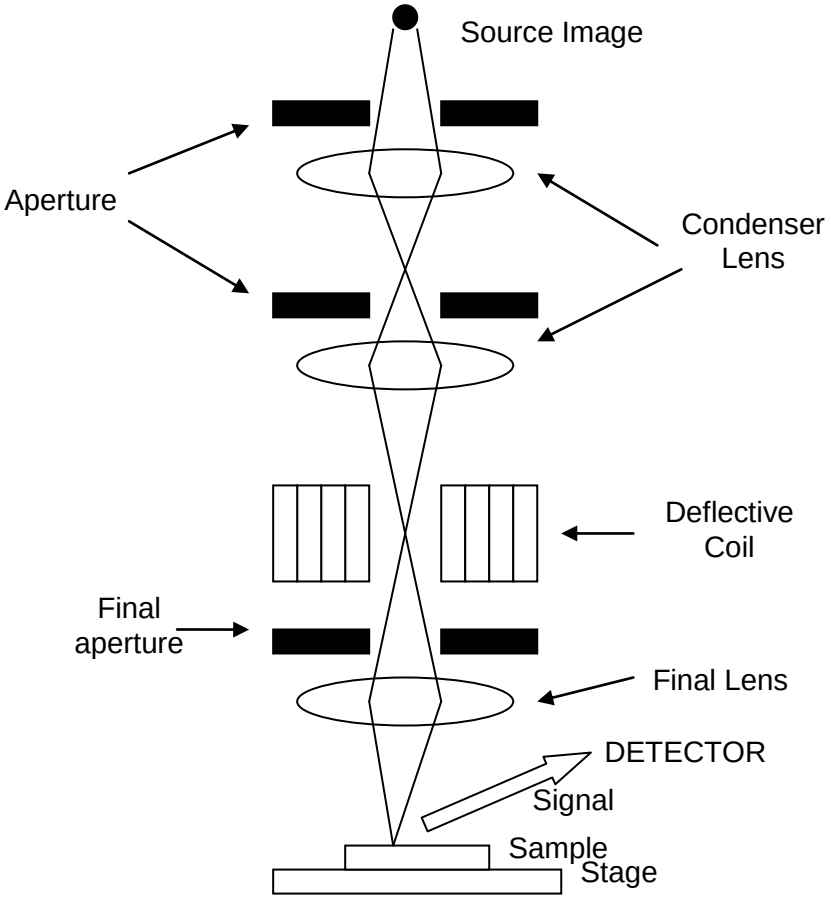
Q1c) **Understanding**

Typical breakdown field of dielectric is ~10MV/cm. The distribution showed that most devices failed at fields lower than 1MV/cm, i.e infant failures. Most likely cause of these infant failures is poor quality oxide layer. Possible ways of improving the oxide layer include:

- Use of novel materials such as multi layer dielectrics to reduce pin holes.
- Minimise antenna effects during fabrication process such as dry etching and ion implantation. The antenna effect can inject charges into the oxide layer.

- Careful control of the oxidation process to reduce generation of traps. For instance minimise the thermal stress to reduce trap densities.
- Careful addition of dopant atoms to passivate the interface.

Q2a) **Bookwork**
i)



Electrons thermionically emitted from tungsten filaments (1-50kV potential difference)
After passing through the condenser and objective lenses, the electron beam is demagnified to ~ 1nm spot.
This beam is then raster scanned over the sample.
The bombarding electrons (primary electrons) dislodge electrons (secondary electrons) from the sample.
The electrons are attracted and collected by a positively biased detector to form signal.
More secondary electrons are emitted from sharp corners, edges and sloped regions than planner surface.

Bookwork
ii) High energy electrons impinging on the samples knock core electrons to be ejected from the atom under characterisation. To stabilise the atom electrons from high energy levels drop to lower levels and emit x-ray photons with characteristics of the atom in the process. Thus, EDX can be use to identify atomic species such as detection of contaminants in Si.

High energy electrons create more electron-hole pairs in semiconductors, polymers and ceramics. The created electron-hole pairs may recombine and emit light. This process is known as catholuminescence (CL).CL can be used for characterisation of defects in materials since they act as non-radiative recombination sites.

Q2b) **Bookwork**

i) Stages in IC packaging are as follows. The wafer is cut into individual die which is then attached to a substrate or carrier using epoxy. Next, bonding of devices to the substrate is performed using Au ball bonding or Al wedge bonding. This is followed by plastic encapsulation for mechanical support and device protection from the environment.

ii) Two of the following

Types of failure mechanism	Possible Causes
Ball bond lifting	Contamination on bond pads, incorrect bonding parameters, Kirkendall voids, bond pad corrosion
Wedge bond lifting	Contamination, incorrect parameter settings, corrosion
Ball bond neck break	Incorrect parameter settings, incorrect wire loopings, die to package delamination, excessive thermal treatment (bamboo grain formation)
Wedge bond heel break	Incorrect parameter settings, incorrect wire loopings, leadfinger to package delamination,
Bond to metal short	Incorrect parameter settings, incorrect bond placement, insufficient bond pad-to-metal distance
Bond to bond short	Incorrect parameter settings, incorrect bond placement, insufficient bond pad-to-bond pad distance
Wire to wire short	Incorrect wire looping, insufficient wire-to-wire distance
Cratering	Incorrect parameter settings, excessive bond pad probing

Bookwork and understanding

iii) Flip-chip bonding refers to the process the die/chip is mounted on a substrate using interconnect materials such as solder bump and conductive adhesive so that the active are of the chip faces the substrate.

The main advantages are possibility of integrating chips having different technologies (compound semiconductor and Si) to form hybrid modules as well as combining the functions of several IC chips with other discrete active and passive components to form hybrid circuits. In addition higher ratio of device to substrate area can be achieved providing higher packing density. The multichip module reduces the number of connections, solder joints and wiring significantly compare to traditional single chip package. This leads to improvement in system performance and reliability.

Bookwork

Q3a) Select from

Catastrophic failure: Damage to the cleaved surface occurs in lasers operating at high current densities.

- Non-radiative recombination at energy states originated from material defects and defects introduced by poor cleaving cause heating which can create more defects. These defects contribute to more recombinations and heating.
- In severe cases this runaway heating leads to melting of the surface region.

Reduced intensity: Non-radiative recombinations at defects result in appearance of dark line defects and dark spot defects and hence reduced intensity.

- Dark line defects seem to be more severe in devices that were damaged during packaging suggesting that it is associated with dislocations.

Increased threshold current: Possible causes of this include

- Dissociation of point defects under high photon flux conditions. (e.g: dissociation of Zn + O in GaP LEDs)
- Migration of defects into active regions has also been suggested as a possible reason.
- Increased thickness of oxide layer at the facet leads to reduced intensity.

Die-bond packaging degradation: At elevated temperatures

- Interdiffusion of different metal leads to weakening of contacts
- Electromigration
- Oxidation of metals, metal diffusion can change contact resistance

Exposure to moisture can also cause corrosion of metal contacts.

Q3b) **Bookwork**

Electrostatic discharge usually

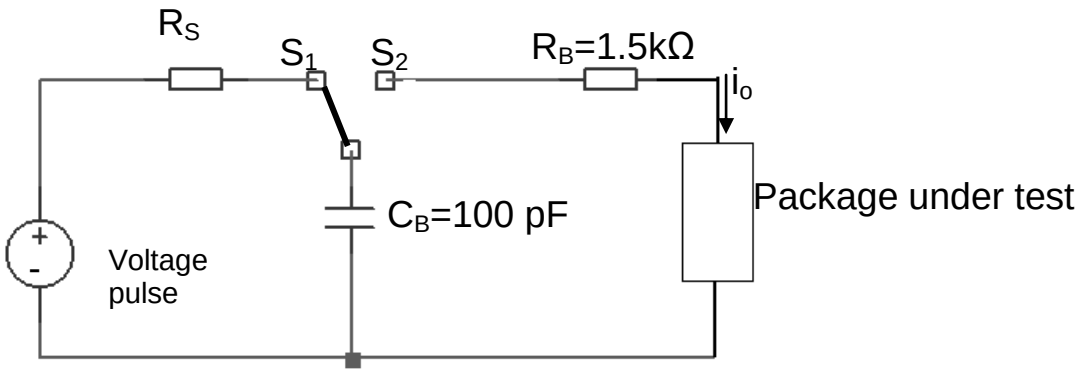
- Involves tens of kilovolts
- Large current flow due to large voltage generated by static charge
- Occur in ns time scale

ESD occurs when charge is transferred from

- a charged body to a device.
- a charged device to a grounded surface.
- a charged machine to a device.

In all cases charge transfers from the object with higher potential to the object with lower potential until equal potential is achieved.

Q3c) **Bookwork and calculation**



i) Human Body Model assumes that the human body can be replaced by C_B= 100pF and R_B=1.5kΩ. Device resistance R_d = 20Ω.

A voltage pulse is used to charge up the capacitor C_B when the switch is at S_1. When the switch is placed at S_2, C_B discharges through RB and the package under test causing a large current to flow through the package since the discharge typically last for a short time. In this case, ~ $5x(R_B+R_d)xC_B$ = 760 ns.

ii) Max. current in circuit = $V_{HBM}/(R_B+R_d)$.
Max. current flowing through device to cause current spiking = $50x10^6x4x10^{-8}$ = 2A.
The Human Body Model voltage, V_{HBM} = 2x1520 = 3040 V.

Therefore VHBM > 3040 V should be used to study metal spiking due to ESD.

Q3d) **Understanding**
i) Failure due to ESD is significantly higher when the laser diode is under reverse bias. In the reverse bias the power dissipation is IV_r across the depletion small depletion region, δ. In the forward, the power I^2R is dissipated across the device with length D. Therefore the power density in the reverse bias, IV_r/δ > power density in forward bias I^2R /D since D > δ.
ii) The results suggest that approximately 1% (corresponding to voltage of 3kV) of the diodes will fail since laser diodes are operated under forward bias. This indicates that the laser diodes have been sufficiently well designed to handle ESD.

Q4a) **Bookwork**
i) Total failure rate = 10.01+7.2+8.1=25.31 x 10^{-6} /hour.
ii) For an exponential distribution, MTTF = $1/25.31x10^{-6}$ = 39510 hours.
Reliability after 1000 hours = $\exp(-25.31x10^{-6}x1000)$ = 0.975.
iii) It is obvious that the failure rate and the MTTF are worse than the individual component when the components are connected in series.

Q4b) **Bookwork Calculation**
i) ln(1000) = 6.9. From figure 4.1, this approximately corresponds to
ln[-ln(1-F(t))] = -0.1
1-F(t) = exp(-exp(-0.1)). Therefore F(t) = 0.595, i.e 59.5% of the devices will fail after 1000 hours.
To find the median time, F(t) = 0.5. ln[-ln(0.5)] = 0.4. From figure 4.1, this gives ln(t) = 6.6 and hence t=750 hours.

ii) **Understanding**

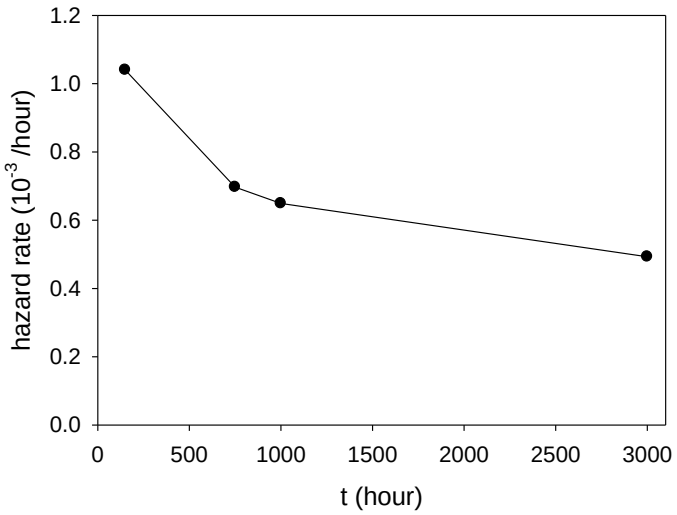
Since the a straight line can be fitted, we have
$\ln[-\ln(1-F(t))] = m\ln(t) + C$. Let $C=m\ln(n)$, we can show that $F(t) = 1-\exp(-(t/n)^m)$ which is a Weibull model.

To work out the value of n, let F(t) = 0.63, $\ln[-\ln(0.37)] = -5.8\times10^{-3} \sim 0$.
Therefore ln(t) = 7.05, t = n = 1212 hours.

The full expression for failure probability becomes $F(t) = 1 - \exp(-(t/1212)^{0.75})$

The hazard rate $\lambda(t) = \beta t^{\beta-1}/\alpha^{\beta}$ where $\beta = 0.75$ and $\alpha = 1212$.
$\lambda(150) = (0.75\times150^{-0.25})/(1212^{0.75}) = 1.04\times10^{-3}$ /hour
$\lambda(750) = (0.75\times750^{-0.25})/(1212^{0.75}) = 6.97\times10^{-4}$ /hour
$\lambda(1000) = (0.75\times1000^{-0.25})/(1212^{0.75}) = 6.49\times10^{-4}$ /hour
$\lambda(3000) = (0.75\times3000^{-0.25})/(1212^{0.75}) = 4.93\times10^{-4}$ /hour

iii)



Understanding

iv) The gradient of m = 0.75 and the sketch in part (iii) suggest that the hazard rate is high for t < 750 hours. This is likely to be due to infant mortality. This failure could be due to excessive dislocations in the InGaAs, for instant due to lattice mismatch with InP substrate. These dislocations act as generation recombination centres that produce large leakage current. TEM, EBIC and CL are possible characterisation techniques that can be used to study the dislocations.