The University Of Sheffield.

Data Provided: Weibull probability plotting paper

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Autumn Semester 2011-12 (2.0 hours)

EEE6008 Reliability and Failure

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. A batch of 50 electronic components was placed on accelerated life test. 7 of these were found to have failed after 2970, 2120, 3820, 4150, 5550, 1050 and 4885 hours.

i) Rank the data and calculate the median rank using Bernard's approximation. **(2)**

ii) Plot and label the time to failure data on the Weibull probability plotting paper provided. **(2)**

iii) Determine the values for the timescale parameter, η, and shape parameter, β. **(2)**

iv) Sketch how the failure rate varies with time for these components and suggest 2 possible failure mechanisms. **(2)**

v) Deduce the mean time to failure of the components and predict the percentage of components that will have failed after 20,000 hours.

b. i) A system has been designed with 10 components in series. What is the minimum reliability each component may have if the overall reliability must not be less than 97%?

ii) What is the overall reliability if components with only 85% reliability are used instead? **(2)**

iii) If these components (85% reliability) were to be connected in a parallel configuration, plot the percentage comparative reliability over a single component and the incremental reliability as a function of the number of components connected (up to the first 4 components). **(2)**

iv) With use of a sketched cost versus reliability plot, describe the trade-off between cost and reliability of a component or system. **(4)** **(2)**

2. **a.** Incorrect handling of sensitive electronics can result in damage through electrostatic discharge (ESD).

i) Explain how ESD can cause junction burnout in a semiconductor device **(3)**

ii) List 3 strategies to minimise the risk of ESD to sensitive electronics. **(3)**

b. The human body model is commonly used to simulate ESD from a person into an electronic device. If a pulse of 3000V is discharged from a person to a photodiode with area $4\times10^{-8}m^2$ and resistance of 20Ω.

i) Draw the equivalent circuit for the human body model. **(2)**

ii) Calculate the time constant of discharge and estimate the time span over which the discharge occurs. Assume a negligible voltage drop across the photodiode compared with the ESD pulse. **(2)**

iii) Calculate the maximum current density flowing through the photodiode. **(2)**

c. Outline how the electron beam induced current (EBIC) technique performed in scanning electron microscope (SEM) can characterise the ESD damage in a photodiode. **(2)**

d. Photodiodes, together with lasers and optical fibres are also susceptible to damage by high energy particle irradiation. Describe the process of damage to these important optical fibre system components. **(6)**

3. **a.** The deposition of SiO_2 layers upon Si is commonly used in the fabrication of integrated circuits to act as a dielectric layer. SiO_2 is typically deposited at 300°C and then allowed to cool to 20°C. Young's modulus, E, is 94GPa for SiO_2 and 160GPa for Si. Poisson ratio, υ_f, is 0.25 for SiO_2 and 0.22 for Si. The coefficient of thermal expansion is $0.25\times10^{-6}K^{-1}$ for SiO_2 and $0.22\times10^{-6}K^{-1}$ for Si.

i) Calculate the thermal stress that will develop in the SiO_2 film. **(2)**

ii) Sketch and label the film/substrate interface under stress and state whether the SiO_2 film is under tensile or compressive stress? **(2)**

b. Aside from stress related problems, provide 3 possible defects/contaminants introduced during the chemical vapour deposition of SiO_2 layers. **(3)**

c. Explain how weak spots in oxide layers originate and how they can result in breakdown of the oxide layer. **(6)**

d. A ramp voltage dielectric test was conducted on devices known to have been subject to some metal contamination during processing. Sketch how you expect the resultant Weibull probability plot to look. Please also state why you think a Weibull distribution provides the best model for this scenario. **(3)**

e. Hot carrier effects resulting from reduced device dimensions but high applied voltages present a particular problem in modern ICs. Describe one mechanism by which hot carrier effects occur in MOSFETs and discuss how its influence may be reduced. **(4)**

4. **a.** List 3 possible failure mechanisms that may occur during the following stages of IC packaging:

i) Wafer thinning

ii) Die attachment

iii) Wire bonding

iv) Moulding **(6)**

b. Describe the process of popcorn cracking in plastic encapsulation and discuss a suitable characterisation method for detecting failures caused by popcorn cracking. **(6)**

c. Explain how conductor degradation caused by electromigration could be mitigated through application of the Blech effect. **(4)**

d. Describe 4 possible additional strategies that could be employed to minimise the damaging effect of electromigration in metallic conductors. **(4)**

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