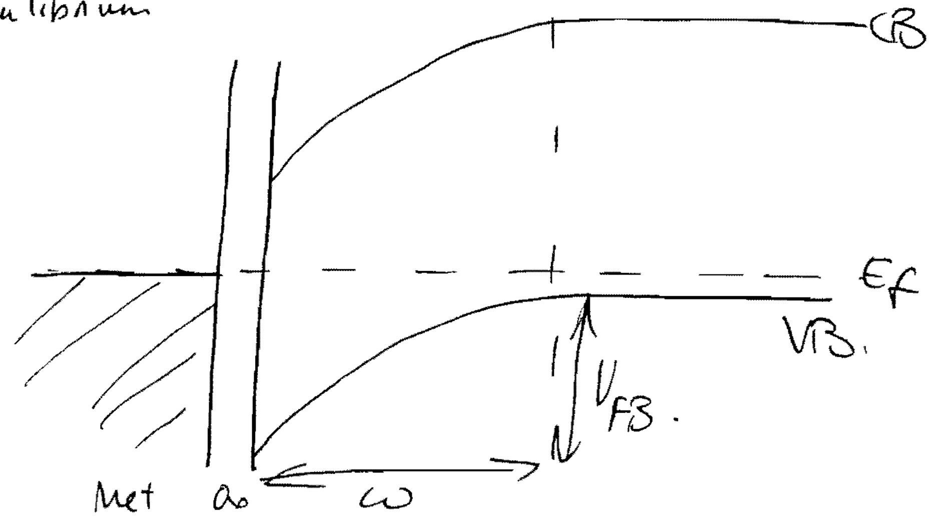
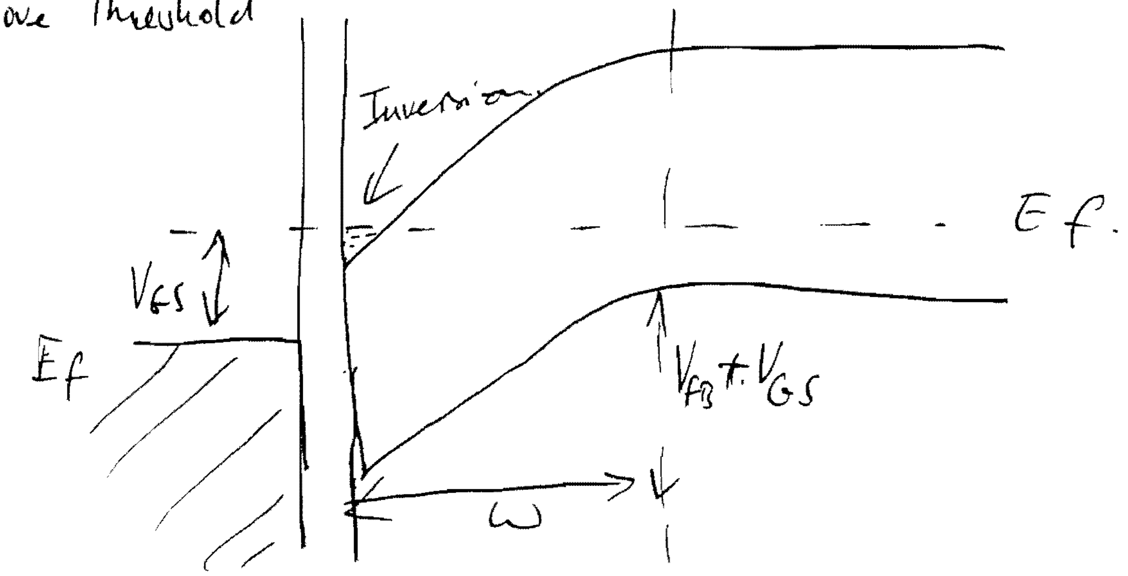
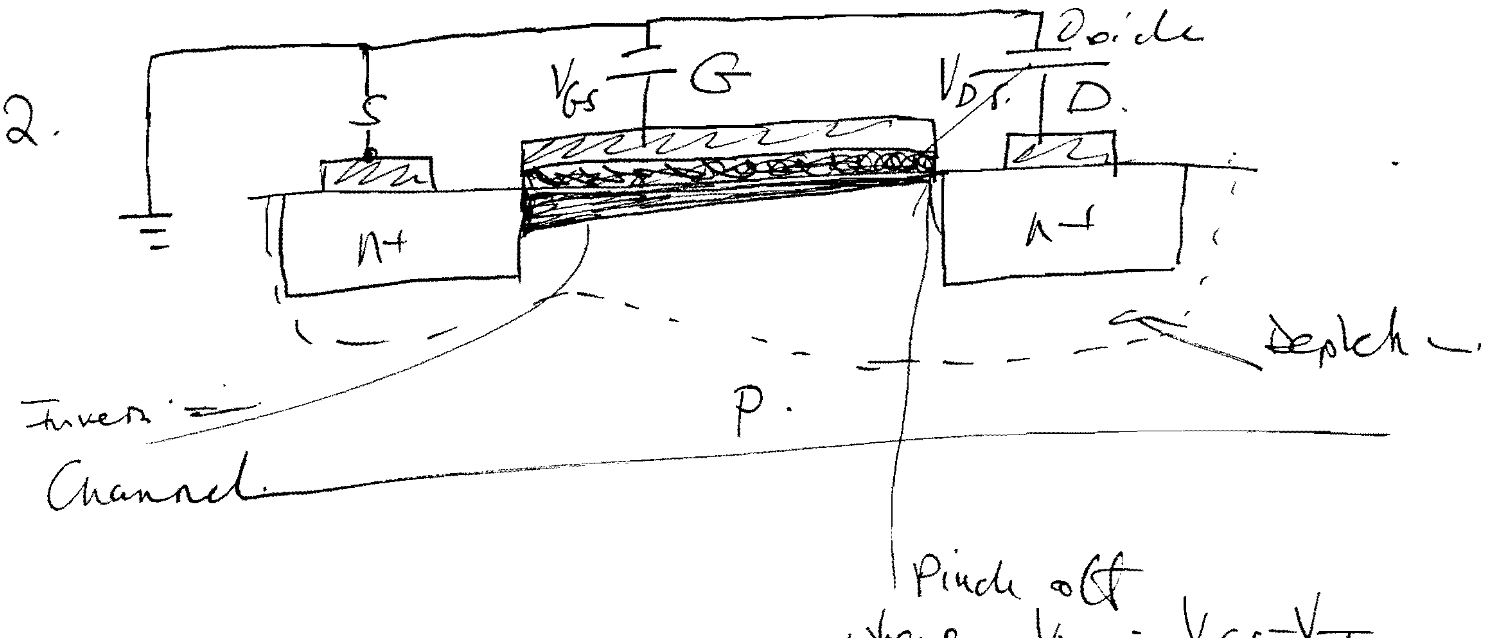
1a In equilibrium



b Above Threshold



2.



J and I must be continuous.

$J_D = n(x)\, q\, v \qquad I_D = A \times n(x)\, q\, v.$

area.

As the cross section reduces at pinch off $n(x)$ must increase to compensate. Due to the high $n(x)$, Electrons spread out towards the drain (at higher voltage than the gate) and also into the substrate, producing a broad elongated ~~channel~~ distribution. Lateral fields are very high → electrons reach saturation velocity → I_D independent (or only weakly dependent) on the drain voltage and is controlled by V_{gs}.

1c.

$f = f_T$ when current gain $= 1$.

i.e. when output current = input current

Output current $= g_m V_{GS}$

Input $= \omega C_{ox} Z L . V_{GS}.$

$\text{Out}/\text{In} = \dfrac{g_m V_{GS}}{\omega C Z L V_{GS}}. \qquad \omega = \dfrac{2\pi}{f}$

1c cont.

Given $g_m = \frac{2\mu C}{L}(V_{GS} - V_T)$

Substitute in

$$f_T = \frac{g_m}{2\pi C_{ox} Z L} = \frac{2\mu C_{ox}}{2\pi C_{ox} Z L}(V_{GS} - V_T)$$

$$f_T = \frac{\mu}{2\pi L^2}(V_{GS} - V_T).$$

Dependent on mobility and $\frac{1}{\text{gate length}^2}$.

State of the art CMOS

SiGe strained channel – electron mobility increased by factor of 2–3.

43/32 nm gate length used. (c.f. >90nm a couple of years ago). Short gate uses EUV lithography advances.

1d.

$$I_D = \frac{Z \mu C_{ox}}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS}.$$

$$I_D(2V) - I_D(1V) = 50\mu A$$

$$= \frac{Z \mu C_{ox}}{L}\left[V_{GS}^{2V} - V_{GS}^{1V} \text{ rest cancel}\right] V_{DS}.$$

$$= \frac{Z \mu C_{ox}}{L}[1] \cdot 0.1$$

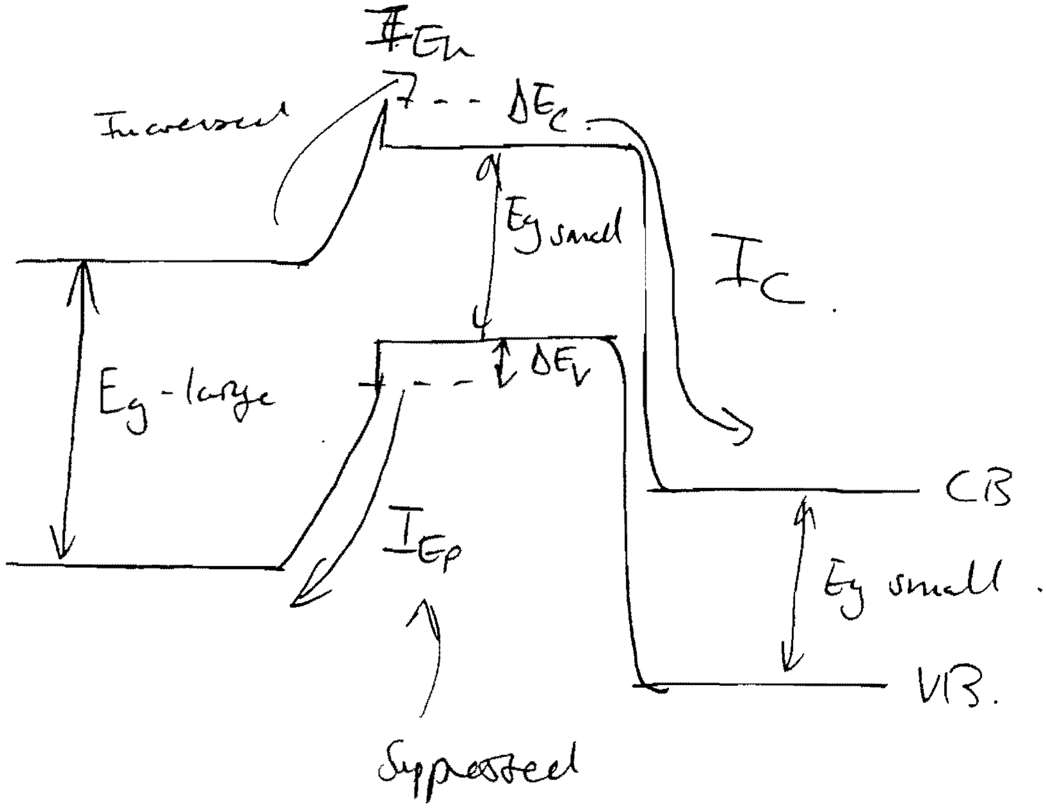
$$\mu = \frac{\Delta I_D \cdot L}{Z \cdot C_{ox} \cdot [0.1]}$$

$$\mu = 0.125 \ m^2 V^{-1} s^{-1}$$

$$1250 \ cm^2 V^{-1} s^{-1}$$

2a: HBT - wide gap emitter

Through a choice of an appropriate materials system can have $\Delta E_C \not> < \Delta E_V$ (eg: GaAs / AlGaAs).
Lower barrier for electrons than for holes.



E-B Heterojunction 'spike' needs to be graded, otherwise it will act as an addition barrier to I_{En}.

2b $\beta = \cancel{1200}\ 600 = \dfrac{\alpha\gamma}{1-\alpha\gamma}$

Assume $\alpha = 1$.

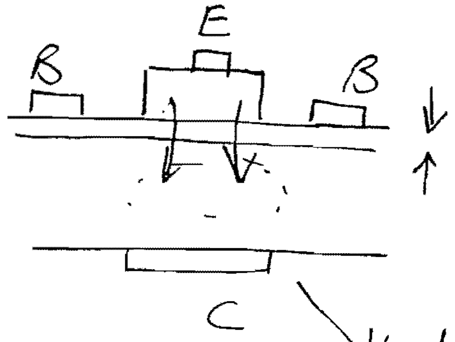
$600(1-\gamma) = \gamma \qquad 600 - 600\gamma = \gamma$

$\gamma = \dfrac{\cancel{1200}\ 600}{\cancel{1201}\ 601} = 0.998$

$I_C / I_E = \alpha\gamma \simeq \gamma \qquad I_C = 4.992\mu A \quad I_B = 8nA$

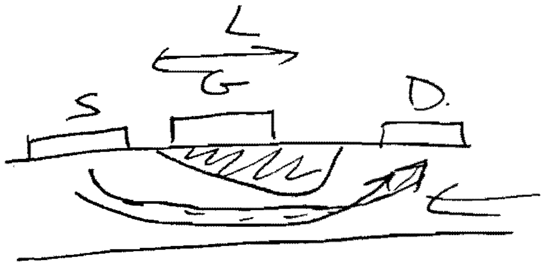
2c

Bipolar



Vertical current flow.
large area w.r.t. device size.

FET



lateral current flow.
small area compared to
FET surface area.

Large vertical area for current flow in the Bipolar case is more compatible with higher current density

f_T for FET is determined by gate length L.
for BJT is determined by base + collector thickness.

FET – gate length defined by lithography.
Difficult to have < 50nm gate length.
BJT – dimensions defined by epitaxy
in principle easy to have << 50nm layer dimensions

BiCMOS - uses CMOS logic gates, but has an additional step which includes bipolar devices on the output stages. Very good compromise compared to seperate IC

Advantages - BJT is faster, greater power handling.

Disadvantages - Expensive processing steps, BJT is power hungrey.

2d.

Base width = 75nm   Collector thickn 200nm

$r_c (\Omega)$	45	22	25.
$r_e (\Omega)$	26	26	30
$r_b (\Omega)$	300	380	120.
C_{cb} (fF)	4.0	4.0	5.0
C_{be} (fF)	(14)	10.5	9.6

$D_e = \mu \frac{kT}{q} = 0.026 \times 0.05 = 1.3 \times 10^{-3}\ m^2 s^{-1}$

$W_B / 2D_e = \frac{(75 \times 10^{-9})^2}{2 \times 1.3 \times 10^{-3}} =$

$\tau_{BE} = r_e C_{BE} =$	~~0.078~~ 0.384	~~0.0910~~ 0.273	~~0.080~~ p. 0.24
$\tau_{BC} = (r_e + r_c) C_{BC}$	0.213	0.168	0.176
$\tau_B = \frac{W_B^2}{2D_e}$ (ps)	2.16	2.16	2.16
$\tau_c = \frac{W_c}{2v_{sat}}$ (ps)	|	|	|
$\tau_{EC} = \sum \tau$ (ps)	3.737	3.601	3.571

$$f_T = \frac{1}{2\pi \tau_{EC}} = 42.5\ ,\ 44.1\ ,\ 44.5\ \text{GHz}$$

$$f_{max} = \left(\frac{f_T}{8\pi r_{bb'} C_{BC}}\right)^{1/2}$$

$$= 37.5\ ,\ 20.9\ ,\ 45.6\ \text{GHz}$$

3a. Moore's law - doubling of no. transistors / IC every 18 months (every 2 years in Moore's origional statement
Increase in density comes from continual advancement in lithographic techniques enabling smaller + smaller dimensions.

Moores law has similar relationships for transistor density, cost per transistor, processor speed etc. So in terms of processing performance then should also double in 18 mths.

Limitations for the future.
Lithography - although e-beam + x-ray are available, mass production favours EUV (optical) - already pretty much at the limitations of this due to λ.

Power density - struggling with high power dissipation
Not at the limit yet - V could be further reduced

Physical thickness of oxide <20nm QM tunneling - leakage (power dissip)
Short gate - low source to channel barrier height leaky channel.
Balistic transport regime (<20nm) - problems with pinch-off - Different design.

Parasitics, Parasitics Parasitics.

b) (i) Voltage - low operating V needed to reduce power dissipation

limited by V_T - with components from interface charge + channel doping

V_T currently ~0.3V needs to be >100mV otherwise off state current will be too large. Also logic swing needs to be $\geq 4kT$ (>100mV)

Current ULVP ~1.05V - this is a considerable advange on a few years ago (eg. before 2000 - 5V)
Not yet at the limit and there is potential to reduce to ~0.5V
But signal/noise degraded, also yield degraded because one needs much better tolerance
Ultimate limit - V_T fluctuations due to random dopant/impurity

(ii) Oxide

Need to maintain C_g and hence I_D ang g_m.

$I_D, g_m \propto \frac{1}{d_{ox}}$. However then QM tunneling

takes place through the gate leading to off-sta

power dissipation. SiO_2 reached its limits 2-3

years ago (few ML). Now use high K HfO_x and

a slightly thicker oxide - Increased capacitance

without further reduction in K.

Other higher K- systems being investigated -

materials challange.

(iii) Gate length

Reducing this increases g_m, I_D and f_T

Limits - now close to practical limits using EUV

technology + double exposure (45/32nm)

Can go lower with e-beam/x-ray lithographi

- expensive, not yet high volume methods.

Ballistic transport at <20nm - degraded channel

Ultimate limit will be QM tunelling ~~from~~

between Source + Drain (indep of gate) at

dimension less that 10nm

(iv) Interconnects

- These get smaller (higher density) - limits are due to increased resistance, mutual inductance + capacitive coupling

present approach uses copper and low k dielectric

Close to limits - copper is about the best material.

Partially overcome by using greater 3d. interconnection topographies.

Ultimately reach the limits of metal interconnect - may need ultra high mobility carbon based interconnects (nanotubes, graphene).

3b.

LVP $-0.35 + 2 \times 0.38 \ast \left(\frac{2 \times 1.6 \times 10^{-19} \times 12}{8.85 \times 10^{-12} \times 1 \times 10^{2}} \times 2 \times 0.38 \right)^{\frac{1}{2}}$

Cox.

5.08×10^{-4}

50.82

$C_{ox} = \frac{\varepsilon_r \varepsilon_0}{\text{thickness}}$

$= \frac{3.9 \times 8.85 \times 10^{-12}}{10 \times 10^{-9}} \ast = 3.45 \times 10^{-3}.$

$V_T = 0.76 - 0.35 + 0.147 = 0.557V.$

ULVP $-0.\cancel{4}8 + 2 \times 0.40 = 0.32$

$\left(2 \times 1.6 \times 10^{-19} \times 12 \times 8.85 \times 10^{-12} \times 5 \times 10^{22} \times 2 \times 0.4\right)^{1/2}$

$= 1.166 \times 10^{-3}$

$C_{ox} = \frac{7.5 \times 8.85 \times 10^{-12}}{\cancel{5} \times 10^{-9}} = \cancel{3}.32 \times 10^{-6}$

$0.32 + 0.03V.$

$V_T = 0.35 V$

V_T will be increased by the presence of the fixed interfacial charge. Increase will be Q_{iff}/C_{ox}.

From before

LVP $\quad C_{ox} = 3.45\times10^{-3}\ F\ m^{-2}$

ULVP $\quad C_{ox} = 1.32\times10^{-2}\ F.\ m^{-2}$

So

$Q/C \ = \ 0.290$ (LVP)

0.075 (ULVP).

V_T LVP $\quad 0.557 + 0.29 \ = 0.847$

ULVP $\quad 0.35 + 0.075 \ = 0.425$.

A substrate bias can be applied to counteract the fixed charge

$$E_{max} = \left(\frac{5 e N_D}{\epsilon \times 10^{-24}}\right)^{1/5} = 2.76 \text{ Vm}^{-1}$$

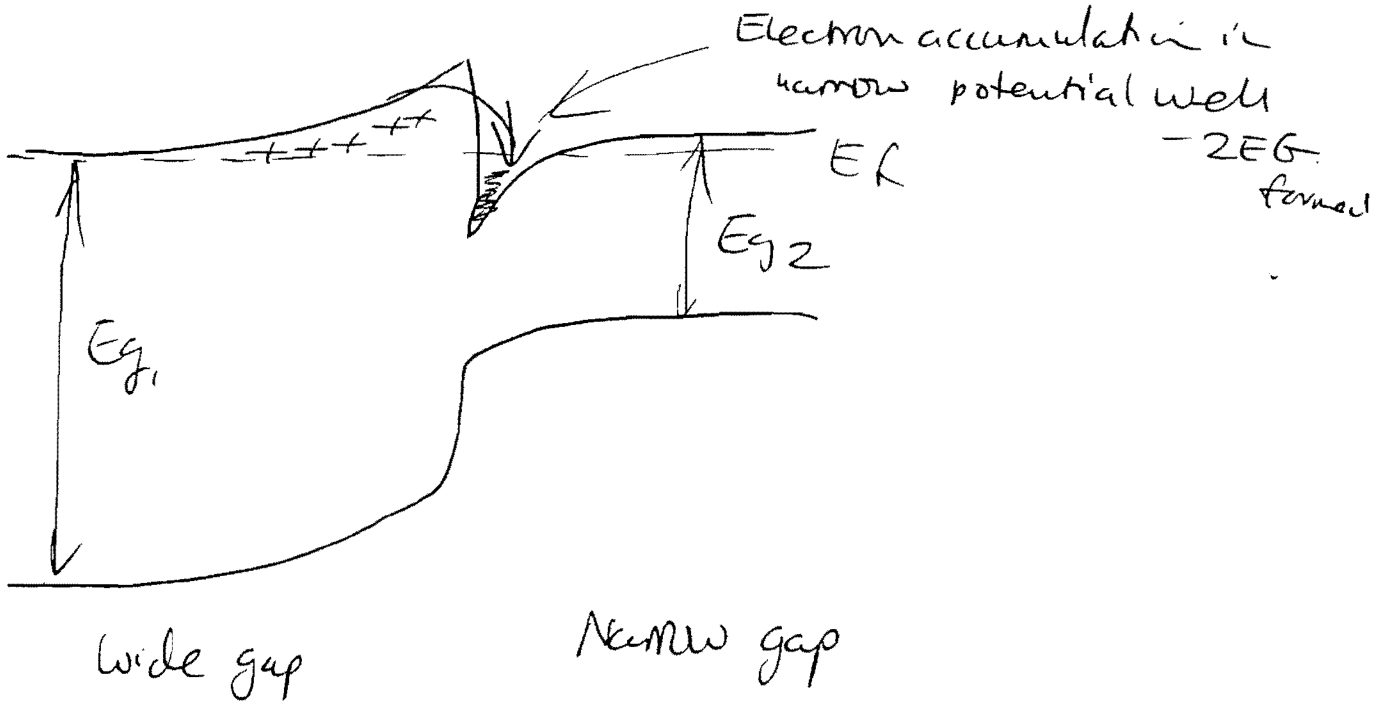
$$V = \frac{E_{max}}{2} \times L \qquad L = \frac{E_{max}\epsilon}{eN_D} \text{ (poisson)}$$

$$\text{So } L = \frac{2.09 \times 10^{7} \times 10^{10}}{1.6\times 10^{-19} \times 2\times 10^{21}} = 6.5 \mu m$$

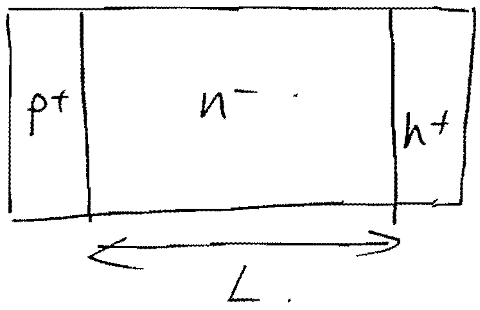
$$V \text{ (Breakdown)} = \frac{2.\cancel{79}6\times 10^{7}}{2} \times 6.5$$

$$= 67.9 V.$$

c.



4a. IMPATT.



$\tau = \frac{L}{V_{sat}}$

period $= 2\tau = \frac{2L}{V_{sat}}$ $f = \frac{1}{2\tau} = \frac{V_{sat}}{2L}$ $L = \frac{V_{sat}}{2f}$

$L = 0.588\,\mu m$.

Breakdown field $= 3\times10^{7}\,V.m^{-1} = \frac{V}{L}$

$V = 17.6\,V$

b) Avalanche condition $\int_0^L \alpha(E).dx = 1$.

$\frac{dE}{dx} = \frac{eN_D}{\varepsilon}$ So $dx = \frac{\varepsilon}{eN_D}.dE$

$\frac{\varepsilon\times10^{-24}}{eN_D}\int E^4.dE = 1$.

$\frac{\varepsilon\times10^{-24}}{eN_D}.\frac{E_{max}^5}{5} = 1$.

C. (Cont)

μ - increased due to spatial separation of electrons from their donors (reduced ionised impurity scattering)

Distance from the gate to the channel can also be low (<<100nm) - Gate acts effectively on the channel without field loss (doping can be very low above the channel)

so g_m + f_T both improved by increase in μ.

g_m increased and also more stable ~~to~~ due to close proximity

pseudomorphic - use a strained channel (eg: InGaAs in GaAs/AlGaAs based HEMT)

InAs/InSb - high μ, high v_{sat}. Advantageous to used an In containing channel.

InGaAs is strained to GaAs. However the strain can be accomodated if the strain is low (composition low) and the thickness is low)

$In_{.2}Ga_{.8}As$ and 10-20nm channel - well within critical thickness. Similar arguments apply for InGaN. Cannot increase the In content too much - dislocations

metamorphic

Use a channel composition beyond that of the pseudomorphic case - allow that by growing buffer layers that relax toward a new lattice constant which can accomodate the channel.

limitations - relaxation of the buffer layer - dislocations, morphology issues - device reliability?

4d $g_m = \dfrac{a 2 q N_D \mu}{L}$ $a N_D$ = 2DEG sheet conc $= N_S$.
$= 3\times10^{16}$

$$g_m = \frac{3\times10^{16} \times 1.6 \times10^{-19} \times 1.6}{150 \times10^{-9}} = 5.1\times10^{5}$$

$$f_T = \frac{1}{2\pi \tau_T} \qquad \tau_T = \frac{L}{V_{sat}} = \frac{150\times10^{-9}}{1\times10^{5}}$$

$= 1.5\,ps$

$f_T = 106\,GHz$.

$$g_m = \frac{a 2 q N_D \mu}{L} \qquad V_{sat} = \mu \frac{V_p}{L}. \qquad \mu = \frac{V_{sat}\, L}{V_p}$$

$$g_m = \frac{a 2 q N_D V_{sat}}{V_p}.$$

$$g_m = \frac{N_S\, q\, V_{sat}}{V_p} = 2.4\times10^{3}\ S.m^{-1}$$