Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (2 hours)

EEE6207 Advanced Computer Systems

Answer **THREE** questions. **No marks will be awarded for solutions to a forth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. **a.** Distinguish between Deadlock:

i. Prevention
ii. Avoidance
iii. Recovery
iv. Ignorance **(6)**

b. Explain what the graphical items, shown in **Figure 1A**, represent with reference to *Resource Allocation Graphs* (RAG).

(a) **(b)**

Figure 1A: Elements from Resource Allocation Graphs **(2)**

c. Explain the meaning of the three kinds of arcs that can be used to connect elements **(a)** and **(b)** from **Figure 1A**. **(3)**

d. Describe the system state that the RAG in **Figure 1B** represents.

Is the system in **Figure 1B** *deadlocked*? Show why this is the case (by reducing the graph).

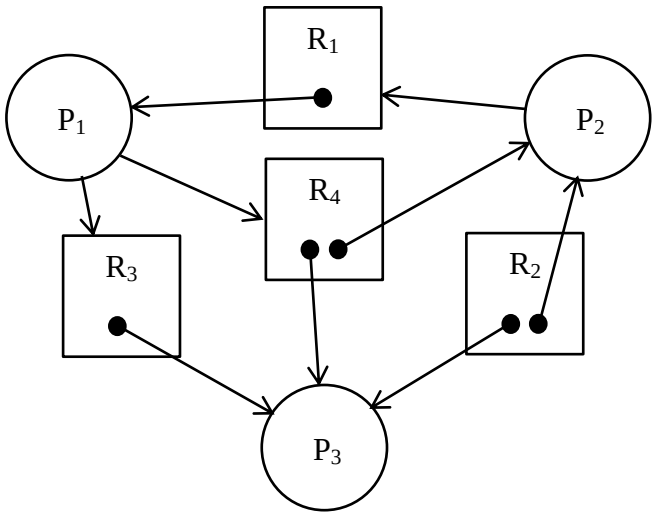

Figure 1B: Resource Allocation Graph

(5)

e. A dotted arc is added to the RAG in **Figure 1B**, pointing from P_3 to R_1. Comment on what this might mean about whether the system is Deadlocked. **(4)**

2. A pipelined system is as shown in **Figure 2**.

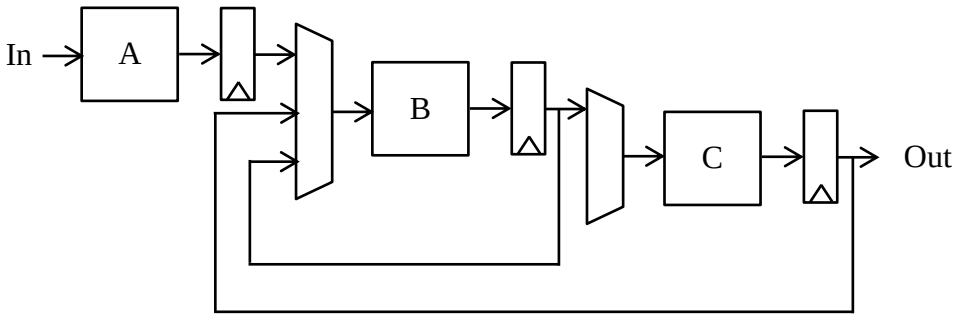

Figure 2: A Processing Pipeline

The sequence of processing is as follows:

$$\text{In} \rightarrow \text{A} \rightarrow \text{B} \rightarrow \text{C} \rightarrow \text{B} \rightarrow \text{B} \rightarrow \text{C} \rightarrow \text{Out}$$

a. Draw the reservation table for this sequence of processing **(6)**

b. Calculate the throughput and the utilisation of the processors. **(2)**

c. You recognise that there is a simple way to improve performance (without replicating any of the functional blocks).

Identify this simple way of improving performance. **(4)**

Calculate the improved throughput. **(3)**

d. You need to improve the performance to 0.5 datum / clock cycle. How would you do this? **(5)**

3. **a.** Identify the states that a *process* can be in and the transitions between the various states (e.g. what conditions can give rise to a transition). **(3)**

b. Distinguish between a blocking and non-blocking call (made, for example, for the purposes of *inter-process communication*). **(2)**

c. Describe the elements of a typical semaphore. **(3)**

d. **i.** What problems are encountered in implementing a semaphore practically? **(2)**

ii. Describe a practical implementation of a semaphore that addresses these problems (in particular, identifying hardware mechanisms that must exist). **(4)**

e. Two processes must communicate with each other. The first process, ***A***, initiates the process by sending data to the second process, ***B***. ***B*** then responds by sending data back to ***A***. The process repeats. Show how this communication should be performed (either using semaphores and shared memory or other *inter-process communication* constructs that might be available in typical operating systems). **(6)**

4. **a.** A set of processors is connected by a *cross-point switch* to a number of disjoint memory modules:

i. Draw a schematic to represent this system organisation. **(2)**

ii. What is the principal feature of the cross-point switch that helps to improve performance in this system organisation. **(2)**

b. The probability, P_A, that a memory access issued by a processor in part **a.** goes ahead without being blocked is:

$$P_A = \frac{M}{NRT_{acc}}\left(1 - \left(1 - \frac{RT_{acc}}{M}\right)^N\right)$$

What do each of the terms in this equation mean and what assumptions are used to arrive at this equation. **(4)**

c. If a particular memory access through the *cross-point switch* is blocked (by another memory access) then the processor must try again (in the next time-slot) until it successfully completes the transfer of data. In this case, show that the effective access time (using relevant terms from the equation above) is:

$$accesstime = \frac{T_{acc}}{P_A}$$

(4)

d. Eight processors must be connected via a *cross-point switch* to a set of memory blocks (the number of which blocks is to be determined). Each processor is generating 10^9 memory accesses per second. However, there is an internal cache in each processor such that the overall miss rate on a cache is 1%. If a processor does miss, the basic time to complete a memory operation through the *cross-point switch* to the memories is 50ns.

Derive an expression to identify the relative performance of systems with different numbers of disjoint blocks of memory (hint: consider how long it takes to complete the number of accesses that should be completed within one second). **(8)**

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