EEE225 Problem Sheet 4 - NJP

1. A simple processor has an 8 bit data bus and an 8 bit address bus. It needs to communicate with 4 peripheral devices each of which has an 8 bit data bus, a 6 bit address bus and an active high chip select line (CS). Show with the aid of a diagram how this can be achieved.

2. An Ethernet card needs to be interfaced to a computer CPU. Describe how it could be achieved as (i) an isolated I/O device (ii) a memory mapped device.

3. A small computer system with a 16-bit wide address bus is required to contain two memory chips: a 4K x 8 ROM chip and a 1K x 8 SRAM chip.

   Each of these chips is to be based at the following addresses:

   4K x 8 ROM 0000H
   1K x 8 SRAM 1000H

   Draw a memory map of the proposed system.

   Draw a circuit diagram of the memory interfacing circuitry together with suitable logic circuitry to locate the chips at their required addresses.

   In such a system, why would the ROM chip usually be based at 0000H?

4. Repeat the design described in Question 3 above but this time for a system in which there are three 4K x 8 memory chips.

   For a 16-bit wide address bus and therefore a total memory space of 64K, only the bottom 12K will be used. What is the consequence of this?

5. How many comparators would be required for a 10-bit flash ADC?

6. Sketch the diagram for a 2-bit flash ADC with a 10V reference voltage. Describe how an 8V analog input would be converted.

7. An analog signal which can vary between 0 to 15 volts is to be converted to an 8-bit digital value. Calculate the correct encoding for 5V. Show with a series of register values, how a successive approximation method would reach this value. Consider the MSB of the SAR digital-to-analog converter to output 7.5V and each subsequent bit to give half of the previous value.