Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2010-2011 (2 hours)

EEE331 Analogue Electronics 3

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

1. a. Sketch the behaviour of collector current versus base current for a bipolar junction transistor (BJT) in common emitter configuration, taking into account both leakage and clipping. Explain the difference between small signal current gain (β) and large signal current gain (h_{FE}) and state when they are identical. **(5)**

b. Using the standard Ebers-Moll equation for the collector current of a BJT, derive an expression for its transconductance. Comment on its temperature dependence: will it go up or down with temperature, and how much will its relative change be if the BJT heats up from room temperature (20°C) to 80°C? **(4)**

c. (i) Name the transistor circuit shown in Figure 1.
(ii) Explain the functions of all resistors and capacitors marked.
(iii) Calculate the voltage gain.
(iv) Draw a small signal equivalent circuit that would be appropriate for high-frequency signals. Neglect the emitter capacitance but take the Miller effect into account
(v) Calculate approximate transition frequencies for input and output side.
(vi) Which will dominate for large voltage gains?

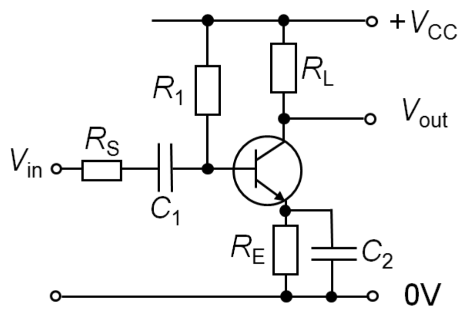

Figure 1

(8)

d. Explain the different bias settings of class B and class C amplifiers using appropriate diagrams. Compare qualitatively the differences with respect to distortion, sensitivity, maximum voltage swing at input and power consumption. **(3)**

2. **a.** Sketch the circuit for a Darlington pair of two different transistors T_1 and T_2 with signal resistor R_S at T_1 and load resistor R_L at T_2. Determine the voltage gain under the approximation that both small signal current gains β_1 and β_2 are >>1. Explain which of the transistors influences the voltage gain more strongly. **(5)**

b. (i) Calculate for the Wilson current mirror shown in Figure 2 the ratio of output to input current for the general case that all three transistors have different small signal current gains of β_i, i=1,2,3. Assume the base currents to transistors T_1 and T_2 at point B are equal. Neglect the Early effect.

(ii) Which transistor has the least effect on the current ratio and why?

(iii) Show that for that case that all transistors are identical ($\beta_1=\beta_2=\beta_3=\beta$) and β>>1 the result approximates to $1/(1+2/\beta^2)$.

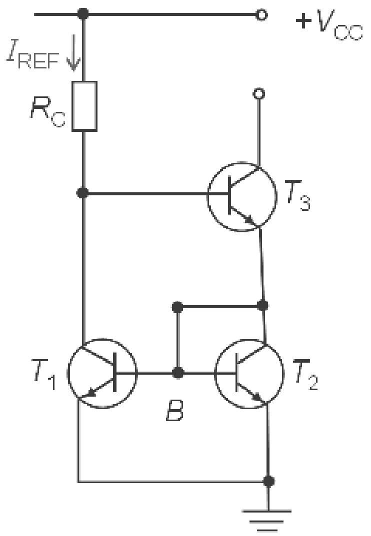

Figure 2 **(6)**

c. Sketch the circuit for a cascode pair with BJTs, including input and output voltage connections. Derive the small signal expression for its current gain and compare this to a single BJT in common emitter configuration. **(3)**

d. Identify the type, function and configuration of the BJTs in figure 3, state the classes of both amplifiers and draw a sketch of their characteristics. Which will have the smoother transfer characteristic?

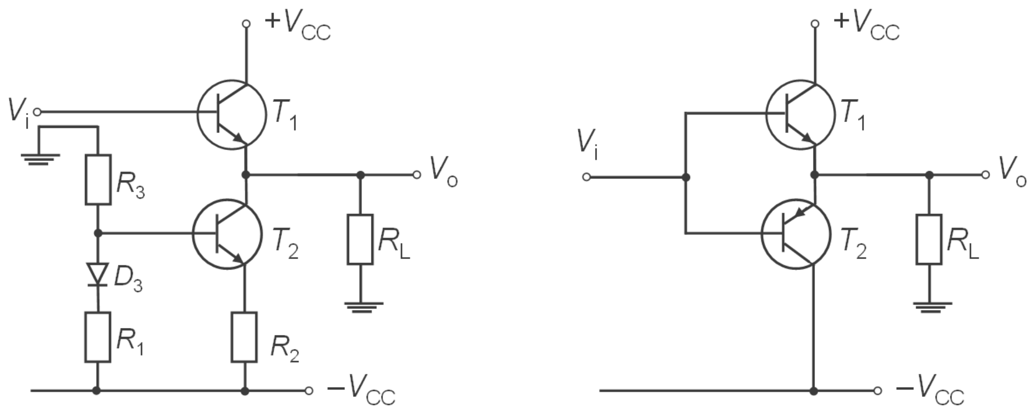

Figure 3 **(6)**

3. **a.** (i) Sketch the small-signal hybrid-π equivalent model of a metal-oxide-semiconductor field effect transistor (MOSFET). Neglect all body or substrate effects.

(ii) Derive an expression for the small signal current gain, assuming for the transconductance $g_m >> \omega C_{GD}$. Use the standard square-model for the drain current and the definition of the transconductance to express the transconductance in terms of drain current i_D and overvoltage V_{ov}.

(iii) Inserting this into the expression for the transition frequency f_t (where gain is unity), show that the result is $f_t = i_D/[\pi V_{ov}(C_{GS}+C_{GD})]$.

(iv) What does this mean for the physical design of improved MOSFETs? **(6)**

b. The square law model for the drain current of a MOSFET in the saturation region states $i_D = ½\, \mu\, C_{ox}\, W/L\, (V_{GS} - V_{to})^2$ where μ is the carrier mobility, C_{ox} the specific oxide capacity per oxide area and W and L are the width and the length of the transistor channel, respectively.

(i) Considering the MOSFET as a plate capacitor of area $A=WL$, calculate the drain current density.

(ii) Explain for given materials which design parameters for the MOSFET layout are important to achieve a high drain current density.

(iii) If you take into account that you cannot increase V_{GS} significantly without risking breakdown due to high electric fields across the gate oxide, which is the most important design parameter? **(4)**

c. Sketch the phenomenon of latch-up for a complementary pair of a p-channel MOSFET T_1 and an n-channel MOSFET T_2 that are fabricated on the same n-doped substrate. Explain what latch-up is, why it occurs and what the consequences can be. Explain the benefit of a dielectric with low dielectric constant to encapsulate T_2. **(7)**

d. Consider an active loaded MOSFET differential amplifier with two matched transistors T_1 and T_2 with the following technical specifications: W/L=200, μC_{ox}=0.2mA/V^2, V_{SS}=12V, I=0.4mA, R_{SS}=20kΩ. Calculate overdrive voltage V_{ov}, conductance G_m, output resistance R_0, differential mode gain A_{dm}, common mode gain A_{cm} and common mode rejection ratio (CMRR) in dB. **(3)**

4. **a.** Name the order and type of filter shown in Figure 4. Justify qualitatively its frequency behaviour. Derive its corresponding leap-frog structure. Write down the equations for all components.

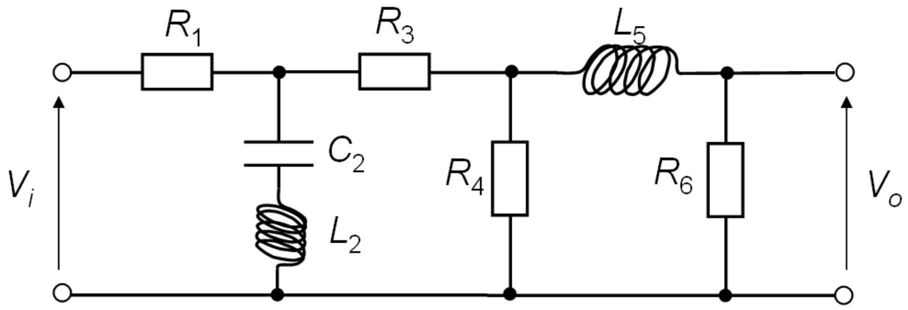

Figure 4 **(6)**

b. Find the zeros and poles and sketch the Bode plot of the magnitude <u>and</u> phase of the transfer function $T(s) = s^3/[(1+s/10)(1+s/10^2)(1+s/10^5)(1+s/10^6)]$. Name the order and the type of the filter. What is the transition frequency of unity gain? Considering both gain and phase margins, state over which frequency range this transfer function would be stable and whether it would be a good high-frequency amplifier. **(8)**

c. Sketch a block diagram of a non-inverting voltage amplifier with frequency-dependent amplification factor $A(s)$ and feedback $F(s)$. Calculate

(i) the loop gain,

(ii) the voltage gain,

(iii) the de-sensitivity factor.

Show from this for a single-pole amplifier with mid-band gain A_m, where $A(s)=A_m / (1+s/\omega_t)$ for a pole frequency ω_t and frequency-independent feedback F that the product of gain and bandwidth is constant. Explain this using a simple Bode plot. **(6)**

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