Data Provided: None

The University Of Sheffield.

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

Spring Semester 2014-15 (3.0 hours)

EEE225 Analogue and Digital Electronics

In **Part A**, answer **FIVE** questions. **No marks will be awarded for solutions to a sixth question. In Part B,** answer **all questions**. Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

Physical constants:

Charge on electron:	-1.602×10^{-19} C
Free electron rest mass:	$m_0 = 9.110\times10^{-31}$ kg
Speed of light in vacuum	$c = 2.998\times10^{8}$ m s^{-1}
Planck's constant:	$h = 6.626\times10^{-34}$ Js
Boltzmann's constant:	$k = 1.381\times10^{-23}$ JK^{-1}
Melting point of ice:	0^{o}C = 273.2 K
Permittivity of free space:	$\varepsilon_0 = 8.854\times10^{-12}$ Fm^{-1}
Permeability of free space:	$\mu_0 = 4\pi\times10^{-7}$ Hm^{-1}

PART A

1. Describe with the aid of a diagram the operation of a single-bit SRAM cell, based upon two inverters and two n-channel pass transistors. Explain how both *read* and *write* operations are achieved. **(8)**

2. **a.** Show how a transmission gate can be formed from a pmos and nmos transistor.

b. What is the reason for using complementary transistors in a transmission gate?

c. Show how a 2-to-1 multiplexer could be formed using transmission gates. **(8)**

3. **a.** With the aid of block diagrams, compare the structure of a TTL logic gate with that of a CMOS logic gate.

b. How would you increase the fan-in for each technology? **(8)**

4. **a.** For the pole-zero circuit of figure 4a, write down the low frequency gain and the high frequency gain, v_o/v_i, in terms of circuit components. **(2)**

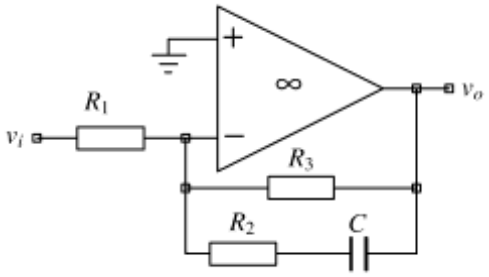

Figure 4a

b. The transfer function of the pole-zero circuit of figure 4a is

$$\frac{v_o}{v_i} = -k\frac{1+j\dfrac{\omega}{\omega_0}}{1+j\dfrac{\omega}{\omega_1}}$$

Where $k = \dfrac{R_3}{R_1}$, $\omega_0 = \dfrac{1}{1+j\omega CR_2}$ and $\omega_1 = \dfrac{1}{1+j\omega C(R_2+R_3)}$.

Sketch a bode plot of the transfer function assuming that ω_1 is much lower in frequency than ω_0. Label the plot with key frequencies, gains and phase shifts. **(6)**

5. A particular amplifier has an infinite input resistance, a voltage gain of 50 V/V and equivalent input noise voltage generator of 4 nV $Hz^{-1/2}$ and 0.01 pA $Hz^{-1/2}$ respectively. The amplifier is fed by a noisy source resistance of 0.6 kΩ. The noise voltage of a resistor $R = \sqrt{4\,k\,T\,R\,\Delta f}$ nV/$\sqrt{\text{Hz}}$ where the symbols have their usual meanings.

a. Draw a noise equivalent circuit of the amplifier and source. **(4)**

b. With an input signal amplitude of zero, the amplifier output voltage is measured using a true rms voltmeter with a noise bandwidth of 20 kHz. What rms noise voltage would you expect the meter to indicate? **(4)**

6. A particular operational amplifier used with negative feedback applied is observed to have a closed loop gain of 1 and behave like a first order system in terms of its frequency response and output when driven by a step input.

a. State the equations in the time and frequency domain that the amplifier obeys. **(2)**

b. Describe the unity gain compensation scheme that the operational amplifier designer has used in order to achieve this response. *(Hint: To obtain full marks your description must include a sketch of the open loop bode plot before and after* **(6)**

compensation.)

7. Starting from the charge neutrality condition and assuming that the acceptor and donor doping densities in a semiconductor are known, derive expressions from which the equilibrium majority and minority carrier concentrations can be estimated for,

i) an n-type extrinsic doped semiconductor, and

ii) a compensated near-intrinsic doped structure.

(Hint: State any assumptions that you make. You must show the derivation for full marks)

(8)

8. Show clearly the conduction band, valence band and Fermi-level positions of a semiconductor p-n junction laser under lasing conditions.

Draw a typical light output versus junction current characteristic for this device and identify the different regions.

Sketch the typical spectral output (as a function of wavelength) of such a device when it is biased well below the lasing threshold current.

(8)

9 Draw the band diagram for an ideal metal- n-type semiconductor junction in equilibrium for the cases when:

i) the junction rectifies

ii) the junction is ohmic

Make clear the relative work functions for the metal and semiconductor in both cases, the position of the Fermi levels and the magnitude of any potential barrier.

State the direction of majority and minority current flow for the case of the rectifying junction when it is forward and reverse biased.

(8)

PART B

10. a. A 4-bit Digital-to-Analog Converter is shown in **Figure 10.**

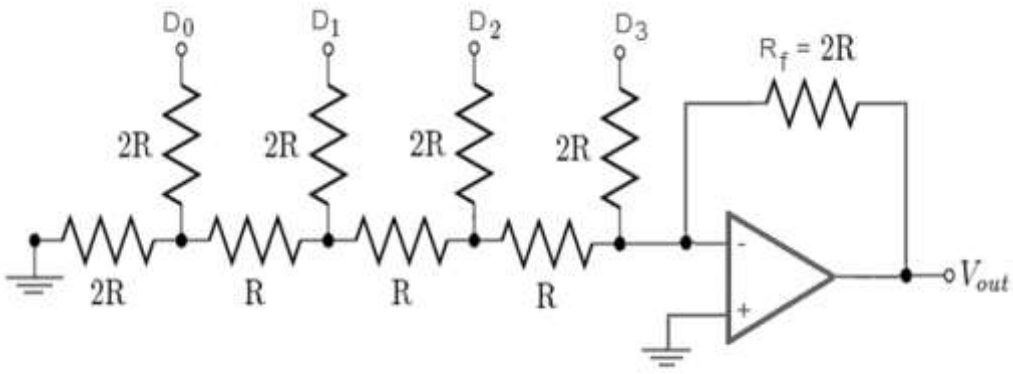

Figure 10. R-2R ladder DAC.

For input voltage levels of 3.3V, calculate the output voltage for the input $D_0D_1D_2D_3 = 1101$. **(8)**

b. The following Verilog code describes a certain logic gate at the switch-level.

```
module mygate(Y,A);
input A;
output Y;
supply1 POWER;
supply0 GROUND;
pmos t1 (Y, POWER, A);
nmos t2 (Y, GROUND, A);
endmodule
```

Draw a transistor-level circuit diagram for this logic gate. Produce a table indicating the state of each of the transistors for all possible combinations of the input **A**. Hence, deduce the logic function of the gate.

A 500Ω resistive load is connected between the output of the gate (Y) and GROUND. The supply (POWER) is set to 3.3V and the input (A) is set to 0V.

Calculate the current flowing through the resistive load and the voltage at the output (Y) of the gate.

You may assume that the *on* resistance (R_{DS}) of a pmos transistor is 75Ω and that of an nmos transistor is 25Ω. The *off* resistance for both transistors is 500,000 Ω. **(12)**

11. a.

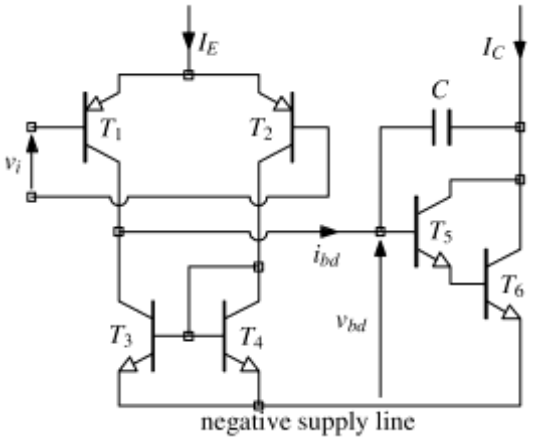

Figure 11a

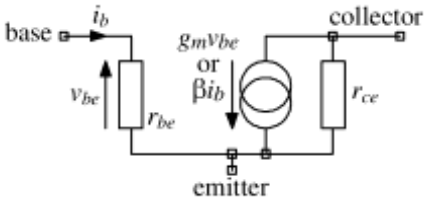

Figure 11b

Figure 11a shows the simplified circuit diagram of the input stages of a typical operational amplifier. All the transistors used have large signal and small signal current gains of 250.

i) State the main purposes of the transistor pairs (T_1 and T_2), (T_3 and T_4) and (T_5 and T_6). **(6)**

ii) Using the small signal equivalent circuit of figure 11b show that the input resistance of the T_5, T_6 combination, $r_i = v_{bd}/i_{bd}$, is

$$r_i = r_{be5} + (\beta_5 + 1) r_{be6}$$

(5)

You can assume here that r_{ce} is so large that its effects can be neglected.

You may find the relationships $g_m = \frac{eI}{kT}$, $r_{be} = \frac{\beta}{g_m}$, $h_{FE} = \frac{I_{Coll}}{I_{Base}}$ useful in this question. Assume that $kT/e = 0.026$ V.

b. **i)** A particular amplifier with a dc gain of 100 V/V is observed by experiment to behave like a first order system. Measurement shows that the magnitude of amplifier gain has dropped to 50 V/V at a frequency of 120 kHz. Calculate the -3dB frequnecy. **(4)**

ii) A different amplifier has a GBP = 100 kHz. Evaluate the |gain| and phase shift of this amplifier at a frequency of 75 kHz. **(2)**

iii) It was also observed that at 0.05 MHz the biggest sinusoidal signal that could be obtained at the amplifier output without evidence of slew rate limiting was 3 Vrms. Calculate the amplifier slew rate. **(3)**

12. a. An n-type semiconductor with work function 3eV is sandwiched between two metal contacts, M1 with work function 4eV, and M2 with work function 1eV. The resistance of the bulk semiconductor between the contacts is 2Ω. When a DC voltage of +1.5V is applied across the two metal contacts, a large current of 500mA flows. When the polarity of the voltage is reversed, the current that flows is reduced significantly.

Identify the type of metal-semiconductor we have with M1 and M2.

Calculate the magnitude of the reduced current that flows when the voltage was reversed. **(10)**

b. The unsaturated drain characteristic of an induced channel enhancement mode metal-oxide-silicon-transistor (MOST)device can be represented by:

$I_d = \frac{\mu_e C_g}{l^2}\left[V_{gs} - V_T - \frac{V_{ds}}{2}\right]V_{ds}$, where the symbols have their usual meaning.

How does I_d vary with V_{gs} when $V_{gs} - V_{ds} - V_T < 0$?

The source terminal of such a MOST is grounded and the drain terminal is connected directly to the gate terminal. If $\mu_e C_g / l^2 = 4 \times 10^{-4}$ A V^{-2} and $V_T = 2.0$V. Find I_d when V_{ds} =1V, 3V and 4V. **(10)**

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