**Data Provided: None**

The University Of Sheffield.

## DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

**Spring Semester 2006-2007 (2 hours)**

**Introduction to VLSI Design 3**

Answer **THREE** questions. **No marks will be awarded for solutions to a fourth question.** Solutions will be considered in the order that they are presented in the answer book. Trial answers will be ignored if they are clearly crossed out. **The numbers given after each section of a question indicate the relative weighting of that section.**

**1. a. i.** Design a standard-CMOS, transistor-level circuit for an XOR function of two inputs, $A$ and $B$ (hint: $Y = A \oplus B = A.\overline{B} + \overline{A}.B$) and size the transistors for a minimum sized gate. **(8)**

**ii.** How would you change the circuit in part **1.a.i** to produce an XNOR function. **(2)**

**b. i.** Draw a circuit diagram to show how a two input XOR function could be implemented using two transmission gates (TG) and a few inverters. **(6)**

**ii.** How, optimally, would the circuit in part **1.b.i** be changed to produce an XNOR function? **(1)**

**iii.** Does the TG approach to implementation have any advantages or disadvantages over the standard-CMOS approach? If so, what are they? **(3)**

**2.** The circuit in **Figure 2** (which is somewhere inside an IC and part of a bigger circuit) must be altered to allow it to be tested.

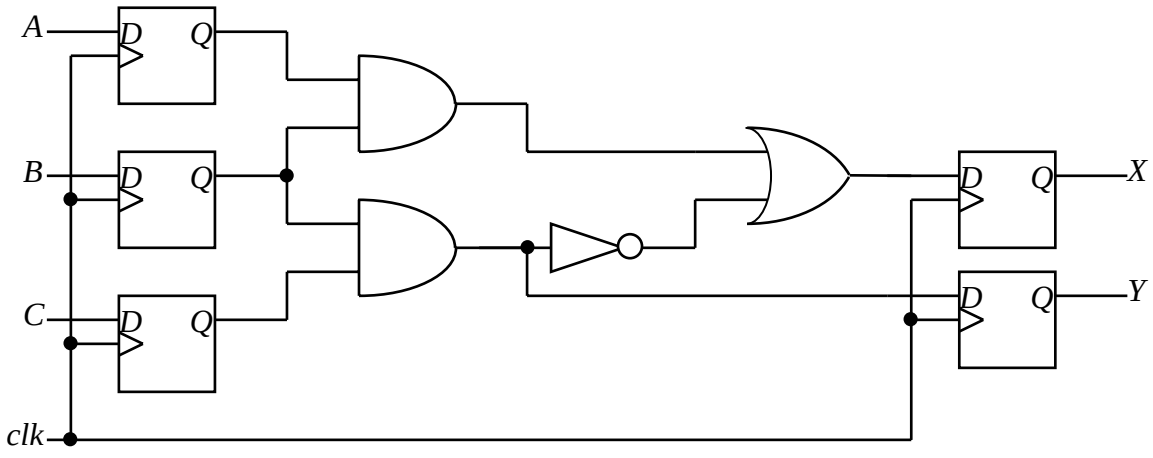


**Figure 2**

**a.** **i.** What changes must be made to the circuit to allow it to be tested (draw a diagram to show what must be done)? **(4)**

**ii.** Assuming a simple stuck-at fault model, identify how many individual tests must be applied and the associated test vectors. **(8)**

**iii.** Are there any problems with testing this particular part of the circuit? **(2)**

**b.** What is BIST and how is it used? What is the significance of the *signature*? **(4)**

How is communication normally made between the outside of an IC and the test structures inside the IC? **(2)**

**3.** A 0.13µm digital IC can be modelled as being equivalent to $15x10^6$ simple, 2-input gates where each gate has, on average, the equivalent of 35µm of wire connected to its output. Each gate has an input capacitance of 3fF on each input and an effective output capacitance of 1.5fF. The wiring, on average, has a capacitance equivalent to 0.2fF/µm.

The IC is clocked at 2GHz with a power supply voltage of 1.8V and, on average, the probability of any wire changing state on the rising edge of the clock is 0.15.

**a.** Derive an expression for the power dissipation in a digital CMOS circuit due to switched capacitance. **(4)**

**b.** **i.** What is the total capacitance that is being switched in the IC? **(2)**

**ii.** What is the power dissipation of the IC, due to switched capacitance, under the stated conditions? **(4)**

**c.** **i.** What is other major contributor to the overall dynamic power dissipation apart from switched capacitance? **(2)**

**ii.** What factors give rise to static power dissipation – what is happening to static power dissipation as the technology is shrunk? **(4)**

**d.** The technology that is used to fabricate the IC is shrunk to 90nm (so that linear dimensions reduce by a factor of 1.4). Estimate, simply, what *might* happen to the power dissipation due to switched capacitance, stating any assumptions that you make. **(4)**

**4.** The circuit in **Figure 4** implements a logic function but is not implemented as a standard CMOS circuit.

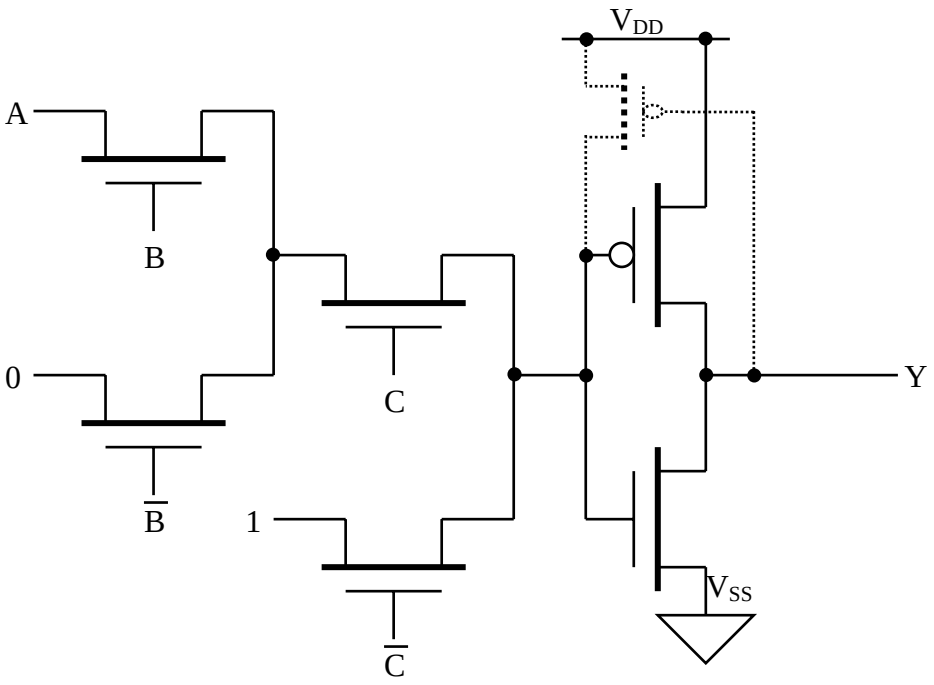


**Figure 4**

**a.** What is the logical function of the circuit (*Hint: you can ignore the dotted transistor when determining the function)*? **(8)**

**b.** Why do you think that the dotted transistor (shown smaller here to denote that it is a *weak* transistor – reduced current drive) is included in the circuit – make sure you describe its purpose? **(4)**

Why is a *weak* transistor needed as opposed to a transistor of normal drive strength? **(4)**

How would you make a *weak* transistor? **(2)**

**c.** In the circuit in Figure 4 there are more *n*-type than *p*-type transistors. Does this make any difference to circuit layout? **(2)**

**NLS / MB**