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Computer Architecture Lab 9 Week 11

Task1:

START:

INP

STA NUM

INP

OR NUM

OUT

HALT

NUM: .data 1 0

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 1
Enter Inputs, the first of which must be an Integer: 0
Output:  1
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

The OR gate outputs 1 if at least one input is 1.
Since one input is 1, the result is 1.

Task2:

START:

INP

STA NUM

INP

NAND NUM

OUT

HALT

NUM: .data 1 0

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 0
Enter Inputs, the first of which must be an Integer: 1
Output:  -1
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

NAND gives the opposite result of the AND gate.
Since one input is 0 and other is 1, AND gives 0, so NAND gives 1.

Task3:

START:

INP

STA NUM

INP

NOR NUM

OUT

HALT

NUM: .data 1 0

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 0
Enter Inputs, the first of which must be an Integer: 1
Output:  -2
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

NOR is the inverse of the OR gate.
Since one input is 1 and other is 0, so OR gives 1 and NOR gives 0.

Task4:

START:

INP

STA NUM

INP

XOR NUM

OUT

HALT

NUM: .data 1 0

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 1
Enter Inputs, the first of which must be an Integer: 0
Output:  1
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

XOR gives 1 only when the inputs are different.
Since one input is 1 and other is 0, so the result is 1.

Task5:

START:

INP

STA NUM

NOT NUM

OUT

HALT

NUM: .data 1 0

```
EXECUTING...
Enter Inputs, the first of which must be an Integer: 1
Output:  -2
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

The NOT gate inverts the input value.
Since the input is 1, the result becomes 0.