Chapter 9

Multiple Choice Questions

1. Computing systems need cache because
A) accessing main memory is slow and cache speeds it up.
B) register access is slow and cache speeds it up.
C) main memory is expensive and cache offsets the cost.
D) All of the about.

Ans: A
Feedback: 9.1.1
Difficulty: Easy

2. Which of the following statement is correct?
A) Base register holds the size of a process.
B) Limit register holds the size of a process.
C) Base and limit registers can be loaded by the standard load instructions in the instruction set.
D) Any attempt by a user program to access memory at an address higher than the base register value results in a trap to the operating system.

Ans: B
Feedback: 9.1.1
Difficulty: Medium

3. If the base register is loaded with value 12345 and limit register is loaded with value 1000, which of the following memory address access will not result in a trap to the operating system?
A) 12500
B) 12200
C) 13346
D) 12344

Ans: A
Feedback: 9.1.1
Difficulty: Easy

4. Assume the value of the base and limit registers are 1200 and 350 respectively. Which of the following addresses is legal?
A) 355
B) 1200
C) 1551
D) all of the above

Ans: B
Feedback: 9.1.1
Difficulty: Easy

5. _____ is the method of binding instructions and data to memory performed by most general-purpose operating systems.
A) Interrupt binding
B) Compile time binding
C) Execution time binding
D) Load-time binding

Ans: C
Feedback: 9.1.2
Difficulty: Medium

6. If the starting address location changes, in which of the following cases, the program has to be recompiled?
A) Execution time binding.
B) Load time binding.
C) Compile time binding
D) Both compile and load time bindings.

Ans: C
Feedback: 9.1.2
Difficulty: Easy

7. If execution time binding is used,
A) logical addresses of process may change over time but physical addresses remain the same.
B) physical addresses of process may change over time but logical addresses remain the same.
C) both physical and logical addresses may change over time.
D) both physical and logical addresses remain the same over time.

Ans: B
Feedback: 9.1.3
Difficulty: Medium

8. Suppose the size of a process is 10,000 bytes and the relocation register is loaded with value 5000, which of the following memory address this process can access?
A) logical address 10,350
B) physical address 4,500
C) physical address 10,350
D) None of the above

Ans: C
Feedback: 9.1.3
Difficulty: Easy

9. An address generated by a CPU is referred to as a ____.
A) physical address
B) logical address
C) post relocation register address
D) Memory-Management Unit (MMU) generated address

Ans: B
Feedback: 9.1.3
Difficulty: Easy

10. Suppose a program is operating with execution-time binding and the physical address generated is 300. The relocation register is set to 100. What is the corresponding logical address?
A) 199
B) 201
C) 200
D) 300

Ans: C
Feedback: 9.1.3
Difficulty: Easy

11. Which of the following is true about dynamic storage allocation?
A) Worst fit provides the best storage utilization.
B) First fit requires less time for allocation than worst fit on average.
C) Best fit is clearly better than first fit in terms of time and storage utilization.
D) First fit is clearly better than best fit in terms of time and storage utilization.

Ans: B
Feedback: 9.2.2
Difficulty: Difficult

12. External fragmentation is
A) when there is some unused memory that cannot be allocated to a process.
B) when the amount of available memory is less than the size of a process.
C) when a process is broken up into smaller parts for memory allocation.
D) when there is enough total memory space to satisfy a request but the available spaces are not contiguous.

Ans: D
Feedback: 9.2.3
Difficulty: Medium

13. Consider a logical address with 18 bits used to represent an entry in a conventional page table. How many entries are in the conventional page table?
A) 262,144
B) 1,024
C) 1,048,576
D) 18

Ans: A
Feedback: 9.3.1
Difficulty: Easy

14. Given the logical address 0xAEF9 (in hexadecimal) with a page size of 256 bytes, what is the page number?
A) 0xAE
B) 0xF9
C) 0xA
D) 0x00F9

Ans: A
Feedback: 9.3.1
Difficulty: Medium

15. A large page size results in
A) lower internal fragmentation
B) larger page table overhead
C) efficient disk I/O
D) All of the above

Ans: C
Feedback: 9.3.1
Difficulty: Medium

16. A frame table stores
A) which frames are allocated.
B) which frames are free.
C) total number of frames.
D) All of the above.

Ans: D
Feedback: 9.3.1
Difficulty: Easy

17. A(n) _____ matches the process with each entry in the TLB.
A) address-space identifier
B) process id
C) stack
D) page number

Ans: A
Feedback: 9.3.2
Difficulty: Medium

18. A page-table base register stores
A) a pointer to the page table in memory.
B) the starting logical address of the page currently being accessed.
C) the starting physical address of the frame currently being addressed.
D) the page size of the page currently being accessed.

Ans: A
Feedback: 9.3.2
Difficulty: Easy

19. A translation look-aside buffer is used to
A) cache page table entries.
B) store the address of the page table in memory.
C) size of the logical address space of the currently running process.
D store page size.

Ans: A
Feedback: 9.3.2
Difficulty: Easy

20. The protection bit in a page table
A) provides protection against unauthorized updates in the page table.
B) marks a page table as read-only or read-write.
C) marks a frame as read-only or read-write.
D) All of the above.

Ans: A
Feedback: 9.3.3
Difficulty: Easy

21. Reentrant code is easier to share when paging is used, because
A) each process can modify that code its own way.
B) the code doesn't change during execution.
C) the code changes are identical for each process.
D) All of the above.
Ans: B
Feedback: 9.3.4
Difficulty: Easy

22. Assume a system uses 2-level paging and has a TLB hit ratio of 90%. It requires 15 nanoseconds to access the TLB, and 85 nanoseconds to access main memory. What is the effective memory access time in nanoseconds for this system?

A) 22
B) 108.5
C) 30.5
D) 117

Ans: D
Feedback: 9.4.1
Difficulty: Difficult

23. Which of the following technique is well suited to support very large address space, e.g. 64-bit address space?
A) Inverted page tables
B) Hierarchical page tables
C) Clustered page tables
D) All of the above

Ans: C
Feedback: 9.4.2
Difficulty: Medium

24. The _____ binding scheme facilitates swapping.
A) interrupt time
B) load time
C) assembly time
D) execution time

Ans: D
Feedback: 9.5
Difficulty: Medium

25. The roll out, roll in variant of swapping is used ____.
A) when a backing store is not necessary
B) for the round-robin scheduling algorithm
C) for priority-based scheduling algorithms
D) when the load on the system has temporarily been reduced

Ans: C
Feedback: 9.5
Difficulty: Medium

26. A page out operation
A) moves a page from memory to the backing store.
B) moves a page from the backing store to memory.
C) moves a page from one frame to another.
D) deletes a page from the backing store.

Ans: A
Feedback: 9.5.2
Difficulty: Easy

27. Replacement question: With segmentation in IA-32 architecture, a logical address consists of _____.
A) segment number and offset
B) segment number, GDT or LDT indicator, protection and offset
C) segment number, page number and offset
D) segment number, page number, GDT/LDT, protection and offset

Ans: B
Feedback: 9.6.1
Difficulty: Easy

28. Replacement Question: Address translation from a logical address to a physical address in IA-32 architecture is comprised of
A) a segmentation unit that translates the logical address to its physical address.
B) a paging unit that translates the logical address to its physical address.
C) a segmentation unit followed by a paging unit that translate the logical address to its physical address.
D) a paging unit followed by a segmentation unit that translates the logical address to its physical address.

Ans: C
Feedback: 9.6.1
Difficulty: Easy

29. The x86-64 architecture provides support for
A) 64-bit physical addresses
B) 48-bit physical addresses
C) 32-bit physical addresses
D) 52-bit physical addresses

Ans: D
Feedback: 9.6.2
Difficulty: Medium

30. The x86-64 architecture provides support for
A) three different page sizes using 3-level paging hierarchy.
B) four different page sizes using 4-level paging hierarchy.
C) four different page sizes using 3-level paging hierarchy.
D) three different page sizes using 4-level paging hierarchy.

Ans: D
Feedback: 9.6.2
Difficulty: Easy

31. A 64-bit architecture with more than 16 quintillion addressable memory
A) can support a majority of today's application requirements, but not all.
B) is large enough to support all current as well as future application requirements.
C) is large enough to support all current application requirements but may not be able to support all future application requirements.
D) All of the above.

Ans: C
Feedback: 9.7
Difficulty: Medium

Essay Questions

1. How is a limit register used for protecting main memory?

Ans: When the CPU is executing a process, it generates a logical memory address that is added to a relocation register in order to arrive at the physical memory address actually used by main memory. A limit register holds the maximum logical address that the CPU should be able to access. If any logical address is greater than or equal to the value in the limit register, then the logical address is a dangerous address and an error results.
Feedback: 9.1.1
Difficulty: Medium

2. What is the advantage of using dynamic loading?

Ans: With dynamic loading a program does not have to be stored, in its entirety, in main memory. This allows the system to obtain better memory-space utilization. This also allows unused routines to stay out of main memory so that memory can be used more effectively. For example, code used to handle an obscure error would not always use up main memory.
Feedback: 9.1.4
Difficulty: Medium

3. When does external fragmentation occur?

Ans: As processes are loaded and removed from memory, the free memory space is broken into little pieces. External fragmentation exists when there is enough total memory space to satisfy a request, but the available spaces are not contiguous; storage is fragmented into a large number of small holes. Both the first-fit and best-fit strategies for memory allocation suffer from external fragmentation.
Feedback: 9.2.2
Difficulty: Medium

4. Distinguish between internal and external fragmentation.

Ans: Fragmentation occurs when memory is allocated and returned to the system. As this occurs, free memory is broken up into small chunks, often too small to be useful. External fragmentation occurs when there is sufficient total free memory to satisfy a memory request, yet the memory is not contiguous, so it cannot be assigned. Some contiguous allocation schemes may assign a process more memory than it actually requested (i.e. they may assign memory in fixed-block sizes). Internal fragmentation occurs when a process is assigned more memory than it has requested and the wasted memory fragment is internal to a process.
Feedback: 9.2.2
Difficulty: Medium

5. Explain the basic method for implementing paging.

Ans: Physical memory is broken up into fixed-sized blocks called frames while logical memory is broken up into equal-sized blocks called pages. Whenever the CPU generates a logical address, the page number and offset into that page is used, in conjunction with a page table, to map the request to a location in physical memory.
Feedback: 9.3.1
Difficulty: Medium

6. Using Figure 9.12, describe how a logical address is translated to a physical address.

Ans: A logical address is generated by the CPU. This logical address consists of a page number and offset. The TLB is first checked to see if the page number is present. If so, a TLB hit, the corresponding page frame is extracted from the TLB, thus producing the physical address. In the case of a TLB miss, the page table must be searched according to page number for the corresponding page frame.
Feedback: 9.3.2
Difficulty: Medium

7. Describe how a transaction look-aside buffer (TLB) assists in the translation of a logical address to a physical address.

Ans: Typically, large page tables are stored in main memory, and a page-table base register points are saved to the page table. Therefore, two memory accesses are needed to access a byte (one for the page-table entry, one for the byte), causing memory access to be slowed by a factor of 2. The standard solution to this problem is to use a TLB, a special, small fast-lookup hardware cache. The TLB is associative, high speed memory. Each entry consists of a key and value. An item is compared with all keys simultaneously, and if the item is found, the corresponding value is returned.
Feedback: 9.3.2
Difficulty: Medium

8. How are illegal page addresses recognized and trapped by the operating system?

Ans: Illegal addresses are trapped by the use of a valid-invalid bit, which is generally attached to each entry in the page table. When this bit is set to "valid," the associated page is in the process's logical address space and is thus a legal (or valid) page. When the bit is set to "invalid," the page is not in the process's logical address space. The operating system sets this bit for each page to allow or disallow access to the page.
Feedback: 9.3.3
Difficulty: Medium

9. Describe the elements of a hashed page table.

Ans: A hashed page table contains hash values which correspond to a virtual page number. Each entry in the hash table contains a linked list of elements that hash to the same location (to handle collisions). Each element consists of three fields: (1) the virtual page number, (2) the value of the mapped page frame, and (3) a pointer to the next element in the linked list.
Feedback: 9.4.2
Difficulty: Difficult

10. What is the context switch time, associated with swapping, if a disk drive with a transfer rate of 2 MB/s is used to swap out part of a process that is 200 KB in size? Assume that no seeks are necessary and that the average latency is 15 ms. The time should reflect only the amount of time necessary to swap out the process.

Ans: 200KB / 2048 KB per second + 15 ms = 113 ms
Feedback: 9.5
Difficulty: Medium

11. Explain why mobile operating systems generally do not support paging.

Ans: Mobile operating systems typically do not support swapping because file systems are typically employed using flash memory instead of magnetic hard disks. Flash memory is typically limited in size as well as having poor throughput between flash and main memory. Additionally, flash memory can only tolerate a limited number of writes before it becomes less reliable.
Feedback: 9.5.3
Difficulty: Medium

12. Replacement questions: Briefly describe the memory management scheme of IA-32. How does it differ from the paging memory management scheme in terms of the user's view of memory?

Ans: Memory management in IA-32 systems is divided into two components— segmentation and paging. The CPU generates logical addresses, which are given to the segmentation unit. The segmentation unit produces a linear address for each logical address. The linear address is then given to the paging unit, which in turn generates the physical address in main memory.
In contrast, in a paging scheme, the user specifies a single logical address, which is partitioned by the hardware into a page number and an offset, all invisible to the programmer.
Feedback: 9.6.1
Difficulty: Medium

13. Describe the partitions in a logical-address space of a process in the IA-32 architecture.

Ans: The logical-address space is divided into two partitions. The first partition consists of up to 8 K segments that are private to that process. The second partition consists of up to 8 K segments that are shared among all the processes. Information about the first partition is kept in the local descriptor table (LDT); information about the second partition is kept in the global descriptor table (GDT).
Feedback: 9.6.1
Difficulty: Difficult

14. Using Figure 9.26, describe how address translation is performed on ARM architectures.

Ans: ARM supports four different page sizes: 4-KB and 16-KB page use two-level paging, the larger 1-MB and 16-MB page sizes use single-level paging. The ARM architecture uses two levels of TLBs - at one level is the micro TLB which is in fact separate TLBs for data and instructions. At the inner level is a single main TLB. Address translation begins with first searching the micro TLB, and in case of a TLB miss, the main TLB is then checked. If the reference is not in the main TLB, the page table must then be consulted.
Feedback: 9.7
Difficulty: Medium

True/False Questions

1. A relocation register is used to check for invalid memory addresses generated by a CPU.

Ans: False
Feedback: 9.1.3
Difficulty: Medium

2. Fragmentation does not occur in a paging system.

Ans: False
Feedback: 9.3
Difficult: Medium

3. A 32-bit logical address with 8 KB page size will have 1,000,000 entries in a conventional page table.

Ans: False
Feedback: 9.3.1
Difficulty: Medium

4. Without a mechanism such as an address-space identifier, the TLB must be flushed during a context switch.

Ans: True
Feedback: 9.3.2
Difficulty: Medium

5. There is a 1:1 correspondence between the number of entries in the TLB and the number of entries in the page table.

Ans: False
Feedback: 9.3.2
Difficulty: Easy

6. Reentrant code cannot be shared.

Ans: False
Feedback: 9.3.4
Difficulty: Easy

7. Hierarchical page tables are appropriate for 64-bit architectures.

Ans: False
Feedback: 9.4.1
Difficulty: Medium

8. Hashed page tables are particularly useful for processes with sparse address spaces.

Ans: True
Feedback: 9.4.2
Difficulty: Easy

9. Hashed page tables are commonly used when handling addresses larger than 32 bits.

Ans: True
Feedback: 9.4.2
Difficulty: Easy

10. Inverted page tables require each process to have its own page table.

Ans: False
Feedback: 9.4.3
Difficulty: Medium

11. Mobile operating systems typically support swapping.

Ans: False
Feedback: 9.5.3
Difficulty: Easy

12. In swapping with paging technique, individual pages of a process are swapped in or out.

Ans: True
Feedback: 9.5.2
Difficulty: Easy

13. The ARM architecture uses both single-level and two-level paging.

Ans: True
Feedback: 9.7
Difficulty: Medium