Surrogate gradients for analog neuromorphic computing

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To rapidly process temporal information at a low metabolic cost, biological neurons integrate inputs as an analog sum but communicate with spikes, binary events in time. Analog neuromorphic hardware uses the same principles to emulate spiking neural networks with exceptional energy-efficiency. However, instantiating high-performing spiking networks on such hardware remains a significant challenge due to device mismatch and the lack of efficient training algorithms. Here, we introduce a general in-the-loop learning framework based on surrogate gradients that resolves these issues. Using the BrainScaleS-2 neuromorphic system, we show that learning self-corrects for device mismatch resulting in competitive spiking network performance on both vision and speech benchmarks. Our networks display sparse spiking activity with, on average, far less than one spike per hidden neuron and input, perform inference at rates of up to 85 k frames/second, and consume less than 200 mW. In summary, our work sets several new benchmarks for low-energy spiking network processing on analog neuromorphic hardware and paves the way for future on-chip learning algorithms.

Introduction

In recent years, deep artifical neural networks (ANNs) have surpassed human-level performance on many difficult tasks (7, 34, 46). The human brain, however, remains unchallenged in terms of its energy-efficiency and fault tolerance. A fundamental property underlying these capabilities is spatiotemporal sparseness (47), which is directly linked to the way how biological spiking neural networks (SNNs) process and exchange information. Spiking neurons receive and integrate inputs on their analog membrane potentials and, upon reaching the firing threshold, emit action potentials, or spikes. These binary events propagate asynchronously through the SNN and are ultimately received by other neurons.

Neuromorphic engineering attempts to mirror the power efficiency and robustness of the brain by replicating its key architectural properties (45, 49). Here, one distinguishes between fully digital, analog, and mixed-signal systems. Digital sys-

tems *simulate* the analog dynamics of spiking neurons, e.g., their membrane potentials (4, 5, 16, 21, 33, 41). In contrast, analog and mixed-signal solutions *emulate* neuronal or synaptic dynamics and states by representing them as physical voltages, currents, or conductance changes evolving in continuous time (10, 26, 31, 43). Thus, by explicitly taking advantage of physical properties and dynamics of the underlying hardware substrate, neuromorphic computing holds the key to building power-efficient and scalable SNNs in-silico (1, 32, 41).

However, to serve meaningful computational purpose, these analog devices require training. The most successful training schemes for ANNs are gradient-based. Yet, extending similar training techniques to SNNs and neuromorphic hardware poses several challenges. First, one has to overcome the binary nature of spikes, which impedes vanilla gradient-descent (3, 11, 37). Second, training has to ensure sparse spiking activity to exploit the superior power efficiency of SNN processing (14). Finally, training has to achieve all of the above while coping with analog hardware imperfections inevitably tied to their manufacturing process.

In this article, we tackle the above challenges by extending previous work on surrogate gradients. Specifically, we developed a general in-the-loop (ITL) training framework and applied it to the mixed-signal BrainScaleS-2 single-chip system. We demonstrate that SNNs trained using our approach solve several challenging benchmark problems by taking advantage of sparse, precisely timed spikes instead of firing rates. The resulting SNNs reach competitive accuracy levels comparable to corresponding software simulations and perform inference with ultra-low latency by taking full advantage of BrainScaleS' hardware acceleration. Crucially, we show that ITL surrogate gradients achieve this through self-calibration, whereby training automatically corrects for device mismatch without the need for costly offline calibration.

The BrainScaleS-2 analog neuromorphic substrate

In this article we relied on the analog BrainScaleS-2 single chip system. It features 512 analog neuron circuits whose dynamics
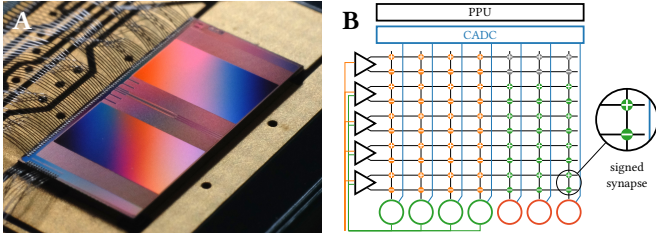
Figure 1: The mixed-signal BrainScaleS-2 chip. (A) Close-up chip photograph. **(B)** Implementation of a multi-layer network on the analog neuromorphic core. Input spike trains are injected via synapse drivers (triangles) and relayed to the hidden layer neurons (green circles) via the synapse array. Spikes in the hidden layer are routed on-chip to the output units (red circles). Each connection is represented by a pair of excitatory and inhibitory hardware synapses, which holds a signed weight value. The analog membrane potentials are read out via the column-parallel analog-to-digital converter (CADC) and further processed by the plasticity processing unit (PPU).

obey the leaky integrate-and-fire (LIF) equation

$$C\frac{dV}{dt} = -g_{\text{leak}}\left(V - V_{\text{leak}}\right) + I\,, \tag{1}$$

which can optionally be augmented by adaptation currents and an exponential spiking nonlinearity. The membrane potential V is explicitly represented on the chip as an analog voltage measured across a capacitor and evolves continuously in time. The leak conductance g_{leak} pulls the membrane towards the leak potential V_{leak}, resulting in an exponential decay with time constant $\tau_{\text{m}} \equiv C/g_{\text{leak}}$. Due to the substrate's small intrinsic capacitances and comparatively large currents, the dynamics of the spiking neurons implemented on BrainScaleS-2 evolve 10^3 times faster than biological neurons.

Whenever the potential crosses the firing threshold ϑ, an outgoing spike is generated and the membrane is reset. An on-chip event router propagates both internally generated and external spikes to connected neurons, allowing to form feed-forward as well as recurrent topologies. To that end, each neuron integrates stimuli from a column of 256 synapses, where the weights are represented with a resolution of 6 bit. The resulting postsynaptic currents I, which are integrated on the membrane capacitor, follow an exponential time course similar to the membrane dynamics themselves. The sign of a synapse is determined as a presynaptic property. However, we allowed for a continuous transition between positive and negative weights during training by merging synapse circuits of opposing signs (Fig. 1B).

BrainScaleS-2 allows individually adjusting all neuronal parameters, including reference potentials and time constants, on a per-neuron basis to flexibly emulate different target dynamics. This fine-grained control also facilitates calibration to mitigate deviations induced by variations in the production process. In this article, we however make use of this parameterization to actively *decalibrate* the system, thereby allowing us to systematically explore self-calibration properties of our learning algorithm.
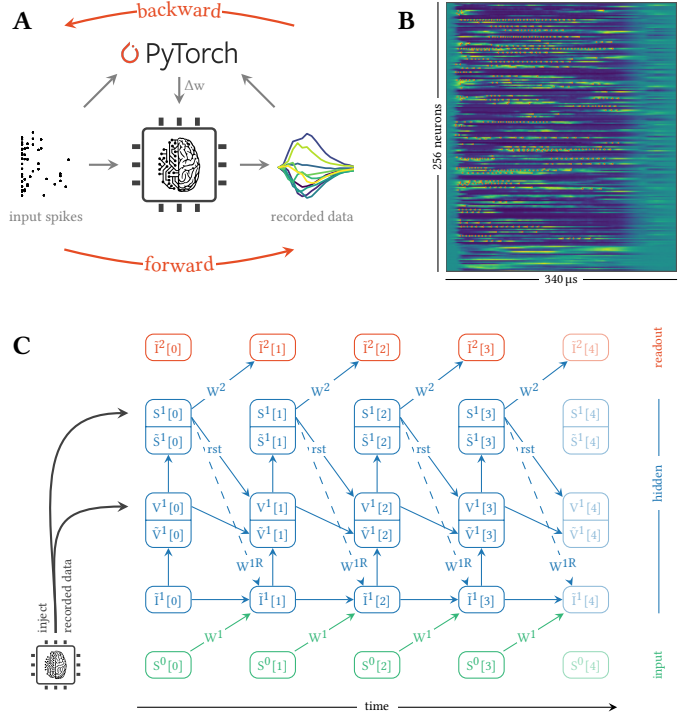
Figure 2: Surrogate gradient learning on BrainScaleS-2. (A) Illustration of our ITL training scheme. The forward pass is emulated on the BrainScaleS-2 chip. Observables from the neuromorphic substrate as well as the input spike trains are processed on a conventional computer to perform the backward pass. The calculated weight updates are then written to the neuromorphic system. **(B)** Parallel recording of analog traces and spikes from 256 neurons via the CADC. **(C)** The differentiable computation graph results from the integration of LIF dynamics. The time dimension is unrolled from left to right and information flows from bottom to top within an integration step. Synaptic currents are derived from the previous layer's spikes and potential recurrent connections, multiplied by the respective weights ($W^{(R)}$). Stimuli are integrated on the neurons' membranes (V) which trigger spikes (S) upon crossing their thresholds. These observables are continuously synchronized with data recorded from the hardware. Spikes as well as reset signals (rst) are propagated to the next time step, which also factors in the decay of currents and potentials.

In-the-loop surrogate gradients on analog hardware

To train SNNs on BrainScaleS-2, we developed a general learning framework to optimize recurrent and multi-layer networks. Our approach is based on the notion of surrogate gradients, which overcome vanishing gradients and critical points associated with non-differentiable spiking dynamics [37]. Surrogate gradient learning flexibly supports arbitrary differentiable loss functions and can seamlessly exploit both rate- and spike timing-based coding schemes.

Broadly, our ITL approach works as follows (Fig. 2): First, we emulate the forward pass on the analog neuromorphic substrate and record both spikes and internal membrane traces (Fig. 2A,B). By injecting the latter into an otherwise approximate software model we effectively render the neuromorphic SNN differentiable. This permits the evaluation of surrogate gradients and the calculation of weight updates using backpropagation through time (BPTT) on GPU-enabled auto-

differentiation libraries (38) in combination with state-of-the-art optimizers. At the same time, our learning algorithm self-corrects for parameter mismatch of the analog components (Fig. 2C). Finally, we close the loop by transferring the updated weights back to the analog system.

In the following we elaborate on the two central steps, namely the recording of data from the neuromorphic system and their integration into the computation graph.

Recording spikes and analog membrane traces. Surrogate gradient learning crucially relies on the neurons' membrane potentials. On an analog system like BrainScaleS-2, these are represented as physical voltages and are hence not readily available for numerical computation. The required digitization is often challenging due to the inherent parallelism of these substrates. This bottleneck is further emphasized by accelerated systems.

BrainScaleS-2 solves this problem by incorporating column-parallel analog-to-digital converters (CADCs) to simultaneously digitize the membrane potentials of all neurons (Fig. 1B). We trigger the ADC conversions via the embedded plasticity processing units (PPUs) (20) to ensure higher and more stable sampling rates compared to a host-based scheduling. This furthermore enables the implementation of a fast inference mode, where only classification results are transmitted to the host. When training the network, however, each recorded sample is instantly transferred to an intermediate external memory region, from where it is asynchronously read by the host machine at the end of an input pattern or batch. In total we reach a sample rate of approximately $0.6\,\mathrm{MSample\,s^{-1}}$, corresponding to a sampling interval of $1.7\,\mu\mathrm{s}$. For 256 neurons, this yields a total data rate of $1.2\,\mathrm{Gbit\,s^{-1}}$. In addition to the sampled membrane traces, we continuously record and time stamp the spike events emitted by the substrate.

A computation graph for analog circuits. To compute weight updates based on surrogate gradients, we incorporate these aggregated data into a computation graph that approximates the underlying neuronal dynamics on the neuromorphic substrate. To that end, we iteratively simulate the neuronal dynamics to obtain the graph in which we inject the *actual* recorded membrane traces. Thus we use measured quantities, where available, and only rely on the model *estimates* for internal variables that are not measured, e.g., the synaptic currents.

We formulate the graph on a regular time grid of time step Δt derived from the sampling period of the membrane traces. Although the spike trains from the neuromorphic substrate are known with much higher temporal resolution, they are also aligned to these bins. Depending on the coding scheme and network topology, an increased resolution can be beneficial and allow to better capture causal relations between spikes. In this case, the computation graph can be evaluated on a finer time scale and for that purpose operate on interpolated membrane traces.

To reconstruct the internal states we start by assuming ideal LIF dynamics (Eq. 1), which we integrate using the forward Euler method. The membrane evolution is estimated recursively by taking into account its temporal decay and the calculated synaptic currents $\tilde{I}[t]$, which in turn are based on the presynaptic spikes $\tilde{S}_j[t]$ of neuron j:

$$\tilde{V}[t+1] = \tilde{V}[t] \cdot \mathrm{e}^{-\Delta t/\tau_\mathrm{m}} + \tilde{I}[t], \tag{2}$$

$$\tilde{I}[t+1] = \tilde{I}[t] \cdot \mathrm{e}^{-\Delta t/\tau_\mathrm{s}} + \sum_j W_j \tilde{S}_j[t]. \tag{3}$$

Eq. 3 can be augmented by an additional term to encompass recurrent connections. The modelled state variables, indicated by the tilde (˜), represent the estimates of the on-chip dynamics. Since these can deviate from the actual emulation and hence distort the resulting gradients, we in their place insert the normalized recorded data. For this purpose, we introduce an auxiliary identity function $f(x, \tilde{x}) \equiv x$ and define surrogate derivatives $\partial f/\partial x = 0$ and $\partial f/\partial \tilde{x} = 1$. Eq. 2 can now be modified to

$$\tilde{V}[t+1] = f\left(V[t+1], \tilde{V}[t] \cdot \mathrm{e}^{-\Delta t/\tau_\mathrm{m}} + \tilde{I}[t]\right). \tag{4}$$

A similar approach is taken for spikes by defining $\tilde{S}_j[t](S_j[t], \tilde{V}_j[t]) \equiv S_j[t]$ with associated derivatives

$$\frac{\partial \tilde{S}_j[t]}{\partial S_j[t]} = 0, \qquad \frac{\partial \tilde{S}_j[t]}{\partial \tilde{V}_j[t]} = \left(\beta \cdot |\tilde{V}_j[t] - \vartheta|\right)^{-2}, \tag{5}$$

where β describes the steepness of the surrogate gradient (52).

When performing the backward pass and to this end calculating $\partial\mathcal{L}/\partial\theta = \dots \partial\tilde{S}/\partial\tilde{V} \cdot \partial\tilde{V}/\partial\theta$, the sampled values for the membrane potential are used whenever an expression containing $\tilde{V}$ is evaluated, e.g. in $\partial\tilde{S}/\partial\tilde{V}$. The estimates, in contrast, are used to determine further derivatives $\partial\tilde{V}/\partial\theta$ which occur in the recursion relation of BPTT.

Flexible choice of a loss function. The suggested framework allows to operate on any differentiable loss that can be formulated on the data acquired from the neuromorpic system. This encompasses loss functions based on the spiking activity of the neurons as well as on their membrane voltages (cf. Materials and methods).

The task-specific loss can be augmented by regularization functions. These might, on one hand, target an improved generalization performance or, on the other hand, an adaptation to hardware-specific constraints such as finite weights and dynamic ranges of analog signals. Such terms can furthermore be directly tailored to shape the activity of the emulated SNNs and result in sparse firing patterns.

Results

We trained BrainScaleS-2 on a series of spike-based vision and speech recognition tasks using our ITL learning framework. Specifically, we chose classification tasks requiring evidence integration on widely different time scales which allowed us to probe the efficiency of our approach on both feed-forward or recurrent network topologies.

First, we trained a feed-forward network consisting of a single hidden layer with 246 neurons on the MNIST dataset (29). To accommodate the data to a fan-in of 256 inputs, we reduced the original 28 × 28 images to 16×16 pixels. We then converted the pixels into a spike-latency code (cf. Materials and methods). The network was optimized using
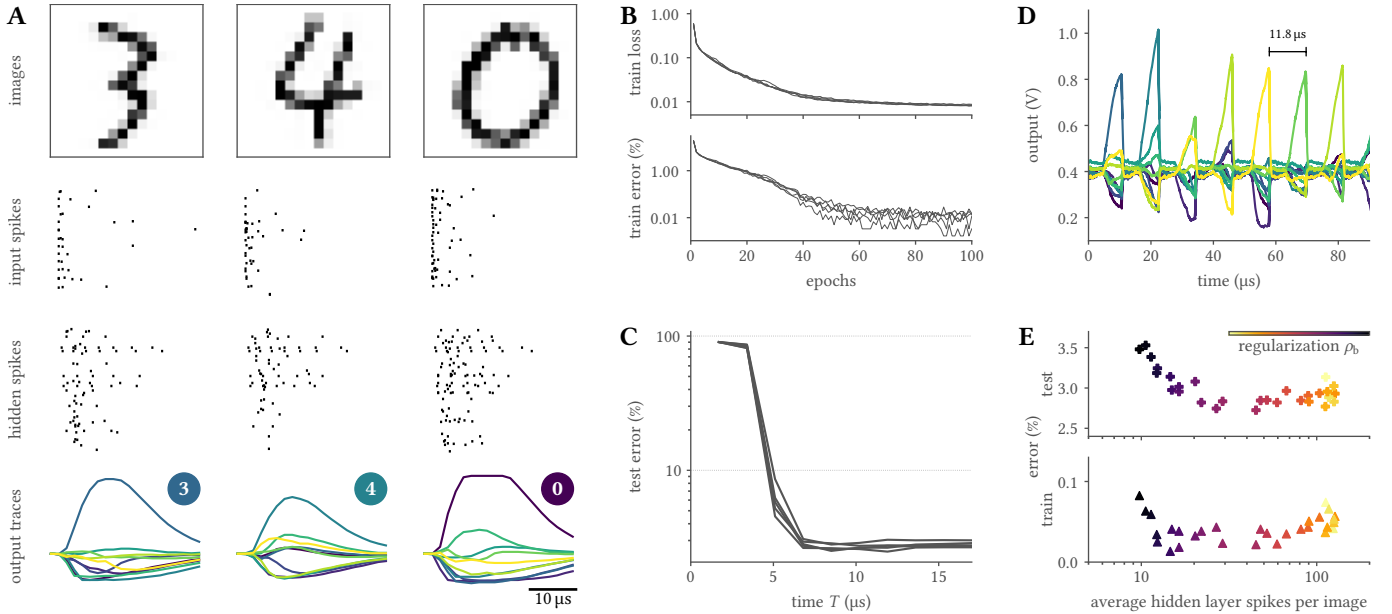
Figure 3: Classification of the MNIST dataset. (A) Three snapshots of the SNN activity, consisting of the downscaled 16×16 input images (top), spike raster of both the input spike trains and hidden layer activity (middle), and readout neuron traces (bottom). The latter show a clear separation, and hence a correct classification of the presented images. **(B)** Loss and accuracy over the course of 100 training epochs for five initial conditions. **(C)** The time to decision is consistently below 10 μs. Here, the classification latency was determined by iteratively re-evaluating the max-over-time for output traces (see panel A) restricted to a limited interval $[0, T]$. **(D)** This low latency allowed to inject an image every 11.8 μs, corresponding to more than 85 k classifications per second. This was achieved by artificially resetting the state of the neuromorphic network in between samples. **(E)** The neuromorphic system can be trained to perform classification with sparse activity. When sweeping the regularization strength, a state of high performance was evidenced over more than an order of magnitude of hidden layer spike counts.

the Adam optimizer (28) to minimize a max-over-time loss $\mathcal{L} = \text{NLL}(\text{softmax}(\max_t V_i^O[t]), y^\star)$, with the negative log-likelihood NLL, the membrane traces of the output layer $V_i^O[t]$, and the true labels $y^\star$. To prevent excessive amplitudes and in turn clipping of V_i^O on the analog substrate, we included a penalty $\rho_a \cdot \text{mean}_i((\max_t V_i^O[t])^2)$. We furthermore added an activity shaping term to promote sparse activity patterns (cf. Eq. 6). Notably, this contribution could only reduce the network's activity and did not act as an upwards pulling homeostatic force. Being based on surrogate gradients, our approach nevertheless allowed training the network starting from a quiescent hidden layer.

During training, the neuromorphic substrate learned to correctly infer and represent the correct class memberships as the maximally responsive output units (Fig. 3A,B). Interestingly, the inhibition of the other units was not explicitly demanded by the loss function but emerged naturally through optimization. After 100 epochs, the model almost perfectly fit the training samples and achieved an overall accuracy of (97.2 ± 0.1) % on held out test data (Table 1). We were able to reduce overfitting by augmenting the data through random rotations of up to 15°. Dropout similarly improved test performance and combining it with data augmentation resulted in an accuracy of (97.6 ± 0.1) % on BrainScaleS-2.

As a comparison, we trained the same SNN purely in software and in that process ignored all hardware-specific constraints, including the finite weight resolution. With an accuracy of (97.5 ± 0.1) % on the test data, the software implementation only slightly surpassed BrainScaleS-2. As a baseline for the downscaled 16×16 MNIST dataset, we furthermore trained

Table 1: Comparison of results achieved with networks trained on BrainScaleS-2 and in software as well as an ANN baseline.

| | implementation | remarks | accuracy (%) | |
			train	test
16×16 MNIST	BSS-2		100.0 ± 0.0	97.2 ± 0.1
	BSS-2	dropout + rotation	97.3 ± 0.1	97.6 ± 0.1
	software		100.0 ± 0.0	97.5 ± 0.1
	software	dropout + rotation	97.7 ± 0.1	98.0 ± 0.0
	reference ANN		100.0 ± 0.0	98.1 ± 0.1
	reference ANN	dropout + rotation	99.0 ± 0.0	98.7 ± 0.1
SHD	BSS-2		96.6 ± 0.5	76.2 ± 1.3
	BSS-2	augmentation	90.7 ± 0.5	80.6 ± 1.0
	software		100.0 ± 0.0	71.2 ± 0.3
	software	augmentation	90.9 ± 0.2	79.9 ± 0.7

an equivalently sized ANN with rectified linear units (ReLUs) which resulted in an accuracy of (98.1 ± 0.1) %. Dropout as well as augmentation again improved upon these numbers resulting in a best-effort performance of (98.7 ± 0.1) %. Importantly, these accuracy figures – within their uncertainties – resembled results on the full-size MNIST images, suggesting comparability between these two datasets.

Low-latency neuromorphic computation. The output traces of trained networks suggested that for latency-encoded inputs as used above the decision is available long before the end of a stimulus (cf. Fig. 3A). To determine the network's classification latency, we artificially restricted the readout layer's membrane traces (cf. Fig. 3A) to varying time intervals $[0, T]$

over which we based the network's decision as given by the maximally active unit. We found that the readout reached its peak accuracy within 8 μs after the first input spike (Fig. 3C).

Low classification latency, however, does not automatically translate into high inference rates but is also affected by the neuronal and synaptic time constants. These time constants determine the rate by which state variable decay back to baseline within the neuron circuits and, hence, impose a minimum separation of independent stimuli. Still, to translate low classification latency into high inference rates, we added an artificial reset of the neuromorphic units 10 μs after inserting the first input spike. Specifically, we exploited a feature of BrainScaleS-2 that allowed us to concurrently reset the analog membrane circuits and clamped all synaptic currents to their respective baselines (Fig. 3D). This allowed us to infer images with a separation of 11.8 μs, allowing our SNNs to accurately classify more than 85 k images per second with a latency of 8 μs.

Moreover, we measured the system's power consumption. When emulating the trained SNN, the full BrainScaleS-2 chip consumed approximately 200 mW. This figure included the current draw from the analog neuromorphic core, the plasticity processors, all surrounding periphery, and the high-speed communication links. Combining this measurement with the above throughput results in an energy consumption of 2.4 μJ per classified image.

Efficiency through sparse spiking activity. A key advantage of SNNs is their sparse temporal spiking activity, which is presumed crucial for the power efficiency of the brain (47). For similar reasons it is also important for larger neuromorphic systems and, particularly, in scenarios in which several chips cooperate by exchanging spikes over communication channels with limited bandwidth.

To ensure sparse activity on the BrainScaleS-2 system, we augmented the training loss by a regularization term

$$\mathcal{L}_{\text{reg}} = \rho_b \frac{1}{N_H} \sum_{i=1}^{N_H} \left(\sum_t S_i^H[t] \right)^2, \qquad (6)$$

with the strength parameter ρ_b, the hidden layer size N_H, and the corresponding hidden layer spike trains S_i^H (53). We trained the above feed-forward SNNs for a range of different values ρ_b and measured both their accuracy and average hidden layer spike counts. All resulting network configurations were able to fit the training data with high accuracy (Fig. 3E). More importantly, they reached a constant test accuracy of 97.2 % for activity levels down to approximately 20 hidden layer spikes per image. When only using 10 spikes on average, we observed a slight decrease in performance. At such low spike counts, the networks operated in a regime far from the rate coding limit and hence had to rely on individual spikes and their timing.

Self-calibration through ITL learning. The above results were obtained with a calibrated BrainScaleS-2 system in which the parameter deviations due to device-mismatch were largely compensated and the computation graph hence closely matched the emulated dynamics. Nevertheless, a certain degree of residual mismatch remained. To quantify whether and how well our ITL scheme self-calibrates the substrate during learning, we performed a series of additional experiments in
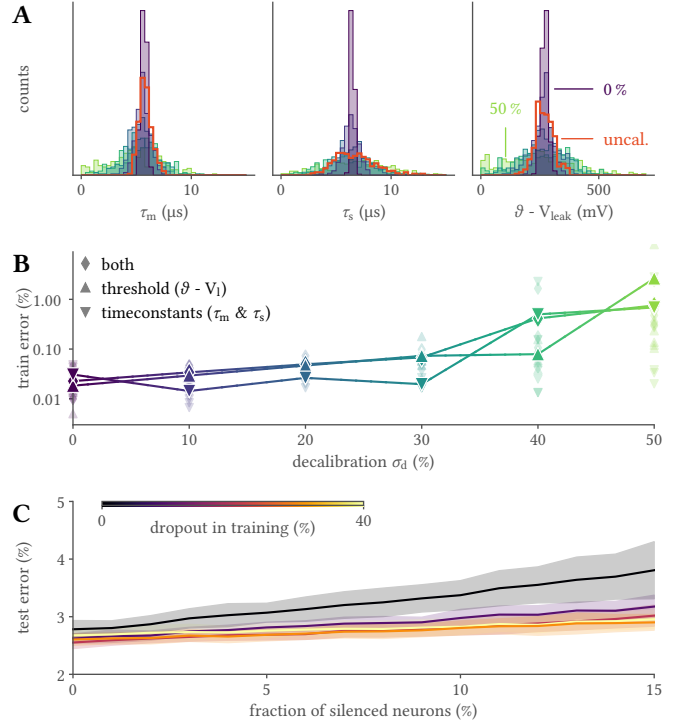
Figure 4: Self-calibration and robust performance on inhomogeneous substrates. (A) Distribution of measured neuronal parameters for various degrees of decalibration in the range of 0 % to 50 %. For this purpose, the analog circuits were deliberately detuned towards individual target values drawn from normal distributions of variable widths. Distributions for uncalibrated parameters are shown in red. **(B)** Despite assuming homogeneously behaving circuits in the computation graph, ITL training widely compensated the fixed-pattern deviations shown in panel A. For configurations with extreme mismatch, some networks suffered from dysfunctional states (e.g. leak-over-threshold). **(C)** When incorporating dropout regularization during training, networks become widely resilient to failure of hidden neurons.

which we deliberately decalibrated the system. Specifically, we calibrated each neuron's time constants and threshold to individual target values. These were drawn from normal distributions with a mean corresponding to the original calibration targets. We generated parameter sets by varying their normalized standard deviations σ_d in the range of 0 % to 50 % (Fig. 4A). This notably exceeded the mismatch present on an uncalibrated BrainScaleS-2 system. To dissect the influence of poorly matching time constants and misaligned thresholds, we first detuned $\tau_{m,s}$ and $\vartheta - V_{\text{leak}}$ separately and finally all of these parameters at the same time. Each of these experiments was repeated for five random seeds.

For each set of parameters, we trained the SNN on the neuromorphic system, still assuming ideal dynamics when constructing the computation graph as done previously. In other words we explicitly ignored the introduced mismatch. Nevertheless, learning performance was hardly affected by decalibration up to $\sigma_d = 30$ %. Beyond that point, error levels remained low but gradually increased. At these levels of decalibration some configurations suffered from pathological network states, caused by some neurons having supra-threshold resting potentials. Thus, even for mismatch levels far above the ones ex-

pected for BrainScaleS-2 and similar systems, ITL learning effectively self-calibrated the analog neuromorphic SNNs.

Training for robustness. We furthermore investigated the resilience of trained SNNs to defects occurring after deployment, e.g., failing neuron circuits. To this end, we simulated neuronal death by artificially silencing randomly selected units in the hidden layer of the network after training. As expected, performance deteriorated with an increasing fraction of disabled neurons (Fig. 4C).

However, when robustness was encouraged during training using dropout, the resilience to such neuronal failures was largely improved. For networks trained with a dropout rate of 40 % the test error increased by only 10 % when silencing 15 % of the hidden layer units. In contrast, it grew by 37 % when dropout was not used during training.

Speech recognition with recurrent SNNs. So far, our analysis was limited to tasks with short time horizons which can be readily solved using feed-forward networks. But other tasks such as speech recognition or keyword spotting may require working memory and thus recurrent architectures. On BrainScaleS-2, recurrent connectivity is readily supported by a flexible event router. Further, recurrence is easily integrated into our ITL learning scheme by adding recurrent connections to Eq. 3.

With these modifications, we trained a network with 186 recurrently connected hidden neurons to classify the SHD dataset (12), which consists of spoken digits from »zero« to »nine« in both English and German, resulting in 20 classes total. This dataset is a natural benchmark for SNNs due to its inherent temporal dimension. Furthermore, it directly provides input spike trains and hence alleviates the need for additional preprocessing, which can confound comparison. To feed the data into our system, we reduced their dimensionality by subsampling 70 out of the original 700 channels (cf. Materials and methods). The network was then trained by optimizing a sum-over-time loss $\mathcal{L} = \mathrm{NLL}(\mathrm{softmax}(\mathrm{sum}_t\ V_i^{\mathrm{O}}[t]), y^\star)$ (Fig. 5A). To prevent pathologically high firing rates, we employed homeostatic regularization during training. Specifically, we added a regularizer of the form $\rho_{\mathrm{r}} \cdot \max(0, \sum_{i,t} S_i[t] - \vartheta_{\mathrm{r}})^2$, where i and t iterate over the hidden layer units and time steps, respectively, ρ_{r} defines the regularization strength, and ϑ_{r} an activity threshold.

After 100 training epochs, the SNN reached $(96.6 \pm 0.5)\,\%$ on the training data and $(76.2 \pm 1.3)\,\%$ on the test set (Fig. 5B, Table 1). The large gap is presumably due to the nature of the dataset, which was designed to especially challenge a network's ability to generalize (12). The two languages included in the dataset exhibit classes with significant phonemic similarity (»nine« vs. »neun«), which are indeed harder to separate by the trained network (Fig. 5C). Most importantly, however, the test set consists to 81 % of two speakers that are not part of the training set and result in higher classification error rates (Fig. 5D). To improve generalization performance, we employed data augmentation. For this purpose, we stochastically shifted events to neighboring input channels drawn from a normal distribution centered around their original channel (cf. Materials and methods). This indeed improved the test performance to $(80.6 \pm 1.0)\,\%$.

As for the feed-forward network, we additionally trained and evaluated the SNN in an equivalent software-only implementation. Without augmentation it reached an accuracy of $(71.2 \pm 0.3)\,\%$ — far below the corresponding hardware results. At the same time, the software simulation was able to perfectly fit the training data, which was not achieved on BrainScaleS-2. We hypothesize that this discrepancy resulted from the intrinsic stochasticity of the analog substrate, which was propagated and amplified by the network's recurrent dynamics and acted as a form of regularization. To test this idea, we applied data augmentation to the simulation. Indeed, this change resulted in a improved test accuracy of $(79.9 \pm 0.7)\,\%$, close to the performance of BrainScaleS-2 under equivalent conditions. Similarly, augmentation closed the gap between software and hardware training accuracy, providing further support for our hypothesis. Thus, our work suggests that intrinsic analog device noise could act as an efficient regularizer. Importantly, our findings illustrate that the flexibility of ITL learning also applies to the realm of recurrent SNN trained on challenging speech processing problems.

Discussion

We have developed a general ITL learning method for recurrent and multi-layer SNNs on analog neuromorphic substrates and demonstrated its capabilities on BrainScaleS-2. The combination of surrogate gradients with ITL training – facilitated by the massively parallel digitization of analog membrane potentials – allowed us to tie on recent achievements in the field of SNN optimization and bring them to an analog substrate. This allowed us to achieve state-of-the-art classification accuracies on multiple benchmark problems, comparable to equivalent software simulations. During training, our framework automatically corrected for device mismatch and thus abolished the need for explicit calibration. The resulting SNNs exhibited spatially and temporally sparse activity patterns and could, furthermore, be optimized for resilience to neuron failure. Ultimately, our method allowed us to exploit BrainScaleS-2 for low-latency neuromorphic inference at high throughput and a low energy footprint.

Most current neuromorphic systems are fully digital and typically allow to simulate software trained models without performance loss (17, 19). This approach is flexible with regard to the SNN training schemes used (2, 6, 8, 24, 25, 30, 35, 37, 40, 42, 51). Still, research on analog and mixed-signal substrates is essential to turn recent advances in material science into efficient neuromorphic processors (13, 27, 32, 41). Key emerging technologies like memristors are ideal candidates for long-term memory storage in neuromorphic systems. However, these respective components are intrinsically analog and subject to drift and manufacturing variability. These imperfections lead to reduced performance when loading software trained models onto the analog substrate. While several studies approached this problem by optimizing for additional robustness during training (8, 50), these techniques are intrinsically limited. Since mature on-chip training solutions are not yet available, ITL learning has emerged as a good compromise that efficiently takes device-specific non-idealities and heterogeneity into account (22, 44). However, previous work relied
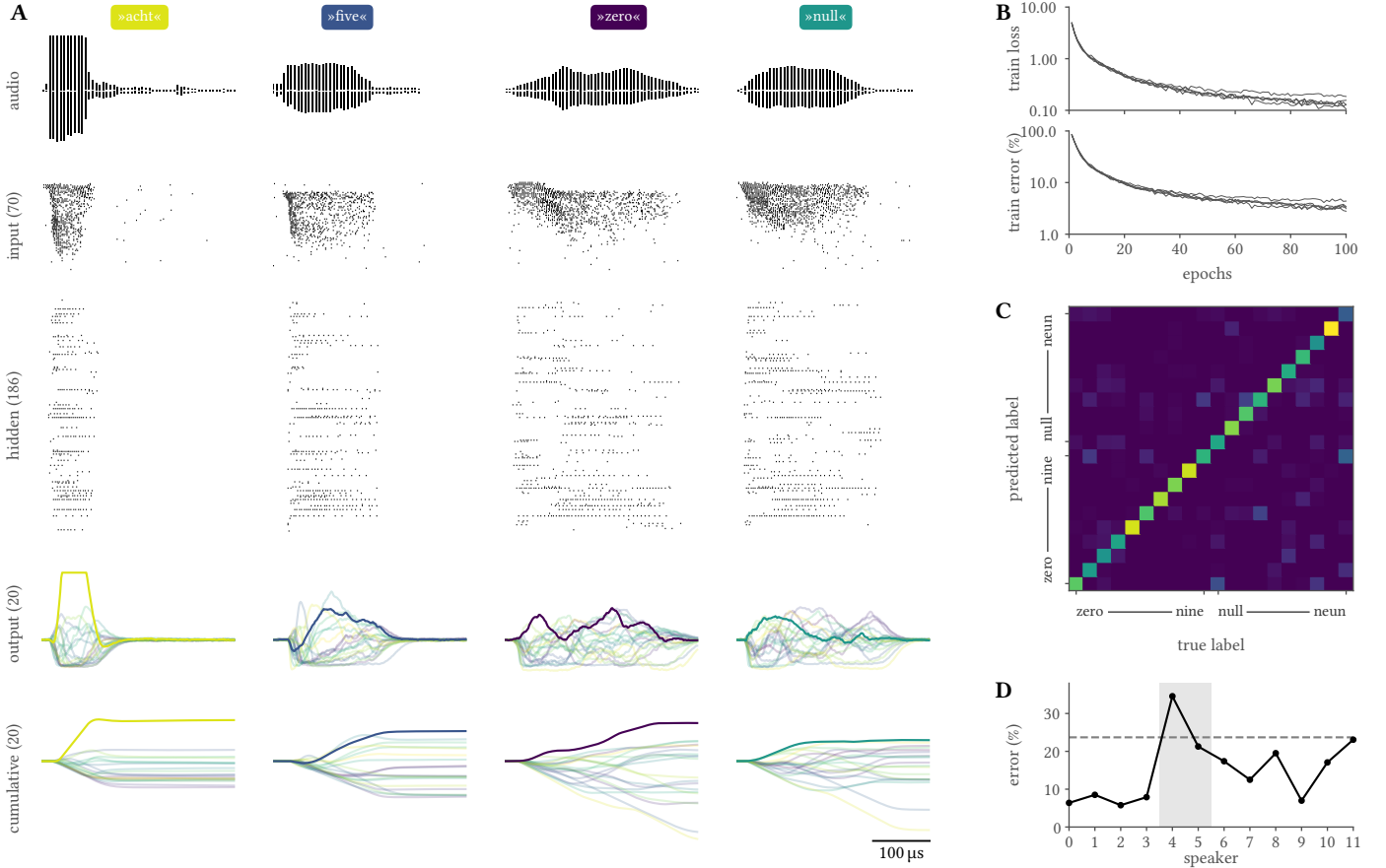
Figure 5: Classification of natural language with recurrent SNNs on BrainScaleS-2. **(A)** Responses of a recurrent network when presented with samples from the spiking Heidelberg digits (SHD) dataset. The input spike trains, originally derived from recordings of spoken digits (see illustrations), were reduced to 70 stimuli. The network was trained according to a sum-over-time loss based on the output units' membrane traces. For visualization purposes, we also show their cumulative sums. **(B)** Over 100 epochs of training, the network developed suitable representations as evidenced by a reduced training loss and error, here shown for five distinct initial conditions. **(C)** Classification performance varies across the twenty classes, especially since some of them exhibit phonemic similarities (»nine« vs. »neun«). **(D)** The trained network generalizes well on unseen data from most speakers included in the dataset. The discrepancy between training and overall test error (dashed line) arises from the composition of the dataset: 81 % of the test set's samples stem from two exclusive speakers (highlighted in gray).

Table 2: Comparison of MNIST benchmark results across neuromorphic platforms.

	platform	reference	architecture	node	accuracy	energy/inference	inferences/s	latency
digital	SpiNNaker	Stromatias et al., 2015 (48)	784-500-500-10	130 nm	95.0 %	– [iii]	– [iii]	–
	TrueNorth	Esser et al., 2016 (17)	CNN	28 nm	99.4 %	108.0 µJ	1 k	–
	Intel	Chen et al., 2019 (9)	236-20	10 nm	88.0 %	1.0 µJ	6.25 k	–
	Intel	Chen et al., 2019 (9)	784-1024-512-10	10 nm	98.2 %	12.4 µJ	–	–
	Intel	Chen et al., 2019 (9)	784-1024-512-10	10 nm	97.9 %	1.7 µJ	–	–
	MorphIC	Frenkel et al., 2019 (18)	784-500-10[i]	65 nm	97.8 %	205 µJ	–	–
	MorphIC	Frenkel et al., 2019 (18)	784-500-10[i]	65 nm	95.9 %	21.8 µJ	250	–
	SPOON	Frenkel et al., 2020 (19)	CNN	28 nm	97.5 %	0.3 µJ[ii]	–	117 µs
analog	BSS-1	Schmitt et al., 2017 (44)	100-15-15-5	180 nm	95.0 %	– [iii]	10 k	–
	BSS-2	Göltz et al., 2021 (22)	256-246-10	65 nm	96.9 %	8.4 µJ	21 k	<10 µs
	BSS-2	this work	256-246-10	65 nm	97.6 %	2.4 µJ	85 k	8 µs

[i] Segmented input and hidden layers. [ii] Based on pre-silicon estimates. [iii] Estimates were given by Pfeiffer et al., 2018 (40).

on rate-based or time-to-first-spike coding schemes. Here, we expanded ITL techniques into the realm of surrogate gradient learning which flexibly interpolates between rate- and timing-based coding schemes on multi-layer and recurrent architectures, thereby simultaneously improving performance and energy efficiency, while also being conducive for fast inference (14).

Comparing the performance of neuromorphic SNN implementations is an intricate task in itself, starting with a lack of standardized benchmarks (12, 15). When aspiring to sound the spectrum of different neuromorphic architectures and SNN coding schemes, one furthermore stumbles upon inhomogeneous standards of determining a system's energy consumption, ranging from pre-silicon estimates of a neuromorphic

core's current draw to full-system lab measurements. We, nevertheless, attempted to contrast our findings with results from previous studies on both digital as well as analog systems (Table 2). Although lacking the essence of temporal spike-based information processing, we considered the MNIST dataset due to its widespread adoption.

Our model on BrainScaleS-2 performed competitively in all metrics and – in terms of accuracy – was surpassed only by much larger or convolutional networks. When considering the energy footprint, BrainScaleS-2 reached values only outperformed by optimized architectures fabricated in much smaller and hence more efficient technology nodes (9, 19). In comparison to other neuromorphic systems, we were able to set new benchmarks in terms of throughput and classification latency.

In summary, our work shows how learning can efficiently compensate for device-specific imperfections, thereby allowing us to employ analog neuromorphic substrates for complex, energy-efficient, and ultra-low latency information processing. Importantly, it also is the first step toward future on-chip learning algorithms that could even take advantage of such device heterogeneity (39). Thus our work gives a glimpse of how powerful learning algorithms will empower future neuromorphic technologies.

Materials and methods

Software environment Our training framework was based on PyTorch's auto-differentiation library (38). It furthermore builds upon the BrainScaleS-2 software stack to configure the neuromorphic system and execute the experiments (36).

Input coding For MNIST we scaled down the dataset to 16×16 pixels by first discarding the two outermost rows and scaling the remaining pixels. The images were then converted to spikes by interpreting the normalized pixel grayscale values x_i as input currents to LIF neuons. Strong enough currents trigger a spike at time $t_i = \tau_{in} \log x_i/(x_i - \vartheta_{in})$, where τ_{in} denotes the input units time constant and ϑ_{in} its threshold.

Since the SHD dataset is provided in form of input spike times, a custom conversion was not required. For SHD we reduced the original 700 input channels by subsampling. Specifically, we omitted the first 70 and then retained every ninth input unit. The time dimension was scaled by a factor of 2000 to account for the system's acceleration factor of of 1000 and further shorten the experiment duration to reduce the computation burden on the host system. When employing data augmentation, a spike originally originating from input channel i was reassigned to a neighboring channel drawn from $\mathcal{N}(\mu = i, \sigma)$. This augmentation was applied prior to downsampling the inputs.

Initialization We used Kaming's initialization (23) for both the hidden and output layer weights. Specifically, weights were drawn from a normal distribution with zero mean and a standard deviation of $\hat{\sigma}_w/\sqrt{N_{H,L}}$.

Weight scaling Weight values had to be scaled, rounded, and cropped to the neuromorphic system's weight resolution of 7 bit signed integers resulting from merging two 6 bit synapse

circuits. The exact scaling took into account analog bias currents and other technical parameters. Due to the absence of a threshold for the non-spiking output layer, its membrane traces could be scaled arbitrarily.

For the MNIST classification, we adopted a dynamic weight scaling for the output weights by aligning the largest absolute weight value as represented in software to the maximum weight possible on the substrate.

Table 3: Parameters for the neuromorphic substrate and learning framework.

parameter	value (MNIST / SHD)
difference threshold-leak $\vartheta - V_{leak}$	$(270 \pm 15)\,\mathrm{mV}$
membrane time constant τ_m	$(5.7 \pm 0.3)\,\mu s$ / $(10.0 \pm 0.3)\,\mu s$
in computation graph	$6.0\,\mu s$ / $10.0\,\mu s$
synaptic time constant τ_s	$6\,\mu s$ / $10\,\mu s$
input unit time constant τ_{in}	$8\,\mu s$ / $-$
input unit threshold ϑ_{in}	0.2 / $-$
surrogate gradient steepness β	50
learning rate η	1.5×10^{-3}
learning rate decay per epoch γ_η	0.03 / 0.025
amplitude regularization strength ρ_a	4×10^{-4} / $-$
burst regularization strength ρ_b	0.005 / $-$
rate regularization strength ρ_r	$-$ / 0.6×10^{-3}
rate regularization threshold ϑ_r	$-$ / 600
time step/sample period Δt	$1.7\,\mu s$
weight initialization spread $\hat{\sigma}_w$	0.24

Contributions

B. Cramer, S. Billaudelle, and F. Zenke conceived the work. B. Cramer and S. Billaudelle implemented the software, performed the experiments, and analyzed the data. S. Kanya and A. Leibfried contributed to the implementation. J. Schemmel is the lead designer and architect of the BrainScaleS-2 neuromorphic system. A. Grübl, V. Karasenko, C. Pehle, K. Schreiber, and Y. Stradmann contributed to the design of the BrainScaleS-2 system. J. Weis contributed the calibration routines. B. Cramer, S. Billaudelle, and F. Zenke wrote the manuscript with input from the other authors.

Acknowledgements

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