**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:

| Name: Hamza Shabbir Sahapurwala | SRN:PES2UG24CS177 | Section: C |
| --- | --- | --- |

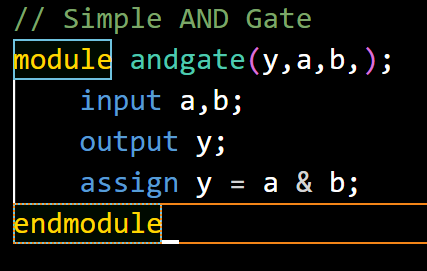
Week Number:1 Program Number:

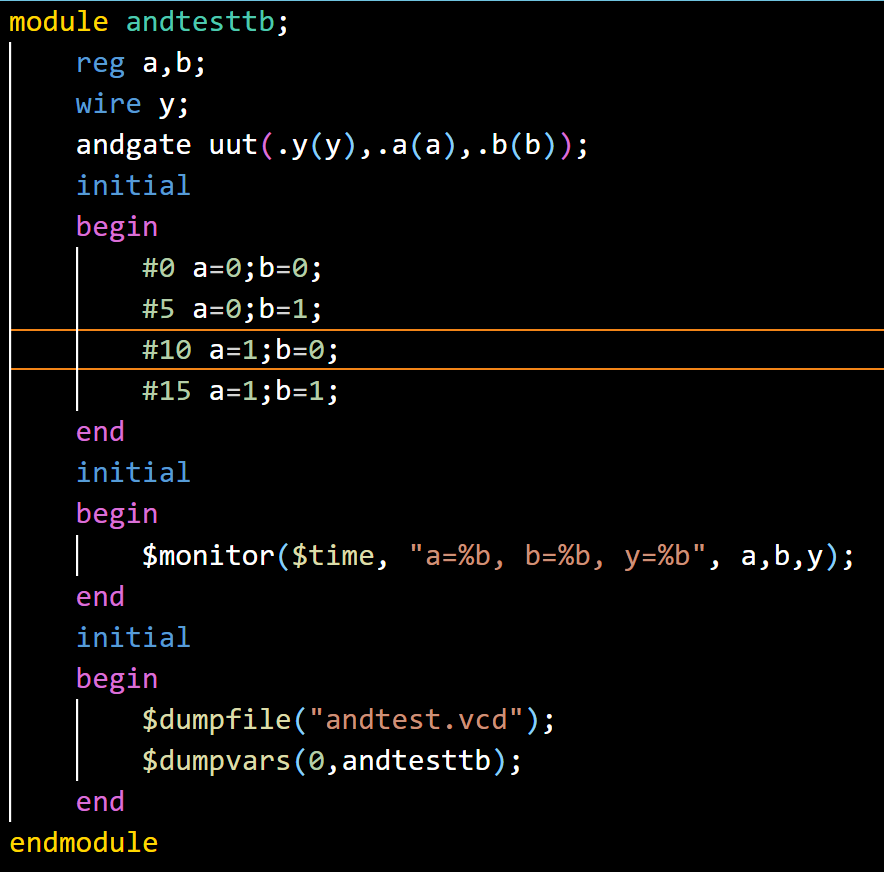
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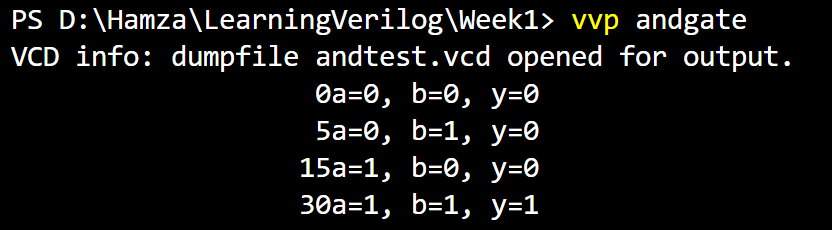
Deliverables

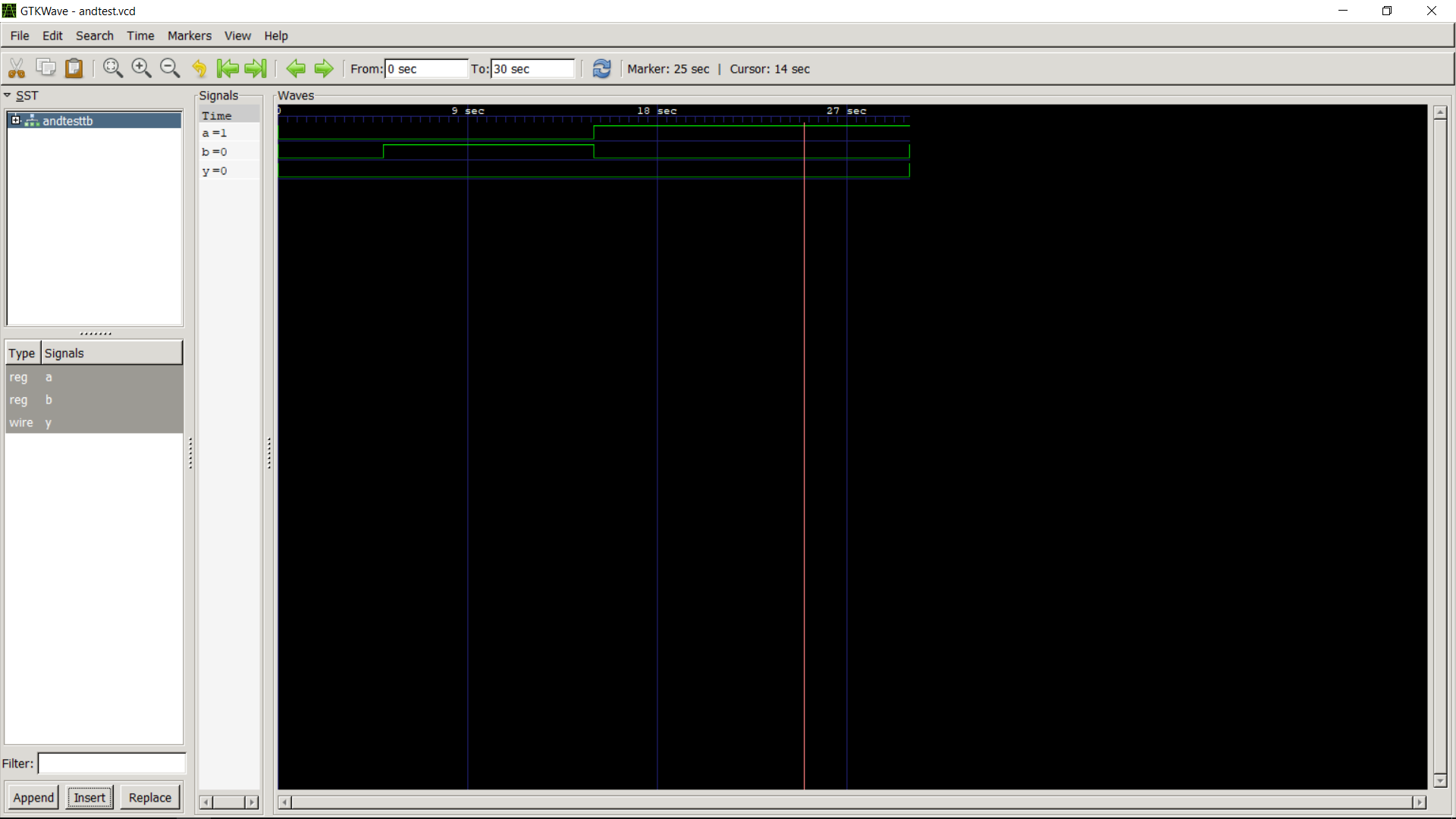
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

And Gate:

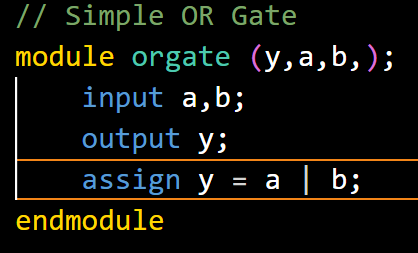


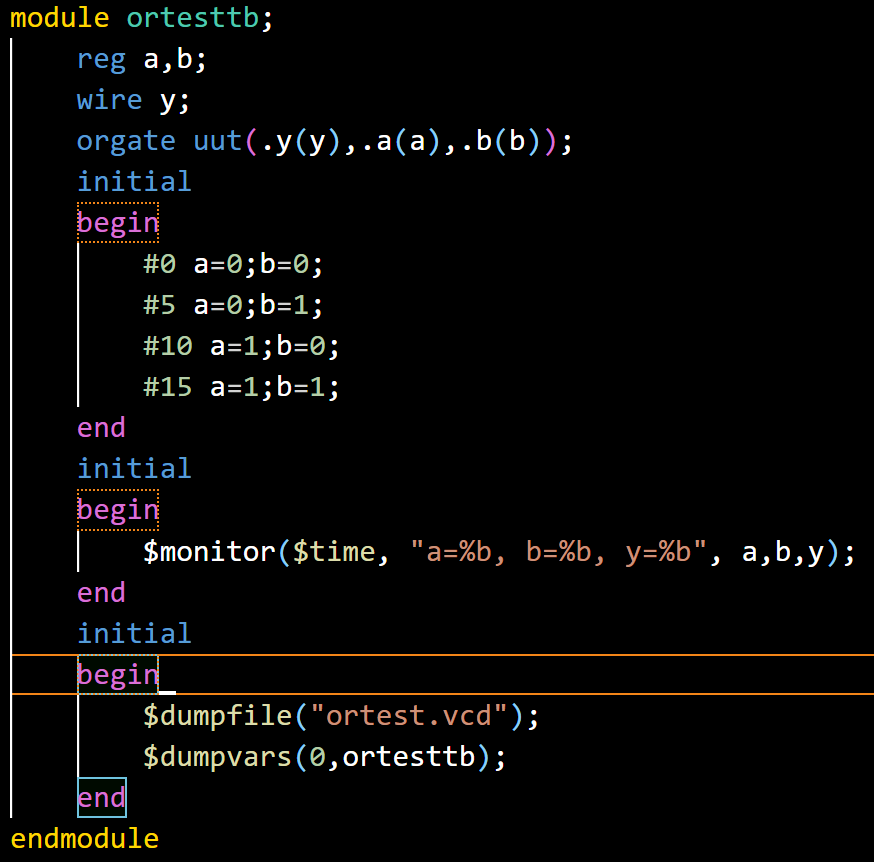


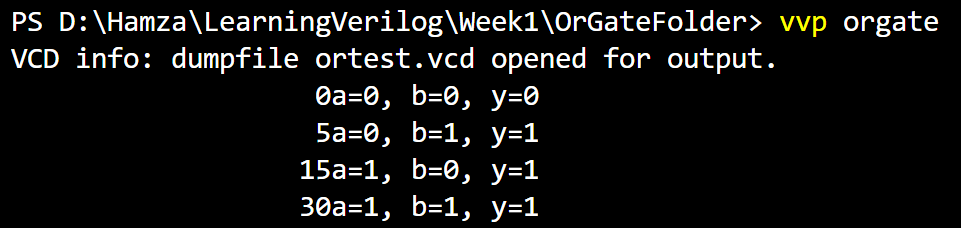


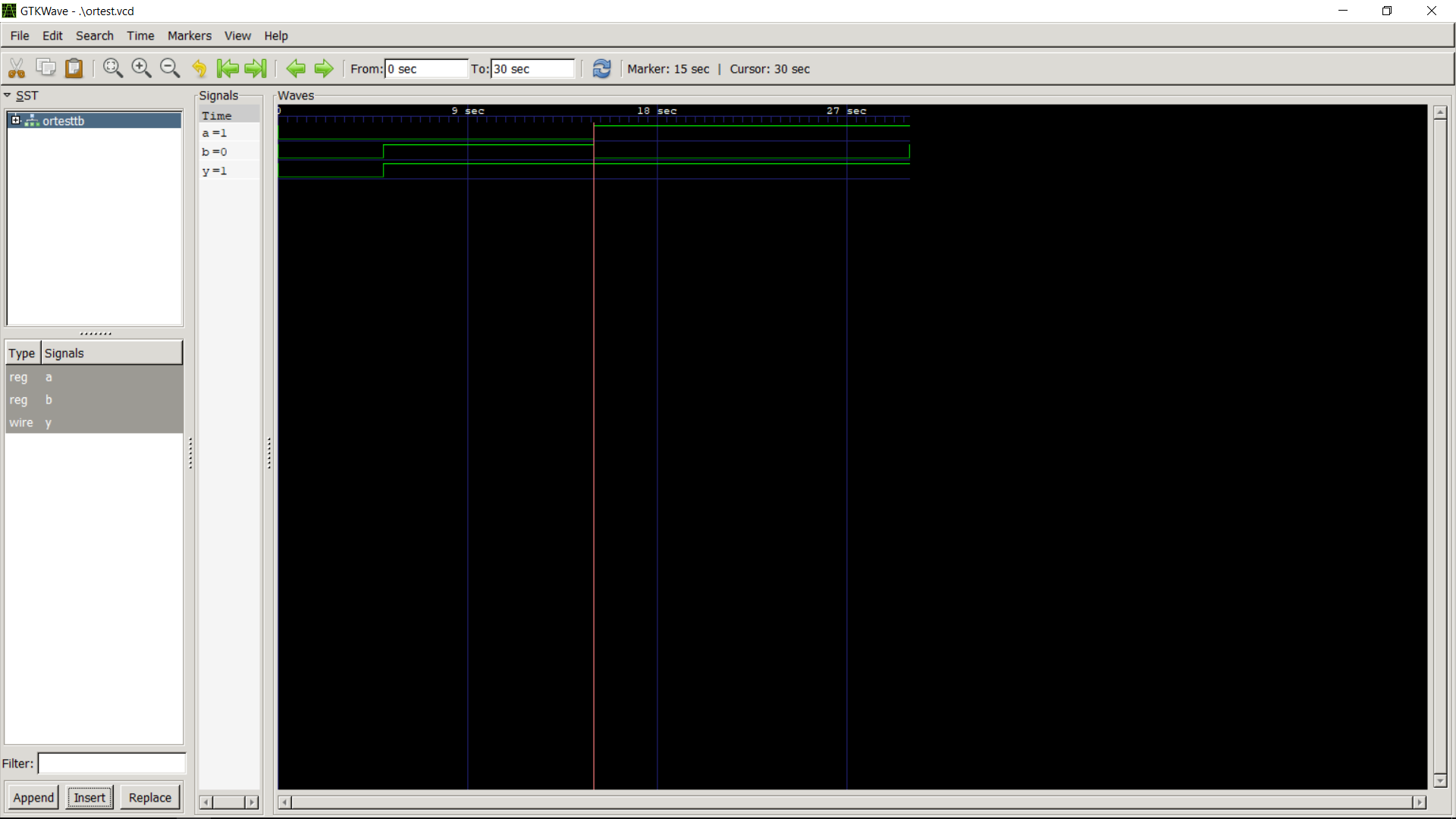


Or Gate:

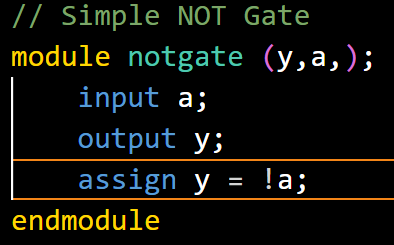


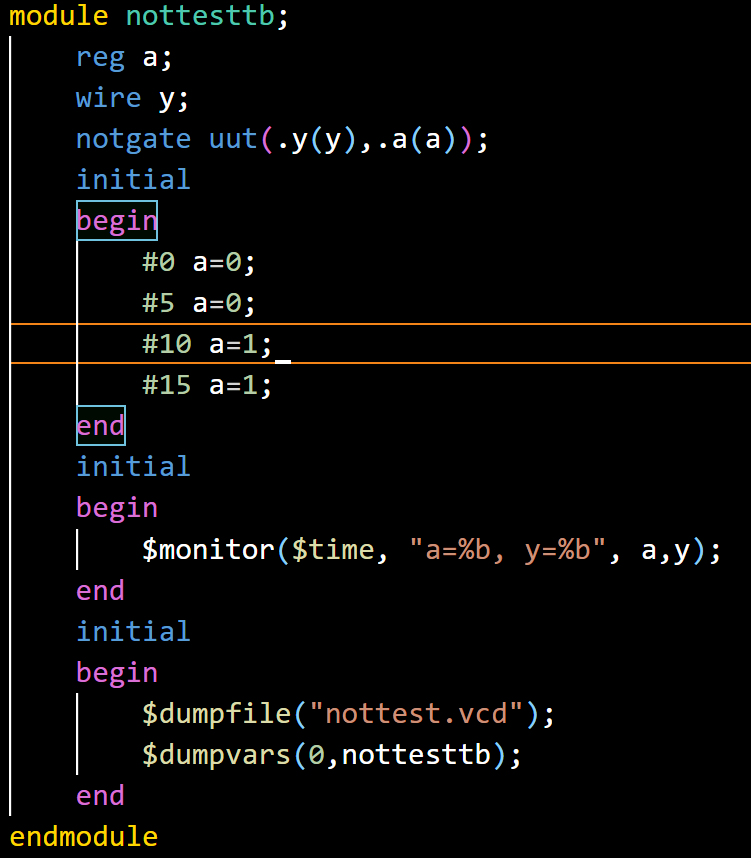


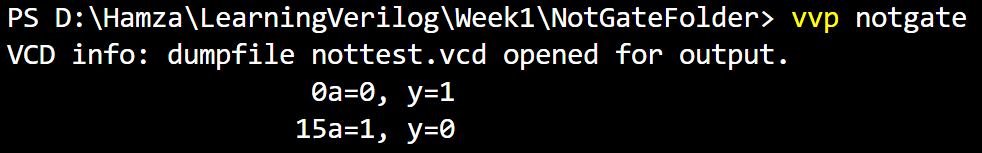


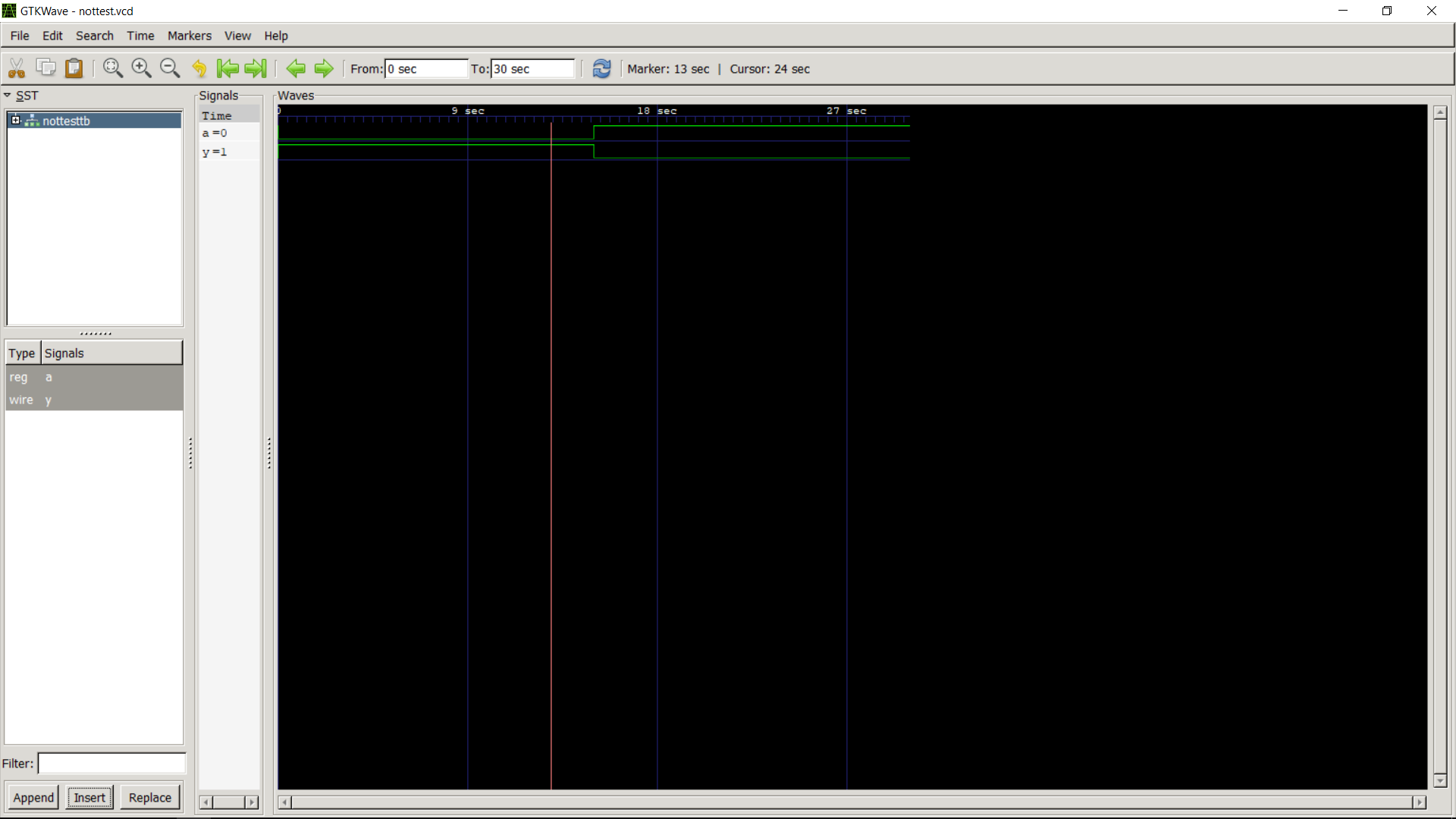


Not Gate:









Xor Gate:

