**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:

|  |  |  |
| --- | --- | --- |
| Name: | SRN: | Section: |

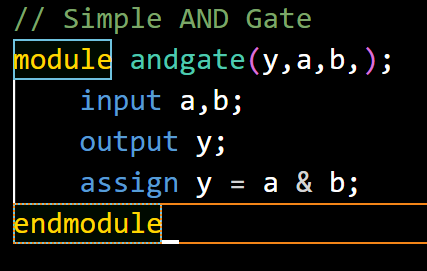
Week Number:1 Program Number:

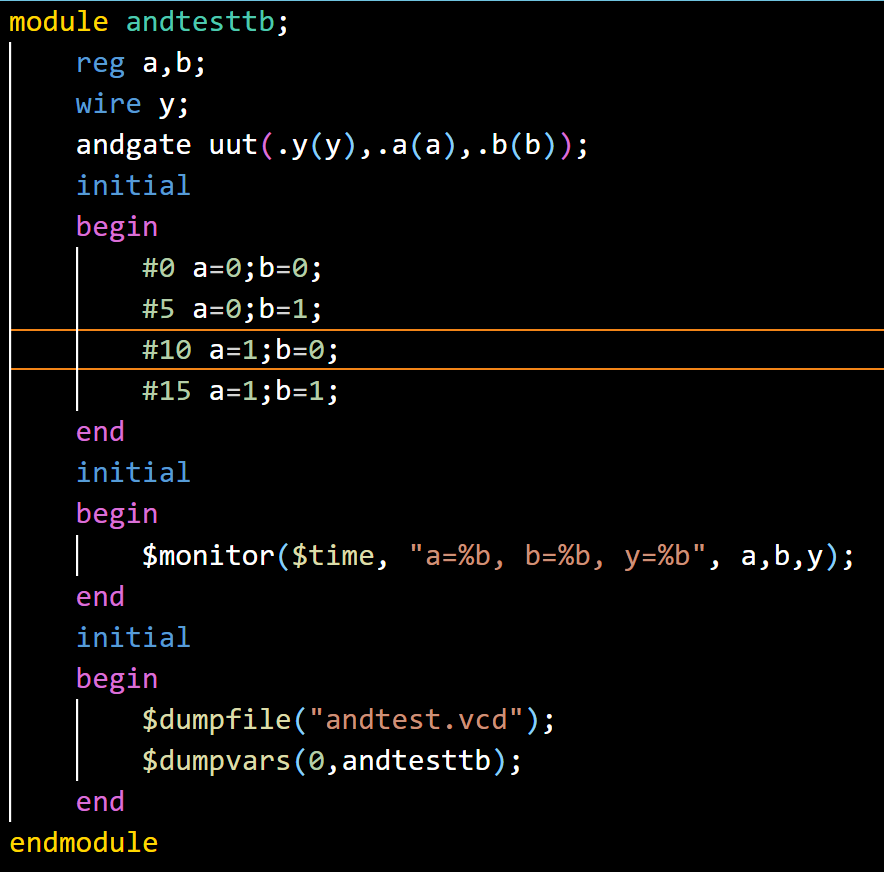
TITLE:

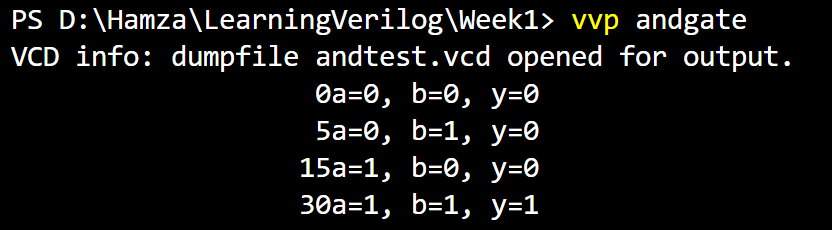
Deliverables

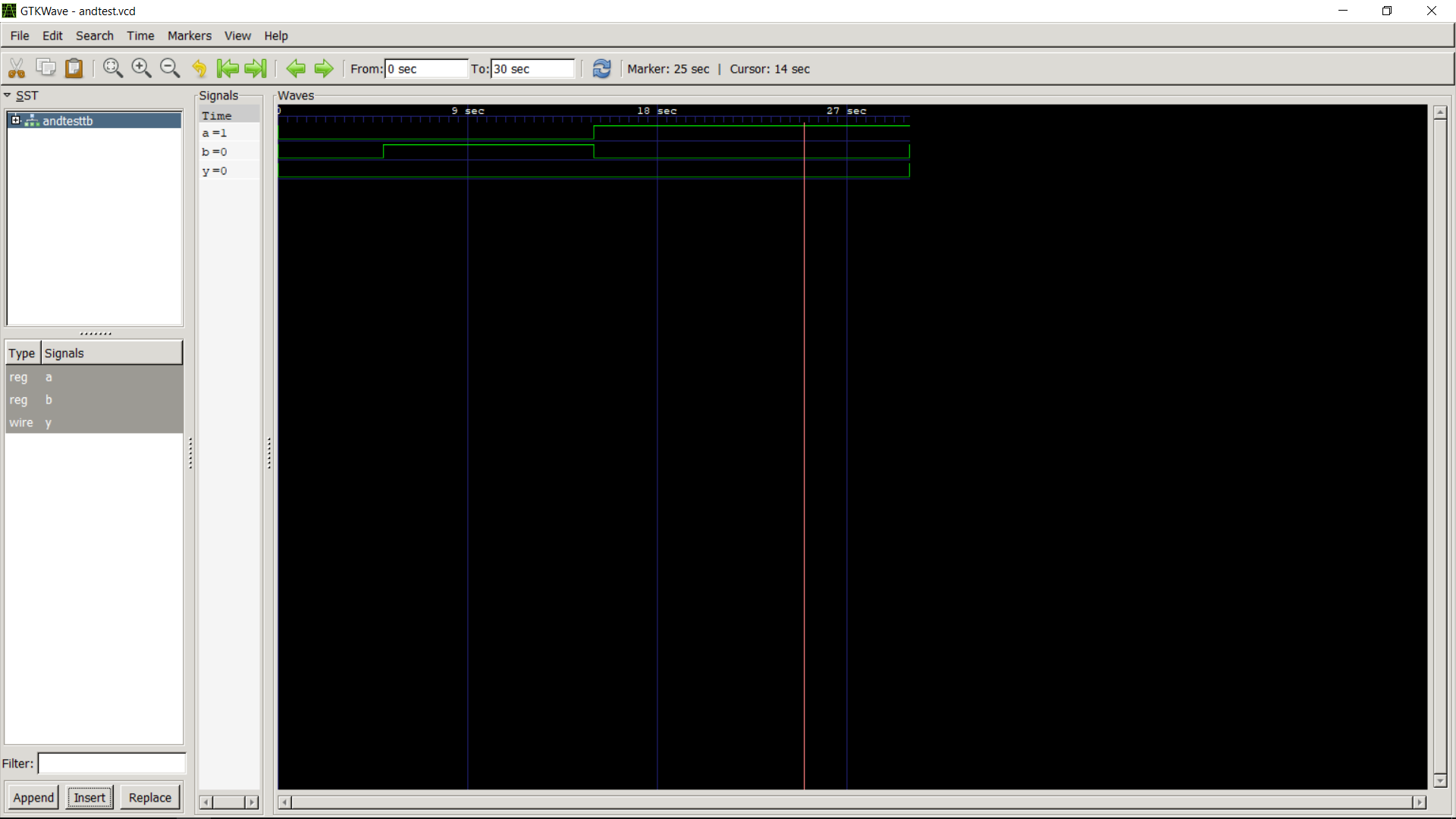
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

And Gate:

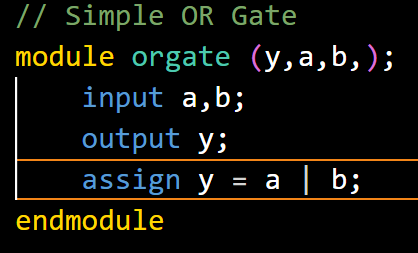


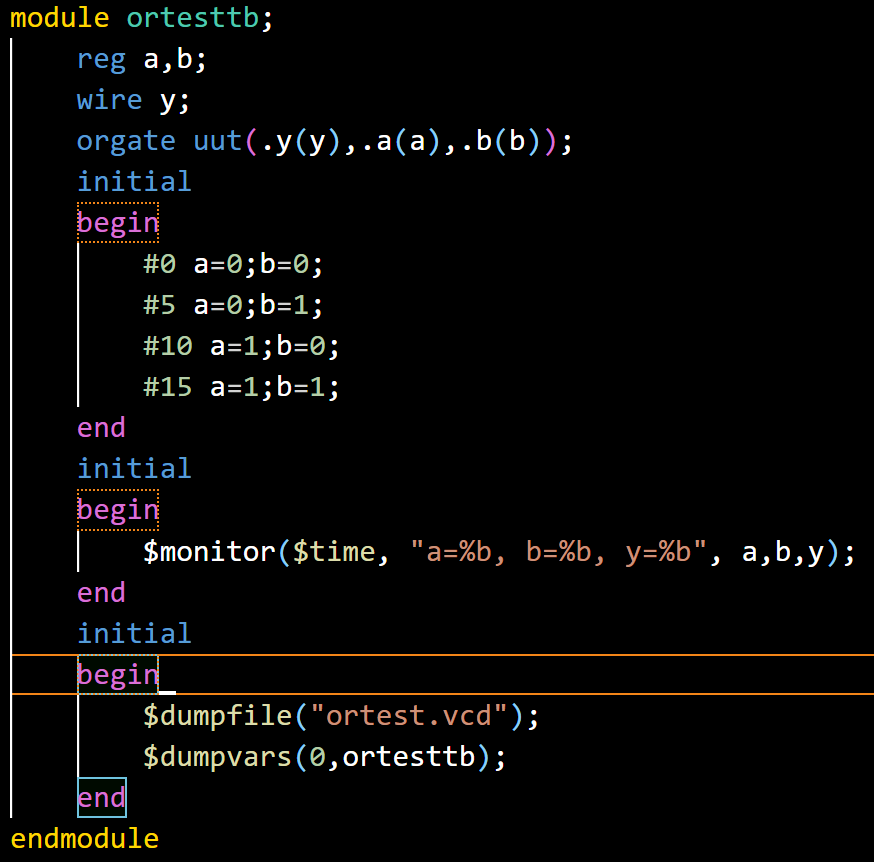


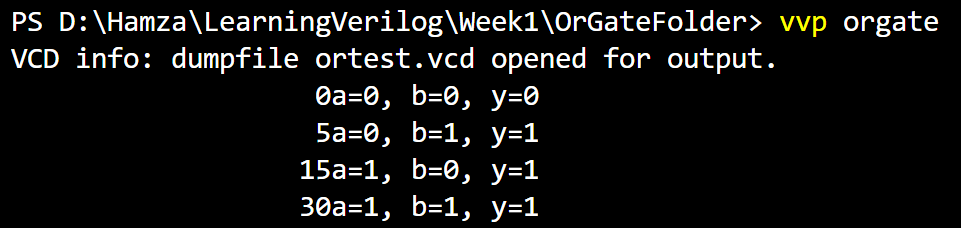


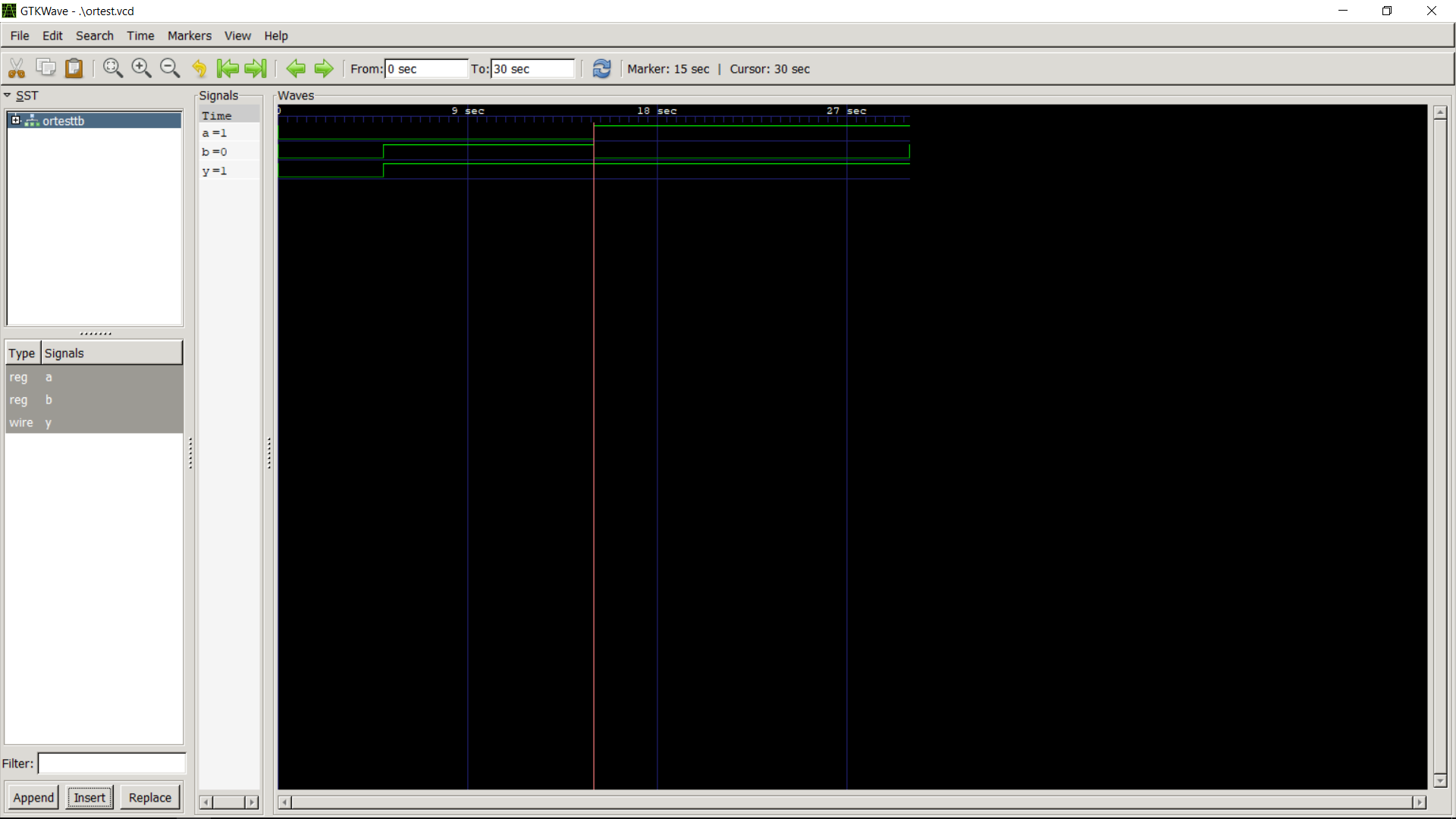


Or Gate:

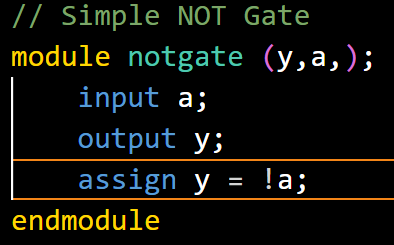


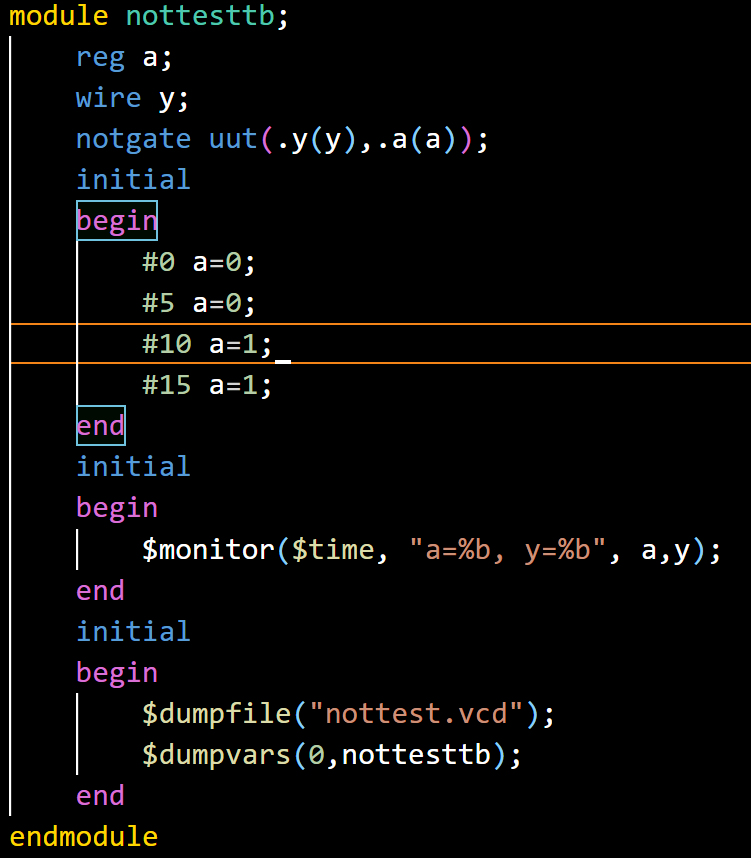


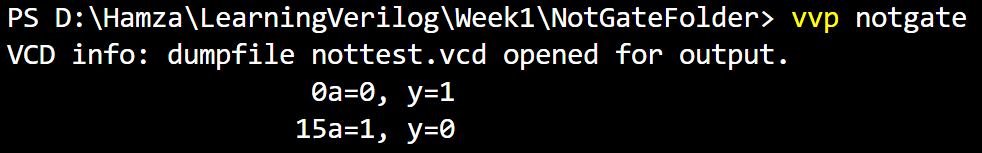


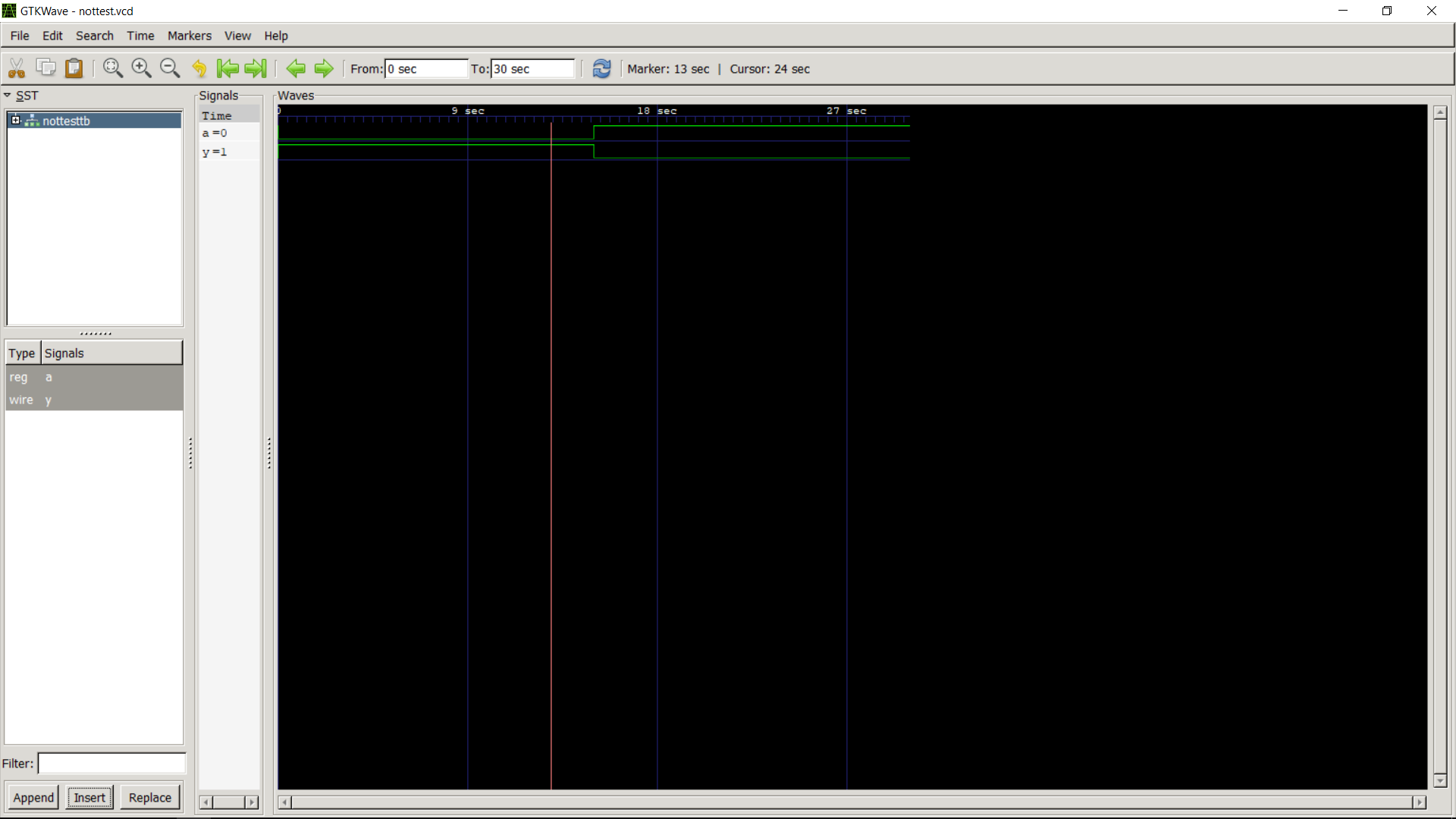


Not Gate:









Xor Gate:

