**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:11/8/2025

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| Name: | SRN: | Section  S |

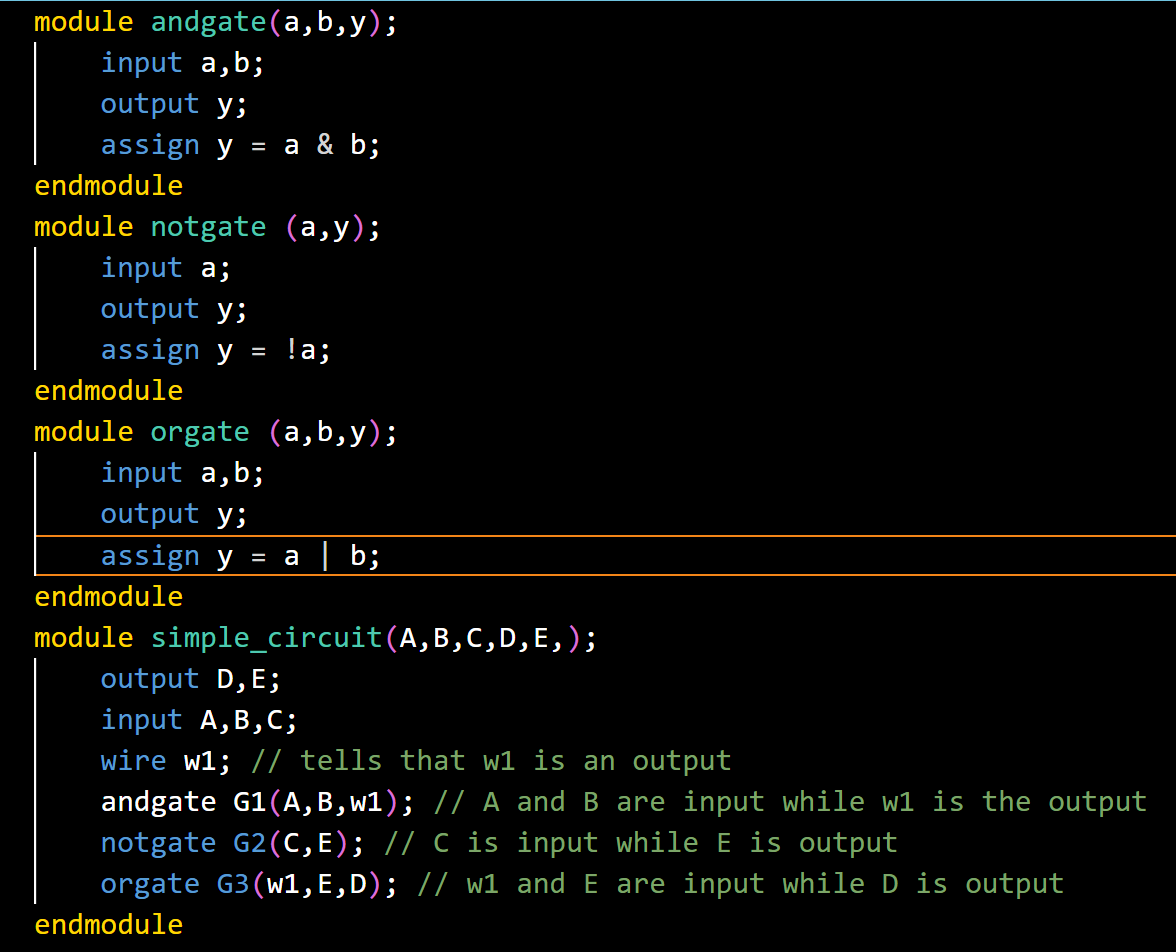
Week Number: 2 Program Number:

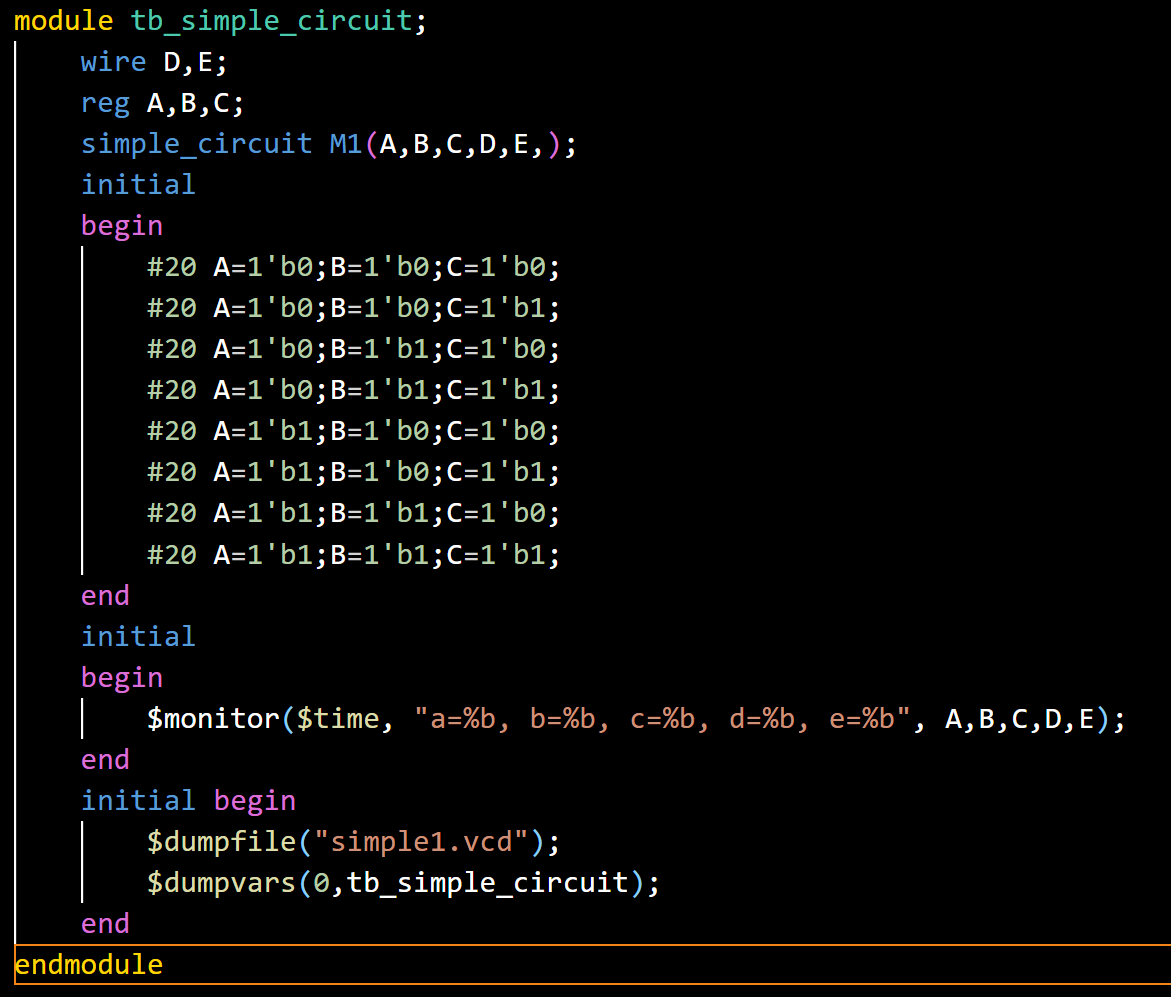
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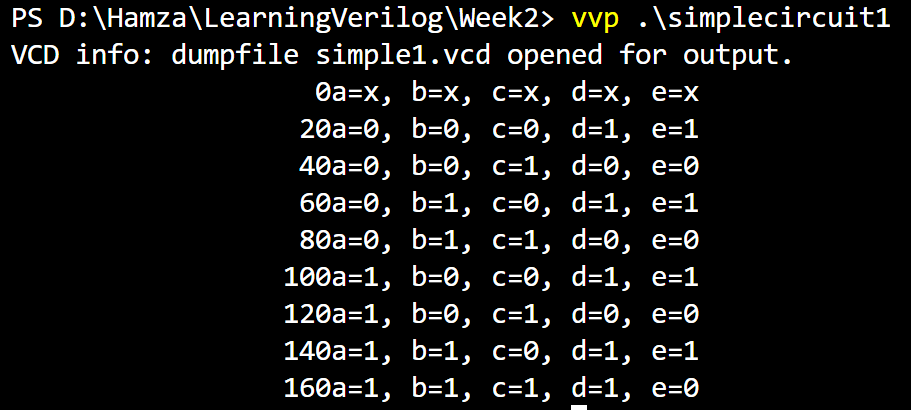
Deliverables

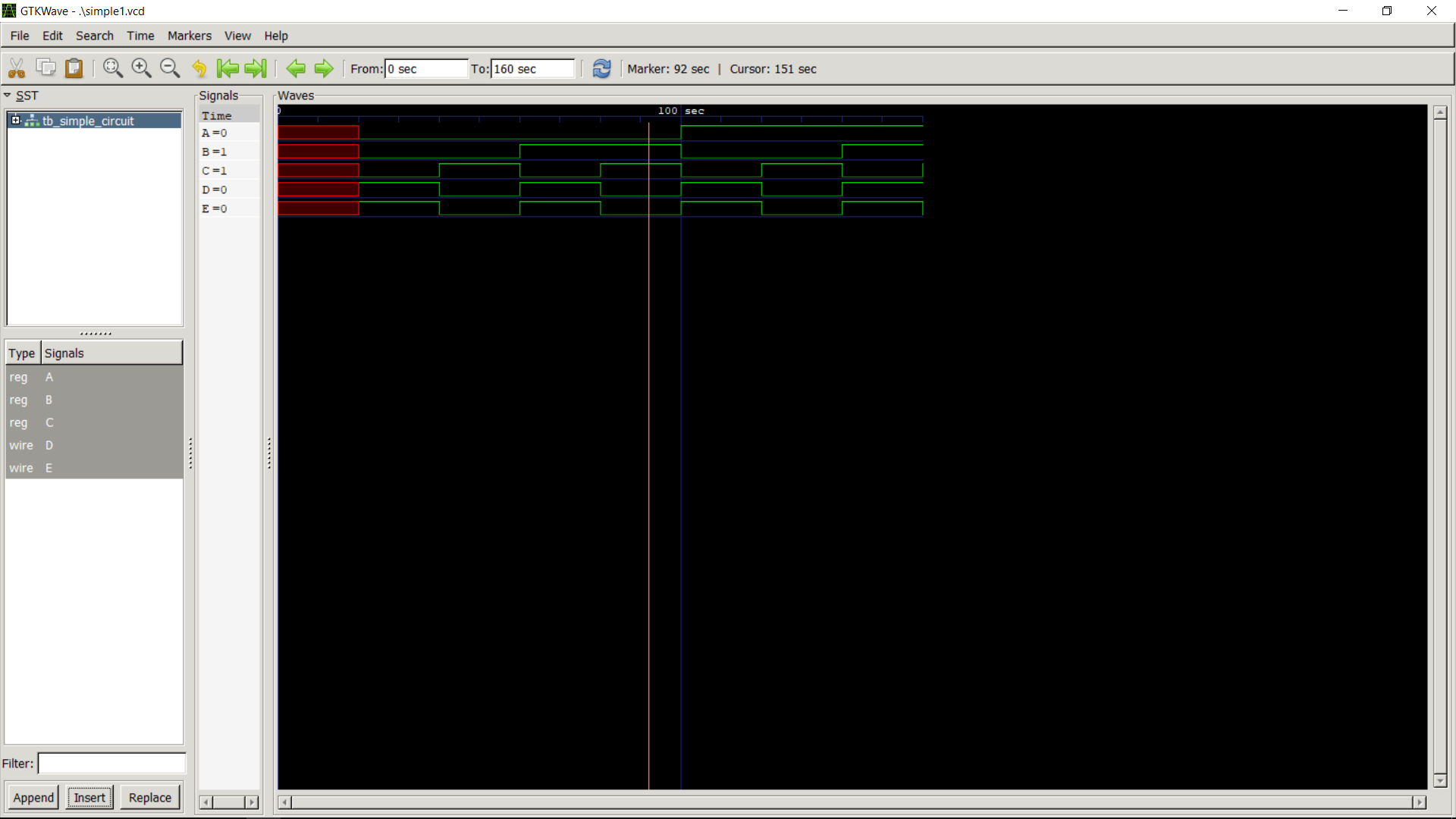
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

Circuit 1:

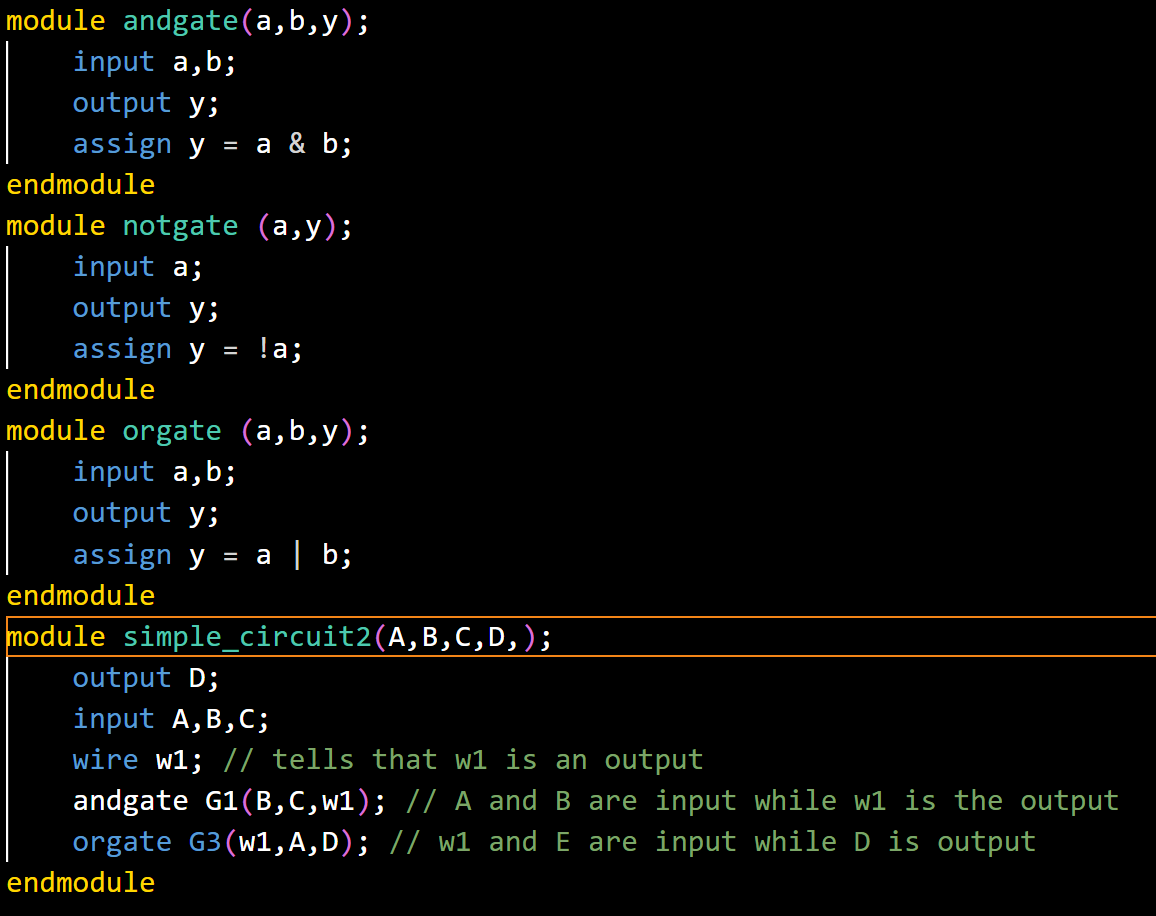


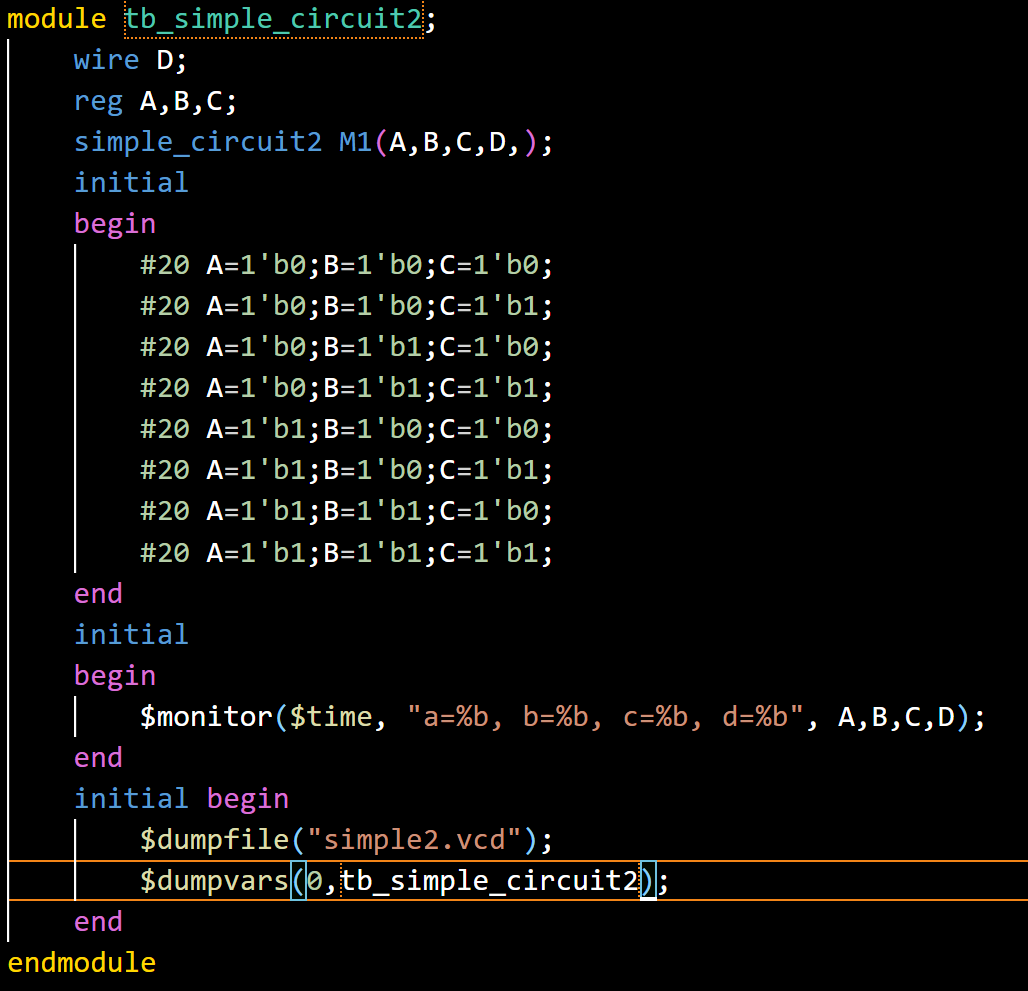


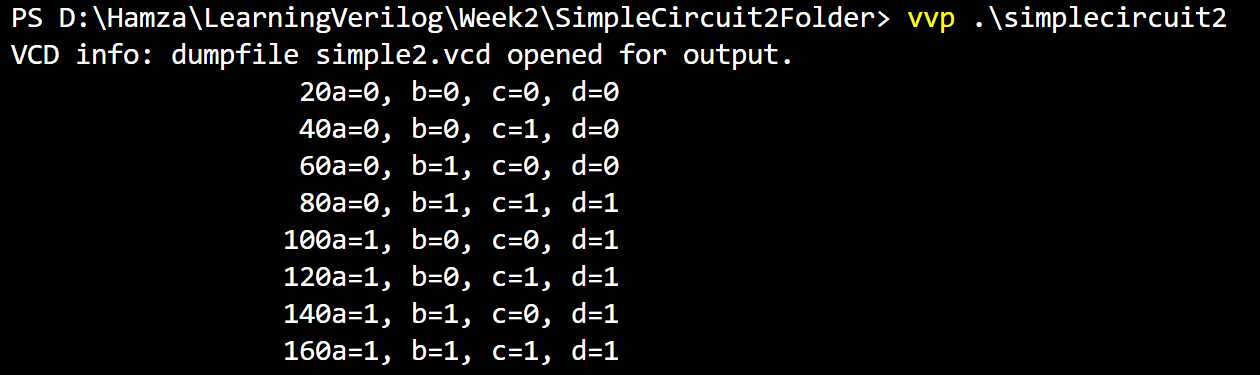


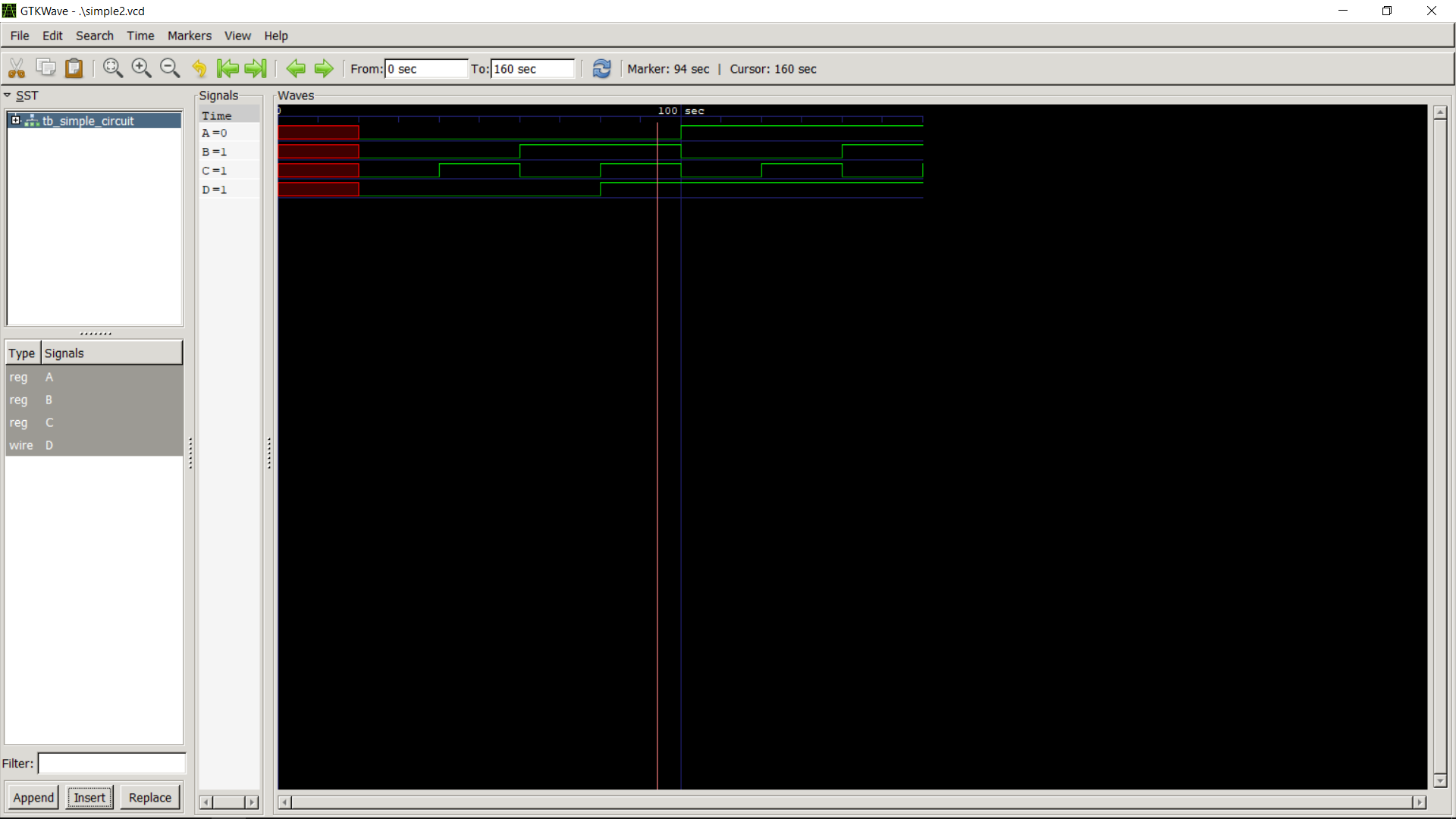


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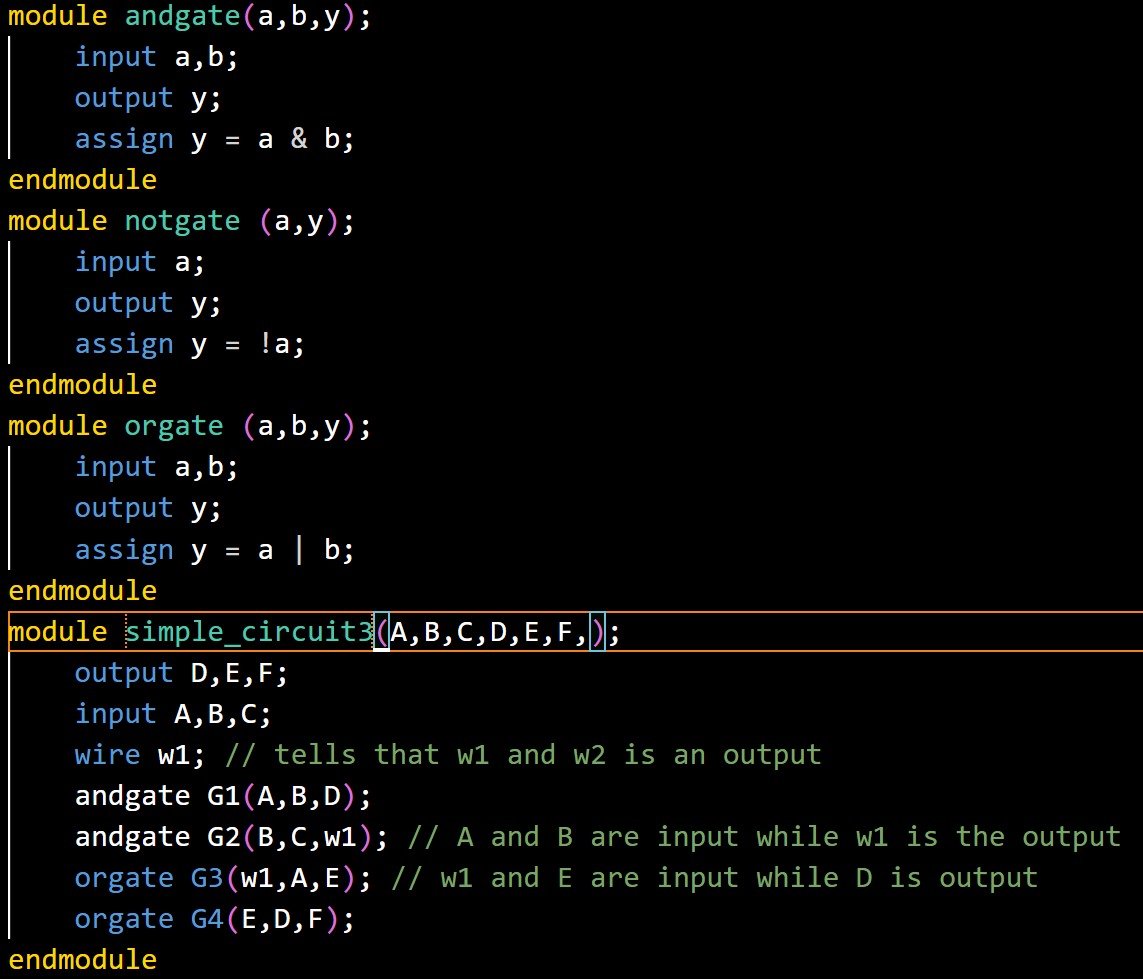


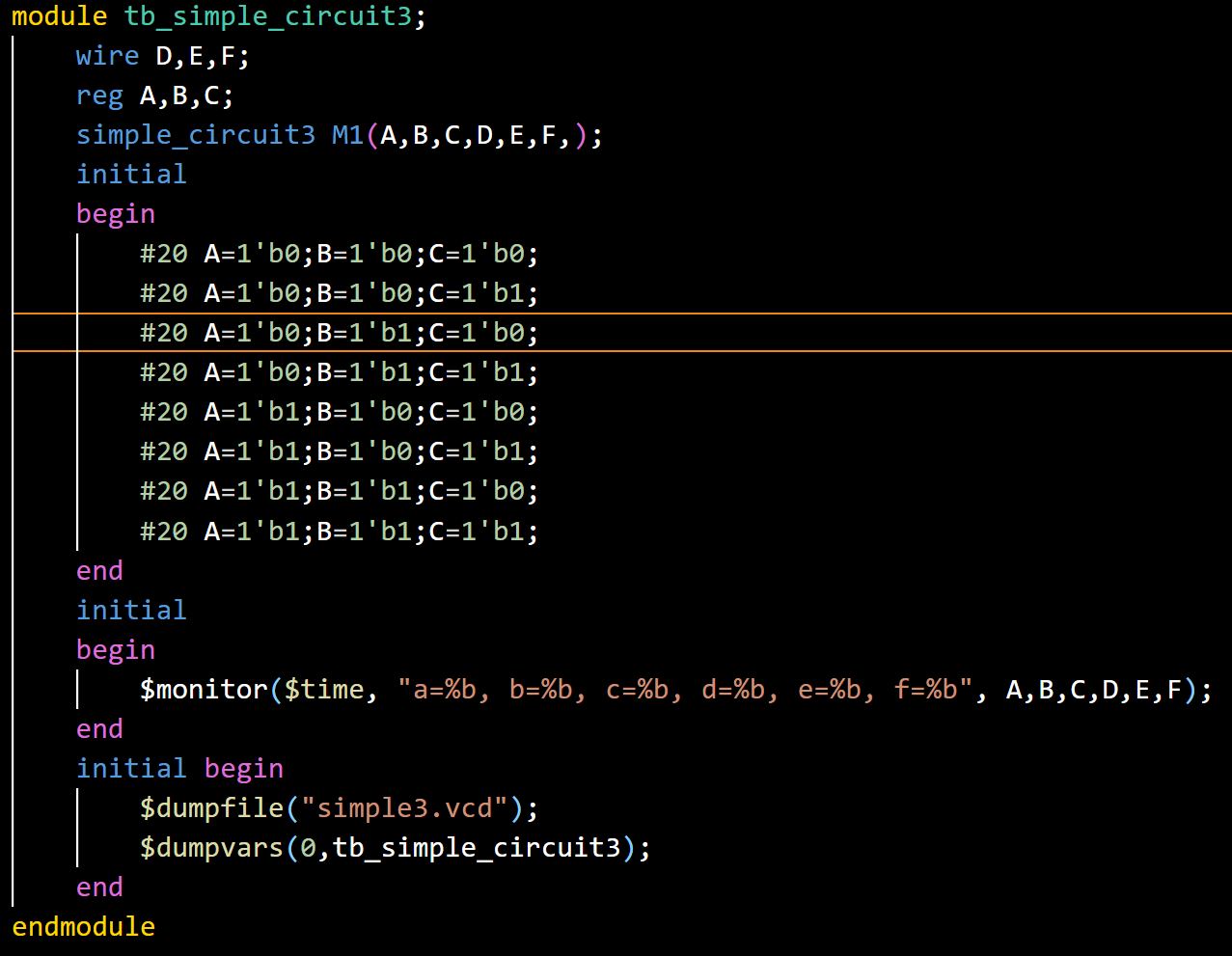


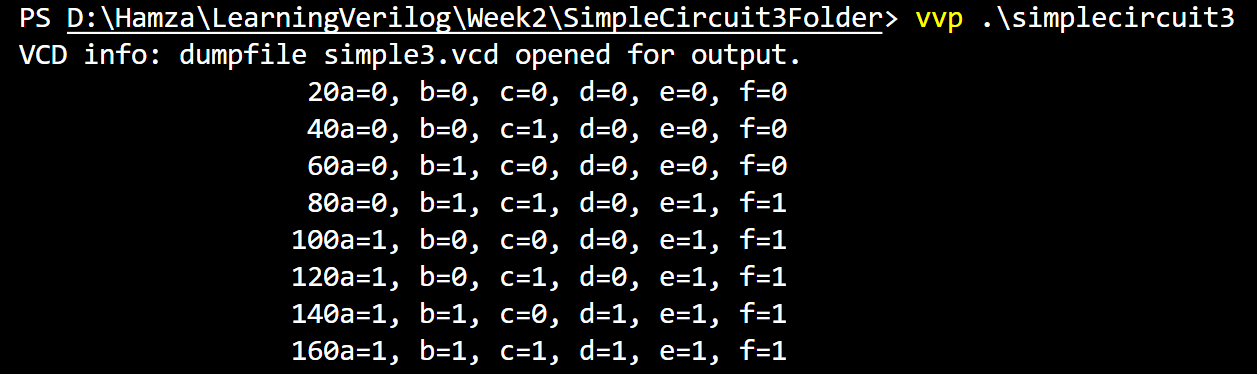


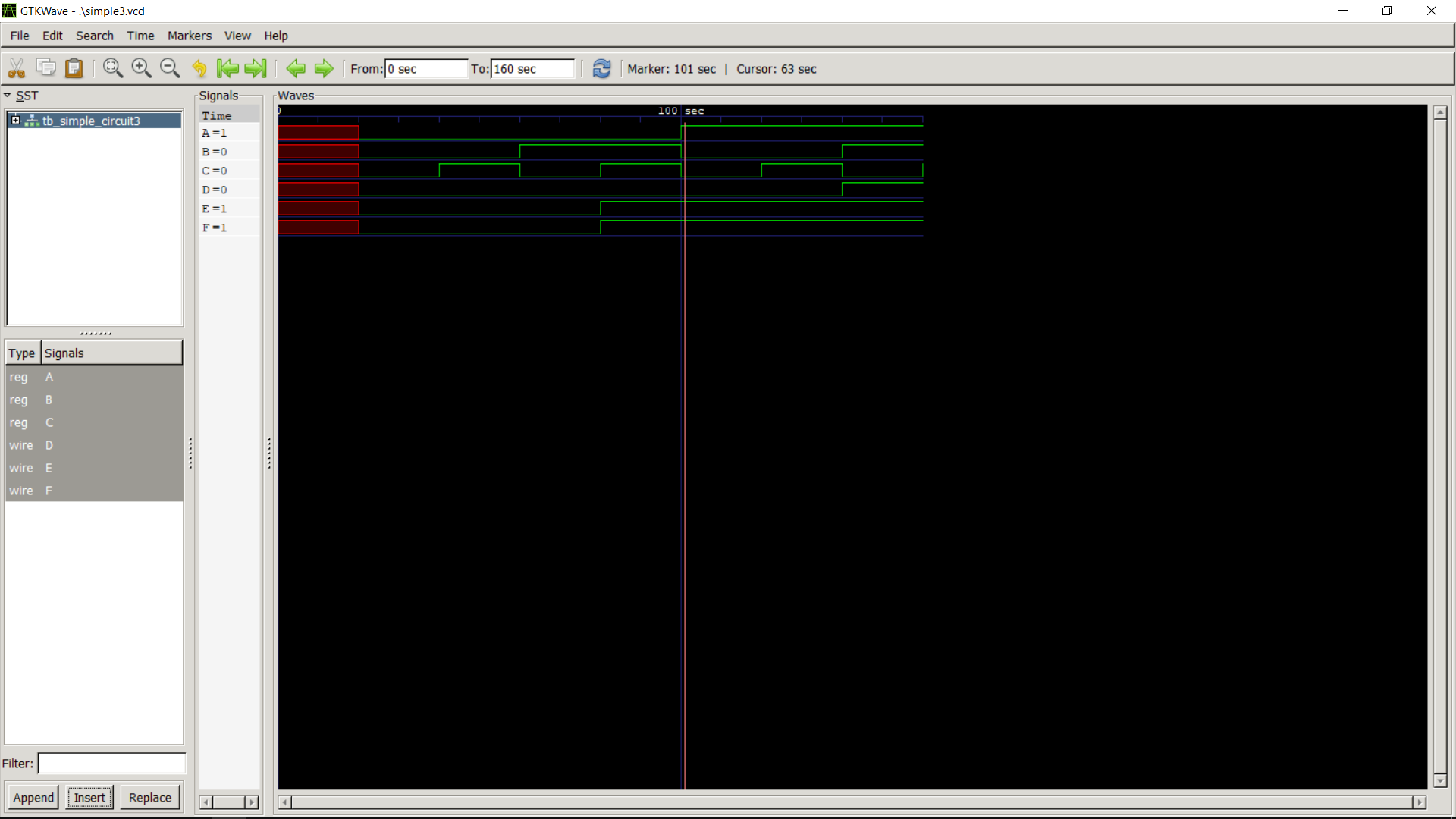


Circuit 3:









Circuit 4:

