**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:18-8-2025

|  |  |  |
| --- | --- | --- |
| Name: | SRN: | Section |

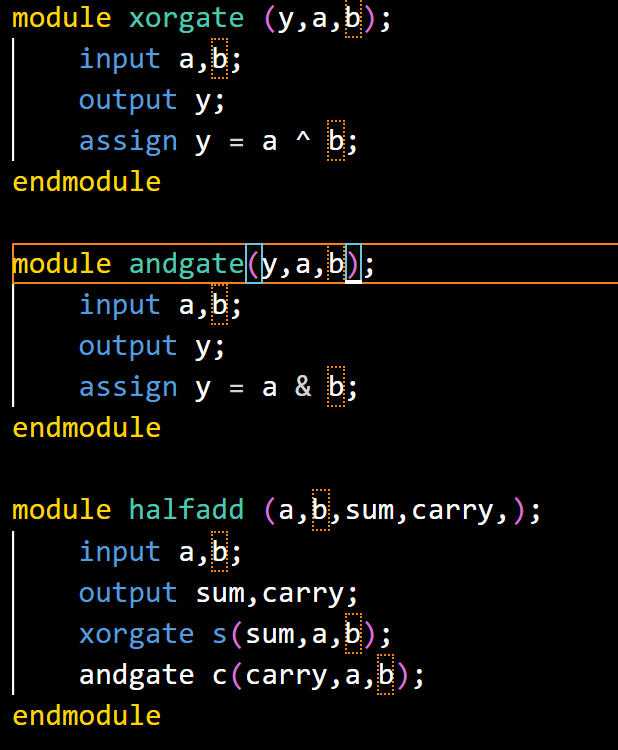
Week Number: 3 Program Number:

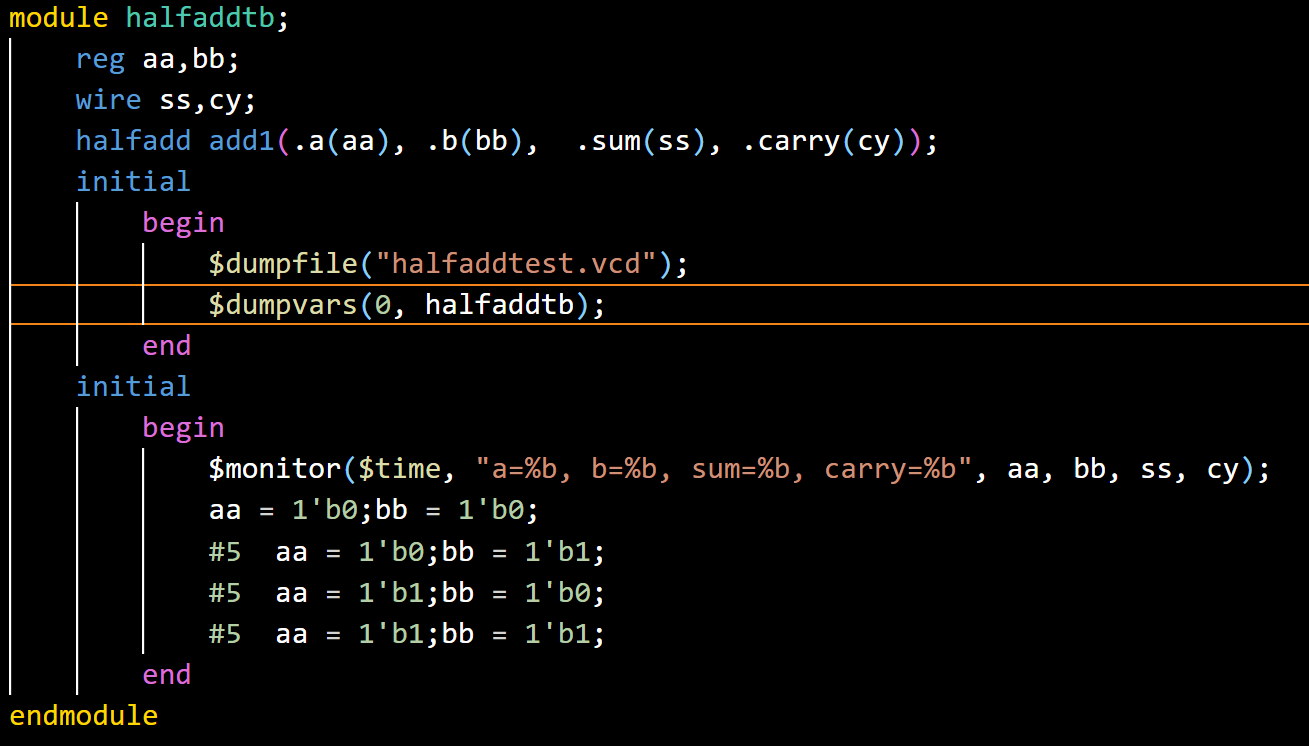
TITLE:

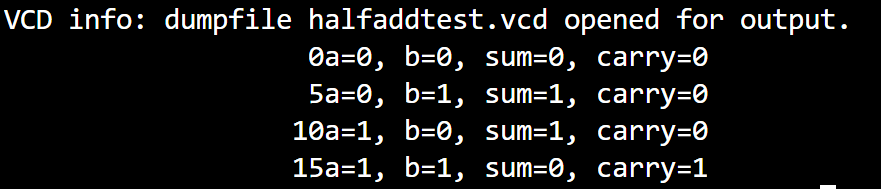
Deliverables

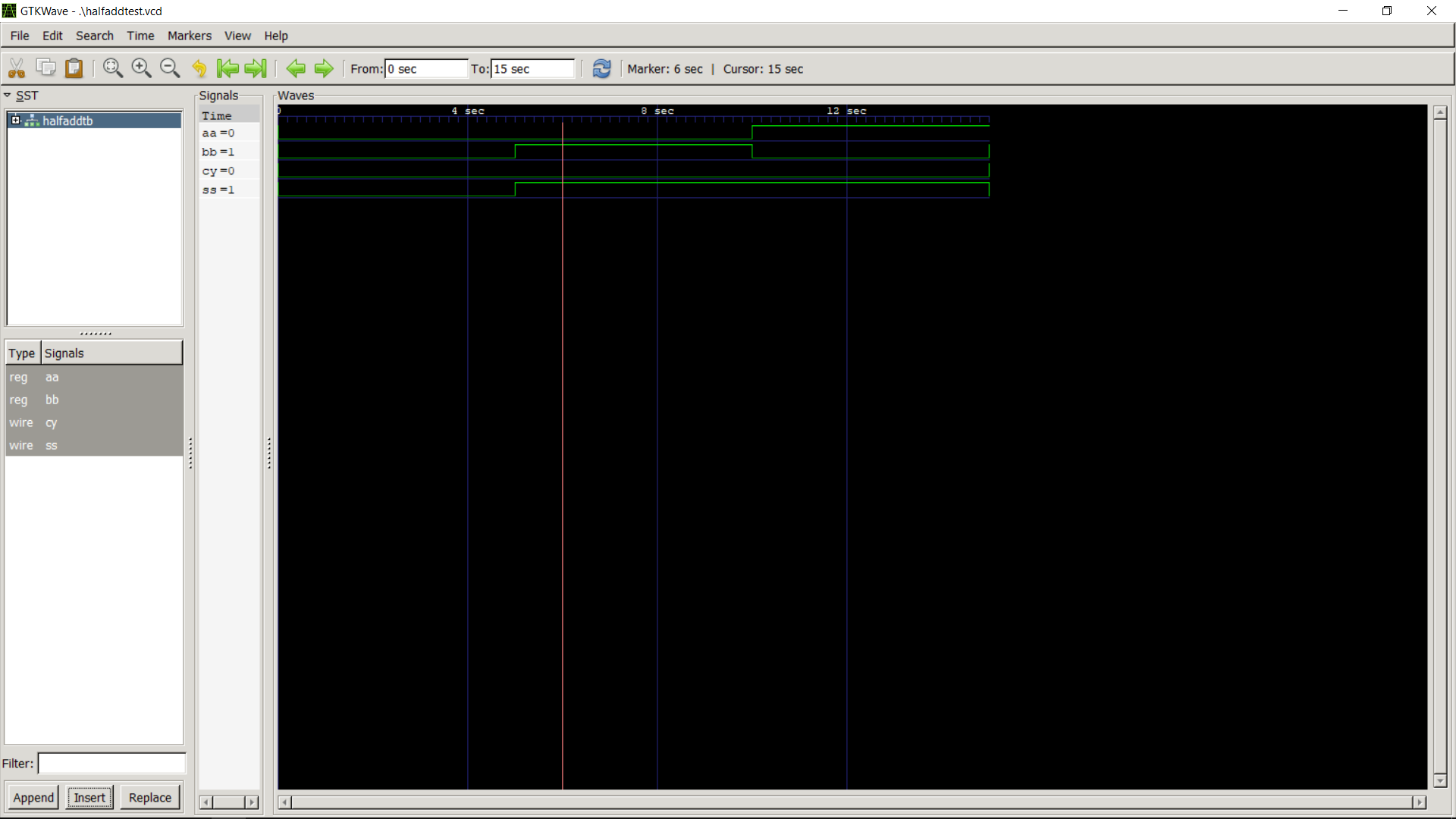
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

Half Adder:

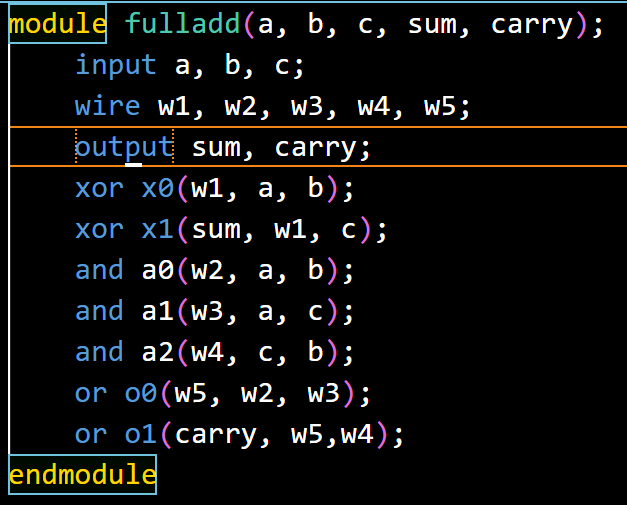


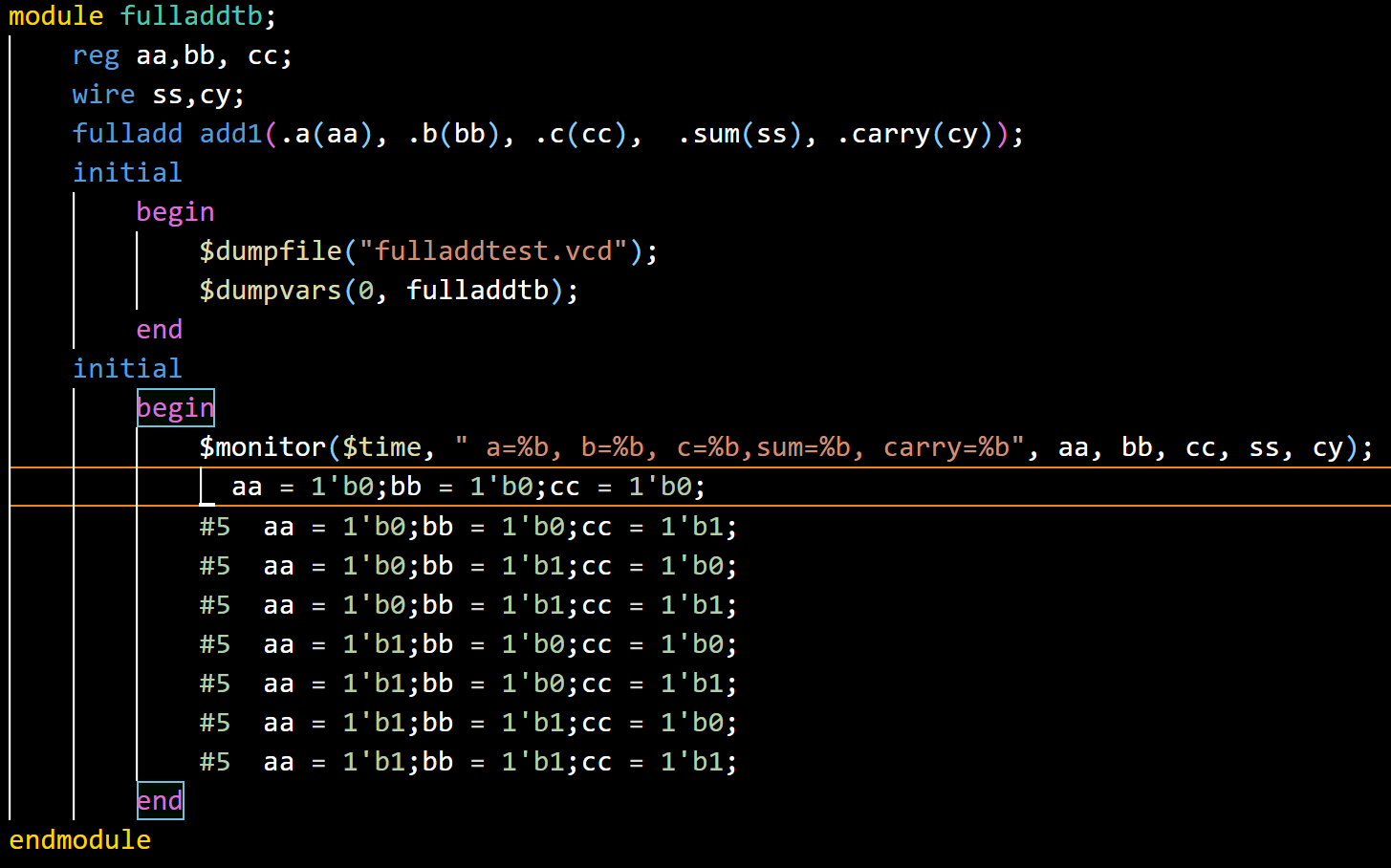


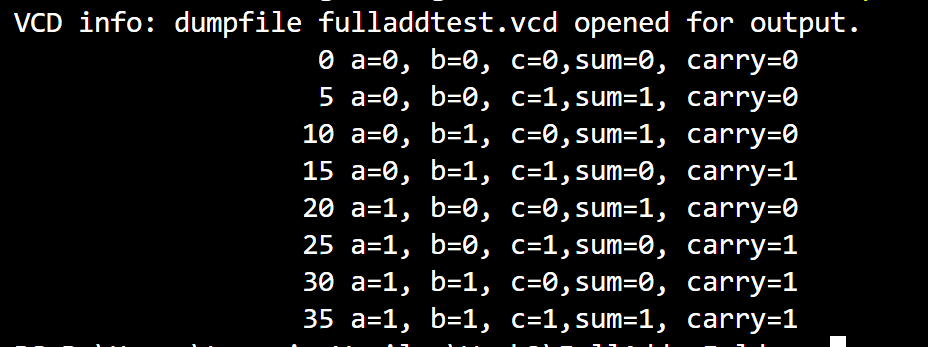


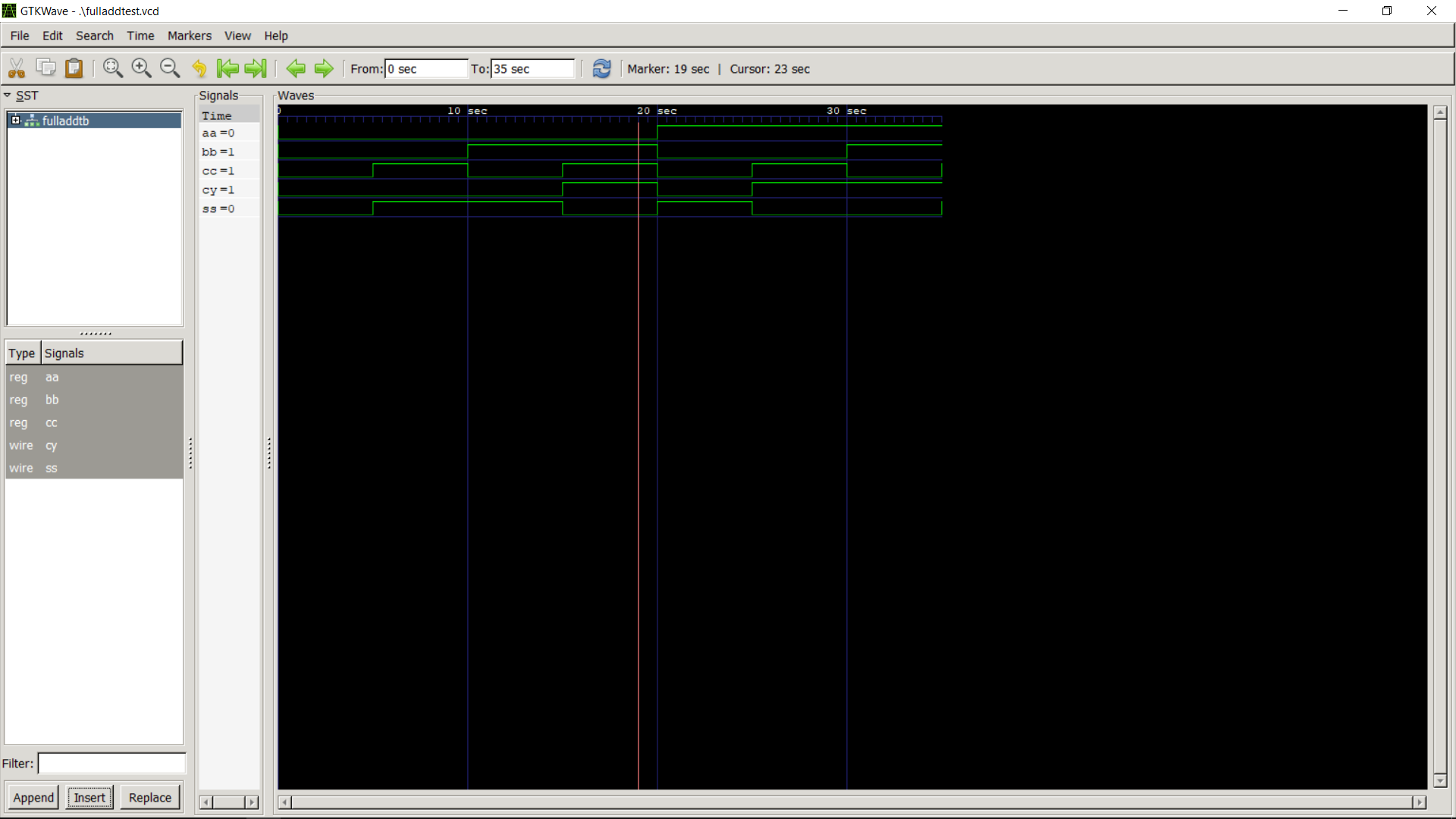


Full Adder:









Ripple Adder:

