**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:25-8-2025

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| --- | --- | --- |
| Name: | SRN: | Section |

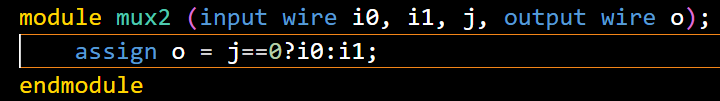
Week Number: 4 Program Number:

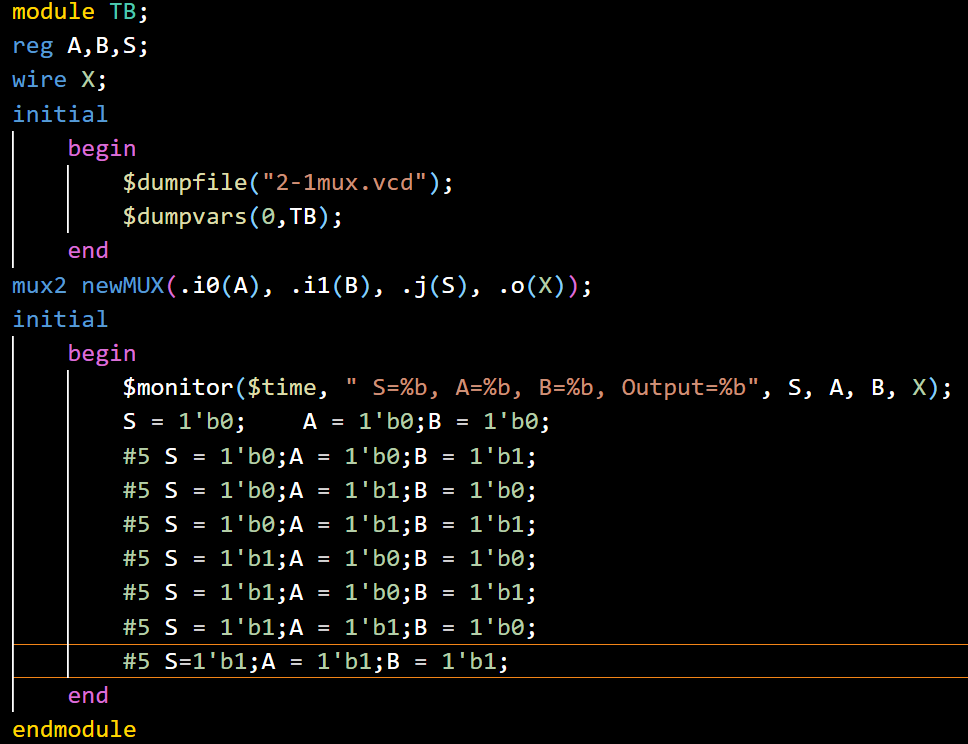
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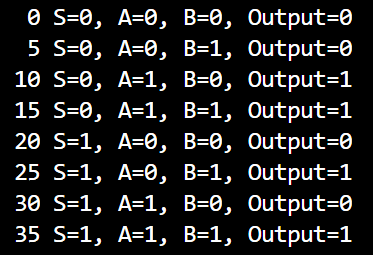
Deliverables

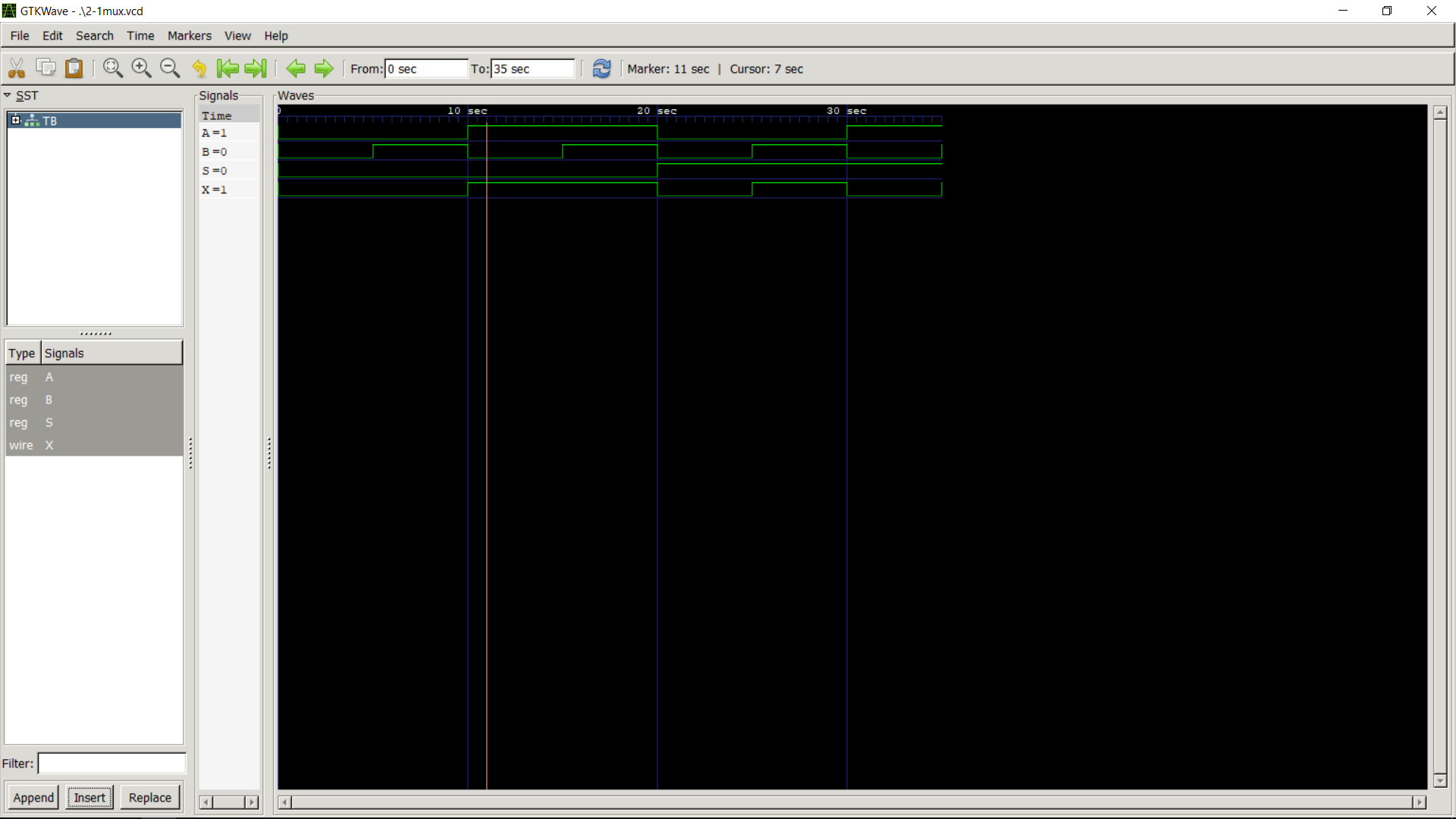
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

2:1 Mux:

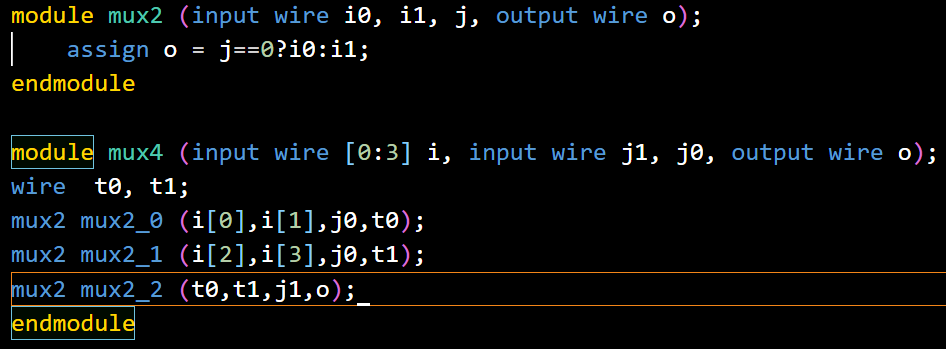


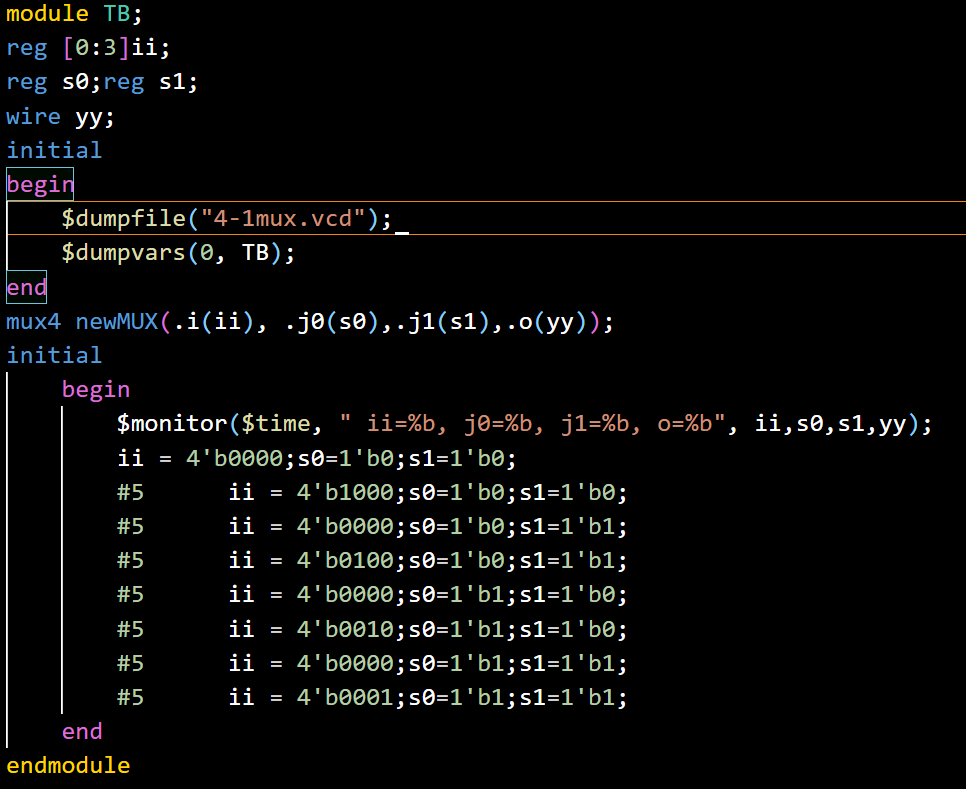


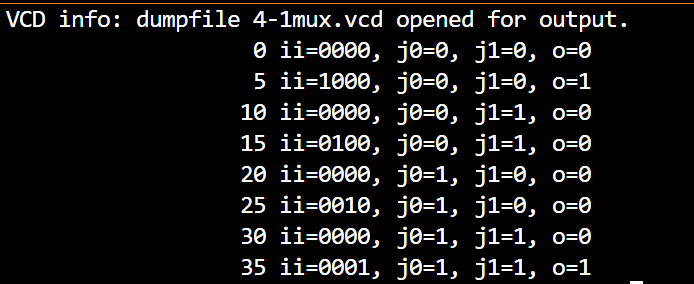


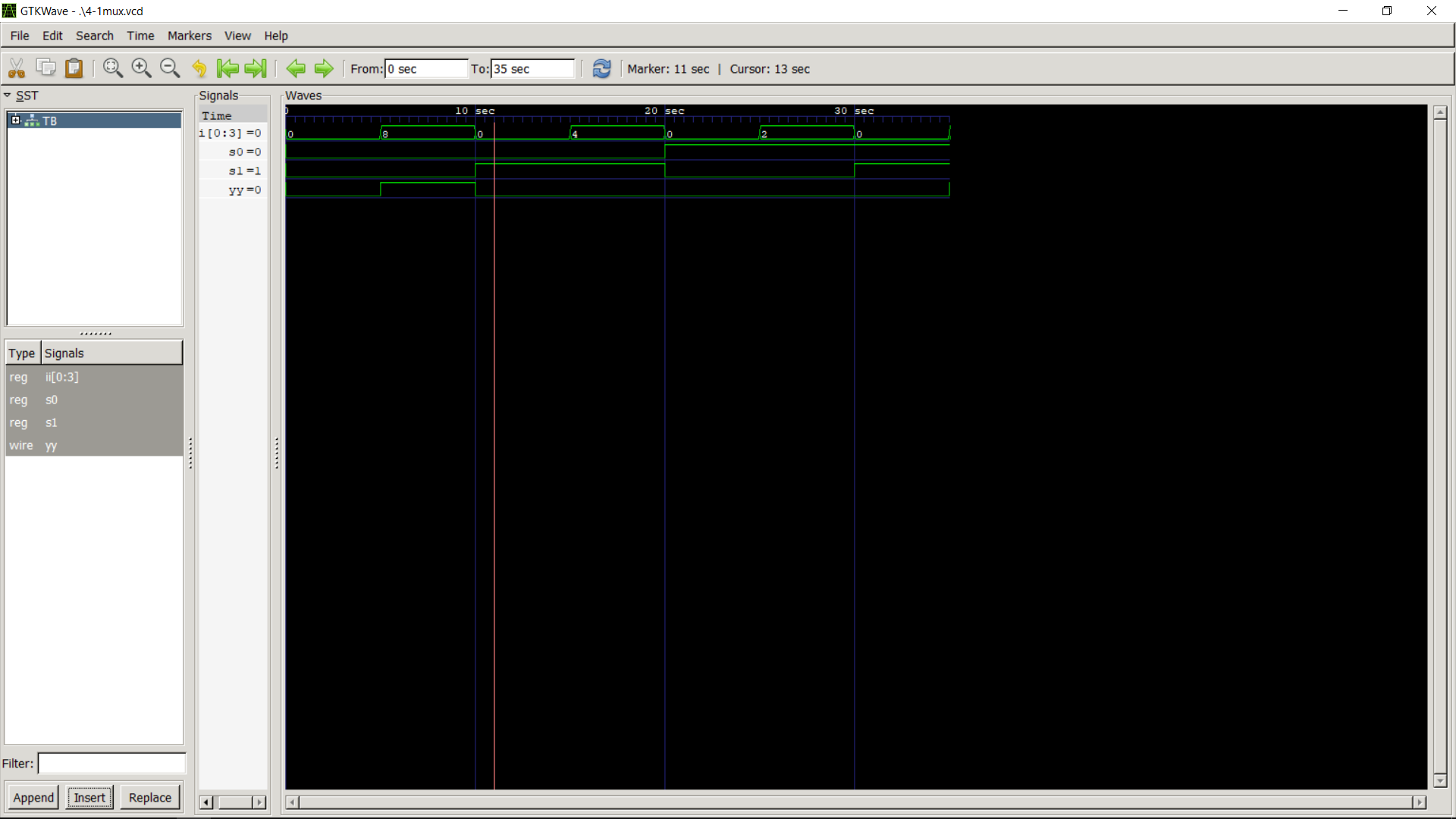


4:1 Mux:









2:1 Demux:

