**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date: 8-9-2025

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| --- | --- | --- |
| Name: | SRN: | Section |

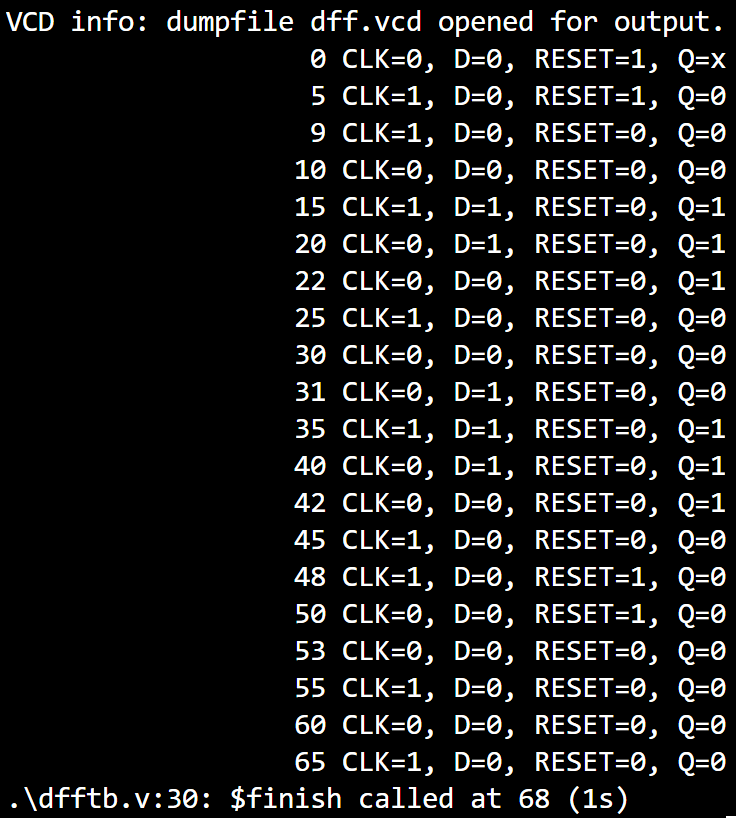
Week Number: 5 Program Number:

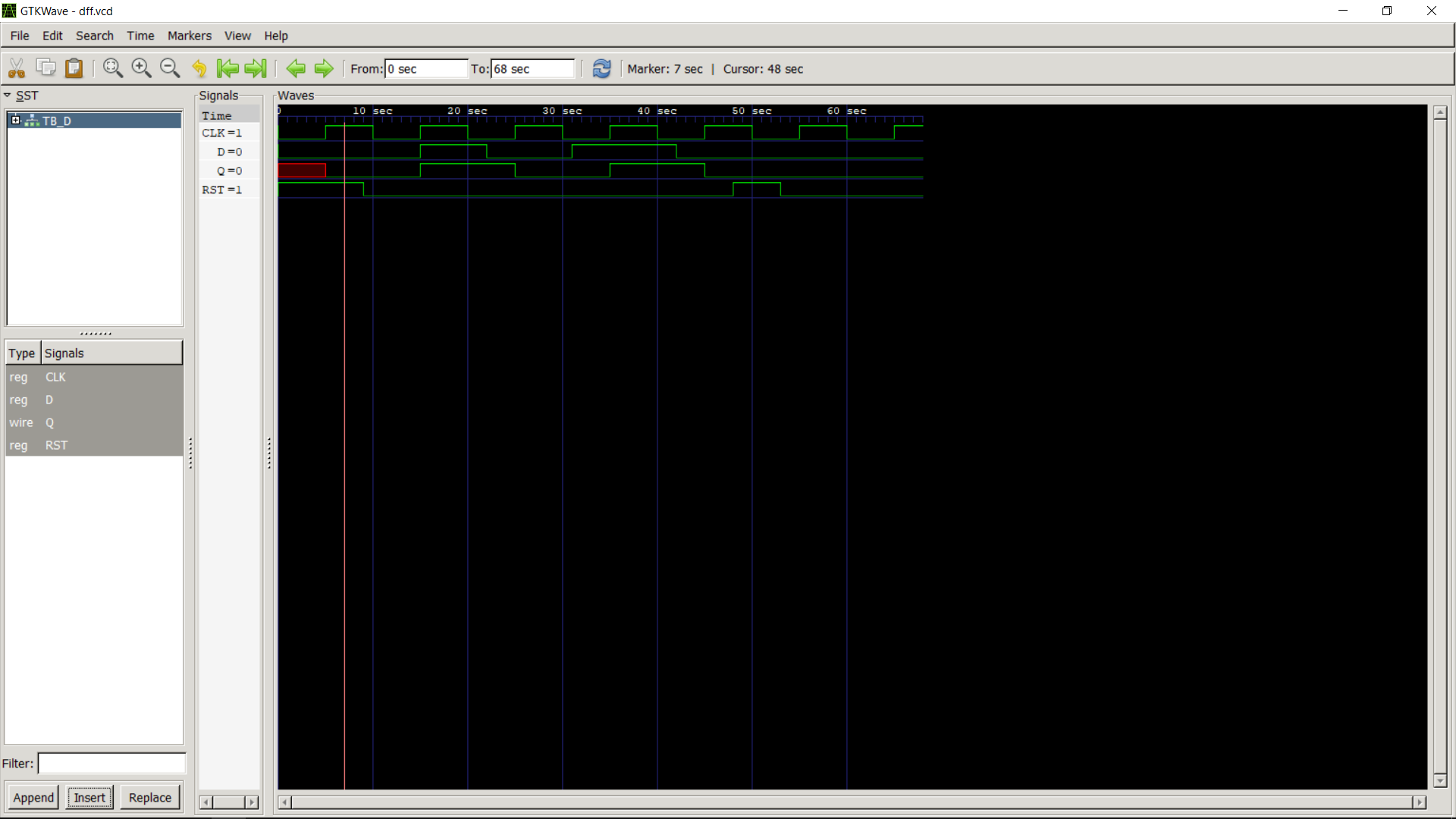
TITLE:

Deliverables

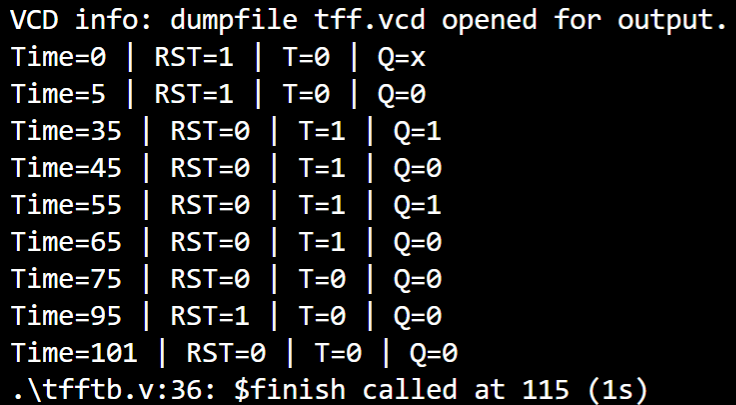
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

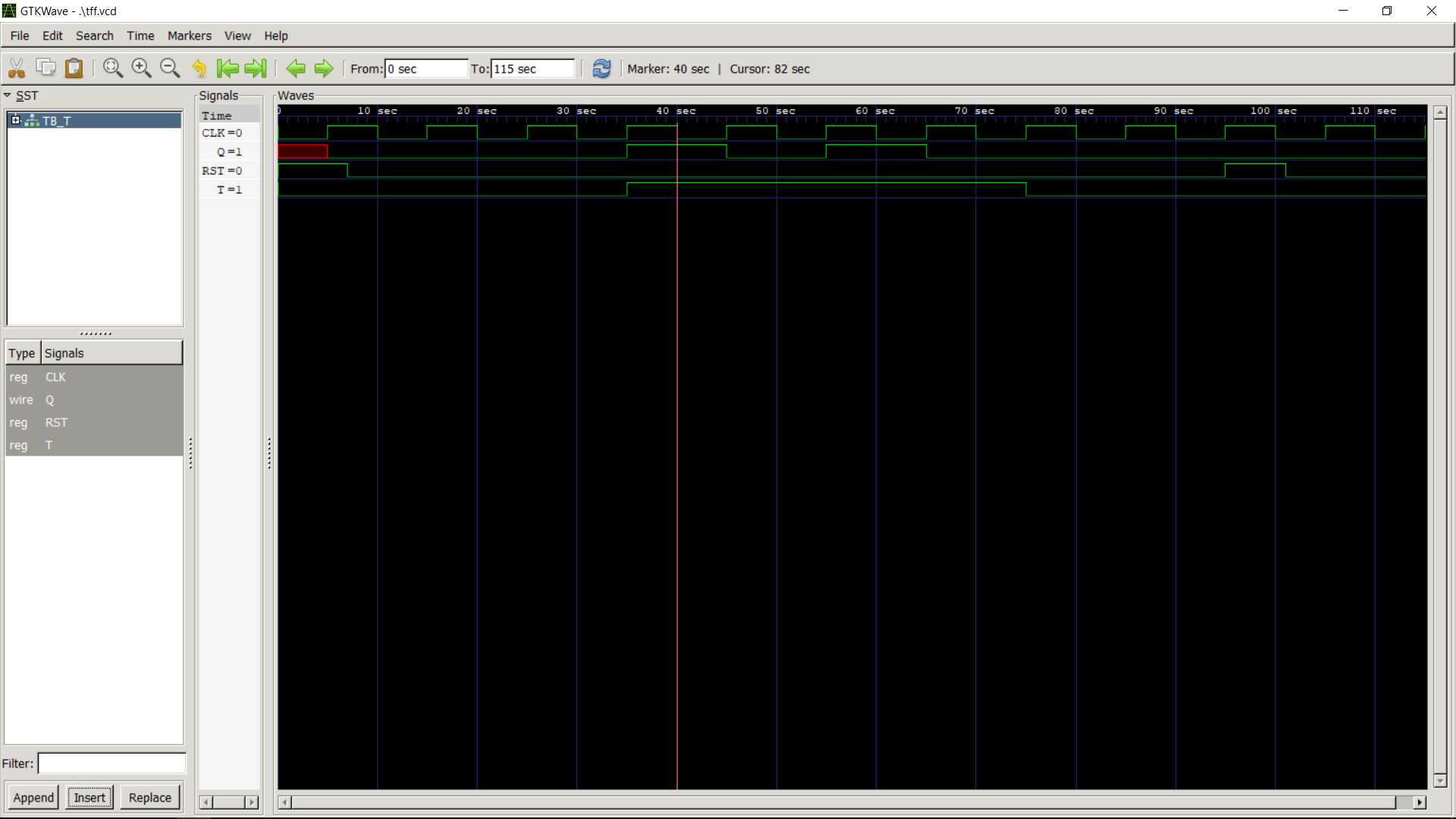
D Flip Flop:





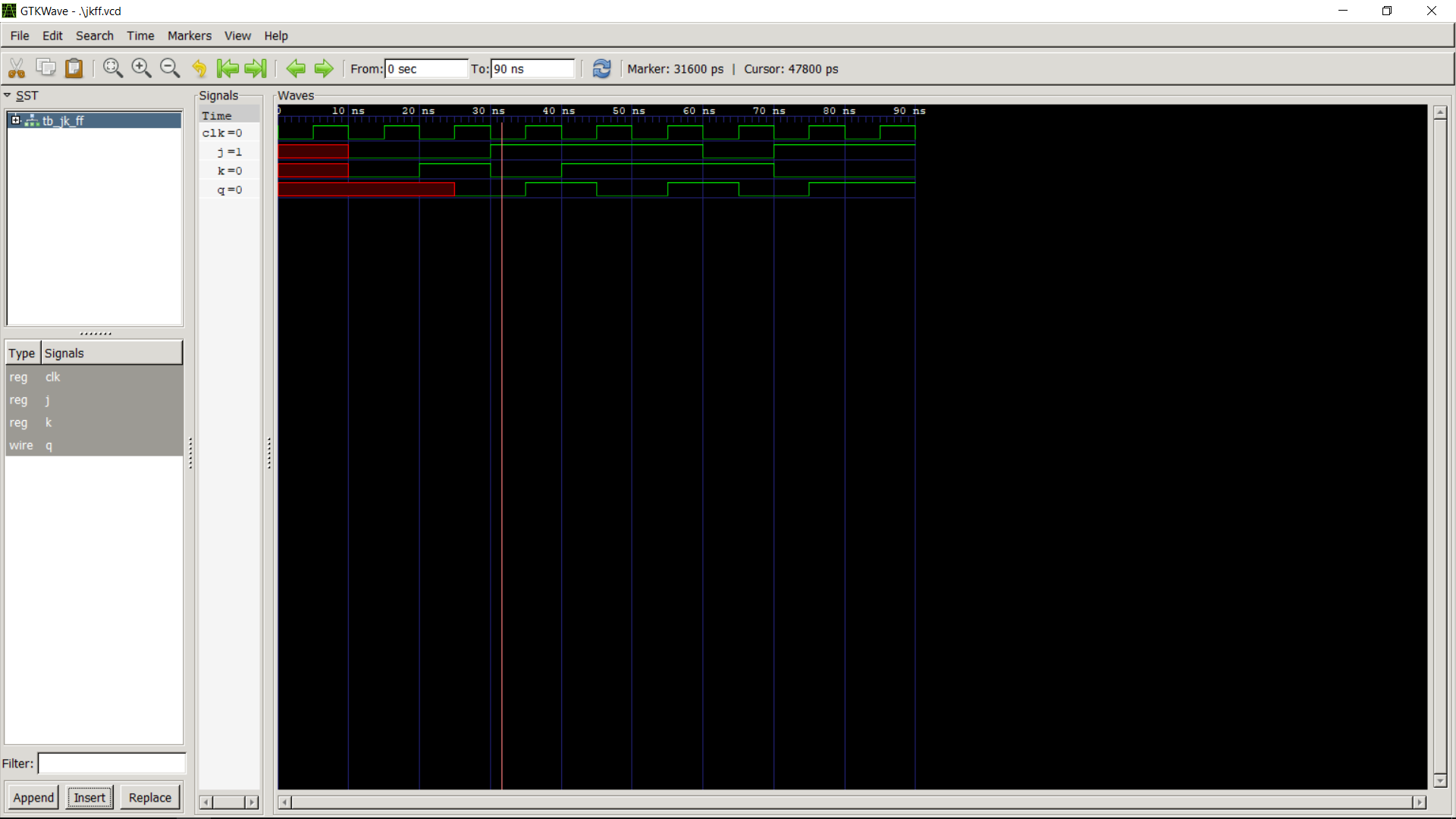
T Flip Flop:



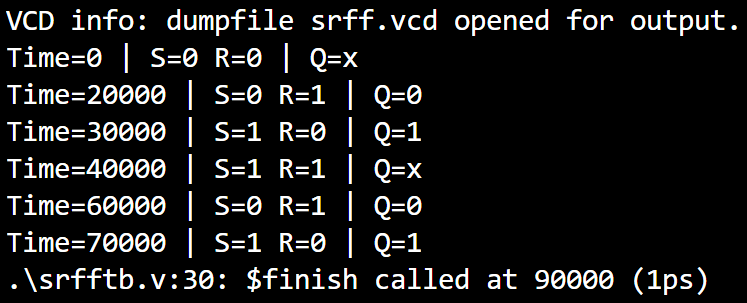


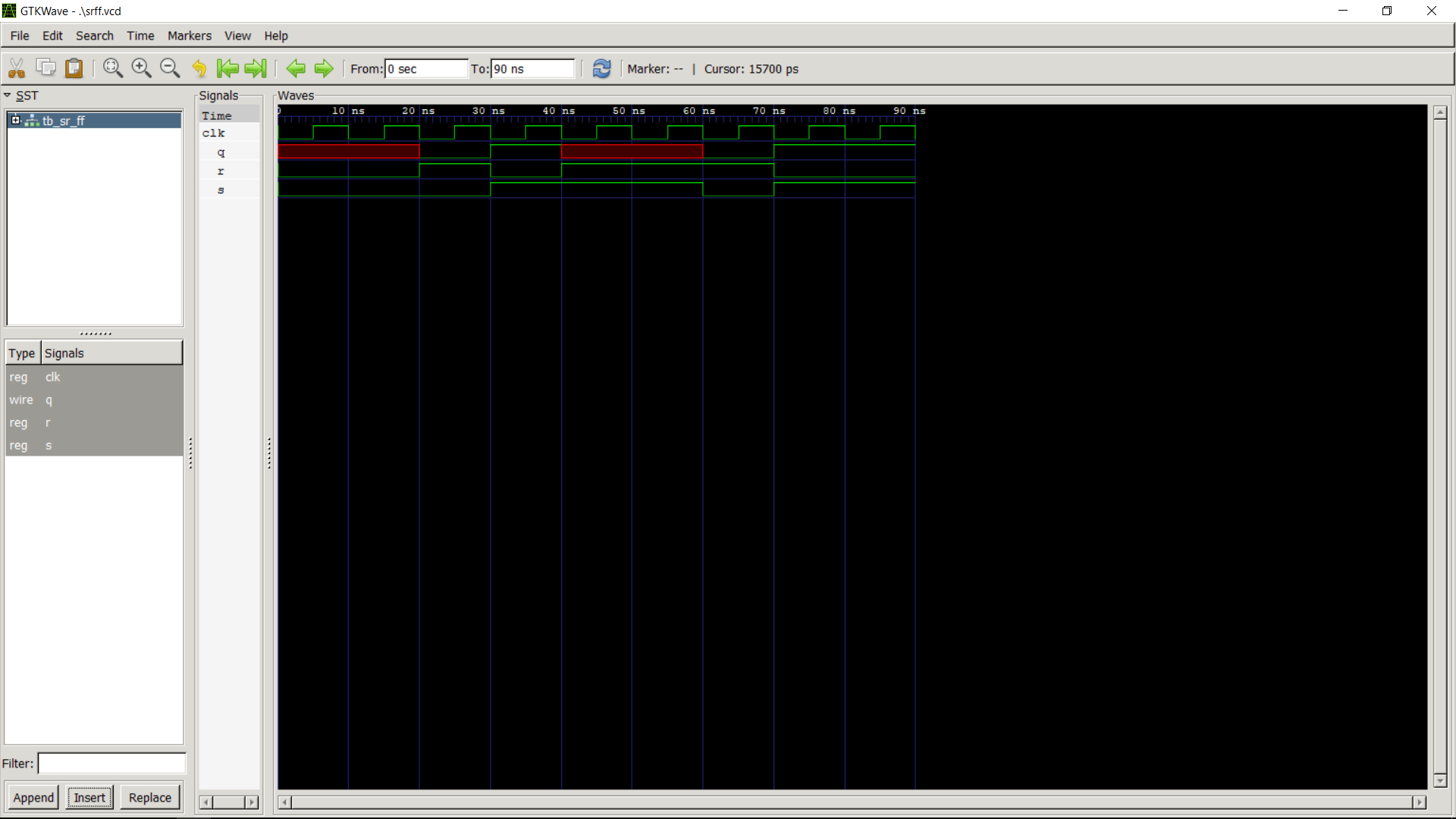
JK Flip Flop:





SR Flip Flop:





T Flip Flop to D Flip Flop:

