**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:29-9-2025

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| --- | --- | --- |
| Name: | SRN: | Section |

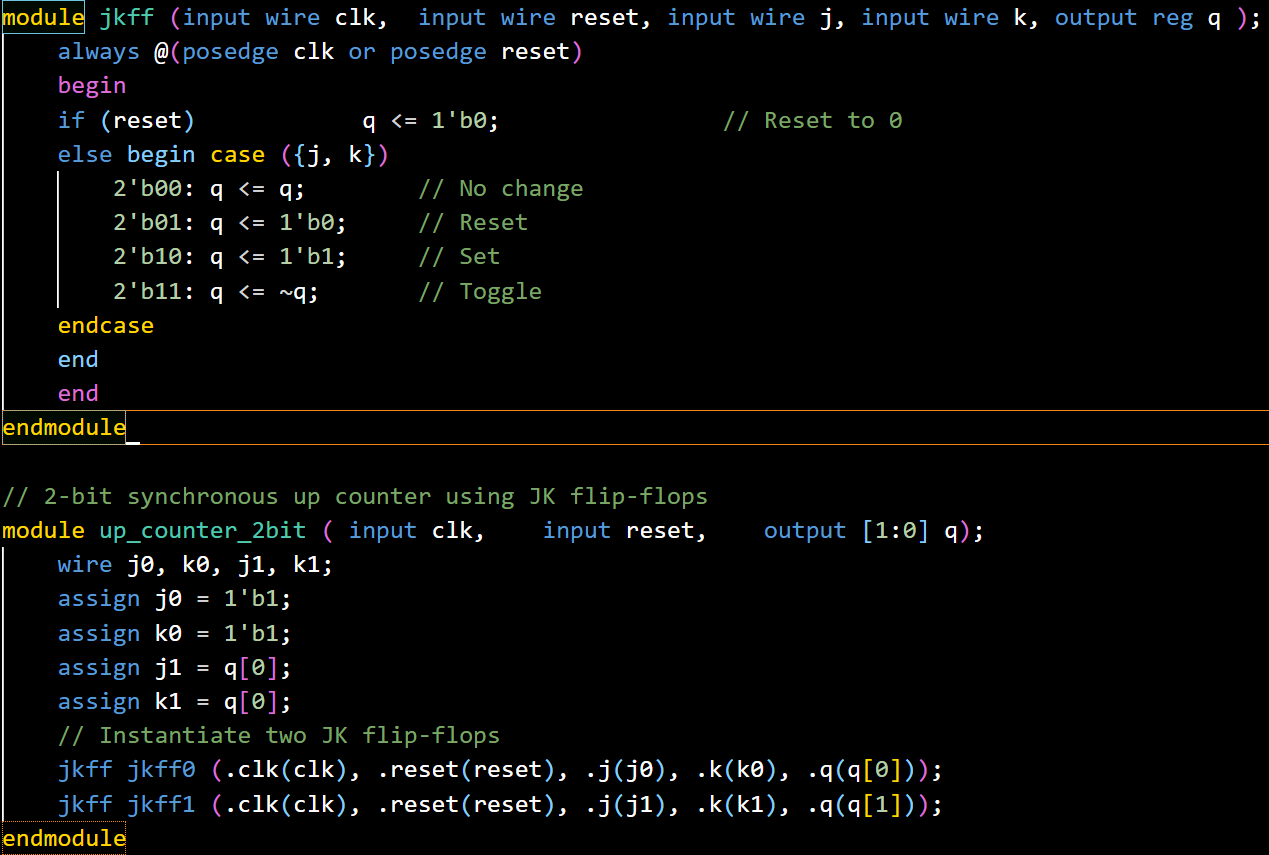
Week Number: 6 Program Number:

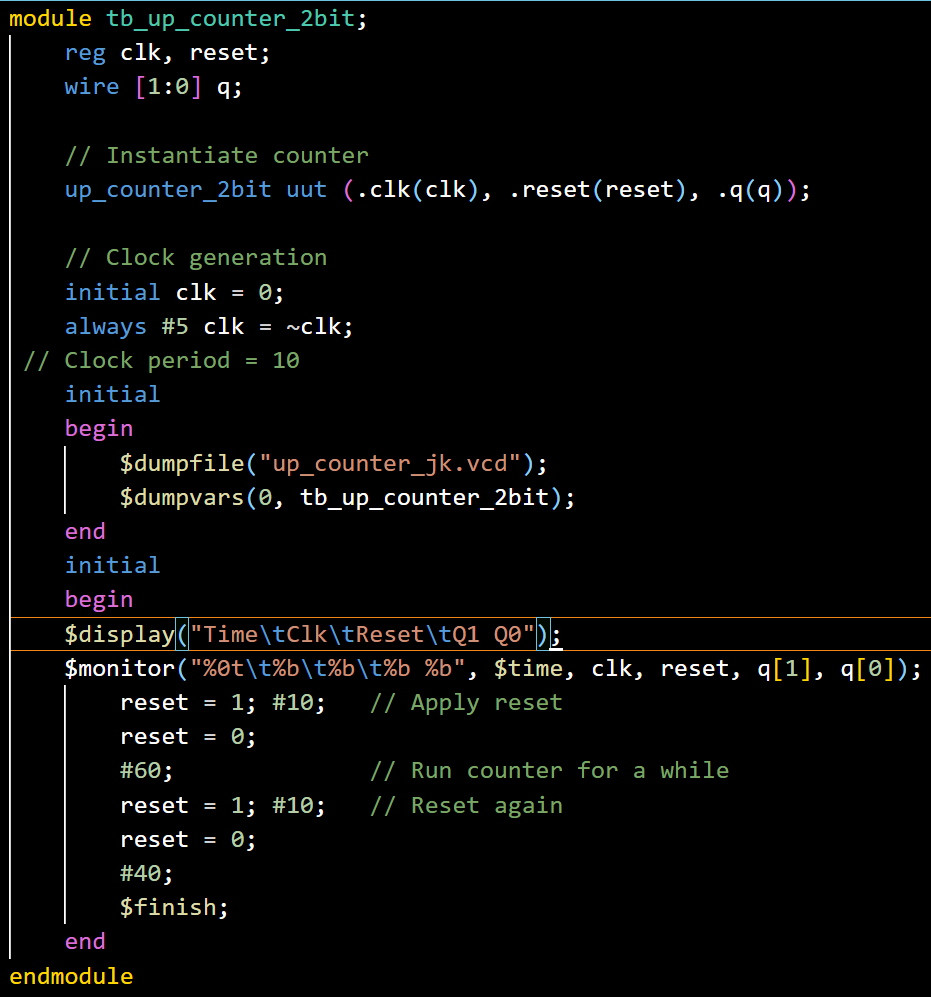
TITLE:

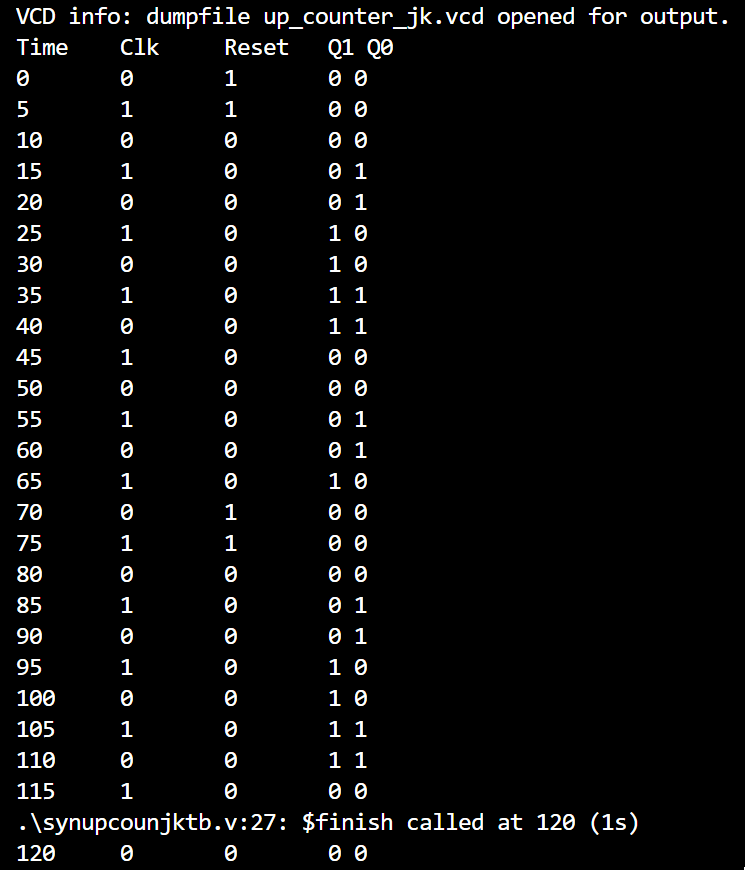
Deliverables

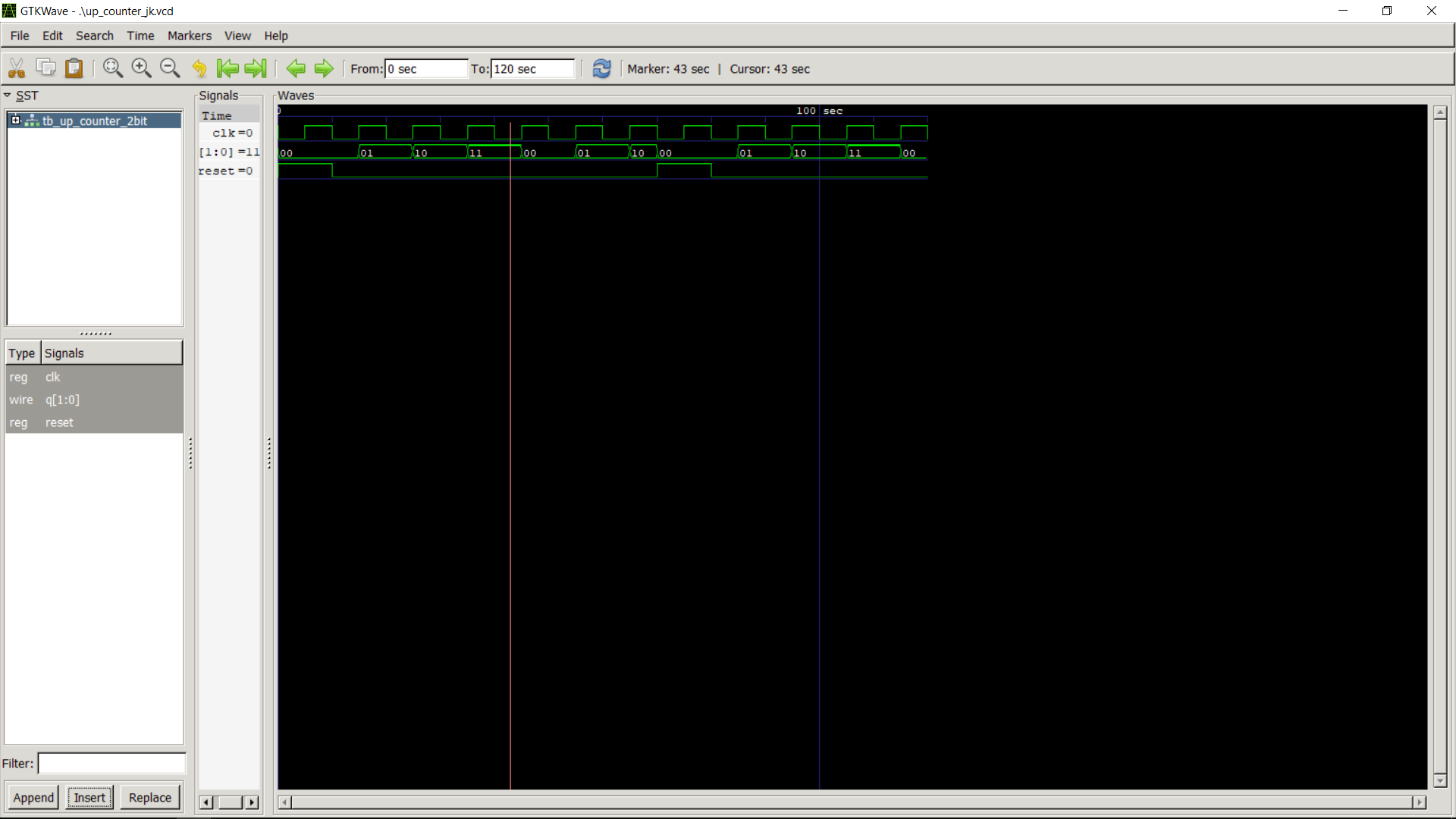
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

2-bit Up Counter JK:

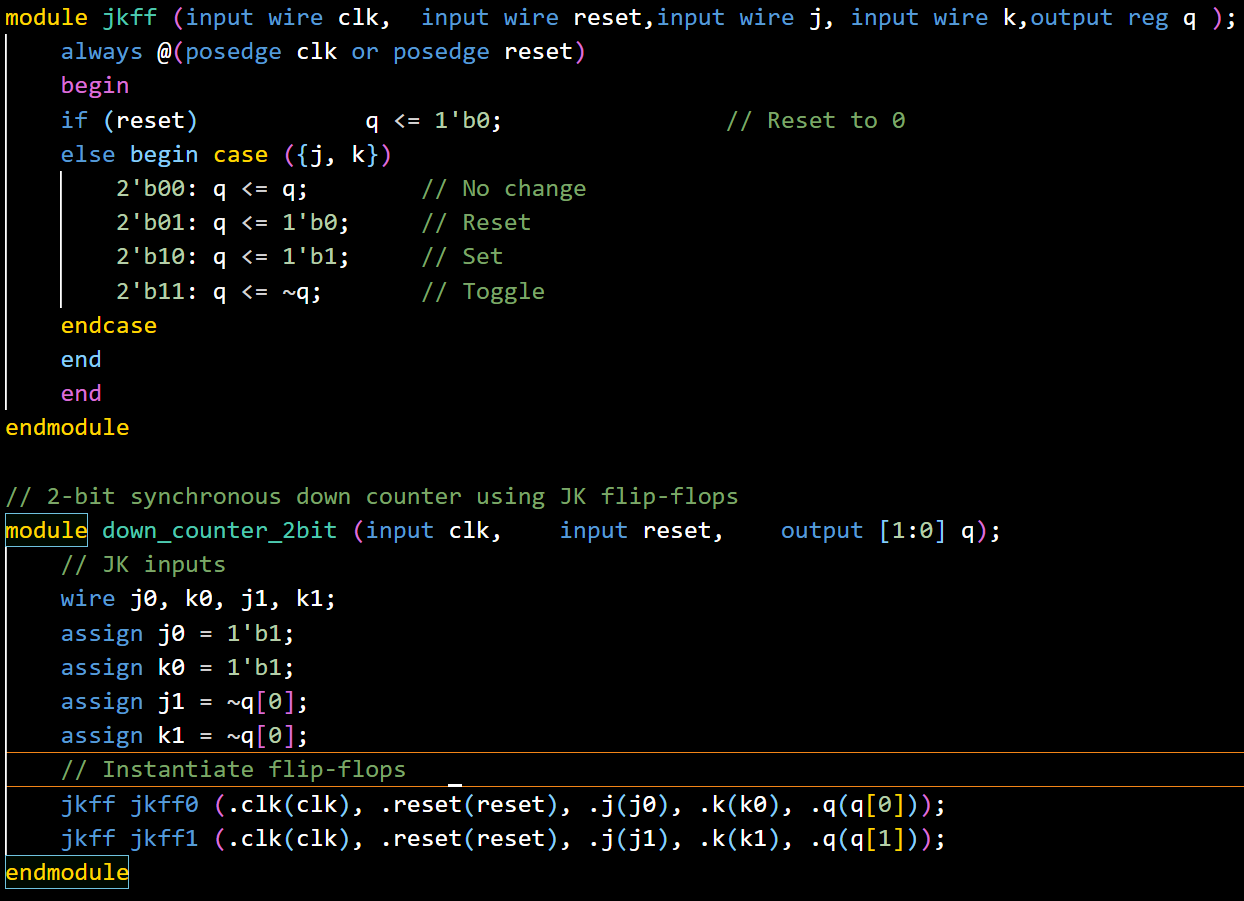


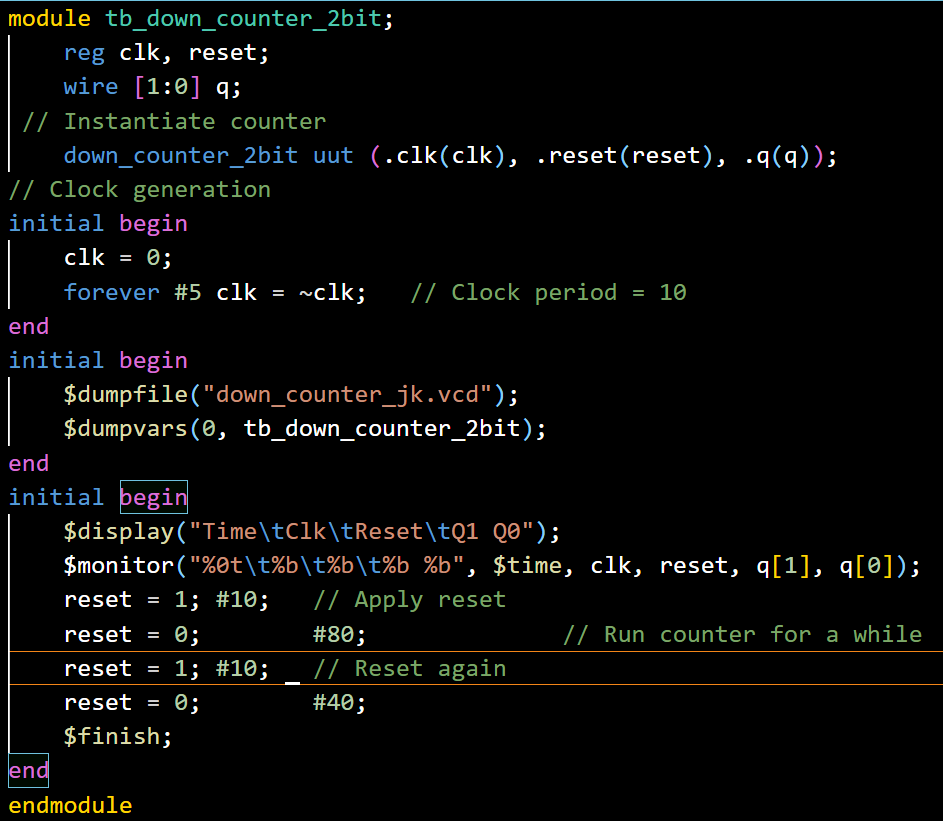


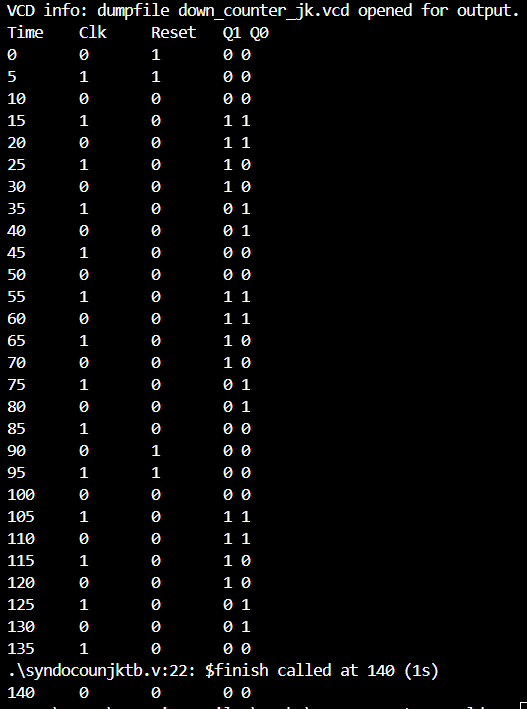


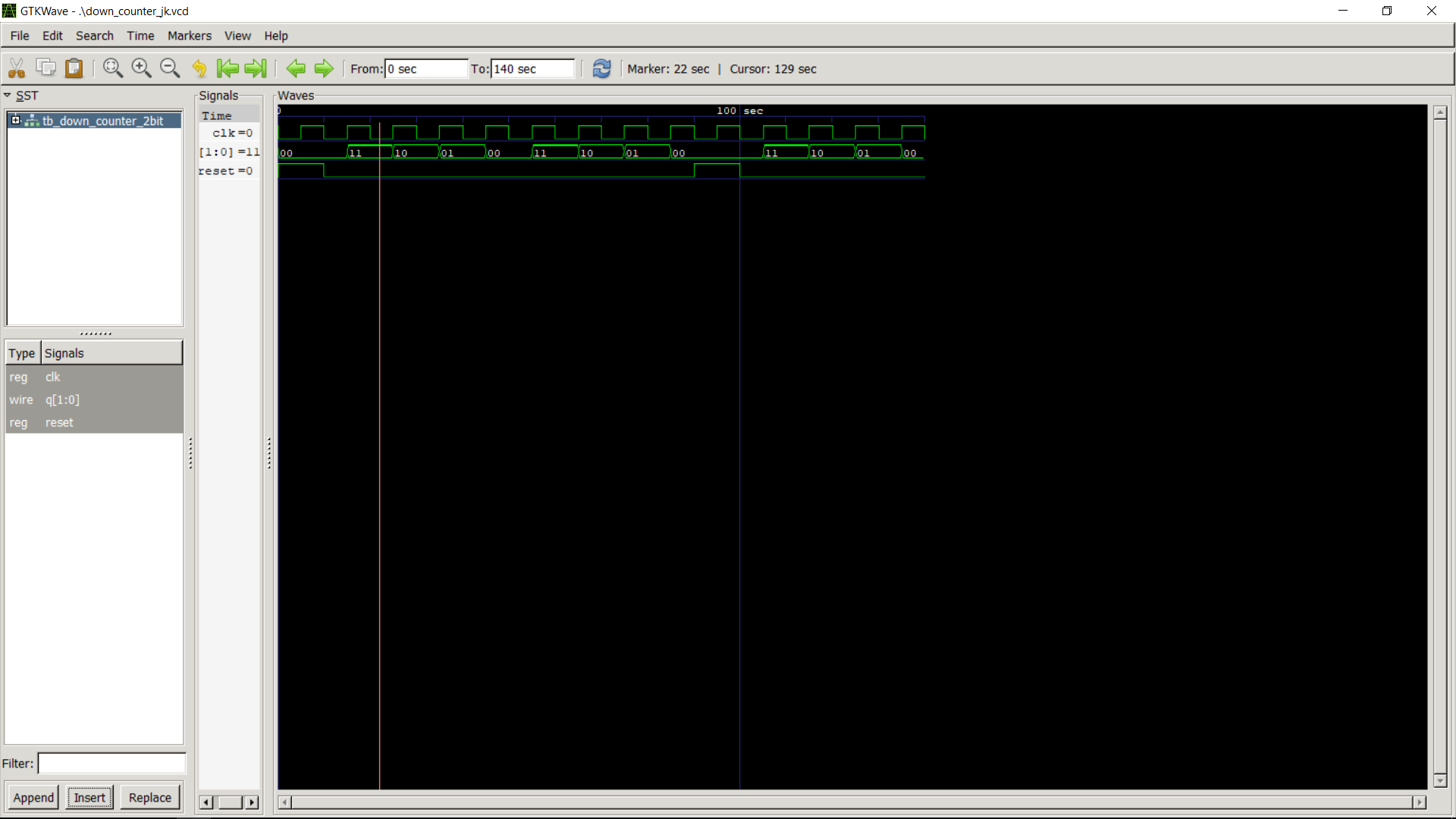


2-bit Down Counter JK:

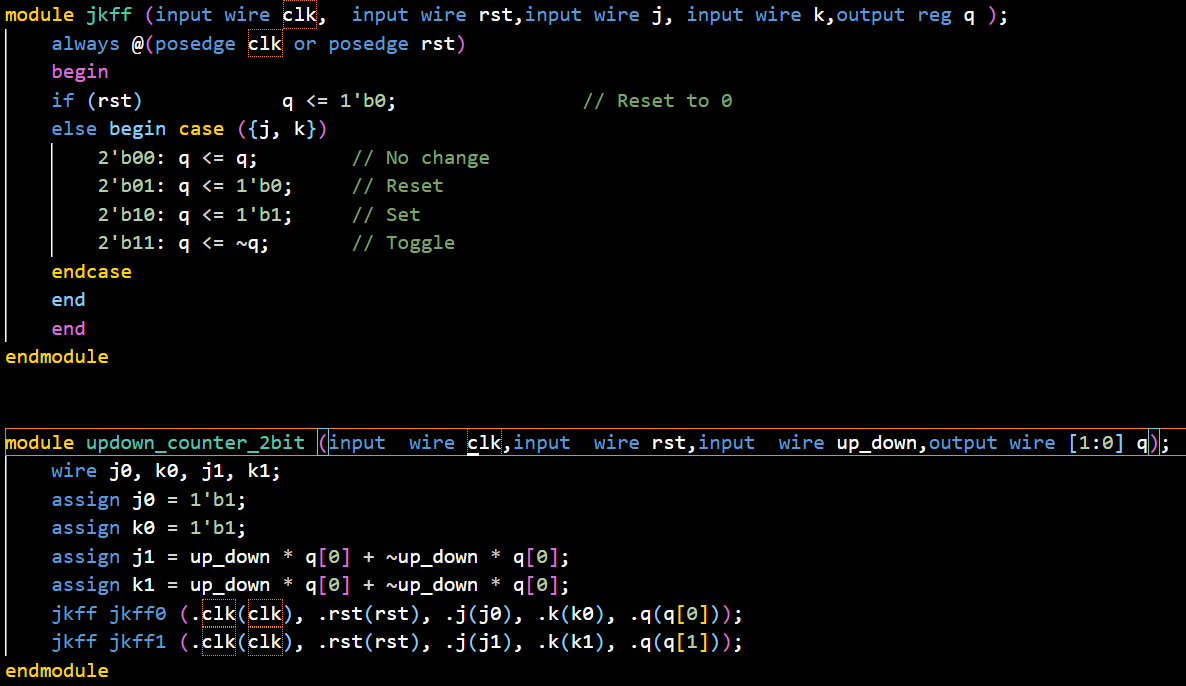


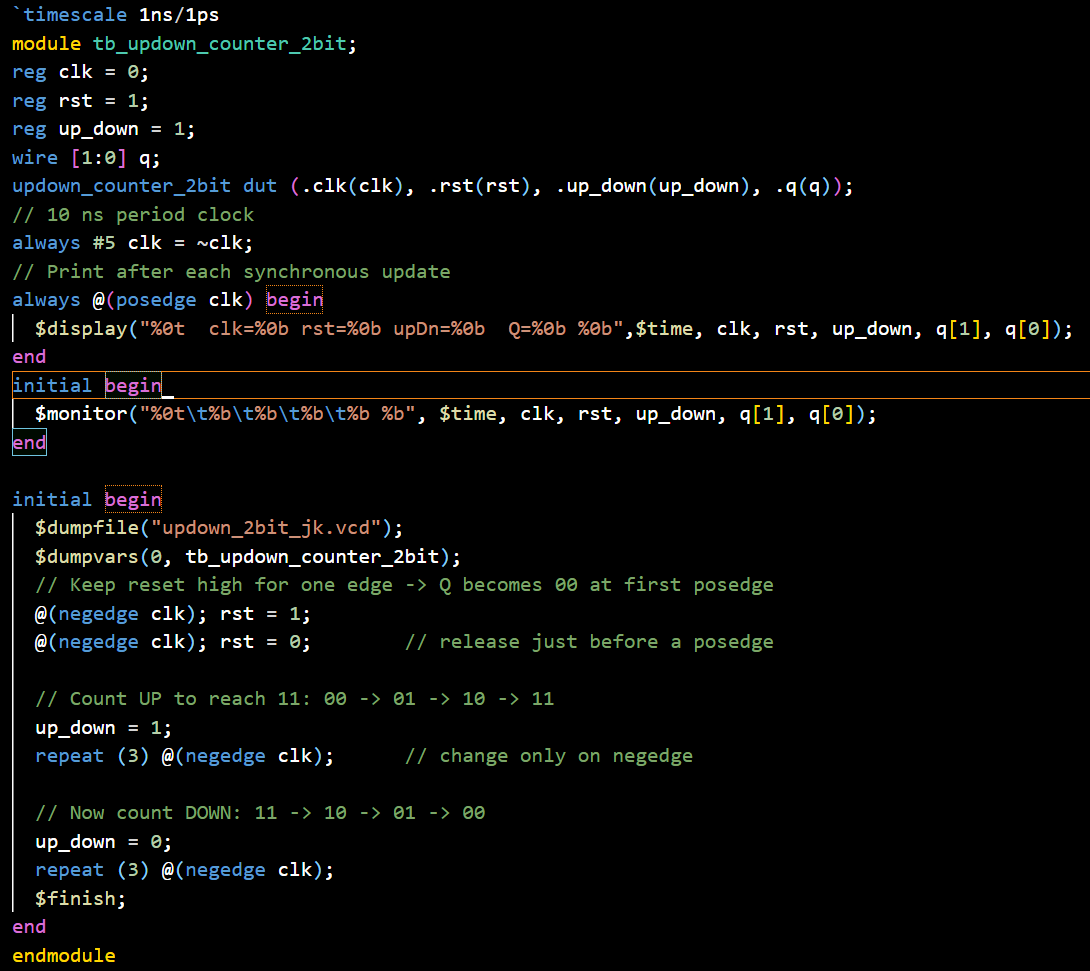


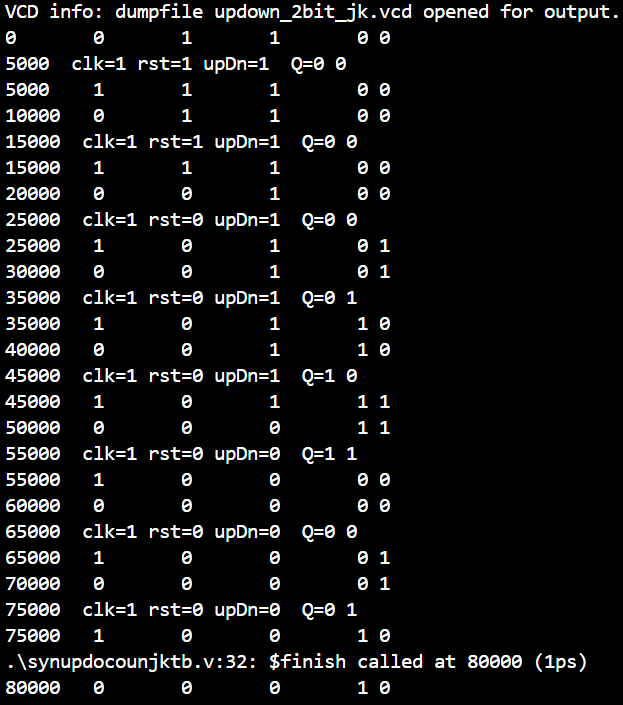


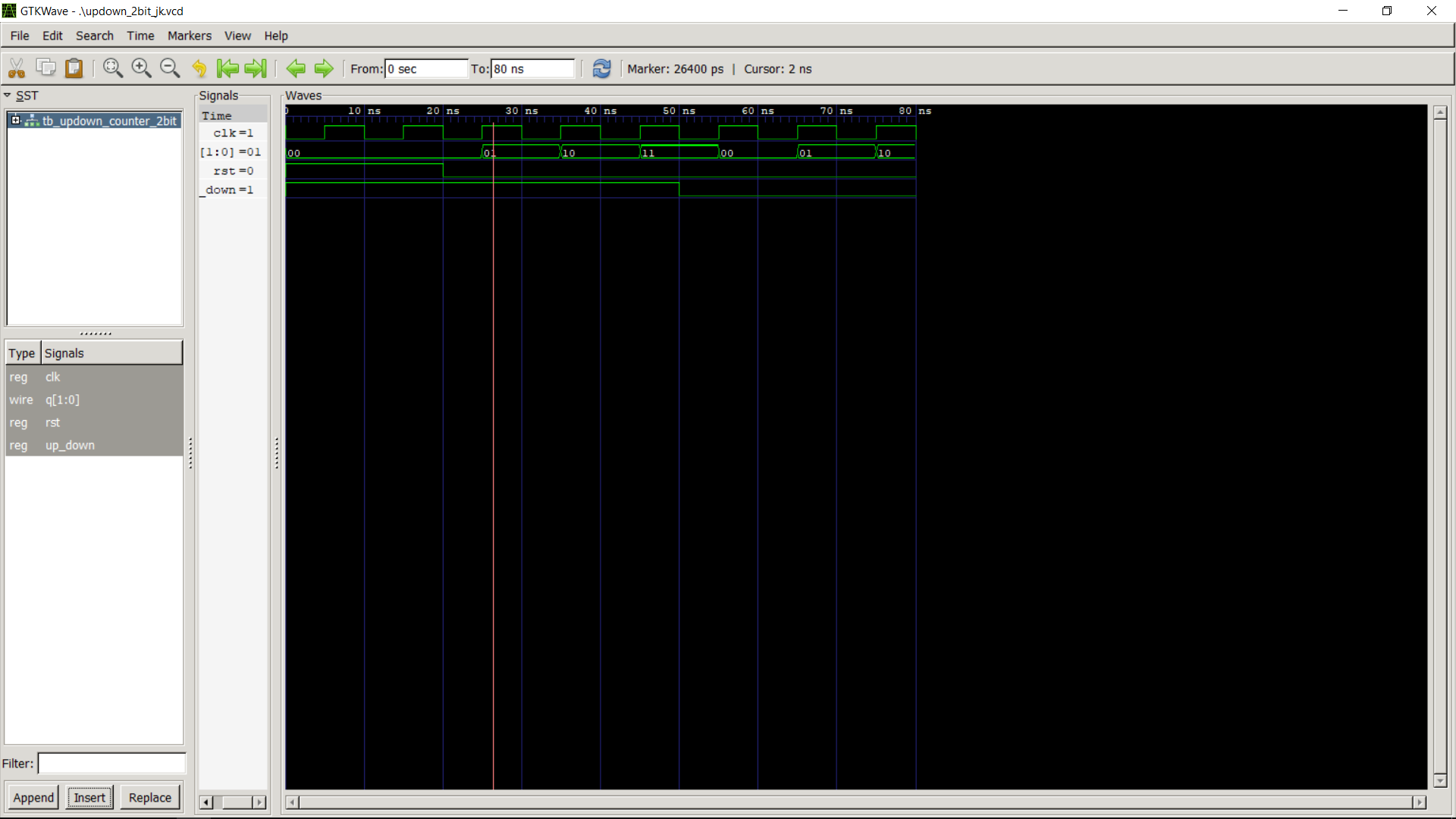


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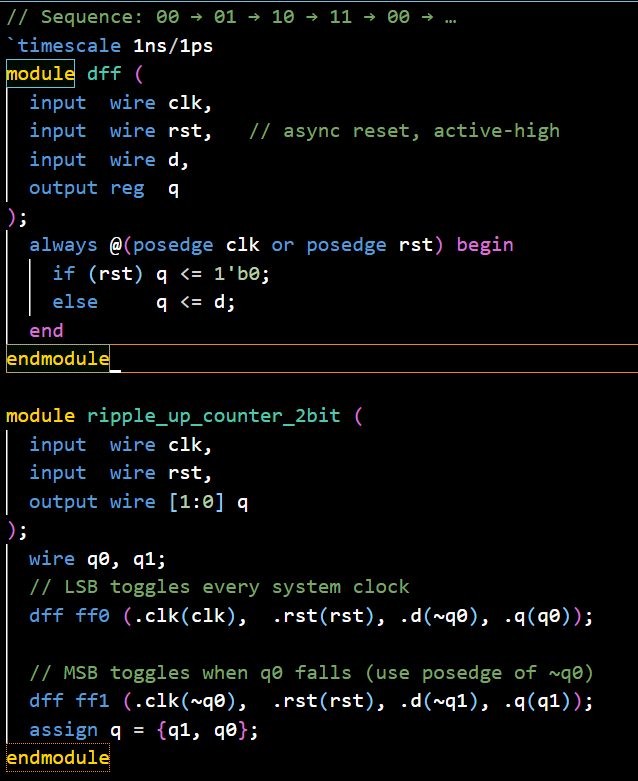


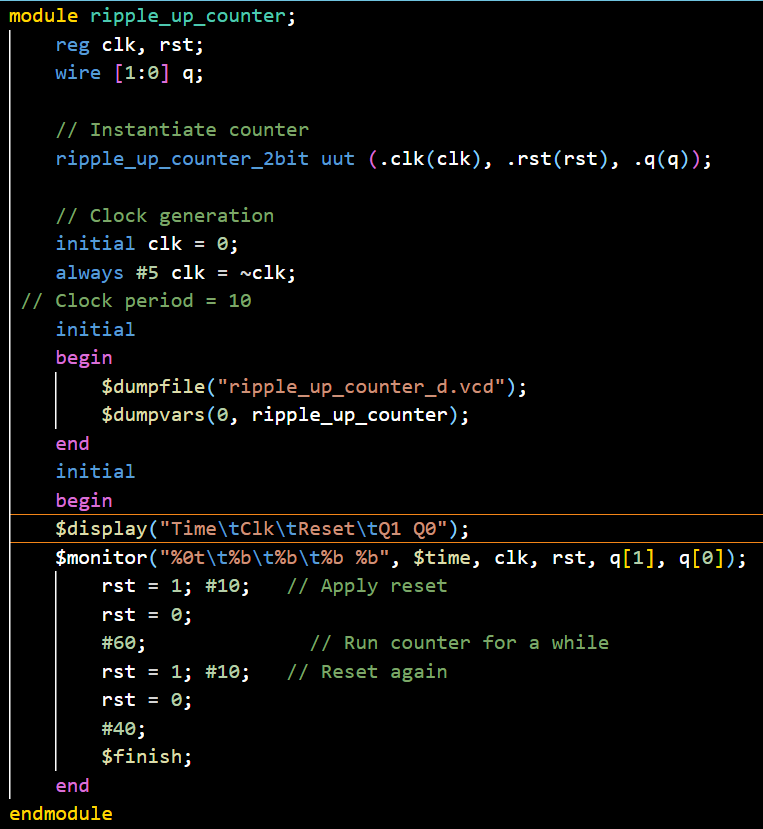


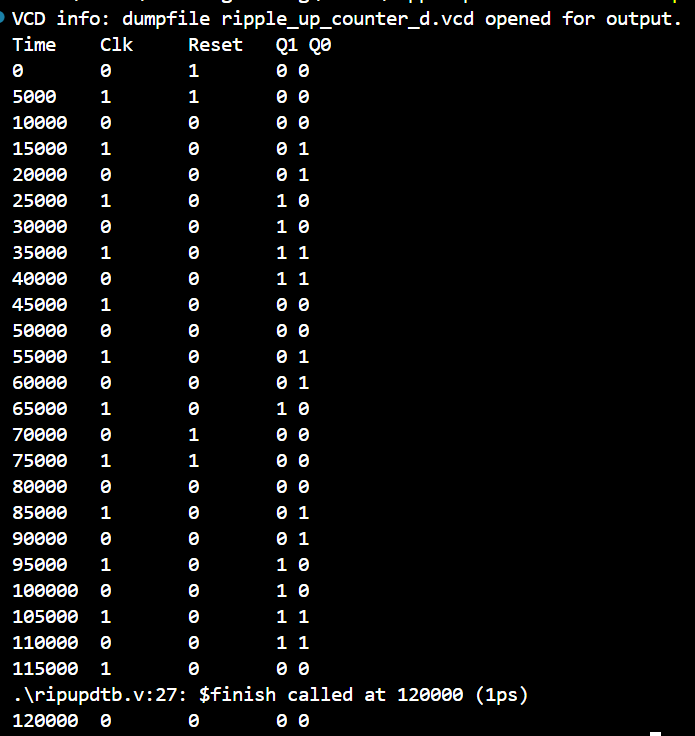


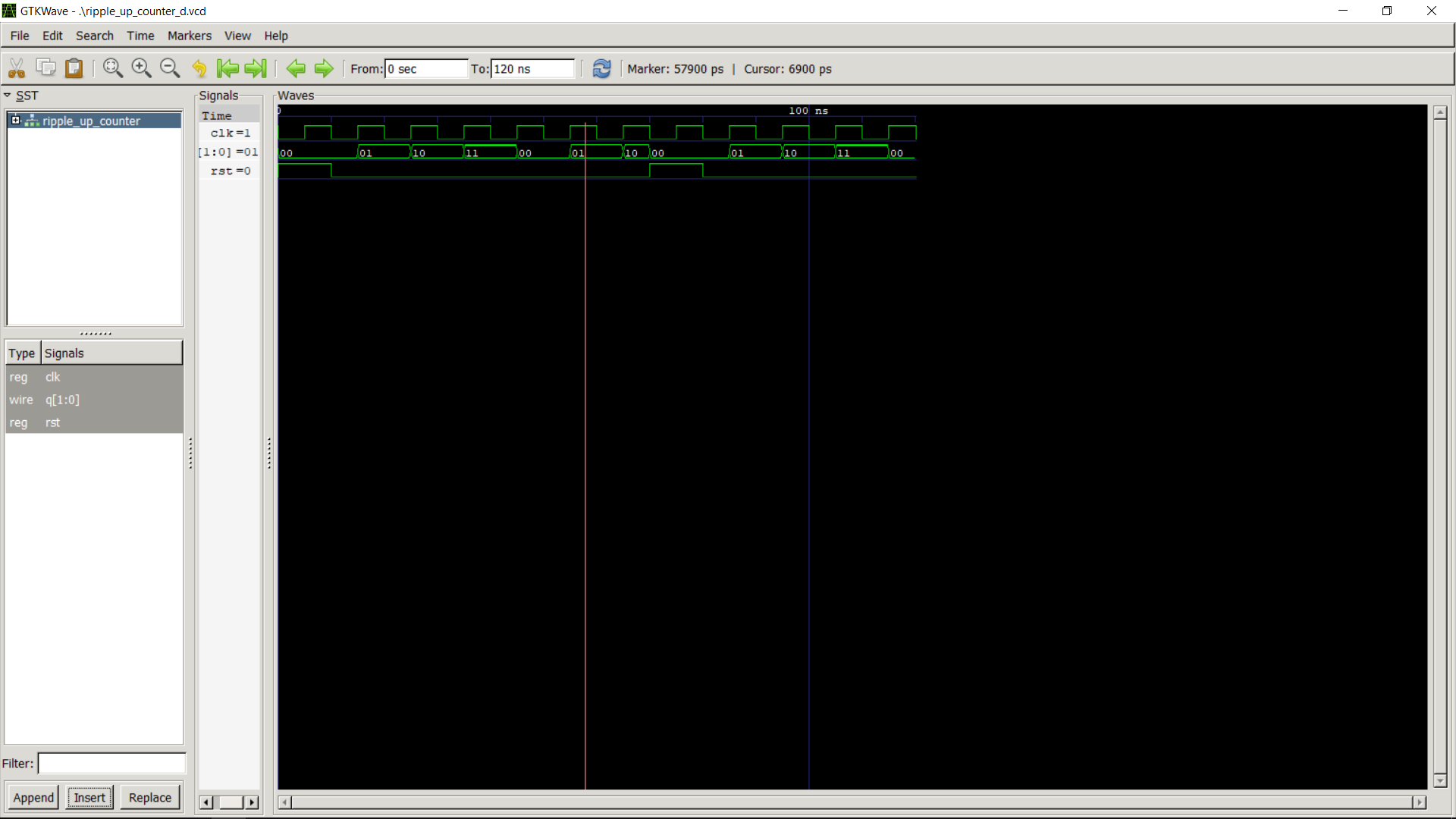


2-Bit Ripple Up Counter using DFF:

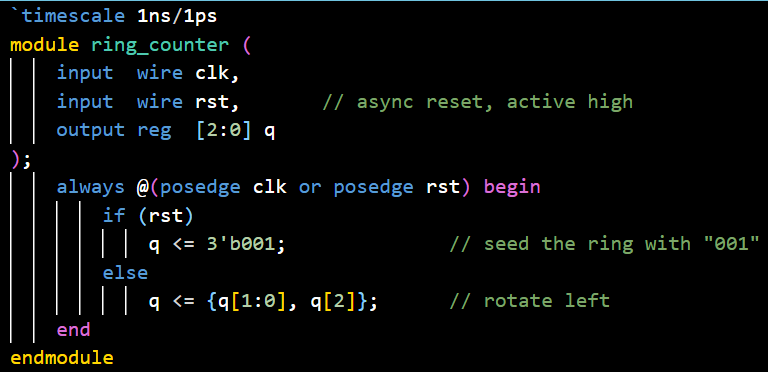


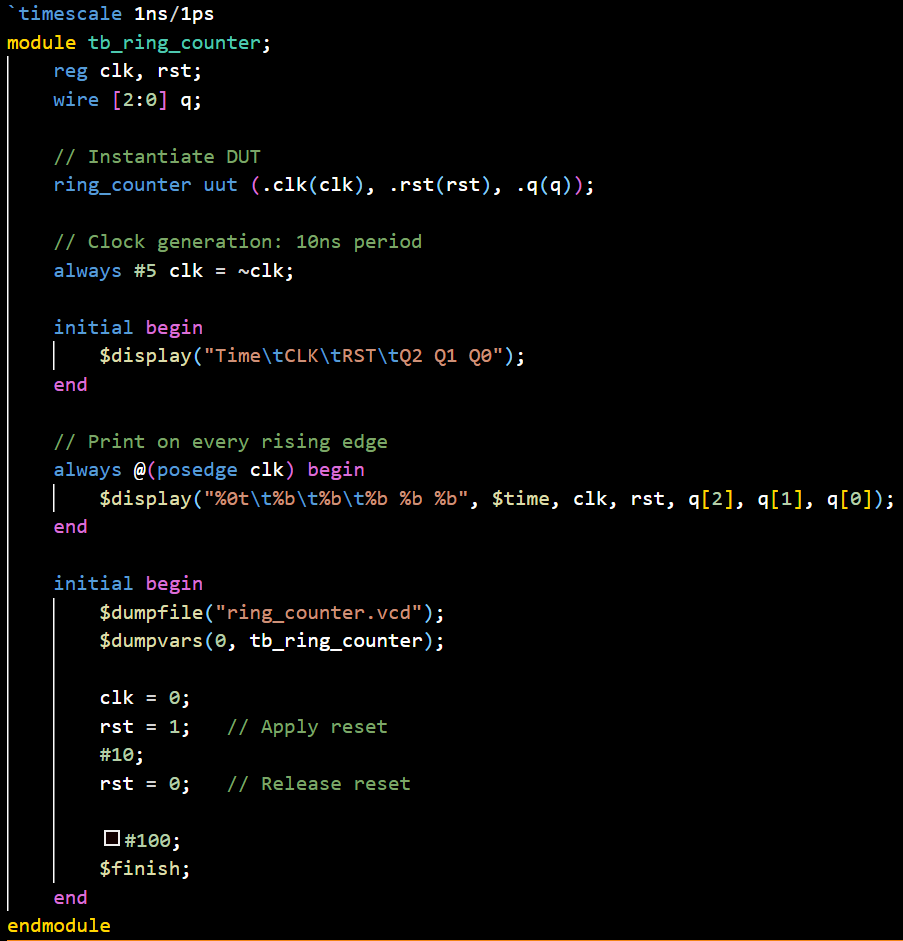


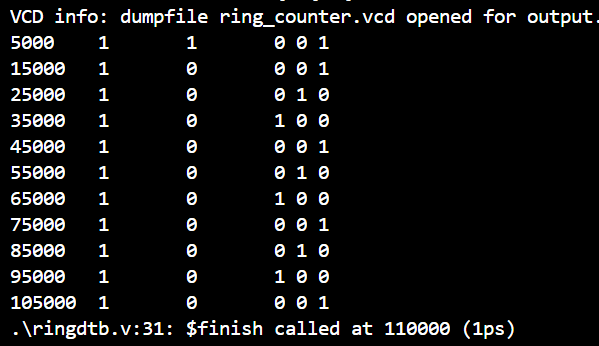


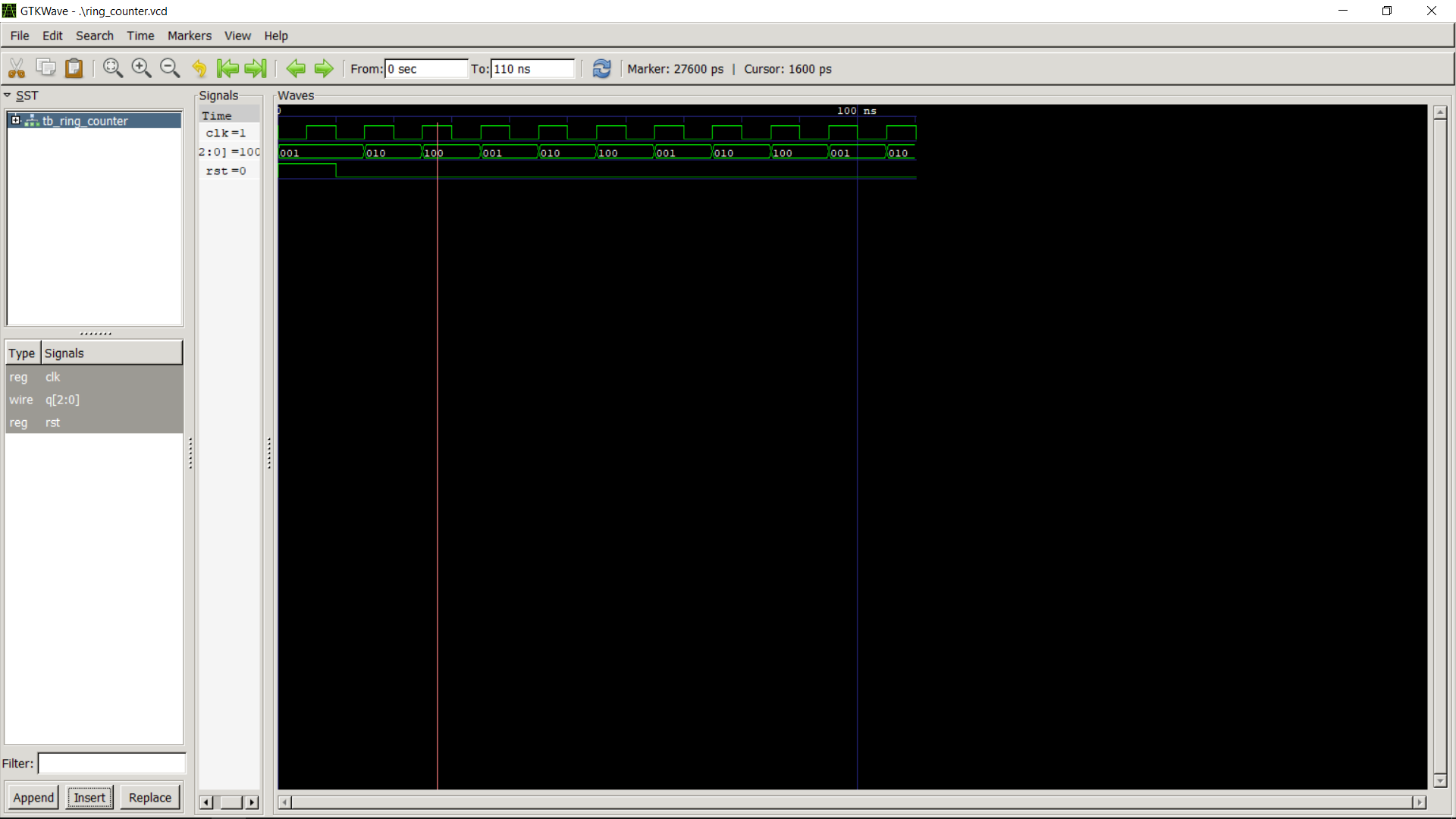


3 bit Ring Counter:









3 bit Johnson Counter:

