**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:13-10-2025

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| --- | --- | --- |
| Name: | SRN: | Section |

Week Number: 8 Program Number:

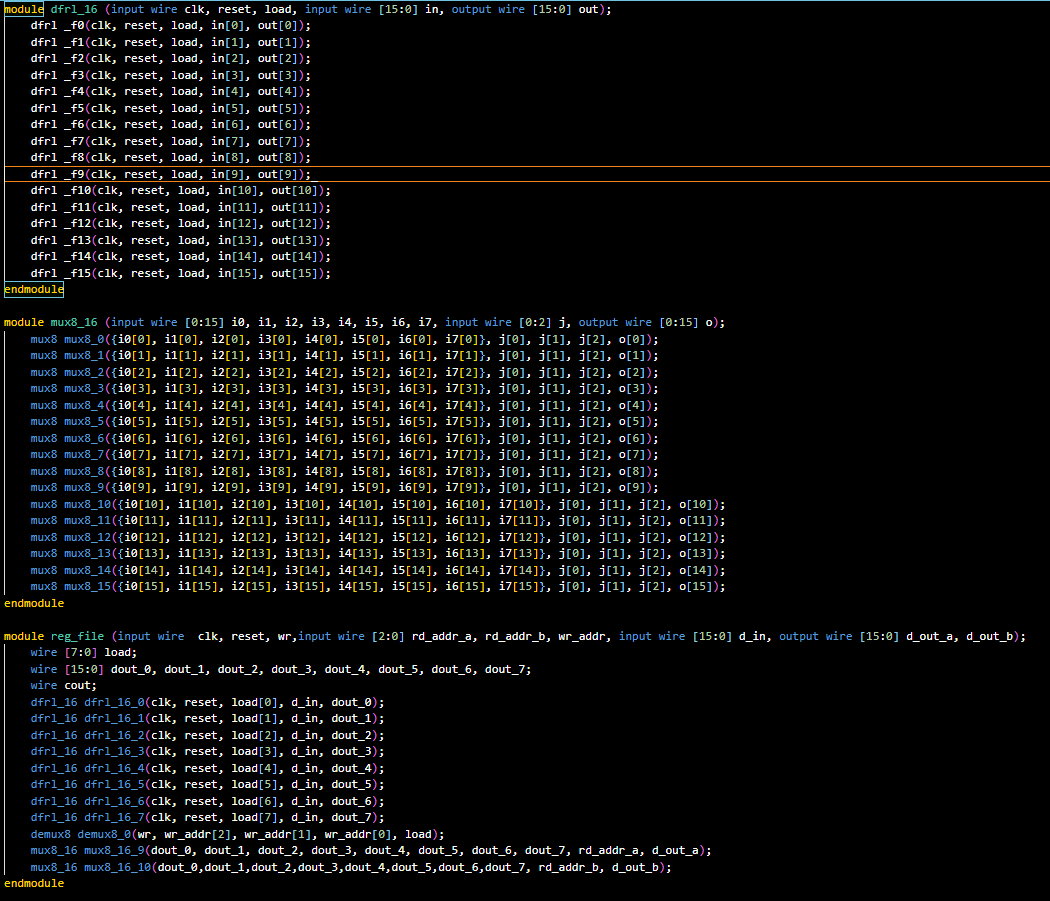
TITLE:Register

Deliverables

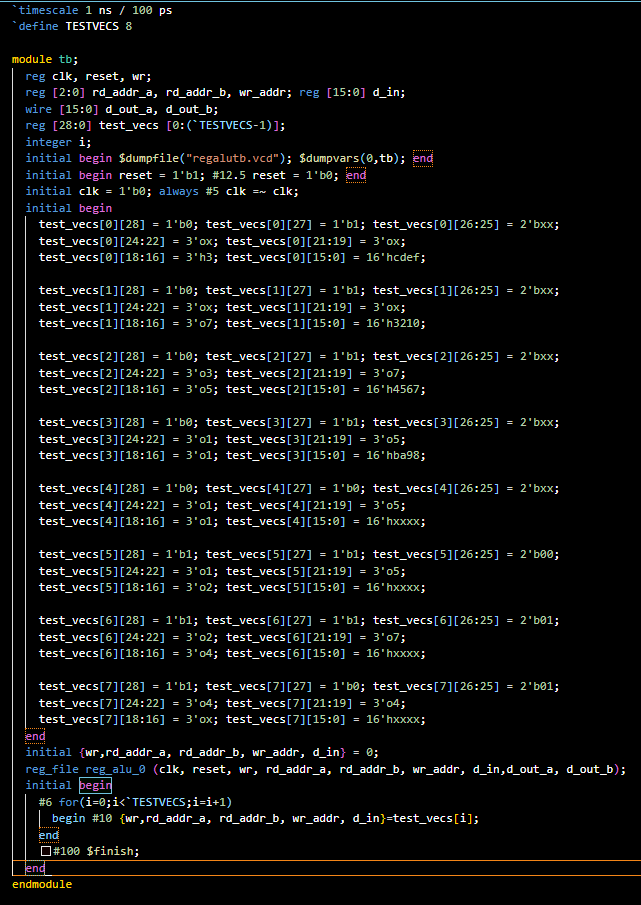
1. Verilog Code Screenshot
2. Verilog VVP Output Screen Shot
3. GTKWAVE Screenshot
4. Output Table to be completed and included

Register:

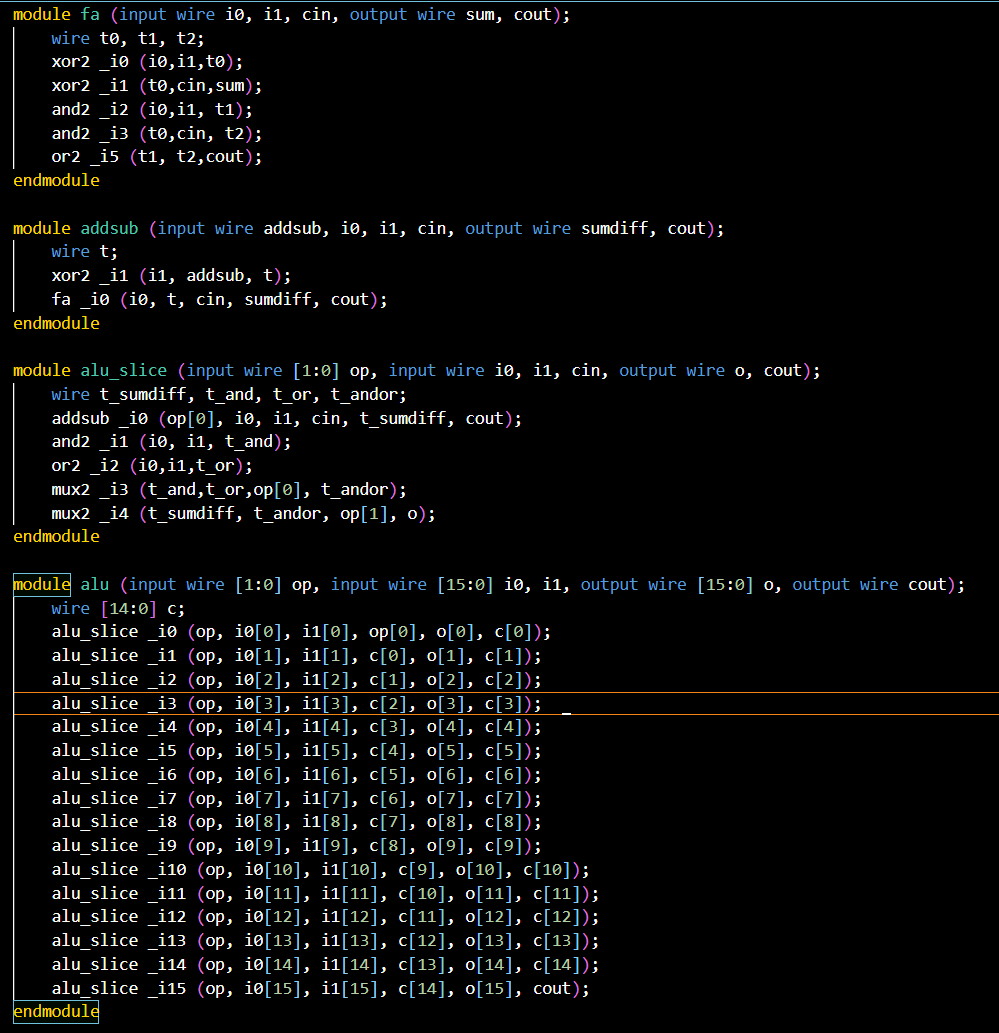
Register.v:



Registertb.v:



ALU.v:



Lib.v:

