Date: 24/02/17

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

Third Year, First Semester Final Examination, Spring 2017

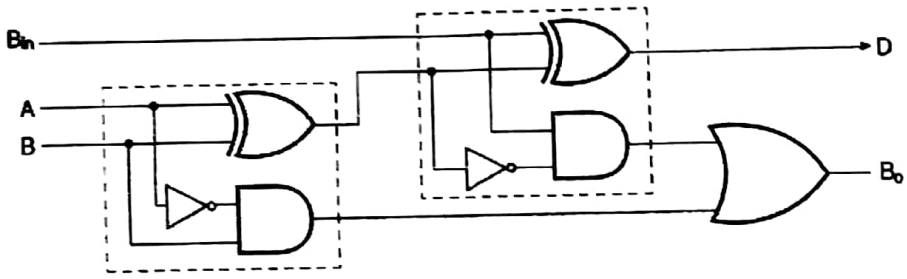
Course No: CSE 3109 Course Title: Digital System Design Full Marks: 70

Time: 3 Hours

[There are 7(Seven) questions. Answer any 5(Five) questions.]

[Marks allotted are indicated in the right margin within '[ ]'.]

1.a) Derive simplified function for D and B_0 of **Figure 1.** [4]



5k

		D	B_0
00	0	X	
01	1	X	
10	X	1	
11	X	0	

Figure 1: Circuit for 1.a)

b) The following register-transfer operations specify a four-state control of the sequence register and decoder type. G is a 2-bit sequence register and T_0, T_1, T_2 and T_3 are the outputs of the decoder. [5]

xT_0: G ← G+1

yT_0: G ← 10

zT_0: G ← 11

$T_1+T_2+T_3$: G ← G+1

Draw the state diagram of the control and design the sequence register with JK flip-flops.

c) Design a combinational circuit using a PLA. The circuit accepts a 2-bit number and generates an output binary number equal to the cube of the input number. Derive the PLA program table for this circuit. [5]

2.a) What is mnemonics? Explain with example. [2]

b) How do Program Counter and Ring Counter differ from each other? Explain with example. [2]

c) Translate the following program into SAP-1 machine language. [4]

		Address	Instruction	
PC	A	0H	LDA 9H	00
		1H	ADD AH	01
MAR Input	ALU	2H	ADD BH	
		3H	SUB CH	01
RAM	B	4H	OUT	010
		5H	HLT	0F
IR	O	9H	01H	0E
		AH	02H	
CU	D	BH	03H	
		CH	04H	

d) Describe the SAP-1 architecture. [6]

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3.

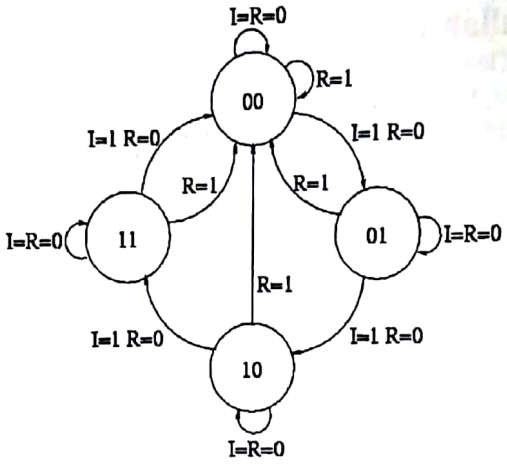

Figure 2: control state diagram for problem 3

The state diagram of a control unit is shown in **Figure 2.** It has four states and two inputs I and R. You must represent the 00 state as T_0, 01 state as T_1, 10 state as T_2 and 11 state as T_3.

a) Design the control using four D flip-flops. [4]

b) Design the control using two J-K flip-flops and a 2×4 decoder. [5]

c) Design the control using a PLA. [5]

4.a) Describe bidirectional register of SAP -2 architecture. [2]

b) Explain handshaking of SAP-2 architecture with example. [3]

c) How much time delay does this SAP -2 subroutine produce? [4]

```
        MVI A,0AH
LOOP1:  MVI B,64H
LOOP2:  MVI C,47H
LOOP3:  DCR C
        JNZ LOOP3
        DCR B
        JNZ LOOP2
        DCR A
        JNZ LOOP1
        RET
```

T states required for MVI, DCR, JNZ and RET is 7, 4, 10/7 and 10 respectively.

d) The traffic lights on a main road show green for 90 s, yellow for 10 s, and red for 40 s. Bits 1, 2 and 3 of port 4 of SAP-2 are the control inputs to peripheral equipment that runs these traffic lights. Write a program in mnemonics for SAP-2 that produces time delays of 90, 10 and 40 s for the traffic lights. [5]

5.a) Describe the write and read operations of a RAM. [2]

b) What is Shift Register? What are the differences between SRAM and DRAM? [3]

c) Design an arithmetic circuit with one selection variable s and two data inputs A and B. When s = 0, the circuit performs the addition operation F = A + B. When s = 1, the circuit performs the decrement operation F = A - 1. [3]

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d) Deign an arithmetic logic unit with three selection variables S_2, S_1 and S_0, that generates the following arithmetic and logic operations. When S_2 =0 the arithmetic operations are done and when S_2 =1 the logical operations are done. [6]

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$	C_{in} = × (don't care)
0	0	F = A + 1	F = A	F = AB (AND)
0	1	F = A – B	F = A – B – 1	F = A⊕B (XOR)
1	0	F = B – A	F = B – A – 1	F = A+B (OR)
1	1	F = A + B + 1	F = A + B	F = A ↑ B (NAND)

6.a) What is Modified Booth's algorithm? Explain with example. [3]

b) Design a 3-bit gray code counter as shown in the state diagram of **Figure 3**. Use J-K flip-flops. [5]

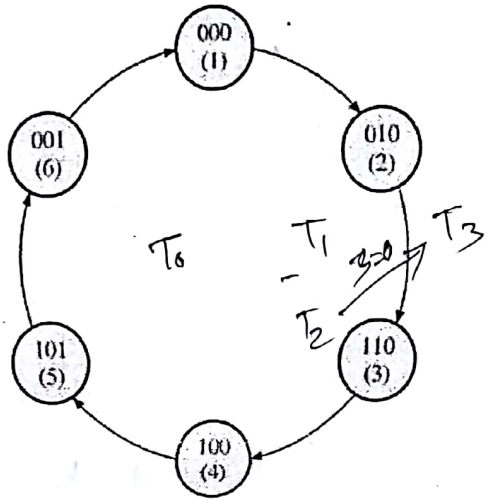

Figure 3: State Diagram for problem 6 (b)

c) If m = 110110 , r = 101101 , x = 6 and y = 6; using the Booth's multiplication algorithm determine the initial value of A , S and P. Show all the steps of Booth's algorithm to find the final value of P. [6]

7. Design a hard-wired control to implement the addition and subtraction of two fixed-point binary numbers represented in sign magnitude form. Your design must include the following steps:

i. Equipment Configuration [2]
ii. Derivation of the Algorithm [2]
iii. Flowchart [2]
iv. Control state diagram and Sequence of microoperations [4]
v. Design of Hard-wired Control [4]

You must use an ALU that has the following function table:

S_2	S_1	S_0	C_{in}	Output
0	0	1	0	F = A + B
0	1	0	1	F = A - B
1	1	1	0	F = A'
0	0	0	1	F = A + 1

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