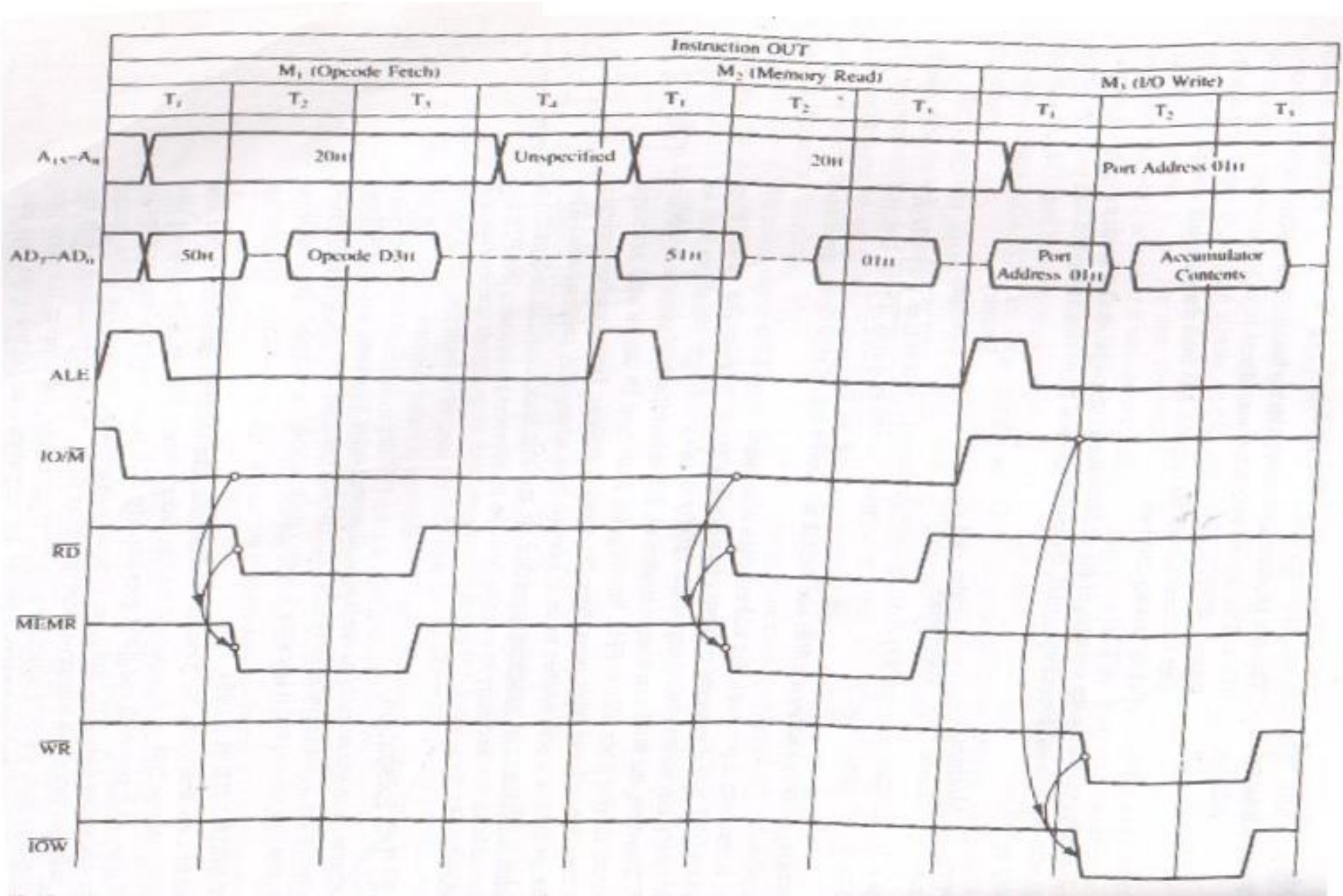
OUT Instruction



OUT Instruction

- In First Machine cycle M1(Opcode Fetch), microprocessor places the 16-bit memory address from the program counter (PC) on the address bus. At T1 20H is placed on A15-A8 and 50H is placed on AD7-AD0. ALE goes high, IO/M' goes low indicates memory related operations. ALE indicates the availability of the address on AD7-AD0. At T2 microprocessor sends RD' control signal which is combined with IO/M' to generate MEMR' signal and processor fetches the instruction code D3 using data bus.

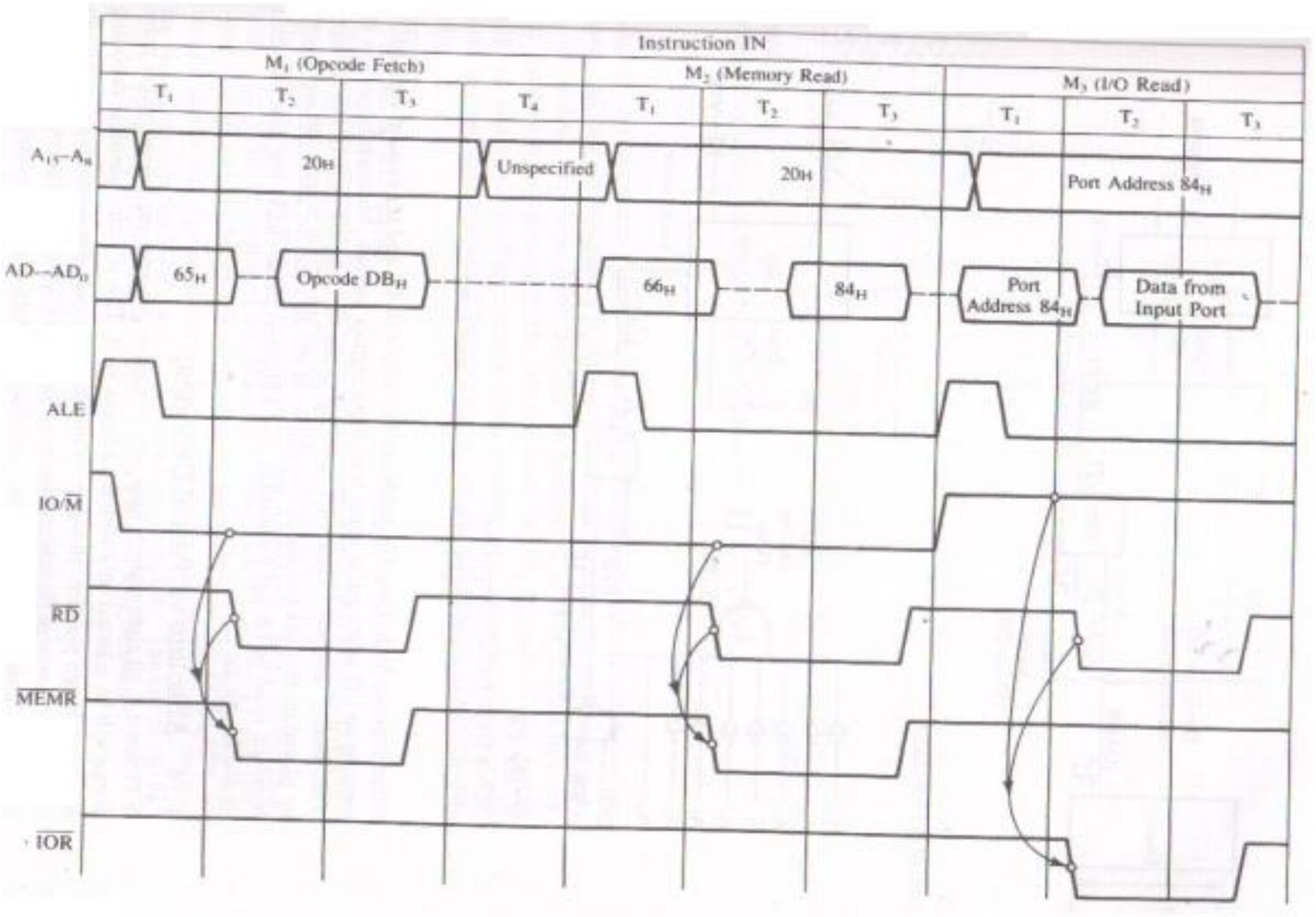
- M2 (memory Read), 8085 places next address 2051H on address bus and get device address 01H.

- M3 (I/O write), 8085 place device address 01H on low and high address bus both.IO/M' goes high to indicate I/O operation. At T2 AC contents are placed on data bus followed by control signal WR'. If we connect data bus to latch we can catch the information and display on LEDs and Printer. By ANDing IO/M' and WR' signals IOW' signal enable output device.

Information necessary for interfacing output device is available during T2 and T3 of

the M3 cycle.

IN Instruction



IN Instruction

- In First Machine cycle M1 (Opcode Fetch), microprocessor places the 16-bit memory address from the program counter (PC) on the address bus. At T1 20H is placed on A15-A8 and 65H is placed on AD7-AD0. ALE goes high, IO/M' goes low indicates memory related operations. ALE indicates the availability of the address on AD7-AD0. At T2 microprocessor sends RD' control signal which is combined with IO/M' to generate MEMR' signal and processor fetches the instruction code DB using data bus.

- M2 (Memory Read), 8085 places next address 2066H on address bus and get device address 84H.

- M3 (Memory Read), 8085 place device address 84H on low and high address bus both and asserts RD' signal. IO/M' goes high to indicate IO operation. At T2 data from input port are paced on data bus and transferred to AC. By ANDing IO/M' and $\overline{RD}$ signals IOR' signal to enable input port.

Memory Mapping Vs Peripheral I/O

- Memory mapped I/O

1) In this device add is 16 bit (A0-A15)
2) MEMR^ and MEWR^ control signals are used
3) Instructions are LDA add, STA Add, MOV A,M
4) Data trans. Bet reg and I/O devices
5) No. of I/O devices interface= 65536

(Theoretically)

I/O mapped I/P

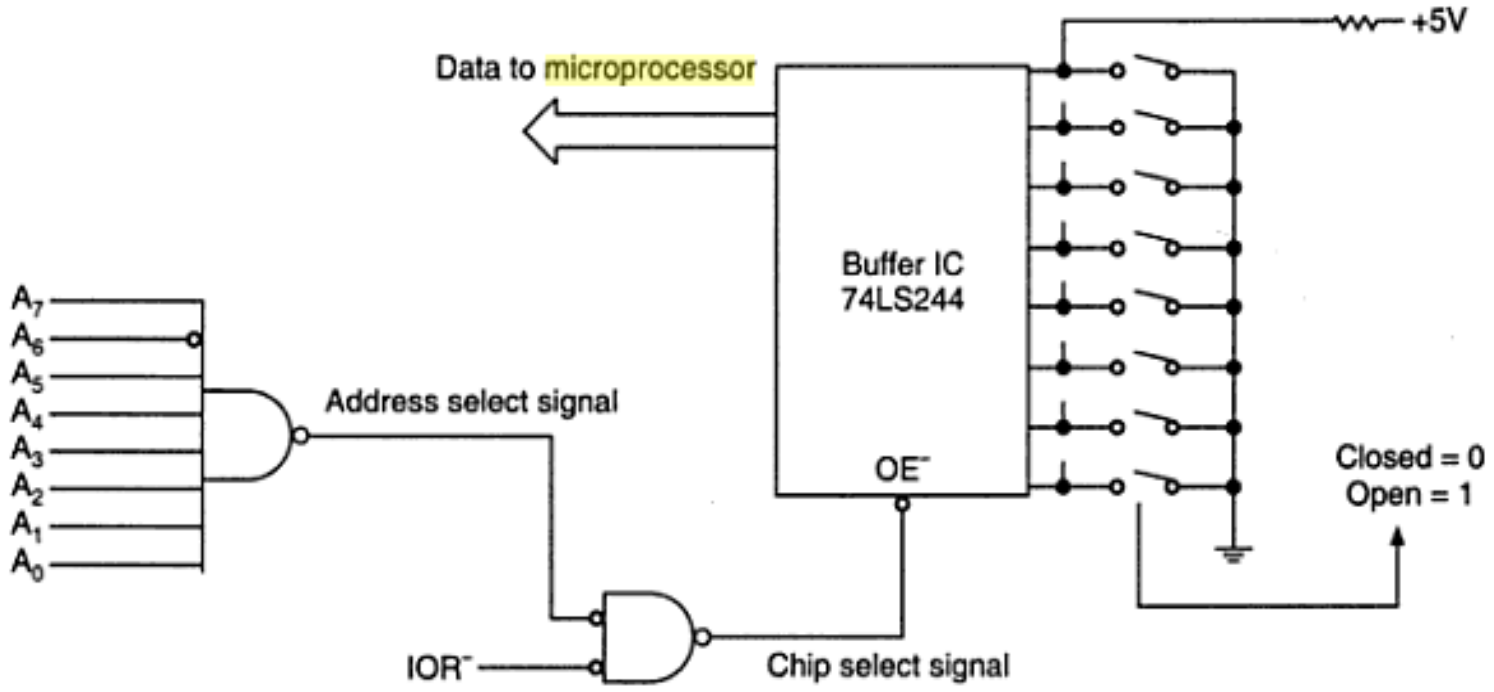
1) In this device add is 8 bit (A0-A7)
2) IOR^ and IOW^ control signals are used
3) Instruction are IN Add, OUT Add
4) Data trans. Bet acc and I/O devices
5) No. of I/O devices interface= 256 only

EXAMPLE 1 Interface 8 switches using buffer IC with 8085 in IO mapped IO scheme. The input switches have an input address 40H.

Solution The interface is shown in Figure . A bubbled NAND gate is used to decode the seven address lines. The output of the bubbled NAND gate is low when the address lines are as follows:

$$A_7A_6A_5A_4A_3A_2A_1A_0 = 01000000B = 40H \text{ and } \overline{IOR} = 0$$

The low output of the bubbled NAND gate will enable the buffer IC 74244 which, in turn, connects the status of the switches to the data bus of the microprocessor.



EXAMPLE .2 Interface 8 switches and 8 LED's using buffer and latch IC as input and output devices, with 8085 in IO mapped IO scheme. The input and output have port address 40H.

Solution The interface is shown in Figure . A bubbled NAND gate is used to decode the seven address lines. The output of the bubbled NAND is low when the address lines are as follows:

$$A_7A_6A_5A_4A_3A_2A_1A_0 = 01000000B = 40H$$

The same address select signal is applied to the bubbled NAND gates which are used to enable the buffer and latch IC.

The bubbled NAND gate 1 will generate the active low OE^- signal when,

$$A_7A_6A_5A_4A_3A_2A_1A_0 = 01000000B = 40H \text{ and } IOR^- = 0$$

which is generated when the instruction IN 40H is executed by the microprocessor.

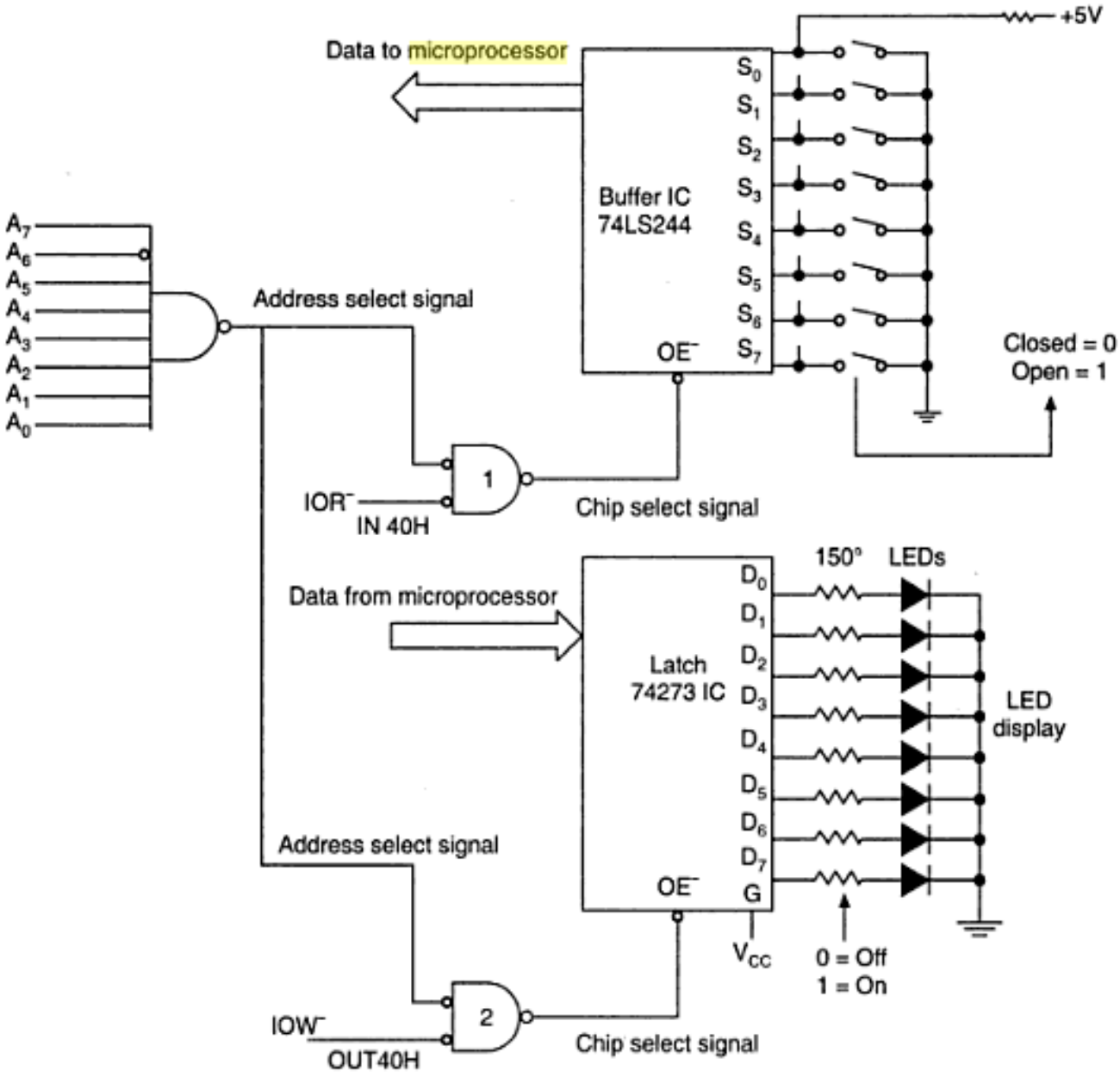
The low output of the bubbled NAND gate 1 will enable the buffer IC 74244 which in turn connects the status of the switches to the data bus of the microprocessor.

Similarly, the bubbled NAND gate 2 will generate the active low OE^- signal for the latch IC when

$$A_7A_6A_5A_4A_3A_2A_1A_0 = 01000000B = 40H \text{ and } IOW^- = 0$$

which is generated when the instruction OUT 40H is executed by the microprocessor.

The low output of the bubbled NAND gate 2 will enable the latch IC 74273 which in turn connects the data bus of the microprocessor to the input of the D – FF. The output of the D – FF will be available to the LED display even when the data is removed from the data bus of the microprocessor.


+5V
Data to microprocessor
S_0
S_1
S_2
S_3
S_4
S_5
S_6
S_7
Buffer IC
74LS244
OE^-
Closed = 0
Open = 1
A_7
A_6
A_5
A_4
A_3
A_2
A_1
A_0
Address select signal
1
IOR^-
IN 40H
Chip select signal
150° LEDs
Data from microprocessor
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
Latch
74273 IC
LED
display
OE^-
G
V_{CC}
0 = Off
1 = On
Address select signal
2
IOW^-
OUT40H
Chip select signal