26.04.16

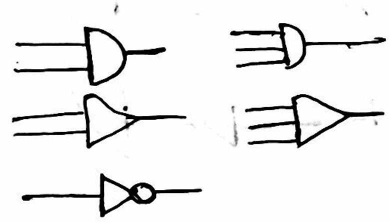
* Basic Logic

  — AND
  — OR
  — NOT

* binary logic use করে যে logic তৈরি হয় তাকে boolean logic বলে।

* Boolean logic কে physically representation -কে gate বলে।

  — AND Gate →
  — OR Gate →
  — Not Gate →

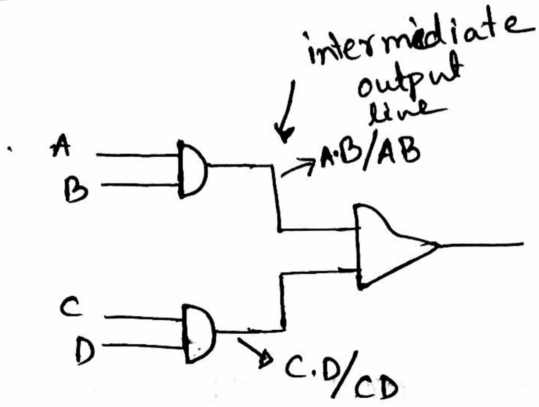


} n-input

* two types of wire
  — Input
  — output

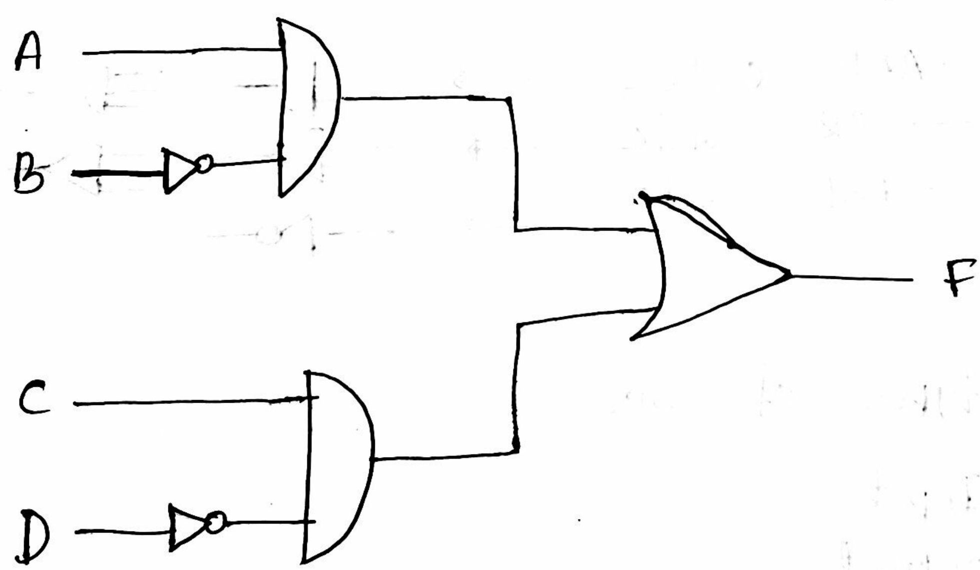
* electricity data pass করে।
* IC - integrated *circuit (set of gates) - design
  ~~AD~~ AND IC - 4টে fabricated আছে।

* Circuit



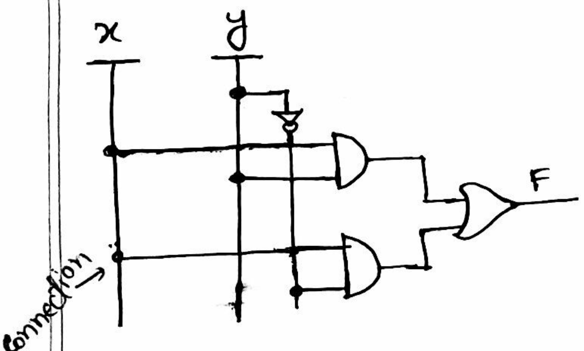
$F = \underbrace{AB + CD}$

* $F(A, B, C, D) = A\bar{B} + C\bar{D}$



* Boolean logic
* Boolean Expression
* Boolean Function

* $F(x,y) = xy + x\bar{y}$



x	y	F
0	0	0
0	1	0
1	0	1
1	1	1

~~Postulates~~ Postulates

27.04.16

* Boolean Algebra (binary logic use করে যে algebra)

1. (a) closure w.r.t (+) op
 (b) closure w.r.t (•) op.

2. (a) Identity element w.r.t (+) is 0 $\quad x+0 \equiv x$
 (b) Identity element w.r.t. (•) is 1 $\quad x \cdot 1 = x$

3 (a) Communative w.r.t (+): $x+y \equiv y+x$
 (b) communative w.r.t (•): $x \cdot y \equiv y \cdot x$

imp
4. (a) (•) is distributive over (+):
$$x\cdot(y+z) \equiv (x\cdot y)+(x\cdot z)$$

 (b) (+) is distributive over (•):
$$x+(y\cdot z) \equiv (x+y)\cdot(x+z)$$

5. (a) $x + \bar{x} = 1$
 (b) $x \cdot \bar{x} = 0$

Theorem 1(a)

$$x+x$$
$$= (x+x)\cdot 1$$
$$= (x+x)(x+\bar{x})$$
$$= x + x\cdot\bar{x}$$
$$= x + 0$$
$$= x$$
$$\therefore x + x = x$$

Theorem 1(b)

$$x\cdot x = xx + 0$$
$$= xx + x\cdot\bar{x}$$
$$= x(x+\bar{x})$$
$$= x\cdot 1$$
$$= x$$
$$\therefore x\cdot x = x$$

Theorem 2(a)

$$x+1 = 1\cdot(x+1)$$
$$= (x+\bar{x})(x+1)$$
$$= x + \bar{x}\cdot 1$$
$$= x + \bar{x}$$
$$= 1$$
$$\therefore x+1 = 1$$

Theorem 6(a)

$$x+xy = x\cdot 1 + xy$$
$$= x(1+y)$$
$$= x\cdot 1$$
$$= x$$
$$x+xy = x$$

* $F(x, y) = xy + x\bar{y}$

$= x(y+\bar{y})$

$= x \cdot 1$

$= x$

* $F(x,y) = x(\bar{x}+y)$

$= x\bar{x} + xy$

$= 0 + xy$

$= xy$

* $F(x,y,z) = x+\bar{y}z$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

* Minterm

* Maxterm

11.05.16

* Canonical forms

- Sum of minterms
- Product of maxterms

* Standard forms

simplified expression

- Sum of Products (SOP)
- Product of sums (POS)

প্রতি variable একবার, And আকারে

* Minterm

binary value represent করে

$x = 1$

$\bar{x} = 0$

x	y	z
↓	↓	↓
1	1	1 = 7

$\bar{x}\bar{y}\bar{z}$	0 0 0 = 0
$\bar{x}\bar{y}z$	0 0 1 = 1
$\bar{x}y\bar{z}$	0 1 0 = 2
$\bar{x}yz$	0 1 1 = 3
$x\bar{y}\bar{z}$	1 0 0 = 4
$x\bar{y}z$	1 0 1 = 5
$xy\bar{z}$	1 1 0 = 6
xyz	1 1 1 = 7

প্রতি Variable একবার, OR আকারে যুক্ত

Max term

$\bar{x} = 1$

$x = 0$

$\bar{x} + \bar{y} + \bar{z}$

$\downarrow \quad \downarrow \quad \downarrow$

1 1 1 = 7

$x + y + z$

$x + y + \bar{z}$

$x + \bar{y} + z$

$x + \bar{y} + \bar{z}$

$x + y + z$

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* Sum of Minterms,

$f(x, y) = \bar{x}\bar{y} + xy$

* Sum of Products.

$f(x, y) = xy + \bar{x}$

* product of Maxterms

$f(x, y) = (x+y) \cdot (\bar{x}+y)$

* product of sums,

$f(x, y) = x \cdot (\bar{x} + \bar{y})$

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$f(x, y, z) = x + \bar{y}z$

MSB → Most significant Bit → 7

LSB → Least significant Bit → 3

$f(x, y, z) = x + \bar{y}z$

Minterm

$\bar{x}\,\bar{y}$
$\bar{x}\,y$
$\bar{x}\,y$
xy

$f(x,y,z) = \bar{x}\bar{y}\bar{z} + x\bar{y}\bar{z} + \bar{x}\bar{y}z + xy\bar{z} + xyz$

$= \bar{x}\bar{y}\bar{z} + x\bar{y}(\bar{z}+z) + xy(\bar{z}+z)$

$= \bar{x}\bar{y}z + x\bar{y} + xy$

$= \bar{x}\bar{y}\cdot z + x$

$= (\bar{x}+x)(x+\bar{y}z)$

$= x+\bar{y}z$

* x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$F(x,y,z) = \Sigma(1,4,5,7)$

$\boxed{\therefore (m_i)' = M_i}$

maxterm $\xleftrightarrow{\text{compliment}}$ minterm

* minterm এর compliment করলে maxterm পাওয়া যায়
* maxterm এর compliment করলে minterm পাওয়া যাবে।

$f = \bar{x}\bar{y}z + x\bar{y}\bar{z} + xyz$

$= m_1 + m_4 + m_7$

$= \Sigma(1,4,7)$

$f' = \bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + \bar{x}yz + x\bar{y}z + xy\bar{z}$

$(f')' = (\bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + \bar{x}yz + x\bar{y}z + xy\bar{z})'$

$\Rightarrow f = (\bar{x}\bar{y}\bar{z})' \cdot (\bar{x}y\bar{z})' \cdot (\bar{x}yz)' \cdot (x\bar{y}z)' \cdot (xy\bar{z})'$

$= (x+y+z)(x+\bar{y}+z)(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})(\bar{x}+\bar{y}+z)$

$= M_0 \cdot M_2 \cdot M_3 \cdot M_5 \cdot M_6$

$= \Pi(0,2,3,5,6)$

16.05.16

* $F(A,B,C) = A + \bar{B}C$

$\bar{B}C$ < $A\bar{B}C$, $\bar{A}\bar{B}C$

$$\bar{B}C = \bar{B}C \cdot 1 = \bar{B}C \cdot (A + \bar{A}) = A\bar{B}C + \bar{A}\bar{B}C$$

A < AB < ABC, $AB\bar{C}$

A < $A\bar{B}$ < $A\bar{B}C$, $A\bar{B}\bar{C}$

$$F = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}C$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$$

$$= \sum(7, 6, 5, 4, 1)$$

$$F(x,y,z) = xy + \bar{x}z$$

$$= (xy + \bar{x})(xy + z)$$

$$= (x + \bar{x})(\bar{x} + y)(x + z)(y + z)$$

$$= (\bar{x} + y)(x + z)(y + z)$$

$$\bar{x} + y = \bar{x} + y + z\bar{z} = (\bar{x} + y + z)(\bar{x} + y + \bar{z})$$

$$x + z = x + z + y\bar{y} = (x + y + z)(x + \bar{y} + z)$$

$$y + z = y + z + x\bar{x} = (x + y + z)(\bar{x} + y + z)$$

$$F' = (\bar{x}+y+z)(\bar{x}+y+\bar{z})(x+y+z)(\bar{x}+y+z)$$
$$(x+y+z)(\bar{x}+y+z)$$

$$= (\bar{x}+y+z)(\bar{x}+y+\bar{z})(x+y+z)(x+\bar{y}+z)$$

$$= \pi(4,5,0,2)$$

* Map Method → the onam, Posl

K-Map (Karno Map) ↑ scientist

2-Variable Map

$x \backslash y$	0	1
0	00	01
1	10	11

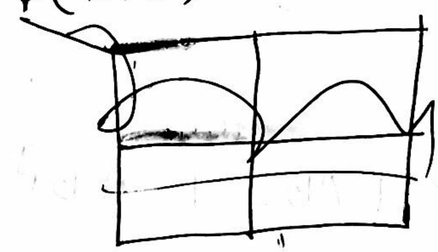
$\bar{x}\bar{y}$ − 0 − 00

$\bar{x}y$ − 1 − 01

$x\bar{y}$ − 2 − 10

xy − 3 − 11

$$F(x,y) = x\bar{y} + \bar{x}y + xy$$



2^n এর multiple 1 নিয়ে circle হবে।

$x \backslash y$	0	1
0		1
1	1	1

$$= x + y$$

circle rules:

1. 2^n এর multiple 1 নিয়ে হবে
2. neighbour 1 হতে হবে।
3. circle এর variable এর different হলে সেটি বাদ যাবে

$x \backslash y$	0	1
0	1	1
1		

minterm এ x এর variable মান 0 হলে $\bar{x}$ হয়

$$= \bar{x}$$

$x \backslash y$	0	1
0		1
1	1	

$= x\bar{y} + \bar{x}y$

x	y	$F = x \oplus y$
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive OR.

$F = \bar{x}y + x\bar{y}$

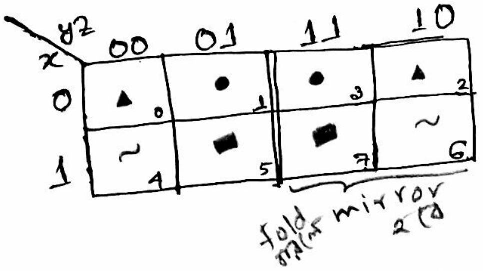
$x \backslash y$	0	1
0	1	1
1	1	1

$= 1$

$$= \bar{x}\bar{y} + \bar{x}y + x\bar{y} + xy$$
$$= \bar{x}(\bar{y}+y) + x(\bar{y}+y)$$
$$= \bar{x}\cdot 1 + x\cdot 1$$
$$= \bar{x} + x$$
$$= 1$$

17.05.16

* 3 variable Map



$000 - \bar{x}\bar{y}\bar{z}$

$001 - \bar{x}\bar{y}z$

$010 - \bar{x}y\bar{z}$

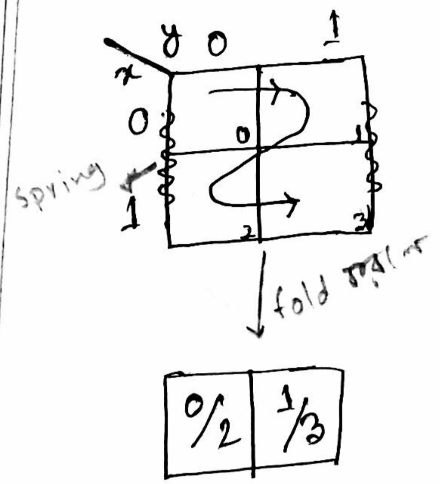
$011 - \bar{x}yz$

$100 - x\bar{y}\bar{z}$

$101 - x\bar{y}z$

$110 - xy\bar{z}$

$111 - xyz$



* $F(x,y,z) = \bar{x}yz + \bar{x}y\bar{z} + x\bar{y}\bar{z} + x\bar{y}z$

x \ yz	00	01	11	10
0			1	1
1	1	1		

$= x\bar{y} + \bar{x}y$

$= x \oplus y$

$F(x,y,z) = \bar{x}z + \bar{x}y + x\bar{y}z + yz$

$\bar{x}z$ — $\bar{x}\bar{y}z = 1$, $\bar{x}yz = 3$

$\bar{x}y$ — $\bar{x}y\bar{z} = 2$, $\bar{x}yz = 3$

yz — $\bar{x}yz = 3$, $xyz = 7$

x \ yz	00	01	11	10
0		1	1	1
1		1	1	

$= z + \bar{x}y$

x \ yz	00	01	11	10
0	1			1
1	1			1

→ 1 by circle 2(?) mirror

$= \bar{z}$

x \ yz	00	01	11	10
0		1	1	
1		1	1	

$= z$

* 4-Variable Map

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

fold করলে mirror হবে

* $F(A,B,C,D) = \Sigma(0,1,4,5,6,8,9,12,13,14)$

AB \ CD	00	01	11	10
00	1	1		
01	1	1		1
11	1	1		1
10	1	1		

1000
1001
1010
1011
1100
1101
1110
1111

$= \overline{C} + B\overline{D}$

AB \ CD	00	01	11	10
00	1	8		1
01	1			1
11				
10	1	1		1

18.06.16

* $F(A,B,C,D) = \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}$

$\bar{A}\bar{B}\bar{C} < \begin{matrix} \bar{A}\bar{B}\bar{C}\bar{D} = 0 \\ \bar{A}\bar{B}\bar{C}D = 1 \end{matrix}$

$\bar{B}C\bar{D} < \begin{matrix} \bar{A}\bar{B}C\bar{D} = 2 \\ A\bar{B}C\bar{D} = 10 \end{matrix}$

$\bar{A}BC\bar{D} = 6$

$A\bar{B}\bar{C} < \begin{matrix} A\bar{B}\bar{C}\bar{D} = 8 \\ A\bar{B}\bar{C}D = 9 \end{matrix}$

AB \ CD	00	01	11	10
00	1	1		1
01				1
11				
10	1	1		1

$= \bar{B}\bar{C} + \bar{A}C\bar{D} + \bar{B}\bar{D}$

* 5-Variable Map

$F(A,B,C,D,E) = \Sigma\,(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$

AB \ CDE	000	001	011	010	110	111	101	100
00	1			1	1			1
01		1	1			1	1	
11		1	1			1	1	
10		1					1	

=

don't care supporting element

Don't care symbol — X

* Dont care condition

$$f(w,x,y,z) = \Sigma(1,3,7,11,15)$$

$$d(w,x,y,z) = \Sigma(0,2,5)$$

এই condition গুলো effect রাখে না

* কিছু input এর জন্য output এ effect রাখে না

wx \ yz	00	01	11	10
00	X	1	1	X
01		X	1	
11			1	
10			1	

$= yz + \bar{w}\bar{x}z \approx 5$

2X → $= yz + \bar{w}\bar{x} \approx 4$

1 $= yz + \bar{w}z \approx 4$

* Tabulation Method

25.05.2016

24.05.2016

* Tabulation Method :

$$F(w,x,y,z) = \Sigma(1,4,6,7,8,9,10,11,15)$$

√ → যে কারো সাথে mapping হবে।

a	b	c
0001 (1) ✓	_001 (1,9)	10_ _ (8,9,10,11)
0100 (4) ✓	01_0 (4,6)	10_ _ (8,9,10,11)
1000 (8) ✓	100_ (8,9) ✓	
0110 (6) ✓	10_0 (8,10) ✓	
1001 (9) ✓	011_ (6,7)	
1010 (10) ✓	10_1 (9,11) ✓	
0111 (7)	101_ (10,11) ✓	
1011 (11)	_111 (7,15)	
1111 (15)	1_11 (11,15)	

Prime Implicants

Decimal	Binary $w\ x\ y\ z$	Terms
1, 9	omit _ 0 0 1	$\bar{x}\bar{y}z$
4, 6	0 1 _ 0	$\bar{w}x\bar{z}$
6, 7	0 1 1 _	$\bar{w}xy$
7, 15	_ 1 1 1	xyz
11, 15	1 _ 1 1	wyz
8, 9, 10, 11	1 0 _ _	$w\bar{x}$

prime implicants

Next Quiz 1 — 8·06·16 → wednesday

Essential Prime Implicants

	1	4	6	7	8	9	10	11	15
✓ $\bar{x}\bar{y}z(1,9)$	X					X			
✓ $\bar{w}x\bar{z}(4,6)$		X	X						
$\bar{w}xy(6,7)$			X	X					X
✓ $xyz(7,15)$				X				X	X
$wyz(11,15)$									
✓ $w\bar{x}(8,9,10,11)$					X	X	X	X	
	✓	✓	✓	✓	✓	✓	✓	✓	✓

$F = \bar{x}\bar{y}z + \bar{w}x\bar{z} + w\bar{x} + xyz$

worst case, $F = \bar{x}\bar{y}z + \bar{w}x\bar{z} + w\bar{x} + \bar{w}xy + wyz$ ✗

- $F(A,B,C) = A$

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$F = A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$

$= A\bar{B}(\bar{C}+C) + AB(\bar{C}+C)$

$= A\bar{B} + AB$

$= A(B+\bar{B})$

$= A$

A → $A\bar{B}$ → $A\bar{B}\bar{C} = 4$, $A\bar{B}C = 5$

A → AB → $AB\bar{C} = 6$, $ABC = 7$

$$\begin{array}{r} \text{1} \rightarrow \text{carry in} \\ 1\,1 \\ +\;0\,1 \\ \hline 0 \\ \text{1} \rightarrow \text{carry out} \end{array}$$

* Adder circuit
↓ 2 bit
sum bit, carry bit

Truth Table তৈরি করার জন্য

* Adder (যোগ করে) →

- Half — carry in বিবেচনা আনবে না।
- full — carry এর basis এ divide করা হয়

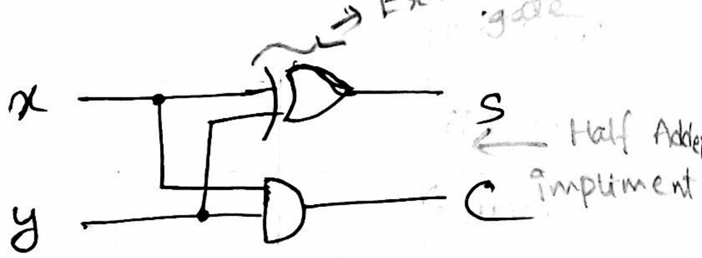
$C = xy$

$S = x\bar{y} + \bar{x}y$

$= x \oplus y$

হাতে রাখার * Carry

- carry in → input থাকবে থাকে
- carry out → generate হবে।



circuit diagram

* Half Adder < And gate, Exclusive OR gate

x	y	C (carry)	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

→ বড় circuit এর complexity কমায়

block diagram

1

1 0

0 0 1

0 1 0

0 1 1 0

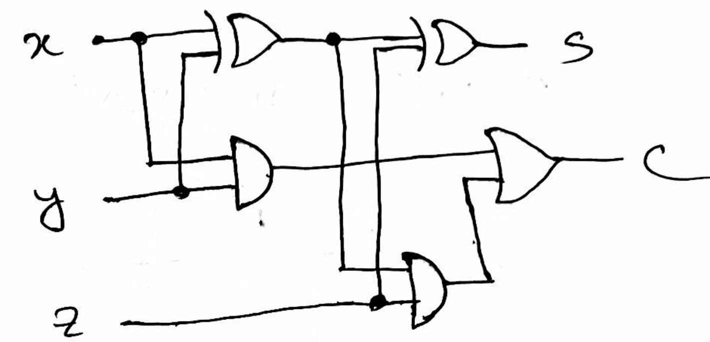
xy

$$\bar{x}\bar{y} + xy = x \odot y$$

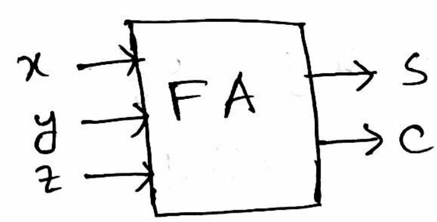
30.05.16

* Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



circuit Diagram
↓
gate level → implemen



$$C = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

$$= z(\bar{x}y + x\bar{y}) + xy(\bar{z} + z)$$

$$= (x \oplus y)z + xy$$

$$S = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$

$$= \bar{x}(y \oplus z) + \cancel{x(\bar{y}\bar{z} + x} \; x(y \oplus z)'$$

$$= x \oplus y \oplus z \qquad [\bar{x}y + x\bar{y} = x \oplus y]$$

* Subtractor

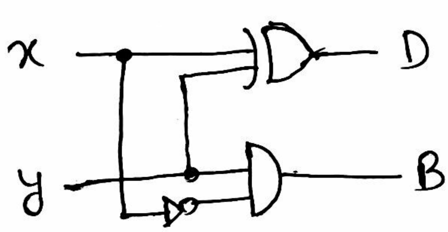
- Half
- full

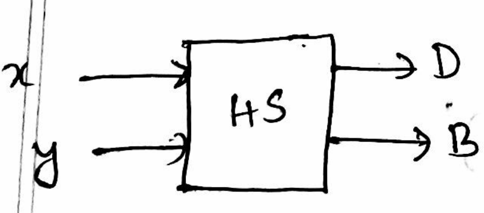
* Half sub (B in বিবেচনা করবে না)

x	y	$B^{(Bout)}$	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

$$B = \bar{x}y$$

$$D = \bar{x}y + x\bar{y}$$
$$= x \oplus y$$



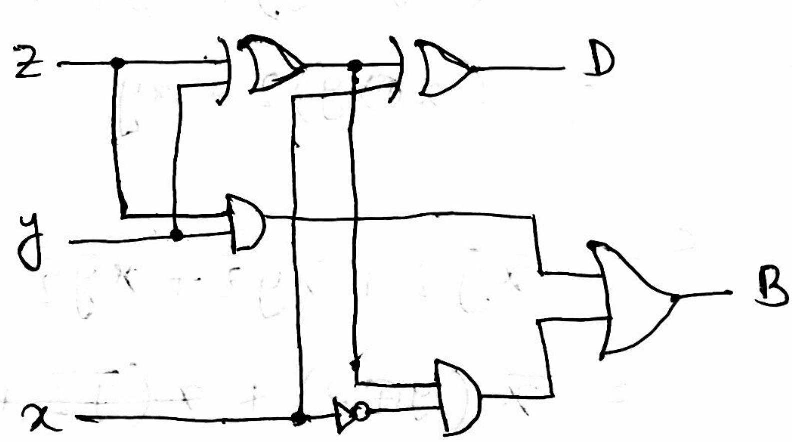


* Full Sub

x	y	z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$B = \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + xyz$$
$$= \bar{x}(y \oplus z) + yz$$

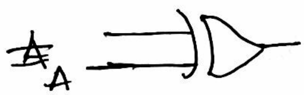
$$D = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$
$$= \bar{x}(y \oplus z) + x(y \oplus z)'$$
$$= x \oplus y \oplus z$$



* negative binary number represent করার জন্য 1's ~~...~~/2's complement

* Special feature of XOR

- Copy Op (একটা অপরটির input ~~...~~ 0 ~~...~~ fixed)
- Inverse Op (অপরটির input 1 দিয়ে fixed)



$$\begin{array}{r} 1000 \\ +1 \\ \hline 1001 \end{array}$$

2's compliment sub

A : 7 $(0111)_2$

B : −5 $(0101)_2 \xrightarrow{\text{2's comp}} (1011)_2$ $(\overline{B}+1)$

2

$$\begin{array}{r} 0111 : A \\ +\ 1011 : \overline{B}+1 \\ \hline 1\ 0010 \end{array}$$

1 → ✗ বাদ, $\underbrace{0010}_{2}$ → 2

$\therefore A - B = A + \overline{B} + 1$

$$\begin{array}{r} 5\ (0101)_2 \\ -\ 7\ (0111)_2 \\ \hline -2 \end{array}$$

$(0111)_2 \xrightarrow{\text{2's comp}} (1001)_2$

$$\begin{array}{r} 0101 \\ +\ 1001 \\ \hline 1110 \end{array}$$

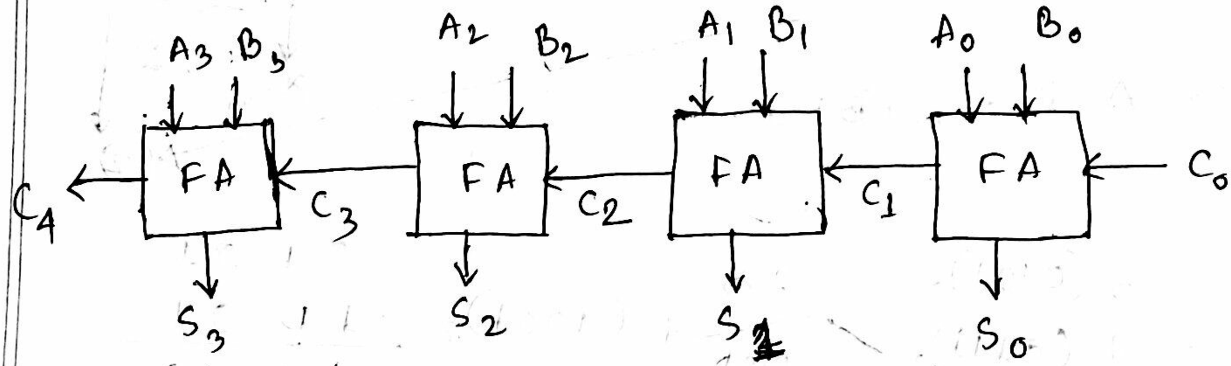
$1110 \xrightarrow{\text{2's comp}}$

$$\begin{array}{r} 0001 \\ +\ 1 \\ \hline -(0010)_2 \end{array}$$

(−2)

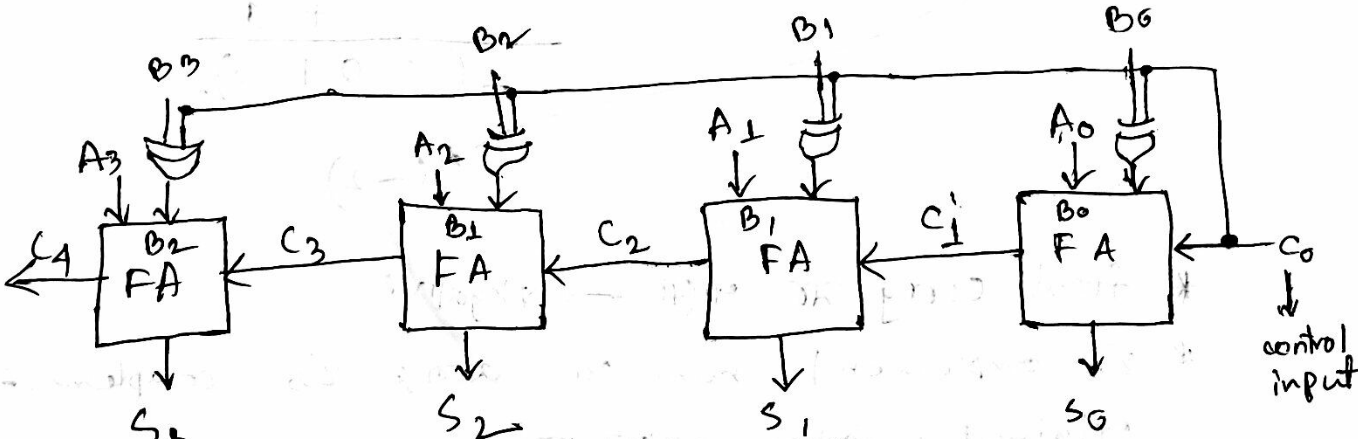
* final carry না থাকলে → Negative
* 2's complement num কে আবার 2's complement করলে original number পাওয়া যায়।

C_i :		C_3	C_2	C_1	C_0
		1	1	0	0
A_i :		A_3	A_2	A_1	A_0
		1	1	1	1
B_i :		B_3	B_2	B_1	B_0
		1	0	1	0
S_i :	C_4	S_3	S_2	S_1	S_0
	1	1	0	0	1
C_{i+1} :		C_4	C_3	C_2	C_1
		1	1	1	0



4-bit Parallel Adder

* $C_0 = 0$ [illegible]
copy 2C[illegible]



4-bit parallel Adder / Subtractor

31.05.16

4-bit parallel Adder/subtractor

* Code conversion circuit

Binary				Excess-3			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Don't care situation

$P = \Sigma(5, 6, 7, 8, 9)$

$Q = \Sigma(1, 2, 3, 4, 9)$

$R = \Sigma(0, 3, 4, 7, 8)$

$S = \Sigma(0, 2, 4, 6, 8)$

S →

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1			X

$S = \bar{A}\bar{D} + \bar{B}\bar{C}\bar{D}$?????

Don't care → $S = \bar{D}$

1 0 → digit by digit

weight

[illegible] binary [illegible] represent [illegible] 4bit [illegible] 4bit [illegible]

Decimel / But representation binary

$$\begin{array}{ccc} 1 & 1 & 0 \\ & \oplus & \oplus \\ 1 & 0 & 1 \end{array}$$

Binary	BCD 8421	Excess-3 (3 বেশি)	2421	84-2-1	Gray
0000	0000	0011	0000	0000	
0001	0001	0100	0001	0111	
0010	0010		1000/0010		
0011	0011		1001/0011		
0100	0100				
0101	0101				101
0110	0110				
0111	0111				
1000	1000				
1001	1001	1100	1111	1111	
1010	10000				
1011	10001				
1100	10010				
1101	10				
1110					
1111					

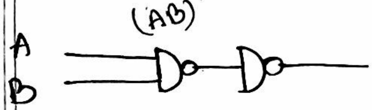
000 ~~*Sol~~ * সব input same হলে gate inverter হিসেবে কাজ করে
000

001 010 011
001 011 010

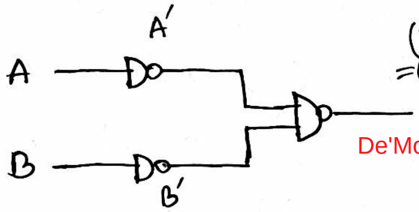
* Universal Gates

- NAND - NOR

$\overline{A}$ $(A\cdot A)' = \overline{A}$



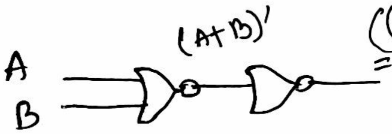
$AB \; ((A\cdot B)')' = AB$



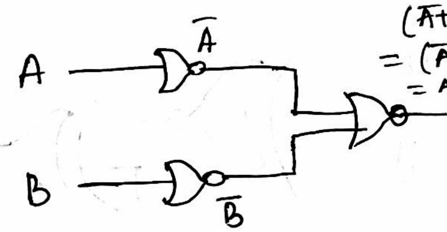
$(\overline{A}\,\overline{B})' = (\overline{A})' + (\overline{B})'$

De'Morgans Law

$\overline{A}$ $(A+A)' = \overline{A}$

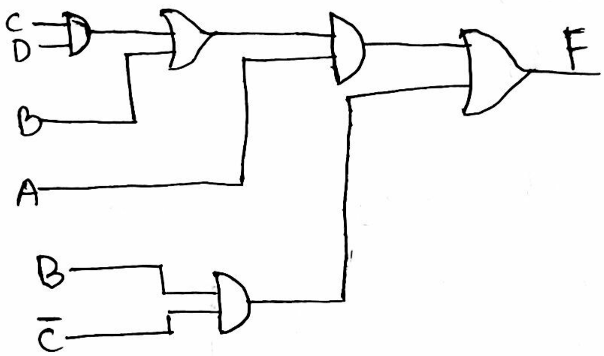


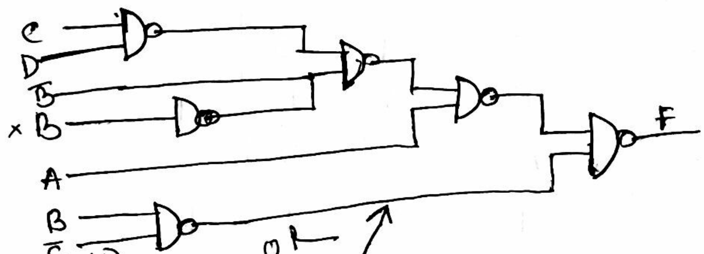
$((A+B)')' = A+B$

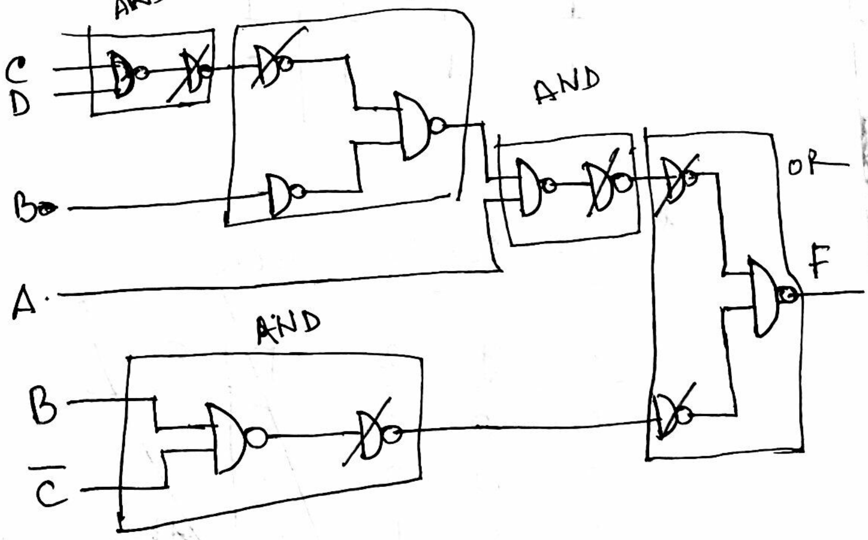


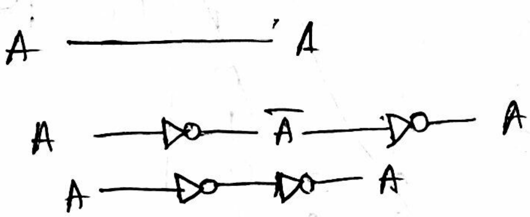
$(\overline{A}+\overline{B})' = (\overline{A})'\cdot(\overline{B})' = AB$

$F(A,B,C,D) = A(B+CD) + B\overline{C}$









01.06.16

*** Parity Bit** (original Bit এর মধ্যে additional bit) send করবে

— Even

— odd

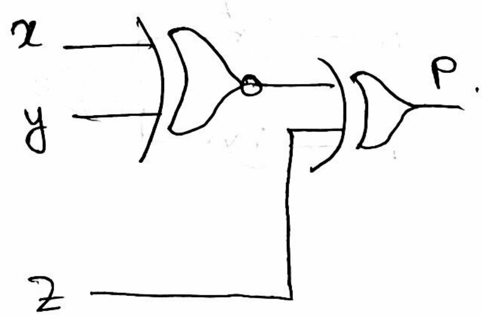
* odd Parity Generator

odd সংখ্যার 1 check করবো। odd হলে — 0 হবে

x	y	z	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

original → send

$$P = \bar{x}\bar{y}\bar{z} + \bar{x}yz + x\bar{y}z + xy\bar{z}$$
$$= \bar{x}(\bar{y}\bar{z} + yz) + x(\bar{y}z + y\bar{z})$$
$$= \bar{x}(y \oplus z)' + x(y \oplus z)$$
$$= x \odot y \oplus z$$



sender { 3bit odd parity Generator circuit

* Odd Parity checker

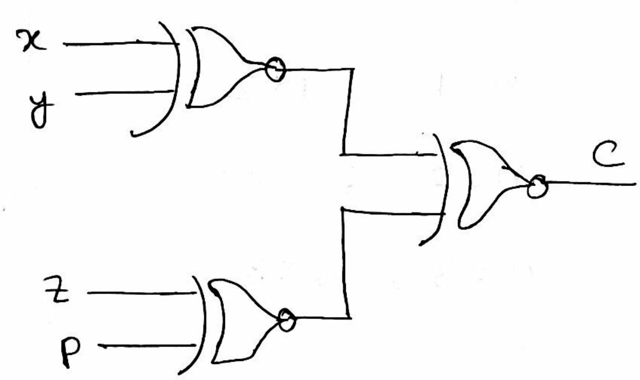
x	y	z	P	c
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	

x \ yz	00	01	11	10
0	1		1	
1		1	[illegible]	1

* odd Parity checker

x	y	z	p	c
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
~~1~~	~~1~~	~~0~~	~~0~~	
1	1	0	0	1
~~1~~	~~1~~	~~0~~	~~1~~	
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$$C = x \odot y \odot z \odot p$$



4bit odd parity checker circuit } ~~sen~~ receiver

06.06.16

* Decoders

$n \times 2^n$

n → inputs

2^n → outputs

$n=1$; 1×2

$n=2$; 2×4

$n=3$; 3×8

$D_0 = \bar{x}\bar{y}\bar{z}$

$D_1 = \bar{x}\bar{y}z$

$D_2 = \bar{x}y\bar{z}$

$D_3 = \bar{x}yz$

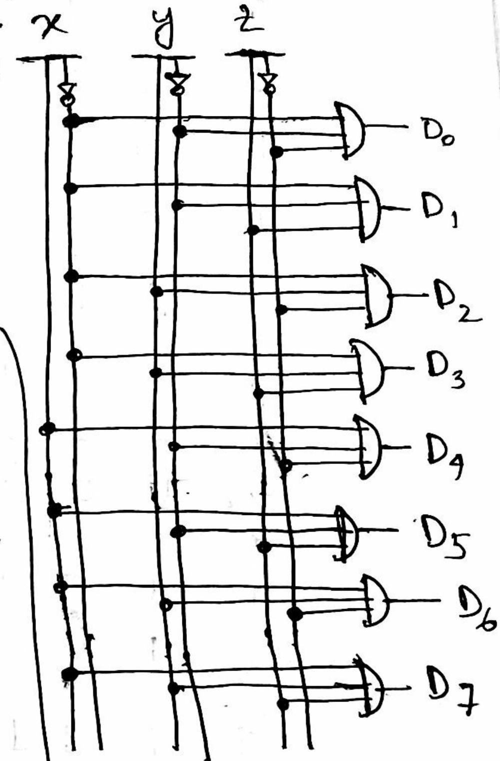
$D_4 = x\bar{y}\bar{z}$

$D_5 = x\bar{y}z$

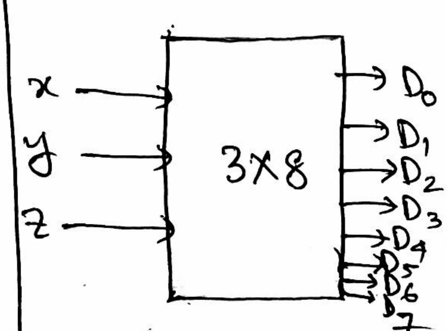
$D_6 = xy\bar{z}$

$D_7 = xyz$

x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

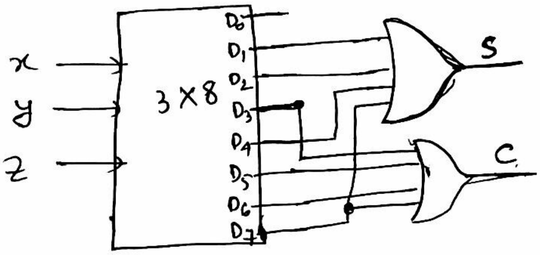


3×8 Decoder circuit

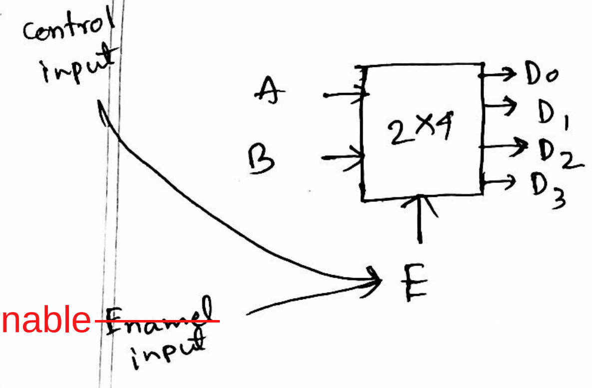


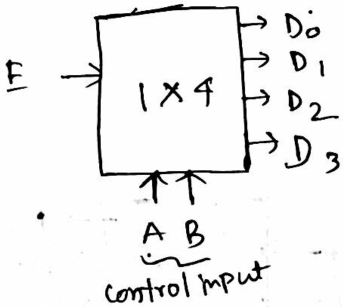
$* \; S(x,y,z) = \Sigma(1,2,4,7)$

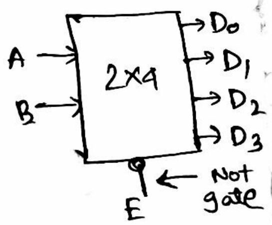
$C(x,y,z) = \Sigma(3,5,6,7)$



* Demultiplexer (updated version)



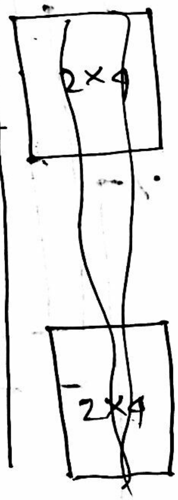




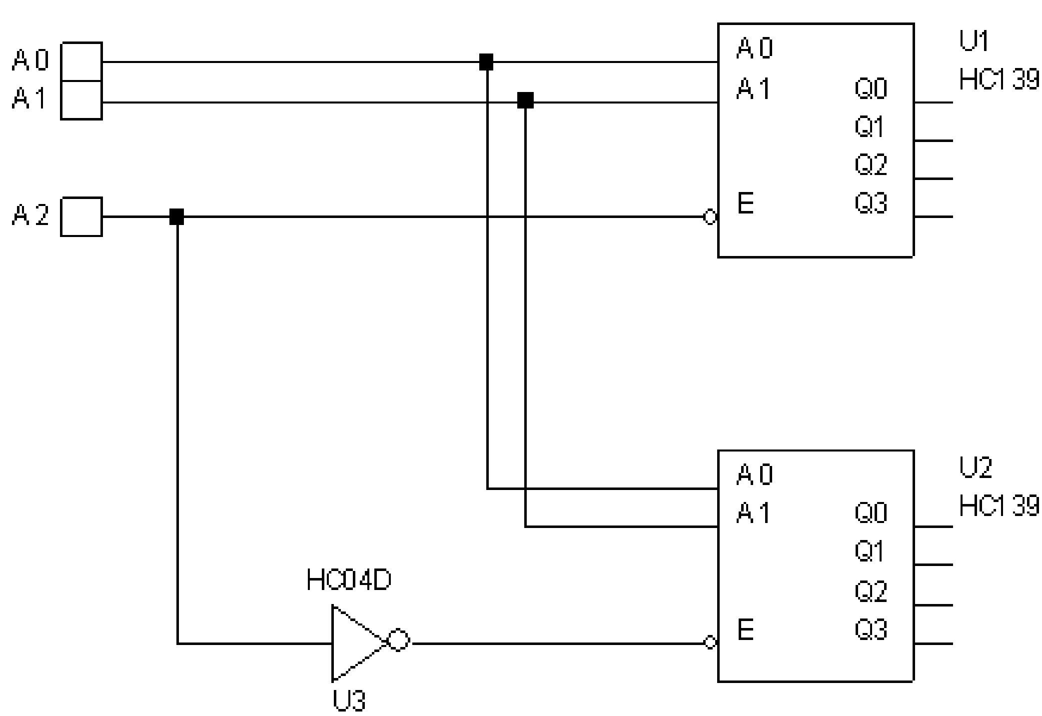
* E এর value 0 হবে, তখন circuit off থাকবে,

E	A	B	D_0	D_1	D_2	D_3
0	X	X	—	—	—	—
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

A	B	E	D_0	D_1	D_2	D_3
0	0					
0	1					
1	0					
1	1					



x	y	z	
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7



07.06.16

* Encoder

$2^n \times n$

inputs, outputs

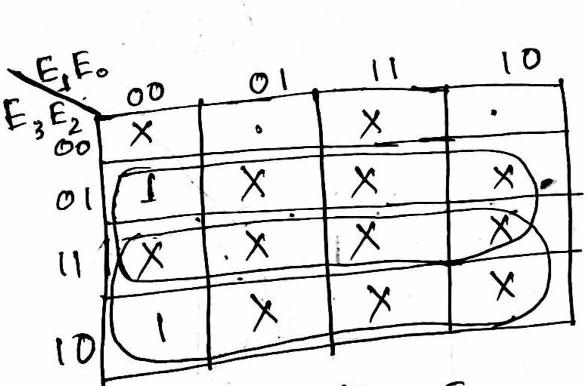
$n = 1$, 2×1

$n = 2$, 4×2

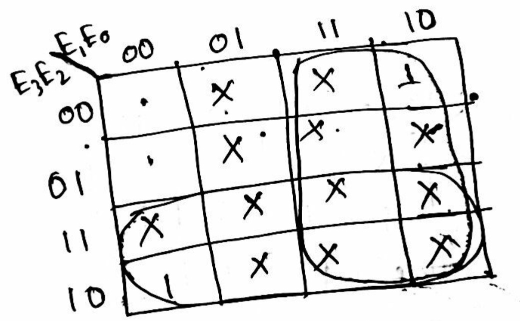
$n = 3$, 8×3

4×2

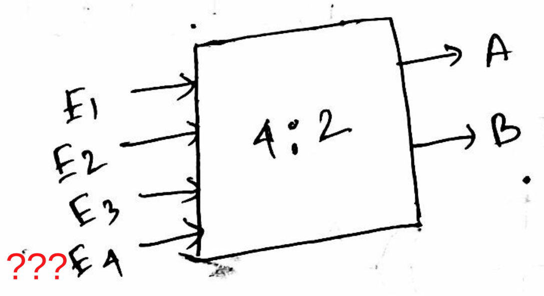
E_3	E_2	E_1	E_0	A	B
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

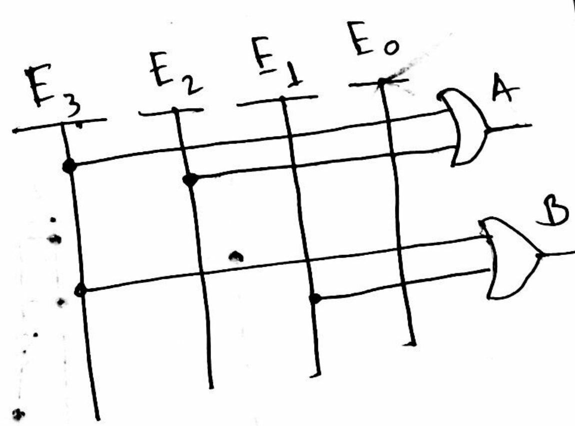


$A = E_3 + E_2$



$B = E_3 + E_1$





Priority Encoder

E_3	E_2	E_1	E_0	A	B
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

$E_3 > E_2 > E_1 > E_0$

001X → 0010, 0011

01XX → 0100, 0101, 0110, 0111

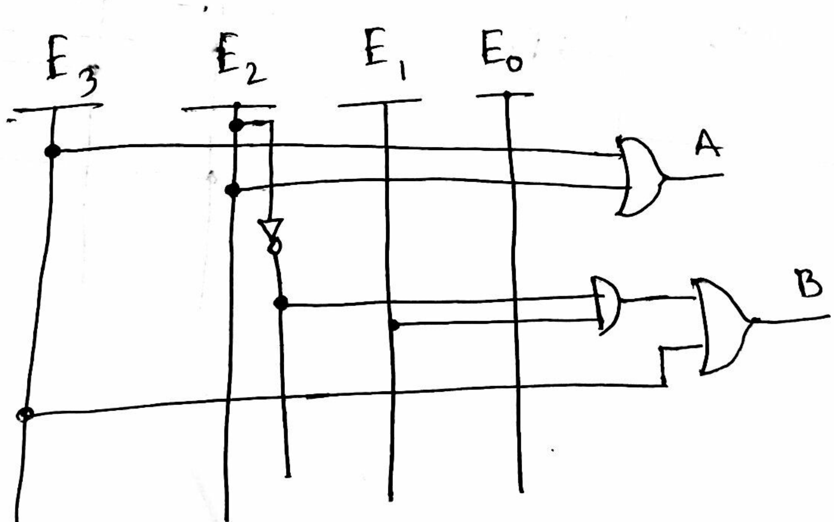
1XXX → 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111

E_3E_2 \ E_1E_0	00	01	11	10
00	X			
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$A = E_3 + E_2$

E_3E_2 \ E_1E_0	00	01	11	10
00	X		1	1
01				
11	1	1	1	1
10	1	1	1	1

$B = E_3 + \bar{E}_2 E_1$



* Implement using one (MUX)

* Multiplexer (MUX)

$2^n \times n \times 1$

2^n → inputs, n → control inputs, 1 → output

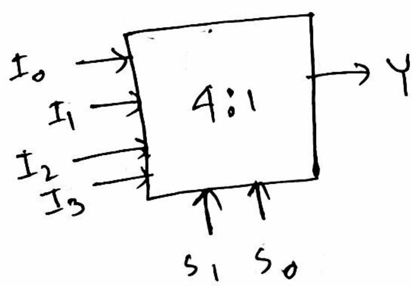
$n = 1, \quad 2 \times 1 \times 1 \approx 2:1$

$n = 2, \quad 4 \times 2 \times 1 \approx 4:1$

$n = 3, \quad 8 \times 3 \times 1 \approx 8:1$

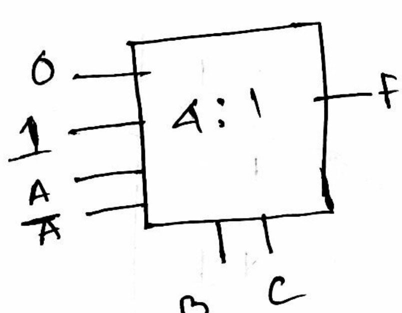
4 : 1

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



000
001
010
011
100
101
110
111

* $F(A, B, C) = \Sigma(1, 3, 5, 6)$



	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	0	1	A	$\bar{A}$

* Implementation Table

13.06.16

* Decimal Adder

final carry out

Binary sum					BCD sum				
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

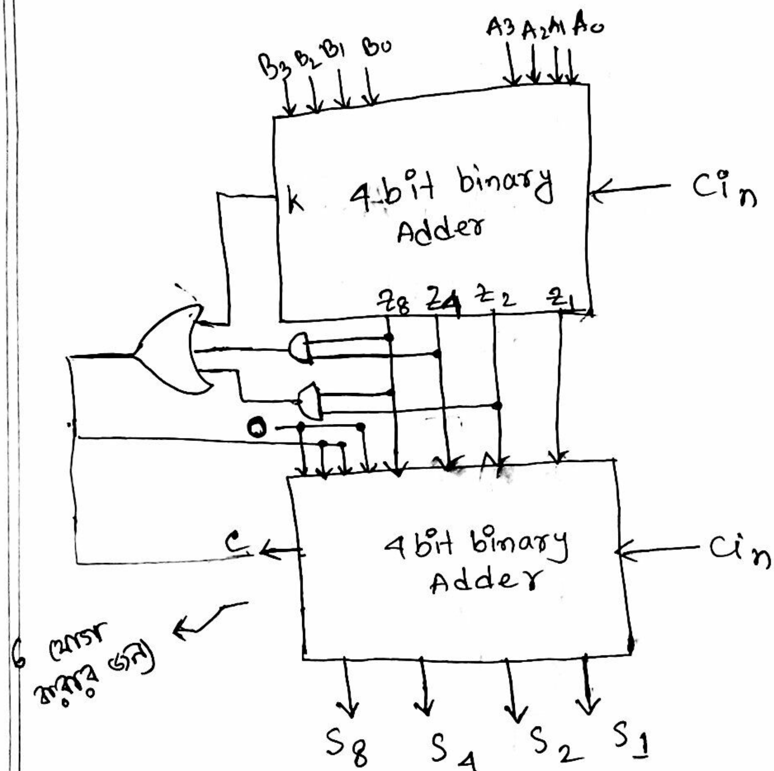
1 0

0.001 0000

10000

$$\boxed{C = K + Z_8 Z_4 + Z_8 Z_2}$$

* design 4-bit decimal Adder



0 1 1 0 → 9 এর বেশি add হবে

0 0 0 0 → 0 এর কম হলে add হবে

* Comparator

$$\left.\begin{array}{l} A > B \\ A < B \\ A = B \end{array}\right\}$$

A	B	$(A=B)= A\odot B$
0	0	1
0	1	0
1	0	0
1	1	1

2 bit

$$\underbrace{(A_1 \odot B_1)}_{x_1} \cdot \underbrace{(A_0 \odot B_0)}_{x_0}$$

$$x = x_1 \cdot x_0$$

3-bit

$$x = x_2 \cdot x_1 \cdot x_0$$

14.06.16

* Comparator

A > B

A	B	F = (A > B)
0	0	0
0	1	0
1	0	1
1	1	0

$F = A\bar{B}$

2 bit

MSB বড় না হলে ছোট সমান হবে। সমান হলে সব bit cheak করতে হবে।

$F = A_1\bar{B}_1 + x_1 A_0\bar{B}_0$

$A_1\ A_0$	1 1
$B_1\ B_0$	0 1
$A > B$	1

$F = A_1\bar{B}_1 + x_1 A_0\bar{B}_0$

$= 1\cdot\bar{0} + 1\cdot\bar{1}$

$= 1\cdot 1 + 1\cdot 0$

$= 1 + 0$

$= 1$

$A =$

0 1
1 0
0

$F = A_1\bar{B}_1 + x_1 A_0\bar{B}_0$

$= 0\cdot\bar{1} + 1\cdot\bar{0}$

$= 0\cdot 0 + 0\cdot 1$

$= 0$

1 0
0 1
1

$F = A_1\bar{B}_1 + x_1 A_0\bar{B}_0$

$= 1\cdot\bar{0} + 0\cdot\bar{1}$

$= 1\cdot 1 + 0\cdot 0$

$= 1$

4 bit

$F = A_3\bar{B}_3 + x_3 A_2\bar{B}_2 + x_3x_2 A_1\bar{B}_1 + x_3x_2x_1 A_0\bar{B}_0$

A < B

A	B	F = (A<B)
0	0	0
0	1	1
1	0	0
1	1	0

$F = \bar{A}B$

A = B

1-bit

$F = A_0 \odot B_0 = x_0$

2-bit

$F = (A_1 \odot B_1) \cdot (A_0 \odot B_0)$

$= x_1 \cdot x_0$

4 bit

$F = x_3 \cdot x_2 \cdot x_1 \cdot x_0$

2-bit

$F = \bar{A}_1 B_1 + x_1 \bar{A}_0 B_0$

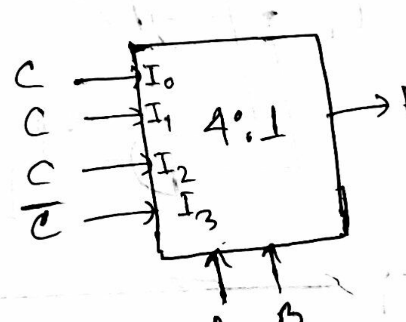
4 bit

$F = \bar{A}_3 B_3 + x_3 \bar{A}_2 B_2 + x_3 x_2 \bar{A}_1 B_1 + x_3 x_2 x_1 \bar{A}_0 B_0$

000
001
010
011
100
101
110
111

* $F(A, B, C) = \Sigma(1, 3, 5, 6)$

	I_0	I_1	I_2	I_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
	C	C	C	$\bar{C}$



21.06.16

* Carry look Ahead Adder

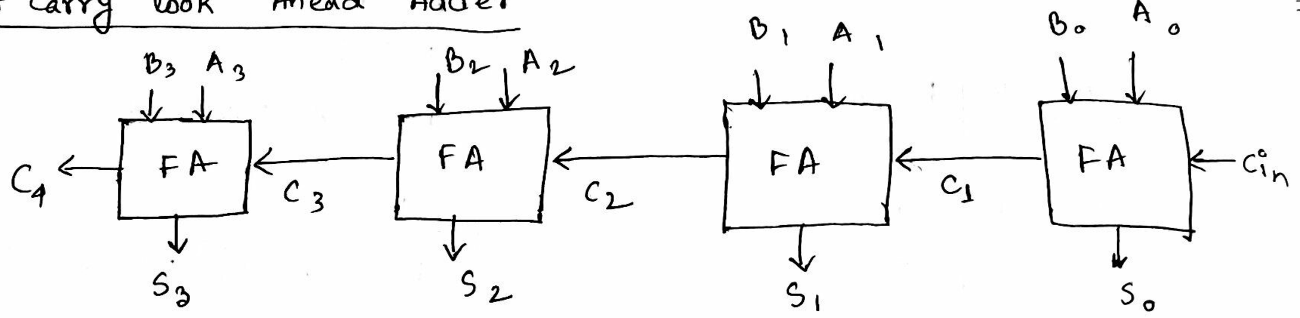
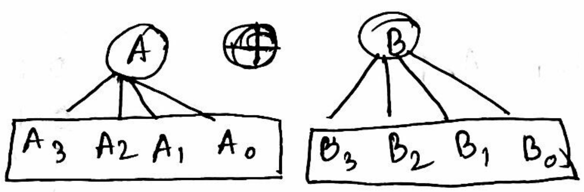


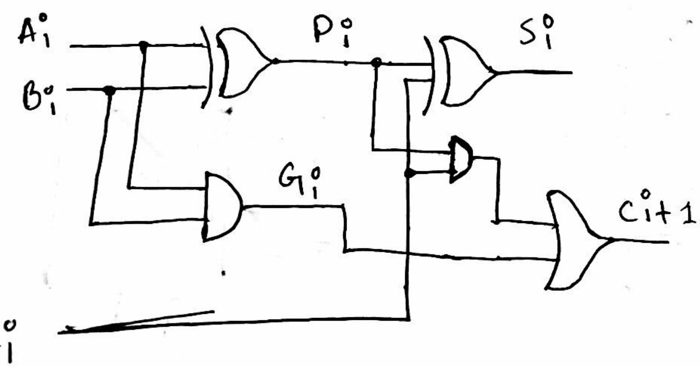
Fig: 4-bit Parallel Adder

disadv : Delay, take too much time when number of bits increased.



$$\begin{array}{cccc} C_3 & C_2 & C_1 & C_0 \\ A_3 & A_2 & A_1 & A_0 \\ B_3 & B_2 & B_1 & B_0 \\ \hline S_3 & S_2 & S_1 & S_0 \\ C_4 & C_3 & C_2 & C_1 \end{array}$$

$i = 0 \cdots 3$



$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i$

$\therefore S_i = A_i \oplus B_i \oplus C_i = P_i \oplus C_i$

$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i$

$C_{i+1} = G_i + P_i C_i$, $i=0$, $C_1 = G_0 + P_0 C_0$

4-bit Addition

$C_0 = 0$

$i = 0, \quad C_1 = \boxed{G_0 + P_0 C_0}$

$i = 1, \quad C_2 = G_1 + P_1 C_1$

$= G_1 + P_1 (G_0 + P_0 C_0)$

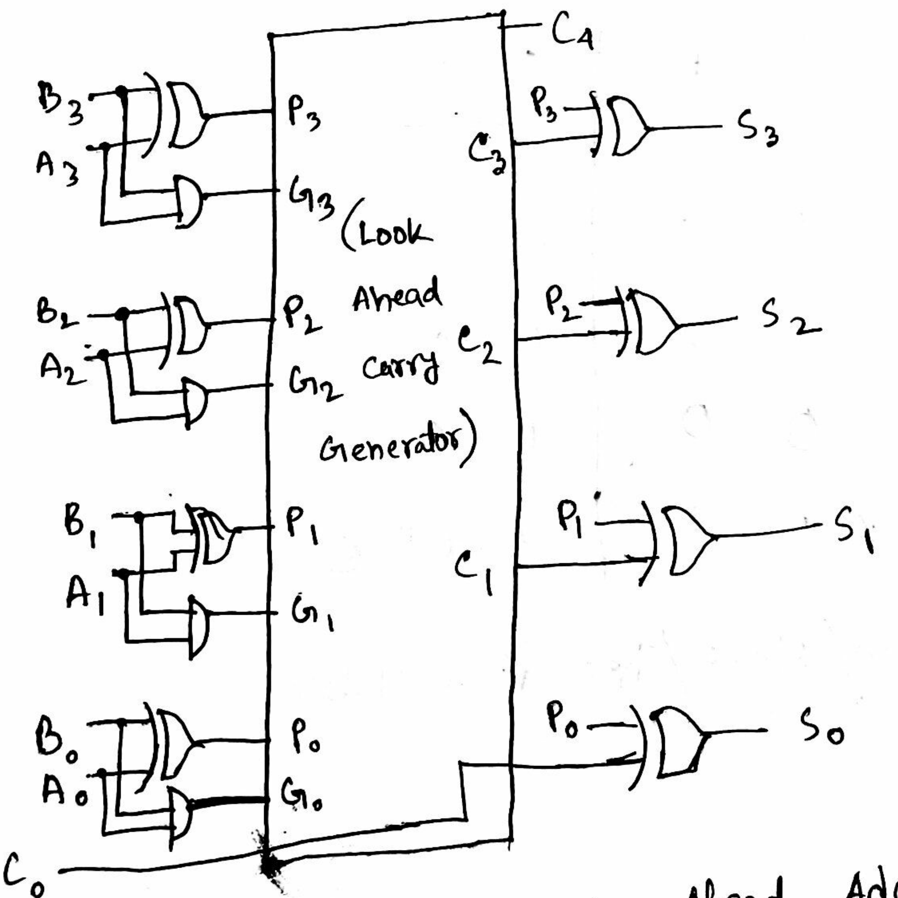
$= \boxed{G_1 + P_1 G_0 + P_1 P_0 C_0}$

$i = 2, \quad C_3 = G_2 + P_2 C_2$

$= \boxed{G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0}$

$i = 3, \quad C_4 = G_3 + P_3 C_3$

$= \boxed{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0}$



4bit Carry Look Ahead Adder

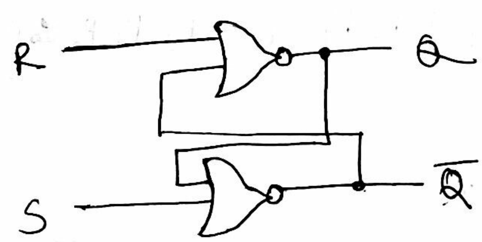
...er Boar.l 2N30 ...tion

* cross couple circuit এর শুরুতে initial value দিতে হয়।

* sequential Circuits

- Cross coupled circuit
- flip-flop
  - → S-R
  - → D
  - → J-K
  - → T

*cross couple ckt NOR/ ...



S	R	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
0	0	1	0
0	0	1	0
× 1	1	undefined	

Truth/state/Transtion Table

* output এ 1 value set করতে হবে।

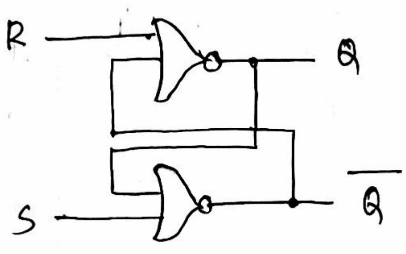
* 00/11 হবে না

* যেই output এ 0 থাকবে, সেটা আগে start হবে।

22.06.16

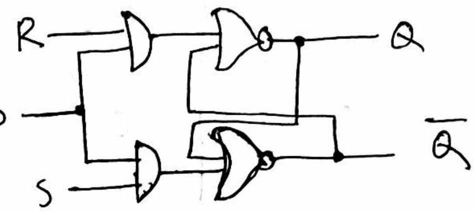
* S-R Latch

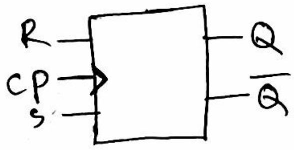
cross couple ckt NOR/NAND দিয়ে হয়।



S	R	Q	$\overline{Q}$
1	0	1	0
0	0	1	0
0	1	0	1
1	1	–	–

* S-R ~~flip~~ flip-flop



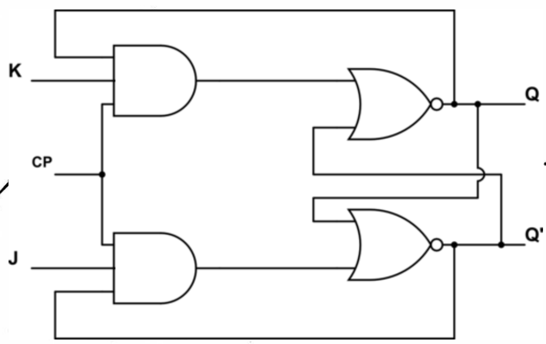


positive ← CP

State table (characteristic Table)

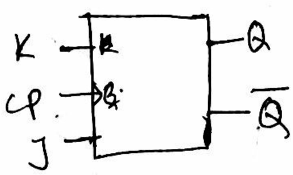
S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	–

* J-K flipflop



Clock ← pulse

control input ↓ flip-flop activate করে।



Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	X → don't care
0	1	1	0
1	0	0	1
1	1	X	0

component.

* flip-flop onekind of memory device
* 1টা flip-flop 1bit hold করে
* flip-flop এ output fixed, input এর expression বের করতে হবে.

* 13.07.16 – Quiz-2
MUX
Decoder

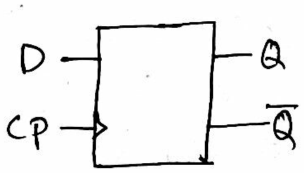
State table

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}(t)$

Excitation table

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

* D flip flop



Present time = t+1

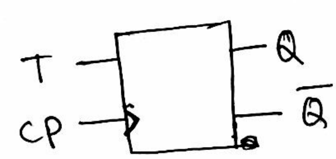
D	Q(t+1)
0	0
1	1

output, Previous output → Q(t); D → input

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

* যার input দিবো, তাই দেখো → buffer gate
↓D-flipflop

T flip-flop



T	Q(t+1)
0	Q(t) → Previously যা set করা ছিল
1	$\overline{Q}(t)$

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

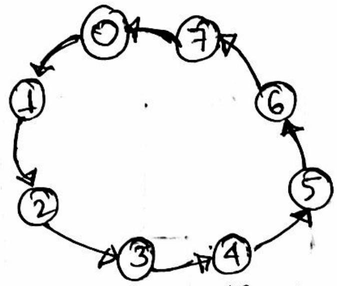
0 দিলে previous টাই থাকবে।
1 দিলে " " উল্টায় যাবে।

* seq ckt → input, output both ই dependent
* 3bit up counter ckt design (state diagram থেকে করব)
* 3bit down counter ckt

* state diagram দিয়ে counter ckt design করব

12·07·16

(*)



State diagram

state diagram থেকে excitation table করতে হবে →

Previous state/output			Input		
A_2	A_1	A_0	TA_2	TA_1	TA_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	0	0	1
1	1	1	1	1	1

Excitation Table

A_2 \ A_1A_0	00	01	11	10
0			1	
1			1	

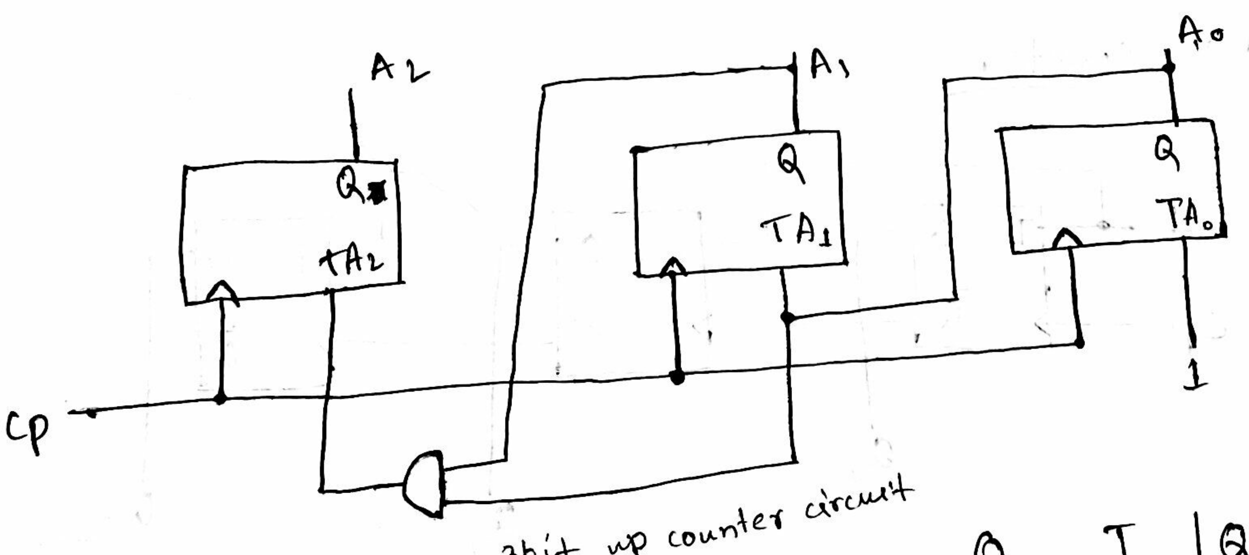
$TA_2 = A_1 A_0$

A_2 \ A_1A_0	00	01	11	10
0		1	1	
1		1	1	

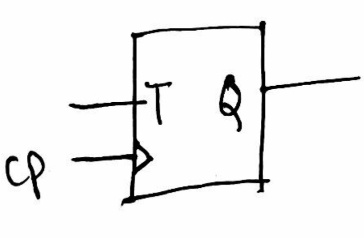
$TA_1 = A_0$

A_2 \ A_1A_0				
	1	1	1	1
	1	1	1	1

$TA_0 = 1$



3bit up counter circuit



Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

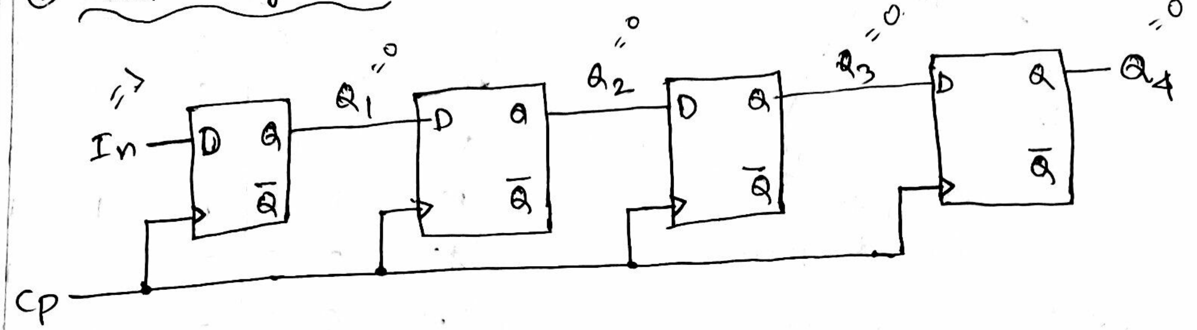
Excitation Table

Specif

* D-flipflop এর timing diagram দেখো ।

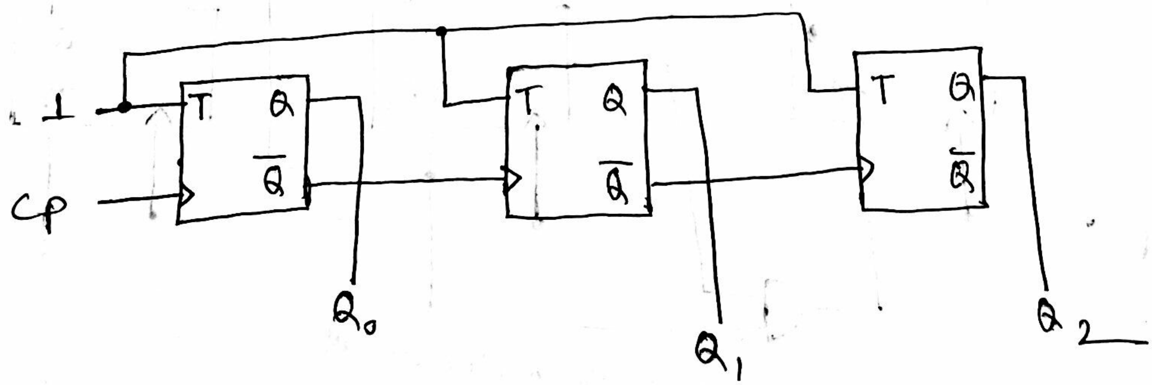
18.07.16 ~~12.07.16~~

Shift Register



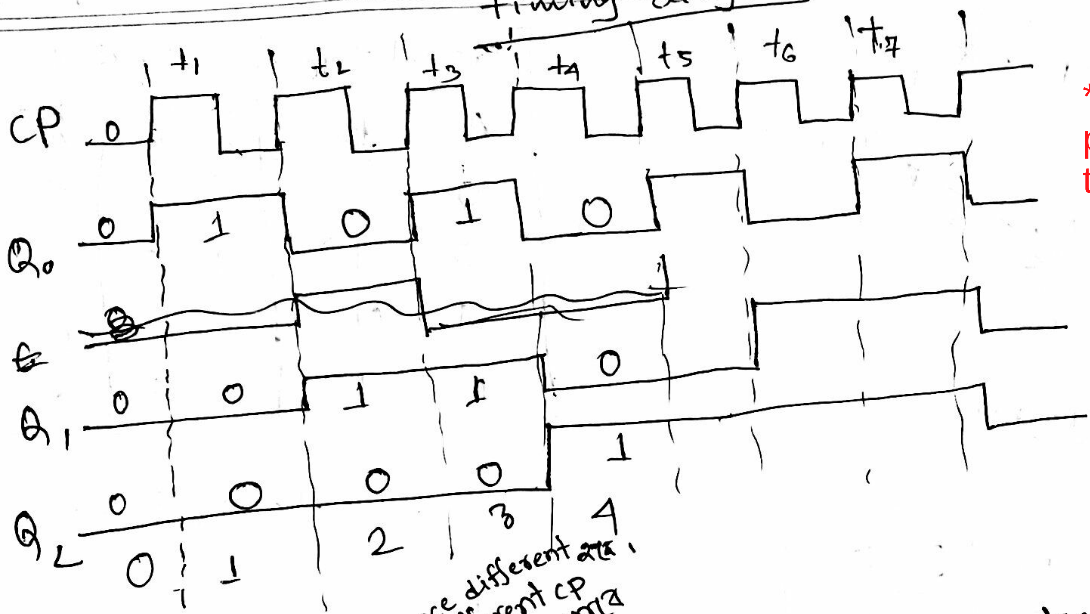
	I_n	Q_1	Q_2	Q_3	Q_4
→ initial		0	0	0	0
t_0 →	1	1	0	0	0
t_1 →	0	0	1	0	0
t_2 →	1	1	0	1	0
t_3 →	1	1	1	0	1

* Up counter



* clock start হয় (+ve) pulse থেকে
circuit এর output, timing diagram এর মাধ্যমে দেখাও,
* 7টি cp এর জন্য timing diagram দেখাও।

timing diagram



*This is definitely positive edge triggered

Clock pulse এর basis এ classification

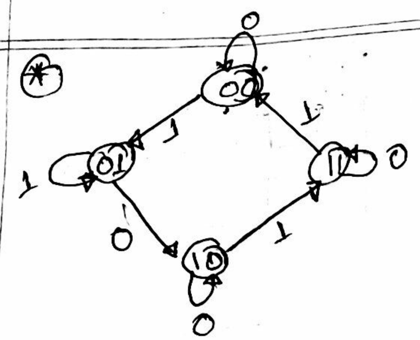
— Asynchronous circuit
— Synchronous circuit
source same একই cp-পাবে।

J-K

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

19.07.16



State Diagram

Present state A	Present state B	Next state x = 0: A	Next state x = 0: B	Next state x = 1: A	Next state x = 1: B
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

State Table

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

A \ Bx	00	01	11	10
0				1
1	X	X	X	X

$JA = B\bar{x}$

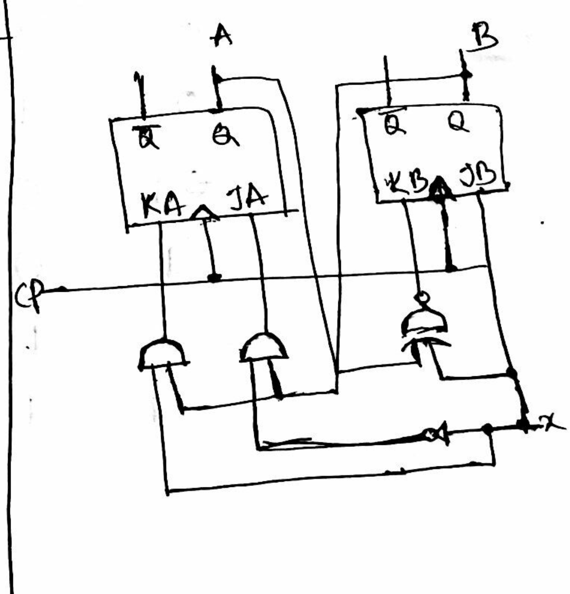
$KA = Bx$

$JB = x$

$KB = A \odot \cancel{x}$

Present state A	Present state B	input x	Next state A	Next state B	JA	KA	JB	KB
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	~~X~~	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Excitation table

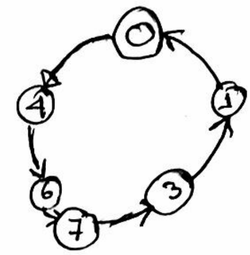


* Quiz - 3 (1/08/16)
- simple counter implementation using J-K/T/D flip-flops

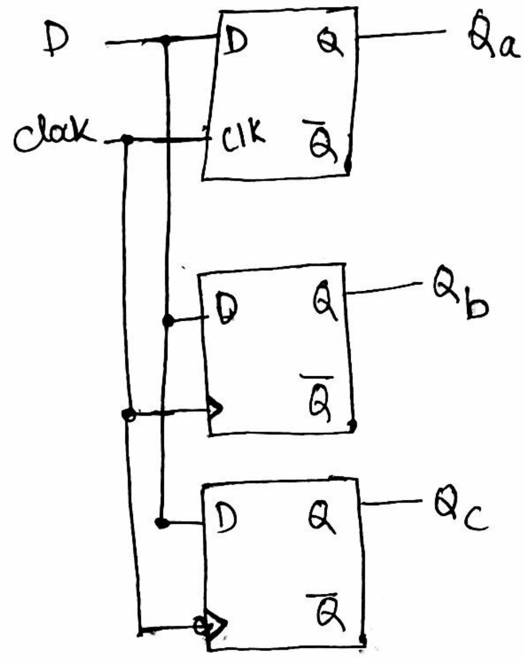
25.07.16

* Johnson Counter → 3bit Johnson counter →

0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	0	0



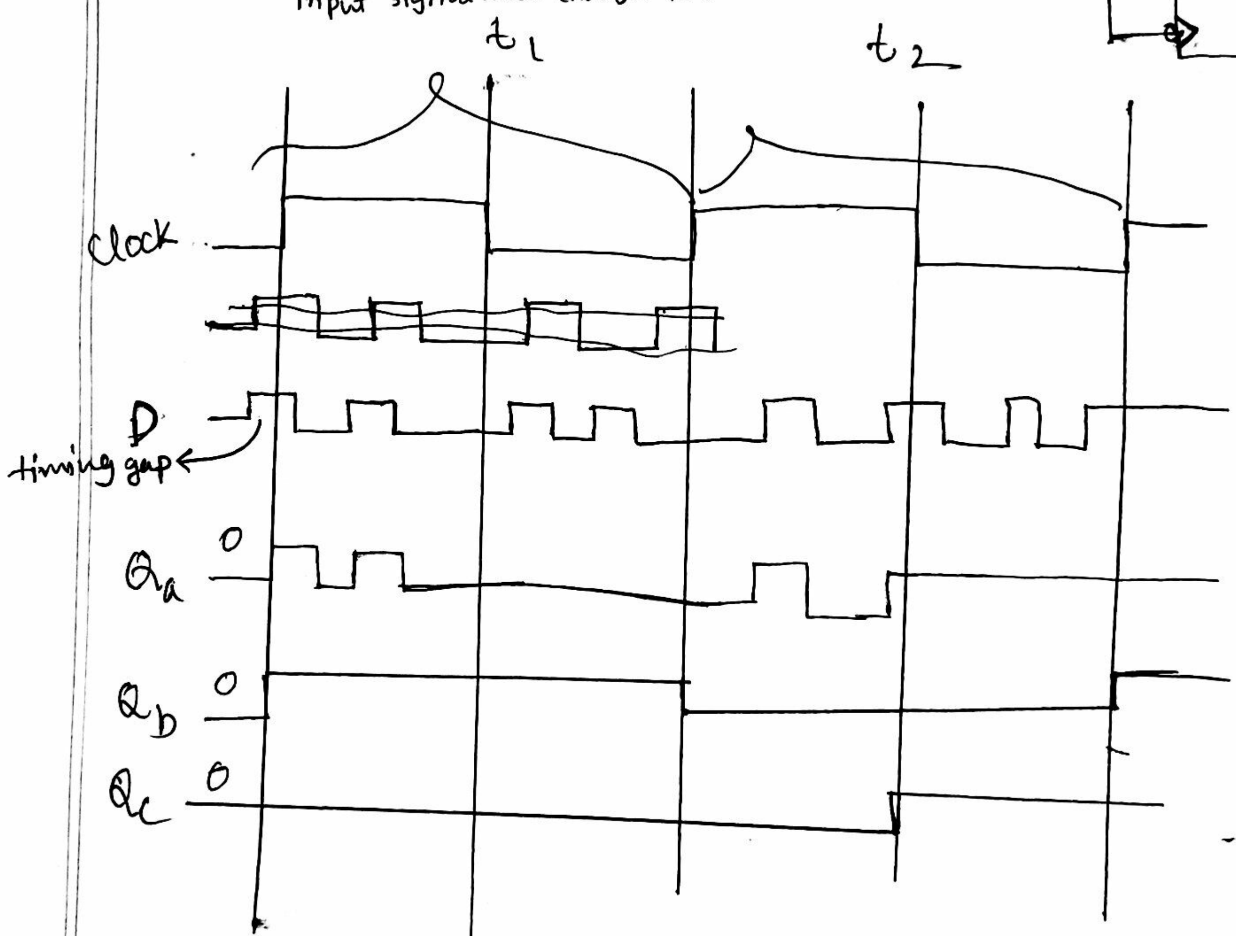
* BCD counter
* up counter
* Down counter



* Clock types

- Positive Edge triggered
- Negetive Edge triggered
- level sensitive (—clk)

* level → positive cycle এ active হবে শুধু।
→ last এ যেই input থাকবে সেটাই হবে।
→ Input signal wise change হবে।



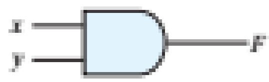
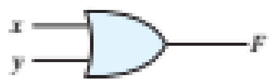
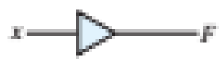
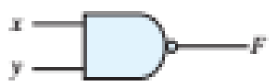
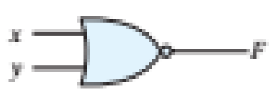
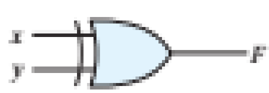
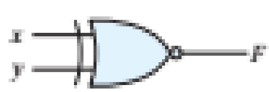
*level sensitive

Quiz - 4

11.08.16 → 1.50pm — 7A06

sequential circuit → timing diagram

~~27.07.16~~

Name	Graphic symbol	Algebraic function	Truth table
AND		$F = x \cdot y$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = x + y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
Inverter		$F = x'$	x | F 0 | 1 1 | 0
Buffer		$F = x$	x | F 0 | 0 1 | 1
NAND		$F = (xy)'$	x y | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = (x + y)'$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	x y | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	x y | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1