AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, FALL-2012

COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

Time: 03 Hours | Full Marks: 210

There are EIGHT (8) questions. Answer any SIX (6)

1. a) Explain Small Signal Model of diode. [10]
   b) For the clipper circuit shown in fig-1(b) draw the output wave shape with appropriate equation. [20]
   c) Determine the current I in the circuit shown in Fig-1(c).Assume the diode to be of silicon diode and forward resistance of diodes to be zero. [05]

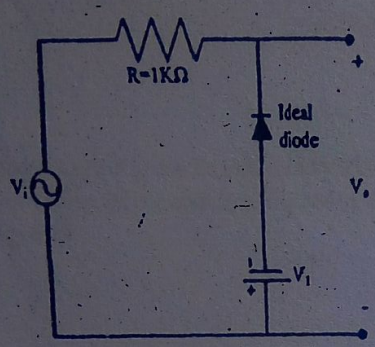

Fig:-1(b)

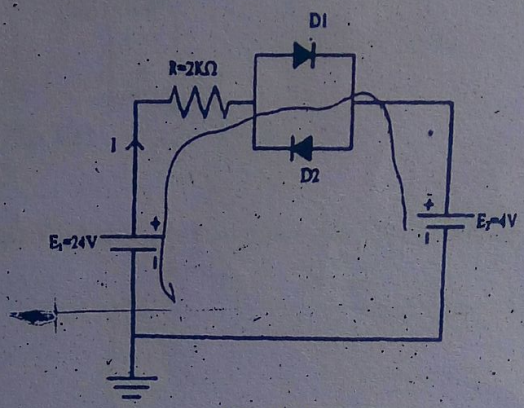

Fig:-1(c)

2. a) For a Full Wave Rectifier circuit, derive the expression of average and RMS Voltage. [15]
   b) Assuming the diode to be ideal, find the values of I and V from the circuit shown in fig-2(b) [18]
   c) For the Zener diode network of Fig-2(c),determine V_L , V_R , I_Z, P_Z [02]

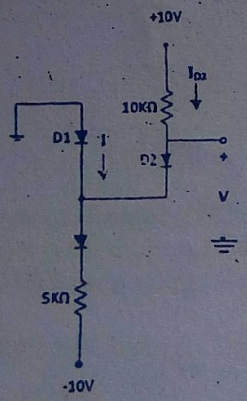

Fig-2(b)

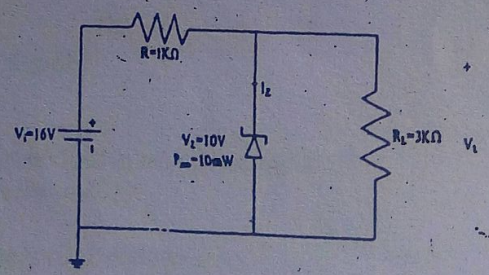

Fig-2(c)

3. a) For the following voltage-divider network shown in fig- 3(a) determine: a) V_{CE} b) I_C (Consider β=100) [18]

b) Describe Small signal model (hybrid pi) for BJT ac Signal analysis. [17]

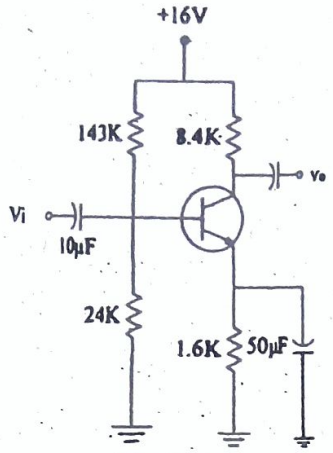

Fig- 3(a)

4. a) How a transistor can be used as a switch? [17]

b) Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base Configuration of fig- 4(b) [18]

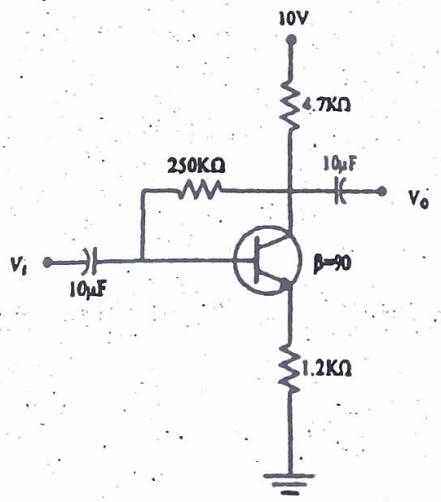

Fig-4(b)

5. a) Write down the advantages of FET over BJT [15]

b) In your own words, briefly explain the basic operation of an enhancement type MOSFET. [10]

c) Why MOSFET can be called as a voltage controlled switch? [10]

6. a) Briefly describe the Hartley Oscillator with circuit diagram and prove that [20]

$$f = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

b) A 1mH inductor is available. Choose the capacitor values in a Colpitt's oscillator so that f=1MHz and m_v=0.25 [15]

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2ND YEAR 1ST SEMESTER, CARRY/CLEARANCE/IMPROVEMENT, FALL-2012
COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

TIME: 3 HRS FULL MARKS: 210

There are EIGHT (8) questions. Answer any SIX (6)

1. a) Briefly explain small signal model for diode. [15]
   b) Determine I and V for the circuit in fig-1(b) [05]
   c) Determine V for the circuit in fig-1(c) [15]

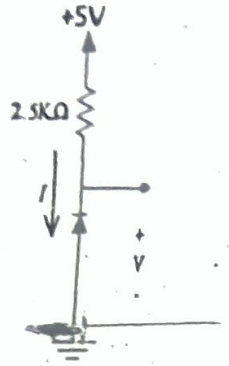

Fig-1(b)

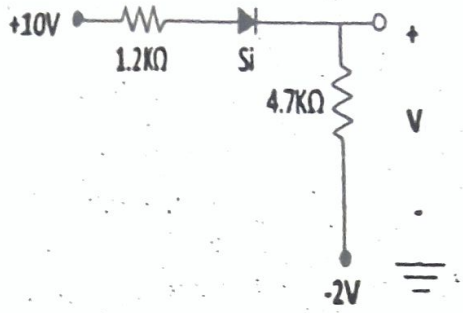

Fig-1(c)

2. a) For a Sinusoidal input derive the RMS and DC voltage equation for a Half wave Bridge rectifier. [15]
   b) For the clipper circuit shown in fig-2(b) draw the output wave shape with appropriate equation. [15]
   c) Write down the advantages of half wave and full wave rectifiers. [05]

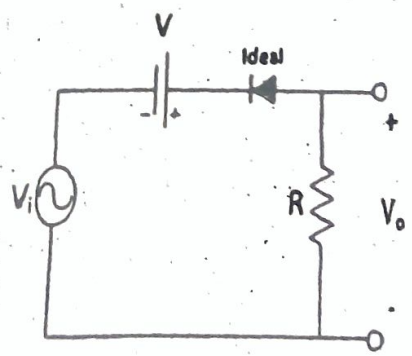

Fig-2(b)

3. a) How we can use a transistor as an amplifier? In BJT how can you change its Q-point? [15]
   b) For the following voltage-divider network shown in fig-3(b) determine: [20]
   a) V_{CE} b) I_C (Where β=100)

Fig:- 3(b)

4. a) For the following circuit in Fig:-4(a) find the Q- point. Given β=100, R_B=62 KΩ, R_C=375Ω, V_{BB}=10 V, V_{CC}=15 V, and V_{BE}=0.7 V. Also prove that the BJT is in active mode. [15]

(b) Prove with necessary circuit diagram and equations that fixed bias is β dependent but self bias is β independent [20]

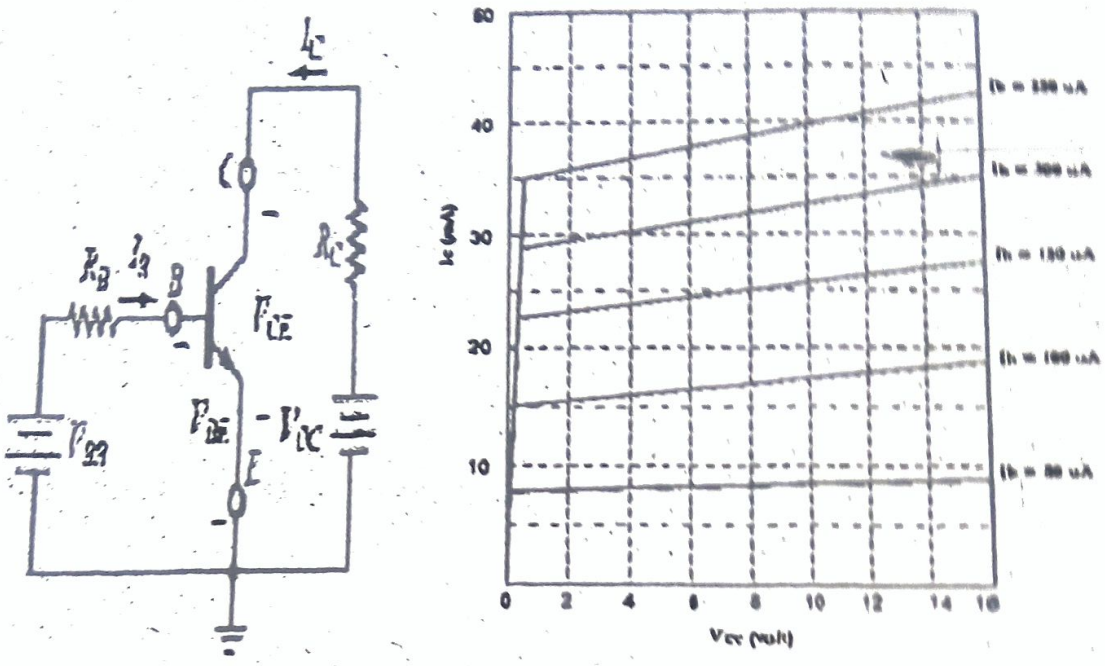

Fig:-4(a)

5. (a) What is FET? Give the classification of FET. Briefly explain the basic operation of JFET. [25]

(b) In your own words, briefly explain the basic operation of a Depletion type MOSFET. [10]

6. (a) Briefly describe the Wien Bridge oscillator and give its advantages and disadvantages. [17]

(b) Draw the circuit diagram of Hartley Oscillator. [18]

Given that L_1=1000μH, L_2=100μH, C=20pF. Calculate:

(i) operating frequency and

(ii) Feedback fraction for Hartley oscillator. The mutual inductance between the coils, M=20μH.

Write short notes on:

a) Application of Silicon Controlled Rectifier. [35]
b) Unijunction transistor.
c) Advantages of TRIAC over SCR.

a) Write down IC fabrication steps and briefly explain the process. [25]
b) Show that DIAC-TRIAC combination can be used for load power control. [10]

COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

TIME: 3 HRS FULL MARKS: 210

There are EIGHT (8) questions. Answer any SIX (6)

1. (a) Briefly explain small signal model for diode. [10]
   b) Determine the currents I_1, I_2 and I_{D_2} for the network of Fig:-1(b) [15]
   c) Determine the current I_1 for the circuit in Fig:-1(c) [10]

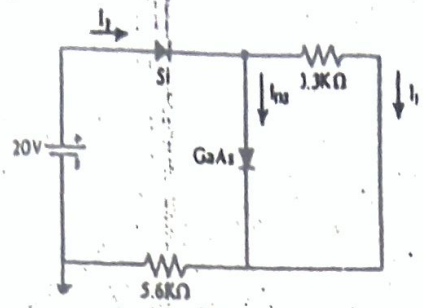

Fig-1(b)

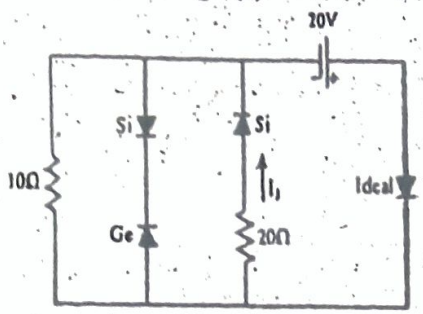

Fig-1(c)

2. a) For a Sinusoidal input derive the RMS and DC voltage equation for a Full wave Bridge rectifier. [18]
   b) For the network in Fig:-2(b), determine the range of R_L and I_L that will result V_{RL} being maintained at 10 V. [17]

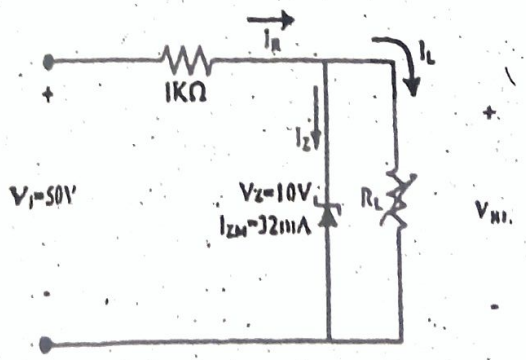

Fig-2(b)

3. a) For the network in fig:-3(a) determine (i)r_e (ii)Z_i (iii)Z_o (iv)A_v (Consider $r_o=\infty\ \Omega$) [17]
   b) For the following voltage-divider network shown in fig:- 3(b) determine:- [18]
   a) V_{CE} b)I_C (Where β=100)

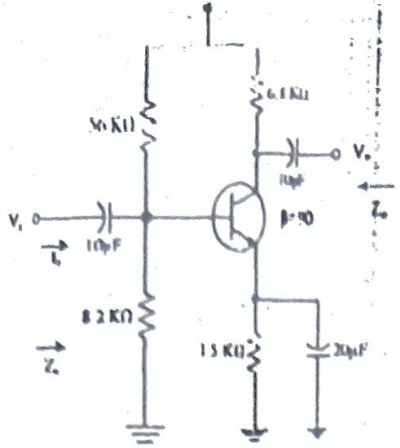

Fig-3(a)

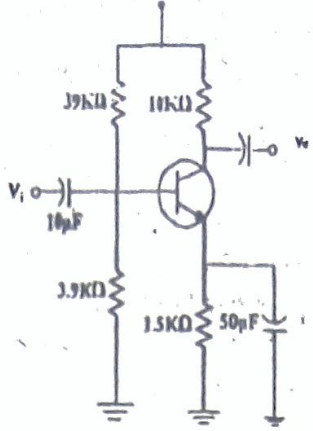

Fig-3(b)

4. a) Compare different characteristics of BJT, Enhancement type MOSFET and Depletion type MOSFET [18]
   b) In your own words, briefly explain the basic operation of an Enhancement type MOSFET [17]

5. a) Explain Barkhausan criterion for a basic sinusoidal oscillator structure. [15]
   b) Show that for a Colpitts oscillator, we need to ensure $g_m R > C_2/C_1$ to start oscillation; and frequency of the oscillation is $\omega_0 = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$ [20]

6. a) Write down Thyristor turn on techniques [20]
   b) If the converter of Fig:-6(b) has purely resistive load R and delay angle $\alpha = \frac{\pi}{2}$, determine [10]
   (a) the rectification efficiency, (b) the form factor (FF), (c) Ripple Factor (RF), (d) the TUF and (c) the peak inverse voltage (PIV) of the thyristor T_1
   c) Can you make a TRIAC using two thyristor? Explain. [05]
   Draw the I-V characteristics curve of a TRIAC

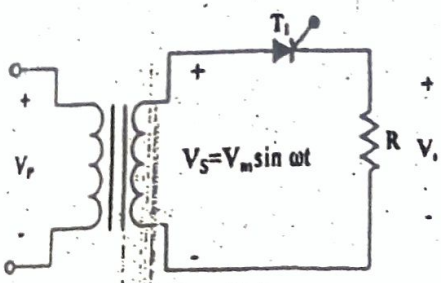

Fig:-6(b)

7. a) What is Noise Margin of a Digital Logic inverter? Explain with a voltage Transfer Characteristics (VTC) [15]
   b) Find the Dynamic Power Dissipation of the inverter in fig:- 7(b). The inverter is switched at 50MHz [5]
   c) Explain Photolithography and Chemical Vapor Disposition (CVD) process in VLSI fabrication process. [15]

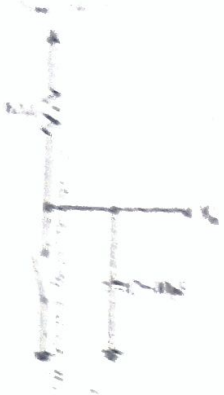

Fig. 7(b)

8. a) Sketch.
transistor equivalent potential diagram, energy band diagram, particle flow diagram of P-N junction when applied with a i)forward bias ii)No Bias [15]

b) Explain why CMOS inverter have no static power dissipation. [10]

c) Explain with I-V characteristics curve how a thyristor differ from a diode. [10]

TIME: 3 HRS FULL MARKS: 210

There are EIGHT (8) questions. Answer any SIX (6)

1. a) Briefly explain small signal model for diode. [10]
   b) Determine the currents I_1, I_2 and I_{D_2} for the network of Fig:-1 (b) [15]
   c) Determine the current I_1 for the circuit in Fig:-1(c) [10]

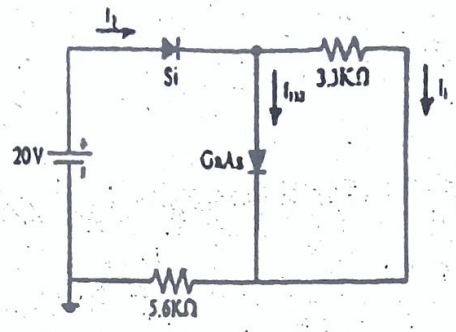

Fig-1(b)

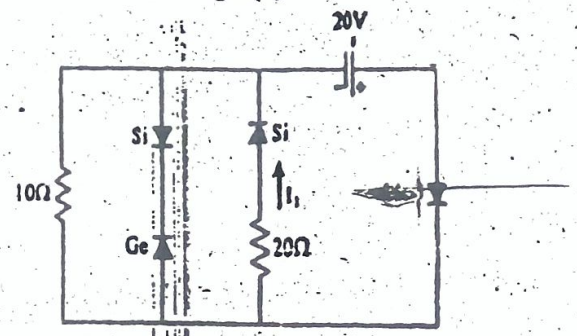

Fig-1(c)

2. a) For a Sinusoidal input derive the RMS and DC voltage equation for a Full wave Bridge rectifier. [18]
   b) For the network in Fig:-2(b), determine the range of R_L and I_L that will result V_{RL} being maintained at 10 V. [17]

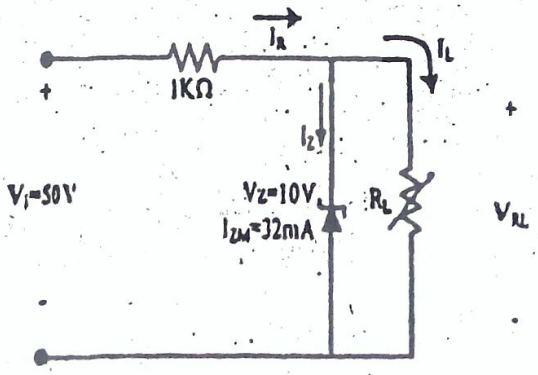

Fig-2(b)

3. a) For the network in fig:-3(a) determine (i)r_e (ii)Z_i (iii)Z_o (iv)A_v (Consider $r_o=\infty\ \Omega$) [17]
   b) For the following voltage-divider network shown in fig:- 3(b) determine:- [18]
   a) V_{CE} b)I_C (Where $\beta=100$)

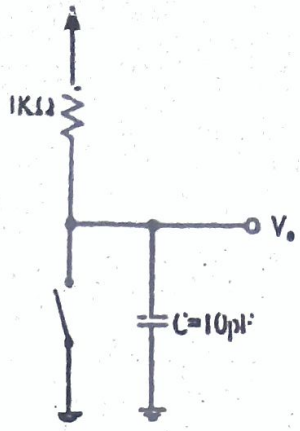

Fig:-7(b)

8. a) Sketch: [15]
transition region , electrostatic potential diagram , energy band diagram, particle flow diagram of a P-N junction when applied with a i)forward bias ii)No Bias

b) Explain why CMOS Inverter have no static power dissipation. [10]

c) Explain with I-V characteristics curve how a thyristor differ from a diode. [10]

COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

TIME: 3 HRS FULL MARKS: 210

There are EIGHT (8) questions. Answer any SIX (6)

1. a) Sketch Transition region , electrostatic potential diagram , energy band diagram, particle flow diagram of a P-N junction when applied with a i)Forward bias ii)Reverse bias(Explain how current flow in forward bias but stops at reverse bias in a P-N junction) [20]

   b) For the clipper circuit shown in fig-1(b) draw the output wave shape with appropriate equation. [15]

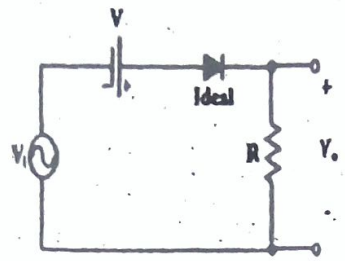

Fig:-1(b)

2. a) Determine V for the circuit shown in fig-2(a). [17]

   b) Determine the range of values of V_i that will maintain the Zener diode of the circuit given in Fig- 2(b) in "on" [18]

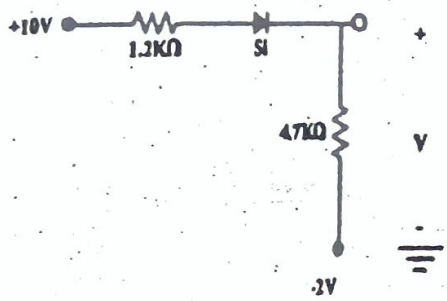

Fig-2(a)

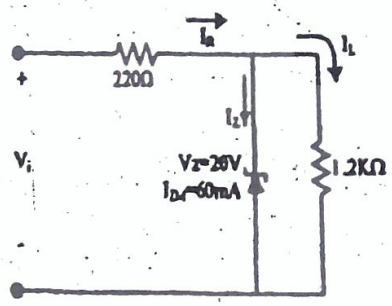

Fig-2(b)

3. a) Determine the currents I_E and I_B and the voltage V_{CE} and V_{CB} for the common-base configuration of Fig 3(a) [15]

   b) Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network given in fig 3(b) [20]

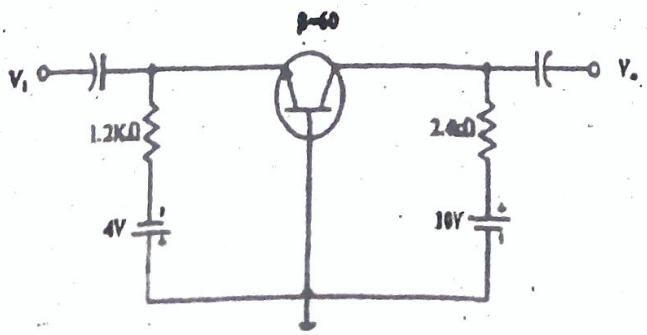

Fig-3(a)

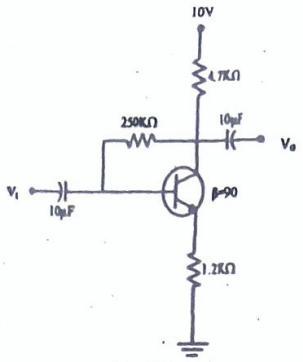

Fig-3(b)

4. a) Write down 5 advantages of using MOSFET instead of BJT. [10]
   b) The emitter-bias configuration of fig:-4(b) has the following specification [20]
   $I_{C_Q} = \frac{1}{2} I_{sat}$, $I_{sat} = 8mA$, V_c=18V. Determine R_C, R_E, R_B
   c) Why MOSFET can be called as a voltage controlled switch? [05]

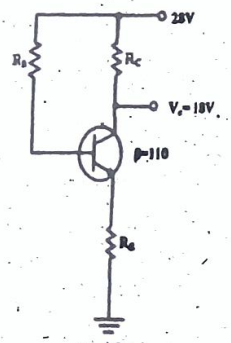

Fig-4(b)

5. a) Explain Barkhausan criterion for a basic sinusoidal oscillator structure. [10]
   b) Show that for a Hartley oscillator we need to ensure $g_m R > L_1/L_2$ to start oscillation; then it will oscillate at a frequency of $\omega_0 = \frac{1}{\sqrt{(L_1+L_2)C}}$ [20]
   c) Design the RC elements of a Wien bridge oscillator for operation at $f_o = 10\ kHz$ [05]

6. a) Using two transistor model explain why even after turning off the gate current of a thyristor it keeps on conducting current from anode to cathode. [20]
   b) Design the triggering circuit of fig-6(b). The parameters of the UJT are V_s=30V, η=0.51, I_p=10μA, V_v=3.5V, and I_v=10mA. The frequency of oscillation is f=60Hz and the width of the triggering pulse is t_g=50μs. Assume V_D=5V, C=0.5μF [15]

29 September 2013

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY
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2ND YEAR 1ST SEMESTER, CARRY/CLEARANCE/IMPROVEMENT, SPRING - 2013
COURSE NO: EEE-2141/EEE-211 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

Full Marks:-210 Time :-3 Hours

Use separate script for each section

SECTION-A

There are 4(Four) questions in this section. Answer any 3(Three) questions.

1. a) Sketch Transition region , electrostatic potential diagram , energy band diagram , particle flow diagram of a P-N junction when applied with a i)Forward bias ii)Reverse bias. Explain how current flow in forward bias but stops at reverse bias in a P-N junction. [18]
   b) Determine V_O wave shape for the network of fig:-1(b) for the input indicated [17]

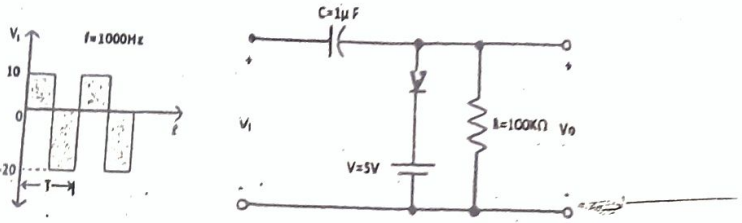


Fig-1(b)

2. a) Determine I, I_1 and V for the circuit shown in fig-2(a). [10]
   b) Determine I_1, I_2 and I_{D2} for the circuit shown in fig-2(b). [10]
   c) Determine the range of values of V_i that will maintain the Zener diode of the circuit given in Fig- 2(c) in "on" [15]

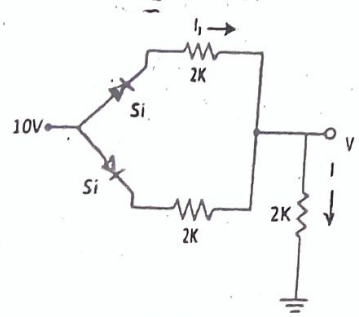


Fig-2(a)

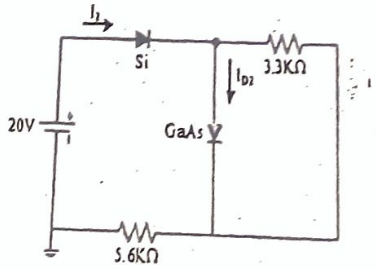


Fig-2(b)

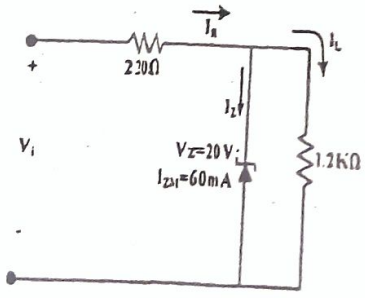


Fig-2(c)

a) For the following circuit sown in fig-3(a) determine:-
   a) r_e b)Z_i c)Z_o d)A_v (where $\beta=100$ and $r_0=\infty$) [17]
b) For the following voltage-divider network shown in Fig- 3(b) determine:-
   a) V_{CE} b)I_C (Where $\beta=100$) [18]

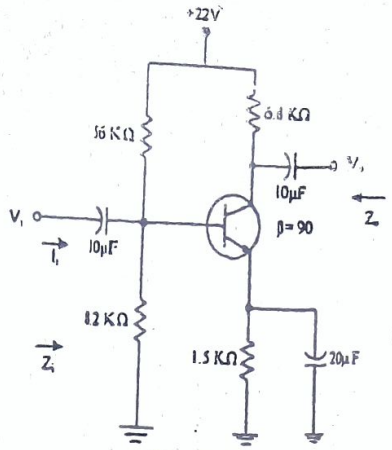


Fig-3(a)

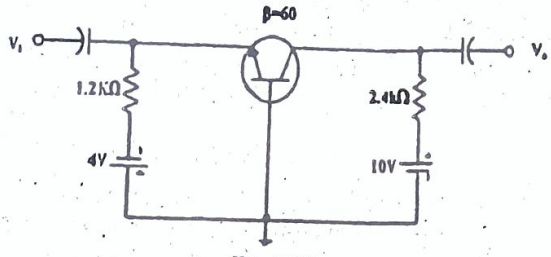


Fig-3(b)

4. a) Write down 5 advantages MOSFET over BJT. [10]
   b) In your own words, briefly explain the basic operation of an Enhancement type MOSFET [20]
   c) We have two logic gates in fig-4(C_1) and fig-4(C_2). Consider A and B as input and Y as output. Write down the truth table for the circuits. (You can also consider +5V as logic '1' and 0V as logic '0') [05]

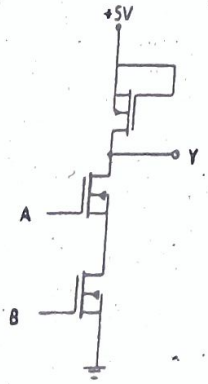


Fig-4(C_1)

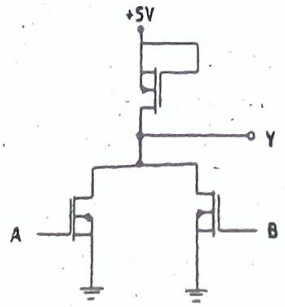


Fig-4(C_2)

SECTION-B

There are 4(Four) questions in this section. Answer any 3(Three) questions

a) What do you understand by the word Oscillator? How can you classify the oscillators? Explain "Barkhausan" criterion for a basic sinusoidal oscillator structure. [15]

b) Briefly describe the Hartley Oscillator with circuit diagram and prove that [15]

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

c) What are the basic differences between Colpitts and Hartley Oscillator? Draw the necessary circuit diagram for both of them. [05]

a) Write down "Thyristor" turn on techniques. How can you turn off a Thyristor? [20]

29th March 2014

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, FALL -2013
COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

Full Marks:-210 **Time :-3 Hours**

There are EIGHT (8) questions. Answer any SIX (6)

1. a) Sketch Transition region , electrostatic potential diagram , energy band diagram, particle flow diagram of a P-N junction when applied with a i)Forward bias ii)Reverse bias. Explain how current flow in forward bias but stops at reverse bias in a P-N junction. [20]

b) Determine the currents I_1, I_2 and I_{D_2} for the network of Fig:-1(b) [15]

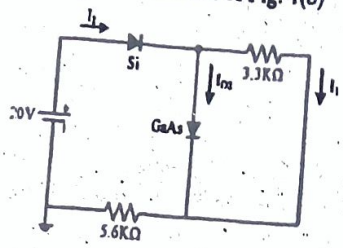


Fig-1(b)

2. a) For the network in Fig:-2(a), determine the range of R_L and I_L that will result V_{RL} being maintained at 10 V. [18]

b) For the clipper circuit shown in Fig-2(b) draw the output wave, V_o with appropriate equation [17]

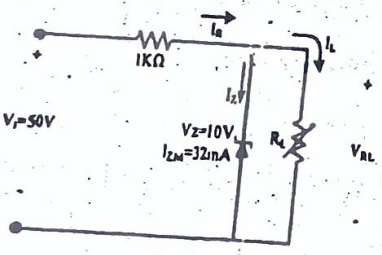


Fig:-2(a)

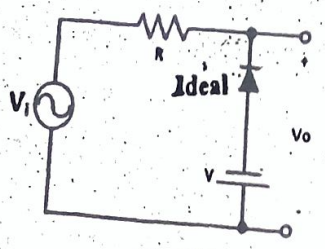


Fig:-2(b)

3. a) For the following voltage-divider network shown in Fig:- 3(a) determine:-
a) V_{CE} b)I_C (Where β=100) [17]

b) For the following circuit shown in Fig-3(b) determine:-
a) r_e b)Z_i c)Z_o d)A_v (where β=100 and r_0=∞) [18]

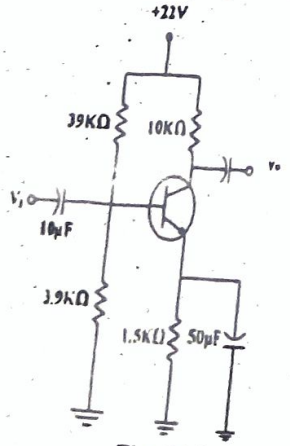


Fig:-3(a)

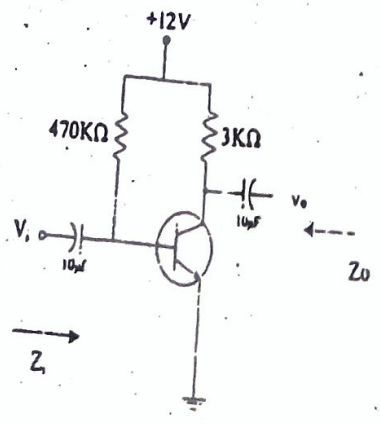
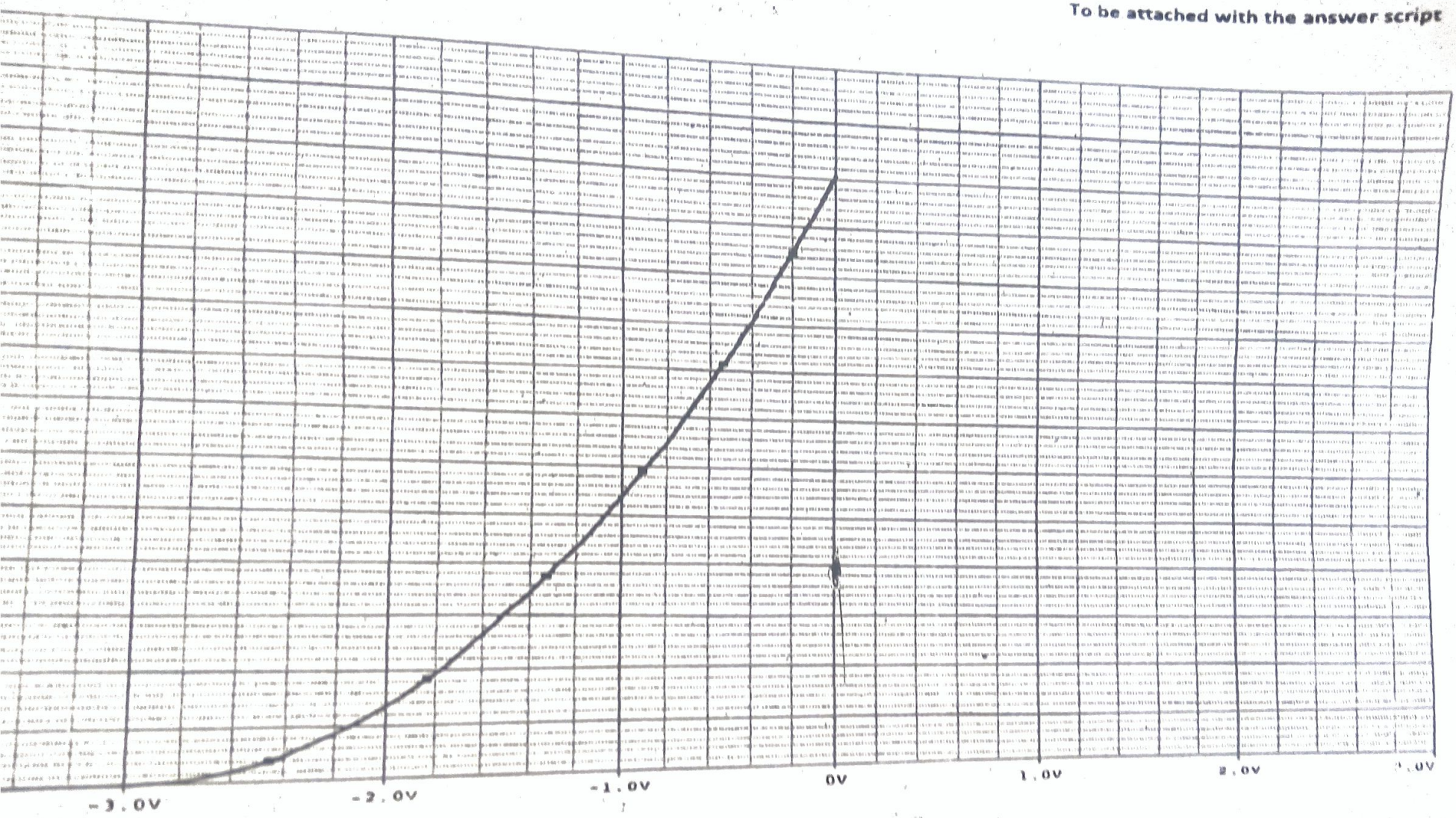


Fig:-3(b)

To be attached with the answer script



Signature of the invigilator

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, FALL-2014
COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

TIME: 3 HRS

FULL MARKS: 210

There are Eight(8) questions. Answer any Six(6)
Marks allotted for each question are indicated in the right margin
(All resistances are in ohms if not specified)

(a) What is semiconductor material? How can we create p-type and n-type semiconductor material from an intrinsic material? **[15]**

(b) What are the circuit models generally used as an equivalent circuit of a diode. Explain shortly. **[20]**

) For the circuit shown in figure 2(a), the diode forward resistance r_f=5Ω and load resistance R_L=800Ω. Determine (i) PIV (ii) DC output voltage (iii) Output and Input power (iv) Rectifier efficiency. **[17]**

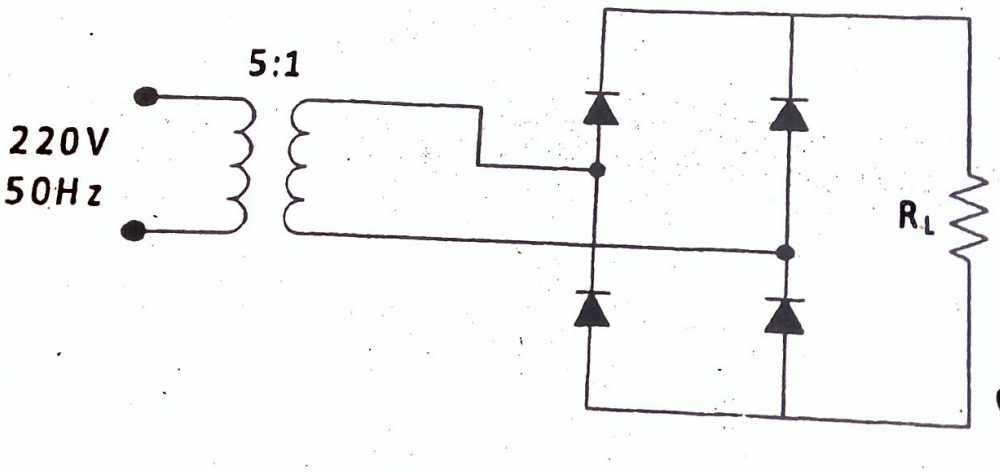


Figure 2(a)

lain the operation of a full-wave bridge rectifier. Show that the efficiency of a full-wave fier is about 81.14%. **[18**

27.4.15

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, FALL-2014
COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICE AND CIRCUITS

TIME: 3 HRS **FULL MARKS: 210**

There are Eight(8) questions. Answer any Six(6)
Marks allotted for each question are indicated in the right margin
(All resistances are in ohms if not specified)

01.

(a) What is semiconductor material? How can we create p-type and n-type semiconductor material from an intrinsic material? **[15]**

(b) What are the circuit models generally used as an equivalent circuit of a diode. Explain shortly. **[20]**

02. (a) For the circuit shown in figure 2(a), the diode forward resistance $r_f=5\Omega$ and load resistance $R_L=800\Omega$. Determine (i) PIV (ii) DC output voltage (iii) Output and Input power (iv) Rectifier efficiency. **[17]**

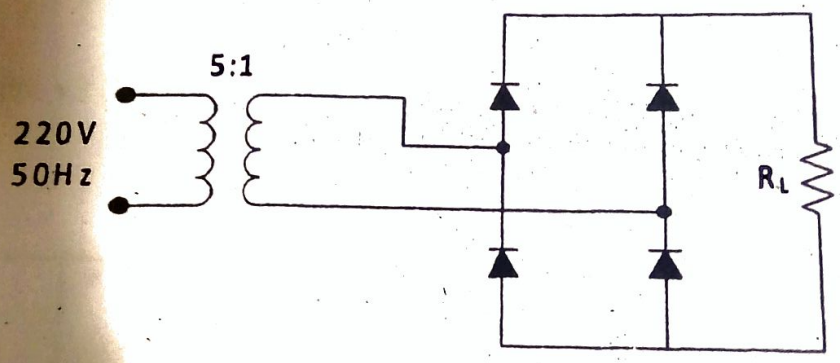


Figure 2(a)

(b) Explain the operation of a full-wave bridge rectifier. Show that the efficiency of a full-wave rectifier is about 81.14%. **[18**

04.

(a) Draw the input and output wave shapes of the following circuits in Figure 4(a): [1

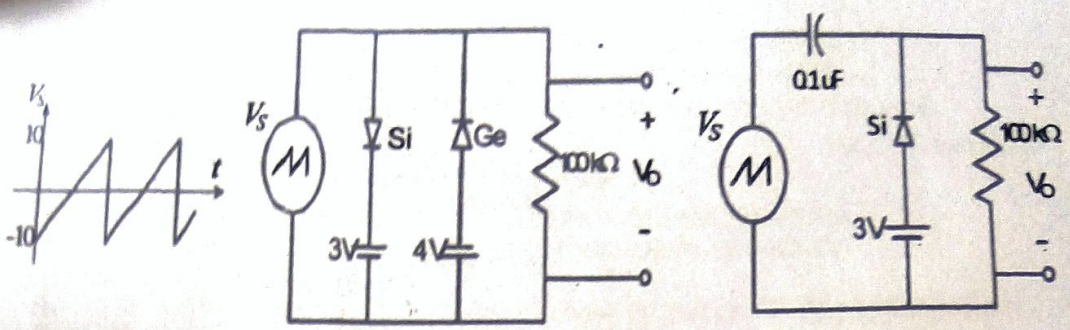


Figure 4(a)

(b) What is pinch-off voltage? Write down the Schockley's equation for a JFET and sketch the transfer characteristics of a JFET, given that $I_{DS} = 10$ mA and $V_P = -4$ V for $V_{GS} = 0$ V. [17

05.

(a) Show the effect on operating point ('Q' point) due to change in R_B, R_C and V_{CC} for a fixed bias transistor circuit shown in Figure 5(a). [17]

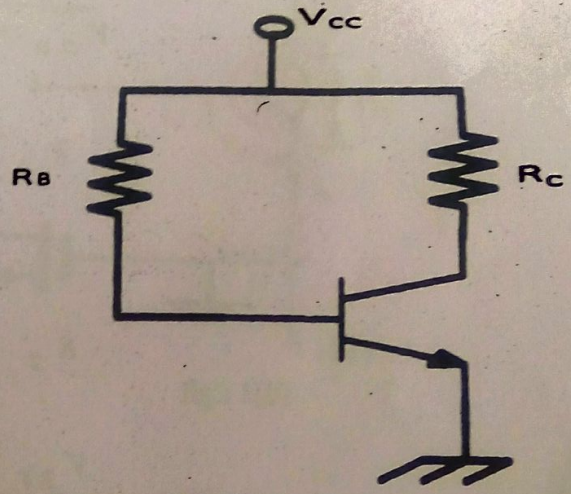


Figure 5(a)

(b)

For the following voltage-divider network shown in figure 5(b) determine: [18]

a) V_{CE} and b) I_C (Where β=100)

22.03.16

[illegible]
[illegible] ENGINEERING
[illegible] Examination, Fall-2015
[illegible] Devices & Circuits
[illegible] Full Marks: 210

SECTION A

[illegible] answer any three (3)
[illegible] in the right margin

Q1.

(a) [illegible] N-type and P-type semiconductor [illegible] [20]

(b) [illegible] the voltage at the emitter terminal is [illegible] [15]
i. [illegible]
ii. [illegible]
iii. [illegible] of the transistor.

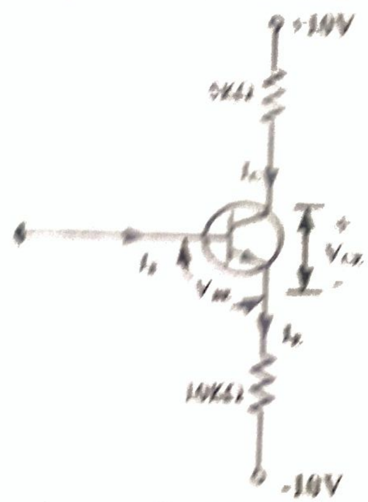


fig.: 1(b)

Q2.

(a) What are the differences between Avalanche breakdown and Zener breakdown mechanism of a diode? [20]

(b) Draw the output voltage wave shape for the following Clipper circuit of fig. 2(b). Consider diodes as ideal. [15]

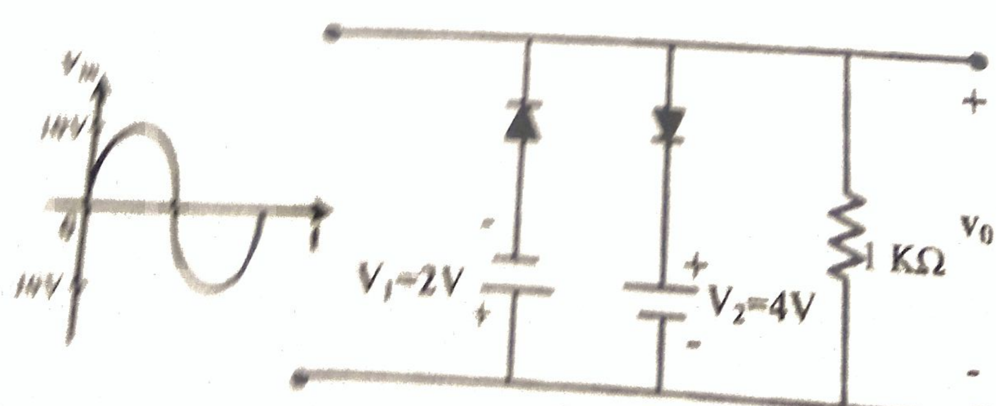


fig.: 2(b)

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, FALL-2015
COURSE NO.: EEE-2141 COURSE TITLE: ELECTRONIC DEVICES & CIRCUITS

22.03.16

TIME: 3 HRS FULL MARKS: 210

SECTION-A

There are four (4) questions in this section. Answer any three (3)
Marks allotted for each question are indicated in the right margin

01

(a) What is an extrinsic semiconductor? Discuss about N-type and P-type semiconductor materials? [20]

(b) For the following circuit shown in fig. 1(b) the voltage at the emitter terminal is measured as $V_E = -0.7v$; If $\beta=50$. Then find; [15]

i. I_E, I_B and I_C
ii. V_B and V_C
iii. And also the mode of operation of the transistor.

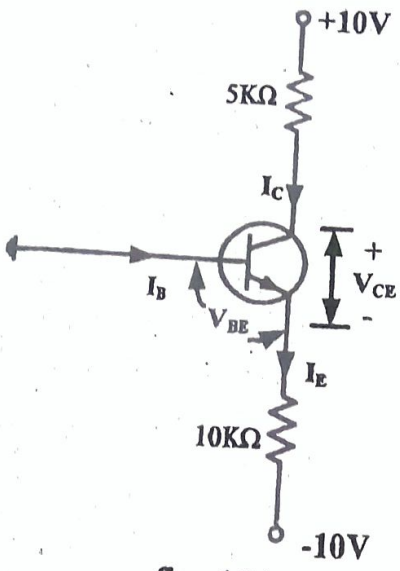


fig.: 1(b)

02

(a) What are the differences between Avalanche breakdown and Zener breakdown mechanism of a diode? [20]

(b) Draw the output voltage wave shape for the following Clipper circuit of fig. 2(b). Consider diodes as ideal. [15]

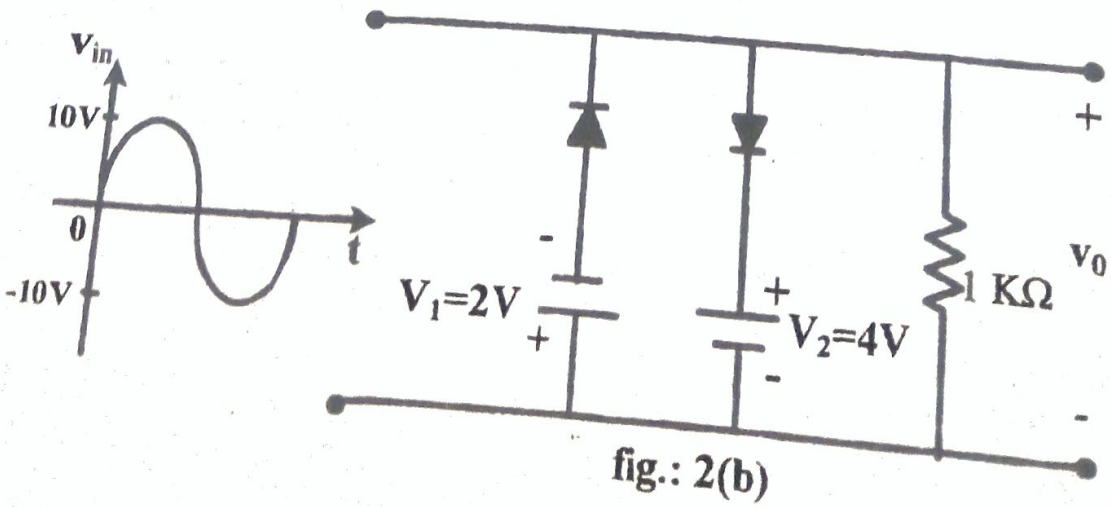


fig.: 2(b)

[illegible]

Time: 3 Hours

Full Marks: 70

SECTION-A

There are four (4) questions in this section. Answer any three (3).
Marks allotted for each question are indicated in the right margin.

01

(a) What is an extrinsic semiconductor? Discuss about N-type and P-type semiconductor materials? [20]

(b) For the following circuit shown in fig. 1(b) the voltage at the emitter terminal is [15] measured as $V_E = 0.7V$. If $\beta = 50$. Then find,

i. I_E, I_B and I_C
ii. V_{CB} and V_{CE}
iii. And also the mode of operation of the transistor.

fig.: 1(b)

02

(a) What are the differences between Avalanche breakdown and Zener breakdown mechanism of a diode? [20]

(b) Draw the output voltage wave shape for the following Clipper circuit of fig. 2(b). [15] Consider diodes as ideal.

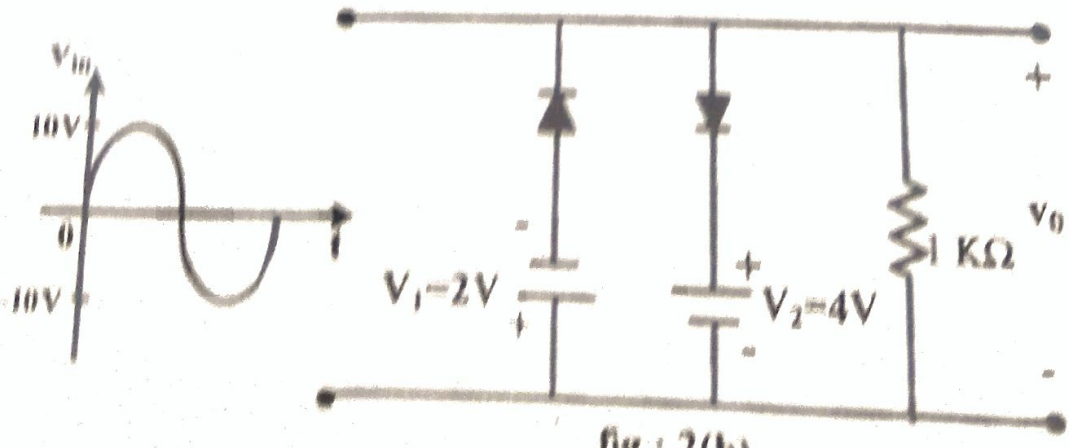


fig.: 2(b)

AHSANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, [illegible]
COURSE NO.: EEE-2141 COURSE TITLE: [illegible]
TIME: 3 HRS

SECTION-A

There are four (4) questions in this section. Answer any three (3).
Marks allotted for each question are indicated in the right margin.

01

(a) What is an extrinsic semiconductor? Discuss about N-type and P-type semiconductor materials? [4]

(b) For the following circuit shown in fig. 1(b) the voltage at the emitter terminal is measured as $V_E = -0.7v$; If $\beta = 50$. Then find; [4]

i. I_E, I_B and I_C
ii. V_B and V_C
iii. And also the mode of operation of the transistor.

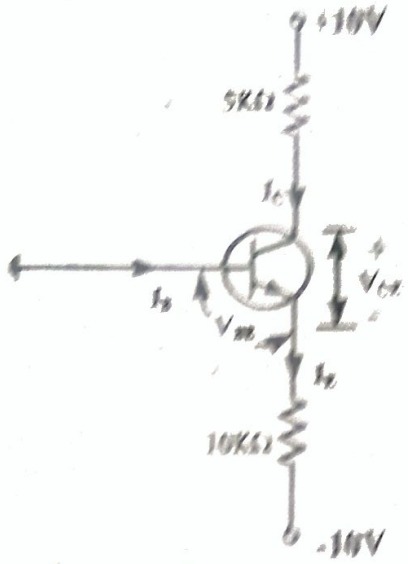


fig.: 1(b)

02

(a) What are the differences between Avalanche breakdown and Zener breakdown mechanism of a diode? [4]

(b) Draw the output voltage wave shape for the following Clipper circuit of fig. 2(b). [4] Consider diodes as ideal.

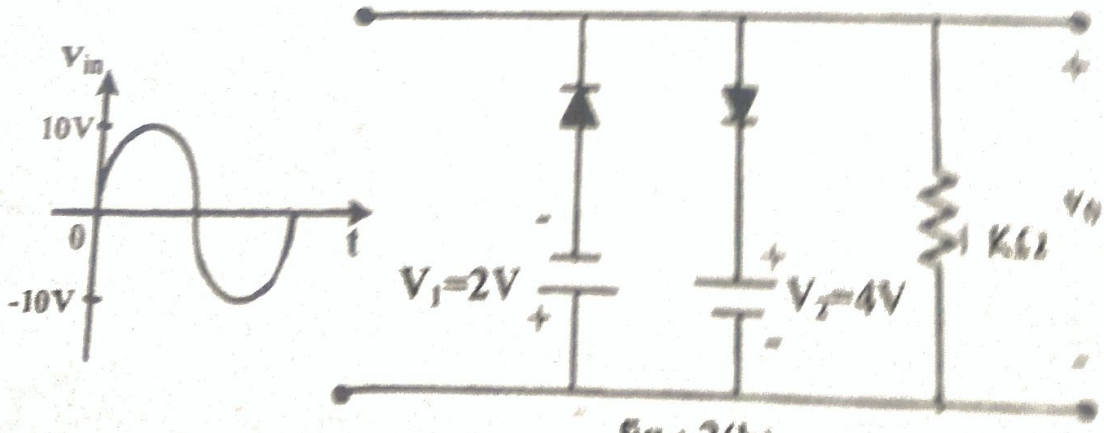


fig.: 2(b)

(b) For the following network shown in fig.3(b), determine the value of output voltage, V_o [15]

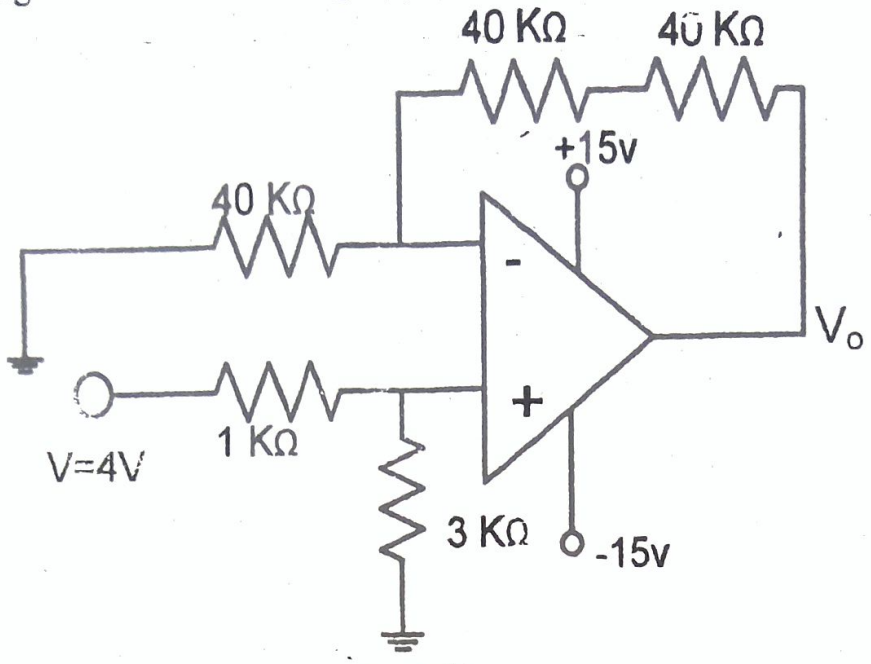


fig.: 3(b)

(a) Describe the construction and operating principle of an N-channel depletion type MOSFET with associated characteristic curves. [20]

(b) Draw a non-inverting positive 2-volt level crossing detector where the input voltage waveform is given as in the fig. 4(b). Also draw the output voltage waveform. [15]

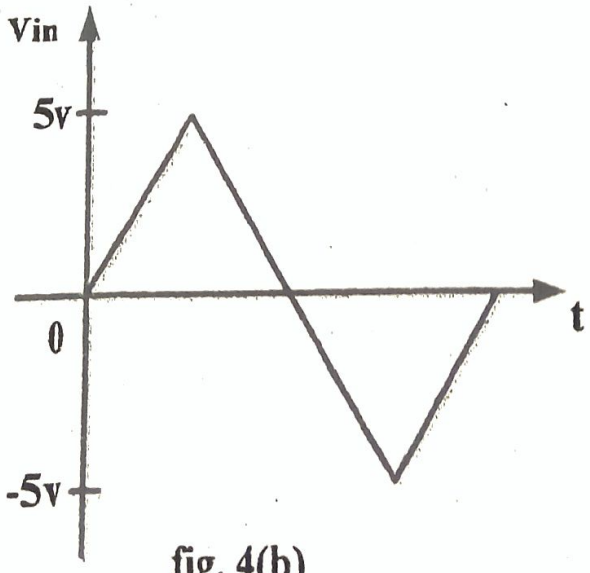


fig. 4(b)

2ND YEAR 1ST SEMESTER, FALL-2015

CLEARANCE/ IMPROVEMENT/ CARRYOVER EXAMINATION

COURSE NO.: EEE-2141 COURSE TITLE: ELECTRONIC DEVICES & CIRCUITS

TIME: 3 HRS FULL MARKS: 210

SECTION-A

There are four (4) questions in this section. Answer any three (3)

Marks allotted for each question are indicated in the right margin

01

(a) What is an extrinsic semiconductor? Discuss about N-type and P-type semiconductor materials? [17]

(b) Derive the Piece-wise linear model of a diode. Using the Piece-wise linear model of a diode, find I_D & V_D of the circuit shown in figure-1(b), Given, $R_D = 20\Omega$ & $V_{Do} = 0.65V$. [18]

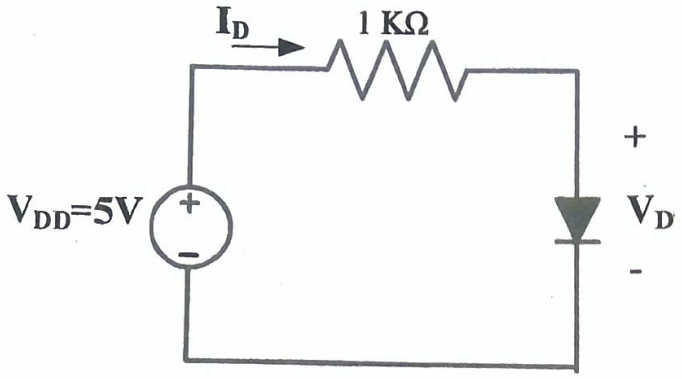
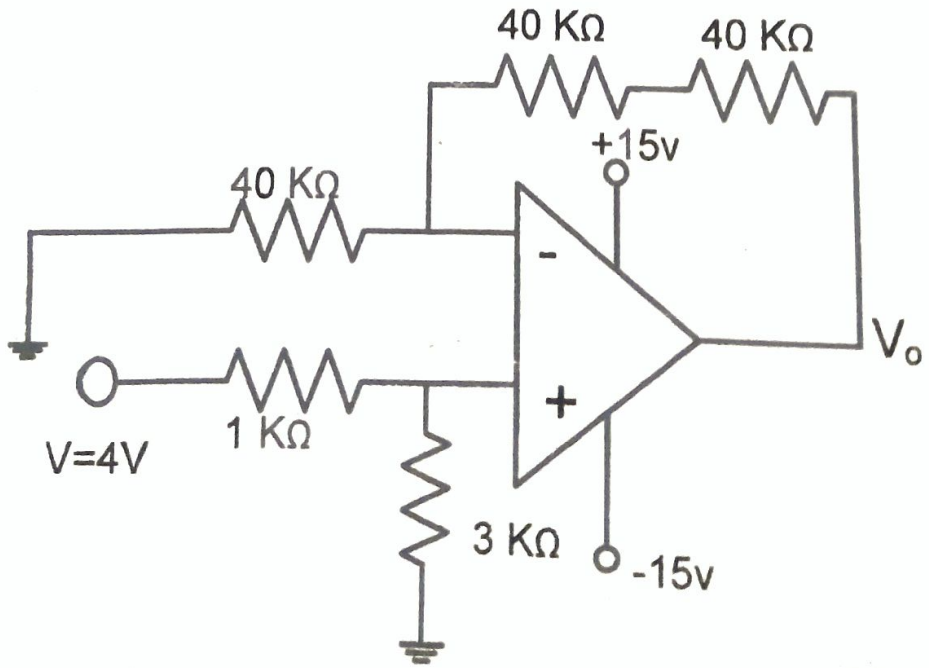


figure: 1(b)

2

(a) Discuss briefly about the following limitations in the operating condition of PN junction: [17]
i) Maximum forward current ii) Peak Inverse Voltage iii) Maximum Power rating.

(b) For the following network shown in figure-2(b), determine the value of output voltage, V_o [18]



03

(a) What is the purpose of biasing a transistor? Draw the circuit of a PNP transistor in the CE configuration. Sketch the output characteristic curve showing the different regions of operation. [17]

(b) For the circuit shown in figure-3(b), determine V_{GSQ}, I_{DQ}, V_{DS}, V_G, and V_S. [18]

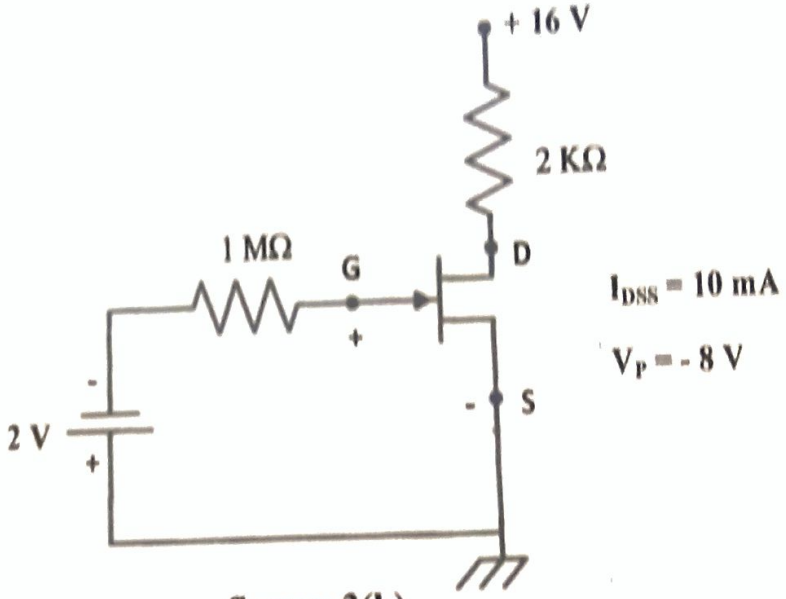


figure: 3(b)

04

(a) Describe the construction and operating principle of an N-channel enhancement type MOSFET with associated characteristic curves. [17]

(b) For the clamper circuit shown in figure-4(b), Draw the output voltage wave shape. [18

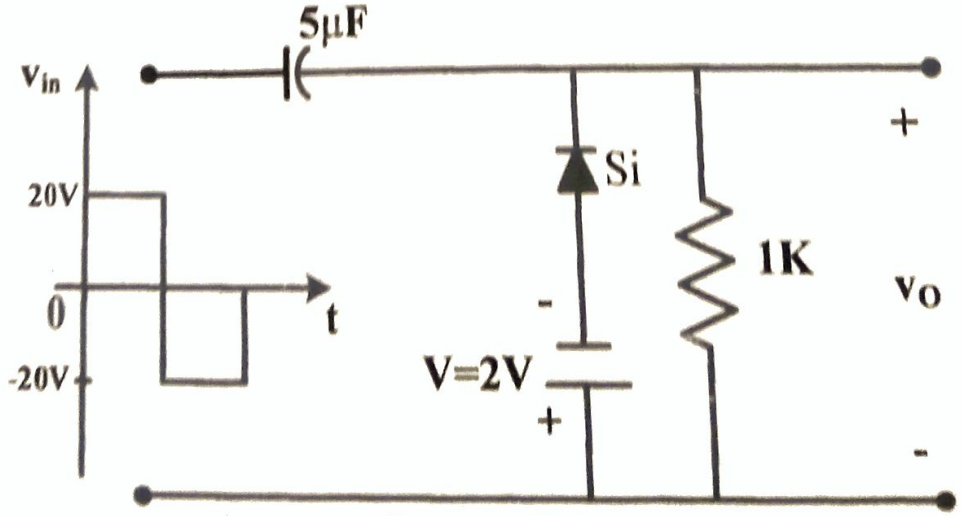


figure : 4(b)

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, SPRING-2016

COURSE NO: EEE-2141 COURSE TITLE: ELECTRONIC DEVICES & CIRCUITS

TIME: 3 HRS FULL MARKS: 210

[USE SEPARATE ANSWER SCRIPTS FOR EACH SECTION]

SECTION-A

There are four (4) questions in this section. Answer any three (3)

Marks allotted for each question are indicated in the right margin

01

(a) What is semiconductor material? Explain with necessary figures how N-type semiconductor can be created from intrinsic material? [15]

(b) Determine the currents I_1, I_2 and I_{D_2} for the network shown in Fig.1(b). Turn on voltage of GaAs 1.2V. [15]

(c) Determine I and V for the circuit shown in Fig.1(c). [5]

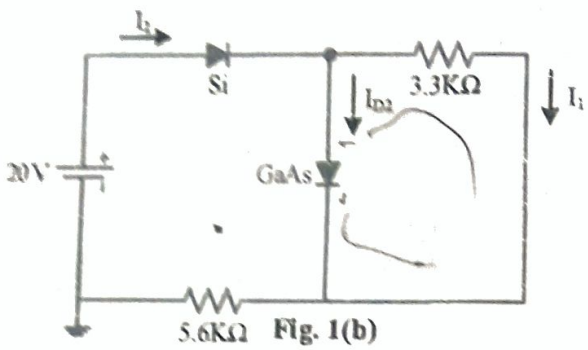


Fig. 1(b)

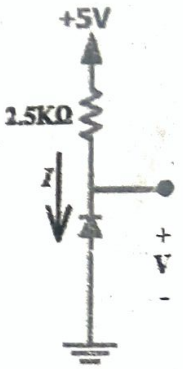


Fig. 1(c)

02

(a) For the network in Fig. 2(a), determine the range of R_L and I_L that will result V_{RL} being maintained at 10 V. [18]

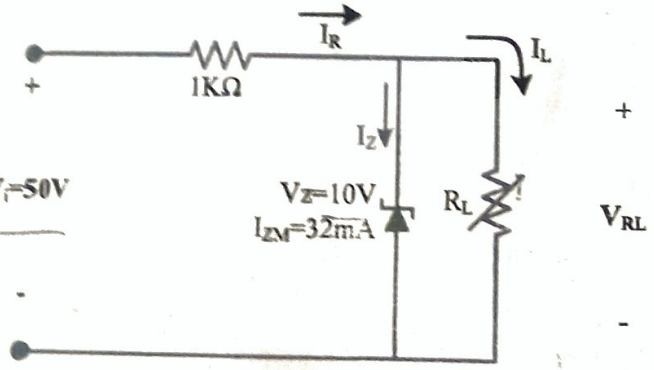
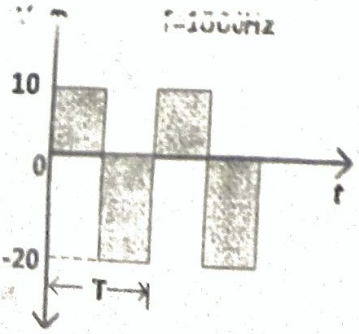


Fig. 2(a)

(b) Determine wave shape at Vo for the network shown in Fig. 2(b) for the input indicated. [17]



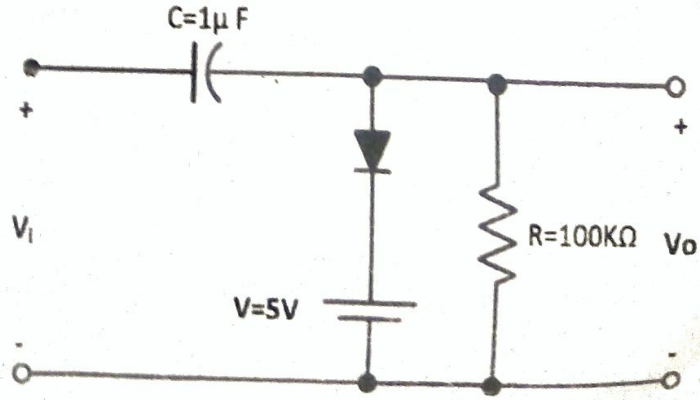


Fig. 2(b)

03

(a) What is rectifier? Draw the Full wave rectifier circuit with load resistance R_L. Describe the operation of the circuit drawing input and output waveforms. Also show that efficiency for a full wave rectifier is 81 % for ideal diodes. [20]

(b) Describe the Zener breakdown mechanism. [15]

04

(a) For the circuit shown in Fig: - 4(a) the I-V characteristics curve for the unknown diode can be found in page 5. Using load line method determine the Q-point and the current flowing in the circuit. Also determine the static resistance of the diode for V=6V. (attach page 5 with the answer script if you answer this question) [15]

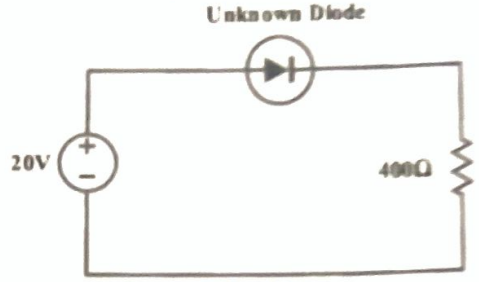


Fig: 4(a)

(b) Describe the construction and operating principle of an N-channel enhancement type MOSFET with associated characteristic curves. [20]

SECTION-B

There are four (4) questions in this section. Answer any three (3)
Marks allotted for each question are indicated in the right margin

05

(a) Draw the input and output characteristics of common emitter (CE) and common base (CB) configuration of a NPN transistor showing different regions of operation. Also write important differences between CE and CB configuration of NPN transistor. [17]

(b) For the emitter stabilized network shown in Fig. 5(b); Determine, [18]

i. I_B, I_C and I_E
ii. V_B V_C and V_E.
iii. V_{CE} and V_{BC}

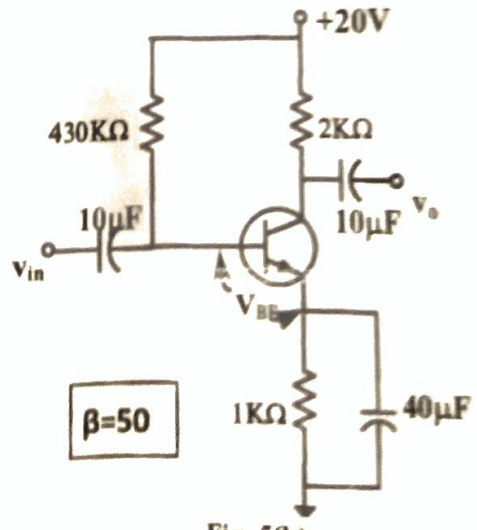


Fig. 5(b)

SECTION-B

There are four (4) questions in this section. Answer any three (3)
Marks allotted for each question are indicated in the right margin

05

(a) Show that, $I_{CEO} = (1+\beta) I_{CBO}$, where the symbols have their usual meaning. [17]

(b) Determine Value of V_{CE}, V_{CB} and mode of operation from the following Circuit of figure-5(b). [18]

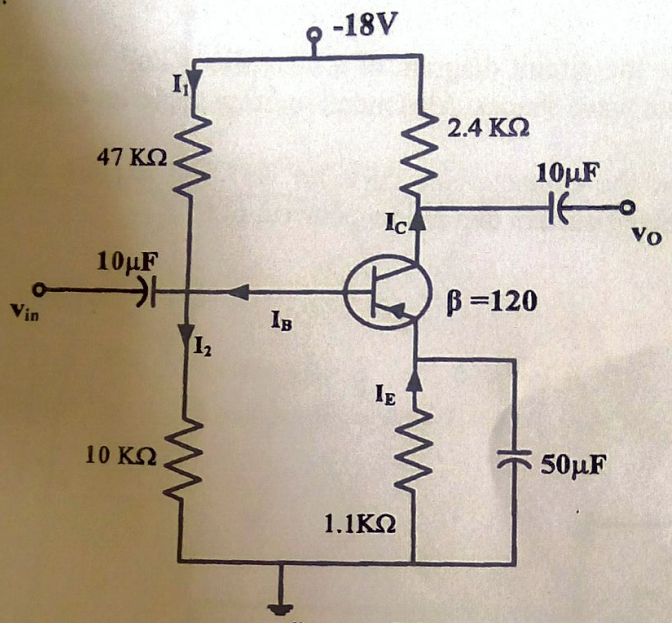


figure: 5(b)

06

(a) What is the purpose of biasing? Describe how a BJT can work as an inverter. [17]

(b) Determine value of V_B, V_C, V_E and I_B, I_C, I_E of the circuit shown in figure-6(b). [18]

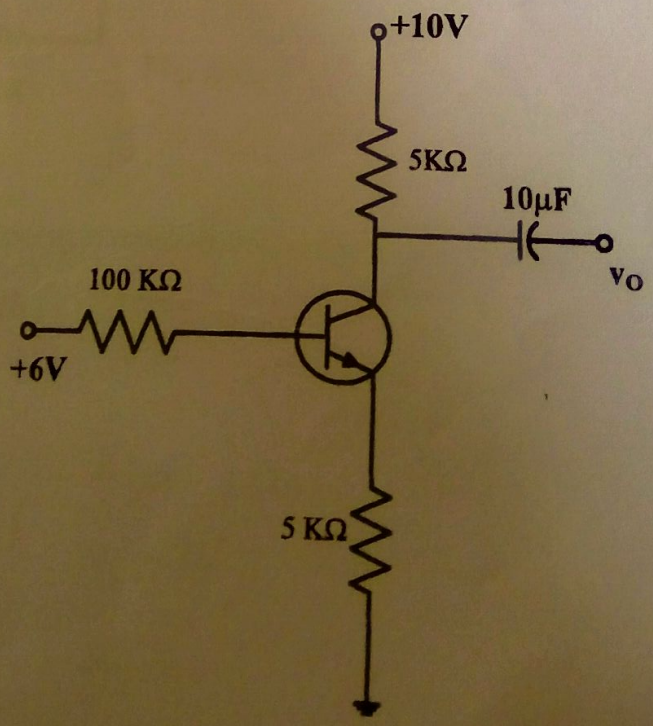


figure : 6(b)

07

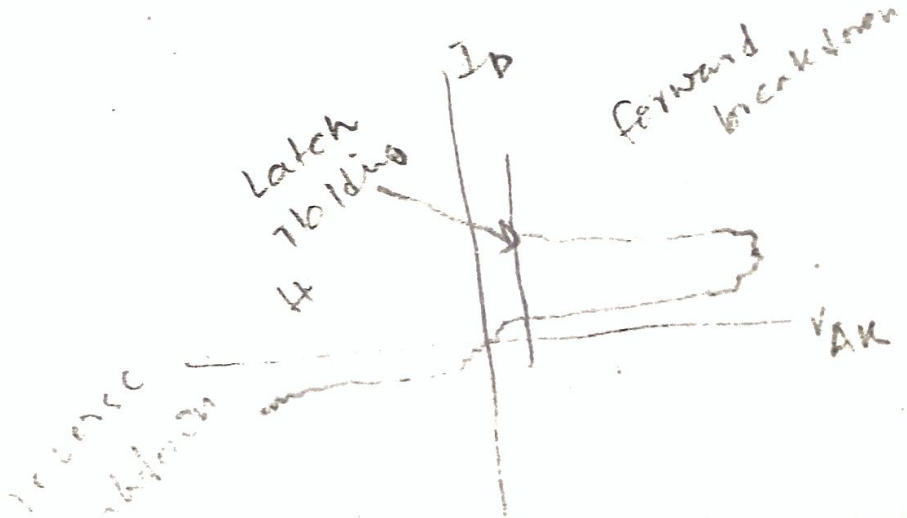
(a) Explain working principle of "Wein-Bridge Oscillator" with necessary circuit diagram. [17]

(b) Design a circuit using OPAMP to have the output voltage [18]
$V_0 = 10V_1 - 11V_2 + 2V_3 - 15V_4$.

08

(a) Draw the circuit diagram of a controlled "Full Wave Rectifier" with input and output wave shapes. Also mention firing angle for each thyristor. [17]

(b) Draw the characteristic curve of UJT and explain its operation. Also Explain Latching current and holding current of SCR. [18]



(a) Write important characteristics of an ideal Op-amp. [12]

(b) Draw an inverting positive 2-volt level crossing detector circuit where the input voltage waveform is given in the Fig. 6 (b). Also draw the output voltage waveform.

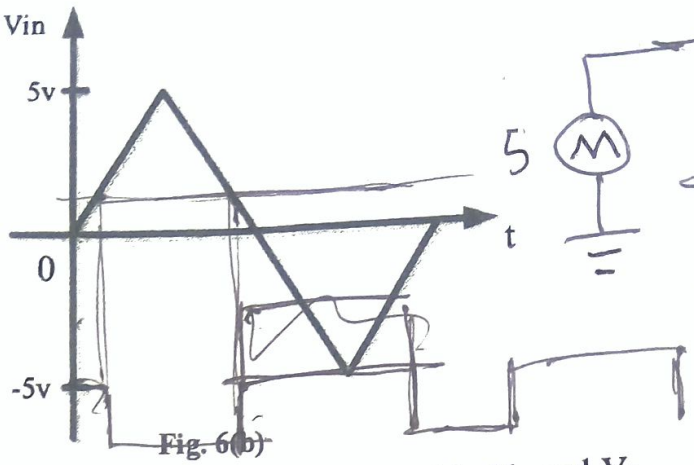
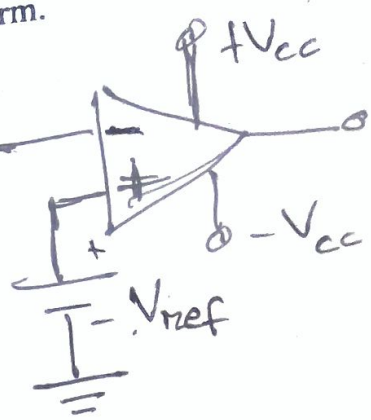


Fig. 6(b)



[18]

(c) For the circuit shown in Fig. 6 (c), find output voltages, V_1, V_2 and V_3.

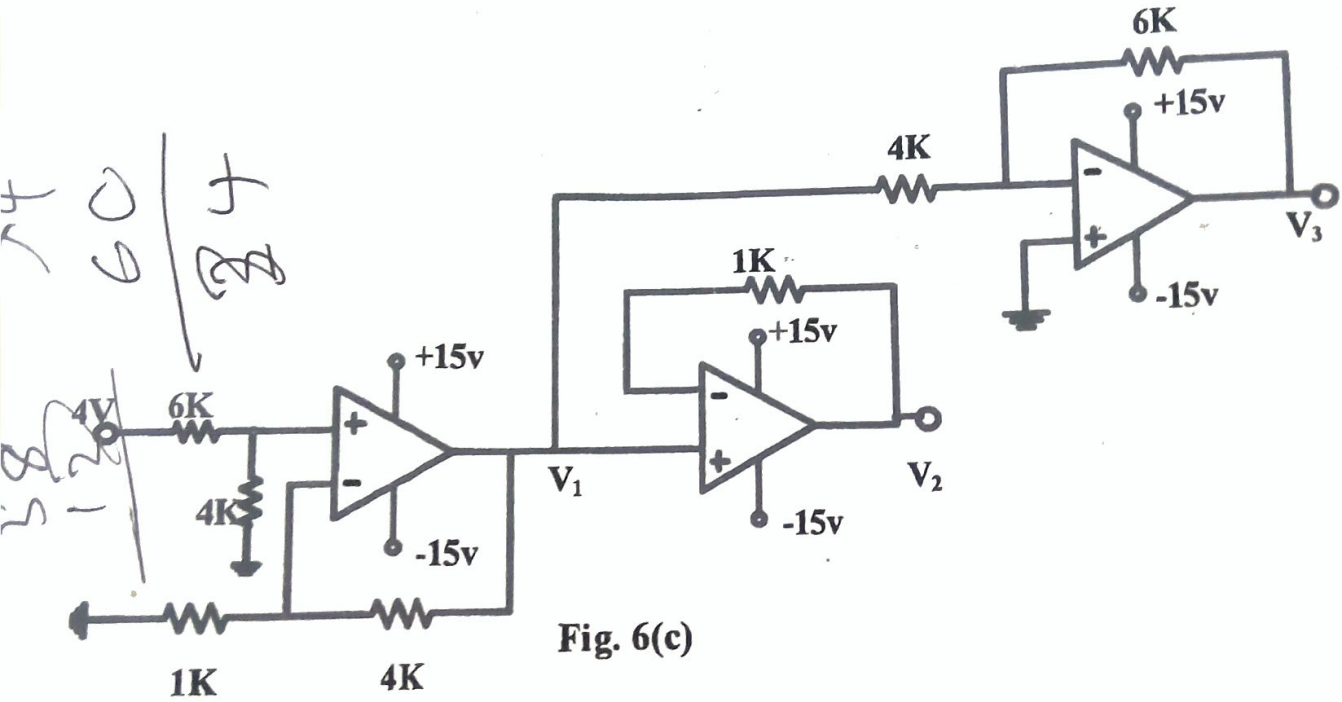


Fig. 6(c)

What is the purpose of biasing a transistor? Describe how a BJT can work as an inverter. [17]

$R_f = 10K$

$V_1 = 4$

$V_1 = \left(1 + \frac{10}{4}\right)4$

$= (1 + 2.5)4 = 14$

7. Determine the DC bias voltage V_{CE}, V_{CB} and mode of operation for the voltage-divider configuration shown in Fig.7(b). Assume, $\beta = 120$. [18]

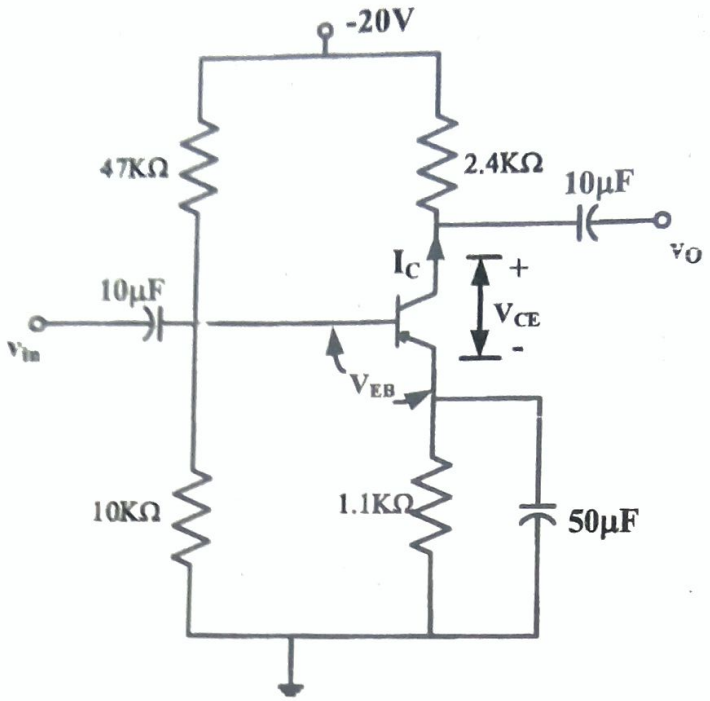


Fig.7(b)

8. (a) Write short note on Diffusion of impurities for IC fabrication. [09]

(b) Draw the circuit diagram of a controlled "Full Wave Rectifier" with input and output voltage waveforms for R load. Also mention firing angle for each Thyristor. [09]

(c) Design a circuit using Op-amp to have the output voltage, $V_0 = -2V_3 - 7V_2 + 2V_1$ [17]

12.09.2017

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
2ND YEAR 1ST SEMESTER, FINAL EXAMINATION, SPRING-2017
COURSE NO.: EEE-2141 COURSE TITLE: ELECTRONIC DEVICES & CIRCUITS

TIME: 3 HRS **Use separate script for each part.** FULL MARKS: 210

SECTION-A

There are four (4) questions in this section. Answer any three (3)
Marks allotted for each question are indicated in the right margin

01

(a) What is an extrinsic semiconductor? Explain why a pentavalent impurity atom is known as donor-typed impurity. **[17]**

(b) Design a clamper circuit to perform the following operation of Fig. 1(b) with necessary equation. **[18]**

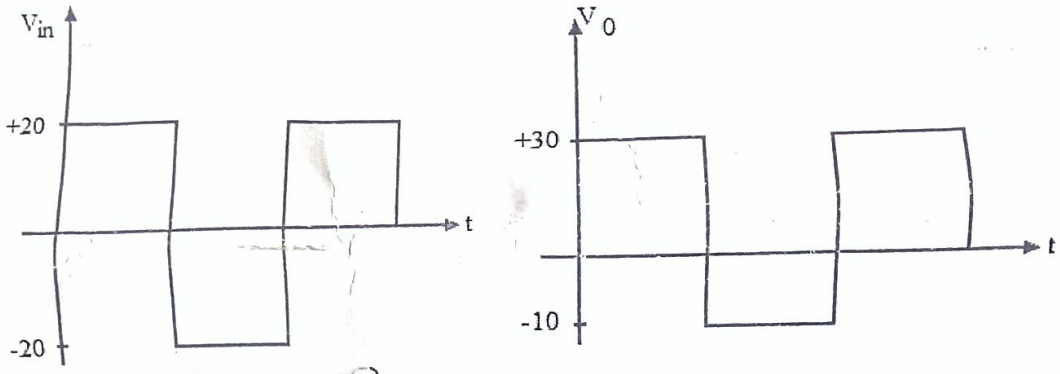


Fig.:1 (b)

02

(a) Using the small signal diode model show that, $i_d = \frac{I_D}{nV_T} v_d$, $r_d = \frac{nV_T}{I_D}$ where the symbols have their usual meaning. **[17]**

(b) Find I_D and V_0 of the circuit shown in Fig.:2 (b). **[18]**

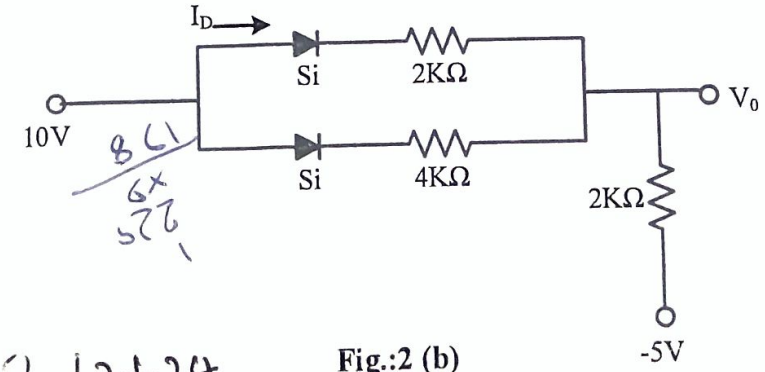


Fig.:2 (b)

03

(a) Draw the circuit diagram of a full wave rectifier with input and output wave shapes with bridge connection and explain its working principle. Also derive the expression of rectification efficiency in this case. [17]

(b) Draw the output wave shapes, V_0 of the circuit shown in Fig.: 3 (b) with necessary equations. [18]

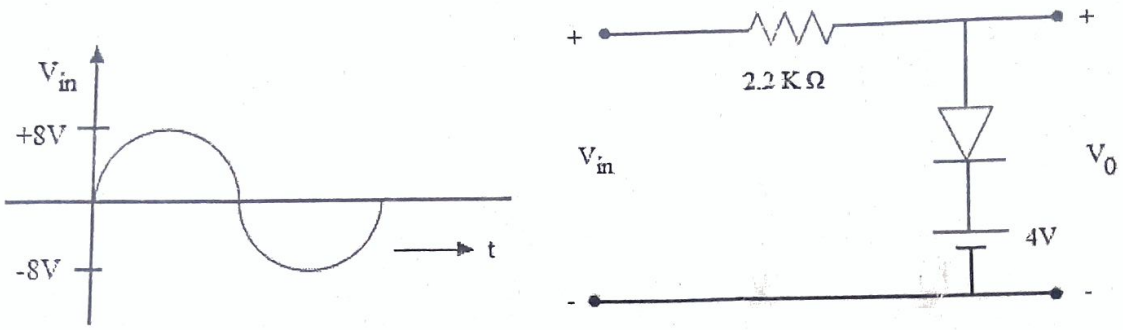


Fig.: 3 (b)

04

(a) From the circuit shown in Fig.: 4 (a), determine the range of R_L and I_L that will result V_{RL} being maintained at 10V. [17]

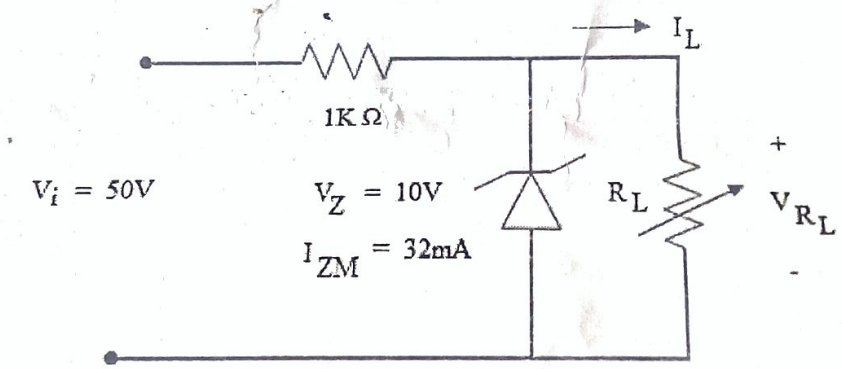


Fig.: 4 (a)

(b) Draw a NPN transistor in the CB configuration biased for operation in the active region. Also sketch typical CB input and output characteristic curve for an NPN transistor. Label all the variables. [18]

SECTION-B

There are four (4) questions in this section. Answer any three (3)

Marks allotted for each question are indicated in the right margin

05

(a) What is the difference between depletion type and enhancement type MOSFET. Describe the construction and operating principle of a N-channel depletion type MOSFET with input and output characteristics curves. [17]

(b) Draw the output voltage waveform of the following comparator circuit of Fig. 5(b). [18]

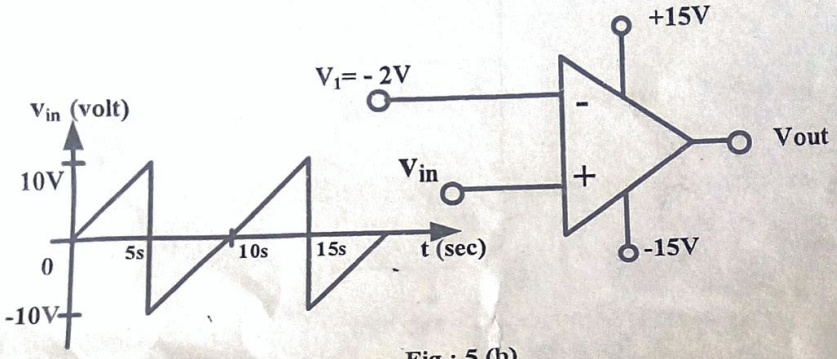


Fig.: 5 (b)

06

(a) Show that, $I_C = \beta I_B + I_{CEO}$, where the symbols have their usual meaning. [17]

(b) For the circuit shown in Fig. 6 (b), find output voltages, V_1 and V_2. [18]

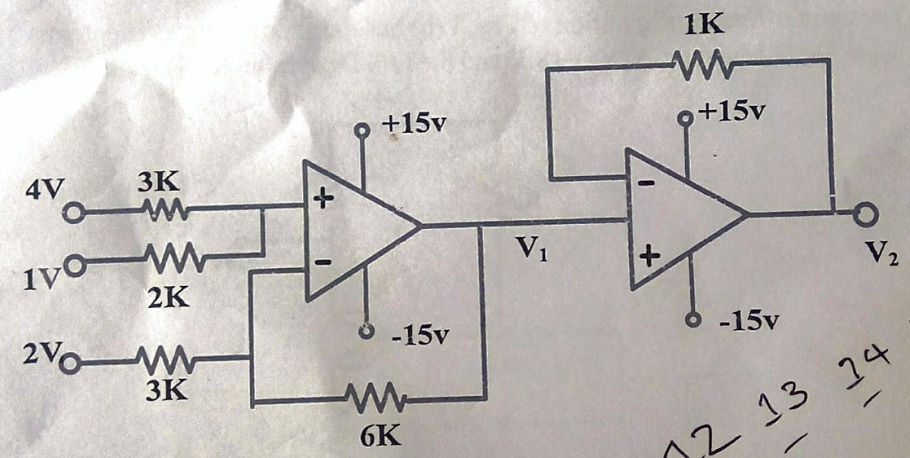


Fig.: 6 (b)

07

(a) Explain BJT amplifying action with relevant figures. [17]

(b) A voltage divider bias circuit is shown in the Fig.7 (b). Determine the operating point. [18]
Assume $V_{BE} = 0.7V$

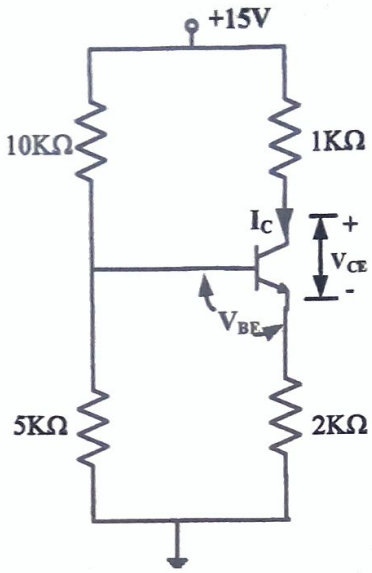


Fig.: 7(b)

08

(a) Write short notes on: [17]
i. Controlled full wave rectifier.
ii. Pinch-off voltage of a MOSFET and
iii. Ion implantation of IC fabrication.

(b) The emitter-bias configuration of Fig. 8 (b) has the following specifications: [18]
$I_{CQ} = \frac{1}{2} I_{Csat}$, $I_{Csat} = 8mA$, $V_C = 18$ V and $\beta = 110$. Determine R_C, R_E, and R_B.

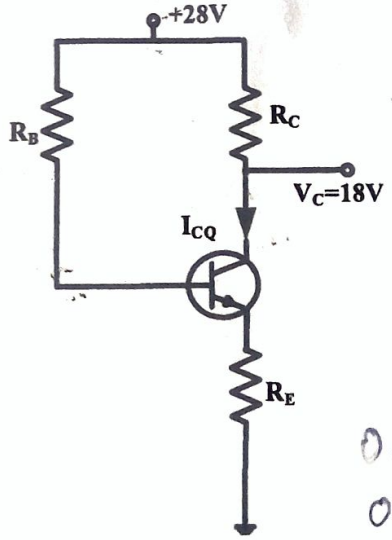


Fig.: 8 (b)