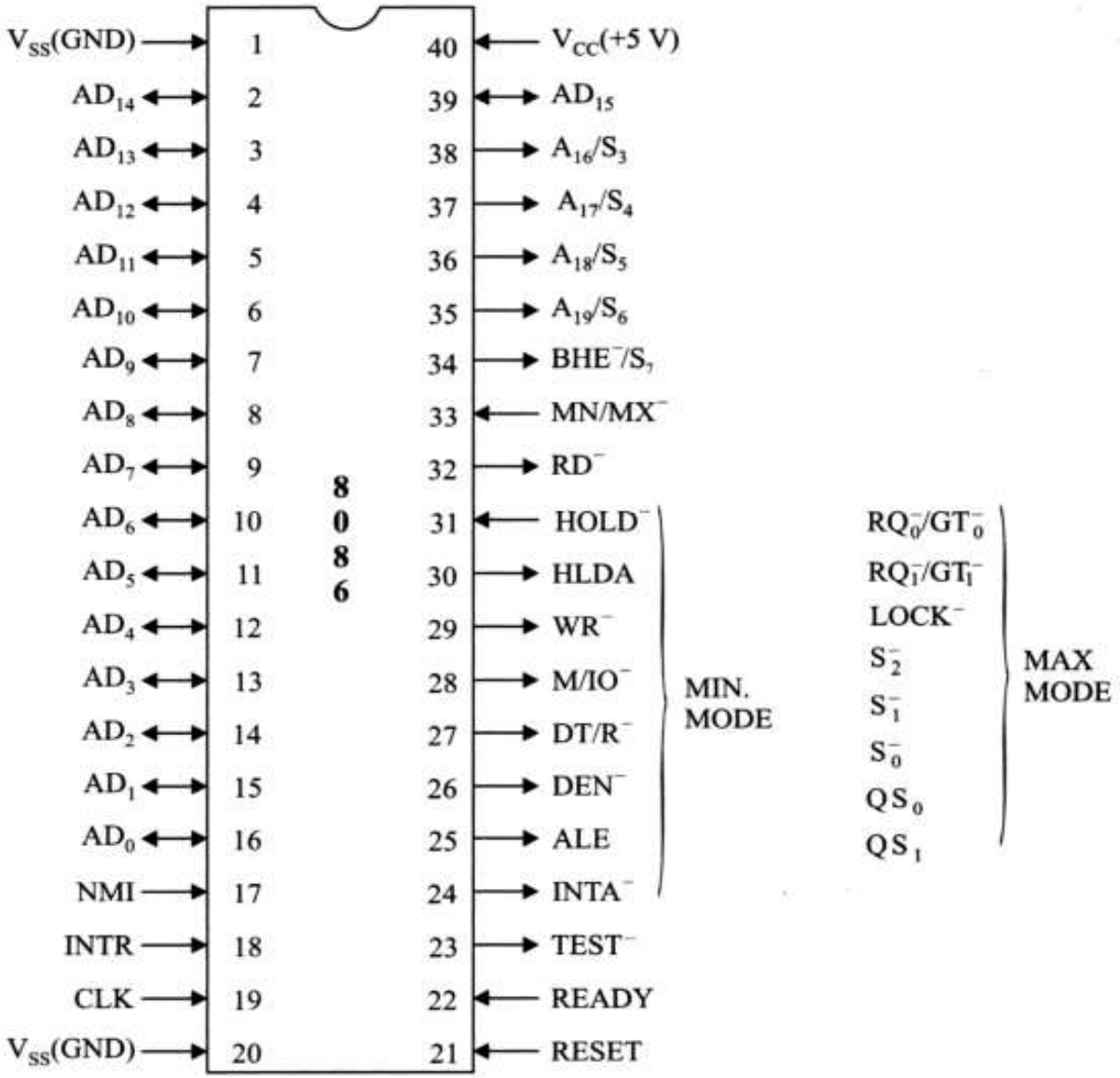
8086 Pin Description

8086 Pin Diagram



Pin Details of 8086
(Common to both Maximum and Minimum mode)

$AD_0 - AD_{15}$

Pin 16-2, 39 (Bi-directional)

- These lines are multiplexed bi-directional address/data bus.
- During T_1, they carry lower order 16-bit address.
- In the remaining clock cycles, they carry 16-bit data.
- AD_0-AD_7 carry lower order byte of data.
- AD_8-AD_{15} carry higher order byte of data.

A_{19}/S_6, A_{18}/S_5, A_{17}/S_4, A_{16}/S_3

Pin 35-38 (Unidirectional)

- These lines are multiplexed unidirectional address and status bus.
- During T_1, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals.

S_3 and S_4 indicate the segment register being used as follows :

S_4	S_3	Register
0	0	ES
0	1	SS
1	0	CS or none
1	1	DS

S_5 gives the current setting of the interrupt flag (IF) and S_6 is always zero.

$\overline{BHE}$ / S_7

Pin 34 (Output)

- BHE stands for Bus High Enable.
- BHE signal is used to indicate the transfer of data over higher order data bus (D_8 – D_{15}).
- 8-bit I/O devices use this signal.
- It is multiplexed with status pin S_7.

$\overline{RD}$ (Read)

Pin 32 (Output)

- It is a read signal used for read operation.
- It is an output signal.
- It is an active low signal.

READY

Pin 22 (Input)

- This is an acknowledgement signal from slower I/O devices or memory.
- It is an active high signal.
- When high, it indicates that the device is ready to transfer data.
- When low, then microprocessor is in wait state.

RESET

Pin 21 (Input)

- It is a system reset.
- It is an active high signal.
- When high, microprocessor enters into reset state and terminates the current activity.
- It must be active for at least four clock cycles to reset the microprocessor.

INTR

Pin 18 (Input)

- It is an interrupt request signal.
- It is active high.
- It is level triggered.

NMI

Pin 17 (Input)

- It is a non-maskable interrupt signal.
- It is an active high.
- It is an edge triggered interrupt.

$\overline{\text{TEST}}$

Pin 23 (Input)

- It is used to test the status of math co-processor 8087.
- The $\overline{\text{BUSY}}$ pin of 8087 is connected to this pin of 8086.
- If low, execution continues else microprocessor is in wait state.

CLK

Pin 19 (Input)

- This clock input provides the basic timing for processor operation.
- It is symmetric square wave with 33% duty cycle.
- The range of frequency of different versions is 5 MHz, 8 MHz and 10 MHz.

V_{CC} and V_{SS}

Pin 40 and Pin 20 (Input)

- V_{CC} is power supply signal.
- +5V DC is supplied through this pin.
- V_{SS} is ground signal.

MN / $\overline{MX}$

Pin 33 (Input)

- 8086 works in two modes:
  - Minimum Mode
  - Maximum Mode
- If MN/$\overline{MX}$ is high, it works in minimum mode.
- If MN/$\overline{MX}$ is low, it works in maximum mode.

MN / $\overline{MX}$

Pin 33 (Input)

- Pins 24 to 31 issue two different sets of signals.
- One set of signals is issued when CPU operates in minimum mode.
- Other set of signals is issued when CPU operates in maximum mode.

Minimum Mode	Maximum Mode
In minimum mode there can be only one processor i.e. 8086.	In maximum mode there can be multiple processors with 8086, like 8087 and 8089.
MN/MX (bar) is 1 to indicate minimum mode.	MN/MX (bar) is 0 to indicate maximum mode.
In minimum mode 8086 generates INTA (bar), ALE, DEN (bar), DT/R (bar), M/IO (bar), HLDA, HOLD and WR (bar), control signals.	In maximum mode 8086 generates QS1, QS0, S0 (bar), S1 (bar), S2 (bar), LOCK (bar), RQ (bar), GT1, RQ (bar)/GT0 control signals.
In minimum mode direct RD WR signals can be used. No bus controller required. A simple de-multiplexing would do the job of producing the control signals. The de-multiplexer produces MEMRD, MEMWR, IORD, IOWR control signals.	In maximum mode a bus controller i.e. 8028 is required to produce control signals. This bus controller produces MEMRDC, MEMWRC, IOWRC, ALE, DEN, DT/R control signals.
The circuit is simpler.	The circuit is more complex.
Multiprocessing cannot be performed hence performance is lower.	As multiprocessing can be performed, it can give very high performance.

Pin Description for Minimum Mode

$\overline{\text{INTA}}$

Pin 24 (Output)

- This is an interrupt acknowledge signal.
- When microprocessor receives INTR signal, it acknowledges the interrupt by generating this signal.
- It is an active low signal.

ALE

Pin 25 (Output)

- This is an Address Latch Enable signal.
- It indicates that valid address is available on bus $AD_0 - AD_{15}$.
- It is an active high signal and remains high during T_1 state.
- It is connected to enable pin of latch 8282.

$\overline{\text{DEN}}$

Pin 26 (Output)

- This is a Data Enable signal.
- This signal is used to enable the transceiver 8286.
- Transceiver is used to separate the data from the address/data bus.
- It is an active low signal.

DT / $\overline{R}$

Pin 27 (Output)

- This is a Data Transmit/Receive signal.
- It decides the direction of data flow through the transceiver.
- When it is high, data is transmitted out.
- When it is low, data is received in.

M / $\overline{IO}$

Pin 28 (Output)

- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.

$\overline{WR}$

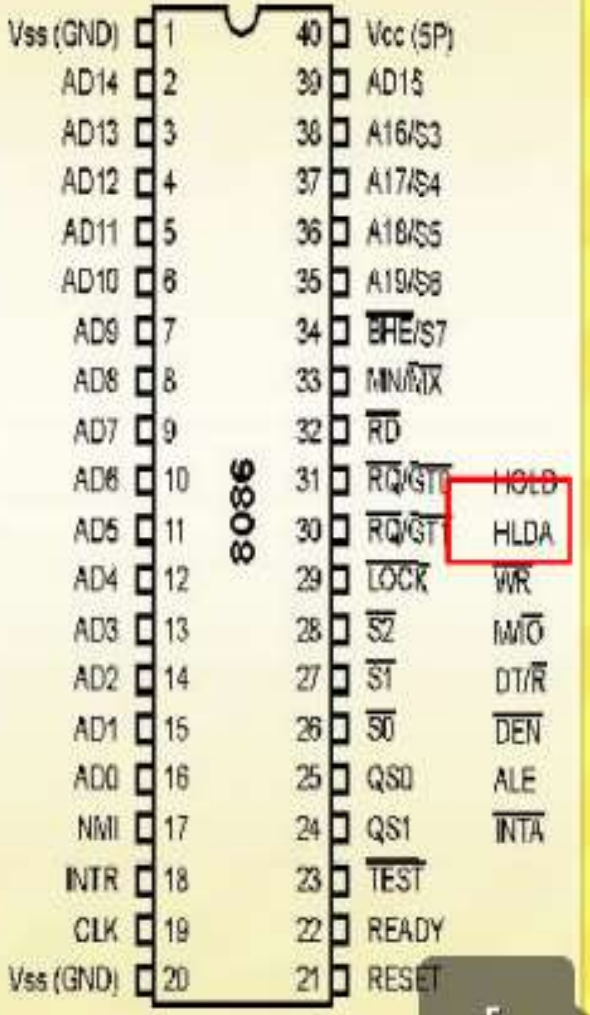
Pin 29 (Output)

- It is a Write signal.
- It is used to write data in memory or output device depending on the status of M/IO signal.
- It is an active low signal.

HLDA

Pin 30 (Output)

- It is a Hold Acknowledge signal.
- It is issued after receiving the HOLD signal.
- It is an active high signal.



HOLD

Pin 31 (Input)

- When DMA controller needs to use address/data bus, it sends a request to the CPU through this pin.
- It is an active high signal.
- When microprocessor receives HOLD signal, it issues HLDA signal to the DMA controller.

Pin Description for Maximum Mode

QS_1 and QS_0

Pin 24 and 25 (Output)

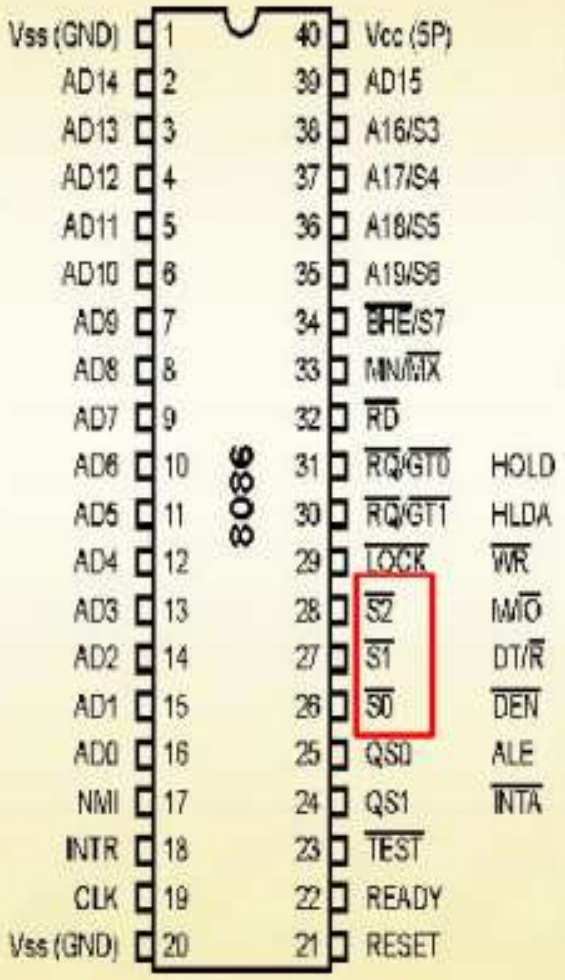
- These pins provide the status of instruction queue.

QS_1	QS_0	Status
0	0	No operation
0	1	1st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue

$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

- These status signals indicate the operation being done by the microprocessor.
- This information is required by the Bus Controller 8288.
- Bus controller 8288 generates all memory and I/O control signals.



$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$

Pin 26, 27, 28 (Output)

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Status
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

LOCK

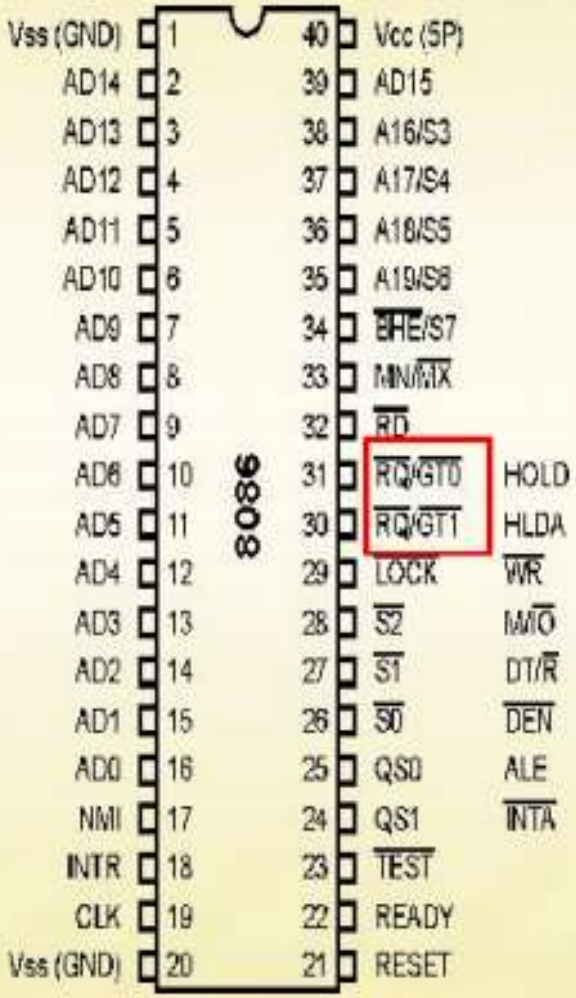
Pin 29 (Output)

- This signal indicates that other processors should not ask CPU to relinquish the system bus.
- When it goes low, all interrupts are masked and HOLD request is not granted.
- This pin is activated by using LOCK prefix on any instruction.

$\overline{RQ}/\overline{GT}_1$ and $\overline{RQ}/\overline{GT}_0$

Pin 30 and 31 (Bi-directional)

- These are Request/Grant pins.
- Other processors request the CPU through these lines to release the system bus.
- After receiving the request, CPU sends acknowledge signal on the same lines.
- $\overline{RQ}/\overline{GT}_0$ has higher priority than $\overline{RQ}/\overline{GT}_1$.



8086 MINIMUM MODE CONFIGURATION

When the MN/$\overline{MX}$ pin of the 8086 is wired to a +5 volt power supply, the processor operates in minimum mode. This mode is intended for small- and medium-sized systems employing only a single processor. All the control signals are generated by the 8086 processor itself. Figure shows such a minimum mode configurations system of 8086.

The minimum mode configuration of 8086 consists of:

1. Three 8-bit latches (IC 8282)
2. Two 8-bit transceivers (IC 8286)
3. One control signal generator
4. One clock generator (8284).

The latches are D-type flip-flops whose outputs are generally buffered. The common examples of latches are 8282 and 74LS373. These latches are used to demultiplexed the multiplexed lines, i.e. AD_0–AD_{15}, A_{16}/S_3–A_{19}/S_6 and $\overline{BHE}/S_7$. The ALE signal controls the D-FF in the latches.

The transceivers are used to separate the data bus from the multiplexed address/data bus. This chip consists of bidirectional buffers. The control signal generator is used to generate the four control signals, i.e. $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ and $\overline{MEMW}$. The clock generator is responsible for the generation of the required clock frequency and to synchronize the READY and RESET signals.

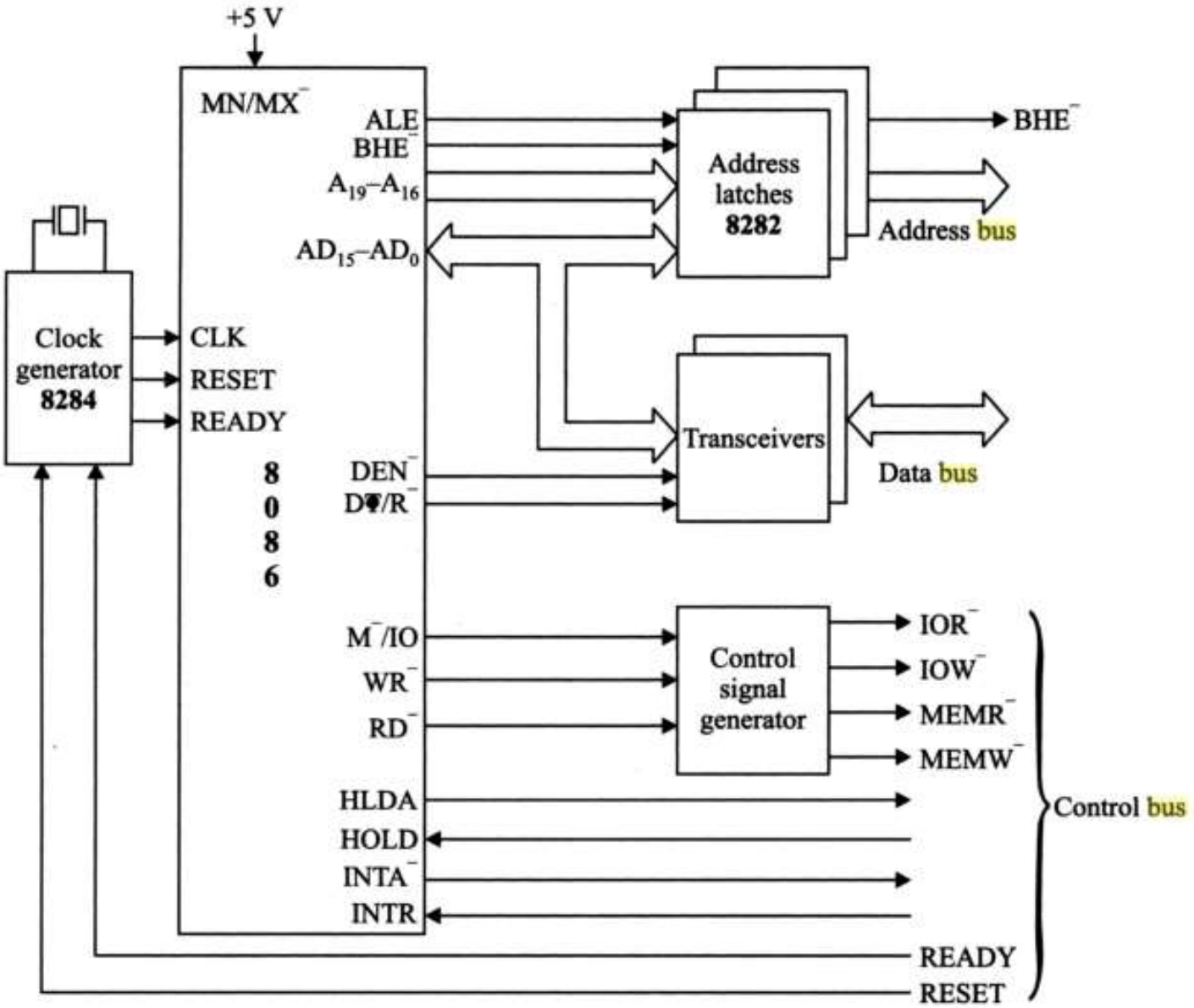


Figure Minimum mode configuration.

MAXIMUM MODE CONFIGURATION OF 8086

In the maximum mode of operation of 8086, more than one processor is present in the system, i.e. another processor is interfaced with 8086. The other processor may be either a numeric coprocessor 8087 or any other independent processor like 8086 or 8088. All the resources like memory, address bus, data buses are shared between the two processors.

The block diagram of the maximum mode configuration system of 8086 is shown in Figure In maximum mode three 8-bit latches (IC 8282), two 8-bit transceivers (IC 8286) and one clock generator (8284) are used along with the bus controller 8288.

The latches are used to demultiplex the multiplexed address/data lines and also address/ status signals. The two transceivers are used to enable the data flow and direction of the data flow. The clock generator is used to generate the clock and also synchronize the READY and RESET signals.

The control signals for maximum mode of operation are generated by the Bus Controller chip 8288. The three status outputs $\overline{S_0}, \overline{S_1}, \overline{S_2}$ from the processor are input to 8288. The outputs of the bus controller are the Control Signals, namely DEN, DT/$\overline{R}$, $\overline{IORC}$, $\overline{IOWTC}$, $\overline{MWTC}$, $\overline{MRDC}$, ALE, etc. These control signals perform the same task as the minimum mode operation. However, the DEN is an active HIGH signal which has to be converted to active LOW by means of an inverter.

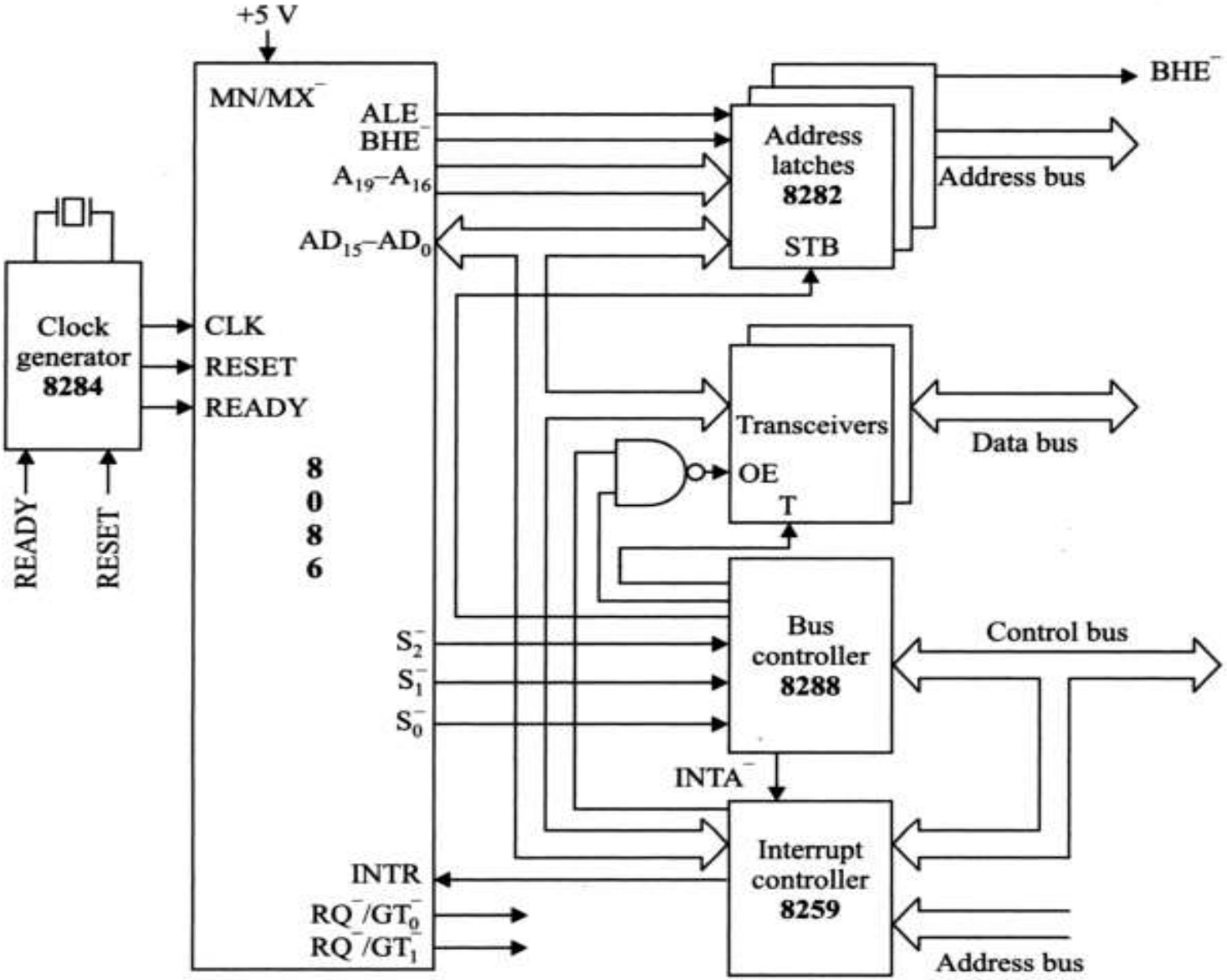


Figure Maximum mode configuration.

Opcode Fetch/Memory Read/IO Read Machine Cycle of 8086 in Minimum Mode

The microprocessors are clocked synchronous state machines, that is, they perform some action when they receive a clock edge. That's why we show the clock signal in the following diagrams: the processor bus unit takes some action when the clock signal occurs.

Bus Read Cycle (Memory or I/O)

1. The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a read or an input cycle.
2. At the beginning of T_1, the processor outputs AD_0–AD_{15}, A_{16}/S_3 to A_{19}/S_6, and $\overline{BHE}/S_7$.
3. The ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the $\overline{BHE}$ signal is latched when ALE goes low, providing the latched address A_0 to A_{19}.
4. During T_2, the processor removes the address and data. S_3 to S_6 and S_7 status is output on the upper 4 address/status lines of the processor.
5. The AD_0–AD_{15} signals are floated as inputs, waiting for data to be read.
6. Data bus transceivers (74HC245) are enabled towards the microprocessor (the READ direction) by the $DT/\overline{R}$ and $\overline{DEN}$ signals.
7. The $\overline{MRDC}$ (i.e. $\overline{MEMR}$) or $\overline{IORC}$ ($\overline{IOR}$) signal is asserted.
8. The signals are maintained during T_3. At the end of T_3, the microprocessor samples the input data.
9. During T_4, the memory and I/O control lines are de-asserted.

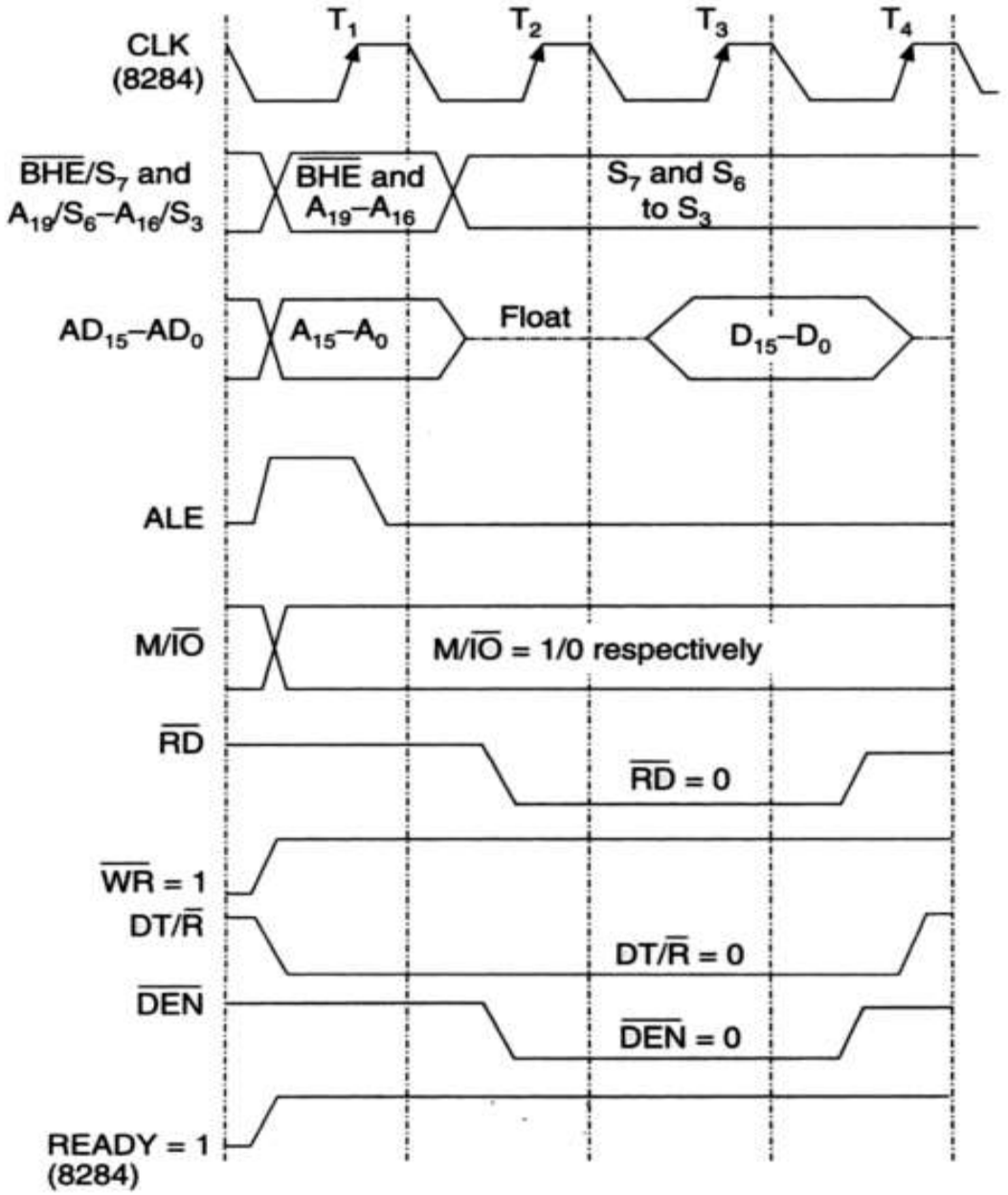


FIGURE Timing diagram of read machine cycle (Memory/IO) in minimum mode.

Opcode Fetch/Memory Read/IO Read Machine Cycle of 8086 in Maximum Mode

Bus Read Cycle (Memory or I/O)

1. The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a read or an input cycle.
2. At the beginning of T_1, the processor outputs $S_2\ \overline{S}_1, \overline{S}_0, \overline{AD_0} - AD_{15}$, A_{16}/S_3 to A_{19}/S_6, and BHE/S_7.
3. The 8288 bus controller transitions the ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the $\overline{BHE}$ signal is latched when ALE goes low, providing the latched address A_0 to A_{19}.
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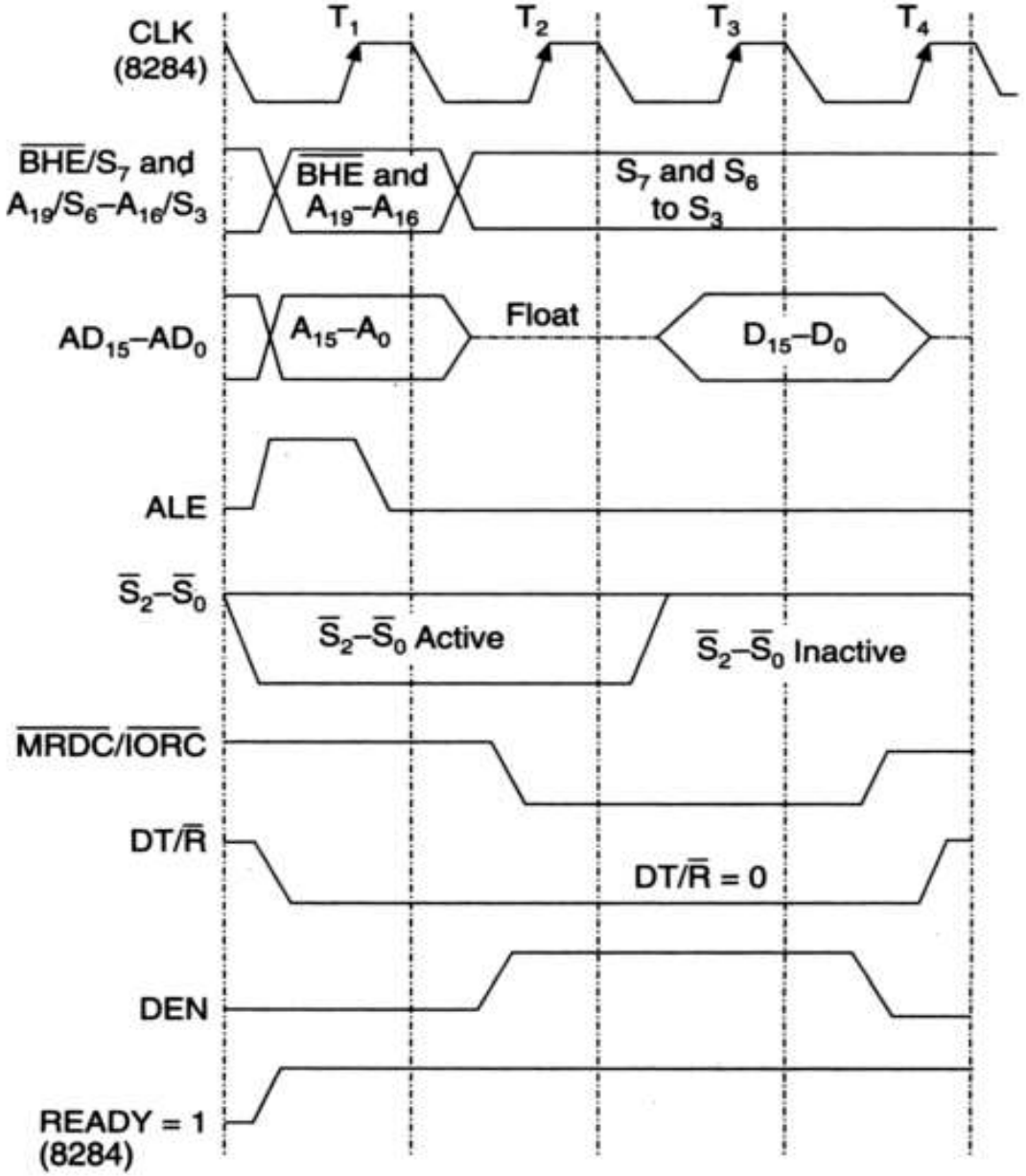

FIGURE Timing diagram of read machine cycle (Memory/IO) in maximum mode.

Memory Write/IO Write Machine Cycle of 8086 in Minimum Mode

Bus Write Cycle (Memory or I/O)

1. The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a write or an output cycle.
2. At the beginning of T_1, the processor outputs $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$, A16/S3...A19/S6, AD_0 to AD_{15}, and $\overline{BHE}$/S7.
3. The transitions of ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the $\overline{BHE}$ signal is latched when ALE goes low, providing the latched address A_0 to A_{19}.
4. During T_2, the processor removes the address and data. S_3 to S_6 status is output on the upper 4 address/status lines of the processor.
5. Output data is driven out on the AD_0 to AD_{15} lines.
6. Data bus transceivers (74HC245) are enabled away from the microprocessor (the WRITE direction) by the DT/$\overline{R}$ and $\overline{DEN}$ signals.
7. The $\overline{MWRC}$ (i.e. $\overline{MEMW}$) or $\overline{IOWC}$ ($\overline{IOW}$) signal is asserted at the beginning of T_3.
8. The signals are maintained during T_3.
9. During T_4, the memory and I/O control lines are de-asserted. In simple Intel Architecture systems, the data is usually written to the memory or output device at the rising edge of the $\overline{MWRC}$ or $\overline{IOWC}$ signal.

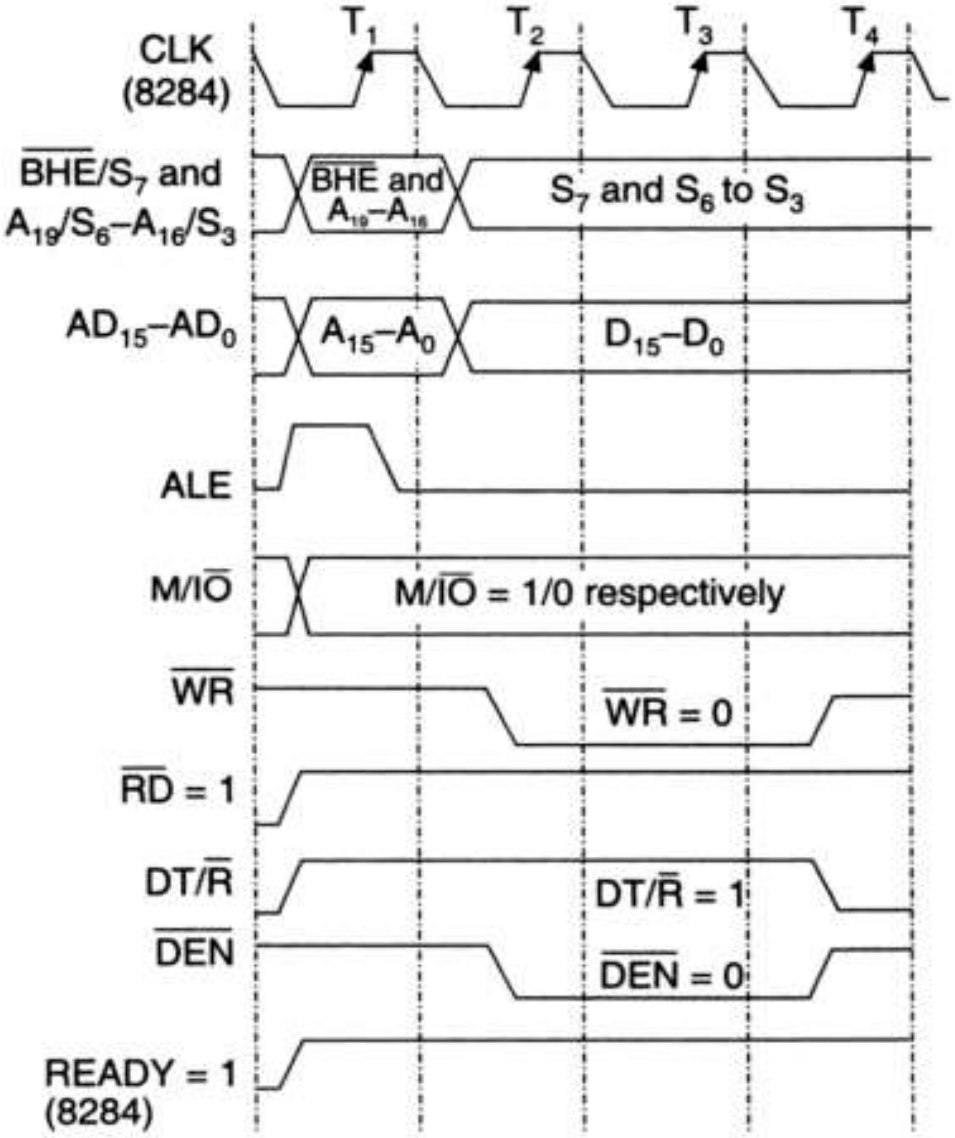

FIGURE Timing diagram of write machine cycle (Memory/IO) in minimum mode.

Memory/IO Write Machine Cycle of 8086 in Maximum Mode
Bus Write Cycle (Memory or I/O)

1. The 4 processor clock cycles are called T states. Four cycles is the shortest time that the processor can use for carrying out a write or an output cycle.
2. At the beginning of T_1, the processor outputs $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$, A16/S3...A19/S6, AD_0 to AD_{15}, and $\overline{BHE}$/S7.
3. The 8288 bus controller transitions the ALE signal from low to high, thereby allowing the address to pass through the transparent latches (74HC373). The address, along with the $\overline{BHE}$ signal is latched when ALE goes low, providing the latched address A_0 to A_{19}.
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5. Output data is driven out on the AD_0 to AD_{15} lines.
6. Data bus transceivers (74HC245) are enabled away from the microprocessor (the WRITE direction) by the $DT/\overline{R}$ and DEN signals.
7. The $\overline{MWRC}$ (i.e. $\overline{MEMW}$) or $\overline{IOWC}$ ($\overline{IOW}$) signal is asserted at the beginning of T_3.
8. The signals are maintained during T_3.
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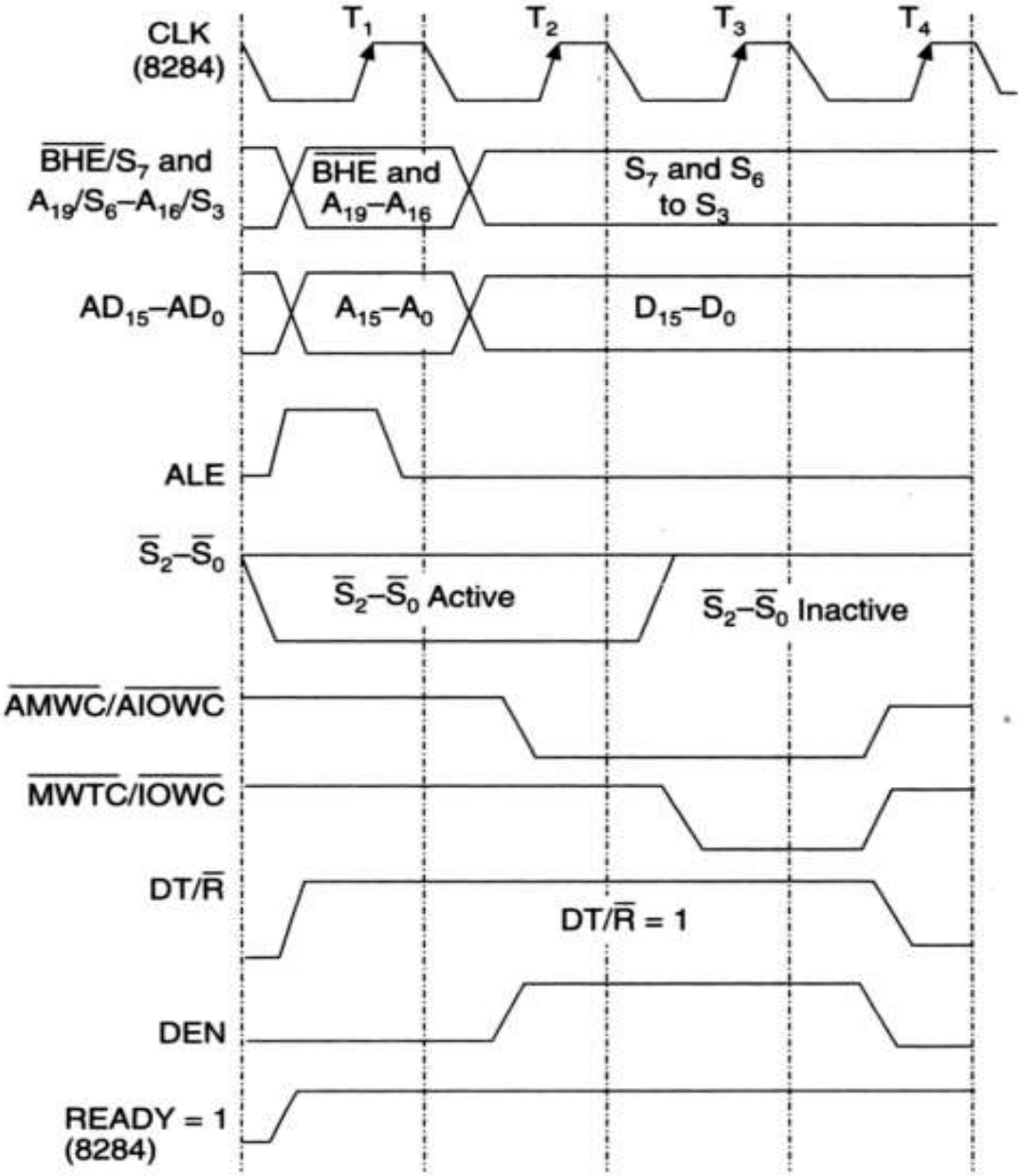

FIGURE Timing diagram of write machine cycle (memory/IO) in maximum mode.