CSE 3107: Microprocessor

Lecture # 4
The Architecture of 8085

Sujan Sarker

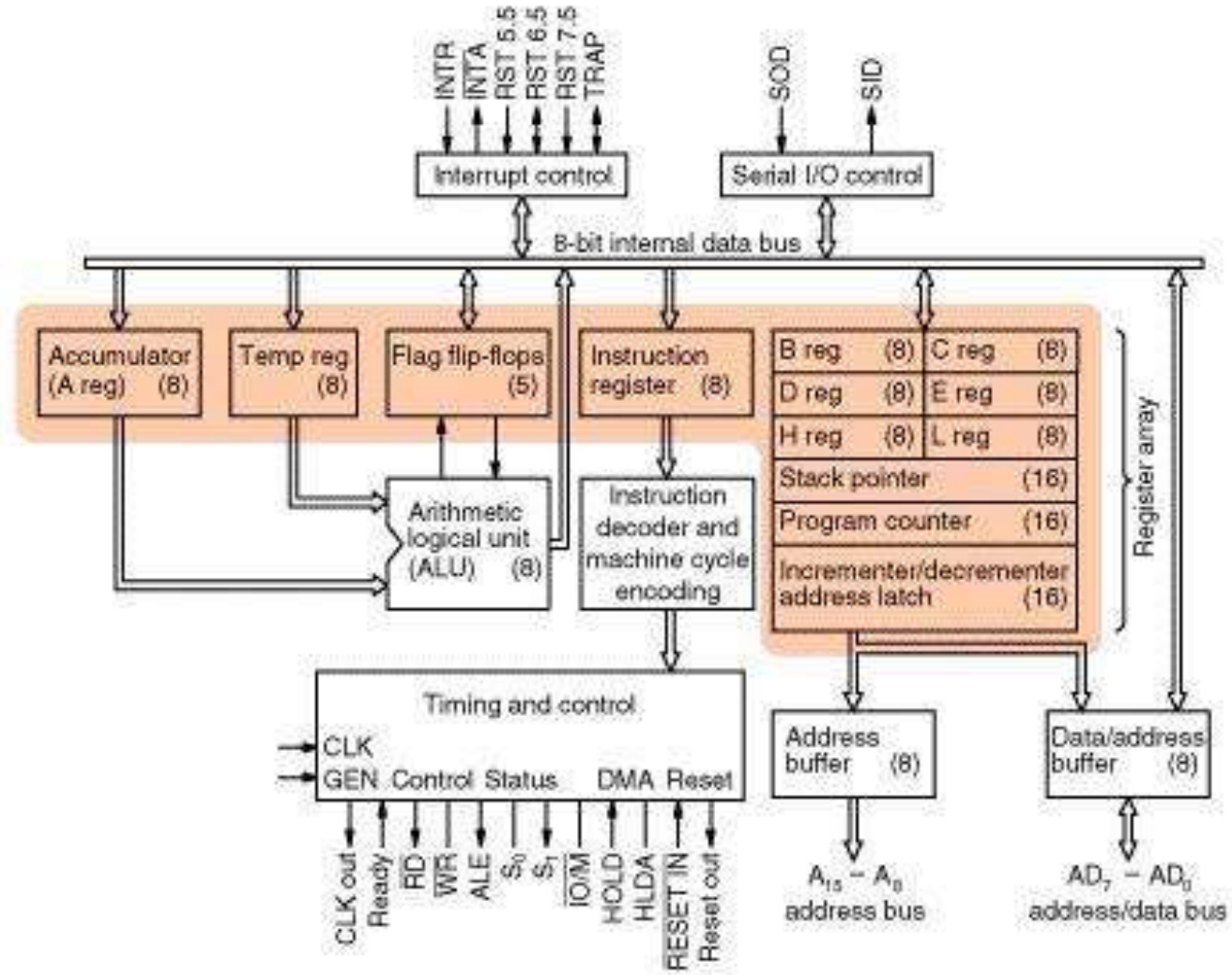
Lecturer, CSE, AUST

CSE | AUST

Spring 2017

Course Website: https://sites.google.com/site/sujanaustcse/courses-spring-2017/cse-3107/

8085 Microprocessor Architecture



Functional Blocks of 8085 ARCHITECTURE

- The various functional blocks of 8085 are as follows:

1. Registers
2. Arithmetic logic unit
3. Data/Address buffer
4. Increment /decrement address latch
5. Interrupt control
6. Serial I/O control
7. Timing and control circuitry
8. Instructions decoder and machine cycle encoder.

Description of 8085 ARCHITECTURE (1/8)

REGISTERS OF 8085:

S. No.	Name of the Register	Quantity	Capacity
1.	Accumulator (or) Register A	1	8-bit
2.	Temporary register	1	8-bit
3.	General purpose registers (B, C, D, E, H and L)	6	8-bit each
4.	Stack pointer (SP)	1	16-bit
5.	Program counter (PC)	1	16-bit
6.	Instruction register	1	8-bit
7.	Incrementer/Decrementer address latch	1	16-bit
8.	Status flags register	1	8-bit

1. ACCUMULATOR
   - This 8-bit register is the most important one amongst all the registers of 8085. Any data input/output to/from the microprocessor takes place via the accumulator (register). It is generally used for temporary storage of data and for the placement of final result of arithmetic/logical operations. Accumulator (ACC or A) register is extensively used for arithmetic, logical, store and rotate operations.

.

Description of 8085 ARCHITECTURE (2/8)

2. TEMPORARY REGISTERS

- The temporary data register of 8085 is an 8-bit register, which is not available to the programmer, but is used internally for execution of most of the arithmetic and logical operations.

3. GENERAL PURPOSE REGISTERS

- The general purpose registers of 8085 are: B, C, D, E, H and L. They are all 8-bit registers but can also be used as 16-bit register pairs—BC, DE and HL. These registers are also known as scratch pad registers.

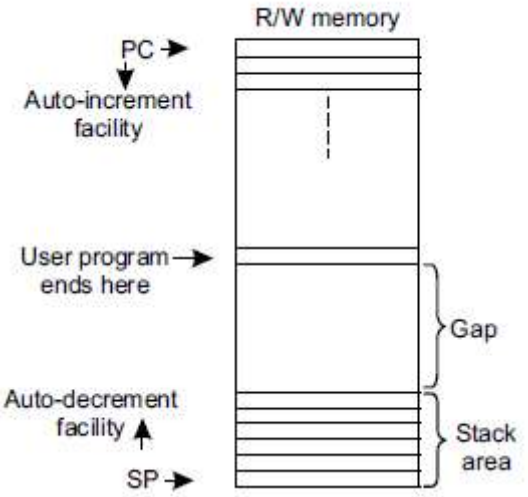
- HL register pair can be used as a data pointer or memory pointer.

- General purpose registers store temporary data during program execution, which can also be stored in different accessible memory locations. But storing temporary data in memory requires bus access—hence more time is needed to store. Thus it is always advisable to store data in general purpose registers.

Description of 8085 ARCHITECTURE (3/8)

4. PROGRAM COUNTER

• Program counter (PC) is a sixteen bit register which contains the address of the instruction to be executed just next. PC acts as a address pointer (also known as memory pointer) to the next instruction. As the processor executes instructions one after another, the PC is incremented—the number by which the PC increments depends on the nature of R/W memory the instruction. For example, for a 1-byte instruction, PC is incremented by one, while for a 3-byte instruction, the processor increments PC by three address locations.



5. STACK POINTER

• Stack pointer (SP) is a sixteen bit register which points to the 'stack'. The stack is an area in the R/W memory where temporary data or return addresses (in cases of subroutine CALL) are stored. Stack is a auto-decrement facility provided in the system. The stack top is initialized by the SP by using the instruction LXI SP, memory address.

• In the memory map, the program should be written at one end and stack should be initialized at the other end of the map—this is done to avoid crashing of program.

Description of 8085 ARCHITECTURE (4/8)

6. INSTRUCTION REGISTER

- Program written by the programmer resides in the R/W memory. When an instruction is being executed by the system, the opcode of the instruction is fetched from the memory and stored in the 8-bit instruction register. The opcode is loaded into the instruction register during opcode fetch cycle. It is then sent to the instruction decoder.

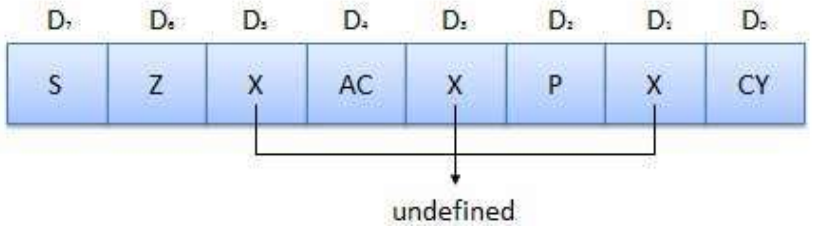
7. INCREMENT/DECREMENT ADDRESS LATCH

- This 16-bit register increments/decrements the contents of PC or SP when instructions related to them are executed.

Description of 8085 ARCHITECTURE (5/8)

8. STATUS FLAGS REGISTER

- It is an 8-bit register in which five bit positions contain the status of five condition flags which are Zero (Z), Sign (S), Carry (CY), Parity (P) and Auxiliary carry (AC). Each of these five flags is a 1 bit F/F. The flag register can't be written into. The flag register format is shown in Fig.



- **Sign (S) flag:** If the MSB of the result of an operation is 1, this flag is set, otherwise it is reset.
- **Zero (Z) flag:** If the result of an instruction is zero, this flag is set, otherwise reset.
- **Auxiliary Carry (AC) flag:** If there is a carry out of bit 3 and into bit 4 resulting from the execution of an arithmetic operation, it is set otherwise reset. This flag is used for BCD operation and is not available to the programmer to change the sequence of an instruction.
- **Carry (CY) flag:** If an instruction results in a carry (for addition operation) or borrow (for subtraction or comparison) out of bit D7, then this flag is set, otherwise reset.
- **Parity (P) flag:** This flag is set when the result of an operation contains an even number of 1's and is reset otherwise.

Description of 8085 ARCHITECTURE (6/8)

ALU

- ALU is responsible for all arithmetic and logic operations of MP.
- The ALU functions as a part which includes arithmetic logic group of circuits. This includes accumulator, flags F/Fs and temporary register blocks.
- 8085 does not have the above two instructions. It can neither multiply nor divide two 8-bit numbers. The same are executed by the processor following the process of repetitive addition or subtraction respectively.

Description of 8085 ARCHITECTURE (7/8)

SERIAL I/O CONTROL

- It is used to accept the serial 1 bit data by using SID and SOD signals and it can be performed by using SIM & RIM instruction.
- RIM instruction is used to input serial data through SID line
- SIM instruction is necessary to output data serially from SOD line.

INTERRUPT CONTROL

- It accepts different interrupts like TRAP, INT5.5,6.5,7.5and INTR.

ADDRESS / DATA BUFFERS

- 8-bit Temporary Storage for Data/Address before transmitting to or after receiving from Data/Address Bus.

INSTRUCTION DECODER & MACHINE CYLE ENCODING

- This section is responsible for decoding the opcode and provide this information to timing & control section.

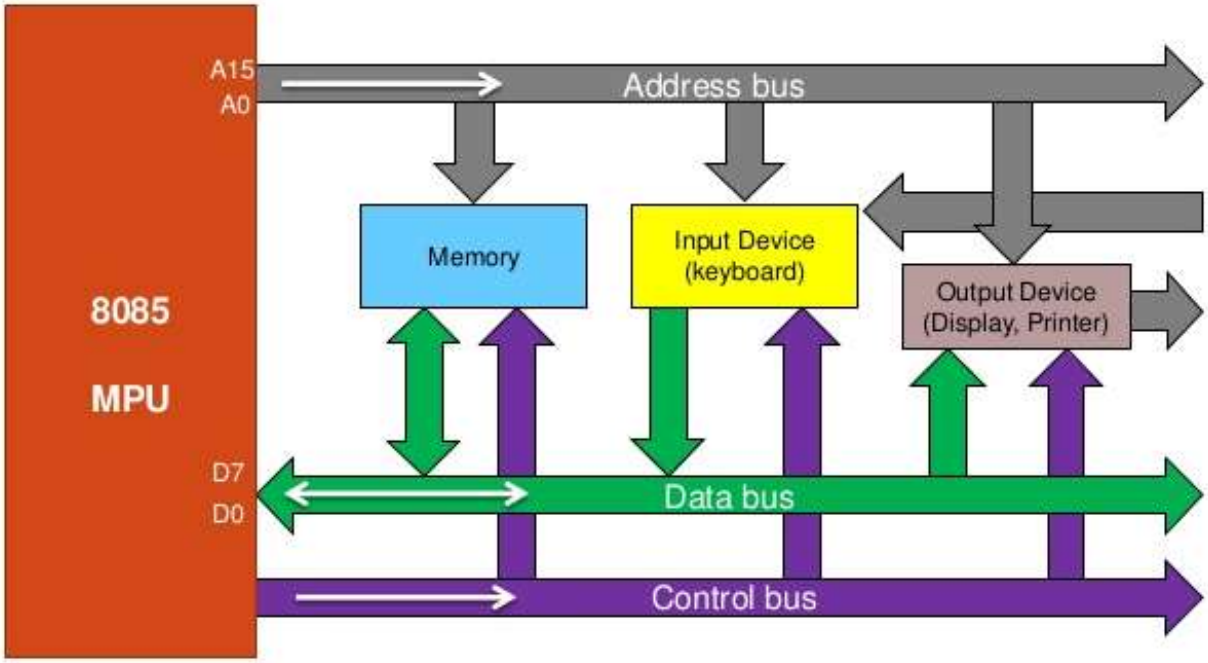
Description of 8085 ARCHITECTURE (8/8)

TIMMING AND CONTROL SECTION

- The T&C section is a part of CPU and generates timing and control signals for execution of instructions. This section includes Clock signals, Control signals, Status signals, DMA signals as also the Reset section. This section controls fetching and decoding operations. It also generates appropriate control signals for instruction execution as also the signals required to interface external devices.

The 8085 Bus Structure

- The microprocessor performs primarily four operations:
    I. Memory Read: Reads data (or instruction) from memory.
    II. Memory Write: Writes data (or instruction) into memory.
    III. I/O Read: Accepts data from input device.
    IV. I/O Write: Sends data to output device.
- The 8085 processor performs these functions using address bus, data bus and control bus.



The Address Bus

- 16 bits wide (A_0 $A_1 \ldots A_{15}$)
  - 16 address lines are capable of addressing a Total of $2^{16} = 65{,}536$ (64k) memory locations. Address locations: 0000 (hex) – FFFF (hex)

- "Unidirectional".
  - Information flows out of the microprocessor and into the memory or peripherals.

- When the 8085 wants to access a peripheral or a memory location, it places the 16-bit address on the address bus and then sends the appropriate control signals.

The Data Bus

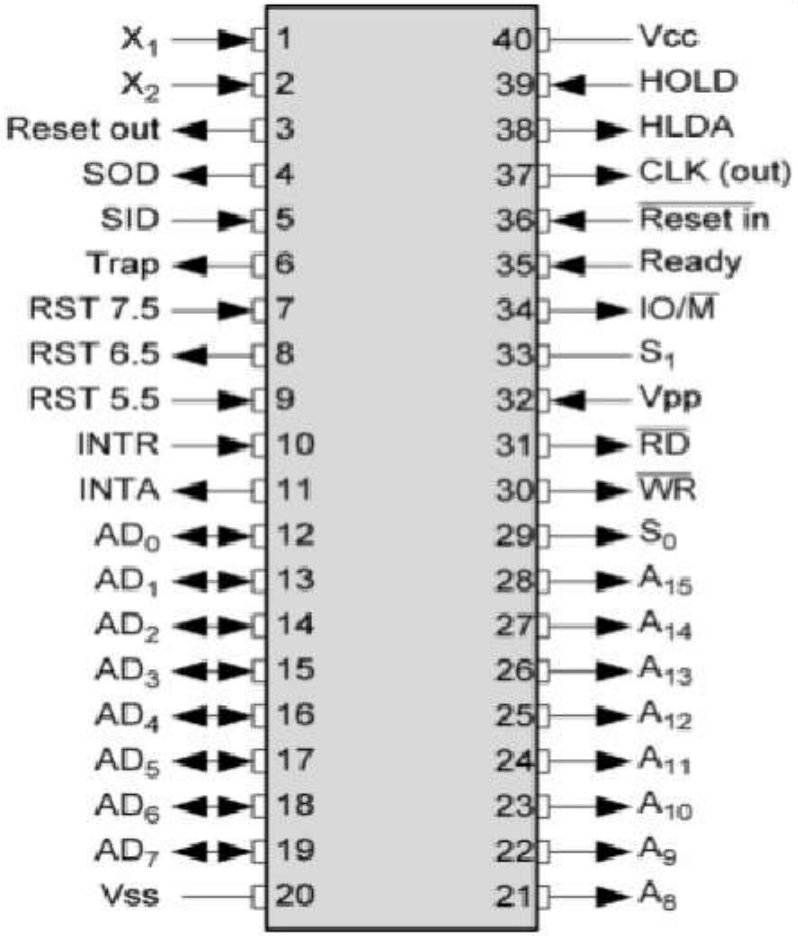
- 8 bits wide (D_0 D_1…D_7)
  - Data range: 00 (hex) – FF (hex)
- "Bi-directional".
  - Information flows both ways between the microprocessor and memory or I/O.
- The 8085 uses the data bus to transfer the binary information.
- Since the data bus has 8-bits only, then the 8085 can manipulate data 8 bits at-a-time only.

The Control Bus

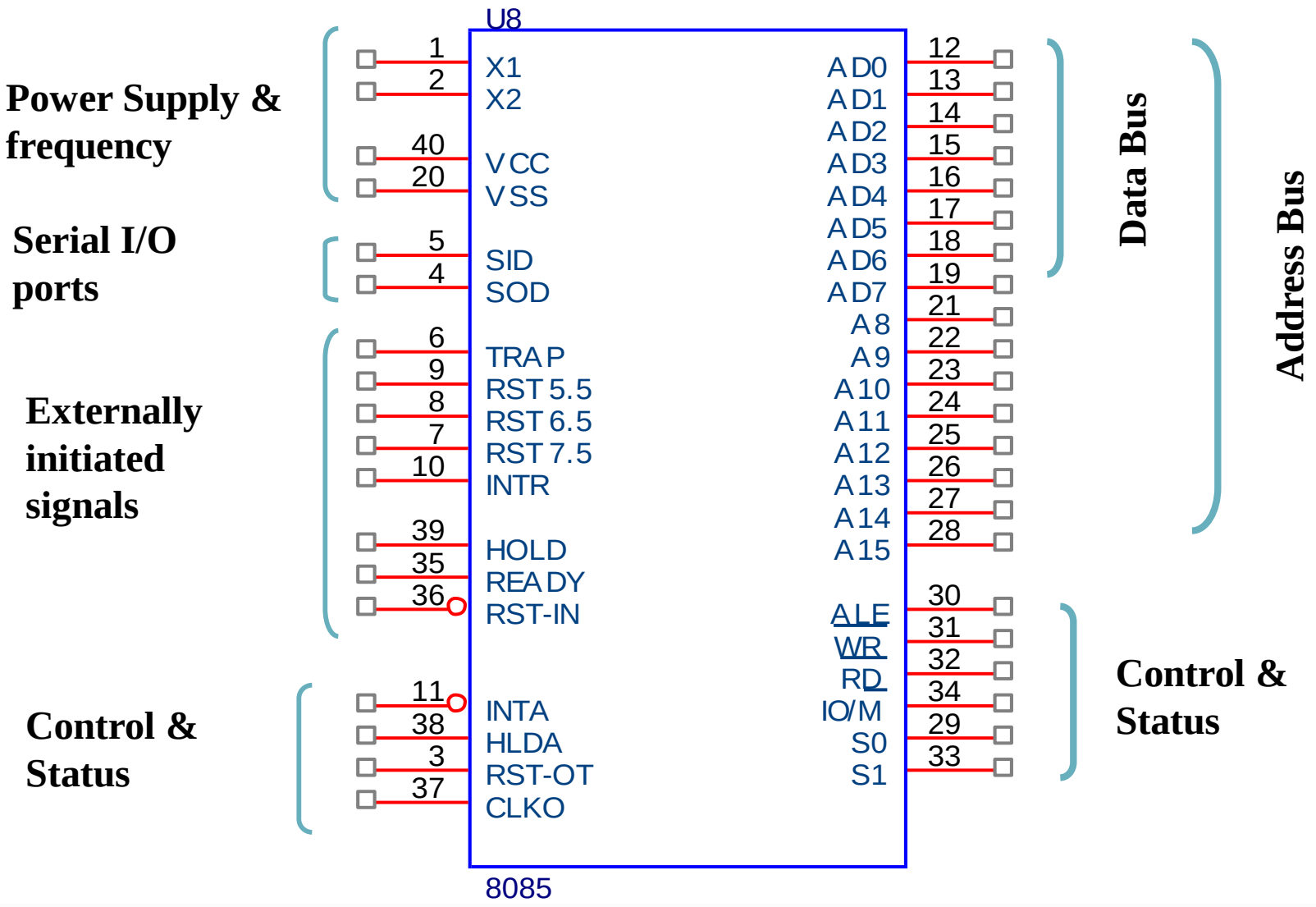
- Comprised of various single lines that carry synchronization signals.
- The MPU uses such lines to provide timing or synchronization signals (control signals).

Pin Diagram of 8085

- A 40-pin IC
- Six groups of signals
  - Address Bus
  - Data Bus
  - Control and Status pins
  - Power Supply & frequency signals
  - Externally initiated Signals
  - Serial I/O ports



Logic Pinout of 8085



8085 Pin Diagram Description (1/7)

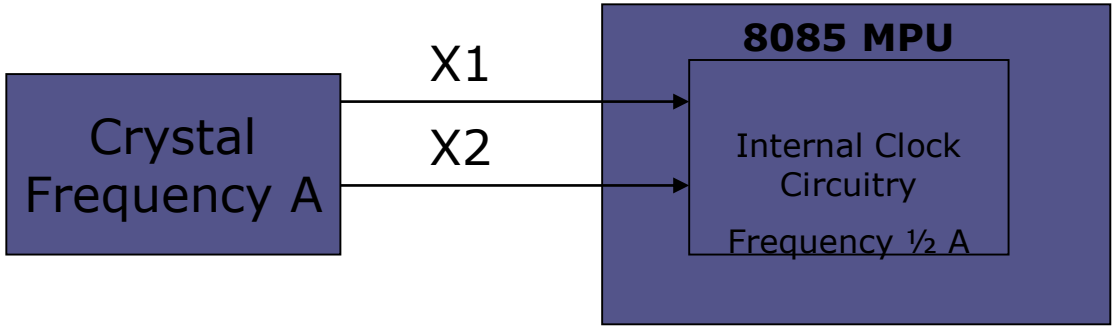
ADDRESS BUS, DATA BUS & ALE

- More functions then 8080 are added therefore less number of pins remain, therefore It has multiplexed address and data bus.(AD0-AD7) from Pin 12 through 19.
- Least Significant 8 Lines of Address Bus shared with 8-bit Data Bus.
- Multiplexed means selecting one at a time, First pins 12-19 work as Address Bus to send address then works as Data Bus to carry Data.
- When these Pins worked as Data Bus and When as Address Bus is Decided by ALE (Address Latch Enable) Output Pin Number 30 Signal.
- When ALE = 1 its Adress, when ALE = 0 its Data.

8085 Pin Diagram Description (2/7)

Power & Clock Signals

- 8085 MPU works on Single +5V Power Supply
- Pin 40 & 20: Vcc is Power and Vss is Ground
- Pin 1 & 2 : X1 & X2 are Input pins that are connected from a crystal to the internal clock circuitry of 8085 MP
- Pin 37: CLK is a Output Pin and it is used for timing & synchronization of other peripherals by MP



8085 Pin Diagram Description (3/7)

RESTART SIGNALS

- Pin 36: $\overline{\text{RESET IN}}$ is Input Pin if it is 0 then it will reset MPU and set Program counter to address 000H
- Data Bus Address Bus and Control lines are TRI-STATED during a Reset. Tri-state means MP will release their control & they are isolated from MP, and any other peripheral can take control of them.
- Pin 3: RESET OUT is a Output pin, if it is 1 then it will inform all peripherals that System is restart.

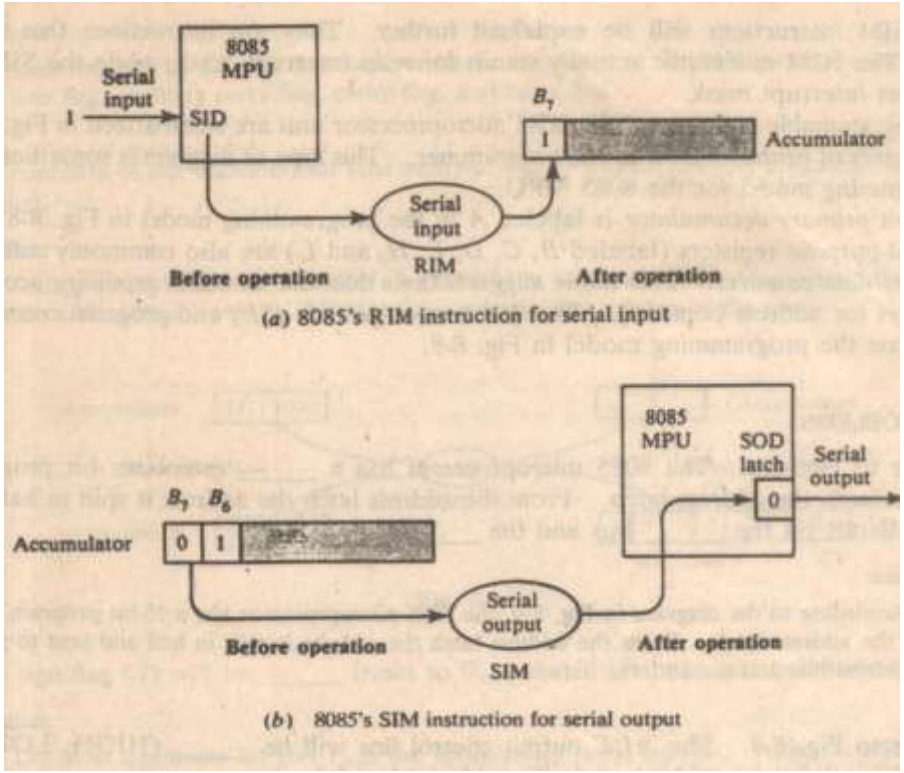
8085 Pin Diagram Description (4/7)

SERIAL INPUT & OUTPUT SIGNALS

• 8085 has two pins for serial data input and output so, serial devices can be directly interfaced with 8085.

• Pin 5: SID is a Serial Input Pin, it is used to input serial data (i.e. one bit at a time) to MSB of Accumulator. This Pin is control by RIM instruction.

• Pin 4: SOD is Serial Output Pin, it is used to send serial data, by SIM instruction.



8085 Pin Diagram Description (5/7)

READY & HOLD SIGNALS

- Pin 35: is READY input port, it is used by other peripherals to inform MP that they are ready to send or receive data
- If READY pin is low means 0 then MP will be in wait state until again the REDY signal is high 1, this mostly occur frequently because of low speed of other peripherals
- Pin39: is HOLD input signal, used by other peripherals to request MP that they want to use the Data & Address Bus (may occur in DMA operations)
- Upon receiving HOLD signal, MP will first finish its own data transfer on busses then
- Address Bus, Data Bus, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$ pins are Tri-stated (means isolated from MP)
- Pin 38: HOLDA, is a Output signal, it is an Acknowledgement to peripheral requesting HOLD, and it inform the requesting peripheral that MP is going to release the control of Buses in next clock cycle

8085 Pin Diagram Description (6/7)

MACHINE CYCLE

- Pins 33: S1, 29: S0, 34: IO/$\overline{M}$ are Output signals that are used to inform other peripherals that what type of machine cycle MP is running.
- IO/M(output): It is a signal that distinguished between a memory operation and an I/O operation.
- When IO/$\overline{M}$ = 0 it is a memory operation and IO/$\overline{M}$ = 1 it is an I/O operation.
- S1 and S0 (output): These are status signals used to specify the type of operation being performed.

S1	S0	States
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

Machine Cycle	Status IO/$\overline{M}$	Status S_1	Status S_0	Control Signals
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA}$ = 1
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified

8085 Pin Diagram Description (7/7)

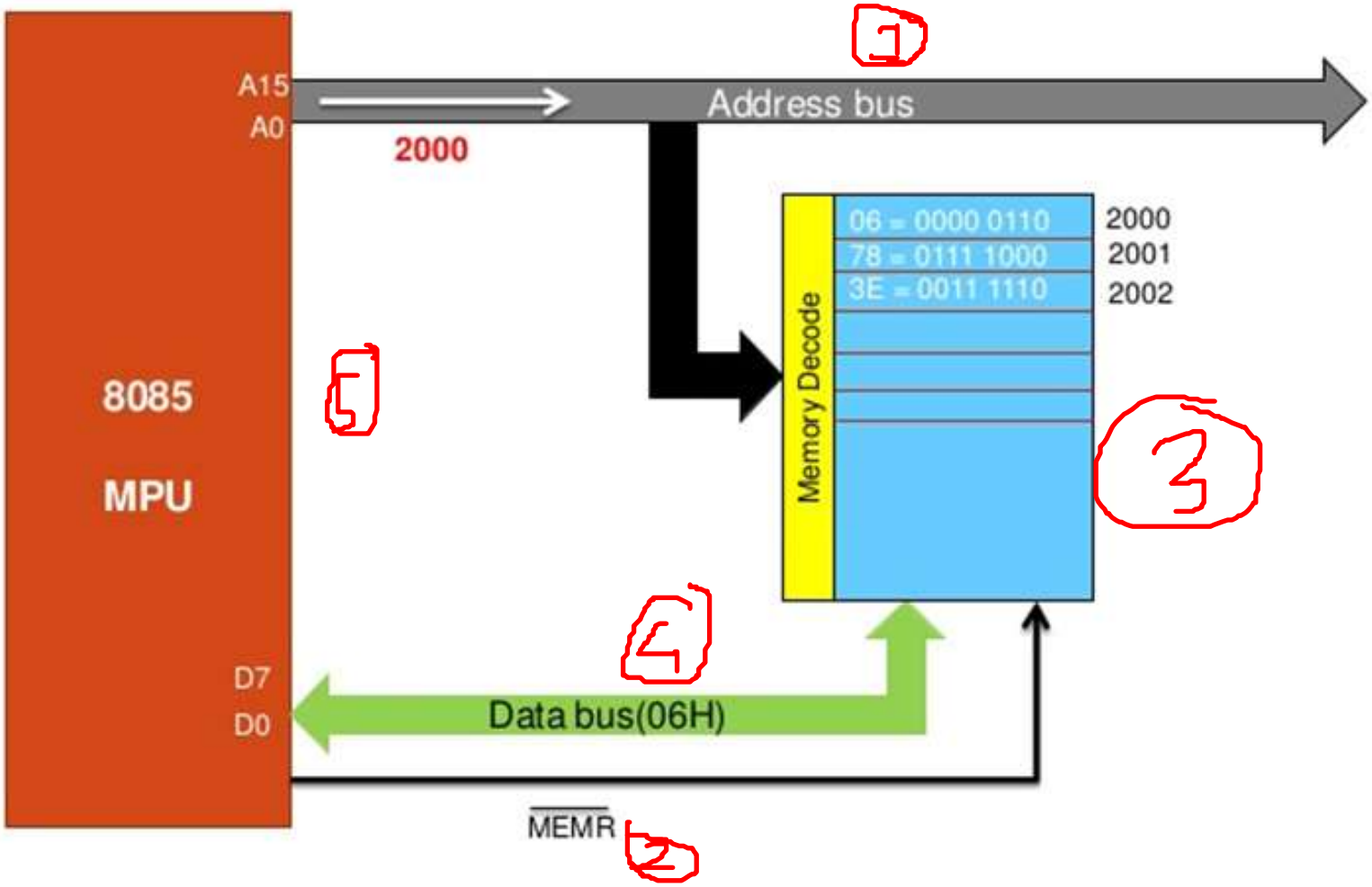
Interrupts SIGNALS

- An interrupt is a signal that alter the normal execution of Microprocessor
- In 8085 there are 5 interrupts Inputs through these interrupt signals can be sent to MP
  - TRAP
  - RST 7.5
  - RST 6.5
  - RST 5.5
  - INTR
- When MP receive interrupt it Acknowledged the interrupting device through $\overline{\text{INTRA}}$ output signal
- Those interrupts that can be enabled or disabled by software are called Maskable interrupts e.g.: RST 7.5, RST 6.5, RST 5.5, INTR
- Those interrupts that can not be disabled are called Non-Maskable interrupts e.g. TRAP

8085 Interrupts and Externally Generated Signals

☐ INTR (Input)	Interrupt Request: This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080A.
☐ $\overline{\text{INTA}}$ (Output)	Interrupt Acknowledge: This is used to acknowledge an interrupt.
☐ RST 7.5 (Inputs) RST 6.5 RST 5.5	Restart Interrupts: These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
☐ TRAP (Input)	This is a nonmaskable interrupt and has the highest priority.
☐ HOLD (Input)	This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of the address and data buses.
☐ HLDA (Output)	Hold Acknowledge: This signal acknowledges the HOLD request.
☐ READY (Input)	This signal is used to delay the microprocessor Read or Write cycles until a slow-responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

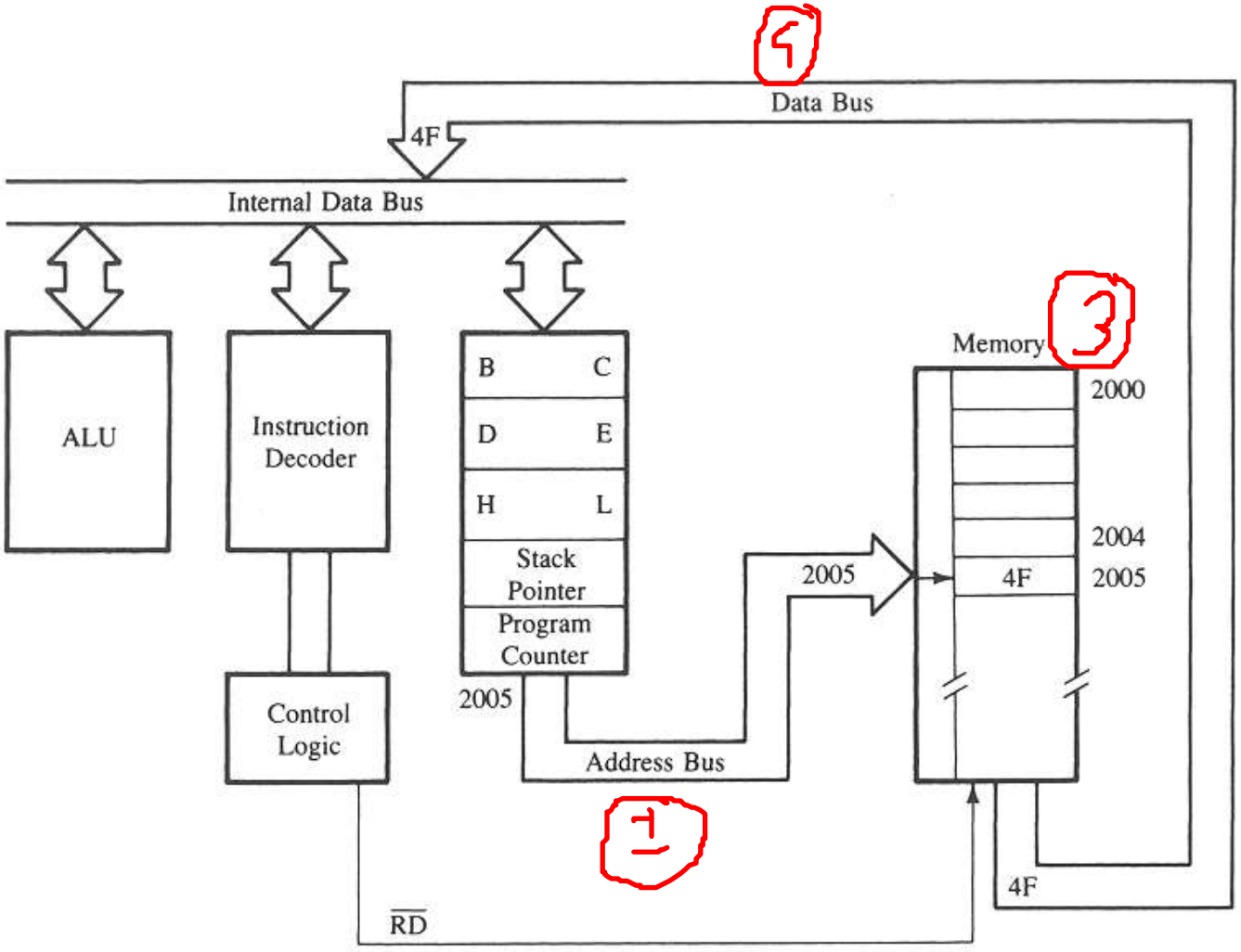
Memory Read Operation



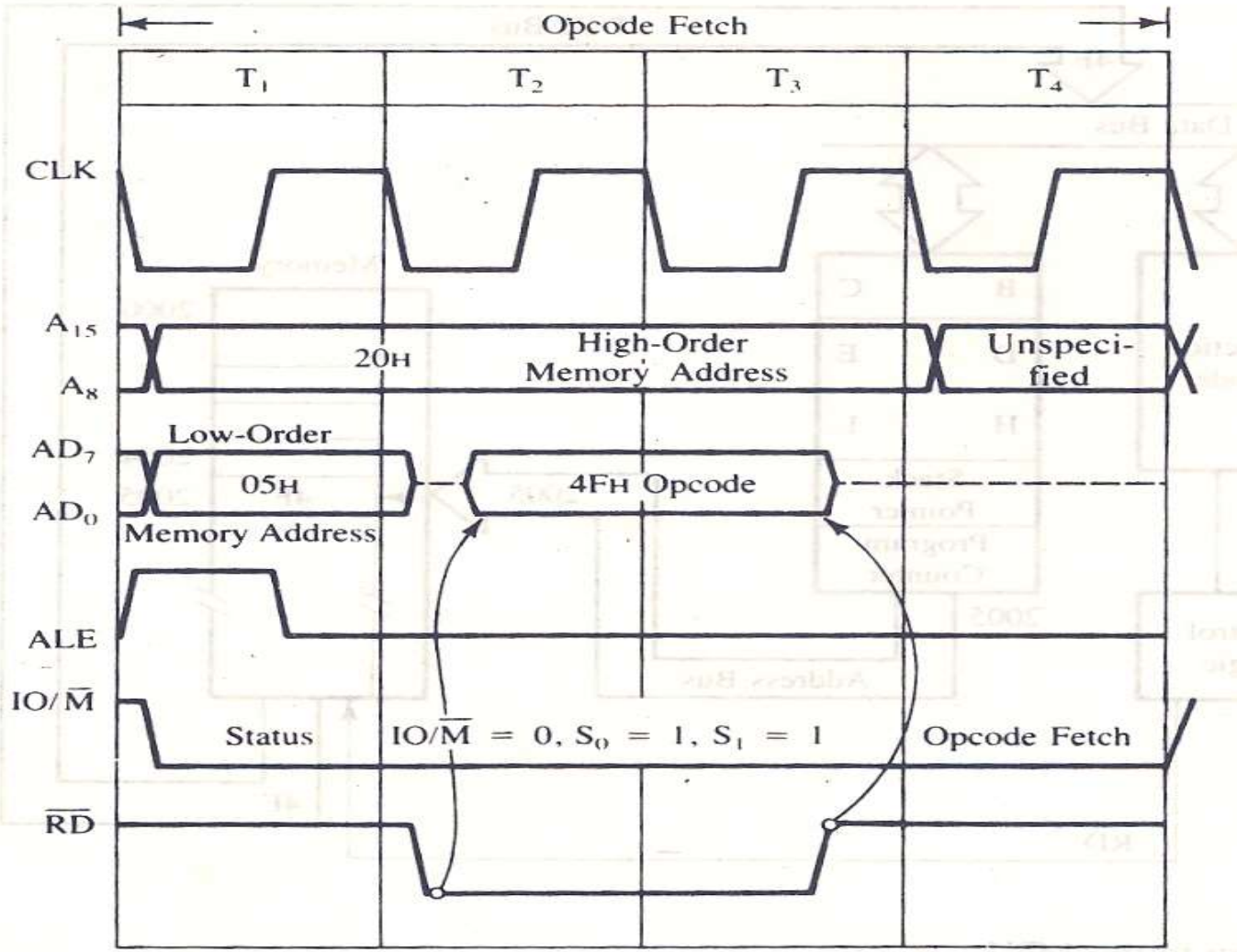
Memory Read Operation (Cont.)

- To read the contents of a memory location, the following steps take place:
  - The microprocessor places the 16-bit address of the memory location on the address bus.
  - The microprocessor activates a control signal called “memory read” which enables the memory chip.
  - The memory decodes the address and identifies the right location.
  - The memory places the contents on the data bus.
  - The microprocessor reads the value of the data bus after a certain amount of time.

Memory Read Operation (Cont.)



Timing Diagram (Cont.)



Thank You ☺