

(1)

Ahsanullah University of Science and Technology

Date: 08/03/2017

Department of Computer Science and Engineering

Third Year, First Semester

Final Examination, Fall 2016

Course No: CSE 3109

Course Title: Digital System Design

Time: 3 Hours

Full Marks: 70

[There are 7(Seven) questions. Answer any 5(Five) questions.]
 [Marks allotted are indicated in the right margin within '()' .]

- 1.a) What is Modified Booth's algorithm? Explain with example. [4]
- b) If $m = 11010$, $r = 01101$, $x = 5$ and $y = 5$; using the Booth's multiplication algorithm determine the initial value of A , S and P . Show all the steps of Booth's algorithm to find the final value of P . [5]
- c) Design a 6×6 bit booth's multiplier. Draw the circuit block diagram. [5]
- d) What is the difference between RAM and ROM? Describe the write and read operations of a RAM. [4]
- b) Prove that the multiplication of two n -digit numbers in any base r gives a product of no more than $2n$ digits in length. [4]
- c) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. Derive the PLA program table for this circuit. [6]
- 3.a) What is programmable logic array? Draw the block diagram of PLA. [3]
- b) Draw the LDA and SUB routines of SAP-I and also their fetch and execution timing diagram. [5]
- c) Describe the architecture of SAP-2. [6]
- 4.a) What is mnemonics? Explain with example. [2]
- b) What is Ring Counter? Draw the symbol and clock and timing signals of a Ring Counter. [3]
- c) How much time delay does this SAP -2 subroutine produce? [3]

```

MVI B,0AH
LOOP1: MVI C,47H
LOOP2: DCR C
JNZ LOOP2
DCR B
JNZ LOOP1
RET
    
```

- d) Serial data is sometimes called a serial data stream because bits flow one after another. In SAP-2 a serial data stream drives bit 7 of port 2 at a rate of approximately 600 bits per second. Write a program that inputs an 8-bit character in a serial data stream and stores it in memory location 2100H. [6]
- 5.a) What is the difference between hard-wired control and microprogram control? What are the advantage and disadvantage in each method? [4]

- (2)
- b) The state diagram of a control unit is shown in Figure 1. It has four states and two inputs x and y .
- i) Design the control using eight D flip-flops. [4]
- ii) Design the control using three J-K flip-flops and a 3×8 decoder. [4]
- iii) Design the control using a PLA. [4]

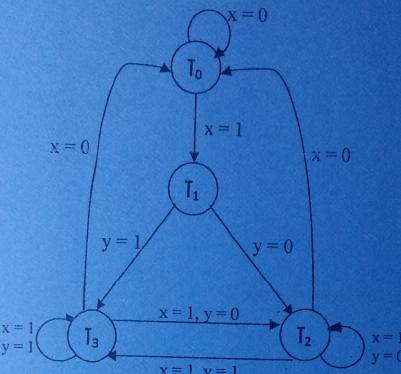


Figure 1: control state diagram for problem 5 b)

- 6.a) Design an arithmetic logic unit with three selection variables S_2 , S_1 and S_0 , that generates the following arithmetic and logic operations. When $S_2=0$ the arithmetic operations are done and when $S_2=1$ the logical operations are done. [7]

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$	$C_{in} = x$ (don't care)
0	0	$F = A$	$F = A + I$	$F = A + B$ (OR)
0	1	$F = A - B - 1$	$F = A - B$	$F = A \oplus B$ (XOR)
1	0	$F = B - A - 1$	$F = B - A$	$F = AB$ (AND)
1	1	$F = A + B$	$F = A + B + 1$	$F = A \uparrow B$ (NAND)

- b) The symbolic micropogram for control memory is given below:

ROM address	Microinstruction	Comments
0	$x = 1$, if ($q_s = 1$) then (go to 1), if ($q_a = 1$) then (go to 2), if ($q_s \wedge q_a = 0$) then (go to 0)	Load 0 or external address
1	$B_s \leftarrow B_s'$	$q_s = 1$, start subtraction
2	If ($S = 1$) then (go to 4)	$q_a = 1$, start addition
3	$A \leftarrow A + B$, $E \leftarrow C_{out}$, go to 0	Add magnitudes and return
4	$A \leftarrow A + B' + 1$, $E \leftarrow C_{out}$	Subtract magnitudes
5	If ($E = 1$) then (go to 0), $E \leftarrow 0$	Operation terminated if $E = 1$
6	$A \leftarrow A'$	$E = 0$, complement A
7	$A \leftarrow A + 1$, $A_s \leftarrow A_s'$, go to 0	Done, return to address 0

Here L variable loads A and E from ALU, y variable complements B_s , z variable complements A_s , and w variable clears E . And the ALU has the following function table:

(3)

S_2	S_1	S_0	C_{in}	Output
0	0	1	0	$F = A + B$
0	1	0	1	$F = A - B$
1	1	1	0	$F = A'$
0	0	0	1	$F = A + 1$

Write the binary microprogram for the control memory and also draw microprogram control block diagram.

What are the values of status bits C and Z after the subtraction of two unsigned numbers ($A - B$)?

Design an arithmetic circuit that multiplies two fixed-point binary numbers in sign-magnitude representation. The product obtained from the multiplication of two binary numbers whose magnitudes consist of k bits each can be up to $2k$ bits long. The sign of each number occupies one additional bit. Your design must include the following steps:

- i. Equipment Configuration
- ii. Derivation of Algorithm
- iii. Flowchart
- iv. Control state diagram and Sequence of microoperations
- v. Design of Hard-wired Control

(4)

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

Third Year, First Semester Final Examination, Fall 2015

Course No: CSE 3109

Course Title: Digital System Design

Full Marks: 70

Time: 3 Hours

[There are 7(Seven) questions. Answer any 5(Five) questions.]
[Marks allotted are indicated in the right margin within '[]'.]

- 1.a) What is programmable logic array? Draw the block diagram of PLA. [3]
- 1.b) A combinational circuit is defined by the functions:

$$F_1(A,B,C) = \sum (3, 5, 6, 7)$$

$$F_2(A,B,C) = \sum (0, 2, 4, 7)$$

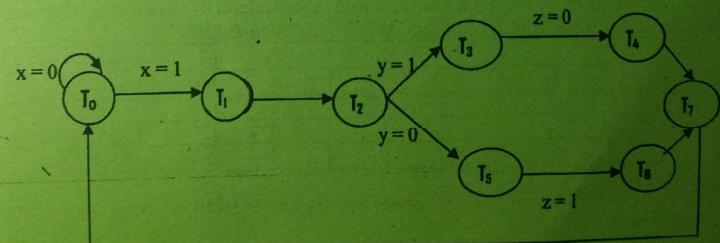
Implement the circuit with a PLA having three inputs, four product terms, and two outputs.
- 1.c) The traffic lights on a main road show green for 50 s, yellow for 6 s, and red for 30 s. Bits 1, 2 and 3 of port 4 of SAP-2 are the control inputs to peripheral equipment that runs these traffic lights. Write a program in mnemonics for SAP-2 that produces time delays of 50, 6 and 30 s for the traffic lights. [6]
- 2.a) What is Shift Register? What are the differences between RAM and ROM? [4]
- 2.b) Describe the architecture of SAP-1. [6]
- 2.c) Write a program for SAP-1 to solve this arithmetic problem.

$$16 + 20 + 24 - 32$$

The numbers are in decimal form.
- 3.a) Design a 4-bit binary counter. [4]
- 3.b) What is Modified Booth's algorithm? Explain with example. [4]
- 3.c) Show all the steps of Booth's algorithm for the following 6 bit numbers:

$$X = 10 \quad Y = -16$$
 [6]
- 4.a) The state diagram of a control unit is shown in Figure 1. It has eight states and three inputs x , y and z . Design the control by the sequence register and decoder method with JK flip-flops G3, G2 and G1. Use the flip-flop outputs as conditions for the present states. [10]

Figure 1: control state diagram for problem 4 a)



5. (b) What is the difference between hard-ware control and microprogram control? What are the advantage and disadvantage in each method? [4]

- 5.a) Draw the block diagram of an 8-bit ALU with a 4-bit status register. The four status bits are symbolized by C, S, Z and V. [3]

- b) Prove that the multiplication of two n -digit numbers in any base r gives a product of no more than $2n$ digits in length. [4]

- c) Design an arithmetic circuit with two selection variables S_1 and S_0 , that generates the following arithmetic operations. Draw the logic diagram of one typical stage. [7]

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A$	$F = A + 1$
1	0	$F = B'$	$F = B' + 1$
1	1	$F = A + B'$	$F = A + B' + 1$

- 6.a) The following register-transfer operations specify a four-state control of the sequence register and decoder type. G is a 2-bit sequence register and T_0 , T_1 , T_2 and T_3 are the outputs of the decoder. [7]

$$xT_0: \quad G \leftarrow G+1$$

$$yT_0: \quad G \leftarrow 10$$

$$zT_0: \quad G \leftarrow 11$$

$$T_1+T_2+T_3: \quad G \leftarrow G+1$$

Draw the state diagram of the control and design the sequence register with JK flip-flops.

- b) The symbolic microprogram for control memory is given below: [7]

ROM address	Microinstruction	Comments
0	$x = 1, \text{if } (q_s = 1) \text{ then (go to 1), if } (q_a = 1) \text{ then (go to 2), if } (q_s \wedge q_a = 0) \text{ then (go to 0)}$	Load 0 or external address
1	$B_s \leftarrow B_s'$	$q_s = 1, \text{ start subtraction}$
2	If ($S = 1$) then (go to 4)	$q_a = 1, \text{ start addition}$
3	$A \leftarrow A + B, E \leftarrow C_{out}, \text{ go to 0}$	Add magnitudes and return
4	$A \leftarrow A + B' + 1, E \leftarrow C_{out}$	Subtract magnitudes
5	If ($E = 1$) then (go to 0), $E \leftarrow 0$	Operation terminated if $E = 1$
6	$A \leftarrow A'$	$B = 0, \text{ complement } A$
7	$A \leftarrow A + 1, A_s \leftarrow A_s', \text{ go to 0}$	Done, return to address 0

Here L variable loads A and E from ALU, y variable complements B_s , z variable complements A_s and w variable clears E. And the ALU has the following function table:

S_2	S_1	S_0	C_{in}	Output
0	0	1	0	$F = A + B$
0	1	0	1	$F = A - B$
1	1	1	0	$F = A'$
0	0	0	1	$F = A + 1$

Write the binary microprogram for the control memory and also draw microprogram control block diagram.

- 7.a) Draw the block diagram and logic diagram of a RAM. [2]

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering

Third Year, First Semester

Final Examination, Spring 2016

Course No: CSE 3109

Course Title: Digital System Design

Time: 3 Hours

Date: 27/09/2016

[There are 7(Seven) questions. Answer any 5(Five) questions.]

[Marks allotted are indicated in the right margin within '[]'.]

Full Marks: 70

1.a) What is Register? What are the differences between SRAM and DRAM? [3]

b) Show all the steps of Booth's algorithm for the following 6 bit numbers:

$$X = -8 \quad Y = -9$$

[5]

c) Design a 5×5 bit booth's multiplier. Draw the circuit block diagram. [6]

2.a) What is Arithmetic Logic Unit? [2]

b) What is PLA? What are the differences between PLA and ROM? [3]

c) Design a 4-bit binary counter by using J-K flip flops. [4]

d) Describe the effect of output carry for the following arithmetic operations. [5]

S_1	S_0	$C_{in} = 0$	$C_{out} = 1$
0	0	$F = A$	$F = A + 1$
0	1	$F = A + B$	$F = A + B + 1$
1	0	$F = A - B - 1$	$F = A - B$
1	1	$F = A - 1$	$F = A$

Consider all inputs contain n bits.

3.a) Determine the truth table, map simplification and PLA program table for the following two functions: [4]

$$F_1 = (B'C' + A'C' + A'B')'$$

$$F_2 = B'C' + A'C' + ABC$$

b) Prove that the multiplication of two n -digit numbers in any base r gives a product of no more than $2n$ digits in length. [4]

c) Design an arithmetic logic unit with two selection variables S_1 and S_0 , that generates the following arithmetic and logic operations. [6]

S_1	S_0	$C_{in} = 0$	$C_{in} = 1$	$C_{in} = \times$ (don't care)
0	0	$F = A + B$	$F = A + B + 1$	$F = A + B$ (OR)
0	1	$F = A$	$F = A + 1$	$F = A \oplus B$ (XOR)
1	0	$F = B'$	$F = B' + 1$	$F = AB$ (AND)
1	1	$F = A + B'$	$F = A + B' + 1$	$F = A'$ (Complement A)

4.a) Write a program for SAP-1 to solve the given arithmetic problem and then translate the program into SAP-1 machine language. [4]

$$16 + 20 + 24 - 32$$

The numbers are in decimal form.

b) Describe the architecture of SAP-2. [5]

c) Draw the OUT and SUB routines of SAP-1 and also draw their fetch and execution timing diagram. [5]

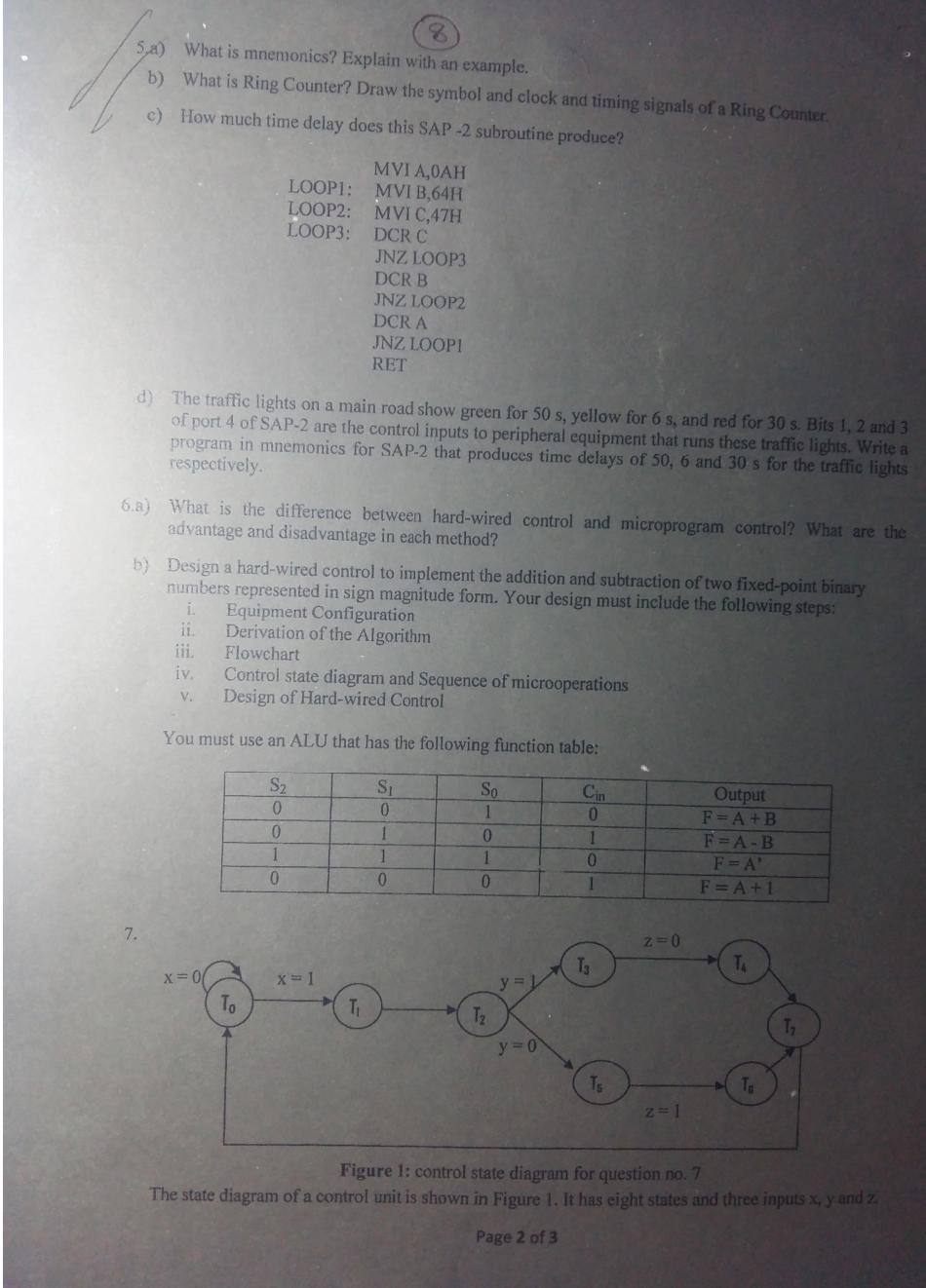


Figure 1: control state diagram for question no. 7

The state diagram of a control unit is shown in Figure 1. It has eight states and three inputs x , y and z .

(9)

- a) Design the control using eight D flip-flops.
 b) Design the control using three J-K flip-flops and a 3×8 decoder.
 c) Design the control using a PLA.

[4]

[5]

[5]

(10)

Date: 13/10/2015

Ahsanullah University of Science and Technology

Department of Computer Science and Engineering
 3rd Year, 1st Semester, Final Examination (Spring 2015)

Course No: CSE3109 Course Title: Digital System Design

Time: 3 Hours

Full Marks: 70

[Directions: There are 7(seven) questions. Answer any 5(five). Marks are shown at the end of each part of question.]

✓ 1

- a) Draw and describe SAP-1 architecture. 4

- b) Design a sequence detector that detects either "1011" or "00" sequence from a continuous bit stream. Non overlapping
 i. Draw the state transition diagram
 ii. Draw the excitation table. 5

✓ 2

- a) Design a 4 bit gray code down counter. (draw the excitation table only) 5

- b) Derive the output of a 4 bit booth multiplier (show every step clearly). Given, X = 0110, Y = 1010. 5

✓ 3

- c) Describe different methods of implementing control circuit. 4

✓ 3

- a) Design a 1-bit ALU using 1-bit full adder. Derive the equations only. 9

S_2	S_1	S_0	C_{in}	Output
0	0	0	0	A (Transfer A)
0	0	0	1	A+1 (Increment A)
0	0	1	0	A+B (Add A and B)
0	0	1	1	A+B+1 (Add A and B with carry)
0	1	0	0	A-B-1 (Subtract B from A with borrow)
0	1	0	1	A-B (Subtract B from A)
0	1	1	0	A-1 (Decrement A)
0	1	1	1	A (Transfer A)
1	0	0	x	A B (A or B)
1	0	1	x	A \oplus B (A Xor B)
1	1	0	x	AB (A and B)
1	1	1	x	A' (Negation of A)

- (11)**
- b) Design a 4 bit universal shift register that performs the following operations depending on control signals (u & v)
- | u | v | Operation |
|-----|-----|-------------|
| 0 | 0 | Left Shift |
| 0 | 1 | Hold |
| 1 | 0 | Right Shift |
| 1 | 1 | Load |
- The following code segment computes GCD of 2 given inputs (U and V)
- ```

GCD(U,V){
 rem = -1;
 while(rem != 0){
 rem = -1;
 while(U > V){
 U = U - V;
 }
 rem = U;
 U = V;
 V = rem;
 }
 Output = U;
}

```
- 

- i. Draw the flow chart for the above-mentioned program.  
ii. Identify the states and draw the state transition diagram.

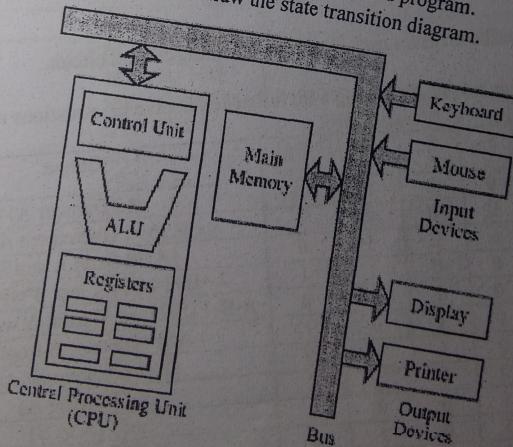


Fig : 1  
The computing system shown in Fig: 1 is claimed to be "Harvard Architecture". Do you agree with the claim? Justify your position.

- (12)**
- ✓ 5 a) Design a 4 bit ALU using 4 bit full adder.

| $S_1$ | $S_0$ | $C_{in}$ | Output                              |
|-------|-------|----------|-------------------------------------|
| 0     | 0     | X        | $A \oplus B$ ( $A \text{ Xor } B$ ) |
| 0     | 1     | X        | $A B$ ( $A \text{ or } B$ )         |
| 1     | 0     | 0        | $A+1$ (Increment $A$ )              |
| 1     | 0     | 1        | $A+B$ (Add $A$ and $B$ )            |
| 1     | 1     | 0        | $A-B$ (Subtract $B$ from $A$ )      |
| 1     | 1     | 1        | $A-1$ (Decrement $A$ )              |

- i. Derive equations for  $X$ ,  $Y$  and  $Z$   
ii. Draw the block diagram. 6  
3
- b) Write short note on Overflow flag. Determine the overflow flag for the ALU of question 5.a if  $S_1 S_0 C_{in} = 101$ ;  $A = 0110$  and  $B = 0011$  5
- ~~a)~~ a) Discuss the basic differences of SAP-1 and SAP-2 computers. 3
- ~~b)~~ b) In SAP-2 computer, there is no SP(Stack Pointer) register. How does the CALL instruction is implemented in SAP-2? Is there any limitation of CALL instruction in SAP-2. Briefly Discuss. 5
- c) Calculate the run time of the following SAP-2 subroutine if the computer has a clock of 1.6MHz frequency. 6

| Code    | T States needed for Instruction        |
|---------|----------------------------------------|
| L1:     | MVI A, 07H<br>MVI B, 10H<br>MVI C, 20H |
| L2:     | DCR B<br>DCR C<br>JNZ L2               |
| L3:     | DCR C<br>JZ L3Exit<br>JMP L3           |
| L3Exit: | DCR A<br>JNZ L1                        |
| Exit:   | NOP<br>RET                             |

(7)

(13)

a) Consider the following code segment

```

Res = 0;
for(i = 0; i <= m; i++) {
 Res1 = 0;
 for(j = 1; j <= n; j++) {
 Res1 = Res1 + Res;
 }
 Res = Res1;
}

```

- Draw the flow chart
- Identify the states and draw state transition diagram.
- Draw block diagram.

3  
4  
3

- b) A RAM image of SAP-1 Computer is given below (Address and Data are given in hexadecimal).

4

| Address | Data |
|---------|------|
| 0H      | 0AH  |
| 1H      | 1BH  |
| 2H      | 2CH  |
| 3H      | E4H  |
| 4H      | 0DH  |
| 5H      | 1EH  |
| 6H      | F7H  |
| 7H      | 0FH  |
| 8H      | E0H  |
| 9H      | F0H  |
| AH      | 67H  |
| BH      | 32H  |
| CH      | 46H  |
| DH      | 78H  |
| EH      | A4H  |
| FH      | B8H  |

67H

Calculate the value of different registers when the machine halts. Assume that, the machine starts from address 0.

Date: 27/4/15

(14)

Ahsanullah University of Science and Technology  
 Department of Computer Science and Engineering  
 Final Examination Fall 2014

3rd Year 1st Semester

Course No.: CSE3109 Course Title: Digital System Design

Full Marks: 70

Time: 3 Hours

[There are 7(seven) questions. Answer any 5(five). Marks are shown in the right margin.]

- a) Design a 4 bit ALU that performs the following operations. Optimize the ALU as much as possible. You can use 4 bit full adder, any number of logic gates. Derive the optimal equations only (9)

| S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | C <sub>in</sub> | Output  |
|----------------|----------------|----------------|-----------------|---------|
| 0              | 0              | 0              | x               | A or B  |
| 0              | 0              | 1              | x               | A xor B |
| 0              | 1              | 0              | x               | A and B |
| 0              | 1              | 1              | x               | A'      |
| 1              | 0              | 0              | 0               | A+1     |
| 1              | 0              | 0              | 1               | A-      |
| 1              | 0              | 1              | 0               | A+B+1   |
| 1              | 0              | 1              | 1               | A+B     |
| 1              | 1              | 0              | 0               | A-B     |
| 1              | 1              | 0              | 1               | A-B-1   |
| 1              | 1              | 1              | 0               | A       |
| 1              | 1              | 1              | 1               | A-1     |

Figure: 1

- b) Write short note on "Carry Flag". What will be the carry flag in above mentioned ALU, if  $A = 0100, B = 0101$ , and  $S_2S_1S_0C_{in} = 1110$ . (3+2)

- ✓ 2 You are asked to design a counter that counts the following sequence with every clock pulse.

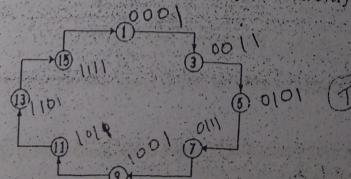


Figure: 2

- a) Design the excitation table. (7)

- b) Draw the block diagram and circuit diagram. (3+4)

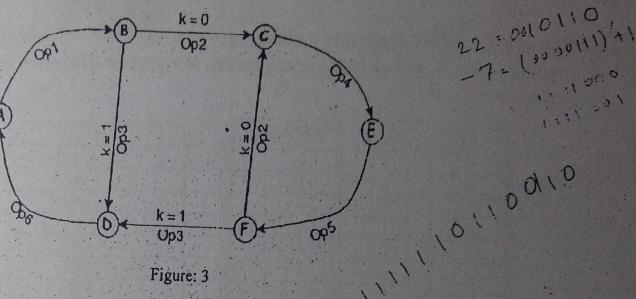
- ✓ 3 a) Design a digital system that detects either "011" or "101" sequence from a continuous data stream with overlapping sequence. Draw the state transition diagram only. (Overlapping sequence means in case of 01101, the system will detect first 011 and then 101) (9)

- b) Write short note on "Overflow flag". What will be the carry flag in ALU in Figure: 1(a), if  $A = 0100, B = 0101$ , and  $S_2S_1S_0C_{in} = 1010$ . (3+2)

01101  
011  
101  
1010

15. a. Show the detailed steps of multiplying “ -7 ” and “22” in a 7 bit number system using booth’s multiplication algorithm. (7)
- b. Draw the block diagram of a booth’s multiplier circuit. Explain your circuit. (2+5)

5. Suppose your company is introducing automation to your factory. As a chief engineer, you have to design the controller of your factory machine. You found state transition diagram of your factory is as in the following figure. (14)



Operations and corresponding control signals are as follows

| Operation | Control Signals |   |   |   |   |
|-----------|-----------------|---|---|---|---|
|           | P               | Q | R | S | T |
| Op1       | 0               | 0 | 0 | 0 | 1 |
| Op2       | 0               | 1 | 0 | 1 | 0 |
| Op3       | 1               | 1 | 1 | 0 | 1 |
| Op4       | 1               | 0 | 1 | 1 | 0 |
| Op5       | 1               | 1 | 1 | 1 | 1 |
| Op6       | 1               | 1 | 0 | 1 | 0 |

Figure: 4

Here ‘k’ is an external input. Design a control unit for this machine using “One Flip-Flop Per State” method.

6. Design a multiplication circuit, which multiplies 2(two) positive numbers each of which is k bit in length. Use normal arithmetic multiplication algorithm. (3)
- a. Draw the flow chart. (4)
- b. Draw that state transition diagram. (4)
- c. Design a control unit using “One Flip-Flop Per State” method. (7)

0111  
1000  
1001

16. Carefully follow the architecture depicted below.

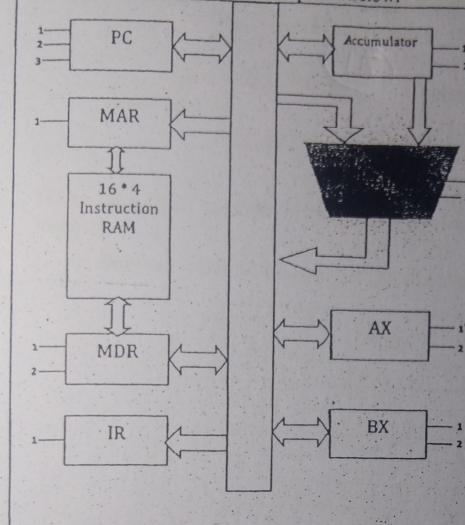


Figure: 5

Using the above mentioned architecture, decompose the following instructions into (6+8) microinstruction sequences. Explain the decomposition.

| Instruction | Functionality                                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| MOV AX, BX  | Moves the data of BX register to AX register. Assume the whole instruction is one word instruction and there is no operand of this instruction |
| JE addr     | Jumps if equal.<br>Show both the successful and unsuccessful condition.                                                                        |

Date: 25/08/2013

Ahsanullah University of Science and Technology  
Department of Computer Science and Engineering

Final Examination Spring 2013

3<sup>rd</sup> Year

1<sup>st</sup> Semester

Course No.: CSE 309

Course Title: Digital System Design

Time: 3 Hours

Full Marks: 70

[Use separate answer scripts for Part A and Part B.]

### Part - A

[There are 4 (four) questions in this section. Answer any 3(three). Marks are shown in the right margin.]

1. a) Design an Arithmetic and Logic Unit (ALU) which has the following functions:

10

| Selection      |                |                |                 | Output           | Function                |
|----------------|----------------|----------------|-----------------|------------------|-------------------------|
| S <sub>1</sub> | S <sub>1</sub> | S <sub>0</sub> | C <sub>in</sub> |                  |                         |
| 0              | 0              | 0              | 0               | F = A - 1        | Decrement A             |
| 0              | 0              | 0              | 1               | F = A            | Transfer A              |
| 0              | 0              | 1              | 0               | F = A + B        | Addition                |
| 0              | 0              | 1              | 1               | F = A + B + 1    | Add with carry          |
| 0              | 1              | 0              | 0               | F = A - B - 1    | Subtraction with borrow |
| 0              | 1              | 0              | 1               | F = A - B        | Subtraction             |
| 0              | 1              | 1              | 0               | F = A'           | Transfer A              |
| 0              | 1              | 1              | 1               | F = A + J        | Increment A             |
| 1              | 0              | 0              | X               | F = A'           | Complement of A         |
| 1              | 0              | 1              | X               | F = A xor B      | XOR                     |
| 1              | 1              | 0              | X               | F = A $\wedge$ B | AND                     |
| 1              | 1              | 1              | X               | F = A $\vee$ B   | OR                      |

- b) What will be the values of the status registers (Zero, Sign, Carry and Overflow) of a 6-bit ALU if the two inputs are A = 111101, B = 111110, C<sub>in</sub> = 0, and the addition operation is performed?

1 2/3

- ✓ 2. a) How can you design a 3-bit magnitude comparator? Explain with figure.
- b) Implement the following function using a 8X1 MUX and a single NOT gate:  
F(A, B, C, D) = L(0, 5, 6, 9, 15)
- c) How can microprogramming be used in SAP-1 computer? Explain briefly. What is the benefit of using it in SAP-1?
3. a) Distinguish between machine cycle and instruction cycle. Give examples.
- b) How can you optimize SAP-1 macro-instructions to remove NOP operations?
- c) Explain the fetch and execution cycles of the LDA instruction in SAP-1 computer architecture with necessary diagrams.
4. a) How much time delay does the following program produce? Consider that the MVI instruction requires seven T states, DCR instruction requires four T states, JNZ requires 10/7 T states and RET requires 10 T states.

5

3

3 2/3

2

3

6 2/3

4 2/3

MVI A, 0CH  
Loop1: MVI B, 64H  
Loop2: MVI C, 40H

Loop3: DCR C  
JNZ Loop3  
DCR B  
JNZ Loop2  
DCR A  
JNZ Loop1  
RET

- b) Write down a program to compute the following sum using SAP-2 instructions:  
Sum = 1 + 2 + 3 + ... + 99

3 + 4

Write down the corresponding machine code of your program. The starting address of the code segment is 2000H. [Assume opcodes of all the instructions used in your program]

### Part - B

[There are 4 (four) questions in this section. Answer any 3(three). Marks are shown in the right margin.]

5. Design a digital system that multiplies two fixed point numbers represented in 2's complemented form (Assume each number to be k-bit).
- Draw flowchart of the system.
  - Draw the state diagram of the system and show the control outputs of each control states.
  - Draw block diagram of data processor part.
  - Design the control using one flip-flop (J-K Flip Flop) per state method.

6. Using J-K flip-flop, design one typical stage of a register that performs the following micro-operation

1 1 2/3

P1 : A  $\leftarrow$  A XOR B

p2: A  $\leftarrow$   $\overline{A} - 1$

p3: A  $\leftarrow$  A +  $\overline{B}$

7. Write short notes on each of the following:

- Micro-programming method
- One flip flop per state method
- USB

1 1 2/3

8. Design a digital system that counts the number of one (1) stored in a register. (Assume the number is n-bit) [For example, if the number is 101011, then the output will be 4]

1 1 2/3

- Draw flowchart of the system.
- Draw the state diagram of the system and show the control outputs of each control states.
- Draw block diagram of data processor part.
- Design the control using micro-programming control.

(19)

Ahsanullah University of Science & Technology  
 Department of Computer Science and Engineering  
 3<sup>rd</sup> Year, 1<sup>st</sup> Semester, Final Examination (Fall 2012)

Course No: CSE 309  
 Full Marks: 70

Course Title: Digital System Design  
 Time: 3 Hours

Directions: There are Seven (7) Questions. Answer any Five (5).  
 [Marks allotted are indicated in the right margin.]

- a) Write down the conditions of setting-resetting the C and V flags. [2]
  - b) For the following relations find out the state of the status flags with suitable examples:
    - i. A < B, for unsigned numbers.
    - ii. A > B, for signed numbers.
  - c) Write down a VHDL code to construct a 2X1 MUX.
  - d) Design an adder/subtractor circuit with one selection variable s and two inputs A and B. When s=0 the circuit performs A+B. When s=1 the circuit performs A-B by taking the 2's complement of B.
2. a) Give examples of best case, worst case and average case of multiplier in case of Booth's multiplication. [3]
- b) Multiply 30 by -2 using Modified Booth's Algorithm. 85 [4]
- c) Count the number of 0's in a register R8 and store the result in R9. Draw a flowchart, show microinstructions and derive the ROM content for this problem. Start from ROM address 000000. Use figures: 1,2,7,8. [7]
3. a) Differentiate between hard-wired control and microprogram control. [2]
- b) Write down the advantages and disadvantages of One Flip-Flop per state method. [2]
- c) Design the control unit of a digital circuit that will perform the addition and subtraction of two fixed point binary numbers represented in sign-magnitude form. Use 'One flip-flop per state' method [Flow-chart, Control block-diagram, sequence of register transfers, input and output functions are required]. [10]

$$A < B \quad C = 0 \quad Z = 0$$

$$\begin{array}{r} 1 \\ 1 \\ 1 \\ 0 \end{array}$$

[4]

[3]

[7]

[10]

- (20)
- a) Using figure:1,2,8 find Control Words for the following operations: [2]
- i. CMP R1,R2
  - ii. R2  $\leftarrow$  CRC R2
- b) Find the memory representation of the following floating point number with relevant steps: (13.385)<sub>10</sub> [5]
- Assume that the starting address of the memory location is 5000H.
- c) Design the control unit of a binary multiplier that multiplies 2 fixed point binary numbers in sign-magnitude representation. Draw the flowchart and find the excitation-table and simplified expressions for each of the gate inputs for the control unit using Sequence Register and Decoder method with two T Flip flops for G2 and G1. [7]
- d) Using JK Flip-flop design one typical stage of an accumulator to perform the following operations: [9]
  - i. A  $\leftarrow$  A+B, control variable P<sub>1</sub>
  - ii. A  $\leftarrow$   $\bar{A}$ , control variable P<sub>2</sub>
  - iii. A  $\leftarrow$  A+1, control variable P<sub>9</sub>
- e) Write down the microinstructions for the execution cycle of LDA operation in SAP-1. [3]
- How can we reduce the wiring capacitance of SAP-2? [2]
- f) For the given table in figure:01 find out efficient simplified expressions for X and Y to perform only logic operations. [2]
- g) What are the differences between DRAM and SRAM? [2]
- h) How PUSH and POP instructions are executed in SAP-3? Write down the execution steps of these instructions. Suppose, BC = 5612H and SP = 2100H. What will happen after the execution of PUSH B instruction? [4+4]
7. a) State some significant differences between SAP-1 and SAP-2 architecture. [2]
- b) Write down three key features of SCSI bus. [3]
- c) Write down a SAP-3 program in mnemonic form that subtracts 700 from 900 and stores the answer in the H and L registers. [4]
- d) Explain the following instructions and give one example of each: [5]
  - i. XRA
  - ii. STA
  - iii. DAD
  - iv. CMA
  - v. ACI

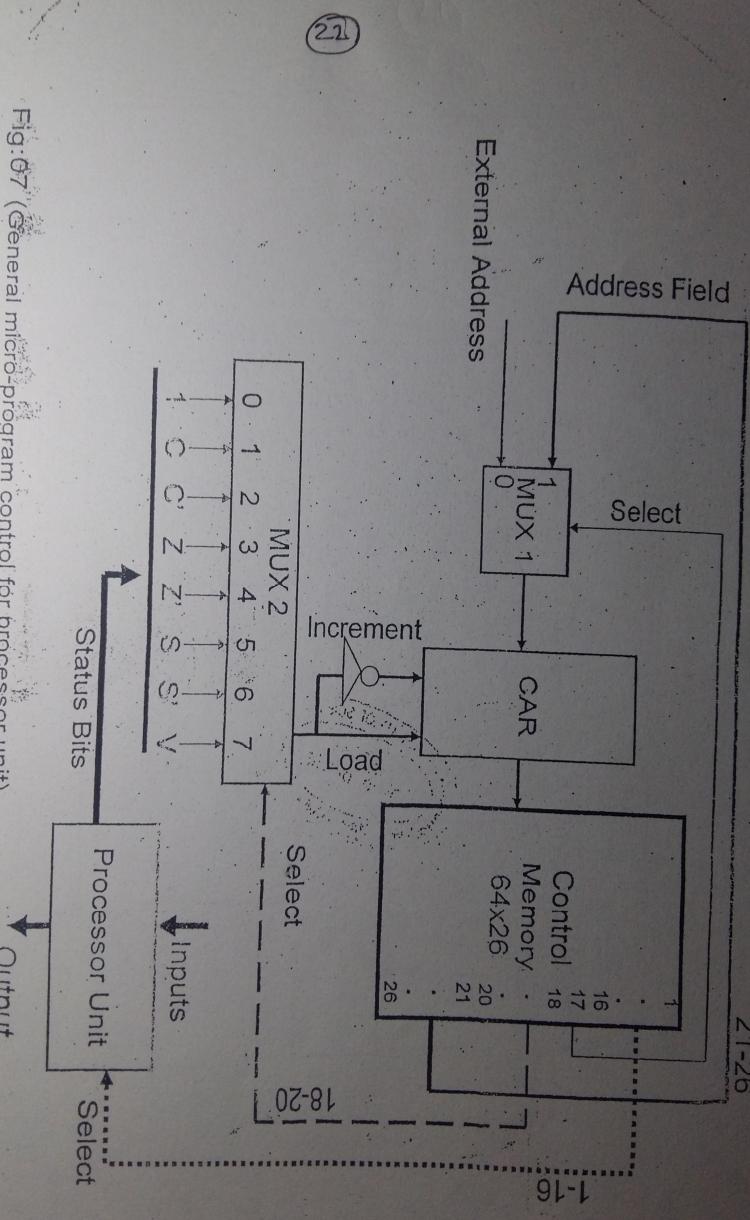


Fig. 67 (General micro-program control for processor unit)

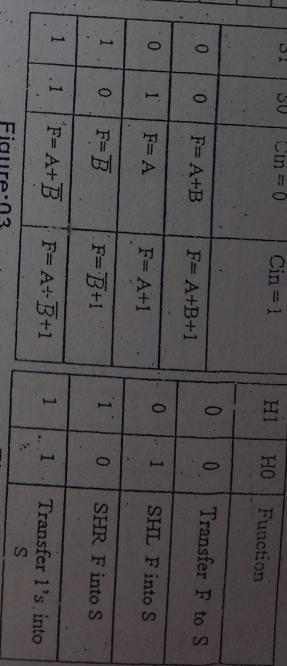
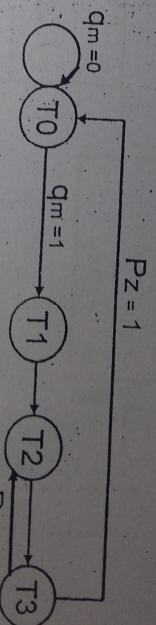


Figure:04

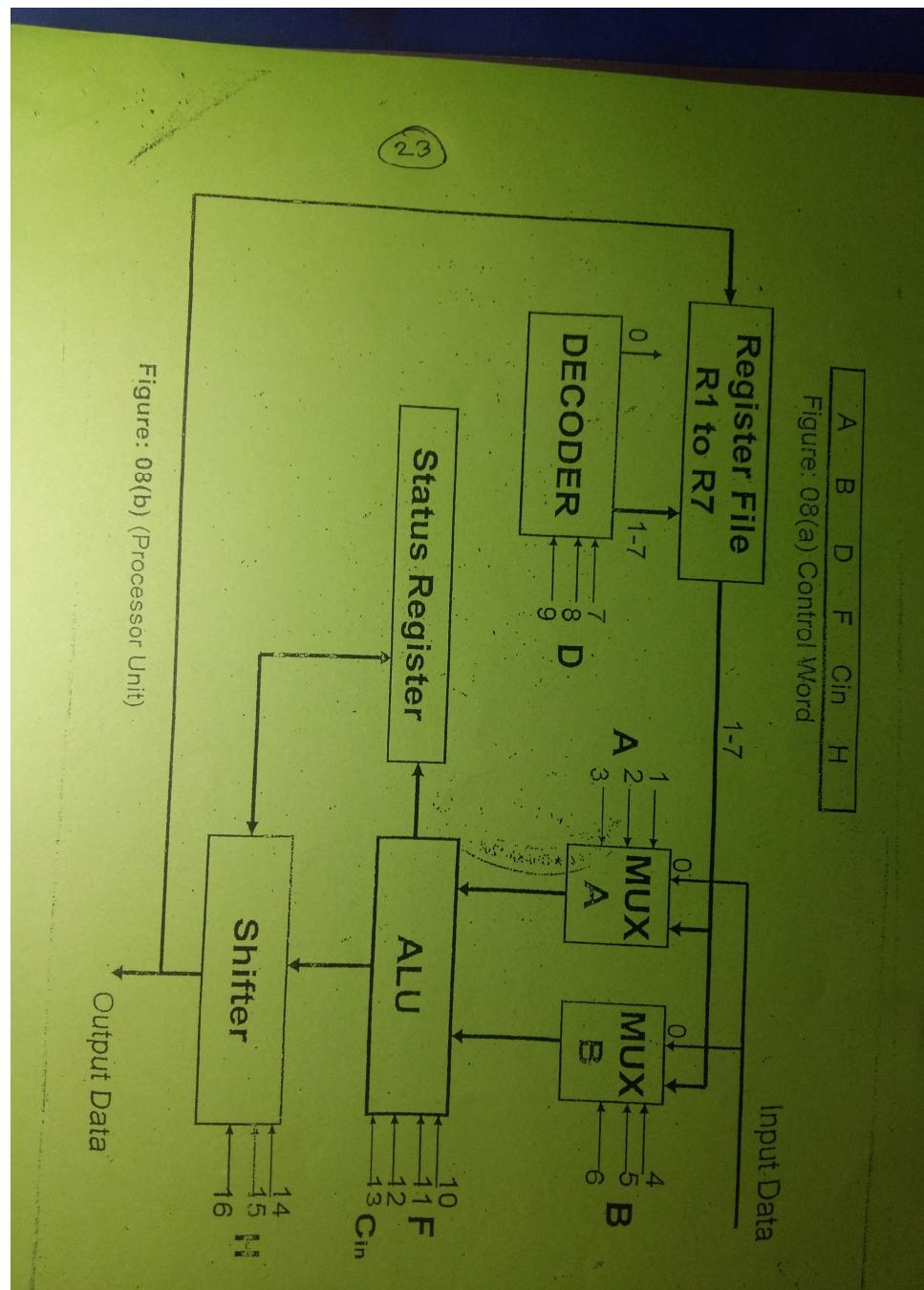


IRE:06

| H2 | H1 | H0 | Function          |
|----|----|----|-------------------|
| 0  | 0  | 0  | No Shift          |
| 0  | 0  | 1  | SFR, If = 0       |
| 0  | 1  | 0  | SHL, If = 0       |
| 1  | 0  | 0  | 0's to output bus |
| 1  | 0  | 1  | -----             |
| 1  | 1  | 0  | CRC               |
| 1  | 1  | 1  | CLC               |

Figure:01 (Table:ALU Operations)

Figure:02 (Table: Shifter Operations)



- (2.4)
- Part: B
- There are 7 (Seven) questions. Answer any 5 (Five) questions.  
Marks are indicated in the right margin.*
1. ✓ Power House is the first power generation company in Ghana established in 1990. Now discuss the type of profit that Power House is earning if the number of company has risen to 30 in 2012? 07
  2. ✓ a. Given  $Q_d = 20 - 0.5P_{\text{Desktop}} + 0.5P_{\text{Laptop}} - 0.2P_{\text{Rain}} + 0.0001Y$  where  $P_{\text{Desktop}} = 25000$ ,  $P_{\text{Laptop}} = 25000$ ,  $P_{\text{Rain}} = 4000$ ,  $Y = 100,000$  and  $Q_{\text{Desktop}} = 50000$ . Use formula of elasticity for appropriate deductions. 02
  - b. Suppose the economy has reached potential output and amount of export earning increases. Discuss the effects on economy. 05
  3. a. Given  $C = 2000 + 0.9Y_D$  where  $Y_D = Y - T$  and  $T = 300 + 0.2Y$ . Find MPC and MPS. 02
  - b. Discuss Long Run Envelope Curve with the help of at least three engineering plants sizes. 05
  4. ✓ a. Find the profit maximizing level of i) output, ii) prices and iii) profit for a monopolist given the demand functions:  
 $x = 50 - 0.5Px$   
 $y = 76 - Py$  and total cost function  
 $C = 3x^2 + 2xy + 2y^2 + 55$  03
  - b. i) Discuss components of Aggregate Demand.  
ii) Discuss two extreme cases of Aggregate Supply. 02
  5. ✓ a. Given the CPI in the year 2010 is 105. A hypothetical Budget survey shows that consumers spend 50% of their income on food, 30% on shelter and 20% on education. Now in 2011 both the prices of food and education rise by 10%. Calculate CPI and ROI for 2011. 03
  - b. Suppose the government of Bangladesh has fixed minimum wage for garment workers at taka 3000/. Discuss the impacts on economy of Bangladesh. 04
- Deduce a model of development using the following assumptions:  
(i) There is a dual economy i.e., the economy is characterized by a 07

(25)

traditional, over-populated rural subsistence sector furnished with zero MPL, and the high productivity modern urban industrial sector.

(ii) The subsistence sector does not make the use of 'Reproducible Capital', while the modern sector uses the produced means of capital.

(iii) The production in the advanced sector is higher than the production in traditional and backward sector.

(iv) The supply of labor is perfectly elastic. In other words, the supply of labor is greater than demand for labor.

7. a. Critically discuss the Law of Diminishing marginal Product. 05  
 b. Given the Labor Force, Employment and Unemployment from 02  
 1972 to 1997 (million person-years) comment on the Growth rate  
 of labor force and Unemployment. \*

| Year    | Labor Force | Employment |         |       | Unemployment Rate (%) | Unemployment Total |
|---------|-------------|------------|---------|-------|-----------------------|--------------------|
|         |             | Domestic   | Foreign | Total |                       |                    |
| 1972/73 | 21.38       | 13.99      | —       | 13.99 | 8.29                  | 38.78              |
| 1977/78 | 24.10       | 16.04      | 0.03    | 16.09 | 8.01                  | 33.24              |
| 1979/80 | 25.29       | 16.09      | 0.05    | 16.14 | 9.15                  | 36.18              |
| 1984/85 | 29.50       | 18.97      | 0.32    | 19.29 | 10.21                 | 34.61              |
| 1989/90 | 34.80       | 22.82      | 0.43    | 23.25 | 11.55                 | 33.19              |
| 1994/95 | 40.47       | 26.88      | 0.95    | 27.83 | 12.64                 | 31.23              |
| 1995/96 | 41.47       | 28.18      | 1.14    | 29.32 | 12.38                 | 29.69              |
| 1996/97 | 42.97       | 29.62      | 1.34    | 30.96 | 12.01                 | 27.95              |