CSE 3107: Microprocessor

Lecture # 6

Instruction Execution and Timing Diagram of 8085

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The Instruction Execution

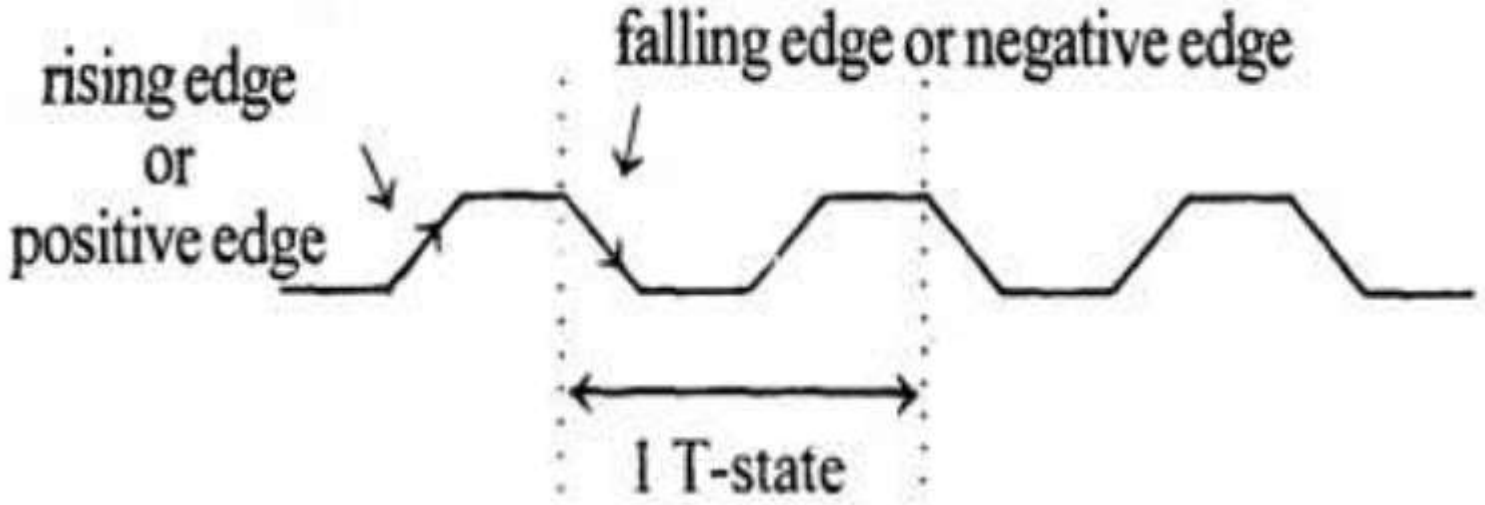
- Each instruction in 8085 microprocessor consists of two part- operation code (opcode) and operand. The opcode is a command such as ADD and the operand is an object to be operated on, such as a byte or the content of a register.
- **Instruction Cycle:** The time taken by the processor to complete the execution of an instruction. An instruction cycle consists of one to six machine cycles.
- **Machine Cycle:** The time required to complete one operation; accessing either the memory or I/O device. A machine cycle consists of three to six T-states.
- **T-State:** Time corresponding to one clock period. It is the basic unit to calculate execution of instructions or programs in a processor.

The Instruction Execution (Cont.)

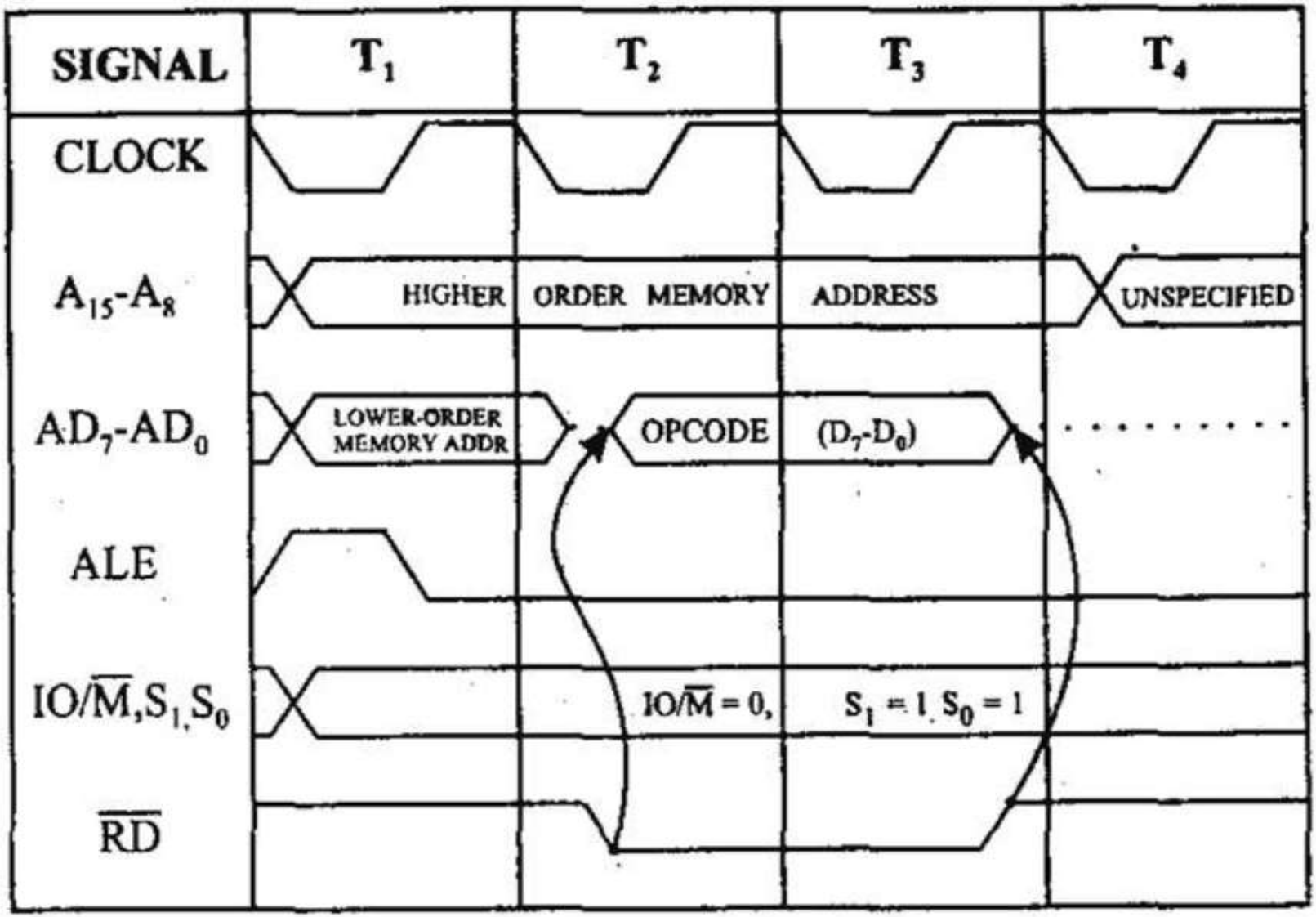
- To execute a program, 8085 performs various operations as:
  - Opcode fetch
  - Operand fetch
  - Memory read/write
  - I/O read/write

The Instruction Execution (Cont.)

Time period, T = 1/f ; where f = Internal clock frequency



Opcode Fetch Machine Cycle



Opcode Fetch Machine Cycle (Cont.)

- It is the first step in the execution of any instruction.
- The following points explain the various operations that take place and the signals that are changed during the execution of opcode fetch machine cycle:
- **T1 clock cycle**
  - The content of PC is placed in the address bus; AD0 - AD7 lines contains lower bit address and A8 – A15 contains higher bit address.
  - IO/ $\overline{M}$ signal is low indicating that a memory location is being accessed. S1 and S0 also changed to 1 to indicate opcode fetch operation.
  - ALE is high, indicates that multiplexed AD0 – AD7 act as lower order bus.

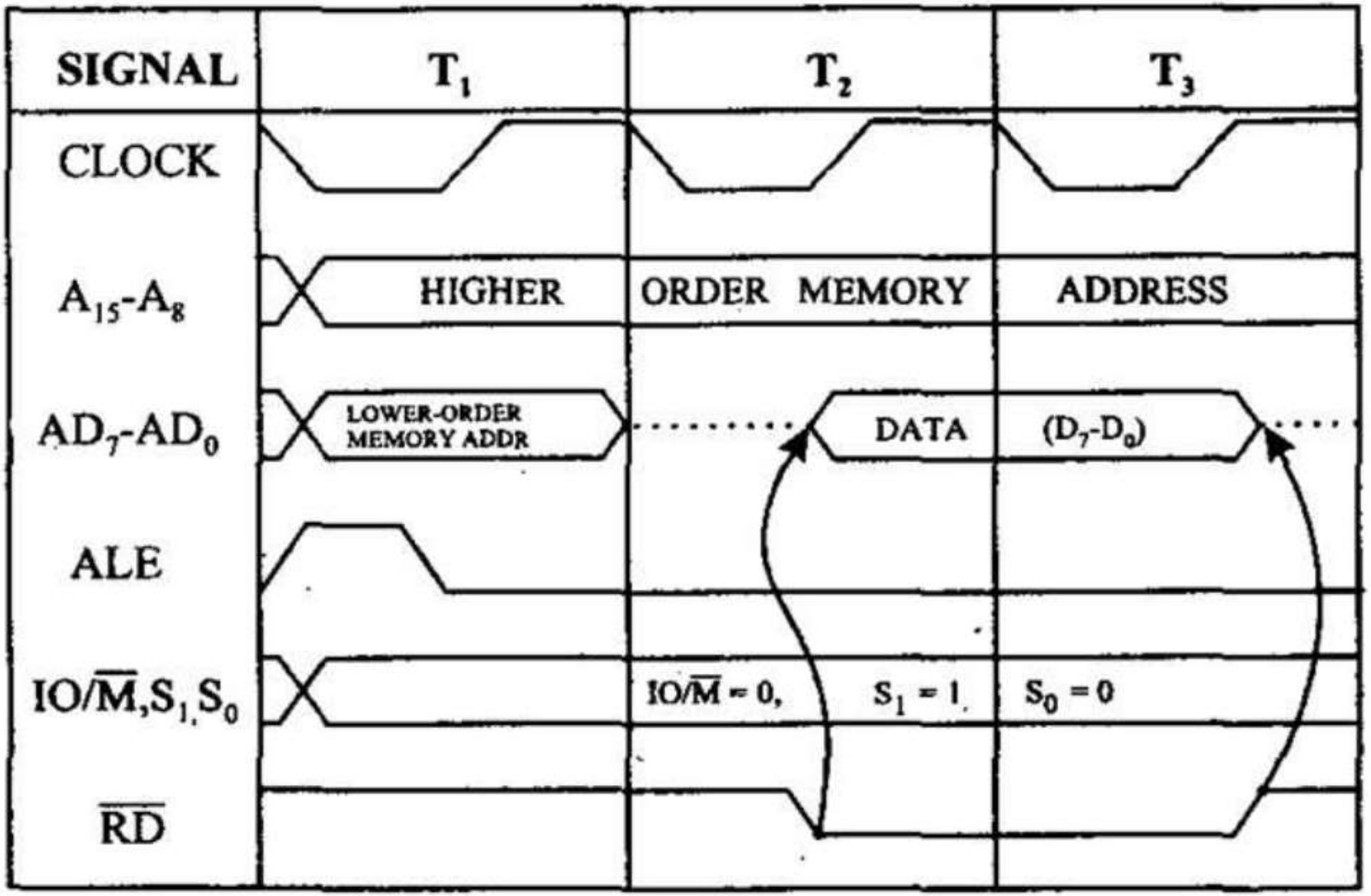
Opcode Fetch Machine Cycle (Cont.)

- **T2 clock cycle**
  - Multiplexed address bus is now changed to data bus.
  - The $\overline{RD}$ signal is made low by the processor. This signal makes the memory device load the data bus with the contents of the location addressed by the processor.
- **T3 clock cycle**
  - The opcode available on the data bus is read by the processor and moved to the instruction register.
  - The $\overline{RD}$ signal is deactivated by making it logic 1.
- **T4 clock cycle**
  - The processor decode the instruction in the instruction register and generate the necessary control signals to execute the instruction. Based on the instruction further operations such as fetching, writing into memory etc takes place.

Memory Read Machine Cycle

- The memory read cycle is executed by the processor to read a data byte from memory.
- The machine cycle is exactly same to opcode fetch except:
  - It has three T-states
  - The S0 signal is set to 0.

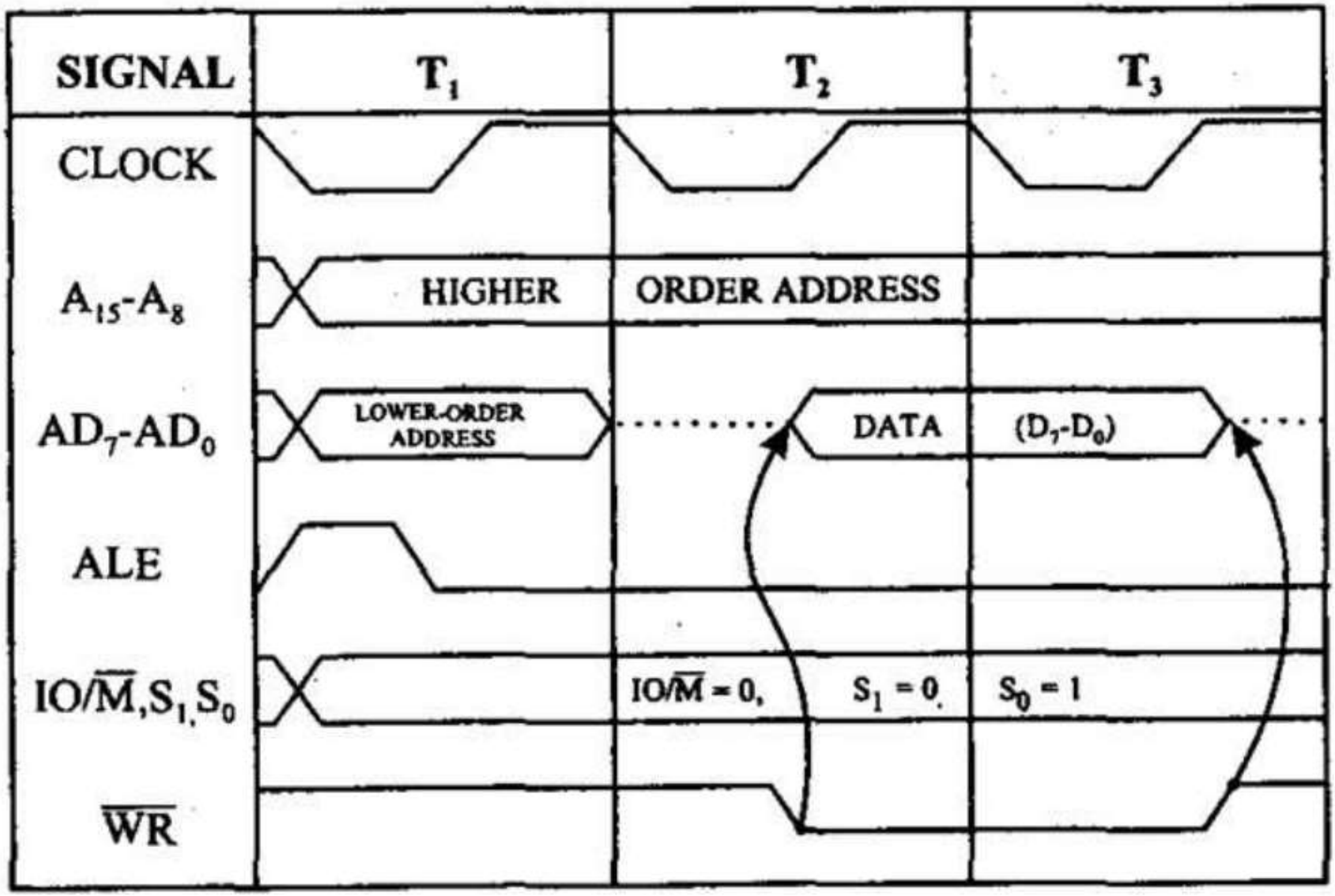
Memory Read Machine Cycle (Cont.)



Memory Write Machine Cycle

- The memory write cycle is executed by the processor to write a data byte in a memory location.
- The processor takes three T-states and $\overline{WR}$ signal is made low .

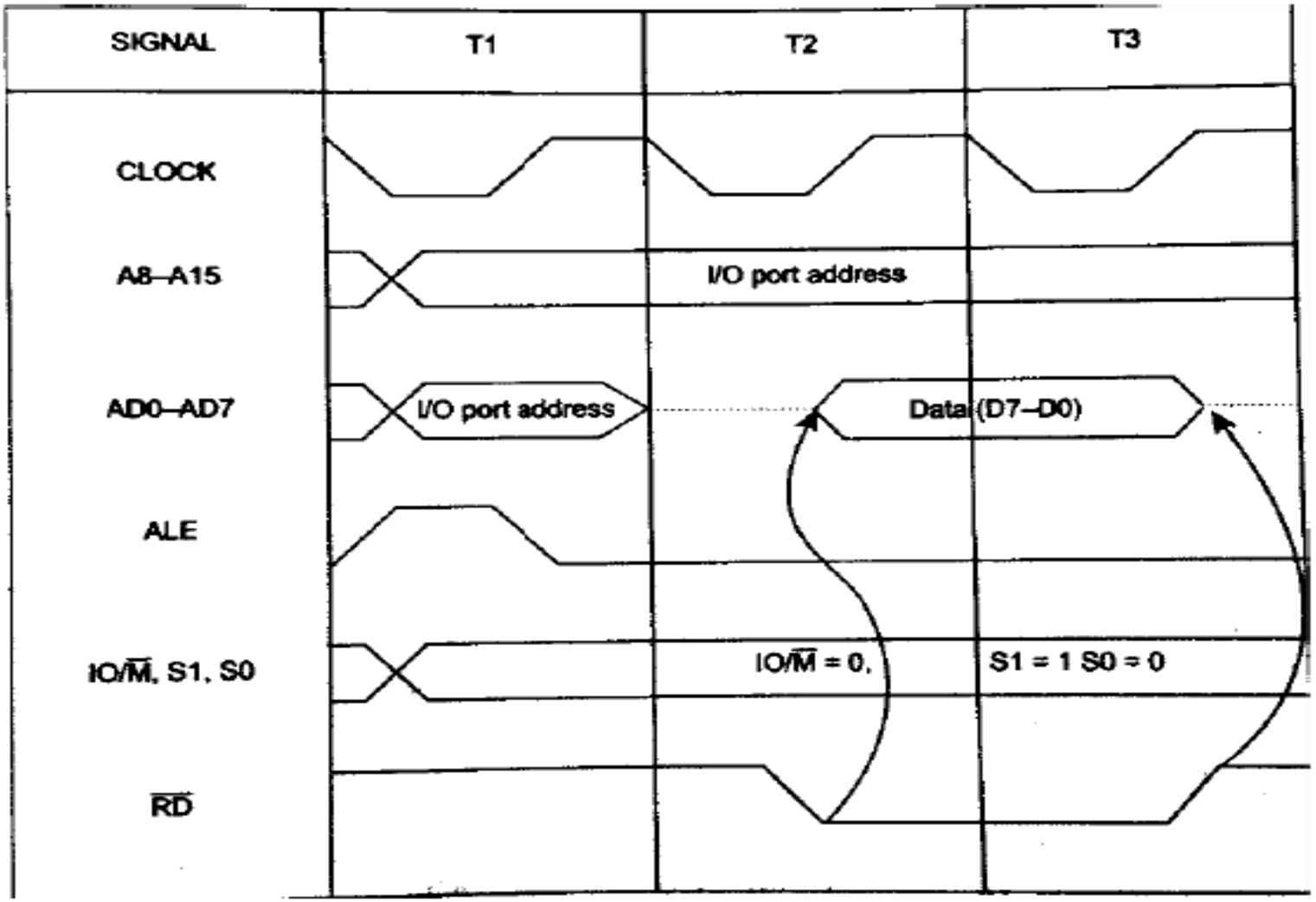
Memory Write Machine Cycle (Cont.)



I/O Read Machine Cycle

- The I/O read cycle is executed by the processor to read a data byte from I/O port or from peripheral, which is I/O mapped in the system.
- The 8-bit port address is placed both in the lower and higher order address bus.
- The processor takes three T-states to execute this machine cycle.

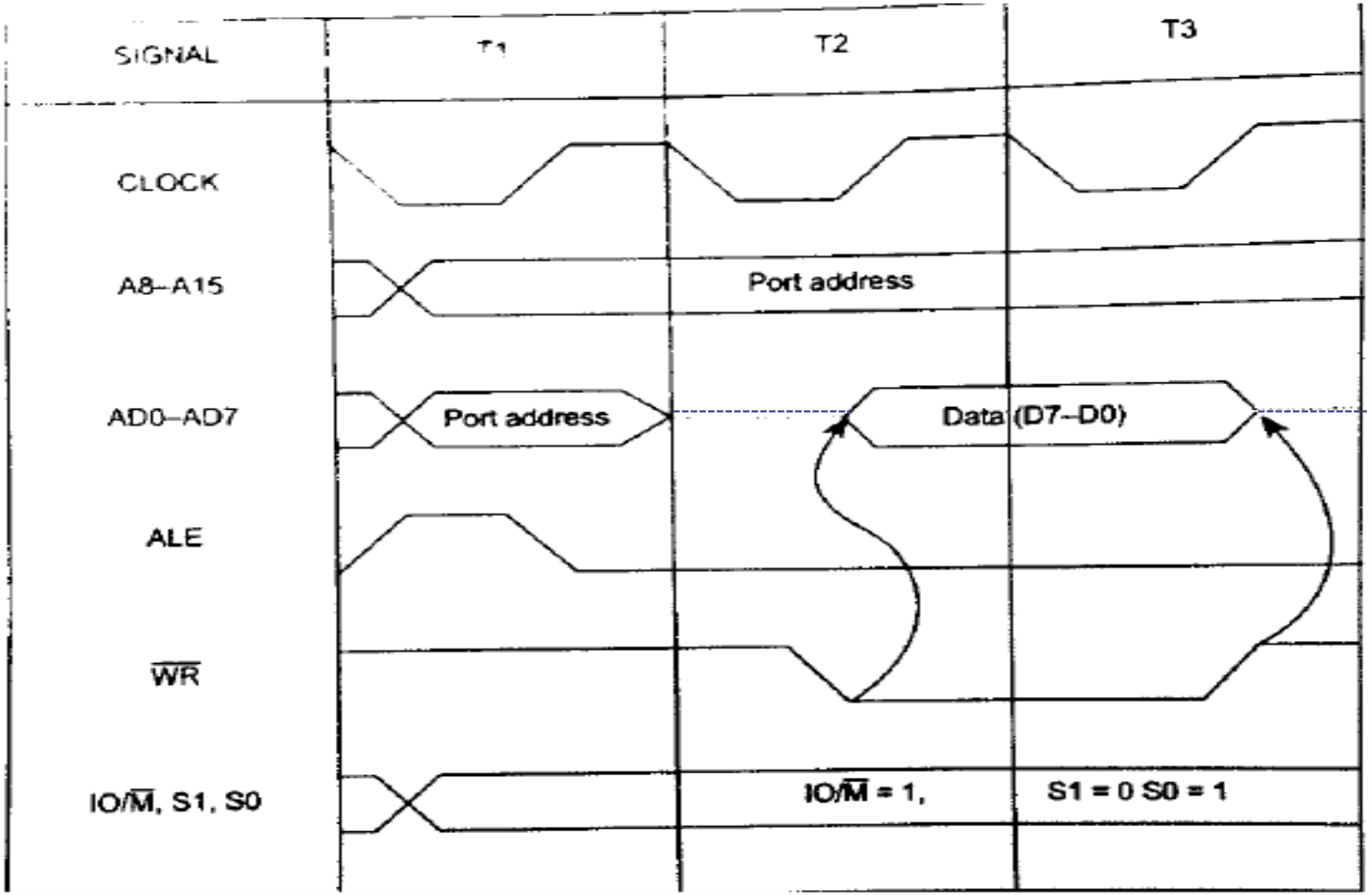
I/O Read Machine Cycle (Cont.)



I/O Write Machine Cycle

- The I/O write cycle is executed by the processor to write a data byte to I/O port or to a peripheral, which is I/O mapped in the system.
- The processor takes three T-states to execute this machine cycle.

I/O Write Machine Cycle (Cont.)



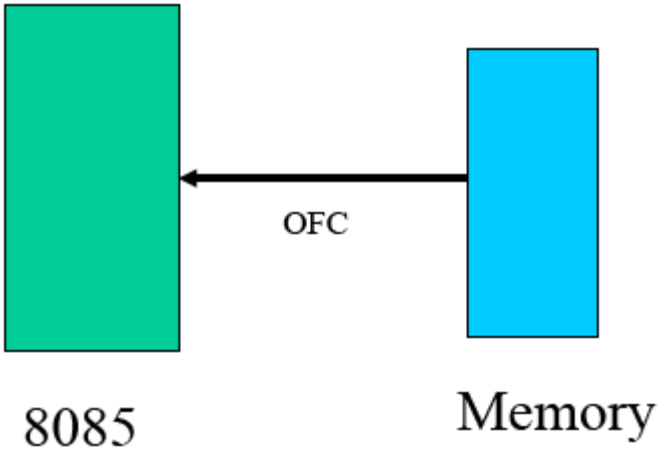
Example 1

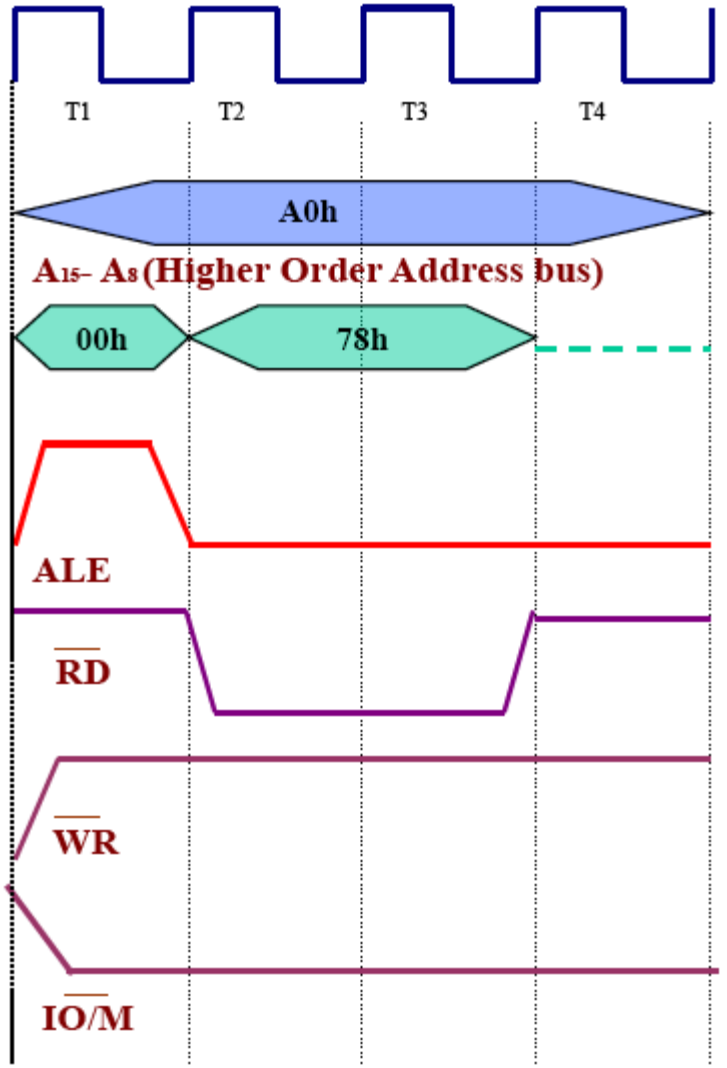
Instruction:

A000h MOV A,B

Corresponding Coding:

A000h 78





Op-code fetch Cycle

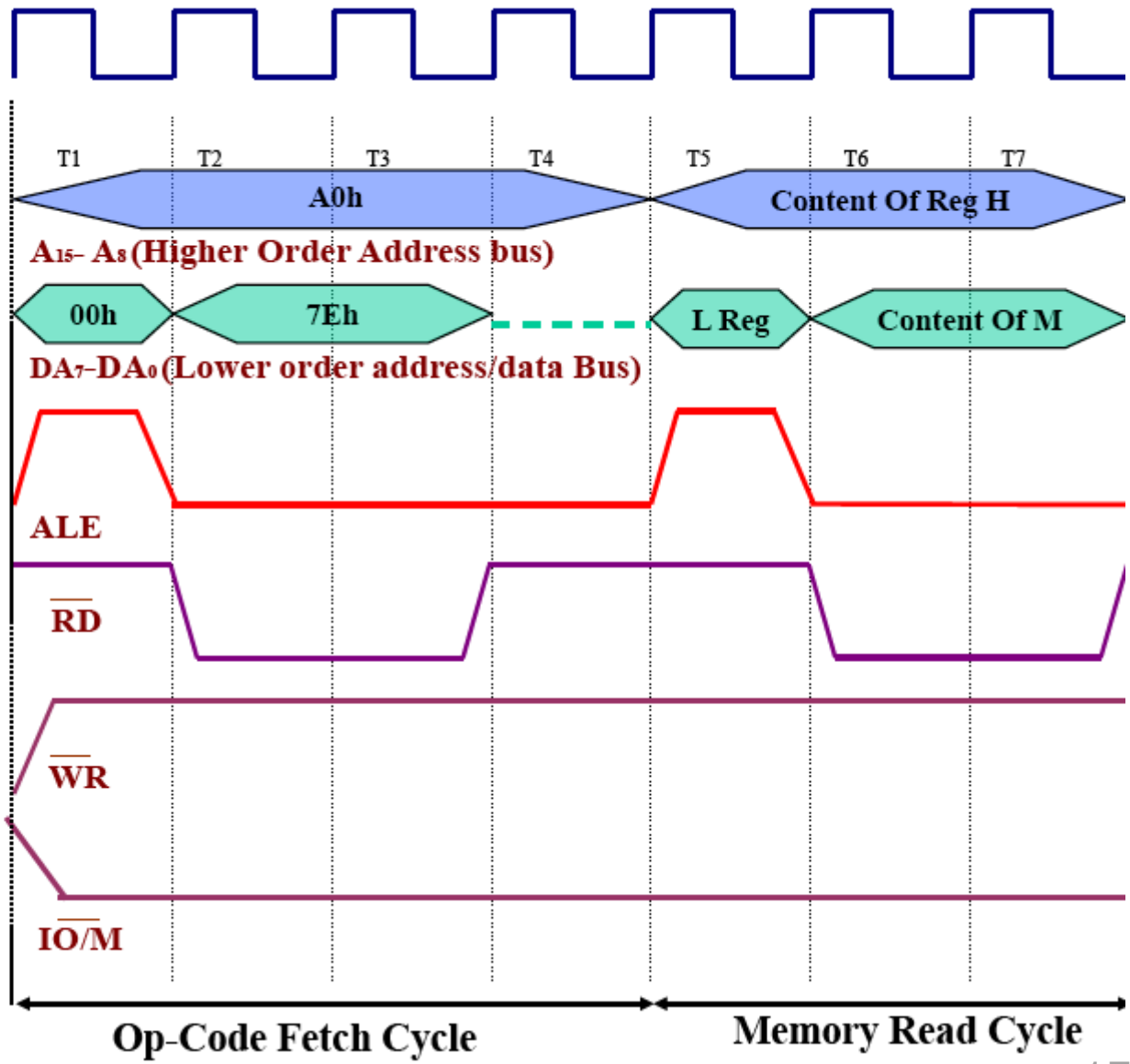
Example 2

Instruction:

A000h MOV A,M

Corresponding Coding:

A000h 7E



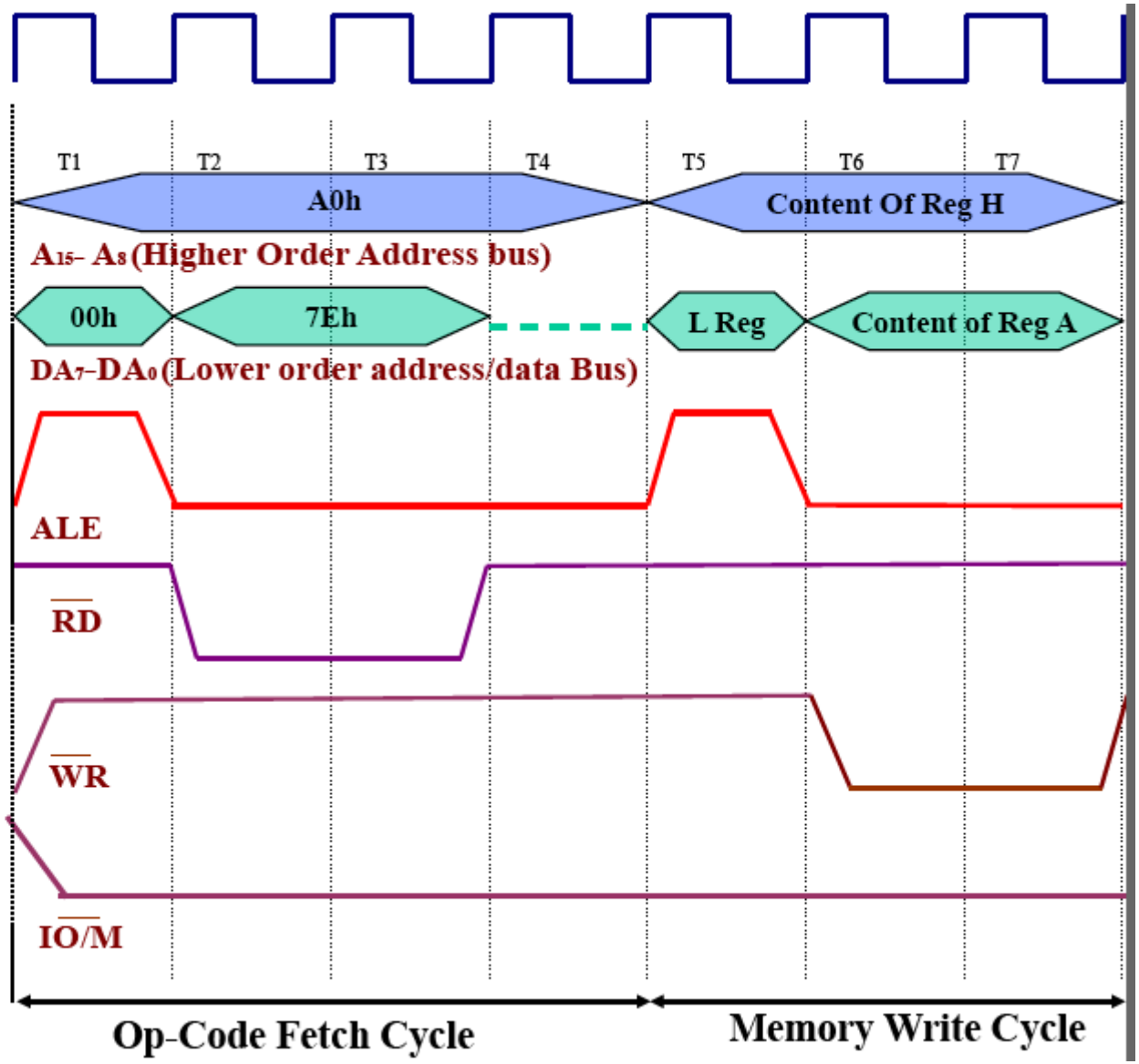
Example 3

Instruction:

A000h MOV M,A

Corresponding Coding:

A000h 77



Example 4

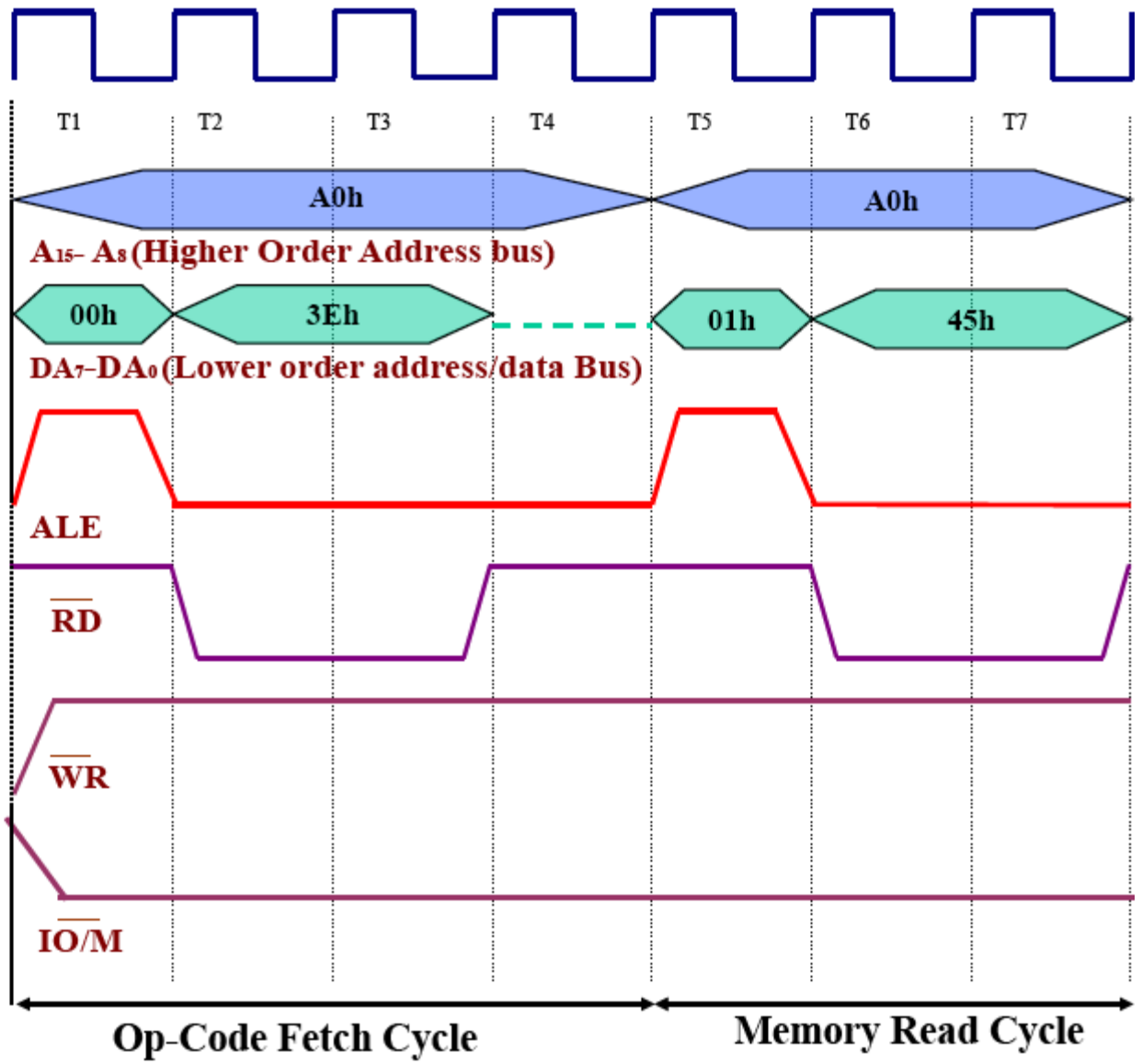
Instruction:

A000h MVI A,45h

Corresponding Coding:

A000h 3E

A001h 45



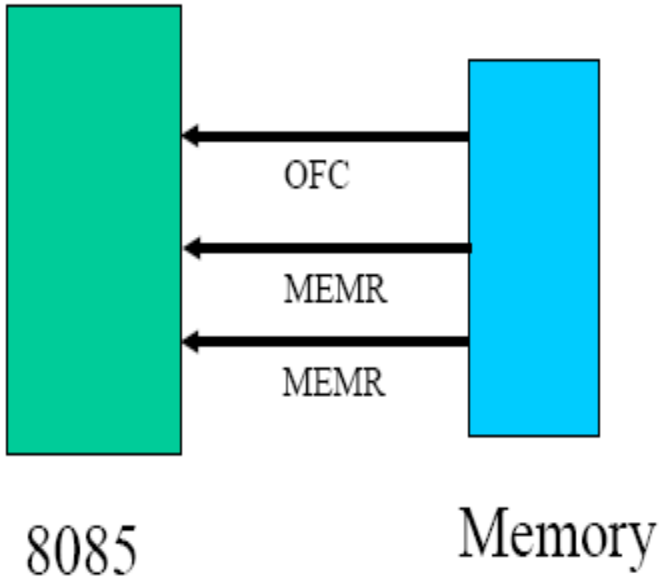
Example 5

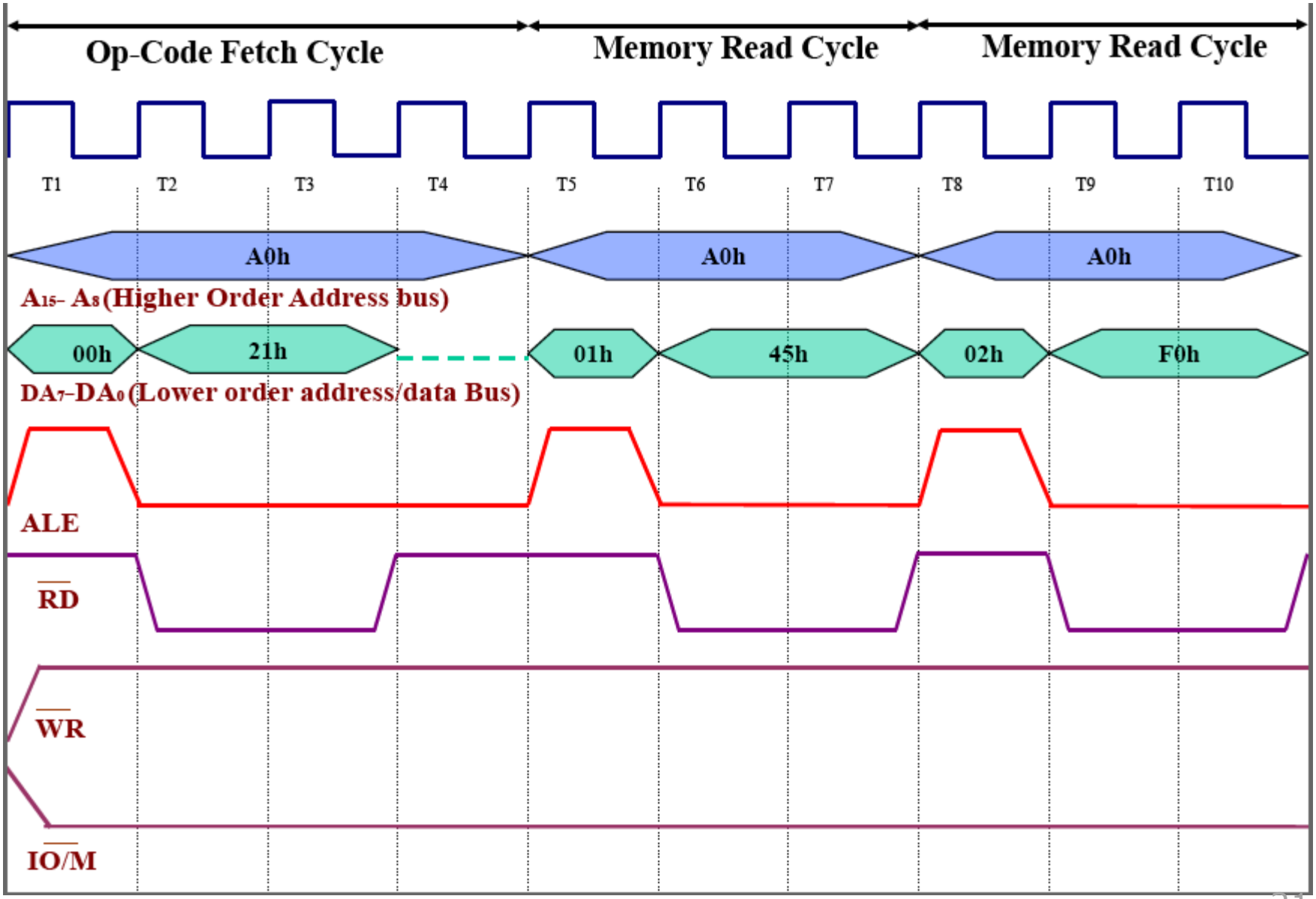
Instruction:

A000h	LXI H,FO45h

Corresponding Coding:

A000h	21
A001h	45
A002h	F0



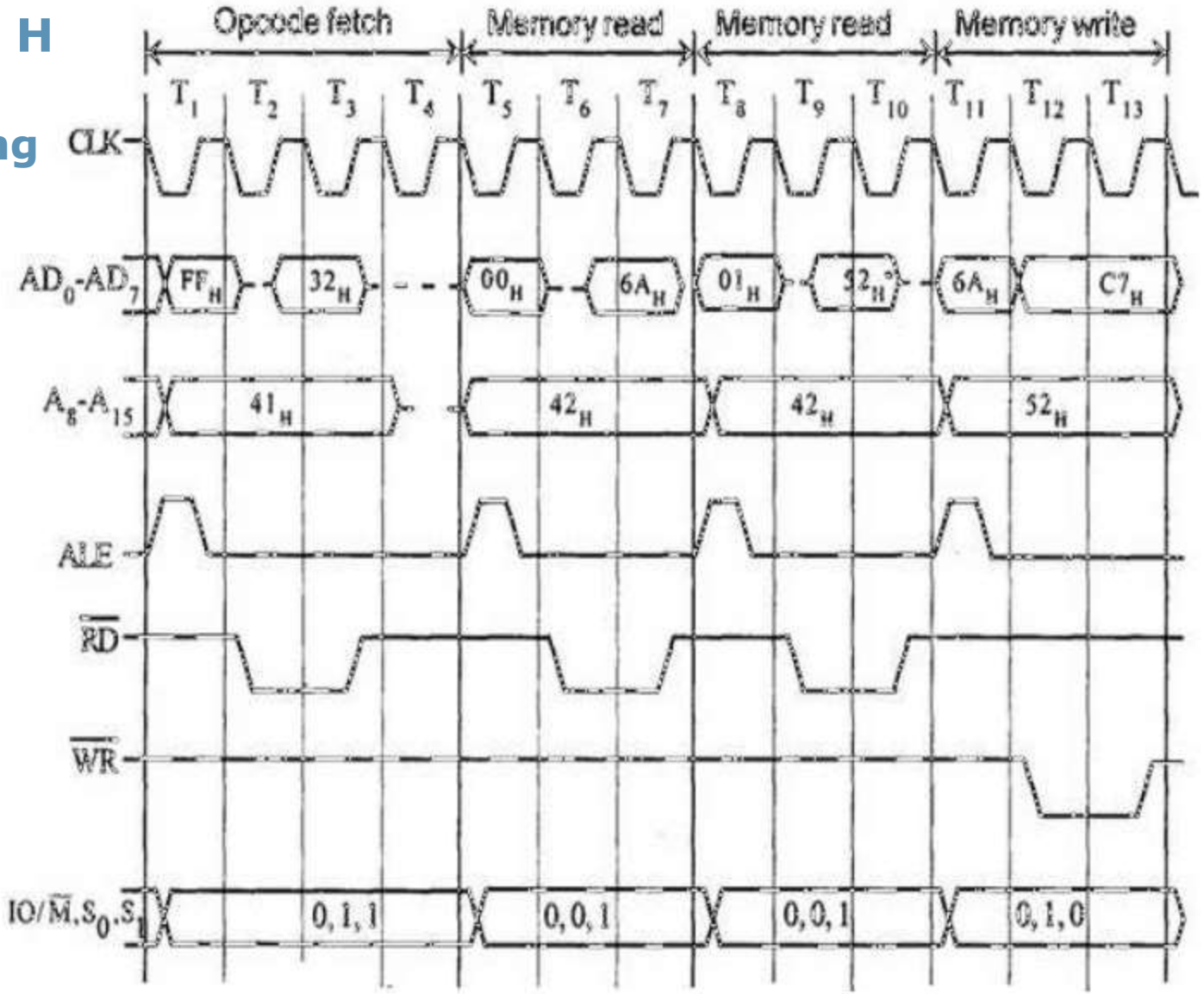

Op-Code Fetch Cycle
Memory Read Cycle
Memory Read Cycle
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
A0h
A0h
A0h
A15- A8 (Higher Order Address bus)
00h
21h
01h
45h
02h
F0h
DA7-DA0 (Lower order address/data Bus)
ALE
RD
WR
IO/M

Example 6:

STA 526A H

Corresponding Coding:

41FFH 32H
4200H 6AH
4201H 52H



Thank You ☺