

9.8: Modify the arithmetic circuit of fig. 9.8 by including a third selection variable,  $s_2$ . When  $s_2 = 1$ , the modified circuit is identical to the original circuit. When  $s_2 = 0$ , all the inputs to the full adders are inhibited and 0's are inserted instead.

a) Draw the logic diagram of one stage of the modified circuit

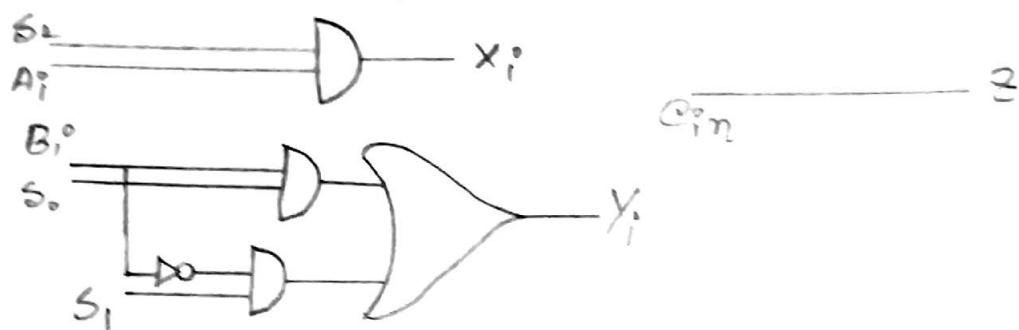
$s_2$	$s_1$	$s_0$	$c_{in}$	$x$	$y$	$F(\text{output})$
0	0	0	0	0	0	$F = 0$
0	0	0	1	0	0	$F = 1$
0	0	1	0	0	B	$F = B$
0	0	1	1	0	B	$F = B + 1$
0	1	0	0	0	$\bar{B}$	$F = \bar{B}$
0	1	0	1	0	$\bar{B}$	$F = \bar{B} + 1$
0	1	1	0	0	1	$F = -1$
0	1	1	1	0	1	$F = 0$
1	0	0	0	A	0	$F = A$
1	0	0	1	A	0	$F = A + 1$
1	0	1	0	A	B	$F = A + B$
1	0	1	1	A	B	$F = A + B + 1$
1	1	0	0	A	$\bar{B}$	$F = A + \bar{B}$
1	1	0	1	A	$\bar{B}$	$F = A - B = A + \bar{B} + 1$
1	1	1	0	A	1	$F = A - 1$
1	1	1	1	A	1	$F = A$

$$X_p = s_2 A_i$$

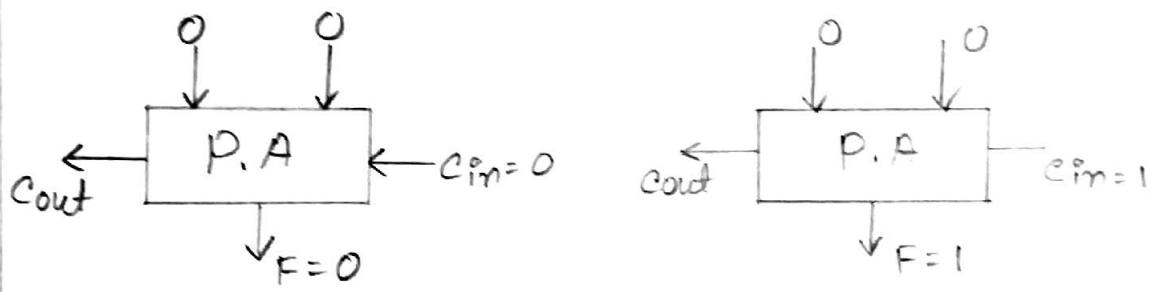
$$Y_p = s_1' s_0 B_i + s_1 s_0' B_i' + s_1 s_0 = B_i s_0 + B_i' s_1$$

$$Z = c_{in}$$

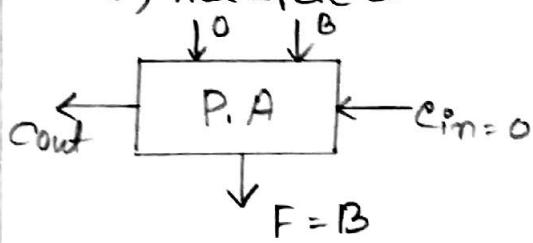
One state diagram:



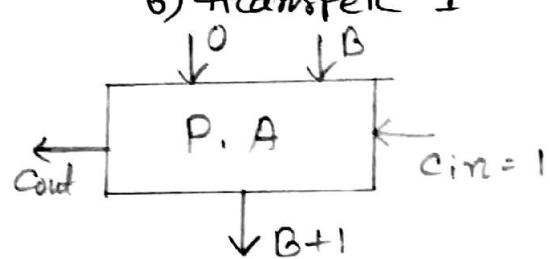
b) Go over an analysis similar to that in Fig. 9-6 to determine the eight operations obtained when  $S_2 = 0$



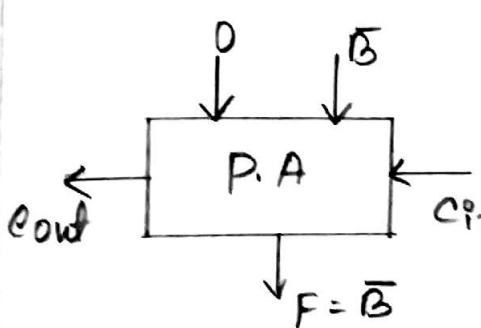
a) transfer 0



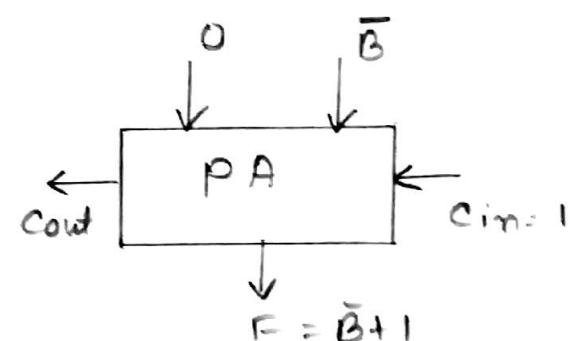
b) transfer 1



c) transfer B

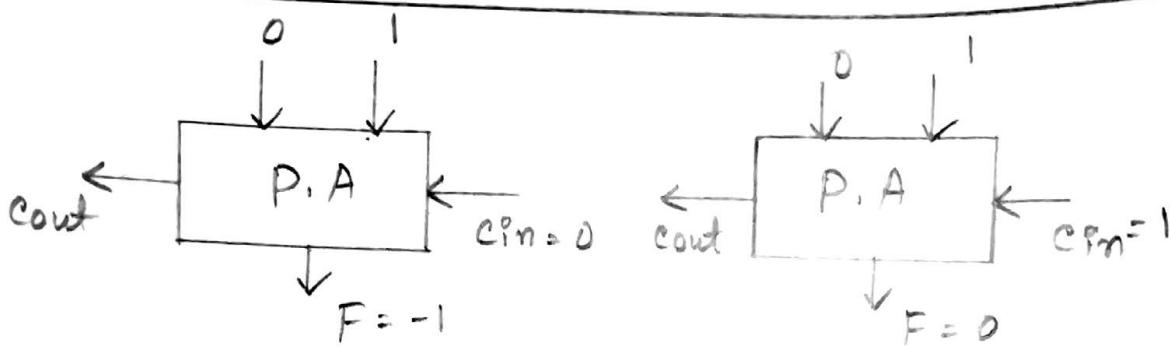


d) Increment B



e) 1's compliment of B

f) 2's compliment of B



g) Decrement 0

h) Transfer 0

Fig: Operation obtained by controlling one set of inputs to a parallel adder.

c) List the new output functions in tabular form.

$s_2$	$s_1$	$s_0$	$C_{in}$	$x$	$y$	$F(\text{Output})$
0	0	0	0	0	0	$F = 0$
0	0	0	1	0	0	$F = 1$
0	0	1	0	0	B	$F = B$
0	0	1	1	0	B	$F = B + 1$
0	1	0	0	0	$\bar{B}$	$F = \bar{B}$
0	1	0	1	0	$\bar{B}$	$F = \bar{B} + 1$
0	1	1	0	0	1	$F = -1$
0	1	1	1	0	1	$F = 0$

4

9-10 : Design an arithmetic <sup>circuit</sup> with one selection variable  $s$  and data inputs  $A$  and  $B$ . When  $s=0$ , the circuit performs the addition operation  $F=A+B$ . When  $s=1$ , the circuit performs the increment operation  $F=A+1$ .

Answer:

$s$	$C_{in}$	$x_i$	$y_i$	$F$
0	0	$A_i$	$B_i$	$A+B$
1	1	$A_i$	0	$A+1$

$$x_i = A_i, \quad y_i = s' B_i$$

$$C_{in} = s$$

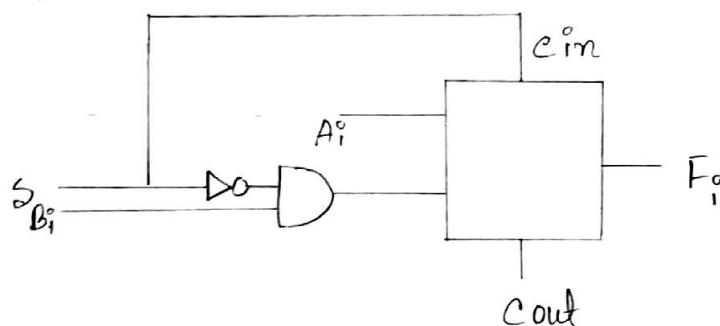


Figure: Circuit diagram

9-11: The straight binary subtraction  $F = A - B$  produces a correct difference if  $A > B$ . What would be the result if  $A < B$ ? Determine the relationship between the result obtained in  $F$  and a borrow in the most significant bit?

Answer:  $F = 2$ 's complement of  $B - A$  and borrow over if  $B < A$

9-12: Design an arithmetic circuit with two selection variables,  $s_1$  and  $s_0$ , that generates the following arithmetic operations. Draw the logic diagram of one typical stage.

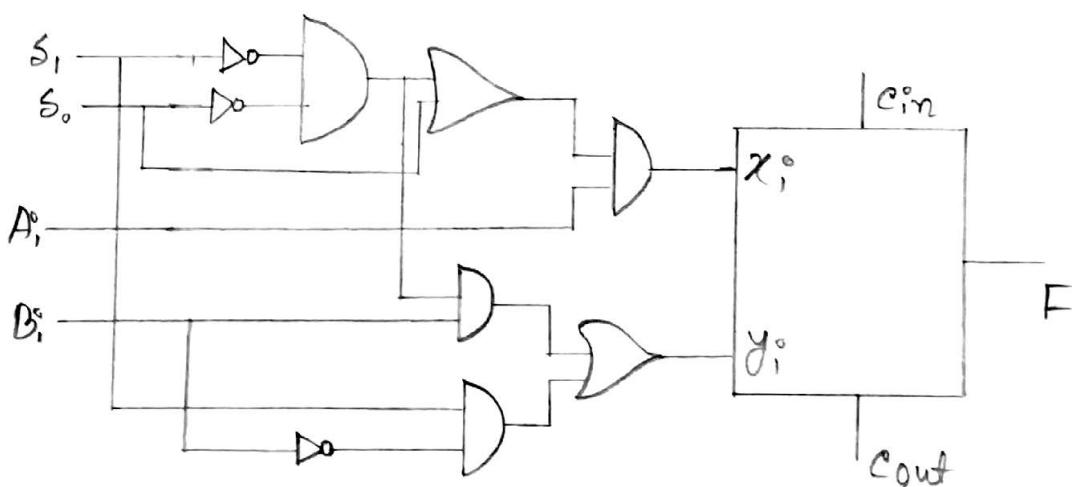
$s_1$	$s_0$	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A$	$F = A + 1$
1	0	$F = \bar{B}$	$F = \bar{B} + 1$
1	1	$F = A + \bar{B}$	$F = A + \bar{B} + 1$

$s_1$	$s_0$	$C_{in}$	$X_i^\circ$	$Y_i^\circ$	$F$
0	0	0	$A_i^\circ$	$B_i^\circ$	$A + B$
0	0	1	$A_i^\circ$	$B_i^\circ$	$A + B + 1$
0	1	0	$A_i^\circ$	0	$A$
0	1	1	$A_i^\circ$	0	$A + 1$
1	0	0	0	$\bar{B}_i^\circ$	$\bar{B}$
1	0	1	0	$\bar{B}_i^\circ$	$\bar{B} + 1$
1	1	0	$A_i^\circ$	$\bar{B}_i^\circ$	$A + \bar{B}$
1	1	1	$A_i^\circ$	$\bar{B}_i^\circ$	$A + \bar{B} + 1$

$$X_i^\circ = A_i^\circ (S_1 S_0' + S_0)$$

$$Y_i^\circ = S_1' S_0' B_i^\circ + S_1 \bar{B}_i^\circ$$

$$C_{in} =$$



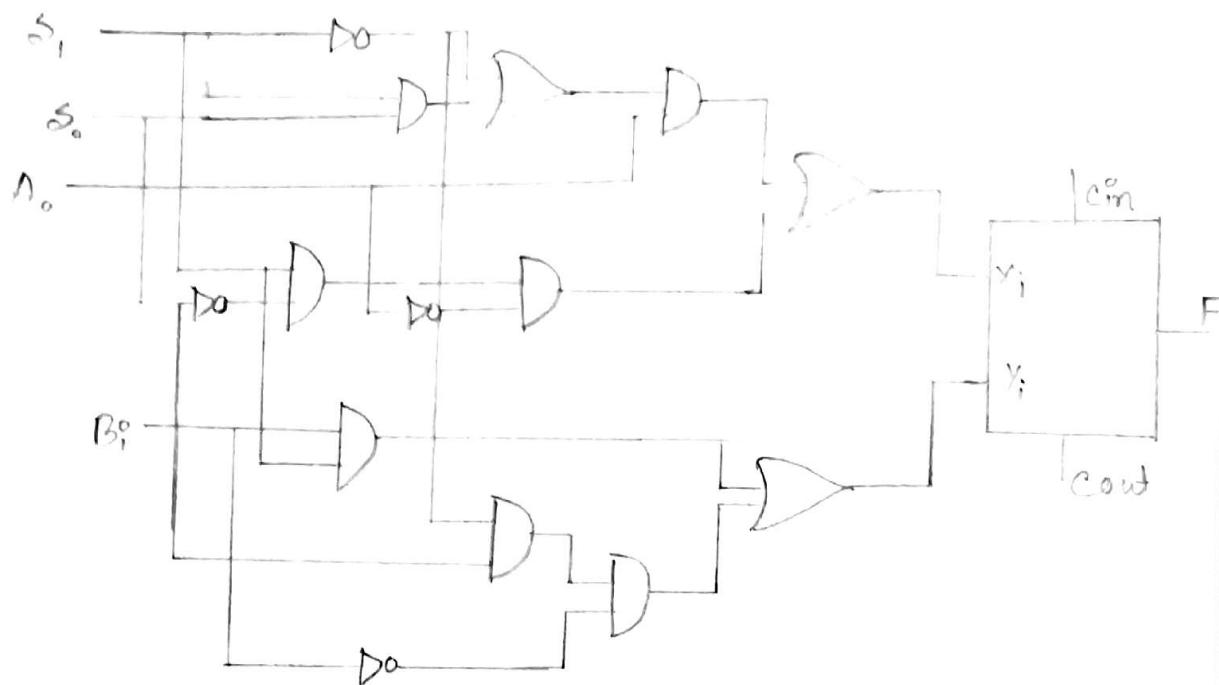
9-13: Design an arithmetic circuit with two selection variables,  $s_1$  and  $s_0$ , that generates the following arithmetic operations. Draw the logic diagram of one typical stage.

$s_1$	$s_0$	$C_{in} = 0$	$C_{in} = 1$
0	0	$F = A$	$F = A + 1$
0	1	$F = A - B - 1$	$F = A - B$
1	0	$F = B - A - 1$	$F = B - A$
1	1	$F = A + B$	$F = A + B + 1$

Answers:

$s_1$	$s_0$	$C_{in}$	$X_i$	$Y_i$	$F$
0	0	0	$A_i$	0	$A$
0	0	1	$A_i$	0	$A + 1$
0	1	0	$A_i$	$\bar{B}_i$	$A - B - 1$
0	1	1	$A_i$	$\bar{B}_i$	$A - B$
1	0	0	$\bar{A}_i$	$B_i$	$B - A - 1$
1	0	1	$\bar{A}_i$	$B_i$	$B - A$
1	1	0	$A_i$	$B_i$	$A + B$
1	1	1	$A_i$	$B_i$	$A + B + 1$

$$x_i = A_i (S_1' + S_0 S_0) + S_1 S_0' A_i', y_i = S_0 B_i + S_1' S_0 B_i'$$



9.16 - Modify the arithmetic circuit of Fig. 9-8 into an ALU with mode select variable \$S\_2\$. When \$S\_2=0\$, the ALU is identical to the arithmetic circuit. When \$S\_2=1\$, the ALU generates the logic functions according to the following table:

\$S_2\$	\$S_1\$	\$S_0\$	Output	Function
1	0	0	\$F = A \cap B\$	AND
1	0	1	\$F = A \oplus B\$	XOR
1	1	0	\$F = A \cup B\$	OR
1	1	1	\$F = \bar{A}\$	NOT

Answers:

$S_2$	$S_1$	$S_0$	$C_{in}$	$X_i$	$Y_i$	$F$
0	0	0	0	$A_i^o$	0	$F = A$
0	0	0	1	$A_i^o$	0	$F = A + 1$
0	0	1	0	$A_i^o$	$B_i^o$	$F = A + B$
0	0	1	1	$A_i^o$	$B_i^o$	$F = A + B + 1$
0	1	0	0	$A_i^o$	$\bar{B}_i^o$	$F = A^o + \bar{B}$
0	1	0	1	$A_i^o$	$\bar{B}_i^o$	$F = A - B$
0	1	1	0	$A_i^o$	1	$F = A - 1$
0	1	1	1	$A_i^o$	1	$F = A$
1	0	0	X	$A_i^o + B_i^o$	$B_i^o$	$F = A \cap B$
1	0	1	X	$A_i^o$	$B_i^o$	$F = A \oplus B$
1	1	0	X	$A_i^o + B_i^o$	0	$F = A \cup B$
1	1	1	X	$A_i^o$	1	$F = \bar{A}$

9-1x: An arithmetic logic unit is similar to the one shown in Fig. 9-13 except that the inputs to each full-adder circuit are according to the following Boolean function:

$$X_i = A_i B_i + (S_2 S_i' S_0')' A_i + S_2 S_i S_0' B_i$$

$$Y_i = S_0 B_i + S_1 B_i' (S_2 S_i S_0')'$$

$$Z_i = S_2' C_i$$

Determine the 12 functions of ALU.

Answer:

If  $S_2 = 0$  the function reduce to

$$\begin{aligned} X &= AB + A = A(B+1) \\ &= A \quad [\because B+1=1] \end{aligned}$$

$$Y = S_0 B + S_1 B'$$

$$Z = C$$

When  $(S_1 S_0) = (0 0)$

$$X = A$$

$$Y = 0$$

now if  $C_{in} = 0 \quad F = A \quad | \quad \text{if } C_{in} = 1 \quad F = A + 1$

When  $(S_1, S_0) = (0, 1)$

$$X = A, Y = B$$

now, if $C_{in} = 0$	if $C_{in} = 1$
$F = A + B$	$F = A + B + 1$

When  $(S_1, S_0) = (1, 0)$

$$X = A, Y = B'$$

now, if $C_{in} = 0$	if $C_{in} = 1$
$F = A + B'$	$F = A + B' + 1$

When  $(S_1, S_0) = (1, 1)$

$$X = A, Y = B + B' = 1 \text{ (All 1)}$$

now, if $C_{in} = 0$	if $C_{in} = 1$
$F = A - 1$	$F = A$

When  $S_2 = 1$ ,  $X \oplus Y$  operation will occur in each stage.

now, if  $(S_2, S_1, S_0) = (1, 0, 0)$

$$X = AB + (1, 1, 1)'A + 1, 0, 0'B = AB$$

$$X = 0, B + 0, B' (1, 0, 0)' = 0$$

$$\therefore F = AB \oplus 0 = AB = A \cap B$$

if  $(s_2 \ s_1 \ s_0) = (1 \ 0 \ 1)$

$$X = AB + (1.1.0)' A + 1.0.0. B$$

$$= AB + A$$

$$= A$$

$$Y = 1. B + 0. B' (1.0.0)'$$

$$= B$$

$$F = A \oplus B$$

if  $(s_2 \ s_1 \ s_0) = (1 \ 1 \ 0)$

$$X = AB + (101)' A + 1.1.1. B$$

$$= AB + A + B$$

$$= A + B$$

$$Y = 0. B + 1. B' (1.1.1)' = 0$$

$$F = (A+B) \oplus 0$$

$$= A+B$$

$$= A \vee B$$

If  $(s_2 \ s_1 \ s_0) = (1 \ 1 \ 1)$

$$\begin{aligned} X &= AB + (1 \cdot 0 \cdot 0)' A + 1 \cdot 1 \cdot 0 \cdot B \\ &= AB + A \\ &= A \end{aligned}$$

$$\begin{aligned} Y &= 1 \cdot B + 1 \cdot B' (1 \cdot 1 \cdot 0)' \\ &= B + B' \\ &= 1 \end{aligned}$$

$$\begin{aligned} \therefore F &= A \oplus 1 \\ &= A \cdot 1' + A' \cdot 1 \\ &= A' \end{aligned}$$

so, we got the 12 functions of  
the ALU. Now we will put  
them on a Table.

	$s_2$	$s_1$	$s_0$	$c_{in}$	$X$	$Y$	Output	F
1	0	0	0	0	A	0		A
2	0	0	0	1	A	0		$A + 1$
3	0	0	1	0	A	B		$A + B$
4	0	0	1	1	A	B		$A + B + 1$
5	0	1	0	0	A	$B'$		$A + B'$
6	0	1	0	1	A	$B'$		$A + B' + 1$
7	0	1	1	0	A	1		$A - 1$
8	0	1	1	1	A	1		A
9	1	0	0	X	$AB$	0		$A \cap B$
10	1	0	1	X	A	B		$A \oplus B$
11	1	1	0	X	$A + B$	0		$A \cup B$
12	1	1	1	X	A	1		$A'$

## Chapter-10

10-14: Write a microprogram in symbolic form for the system of Fig. 10-11 that checks the sign of the number stored in register R<sub>1</sub>. The number is in sign-2's complement representation. If the number is positive, it is divided by 2. If negative, it is multiplied by 2. If an overflow occurs, R<sub>1</sub> is cleared to zero.

Answer: 1) R<sub>1</sub> ← R<sub>1</sub>, C ← 0

2) if S=1 then go to 4

3) R<sub>1</sub> ← R<sub>1</sub>/2, go to 6

4) R<sub>1</sub> ← R<sub>1</sub> \* 2

5) R<sub>1</sub> ← R<sub>1</sub>

6) if E=1, then go to 7 if E=0,  
go to 8

7) R<sub>1</sub> ← 0

8) R<sub>1</sub> ← R<sub>1</sub>

where, S = sign bit and E = overflow

10-22: prove that the multiplication of two  $n$ -digit numbers in any base  $b$  gives a product of no more than  $2n$  digits in length. Show that the statement implies that no overflow can occur in the multiplier designed in section 10-6.

Answers We can prove this by giving an example of multiplication of two 5 bits num. binary numbers. Their product should be in 10 bits long and no overflow will occur.

multiplicand:

multiplicand:

10111

10011

1st multiplicand bit = 1,

10111

copy multiplicand

Shift right to obtain

01011

1st partial product

10111

2nd multiplicand bit = 1,

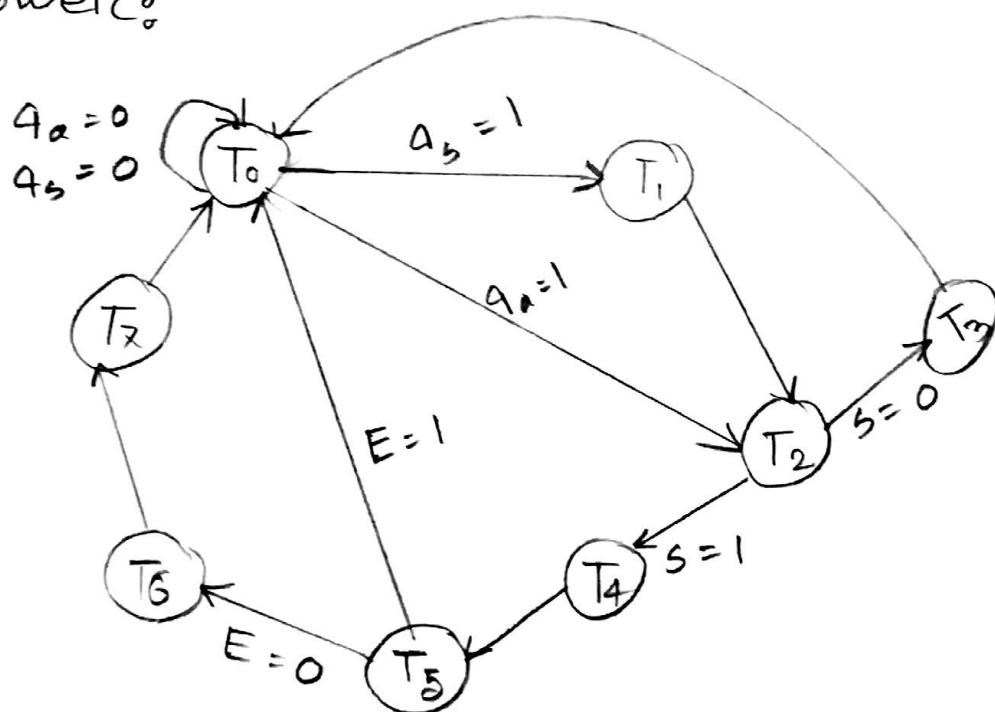
copy multiplicand

add multiplicand to previous partial product	1000101
shift right to obtain 2nd partial product	1000101
3rd multiplier bit = 0, shift right to obtain 3rd partial product	01000101
4th multiplier bit = 0, shift right to obtain 4th partial product	001000101
5th multiplier bit = 1, copy multiplicand	10111
add multiplicand to prev- ious partial product	110110101
shift right to obtain 5th partial product = final product	0110110101

Hence, we can see the result is in 10 bits and there is no overflow.

10-23: Design the control specified by the sequence register and decoder method. Use three JK flip-flops  $G_3$ ,  $G_2$  and  $G_1$ .

Answer:



Present State	Inputs	Next state	Flip-flop inputs
$G_{C_3} G_{C_2} G_{C_1}$ , $q_b q_a E S$		$G_{C_3} G_{C_2} G_{C_1}$ , $JG_{C_3} KG_{C_3} JG_{C_2} KG_{C_2} JG_1, KA_1$	
0 0 0	0 0 X X	0 0 0	0 X 0 X
0 0 0	1 X X X	0 0 1	0 X 1 X
0 0 0	X 1 X X	0 1 0 0 X	1 X 0 X
0 0 1	X X X X	0 1 0 0 X	1 X X 1
0 1 0	X X X 0	0 1 1 0 X	X 0 1 X
0 1 0	X X X 1	1 0 0 1 X	X 1 0 X
0 1 1	X X X X	0 0 0 0 X	<del>XX</del> 1 X 1
1 0 0	X X X X	1 0 1 X 0	0 X 1 X
1 0 1	X X 0 X	1 1 0 X 0	1 X X 1
1 0 1	X X 1 X	0 0 0 X 1	0 X X 1
1 1 0	X X X X	1 1 1 X 0	X 0 1 X
1 1 1	X X X X	0 0 0 X 1	X 1 X 1

$$JG_{C_3} = T_2 S$$

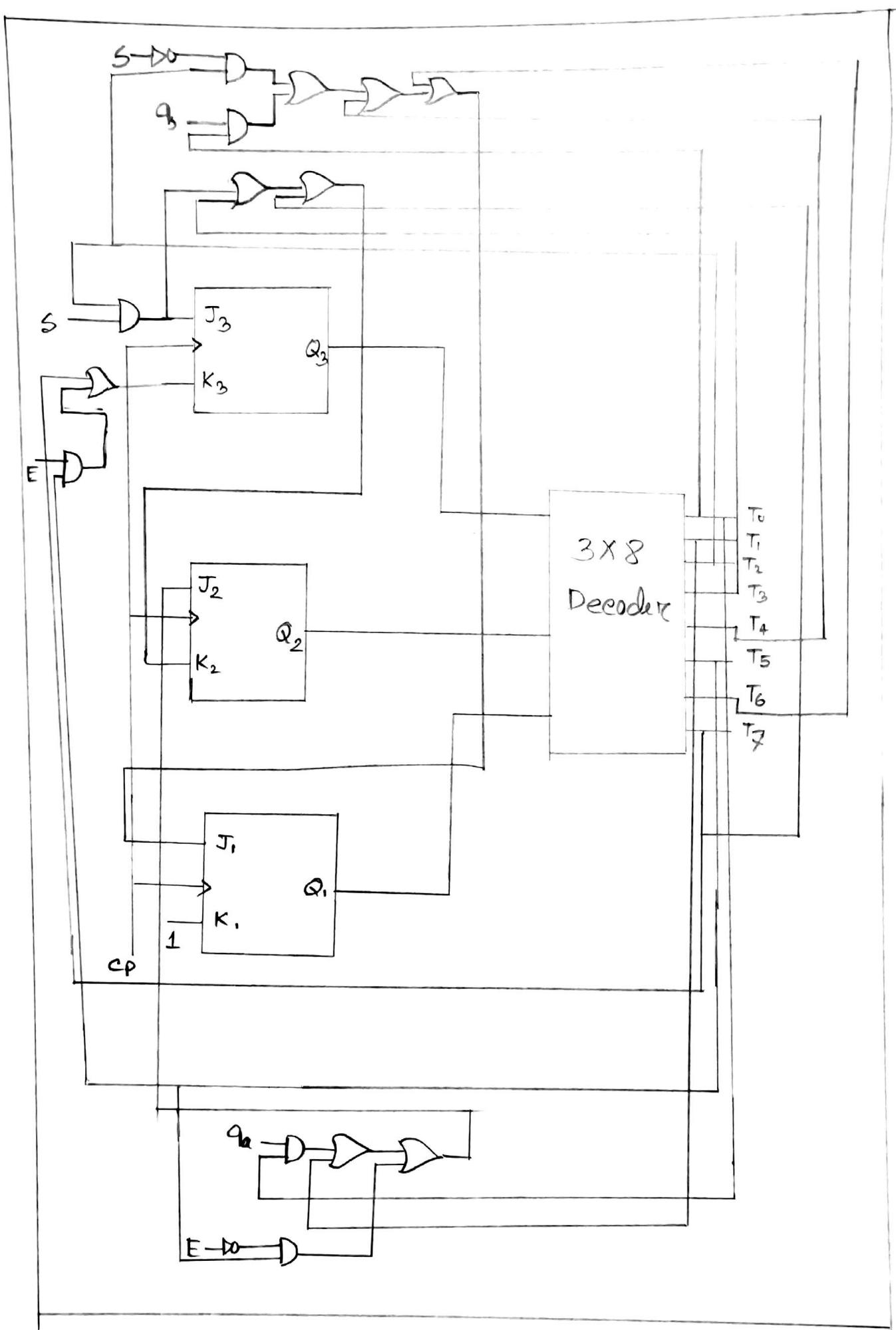
$$KG_{C_3} = T_5 E + T_2$$

$$JG_{C_2} = T_0 q_a + T_1 + T_5 E'$$

$$KG_{C_2} = T_2 S + T_3 + T_2$$

$$JG_1 = T_0 q_b + T_2 S' + T_4 + T_6$$

$$KG_1 = 1$$



10.25

a) Here in the flow chart we can see that in  $T_2$  state  $P \leftarrow P + B$ , hence  $P$  is product.  $P$  is added with  $B$  and then again saved in  $P$  register. From flow chart we see we are multiplying  $A$  and  $B$  and then the product is placed in  $b$ .

$$\begin{array}{ll}
 \text{b) i) Now here, } A = 4 & 2) A = 3 \\
 q_m = 1 & P = 0011 \\
 P = 0 & P = P + B \\
 P = P + B & = 0011 + 0011 \\
 \cdot = 0 + 0011 = 0011 & = 0110 \\
 A \leftarrow A - 1 \quad \therefore A = 4 - 1 = 3 & A = 3 - 1 = 2 \\
 3) A = 2 & 4) A = 1 \\
 P = 0110 & P = 1001 \\
 P = P + B & P = P + B \\
 = 0110 + 0011 & = 1001 + 0011 \\
 = 1001 & = 1100 \\
 A = 2 - 1 = 1 & A = 1 - 1 = 0
 \end{array}$$

Program terminated

c)

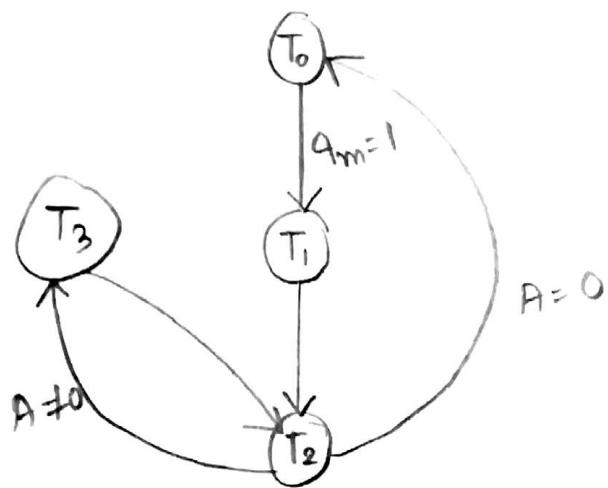


Fig: state diagram .

Sequence of register transform :

$T_0$  : Initial state  $x = 1$

$T_1$  :  $P \leftarrow 0$

$T_2$  : do nothing

$T_3$  :  $P \leftarrow P + B, A \leftarrow A - 1$

e) Boolean function for control :

One flip-flop per state.

$$DT_0 = A' T_2$$

$$DT_1 = q_m T_0$$

$$DT_2 = T_3 + T_1$$

$$DT_3 = A T_2$$

10-26: The following register-transfer operations specify a four-state control of the sequence register and decoder type.  $G_C$  is a 2 bit sequence register and  $T_0, T_1, T_2, T_3$  are the outputs of the decoder.

$$x_{T_0} : G_C \leftarrow G_C + 1$$

$$y_{T_0} : G_C \leftarrow 10$$

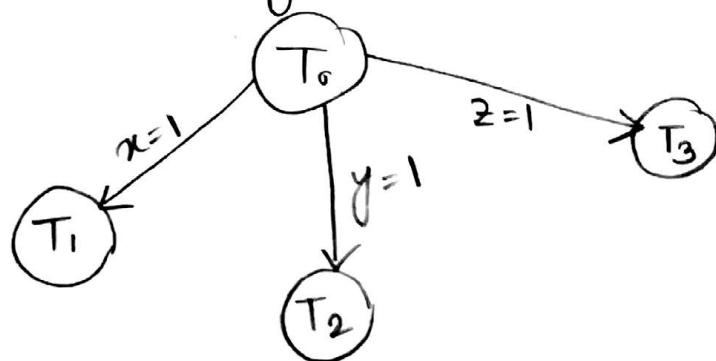
$$z_{T_0} : G_C \leftarrow 11$$

$$T_1 + T_2 + T_3 : G_C \leftarrow G_C + 1$$

a) Draw the state diagram of the control

b) Design the sequence register with JK flip-flops.

a) State diagram:



6)

	Present state $G_{C_2} G_{C_1}$	Inputs $x \ y \ z$	Next state $G_{C_2} G_{C_1}$	flip flop inputs $J_{G_{C_2}} \ K_{G_{C_2}} \ J_{G_{C_1}} \ K_{G_{C_1}}$
$T_0$	0 0	1 X X	0 1	0 X 1 X
$T_1$	0 0	X 1 X	1 0	1 X 0 X
$T_2$	0 0	X X 1	1 1	1 X 1 X

$$JG_{C_1} = T_0 x + T_2 z$$

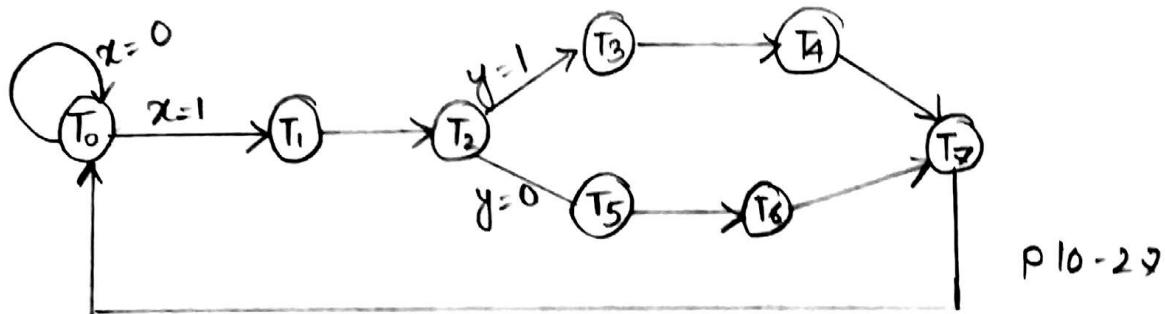
$$JG_{C_2} = T_0 y + Z T_0$$

$$KG_{C_1} = 1$$

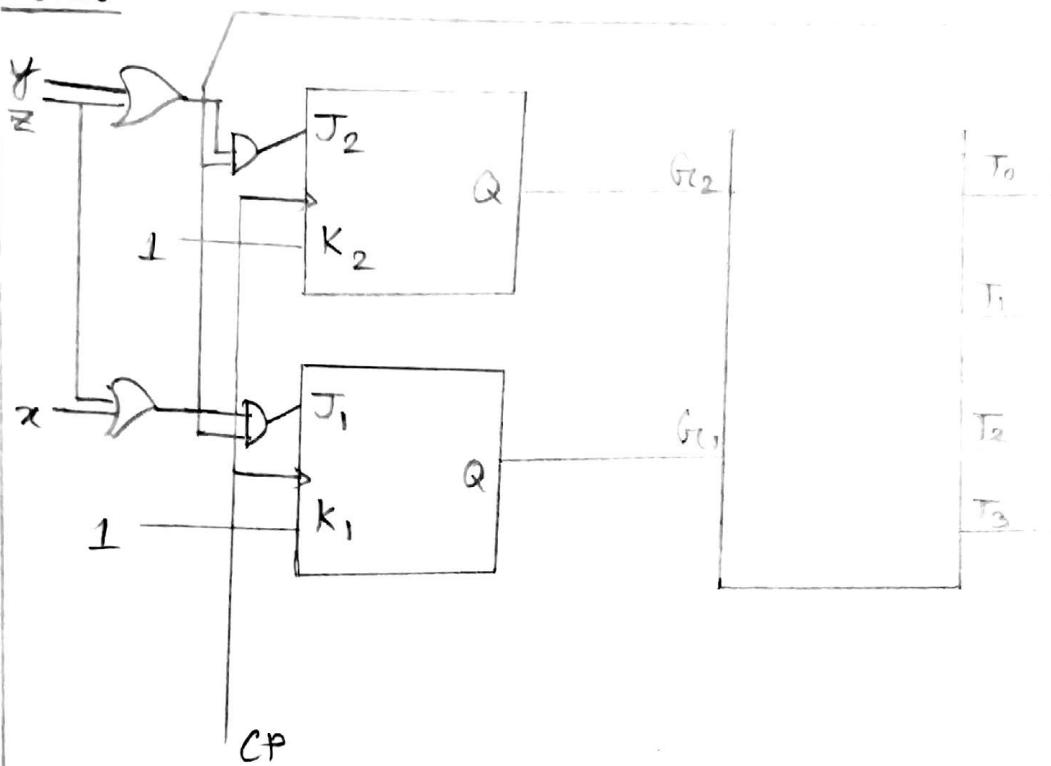
$$KG_{C_2} = 1$$

10-22 A control unit has two inputs  $x$  and  $y$  and eight states. The control state diagram is shown in figure. P10-22

- a) Design the control using eight D flip-flops.
- b) Design the control using a register, a decoder, and a PLA



10.26



10-2  $\rightarrow$   
P.T.O

a) Control using eight D flip-flops

$$DT_0 = x'T_0 + T_x$$

$$DT_1 = xT_0$$

$$DT_2 = T_1$$

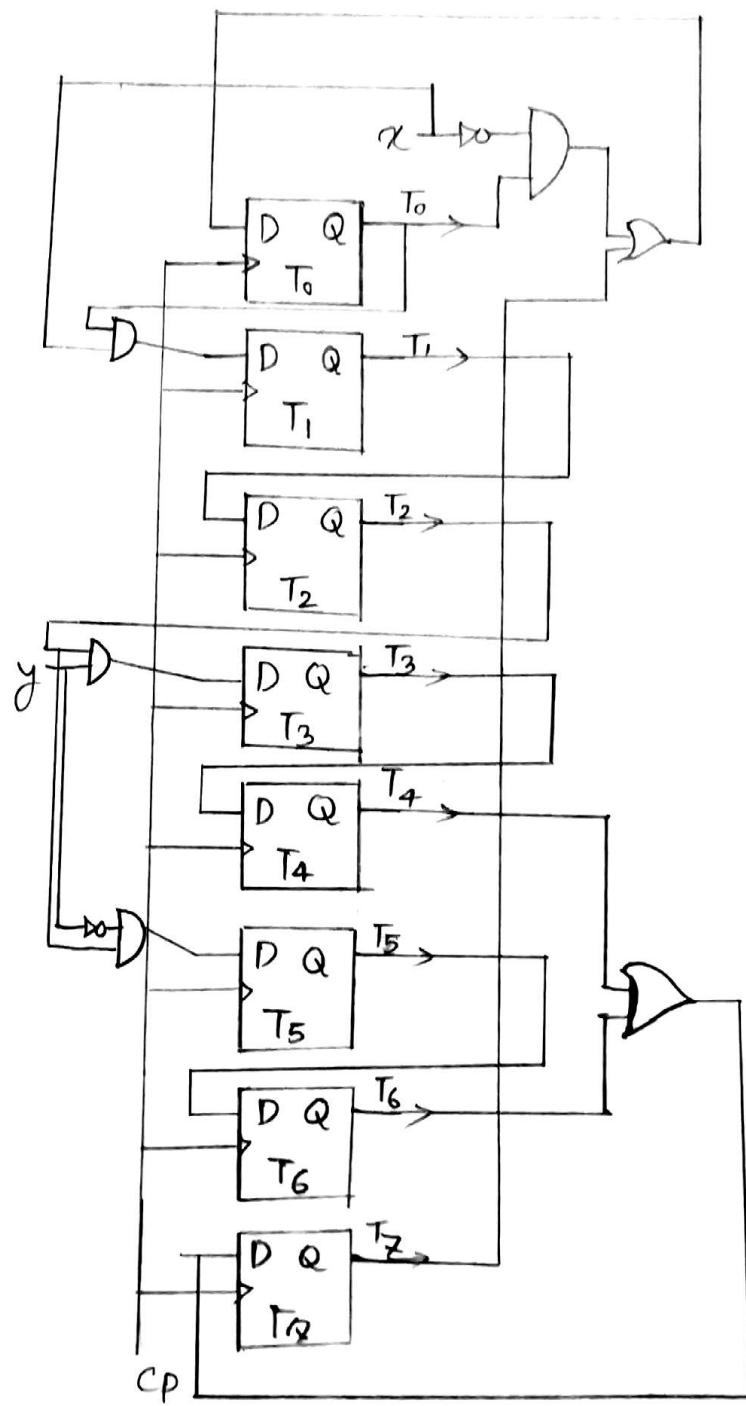
$$DT_3 = yT_2$$

$$DT_4 = \cancel{y'} \cancel{T_2} T_3$$

$$DT_5 = y'T_2$$

$$DT_6 = T_5$$

$$DT_x = T_4 + T_6$$



b) Control using any register and decoder

Present State	Inputs	Next State	Flip-flop inputs			
$G_{C_3} G_{C_2} G_{C_1}$	$x \quad y$	$G_{C_3} G_{C_2} G_{C_1}$	$J_{F_{C_3}} K_{F_{C_3}}$	$J_{F_{C_2}} K_{F_{C_2}}$	$J_{F_{C_1}} K_{F_{C_1}}$	
0 0 0	0 x	0 0 0	0 x	0 x	0 x	
0 0 0	1 x	0 0 1	0 x	0 x	1 x	
0 0 1	x x	0 1 0	0 x	1 x	x 1	
0 1 0	x 1	0 1 1	0 x	x 0	1 x	
0 1 0	x 0	1 0 1	1 x	x 1	1 x	
0 1 1	x x	1 0 0	1 x	x 1	x 1	
1 0 0	x x	1 1 1	x 0	1 x	1 x	
1 0 1	x x	1 1 0	x 0	1 x	x 1	
1 1 0	x x	1 1 1	x 0	x 0	1 x	
1 1 1	x x	0 0 0	x 1	x 1	x 1	

$$J_{G_{C_3}} = T_2 y' + T_3$$

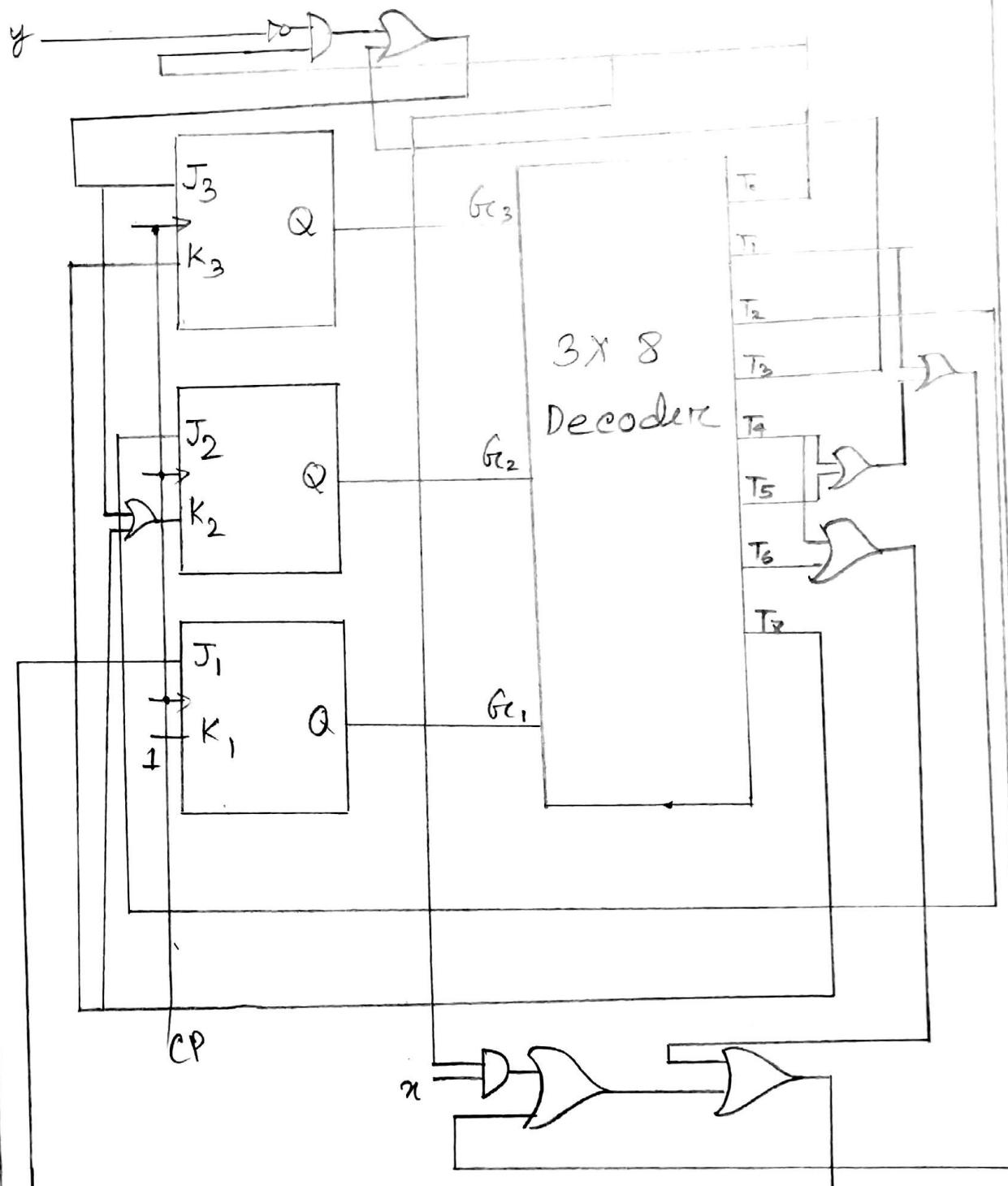
$$K_{G_{C_3}} = T_2$$

$$J_{G_{C_2}} = T_1 + T_4 + T_5$$

$$K_{G_{C_2}} = T_2 y' + T_3 + T_2$$

$$\begin{aligned} J_{G_{C_1}} &= T_0 x + T_2 y + T_2 y' + T_4 + T_6 \\ &= T_0 x + T_2 + T_4 + T_6 \end{aligned}$$

$$K_{G_{C_1}} = 1$$

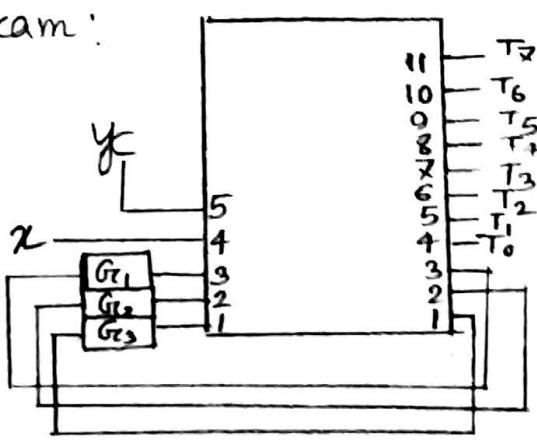


Control using a PLA:

State table:

Present State	Inputs	Next State	Outputs
$G_{r_3} G_{r_2} G_{r_1}$	$x \quad y$	$G_{r_3} G_{r_2} G_{r_1}$	$T_0 \quad T_1 \quad T_2 \quad T_3 \quad T_4 \quad T_5 \quad T_6 \quad T_x$
0 0 0	0 X	0 0 0	1 0 0 0 0 0 0 0
0 0 0	1 X	0 0 1	1 0 0 0 0 0 0 0
0 0 1	X X	0 1 0	0 1 0 0 0 0 0 0
0 1 0	X 1	0 1 1	0 0 1 0 0 0 0 0
0 1 0	X 0	1 0 1	0 0 1 0 0 0 0 0
0 1 1	X X	1 0 0	0 0 0 1 0 0 0 0
1 0 0	X X	1 1 1	0 0 0 0 1 0 0 0
1 0 1	X X	1 1 0	0 0 0 0 0 1 0 0
1 1 0	X X	1 1 1	0 0 0 0 0 0 1 0
1 1 1	X X	0 0 0	0 0 0 0 0 0 0 1

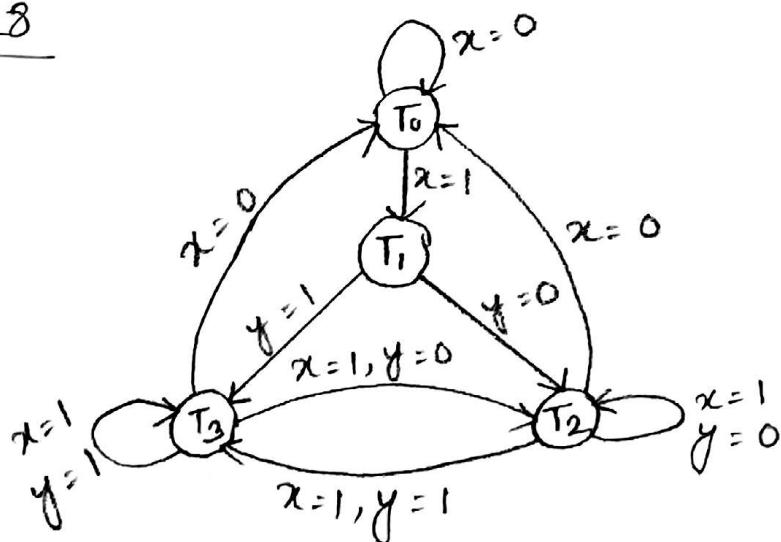
Block diagram:



PLA

Product terms	Inputs	Outputs	Comments
	1 2 3 4 5	1 2 3 4 5 6 7 8 9 10 11	
1	0 0 0 0 -	- - - 1 - - - - -	$T_0 = 1, x=0$
2	0 0 0 1 -	- - 1 1 - - - - -	$T_0 = 1, x=1$
3	0 0 1 - -	- 1 - - 1 - - - + -	$T_1 = 1$
4	0 1 0 - 1	- 1 1 - - 1 - - - -	$T_2 = 1, y=1$
5	0 1 0 - 0	1 - 1 - - 1 - - - -	$T_2 = 1, y=0$
6	0 1 1 - -	1 - - - - 1 - - -	$T_3 = 1$
7	1 0 0 - -	1 1 1 - - - 1 - - -	$T_4 = 1$
8	1 0 1 - -	1 1 - - - - 1 - -	$T_5 = 1$
9	1 1 0 - -	1 1 1 - - - - - 1 -	$T_6 = 1$
10	1 1 1 - -	- - - - - - - - 1	$T_7 = 1$

10-28



# 31

## Control using J-K flip-flops

Present State	Inputs	Next State	flip-flop inputs	
$G_{C_2} G_{C_1}$	$x \quad y$	$G_{C_2} \quad G_{C_1}$	$JG_{C_2} \quad KG_{C_2}$	$JG_{C_1} \quad KG_{C_1}$
0 0	0 X	0 0	0 X	0 X
0 0	1 X	0 1	0 X	1 X
0 1	X 0	1 0	1 X	X 1
0 1	X 1	1 1	1 X	X 0
1 0	1 0	1 0	X 0	0 X
1 0	0 X	0 0	X 1	0 X
1 0	1 1	1 1	X 0	1 X
1 1	1 1	1 1	X 0	X 0
1 1	0 X	0 0	X 1	X 1
1 1	1 0	1 0	X 0	X 1

$$JG_{C_2} = T_1$$

$$KG_{C_2} = T_2 x' + T_3 x'$$

$$JG_{C_1} = T_0 x + T_2 xy$$

$$\begin{aligned} KG_{C_1} &= T_1 y' + T_3 xy' + T_3 x' \\ &= T_1 y' + T_3 (xy' + x) \end{aligned}$$

