Date: 20/9/17

AHSANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY

Department of Computer Science & Engineering

Third year, First Semester — **Final Examination, Spring 2017**

Course No: ***CSE 3107*** — **Course Title:** ***Microprocessor***

Time: 3 hours — **Full Marks: 70**

[Answer any 5 questions out of 7.]
[Marks alloted are indicated in the right margin.]

---

1. (a) Differentiate between Protected Mode and Real Addressing Mode of Pentium processor in terms of accessible memory, maximum segment size and segment read/write protection. [3]

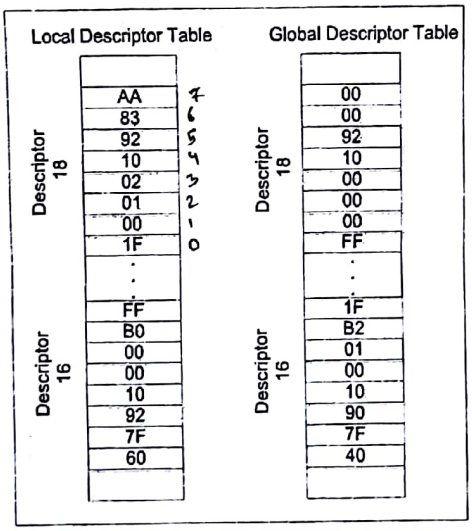
(b) How are the different bit groups of segment register interpreted in Protected Mode? [2]

(c) Figure 1 shows the contents of local and global descriptor tables. Suppose DS contains 0094H. Now, [6]

(i) Find the descriptor number, table indicator and table index RPL.

(ii) Find the base address and end address of the segment.

(iii) Give the status of access right bits.



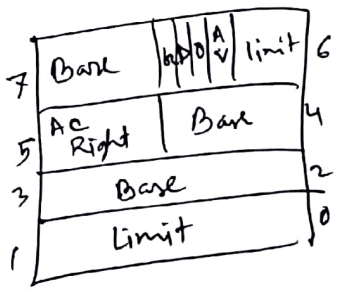


Figure 1: Contents of local and global descriptor tables.

Scanned by CamScanner

(d) Hyper - Threading and Turbo - Boost are the technologies introduced in latest Intel processors to improve performance. Now answer the following questions: [3]

(i) How does Hyper - Threading improve the parallelization of computations?

(ii) How does Turbo - Boost save energy?

2. (a) Draw the internal organization of 8086 microprocessor and describe the operation of BIU. [6]

(b) Describe how 20-bit address is used by 16-bit 8086 microprocessor. A memory location has physical address 80FD2h. In what segment does it have offset BFD2h? [4]

(c) Write the machine codes (in hexadecimal) for the following assembly instructions. Assume that the address of the first byte of the first instruction is 01000h. [4]

Instruction	Corresponding opcode
MOV CX, 08h	B9 08
LOOP1: ADD AX,[SI]	03 04
ADD SI,02h	83 C6
LOOP LOOP1	E2

3. (a) For the following instruction stored in 8085 memory draw the timing diagram showing contents of address bus, data bus and other signals. Also calculate the execution time for memory operations. You can assume the frequency of 8085 be 2 MHz. [6]

AD0 - AD7
A0 - A7
RD WR S0 S1 RD WR
IO/M 0 1 0

Instruction	Hex Code	Starting Address
OUT 8CH	D3 8C	A0FE

OF MR MW

(b) Write a program to simulate a traffic signal system where there are three traffic lights (*Green*, *Yellow* and *Red*) and two pedestrian signs (*Walk* and *Don't Walk*). A pedestrian can only walk when the Red light is turned on. The signal lights and signs are controlled by the data bits of output (*Port# 1C*) as shown below: [6]

Lights/Signs	Data Bits	On Time
Green	D_0	15 Sec
Yellow	D_2	10 Sec
Red	D_4	25 Sec
Walk	D_6	
Don't Walk	D_7	

Scanned by CamScanner

(c) Calculate the COUNT to obtain a 100 μs loop delay, and express the value in Hex. Assuming the system clock period is 0.33 μs. [2]

```
MVI B, COUNT
LOOP: NOP      ; 4 T-states
      NOP      ; 4 T-states
      DCR B    ; 4 T-states
      JNZ LOOP ; 10/7 T-states
```

4 (a) Differentiate between memory mapped I/O and peripheral mapped I/O. [3]

(b) Consider the sequential execution of the following program: [5]

Memory Address	Mnemonic
2100	LXI SP, 2500H
2140	CALL 3070 H
2143	Next instruction

Now show the contents of address bus, data bus, SP, PC and temporary registers in each machine cycle during the execution of the CALL instruction. The opcode of CALL instruction is *CD*.

(c) Consider the following program and answer the questions given below: *[6]*

```
1. LXI SP, 0400H
2. LXI B, 2055H
3. LXI H, 22FFH
4. LXI D, 2090H
5. PUSH H
6. PUSH B
7. MOV A, L
.........
20. POP H
```

(i) What is stored in the stack pointer register after the execution of line 1?

(ii) What is the memory location of the stack where the first data byte will be stored?

(iii) What is stored in memory location 03FEH when line 5 is executed?

(iv) After the execution of line 6, what is the address in the stack pointer register, and what is stored in stack memory location 03FDH?

(v) Specify the contents of register pair HL after the execution of line 20.

Scanned by CamScanner

5. (a) For the following instructions identify the addressing modes and calculate the physical address of the source operand. Assume CS = 2000H, DS = 543AH, SS = 9AC5H, SI = 3200H, DI = 2ABCH, BX = 3F00H, BP = 329AH. [4]

(i) MOV CL, 50h[BX][DI]

(ii) JMP BX

(iii) ADD AX, [SI]

(iv) MOV [BX+100H], AX

(b) Following program sums in AX the elements of the 10 - element array W. Now rewrite the code using based addressing mode. [2]

```
W DW 10, 20, 30, 40, 50, 60, 70, 80, 90, 100

XOR AX, AX
LEA SI, W
MOV CX, 10
ADDNOS:
      ADD AS, [SI]
      ADD SI, 2
      LOOP ADDNOS
```

(c) Find the values of SF, PF, ZF, CF and OF after execution of each of the following instructions. Assume that the flags are initially 0 for each instruction. [5]

(i) ADD AL, BL, where AL contains 80h, BL contains 80h

(ii) SUB AX, BX, where AX contains 8000h, Bx contains 0001h

(iii) INC AL, where AL FFh

(iv) MOV AX, -5

(v) NEG AX, where AX contains 8000h

(d) What do you understand by signed overflow? Suppose that AX and BX both contain positive numbers and ADD AX, BX is executed. Show that there is a carry out of the MSB but no carry into the MSB, if and only if signed overflow occurs. [3]

6. (a) Assume that 8085 microprocessor is completing an RST 7.5 interrupt request. Write a code to check if RST 6.5 is pending and if it is pending, enable RST 6.5 without affecting any other interrupts; otherwise, return to the main program. [4]

(b) What do you mean by Interrupt Vector Table (IVT) in 8086? Find the physical address of INT 13H and INT 8H in the IVT. [3]

Scanned by CamScanner

(c) Assume that: CS = 1000H, DS = 3000H, ES = 4000H, SS = 6000H, SP = 1258H, BP = 3254H, AX = 1234H, BX = 3456H, CX = 8760H, DX = 2893H, DI = 3210H, SI = 1000H. Now show the contents of stack and relevant registers after execution of each of the following instructions: [4]

(i) PUSH AX

(ii) PUSH SI

(iii) POP CX

(iv) POP DX

(d) Explain the following interrupts: [3]

(i) Divide-by-zero interrupt.

(ii) Break point interrupt.

(iii) Overflow interrupt.

7. (a) Differentiate between Minimum Mode and Maximum Mode of 8086. [4]

(b) Draw the block diagram showing the configuration of 8086 when $MN / MX^{-} = 0$ and briefly describe the functionalities of different blocks. [6]

(c) Write 8086 assembly code to interface 8086 with 7-segment FND using Intel 8255A and display digit 5. Your code should include necessary comments. [4]

Scanned by CamScanner