

**Ahsanullah University of Science and Technology**

Department of Computer Science and Engineering

2<sup>nd</sup> Year 1<sup>st</sup> Semester, Final Examination (Spring 2012)

Course No: CSE 205

Course Title: Digital Logic Design

Time: 3 Hours

Full Marks: 70

**[Marks allotted are indicated in the right margin]**There are seven (7) Questions. Answer any five (5).

(1)

a) Obtain Hamming coded message for "10110010011".

3

b) Implement AND, OR and NOT operations using NAND gates only.

3

c) Express the following function in a sum of minterms and a product of maxterms

4

$$F(w, x, y, z) = y'z + wxy' + wxz' + w'x'z$$

d) Simplify the following expressions by using Boolean Algebra:

4

$$\begin{aligned} & \cancel{(B+BC)} \cancel{(B+B'C)} \cancel{(B+D)} \\ & PQ'R' + PQ'R + PQR' + PQR + P'Q'R \end{aligned}$$

(2)

a) Simplify the following Boolean function by means of the tabulation method:

8

$$F(A, B, C, D) = A'B'C'D' + A'B'CD' + AB'CD + AB'CD' + A'BCD + A'BCD' + A'B'CD$$

b) What is don't care condition?

1

c) Design a full-adder circuit. Implement a full-adder with two half-adders and an OR gate.

3+2

(3)

a) Simplify the Boolean function  $F$  in sum of products using the don't care conditions  $d$ :

4

$$F = B'C'D' + B'CD' + ABCD'$$

$$d = B'CD' + A'BC'D$$

b) Obtain output expressions for BCD to excess-3 code converter.

5

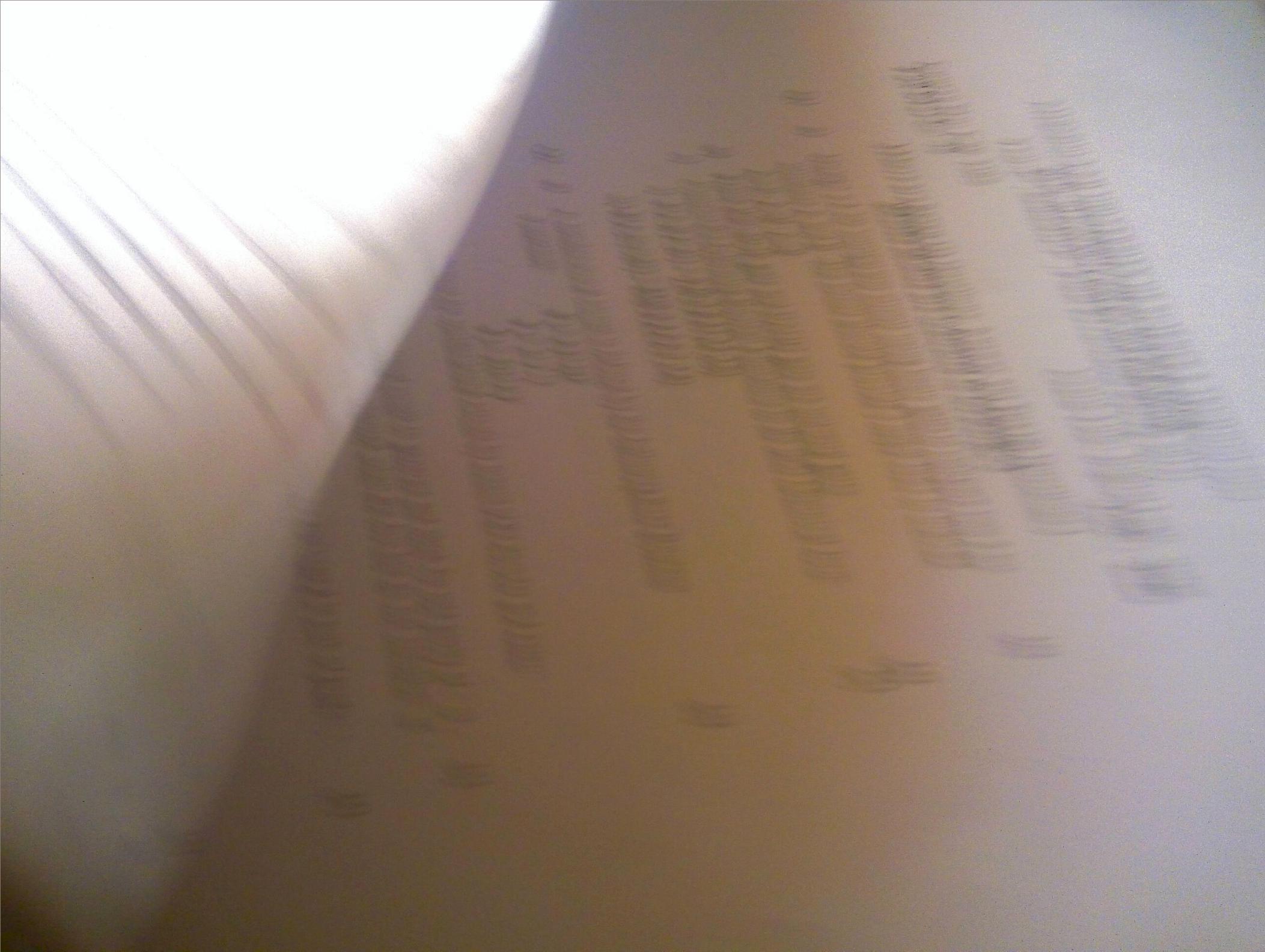
c) Design a combinational circuit that accepts a 3-bit binary number and generates outputs which are the odd parity ( $P_1$ ) and the even parity ( $P_2$ ). Odd and Even parity can be obtained by the following rules:

5

I. For Odd Parity: make the total number of 1's odd (including  $P_1$ )II. For Even Parity: make the total number of 1's even (including  $P_2$ )

a) What is magnitude comparator? Construct a 2-bit magnitude comparator.

1+4



Final Exam Questions

There are seven (7) questions. Answer any two (2) questions. The total marks available is 100.

(Q1) ~~10~~ The function is given by  $F(A, B, C, D) = A + B + C + D$ . Implement the following function by a 4 input OR gate.

$$F(A, B, C, D) = A \oplus B \oplus C \oplus D$$

Are there any don't care inputs? If yes, what are they?

Design a 4 to 16 decoder. A single output will be high at the following four times

and low 4 times

Prove the following expression using Boolean algebra.

$$A \oplus B = \overline{A}B + A\overline{B}$$

(Q2) ~~10~~ Design a 3 bit square combinational circuit

A combinational circuit is defined by the following logic functions:

$$P(0, 1, 2) = Y_1 + Z_1, \quad P(1, 2, 3) = Y_2 + Z_2$$

Implement the combinational circuit by means of the given

or Draw the circuit diagram of a 4 to 1 priority encoder with priorities as follows:  $1_0 > 1_1 > 1_2 > 1_3$

Design a counter circuit using 1 flip-flop for the following sequence

$$0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1$$

Design a JK flip flop and obtain its characteristic table, assuming initial

input  $x$ . When  $x = 0$ , the state of the output terminal remains. When  $x = 1$ , the circuit goes through the following state transitions

$$0 \rightarrow 1 \rightarrow 1 \rightarrow 0 \rightarrow 0 \rightarrow 1$$

Design a 4-bit 2's complement combinational circuit

(Q4) ~~10~~

# AIHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Computer Science and Engineering

Year: 2<sup>nd</sup>, Semester: 1<sup>st</sup>, Final Examination (Spring 2016)

**Course No:** CSE 2105

**Full Marks:** 70

[There are Seven (7) Questions. Answer any Five (5) Questions.]

[Marks allotted are indicated in the margin.]

- (Q1)** The Boolean expression,  $F(A, B, C, D) = \bar{A} + \bar{B}$  is a simplified version of [6] the following Boolean expression:

$$F(A, B, C, D) = \bar{A}\bar{C}(B \odot D) + A\bar{B}(C \oplus D) + A\bar{C}(B \oplus D)$$

Are there any don't care conditions? If so, what are they?

- b)** Design a BCD to Excess-3 code converter with a BCD to decimal decoder [5] and four OR gates.

**c)** Prove the following expression using Boolean algebra, [3]

$$A \odot \bar{B}C = \Sigma(0, 2, 3, 5).$$

**(Q2)** Design a 3-bit square combinational circuit. [5]

A combinational circuit is defined by the following two Boolean functions: [4]

$$F_1(x, y, z) = y' + xz'; \quad F_2(x, y, z) = x + x'y$$

Implement the combinational circuit by means of the decoder.

- d)** Draw the circuit diagram of a (4x2) priority encoder with priorities as follows:  $I_0 > I_1 > I_2 > I_3$ . [5]

**e)** Design a counter circuit using  $T$  flip-flops for the following sequence: [5]

$$0 \rightarrow 2 \rightarrow 4 \rightarrow 6 \rightarrow 0$$

**f)** Design a  $J-K$  flip-flop and obtain its characteristic table, excitation table. [4]

- g)** Design a sequential circuit with two  $D$  flip-flops namely  $D_A$ ,  $D_B$  and one input  $x$ . When  $x = 0$ , the state of the circuit remain same. When  $x = 1$ , the circuit goes through in the following state transitions:

$$00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$$

**h)** Design a 4-bit 2's complement combinational circuit. [5]



**ALISANULLAH UNIVERSITY OF SCIENCE & TECHNOLOGY**  
**Dept. of Computer Science and Engineering**  
**Year: 2<sup>nd</sup>, Semester: 1<sup>st</sup>, Final Examination (Spring 2013)**

Course No: CSE 2105

Full Marks: 70

Course Title: Digital Logic Design  
 Time: 3 Hours

[There are Seven (7) Questions. Answer any Five (5) Questions.  
Marks allotted are indicated in the margin.]

Q1. a) Design a 4-bit comparator circuit using basic gates to compare two 4-bit numbers A and B. The circuit should provide 3 output lines to indicate  $A > B$ ,  $A < B$ ,  $A = B$ . [6]

b) Prove that, NOR gate and NAND gate are universal gates. [4]

c) Convert the following Boolean Functions to the other canonical form. [4]

i)  $F(A,B,C,D) = \sum(0,2,8,12,14,15)$ .

ii)  $F(A,\overline{B},\overline{C},D) = \prod(0,3,4,5,6,7,14)$ .

Q2. a) A combinational circuit is defined by the following three Boolean functions: [5]

$$F_1 = x'y + xy'$$

$$F_2 = x + y' + z$$

$$F_3 = xyz + x'y'$$

Implement the combinational circuit by means of the decoder and extender gates.

b) Design a combinational circuit to generate and check for odd parity of four bits. A logic-1 output is required when the four bits do not constitute an odd parity. [5]

c) Simplify the Boolean function F using the don't-care d in sum of products: [4]

$$F = A'D + A'CD + ABC.$$

$$d = A'B'C + ACD + AB'D.$$

Q3. a) Design a BCD Ripple Counter with JK flip-flops. [6]

b) Draw the circuit diagram of a JK flip-flop and then, obtain its characteristics table and characteristics equation. [4]

c) Design a synchronous 3-bit Up Counter using  $T$  flip-flops. [4]

- Q4. a) Design a BCD to excess-3 code converter with a BCD to decimal decoder and four OR gates. [4]

b) Implement the following function with a **8X1 MUX**. [4]

$$F(A,B,C,D) = \sum(0,1,2,4,8,10,15).$$

- c) Design a 4-bit Carry Look Ahead adder circuit. [6]

Q5. a) Obtain output expression for an 8-to-3 line Priority Encoder with priorities as follows:  $I_0 > I_1 > I_2 > I_3 > I_4 > I_5 > I_6 > I_7$ . [5]

b) Construct an  $8 \times 256$  decoder using  $4 \times 16$  decoders only. Use block diagrams. [5]

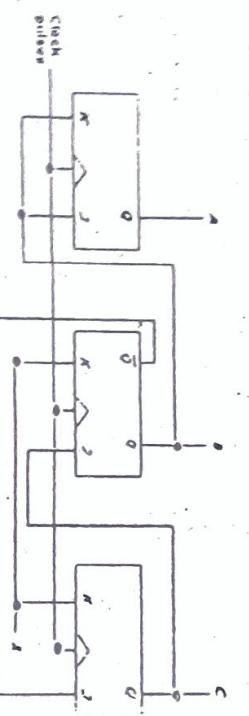
c) Find complement of the following functions: [4]

i)  $F(x,y,z) = (x+y+z)(x'+z)+(x'+y)$ .

ii)  $F(A, B, C, D, E) = (A'B'C + C) + D'E'$ .

Q6. a) How  $JK$  and  $T$  flip-flop can be obtained from  $D$  flip-flop? Show necessary diagram and equations. [4]

b) Draw the timing diagram for 8 clock pulses of the following circuit. [4]



- c) Design a 4-bit Binary Ripple Counter with  $JK$  flip-flops. [6]

- Q7. a) Simplify the Boolean Function  $F$  by means of the Tabulation Method, [6]

$$F(A,B,C,D,E,F,G) = \sum(20,28,38,35,39,52,58,60,102,103,125,127).$$

b) Show the **NAND gate implementation** of the following Boolean Function. [4]

$$F(A, B, C, D) = AB + C(B+A'D) + B'C.$$

- c) Show that  $A \oplus B \oplus C \oplus D = \sum(1,2,4,7,8,11,13,14)$ . [4]

## AHSANULLAH UNIVERSITY OF SCIENCE &amp; TECHNOLOGY

Dept. of Computer Science and Engineering

Year: 2<sup>nd</sup>, Semester: I<sup>st</sup>, Final Examination (Fall 2013)

Course No: CSE 2105

Full Marks: 70

Course Title: Digital Logic Design

Time: 3 Hours

[There are Seven (7) Questions. Answer any Five (5) Questions.]

[Marks allotted are indicated in the margin.]

- Q1.** a) Construct a 4-bit Adder/Subtractor circuit with a select input variable  $v$ ; [5] where the circuit perform addition operation when  $v = 1$  and the circuit perform subtraction operation when  $v = 0$ .

- b) Implement the following four Boolean Functions using three half-adder only:

$$D = A \oplus B \oplus C$$

$$E = A'BC + AB'C$$

$$F = ABC' + (A' + B')C$$

$$G = ABC$$

- c) A combinational circuit is defined by the following four Boolean [5]

Functions:

$$F_1 = x'y' + xyz'$$

$$F_2 = x' + y$$

$$F_3 = xy + x'y$$

$$F_4 = xz + x'z'$$

Implement the combinational circuit by means of the decoder and external gates.

- Q2.** a) Design a combinational circuit that compares two 4-bit numbers,  $A$  and  $B$ , to check if  $A$  is greater than or equal to  $B$ . The circuit has one output line  $x$ , so that,  $x = 1$  if  $A \geq B$  and  $x = 0$  if  $A < B$ . [6]

- b) Design a combinational circuit that generates the 2's complement of a BCD number. [5]

- c) Draw the logic diagram of a 2-to-4 decoder using NOR gates only. [3]

- Q3.** a) Design an asynchronous BCD counter with JK flip-flops and draw its timing diagram with nine timing signals. [6]

- b) Draw the circuit diagram of a JK flip-flop and then, obtain its [5]

characteristics table, characteristics equation and timing diagram.

- c) Design a synchronous 3-bit Up Counter using T flip-flops. [3]

- (Q4.) a) Construct a  $5 \times 32$  decoder with four  $3 \times 8$  decoders/demultiplexers and one  $2 \times 4$  decoder. Use block diagrams. [5]

- b) Implement the following function with a  $8 \times 1$  multiplexer. [5]

$$F(A, B, C, D) = \sum(0, 1, 2, 4, 8, 10, 15).$$

- c) Implement a full-subtractor circuit with a decoder and external gates. [4]

- (Q5.) a) Obtain output expression for an 8-to-3 line Priority Encoder with priorities as follows:  $I_6 > I_0 > I_4 > I_3 > I_2 > I_1 > I_7$ . [5]

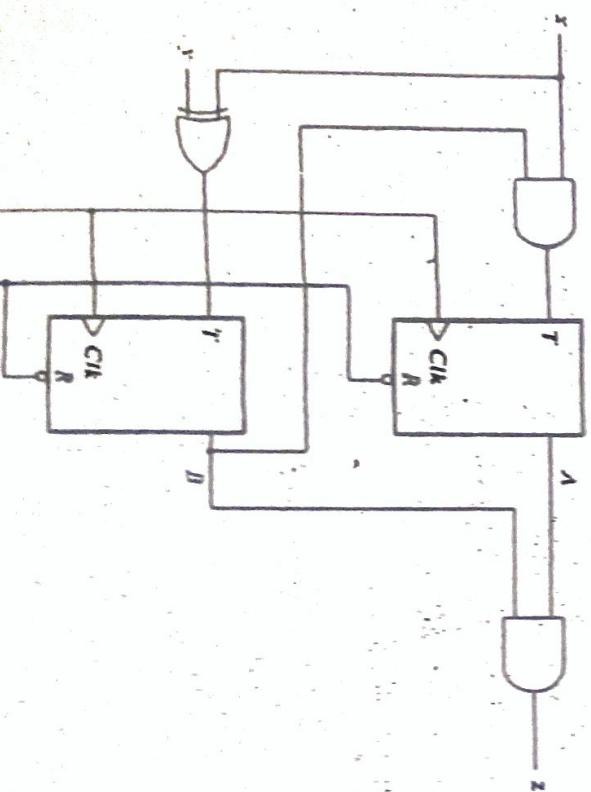
$$\text{Given the Boolean expression } F(x, y, z) = x'y + xyz'$$

- i) Derive an algebraic expression for the complement  $F'$ . [4]

- ii) Show that,  $F \cdot F' = 0$ . [4]

- c) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using even parity bit. [5]

- Q6: a) Derive the state table and draw the timing diagram for 8 clock pulses for the following sequential circuit (Fig. 1). [7]



- Q7**
- b) Construct a 4-bit Johnson counter with ten timing signal. [7]
- b) Show how a JK flip-flop and a T flip-flop can be constructed using a D flip-flop and other logic gates. [4]
- b) Draw a cross coupled circuit using NAND gates only. Derive its characteristics table and show its timing diagram. [4]
- c) Consider the following timing diagram in Fig. 2, assuming that the D and CLK inputs shown are applied to the circuit in Fig. 3, draw waveforms for the  $Q_a$ ,  $Q_b$  and  $Q_c$  output signals. [6]

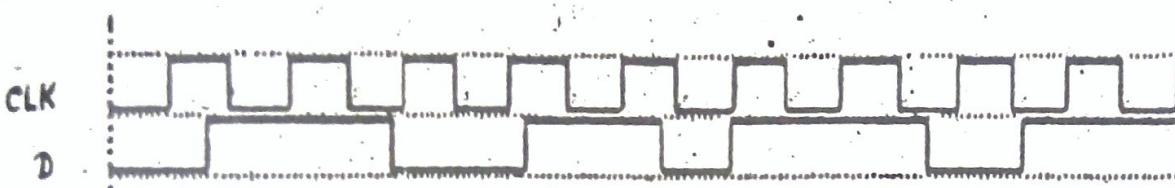


Fig. 2

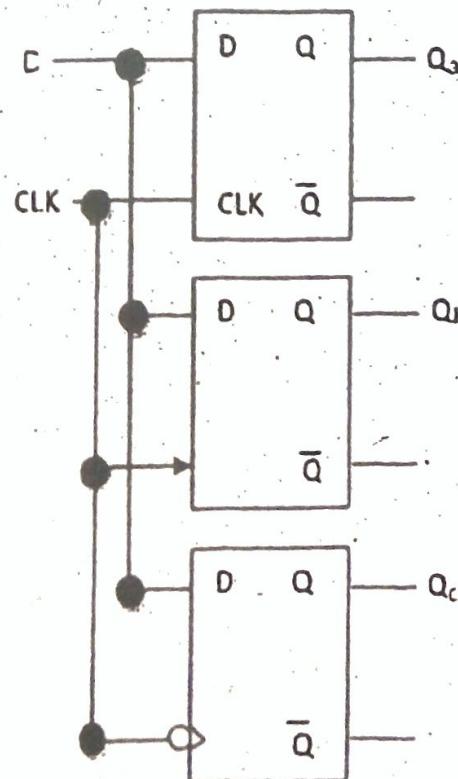


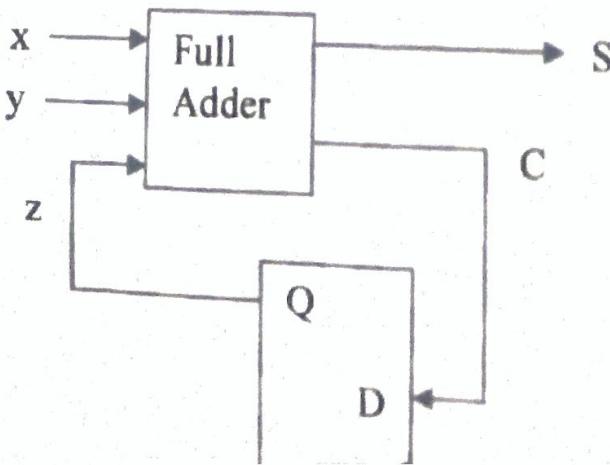
Fig. 3



Course No: CSE 2105  
Full Marks: 70Course Title: Digital Logic Design  
Time: 3 Hours

[There are Seven (7) Questions. Answer any Five (5) Questions.]  
 [Marks allotted are indicated in the margin.]

- Q1. a) Design a combinational circuit to generate and check for odd parity of four bits. [5]
- b) Prove that, NOR and NAND gates are universal gates. [4]
- c) Implement the following function using one multiplexer only, [5]  
 $F(w, x, y, z) = \sum(2, 3, 5, 9, 10, 15).$
- Q2. a) Design a 4-bit binary ripple counter using negative edge triggered  $D$  flip-flops. [5]
- b) Design a 4-bit shift register using  $T$  flip-flops. [5]
- c) Draw the circuit diagram of a  $J-K$  flip-flop. Derive its characteristics table and excitation table. [4]
- Q3. a) Design a counter circuit using  $T$  flip-flops that counts the decimal digit according to the (2 4 2 1) code. [6]
- b) Define the state diagram and the state table for the following sequential circuit. [6]



Q. Define the disadvantage of SR flip-flop.

a) Design a  $2 \times 3$  binary multiplexer circuit using AND gates and full-adders. [5]

b) Design a combinational circuit that converts a 4-bit Binary number to 4-bit Gray code number. [5]

c) Construct a  $4 \times 16$  decoder with two  $3 \times 8$  decoders and one  $1 \times 2$  decoder. Use block diagram. [4]

Q5. a) Draw the circuit diagram of  $T$  flip-flop. Derive its characteristics table and excitation table. [4]

b) Design a counter circuit using J-K flip-flops for the following sequence: 0, 2, 4, 6, 8, 10, 12, 14, 0 and repeat. [5]

c) Design an asynchronous 4-bit Up Counter using  $T$  flip-flops and show its timing diagram. [5]

a) Implement the following Boolean function using NOR gates only, [5]

$$F(2, 3, 4, 7) = 0$$

b) Prove the following expression using Boolean algebra, [5]

$$A \odot B \odot C \odot D = \Sigma(0, 3, 5, 6, 9, 10, 12, 15).$$

c) Construct a  $16 \times 1$  multiplexer with two  $8 \times 1$  and one  $2 \times 1$  multiplexers. Use block diagram. [4]

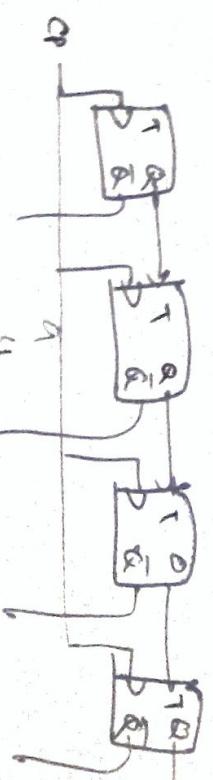
Q7. a) Simplify the Boolean Function  $F$  by means of the Tabulation Method. [6]

$$F(A, B, C, D, E) = \Sigma(5, 7, 11, 15, 17, 20, 28, 30).$$

b) Show that, a full-adder can be converted to a full-subtractor with the addition of one inverter circuit. [5]

c) Implement the following function using NAND gates only. [3]

$$F(A, B, C, D) = \bar{A}CD + \bar{A}C\bar{D} + \bar{B}\bar{C}\bar{D}$$



# AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department of Computer Science and Engineering  
Year: 2<sup>nd</sup>, Semester: 1<sup>st</sup>, Final Examination (Full 2015)

Course No: CSE 2105

Full Marks: 70

Course Title: Digital Logic Design

Time: 3 Hours

[There are Seven (7) Questions. Answer any Five (5) Questions.]

[Marks allotted are indicated in the margin.]

- Q1. a) The Boolean expression,  $F(A, B, C, D) = C + \bar{D}$  is a simplified version of [6] the following Boolean expression:

$$F(A, B, C, D) = B\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{D}(B\odot C) + \bar{A}\bar{C}(B\odot D)$$

Are there any don't care conditions? If so, what are they?

- b) Design a BCD to Excess-4 code converter with a BCD to decimal decoder [5] and four OR gates.

- c) Prove the following expression using Boolean algebra, [3]

$$A\odot\bar{B}C = \Sigma(0, 2, 3, 5).$$

- Q2. a) Design a 3-bit square combinational circuit with one additional output line which detects the odd parity in the squared number. [5]

A combinational circuit is defined by the following two Boolean functions:

$$\begin{aligned} F_1(x, y, z) &= x'y' + xz' \\ F_2(x, y, z) &= x + x'y' \end{aligned}$$

Implement the combinational circuit by means of the decoder and external gates.

- C) Draw the circuit diagram of a  $(4 \times 2)$  priority encoder using NOR gates only with priorities as follows:  $I_2 > I_0 > I_3 > I_1$ . [5]

- Q3. Design a counter circuit using D flip-flops for the following sequence: [5]  
 $0, 8, 12, 14, 15, 7, 3, 1, 0$  and repeat.

- Q4. Design a J-R flip-flop where a J-K flip-flop with an inverter between external input  $K$  and internal input  $K$ . [4]  
(i) Obtain the flip-flop characteristic table.

(ii) Obtain the flip-flop excitation table.

Q

Design a sequential circuit with two  $T$  flip-flops namely  $T_A$ ,  $T_B$  and one input

a. When  $a = 1$ , the state of the circuit remain same. When  $a = 0$ , the circuit

goes through in the following state transitions:

$$00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00$$

Ans.  $\checkmark$

Implement the four Boolean functions listed using three half-adder circuits. [5]

$$D = A \oplus B \oplus C$$

$$E = A'BC + ABC$$

$$F = ABC' + (A' + B')C$$

Left 16

$$G = ABC$$

✓

Design a 4-bit carry look-ahead adder circuit.

Q

Design a combinational circuit that detects an error in the representation of a decimal digit in BCD form.

[5]

Q5. a) What is PLA? Write down the advantages of PLA over ROM. [3]

b) Derive the PLA program table for a combinational circuit that squares a 3-bit number. [6]

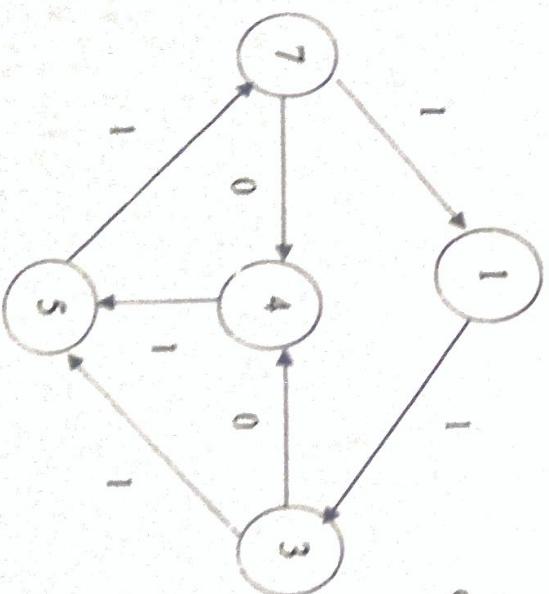
c) Derive the PLA program table for the BCD code to Excess-3 code converter circuit.

[5]

Q6. a) Design an arbitrary counter using  $D$  flip-flops for the following state diagram. [5]



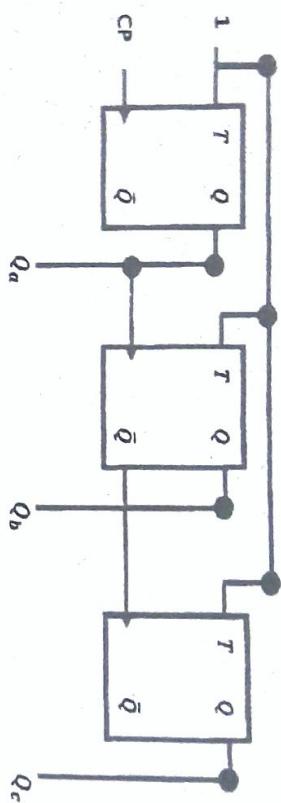
Left 16



Left 16

[4]

- ⑤ Consider the following sequential circuit, where the input of each  $T$  flip-flop is 1 and a positive clock pulse is applied to each flip-flop. Now draw the timing waveforms of the  $Q_a$ ,  $Q_b$  and  $Q_c$  output signals for five clock pulses.



- ⑥ Design a counter circuit using  $J-K$  flip-flops for the following sequence:

0, 1, 3, 7, 6, 4 and repeat.

[5]

Fall '15

(14)

- ⑦ Implement the following function with a multiplexer,

$$F(w, x, y, z) = \sum(0, 2, 4, 10, 14).$$

[5]

- ⑧ Design a decimal adder for two digits represented in the Excess-3 code.

Show that the correction after adding the two digits with a 4-bit binary adder is as follows:

- (i) The output carry is equal to the carry out of the binary adder.

- (ii) If output carry = 1, add 0011.

- (iii) If output carry = 0, add 1101.

Construct the adder with two 4-bit binary adders and other logic gates.

- ⑨ Construct a 4-bit Adder/Subtractor circuit with a select input variable  $s$ , where the circuit performs addition operation when  $s = 0$  and the circuit performs subtraction operation when  $s = 1$ .

(15)

2-2-3  
 $\alpha x^4 x^5 x^2 x^4$   
 $x^5 x^4 x^2$   
 $x^5 x^4 x^2$   
 $x^5 x^4 x^2$   
 $x^5 x^4 x^2$