							MEMORY		
Step	IC	MBR	IBR	MAR	MQ	AC	[300]	[301]	[302]
Initial	0	–	–	–	–	–	3	null	null
1	1	LOAD M(x) 300	ADD M(x)300	300	–	–	3	null	null
2	1	LOAD M(x) 300	ADD M(x)300	300	–	3	3	null	null
3	1	–	–	300	–	6	3	null	null
4	2	STORE M(x) 301	DIV M(x)300	301	–	6	3	null	null
5	2	STORE M(x) 301	DIV M(x)300	301	–	6	3	6	null
6	2	–	–	300	–	2	3	6	null
7	3	LOAD MQ	STORE M(x)302	302	–	2	3	6	null
8	3	LOAD MQ	STORE M(x)302	302	0	0	3	6	null
9	3	LOAD MQ	STORE M(x)302	302	0	0	3	6	0

1. AC was loaded with 3 & updated to 6 after addition
2. AC was then divided by 3 to yield 2, and later reset to 0 after loading from MQ
3. Memory[301] stores 6, and Memory[302] stores 0

INSTRUCTIONS:

1. LOAD M(x) 300, ADD M(x) 300
2. STORE M(x) 301, DIV M(x) 300
3. LOAD MQ, STORE M(x) 302

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300 — 3

301 - null

302 - null