Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Number	COE328
Course Title	Digital Systems - F2022
Semester/Year	Fall 2022
Instructor	Shazzat Hossain
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Lab/Tutorial Report No.	Lab 2 Prelab

Report Title	**Function Implementation and Minimization**

Section No.	11
Group No.	N/A
Submission Date	Sept 28, 2022
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Lab 2: Function Implementation and Minimization

1 Objectives

- Implementation of simple logic functions using NAND gates
- Design, build and test logic functions using the Karnaugh map method

2 Pre-Lab Preparation

Implementation of the simple logic functions with NAND gates

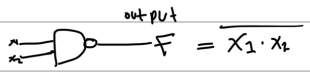
1. Determine 2 ways to implement an inverter with a 2-input NAND gate.
2. Implement a 3-input NAND gate function using 2-input NAND gates only, draw schematics.
3. Implement a 2-input OR function using 2-input NAND gates only, draw schematics.
4. (A) Implement the function $Z = f(A,B) = (A+B)\overline{AB}$ using one 2-input OR gate, one 2-input AND gate and one 2-input NAND gate.
   (B) Implement the same function Z with only NAND gates.
   (C) Make up the truth table for the function. What is the common name of this function?
   (D) Expand and simplify the Boolean equation to express Z as a sum of products. Implement the sum of products using only NAND gates. Note: It is possible to do so with 4 NAND gates and no additional inverters.

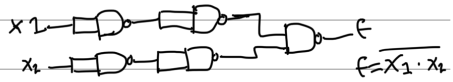
PreLab:

1. Determine 2 ways to implement an inverter with a 2-input NAND gate.

Nand Gate:

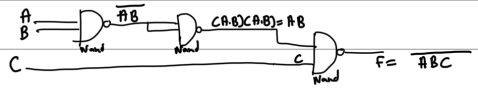
X_1	X_2	F	$\overline{F}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

① 

② 

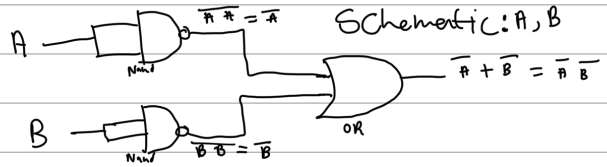
2. Implement a 3-input NAND gate function using 2-input NAND gates only, draw schematics.

Schematic: A, B



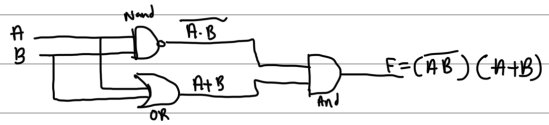
3. Implement a 2-input OR function using 2-input NAND gates only, draw schematics.

Schematic: A, B



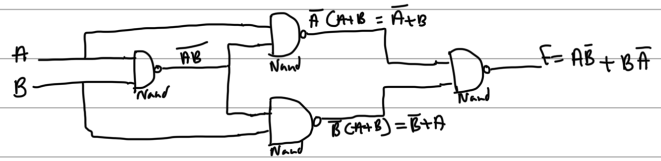
4. (A) Implement the function $Z = f(A,B) = (A+B)AB$ using one 2-input OR gate, one 2-input AND gate and one 2-input NAND gate.

Schematic: A, B



(B) Implement the same function Z with only NAND gates.

Schematic: A, B



$x + \bar{x}y = x + y$

$\bar{x} + xy = \bar{x} + y$

(C) Make up the truth table for the function. What is the common name of this function?

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

Common name of this function is called OR function

(D) Expand and simplify the Boolean equation to express Z as a sum of products. Implement the sum of products using only NAND gates. Note: It is possible to do so with 4 NAND gates and no additional inverters.

$$Z = (A+B)\overline{AB}$$
$$= (A+B)(\overline{A}+\overline{B})$$
$$= \boxed{A\overline{B} + B\overline{A}}$$

$A \cdot \overline{A} = 0$

$B \cdot \overline{B} = 0$