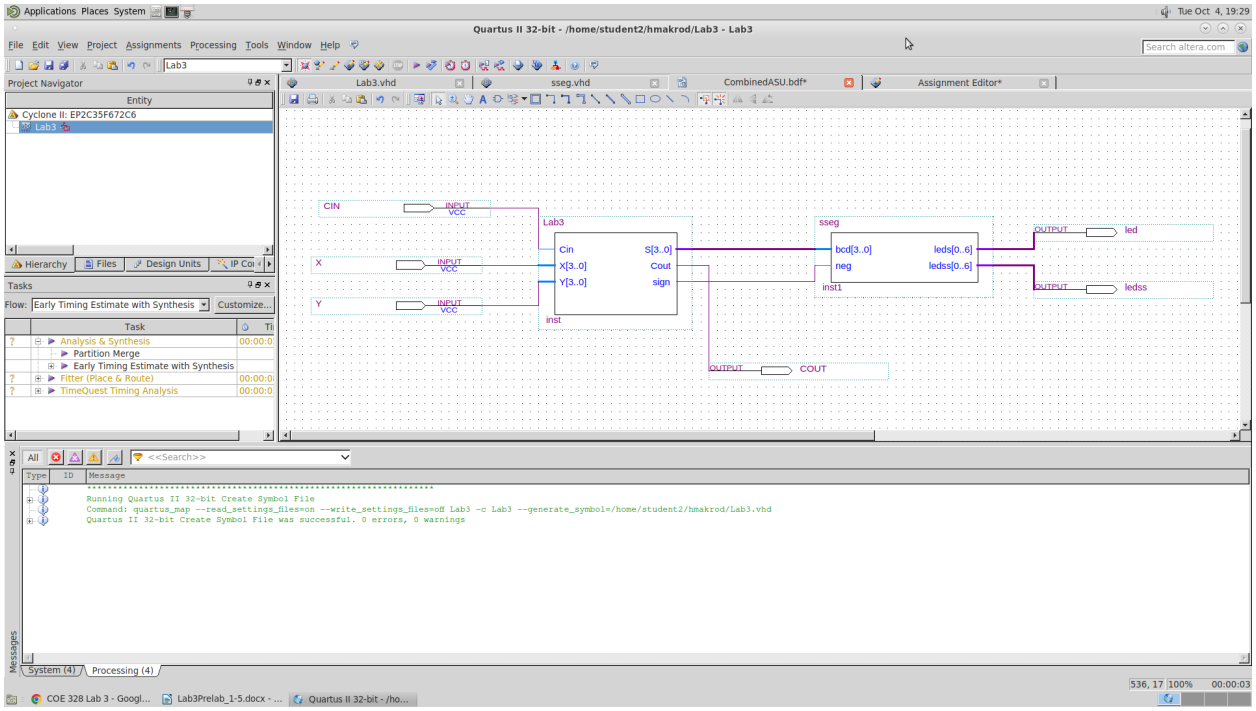
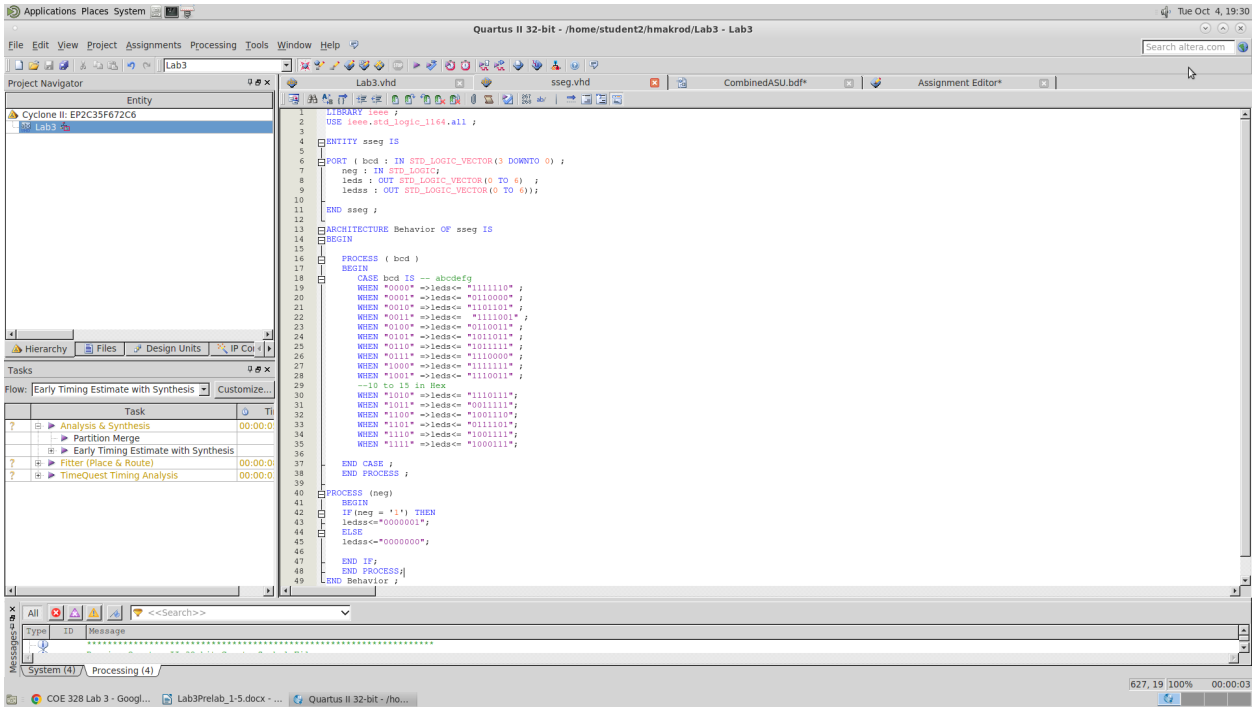
```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;
ENTITY adder4 IS
PORT ( Cin : IN STD_LOGIC ;
X, Y : IN STD_LOGIC_VECTOR(3 DOWNTO 0) ;
S : OUT STD_LOGIC VECTOR(3 DOWNTO 0) ;
Cout, sign : OUT STD_LOGIC ) ;

END adder4 ;
ARCHITECTURE Behavior OF adder4 IS
SIGNAL Sum : STD LOGIC VECTOR(4 DOWNTO 0) ;
BEGIN
Sum <= ('0' & X) + ('0' & Y) + Cin ;
S <= Sum(3 DOWNTO 0) ;
Cout <= Sum(4) ;
sign <= Sum(3);
END Behavior ;
```

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY sseg IS

PORT ( bcd : IN STD_LOGIC_VECTOR(3 DOWNTO 0) ;
        neg : IN STD_LOGIC;
        leds : OUT STD_LOGIC_VECTOR(0 TO 6)  ;
        ledss : OUT STD_LOGIC_VECTOR(0 TO 6));

END sseg ;

ARCHITECTURE Behavior OF sseg IS
BEGIN

        PROCESS ( bcd )
        BEGIN
                CASE bcd IS -- abcdefg
                WHEN "0000" =>leds<= "1111110" ;
                WHEN "0001" =>leds<= "0110000" ;
                WHEN "0010" =>leds<= "1101101" ;
                WHEN "0011" =>leds<=  "1111001" ;
                WHEN "0100" =>leds<= "0110011" ;
                WHEN "0101" =>leds<= "1011011" ;
                WHEN "0110" =>leds<= "1011111" ;
                WHEN "0111" =>leds<= "1110000" ;
                WHEN "1000" =>leds<= "1111111" ;
                WHEN "1001" =>leds<= "1110011" ;
                --10 to 15 in Hex
                WHEN "1010" =>leds<= "1110111";
                WHEN "1011" =>leds<= "0011111";
                WHEN "1100" =>leds<= "1001110";
                WHEN "1101" =>leds<= "0111101";
                WHEN "1110" =>leds<= "1001111";
                WHEN "1111" =>leds<= "1000111";

        END CASE ;
        END PROCESS ;

PROCESS (neg)
        BEGIN
        IF(neg = '1') THEN
        ledss<="0000001";
```

```
        ELSE
        ledss<="0000000";

        END IF;
        END PROCESS
END Behavior ;
```

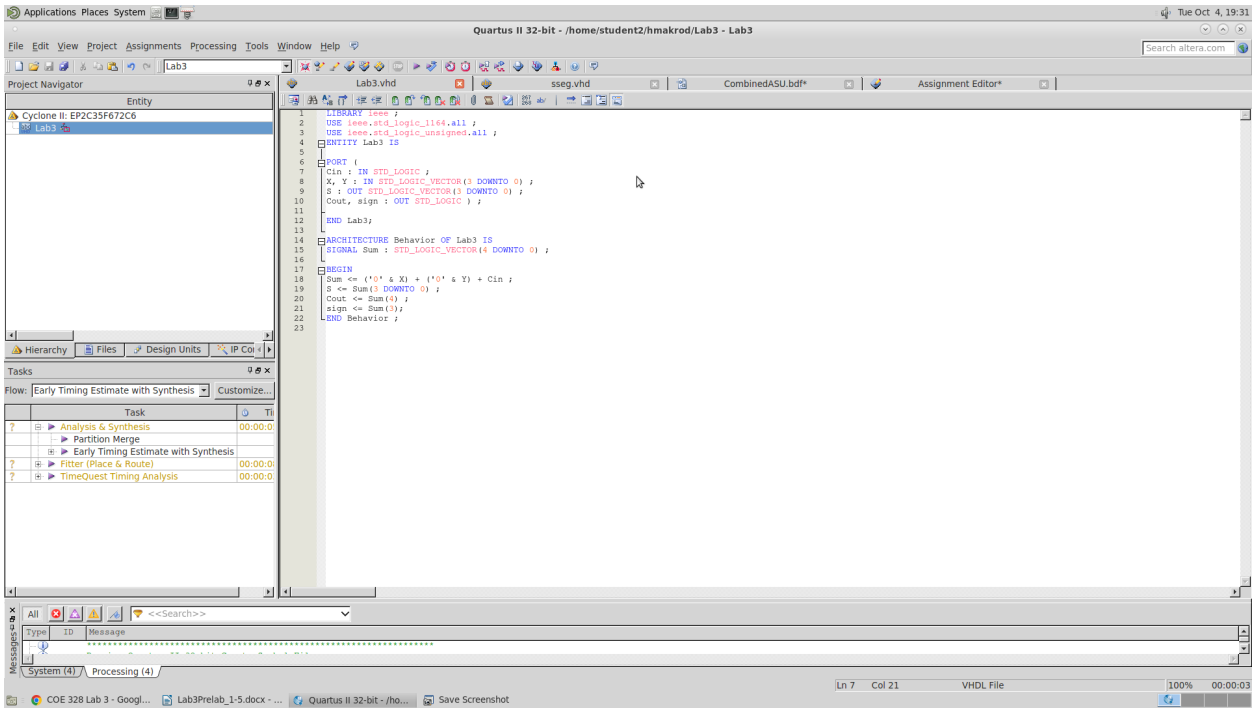



```
LIBRARY ieee ;
```

```
USE ieee.std_logic_1164.all ;

ENTITY sseg IS

PORT ( bcd : IN STD_LOGIC_VECTOR(3 DOWNTO 0) ;
        neg : IN STD_LOGIC;
        leds : OUT STD_LOGIC_VECTOR(0 TO 6)  ;
        ledss : OUT STD_LOGIC_VECTOR(0 TO 6));

END sseg ;

ARCHITECTURE Behavior OF sseg IS
BEGIN

        PROCESS ( bcd )
        BEGIN
                CASE bcd IS -- abcdefg
                WHEN "0000" =>leds<= "1111110" ;
                WHEN "0001" =>leds<= "0110000" ;
                WHEN "0010" =>leds<= "1101101" ;
                WHEN "0011" =>leds<=  "1111001" ;
                WHEN "0100" =>leds<= "0110011" ;
                WHEN "0101" =>leds<= "1011011" ;
                WHEN "0110" =>leds<= "1011111" ;
                WHEN "0111" =>leds<= "1110000" ;
                WHEN "1000" =>leds<= "1111111" ;
                WHEN "1001" =>leds<= "1110011" ;
                --10 to 15 in Hex
                WHEN "1010" =>leds<= "1110111";
                WHEN "1011" =>leds<= "0011111";
                WHEN "1100" =>leds<= "1001110";
                WHEN "1101" =>leds<= "0111101";
                WHEN "1110" =>leds<= "1001111";
                WHEN "1111" =>leds<= "1000111";

        END CASE ;
        END PROCESS ;

PROCESS (neg)
        BEGIN
        IF(neg = '1') THEN
        ledss<="0000001";
        ELSE
        ledss<="0000000";
```

```
        END IF;
        END PROCESS;
END Behavior ;
```




```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_unsigned.all ;
ENTITY Lab3 IS

PORT (
Cin : IN STD_LOGIC ;
X, Y : IN STD_LOGIC_VECTOR(3 DOWNTO 0) ;
S : OUT STD_LOGIC_VECTOR(3 DOWNTO 0) ;
Cout, sign : OUT STD_LOGIC ) ;

END Lab3;

ARCHITECTURE Behavior OF Lab3 IS
SIGNAL Sum : STD_LOGIC_VECTOR(4 DOWNTO 0) ;

BEGIN
Sum <= ('0' & X) + ('0' & Y) + Cin ;
S <= Sum(3 DOWNTO 0) ;
Cout <= Sum(4) ;
sign <= Sum(3);
END Behavior ;
```