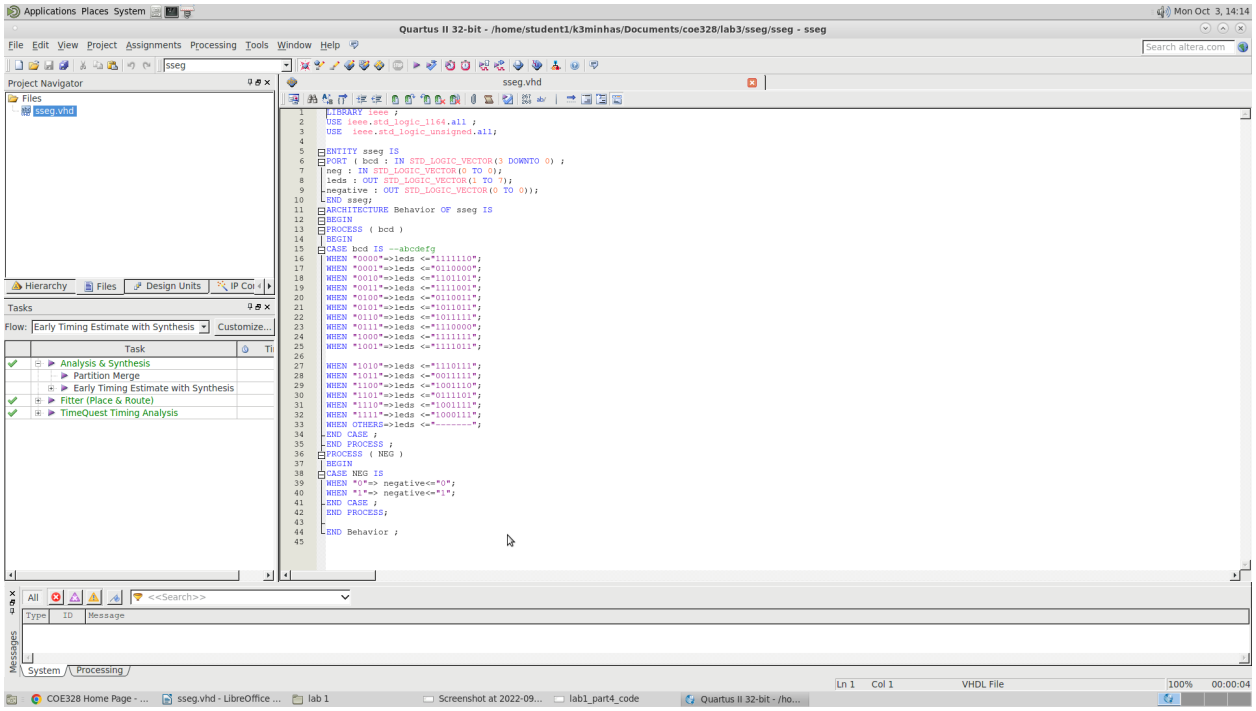
LAB 3:Adder and Subtraction unit

Group Members: Muhammad Abdul Hannan (501096434) & Krisham Singh Minhas ()

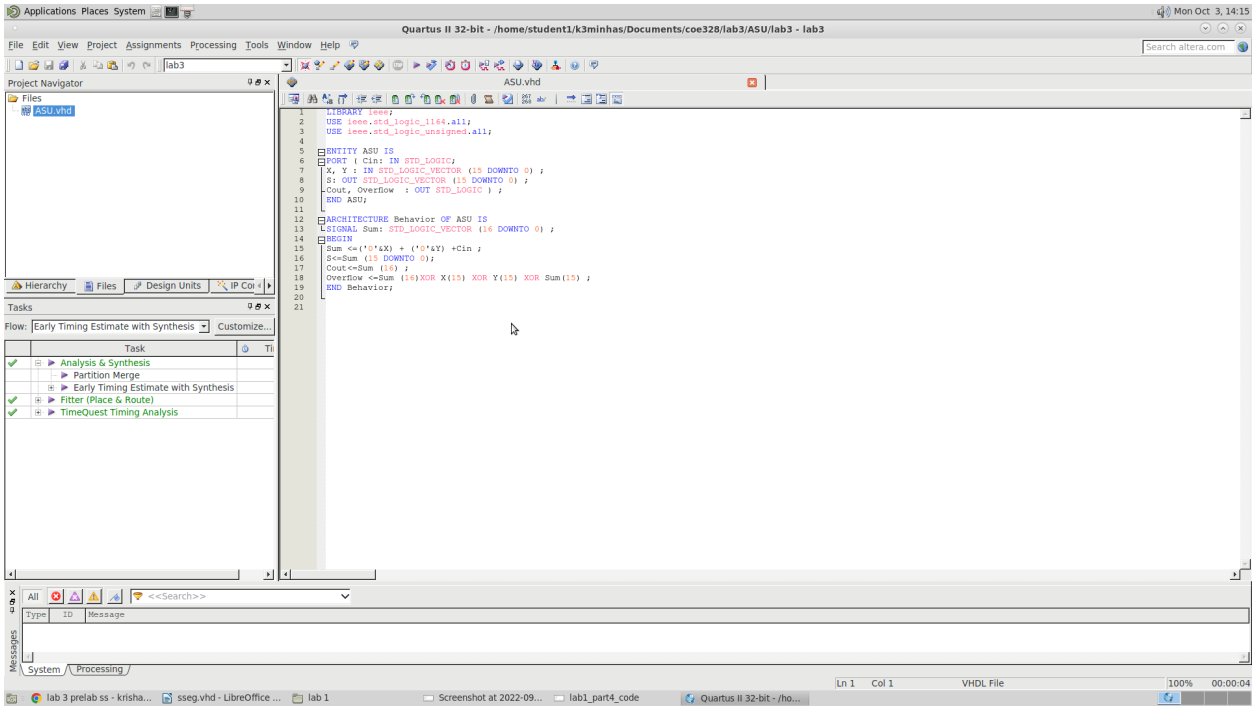
Course: COE328 -08

Instructor: Md Shazzat Hossain

TA: Menglu Li (menglu.li@ryerson.ca)



{SSEG.vhd: VHDL code to represent the sequence 0-F }


Applications Places System
Mon Oct 3, 14:15
Quartus II 32-bit - /home/student1/k3minhas/Documents/coe328/lab3/ASU/lab3 - lab3
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator
Files
ASU.vhd
Hierarchy
Files
Design Units
ASU.vhd
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.all;
3 USE ieee.std_logic_unsigned.all;
4
5 ENTITY ASU IS
6 PORT (Cin: IN STD_LOGIC;
7 X, Y : IN STD_LOGIC_VECTOR (15 DOWNTO 0) ;
8 S: OUT STD_LOGIC_VECTOR (15 DOWNTO 0) ;
9 Cout, Overflow : OUT STD_LOGIC) ;
10 END ASU;
11
12 ARCHITECTURE Behavior OF ASU IS
13 SIGNAL Sum: STD_LOGIC_VECTOR (16 DOWNTO 0) ;
14 BEGIN
15 Sum <='0'&X) + ('0'&Y) +Cin ;
16 S<=Sum (15 DOWNTO 0);
17 Cout<=Sum (16) ;
18 Overflow <=Sum (16)XOR X(15) XOR Y(15) XOR Sum(15) ;
19 END Behavior;
20
21
Tasks
Flow: Early Timing Estimate with Synthesis
Customize...
Task
Analysis & Synthesis
Partition Merge
Early Timing Estimate with Synthesis
Fitter (Place & Route)
TimeQuest Timing Analysis
All
<<Search>>
Type
ID
Message
System
Processing
Messages
Ln 1 Col 1 VHDL File 100% 00:00:04
lab 3 prelab ss - krisha...
sseg.vhd - LibreOffice ...
lab 1
Screenshot at 2022-09...
lab1_part4_code
Quartus II 32-bit - /ho...

{ASU.vhd: }