Ryerson University

Department of Electrical,
Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

ELE 202
Electric Circuit Analysis
LAB COVER PAGE for Part I submission.

Lab #:	2	Lab Title:	Basic concepts, Relationships and Laws of Electrical Circuits.

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Section #:	22
Submission date and time:	Feb 3, 2022, 12:55am
Due date and time:	Feb 3, 2022, 2pm

Document submission for Part I:

- A completed and signed "COVER PAGE – **Part I**" has to be included with your submission. The report will not be graded if the signed cover page is not included.
- Your completed handwritten pages of **Section 4.0** should be scanned (via a scanner or phone images), together with the required MultiSIM images. **Note:** *MultiSIM results must be generated using the Department's licensed version of MultiSIM, and the captured screenshots should show your name (at the center-top) and the timestamp (at the bottom-right corner of your screen).*
- Collate and create a *.pdf* or *.docx* file of the above, and upload it via D2L **any time prior to the start of your scheduled lab**. Upload instructions are provided on D2L.

Zero marks will be assigned for the entire lab if this Part I is not submitted prior to your scheduled lab.

**By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: www.ryerson.ca/senate/current/pol60.pdf.*

3.0 REQUIRED LAB EQUIPMENT & PARTS

- Digital Multimeter (DMM) and Power Supply
- ELE202 Lab Kit:- various components, breadboard, wires and jumpers.

4.0 PRE-LAB: ASSIGNMENT

(a) *I-V* Characteristics of Ohmic Resistor using a simple D.C. Circuit

(i) Assume varying values of the DC source-voltage, **E** applied as shown in **Figure 2.0a.** For each source-voltage value, use Ohm's Law to determine the corresponding value of the current, $\mathbf{I_R}$ when the resistance, **R** is 2.2 kΩ and when it is 3.3 kΩ. Record your theoretical results in **Table 2.0. Use the space below to show your work.**

Pre-Lab workspace

① $I = \frac{V}{R} = \frac{3V}{2.2k\Omega} = 0.0013636A = 1.364mA$

② $I = \frac{V}{R} = \frac{6V}{2.2k\Omega} = 0.002727A = 2.727mA$

③ $I = \frac{V}{R} = \frac{9V}{2.2k\Omega} = 0.0040909A = 4.091mA$

④ $I = \frac{V}{R} = \frac{12V}{2.2k\Omega} = 0.0054545A = 5.455mA$

⑤ $I = \frac{V}{R} = \frac{15V}{2.2k\Omega} = 0.006818A = 6.818mA$

[3 marks]

(ii) Change the resistor to **R** = 3.3kΩ, and repeat **step (i).**

Pre-Lab workspace

① $I = \frac{V}{R} = \frac{3V}{3.3k\Omega} = 0.0009090A = 0.909mA$

② $I = \frac{V}{R} = \frac{6V}{3.3k\Omega} = 0.001818A = 1.818mA$

③ $I = \frac{V}{R} = \frac{9V}{3.3k\Omega} = 0.002727A = 2.727mA$

④ $I = \frac{V}{R} = \frac{12}{3.3k\Omega} = 0.003636A = 3.636mA$

⑤ $I = \frac{V}{R} = \frac{15}{3.3k\Omega} = 0.004545 = 4.545mA$

[3 marks]

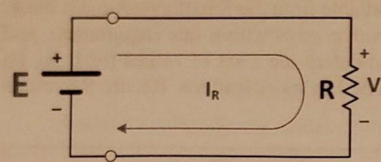


Figure 2.0a: Simple DC Circuit

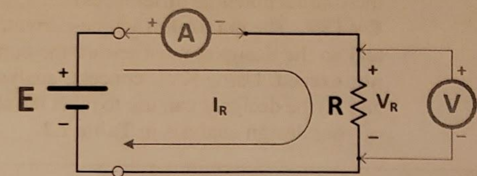


Figure 2.0b: Simple DC Circuit showing Voltmeter & Ammeter connections

R	V_R =>	3V Theory result	6V Theory result	9V Theory result	12V Theory result	15V Theory Result
2.2 kΩ	I_R => (mA)	1.364mA	2.727mA	4.091mA	5.455mA	6.818mA
3.3 kΩ	I_R => (mA)	0.909mA	1.818mA	2.727mA	3.636mA	4.545mA

Table 2.0: Theoretical results of the Simple DC Circuit in Figure 2.0 **[5 marks]**

(b) Series Resistors Circuit - KVL

(i) For the circuit of **Figure 2.1a**, assume the source-voltage, **E = 15V**, $\mathbf{R_1}$ = 3.3 kΩ, $\mathbf{R_2}$ = 2.2 kΩ and $\mathbf{R_3}$ = 1.0 kΩ. Determine the expected current, **I** and the voltages across resistors $\mathbf{R_1}$ (=V_{ab}), $\mathbf{R_2}$ (= V_{bc}) and $\mathbf{R_3}$ (=V_{cd}) for the respective values of resistors shown. Record your theoretical results in **Table 2.1**. Determine the sum $\Sigma V = (V_{ab} + V_{bc} + V_{cd})$ to verify the KVL law.

Pre-Lab workspace

RT = 6.5kΩ IT = 2.308mA VT = 15v
R1 = 3.3kΩ I1 = 2.308mA V1 = 7.615V
R2 = 2.2kΩ I2 = 2.308mA V2 = 5.077V
R3 = 1.0kΩ I3 = 2.308mA V3 = 2.308V

V1 = I1 * R1
= 3.3kΩ X 0.002307
= 7.615V

V2 = I2 x R2
= 2.2kΩ x 0.0023076
= 5.077V

RT = R1 + R2 + R3
= 3.3kΩ + 2.2kΩ + 1.0kΩ
= 6.5kΩ

V3 = I3 x R3
= 1.0kΩ x 0.0023076
= 2.308V

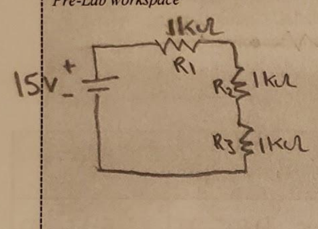
$I = \frac{V}{R} = \frac{15V}{6.5k\Omega}$ = 0.0023076A = 2.308mA

[6 marks]

VT = 7.615 + 5.077 + 2.308
= 15V

(ii) **Design Problem:** Referring to the circuit of **Figure 2.1a**, a designer wishes to create three *equal* potential differences (i.e. $V_{ab}= V_{bc}= V_{cd}$) of **5V** each from a source-voltage, **E = 15V.** The **maximum** source-current, **I** available from the **E** battery-source is **5mA,** and so the designer must ensure the current value stays within this requirement, and **not exceed.** Using KVL concept, analyse and determine a set of values for **I, R_1, R_2** and **R_3** the designer can use to meet the above design specifications. Record the results of your design analysis in **Table 2.2.**

Pre-Lab workspace



$I_T = \frac{V_T}{R_T}$

$= \frac{15V}{3k\Omega}$

$= 5mA$

$V_1 = I_1 \times R1$

$= 5mA \times 1.0k\Omega$

$= 5V$

$V_2 = I_1 \times R1$

$= 5mA \times 1.0k\Omega$

$= 5V$

$V_3 = I_1 \times R1$

$= 5mA \times 1.0k\Omega$

$= 5V$

$RT = 3.0k\Omega$ $IT = 5mA$ $VT = 15V$

$R1 = 1.0k\Omega$ $I_1 = 5mA$ $V_1 = 5V$

$R2 = 1.0k\Omega$ $I_2 = 5mA$ $V_2 = 5V$

$R3 = 1.0k\Omega$ $I_3 = 5mA$ $V_3 = 5V$

$VT = 5V + 5V + 5V$

$= 15V$

[6 marks]

$RT = R1 + R2 + R3$

$= 1 + 1 + 1$

$= 3k\Omega$

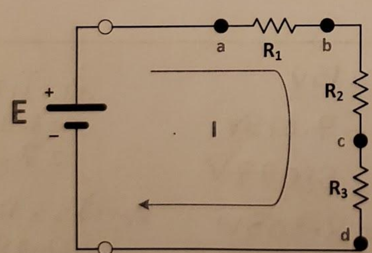


Figure 2.1a: KVL Series Circuit

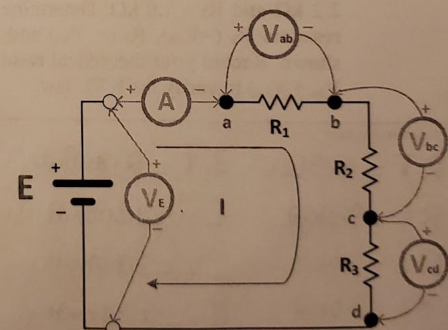


Figure 2.1b: KVL Series Circuit showing Voltmeter & Ammeter connections

V_E	I (mA)	V_{ab} (Volts)	V_{bc} (Volts)	V_{cd} (Volts)	$\Sigma V = (V_{ab} + V_{bc} + V_{cd})$
	Theory result	Theory result	Theory result	Theory result	Theory result
15V	2.308mA	7.615V	5.077V	2.308V	15V

Table 2.1: Theoretical results of the Series Circuit in Figure 2.1a **[2.5 marks]**

Design values => R_1 = 1kΩ ? R_2 = 1kΩ ? R_3 = 1kΩ ?

V_E	I (mA)	V_{ab} (Volts)	V_{bc} (Volts)	V_{cd} (Volts)
	Theory result	Theory result	Theory result	Theory result
15V	5mA	5V	5V	5V

Table 2.2: Theoretical results of the ***re-designed*** Series Circuit in Figure 2.1a **[2.5 marks]**

(c) Parallel Resistors Circuit - KCL

(i) For the circuit of **Figure 2.2a**, assume the source-voltage, **E = 15V**, $\mathbf{R_1}$ = 3.3 kΩ, $\mathbf{R_2}$ = 2.2 kΩ and $\mathbf{R_3}$ = 1.0 kΩ. Determine the expected currents **I**, $\mathbf{I_1}$, $\mathbf{I_2}$ and $\mathbf{I_3}$ as shown in **Figure 2.2a**. Record your theoretical results in **Table 2.3**. Determine the sum $\Sigma I = (I_1 + I_2 + I_3)$ to verify the KCL law.

Pre-Lab workspace

$R_T = 568.966\Omega$ $V_T = 15V$ $I_T = 26.364mA$ $I_T = \frac{V_T}{R_T}$

$R_1 = 3.3k\Omega$ $V_1 = 15V$ $I_1 = 4.545mA$ $= \frac{15V}{568.966\Omega}$

$R_2 = 2.2k\Omega$ $V_2 = 15V$ $I_2 = 6.818mA$ $= 0.026364A$

$R_3 = 1.0k\Omega$ $V_3 = 15V$ $I_3 = 15mA$ $= 26.364mA$

$R_T = 1/R_1 + 1/R_2 + 1/R_3$
$= 1/3.3k\Omega + 1/2.2k\Omega + 1/1.0k\Omega$
$= 1/0.001757575758$
$= 568.966\Omega$

$I_1 = \frac{V_1}{R_1} = \frac{15V}{3.3k\Omega} = 4.545mA$

$I_2 = \frac{V_2}{R_2} = \frac{15V}{2.2k\Omega} = 6.818mA$

$I_3 = \frac{V_3}{R_3} = \frac{15}{1.0k\Omega} = 15mA$

[6 marks]

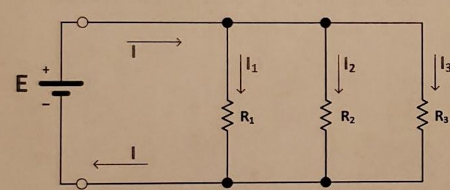


Figure 2.2a: KCL Parallel Circuit

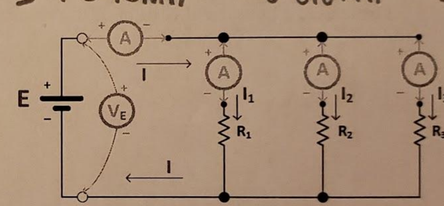


Figure 2.2b: KCL Parallel Circuit with Ammeter & Voltmeter connections

V_E	I (mA) Theory result	I_1 (mA) Theory result	I_2 (mA) Theory result	I_3 (mA) Theory result	$\Sigma I = (I_1 + I_2 + I_3)$ Theory result
15V	26.364mA	4.545mA	6.818mA	15mA	26.363 mA

Table 2.3: Theoretical results of the Parallel Circuit in Figure 2.2a **[6 marks]**