Faculty of Science
Department of Physics
Laboratory Report Cover Page

Course Number	PCS224
Course Title	Physics: Solid State Physics
Semester/Year	Fall Semester 2023
Instructor	Carina Rebello
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Lab/Tutorial Report No.	Lab Experiment #5

Report Title	Lab 5 - MOSFET

Section No.	03
Group No.	44
Submission Date	Nov. 22 12:00 pm
Due Date	Nov. 22 3:00 pm

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Appendices

Introduction

This laboratory session revisits familiar properties, skills, and attributes previously explored in Lab 3. However, the primary focus now rests on delving deeper into the intricacies of a crucial PN semiconductor junction device: the MOSFET, or metal-oxide-semiconductor field-effect transistor. Distinguished by its low power switching capabilities, MOSFETs stand out among common transistors, offering significant advantages in memory and computing applications. This lab rigorously examines the specific characteristics of these transistors, leveraging measured data points gathered across diverse conditions to illuminate their operational intricacies.

Theory

The laboratory materials necessary for this experiment were supplied within the assigned lab rooms. They comprised a MOSFET transistor, an Arduino, 2 Adafruit MCP4745 12-bit 5V DAC breakout boards, an Adafruit INA219 DC High-Side Current Sensor breakout board, an MCP4002 dual op-amp, a TIP41C BJT transistor, an external power supply, a 9V battery, and several wires. To commence, the construction of the breadboard mirrored the provided image in the lab manual, ensuring accurate placement of transistors and wires. Subsequently, adaptations were made to the Arduino code to suit the specific data requirements. In the initial phase of the lab, the gate voltage underwent settings at three distinct values within the range of 0 to 5 volts. Data points were captured using the Arduino app and stored in a spreadsheet for subsequent analysis. Transitioning to the second segment, code modifications were applied to interchange Vgs and Vds, with a predetermined value set for Vds.

Procedure

The upbringing and fabrication of the PN-junctions have led to more new subsequent ‘active’ semiconductor devices. One of the more important devices which were fabricated is called the “metal-oxide-semiconductor field effect transistor” also known as MOSFET. The MOSFET semiconductor exhibits extremely low power switching capabilities when compared to alternative transistors. On the surface of the MOSFET semiconductor, there is a layer of insulation in SiO2, in the case of Silicone substrates. The voltage applied to the gate of the MOSFET controls the flow of current between the source and the drain by depleting or introducing charge carriers in the substrate located under the gate.

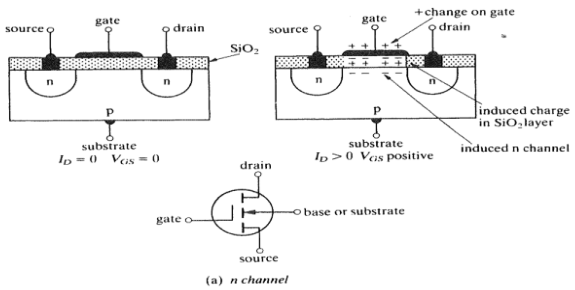


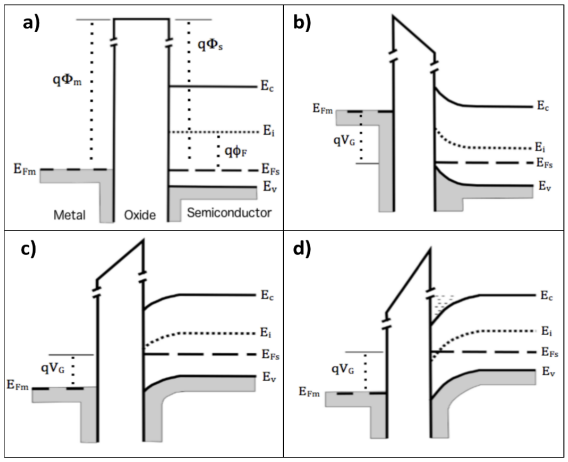
Figure 1: Physical structure of an enhancement mode

In a MOSFET semiconductor, when the Vg is 0 volts, the semiconductor Fermi-levels and the metal align. The semiconductor Fermi-level is $q\phi F$ EV below its intrinsic level of E. It also indicates how strong a p-type substrate is as we can recall the formula on the concentration of majority carriers in a doped p-type semiconductor.

$$P = N_{\alpha} \frac{E_F - E_V}{KT}$$

When the Vg is less than 0 volts applied to a gate, the Fermi-level of the metal increases by qVg. This causes negative charges to be deposited at the gate, attracting additional holes to the semiconductor interface. The semiconductor is known to be in an accumulation state, where the capacitance is given by the following equation.

$$C_{ox} \frac{\epsilon_{ox}}{d_o x}$$



Where ϵ_{ox} is the permittivity of the insulator layer and $d_o x$ is the thickness of the insulator. When the Vg is greater than 0 volts, the redistribution of carrier states causes the band of the semiconductor to bend near the interface just like the Fermi-level and Ei increases separation.

a) Flat band, Vg = 0V
b) Accumulation sate, Vg < 0V
c) Depletion, Vg > 0V
d) Inversion, Vg >> 0V

Figure 2: Ideal MOS under various voltage conditions

Positive charges accumulate at the gate as a result of Vg > 0 volts, resulting in a depelation state in the p-type semiconductor near the oxide-semiconductor interface. The width which is analogous to the depletion region of the PN junction is,

$$W = \left[\frac{2\epsilon_s(\phi_s)}{qN_a}\right]^{\frac{1}{2}}$$

Where ϕ is the potential difference across the depletion region. Due to this, the capacitance becomes into a series combination of the oxide capacitance, $C_d = \frac{\epsilon_s}{W}$. As Vg becomes larger, Ef eventually becomes greater than Ei. In this case, the semiconductor region near the oxide interface becomes "inverted," which means that the conductivity band carrier states are filled with minority electrons, forming an n-channel.The semiconductor depletion layer is at its maximum, while the device's total capacitance is at its lowest. This can be displayed as,

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d}$$

In a non-saturation region, the drain current in a MOSFET semiconductor can be expressed by the following equation.

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS} - V^2_{DS}]$$

$$K_n = \frac{W\mu_n C_{ox}}{2L}$$

Where K_n is referred to as the trans condition parameter. In the situation where is n V_{DS} is small, the drain can be approximated by

$$I_D = K_n[2(V_{GS} - V_{TN})V_{DS}]$$

This equation can be used to determine V_T and K_n when a small V_{DS} is applied. In a saturated region, the drain current can be expressed as,

$$I_D = K_n[V_{GS} - V_{TN}]^2$$

$$K_n = \frac{W\mu_n C_{ox}}{2L}$$

This equation can be used to determine V_T and K_n when a large V_{DS} is applied. This equation assumes that the output impedance is infinite or that the output current I_D does not change as V_{DS} increases. The transconductance gain is another quantity used in this lab which is defined from the following equation.

$$g_{fs} = \frac{\partial I_{DS}}{\partial V_{GS}}$$

Results and Calculations

Vds (V)	Id (mA)
0	0.2
1	0.5
2	1.1
3	2.2
4	3.4
6	6.8
7	8.1
9	9.4
11	10.8
12	11.9
14	13.1
15	14.5
18	15.9
19	17.1
20	18.2
21	18.5
22	19.3
23	19.9
24	20.3
25	20.9
26	21.9
0	0.1
0	-0.1
0	-0.1

Table 1: V_{DS} vs I_D for V_{GS}=3V

Vds (V)	Id (mA)
0	0.3
1	0.9
2	1.3
3	2.9
4	4.2
6	6.9
7	8.1
9	9.5
11	11
12	12.1
14	13.6
15	14.9
18	16.4
19	17.2
20	18.9
21	19.8
22	20
23	20.7
24	21.9
25	22
0	-0.1
0	0
0	-0.1

Table 2: V_{DS} vs I_D for V_{GS}=3.5V

Vds (V)	Id (mA)
0	0.2
1	0.6
2	1.4
3	3.1
4	4.7
6	7.1
7	8.3
9	9.6
11	10.8
12	12.3
14	13.6
15	15.1
18	16.4
19	18.4
20	19.6
21	20.2
22	20.4
23	21.4
24	22
0	0.2
0	0
0	0

Table 3: V_{DS} vs I_D for V_{GS}=4V

Vds (V)	Id (mA)
0	0.2
1	0.8
2	1.5
3	3.4
4	4.9
6	7.5
7	8.6
9	10
11	11.2
12	12.5
14	13.9
15	15.4
18	16.6
19	18.1
20	19.1
21	19.6
22	20.5
23	22
0	0
0	0.3
0	0.4

Table 4: V_{DS} vs I_D for V_{GS}=4.5V

Vds (V)	Id (mA)
0	0.3
1	1
2	2
3	5
4	7.5
6	10
7	11.5
9	12.7
11	14
12	15.6
14	16.7
15	18
18	18.5
19	19.4
20	19.8
21	21
22	21.9
0	0.1
0	0.1
0	0

Table 5: V_{DS} vs I_D for V_{GS}=5V

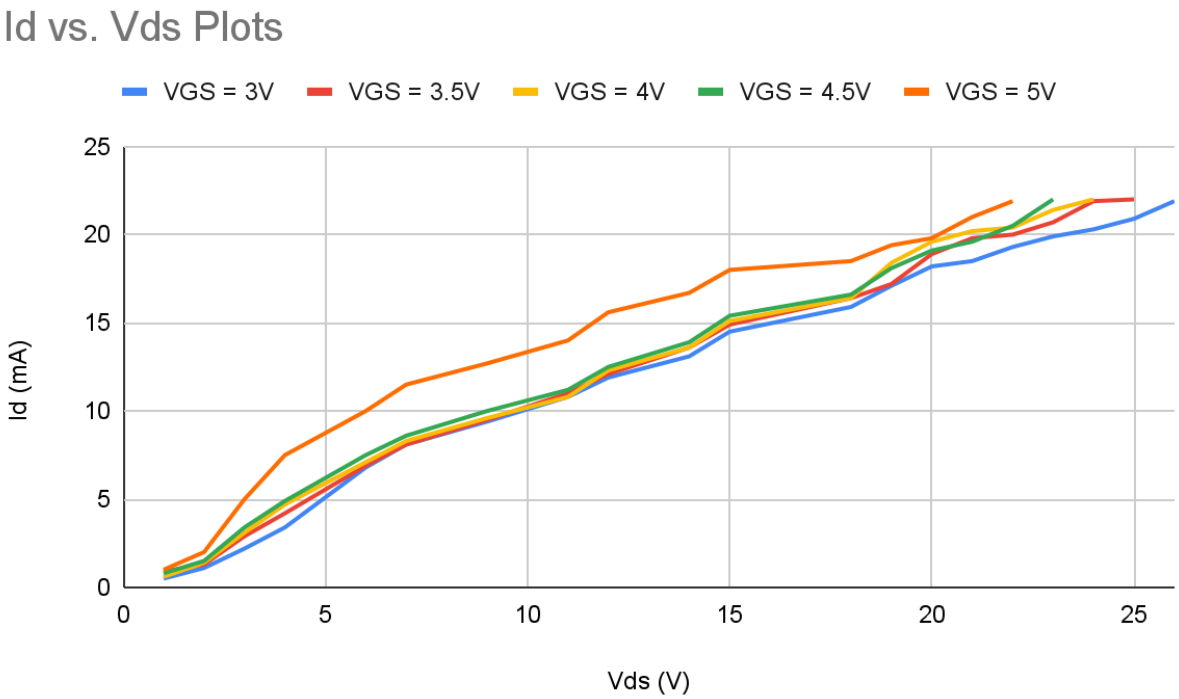


Figure 3: Plot of I_D vs V_{DS} for different V_{GS} values

Looking at our graph, we can see that as we increase the gate voltage, the drain voltage increases for every value of the drain current. Therefore, our MOSFET is in saturation mode. We can also see that the threshold voltage for each value of V_{GS} is almost the same, at around 0.45V.

Vgs (V)	Id (mA)
0	0
0.01	0
0.02	0
0.04	0
0.05	0
0.06	0
0.07	0
0.09	0
0.11	0
0.12	0
0.14	0
0.15	0
0.17	0
0.19	0
0.2	0
0.22	0
0.24	0
0.25	0
0.26	0
0.28	0
0.3	0
0.32	0
0.34	0
0.35	0
0.36	0
0.38	0
0.4	0
0.42	0
0.44	0
0.46	0
0.47	0
0.48	0
0.5	0
0.52	0

0.54	0
0.56	0
0.57	0
0.59	0
0.61	0
0.63	0
0.64	0
0.66	0
0.68	0
0.69	0
0.71	0
0.73	0
0.75	0
0.77	0
0.78	0
0.8	0
0.82	0
0.84	0
0.86	0.01
0.88	0.1
0.89	0.21
0.9	0.43
0.92	0.87
0.94	10
0.96	20
0.98	30
1	70
1.01	80
1.03	100
1.05	149
1.07	198
1.09	238
1.11	290
1.14	339
1.16	380

1.18	446
1.19	535
1.21	599
1.24	667
1.25	689
1.27	723
1.29	732
1.31	739
1.33	742
1.35	749
1.36	749
1.38	750
1.39	749
1.42	750
1.44	751
1.46	754
1.47	754
1.49	754
1.51	755
1.52	755
1.55	754
1.56	754
1.58	755
1.6	754
1.62	755
1.64	755
1.66	755
1.67	754
1.7	755
1.72	756
1.73	755
1.76	756
1.77	755
1.8	756
1.81	756

1.83	755
1.85	756
1.87	756
1.89	757
1.91	756
1.93	756
1.94	757
1.96	756
1.98	756
2	757
2.02	756
2.04	757
2.07	756
2.08	756
2.1	756
2.12	757
2.14	757
2.16	758
2.18	758
2.21	757
2.22	758
2.24	758
2.26	759
2.28	759
2.31	758
2.33	759
2.35	758
2.36	759
2.38	758
2.41	759
2.43	758
2.45	758
2.47	759
2.49	758
2.5	759

2.53	759
2.55	759
2.57	760
2.59	759
2.6	760
2.62	760
2.63	759
2.65	760
2.66	759
2.67	759
2.67	760
2.68	760
2.7	760
0	0.2
0	0.3
0	0.3
0	0

Table 6: V_{GS} vs I_D for V_{DS}=5V

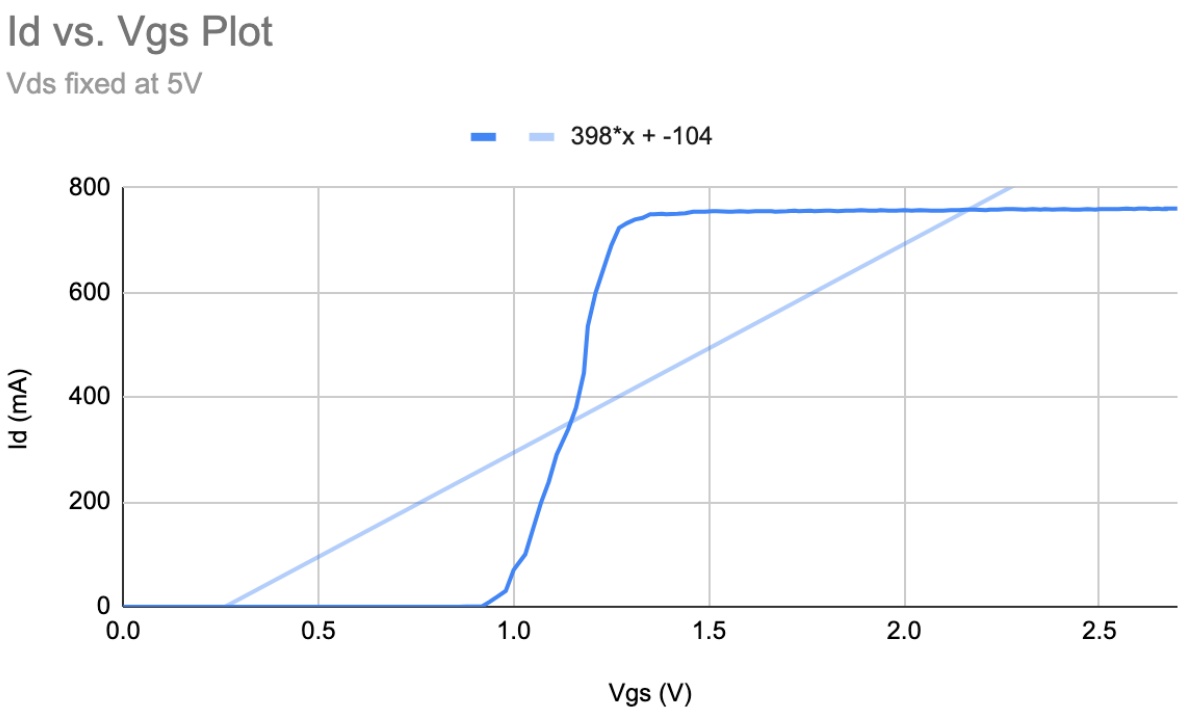


Figure 4: Plot of I_D vs V_{GS} for different V_{DS} = 5V

V_t = 1.0V Transconductance (g_{fs}) = slope = 398 mA/V

$$\%\ error\ of\ V_t = \left|\frac{measured-accepted}{accepted}\right| \times 100 = \left|\frac{1.0V-1.05V}{1.05V}\right| \times 100 = 4.76\%$$

$$\%\ error\ of\ g_{fs} = \left|\frac{measured-accepted}{accepted}\right| \times 100 = \left|\frac{0.398-1.0}{1.0}\right| \times 100 = 60\%$$

Discussion

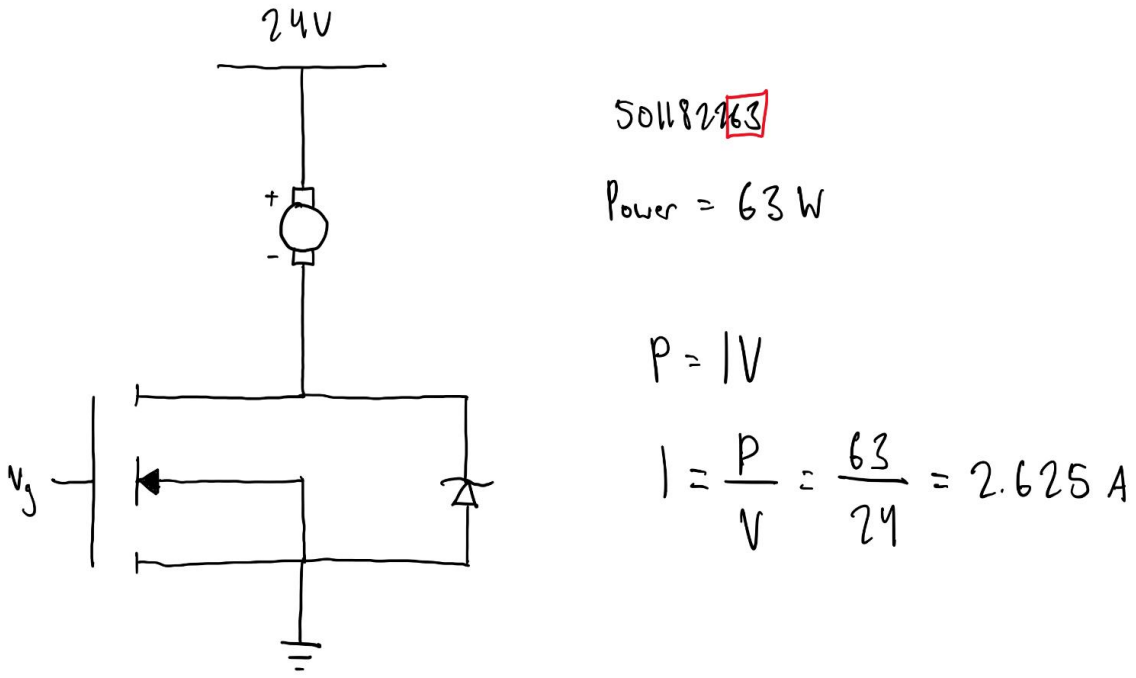


Figure 5: Model MOSFET Switch

The most appropriate value of VGS from our graph is 3V. Since the current is grounded, the source will contain maximum power (55W). The MOSFET will not survive since the power diode will not allow current to flow in the opposite direction.

Conclusions

In this lab, we observed the relationship between the drain voltage and the drain current and how it changed as the gate voltage increased. We discovered that as we increased the gate voltage, the drain voltage also increased, meaning that our MOSFET was in saturation mode. Then we observed the relationship between the gate voltage and drain current as a fixed drain voltage and determined the threshold voltage and transconductance from the graph. We compared our values to a datasheet found online and got an acceptable percent error for the threshold voltage, but a larger one for the transconductance.

References

W. Moebs, S. J. Ling, and J. Sanny, "university physics volume 1," *OpenStax*, 19-Sep-2016. [Online]. Available: https://openstax.org/books/university-physics-volume-1.

Figure 6: Data sheet for 2N7000 MOSFET Transistor
http://www.datasheet.es/PDF/73031/2N7000-pdf.html#google_vignette

2N7000

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS(1) (continued)					
On–State Drain Current (V_{GS} = 4.5 Vdc, V_{DS} = 10 Vdc)		$I_{d(on)}$	75	—	mAdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 200 mAdc)		g_{fs}	100	—	μmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5.0	
SWITCHING CHARACTERISTICS(1)					
Turn–On Delay Time	(V_{DD} = 15 V, I_D = 500 mA, R_G = 25 Ω, R_L = 30 Ω, V_{gen} = 10 V)	t_{on}	—	10	ns
Turn–Off Delay Time		t_{off}	—	10	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

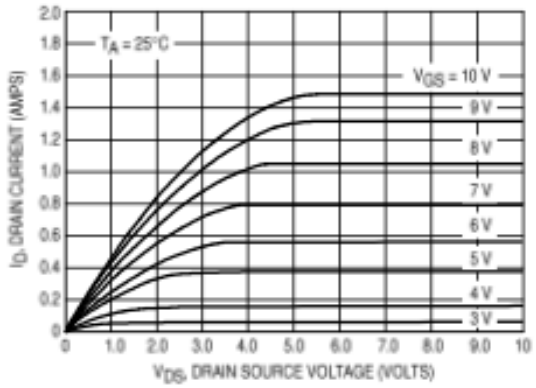


Figure 1. Ohmic Region

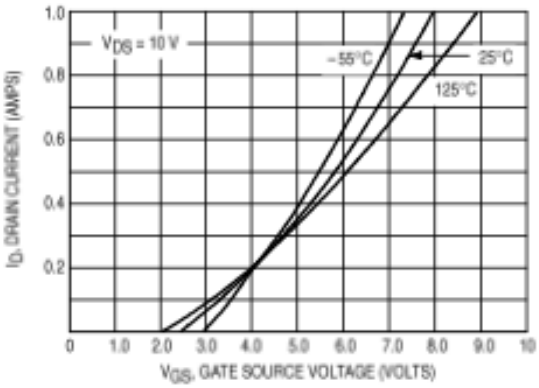


Figure 2. Transfer Characteristics

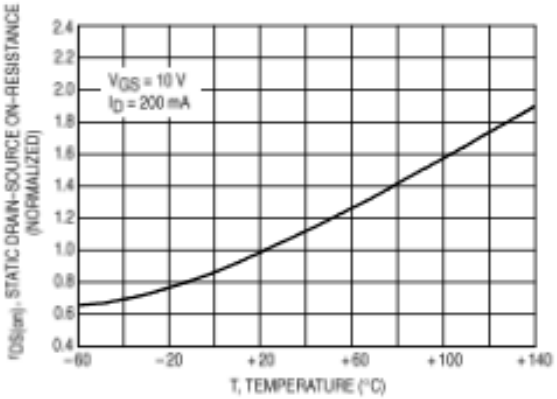


Figure 3. Temperature versus Static Drain–Source On–Resistance

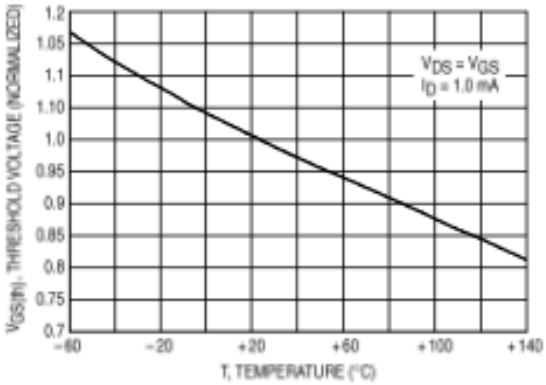


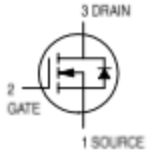
Figure 4. Temperature versus Gate Threshold Voltage

TRANSYS ELECTRONICS LIMITED

2N7000

FET Transistor

N–Channel — Enhancement



TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \leq 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 200 500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16" from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μAdc)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 Vdc, V_{GS} = 0) (V_{DS} = 48 Vdc, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1.0 1.0	 μAdc mAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	−10	nAdc
ON CHARACTERISTICS(1)				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc)	$V_{GS(th)}$	0.8	3.0	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 75 mAdc)	$r_{DS(on)}$	 — —	 5.0 6.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 75 mAdc)	$V_{DS(on)}$	 — —	 2.5 0.45	Vdc

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

```
 // Call libraries required for external breakout boards and communications.
#include <Wire.h>
#include <SPI.h>
#include <Adafruit_MCP4725.h> // DAC library
#include <Adafruit_INA219.h> // INA219 current sensor library

// Declare a current sensor object.
Adafruit_INA219 ina219; // Commands like ina219.getCurrent_mA() will read the current.

// Declare our voltage supply objects.
Adafruit_MCP4725 dac_vds;
Adafruit_MCP4725 dac_vgs;
#define DAC_RESOLUTION (9) // Set this value to 9, 8, 7, 6 or 5 to adjust the resolution.

// Declare some useful variables.
int stepFunction = 0; // Will allow us to increment VDS or VGS as desired.

void setup(void) {
   Serial.begin(9600); // Initiates serial communication, so we can send our data to
                       // our computer.
   // Initialize the INA219 sensor (current sensor).
   ina219.begin();
   // Initialize our DAC breakout boards.
   dac_vds.begin(0x62); // 0x62 sets the hex address of dac_vds
                        // so the arduino addresses the correct DAC.
   dac_vgs.begin(0x63);
}

void loop() {

// Set the Drain voltage, VDS.
// Since the DAC provides 12-bit resolution, the command
// dac_vgs.setVoltage(0, false) sets the output voltage to 0V and
// dac_vgs.setVoltage(4095, false) sets the output voltage to 5V.
// Set your desired voltage by selecting a linear range from 0 to 4095.
float VDS = 5; // Fix VDS voltage at 5V
dac_vgs.setVoltage((VGS/5.0)*4095, false);

// Print Gate voltage to serial port.
```

```
  Serial.print("DRAIN VOLTAGE VDS (V) = " );
  Serial.println(VDS);

// Print table headers to serial port.
  Serial.print("VGS");
  Serial.print("  ");
  Serial.println("ID");

// Sweep VGS from 0 to 5V (approximately... may be lower due to BJT stage).
// Question: If we increase DAC output by “i+=20” what is the corresponding
// change in voltage?

for (int i=0; i<4096;i+=20) {
    dac_vds.setVoltage(i, false);
    delay(5); // Delay for 5ms to stabilize circuit.

    // Read VGS and ID at/across transistor.
    Serial.print(ina219.getBusVoltage_V());
    Serial.print("  ");
    Serial.println(ina219.getCurrent_mA());

    // To prevent overheating from excessive current we shut down VGS for a few ms.
    // We are effectively pulsing the transistor to ensure we don’t exceed
    // Pmax rating.
    dac_vds.setVoltage(0, false); // Set VGS to 0V to allow cooling.
    delay(10); // Delay 10ms to allow MOSFET to cool.
}
delay(10000); // Delay 10s to allow BJT to cool between cycles
}
```