Course Name: Information and Communication Technologies Lab Code: CEN1005
LAB # 9: Implementation of Logic gates in Electronic Workbench

Department	Registration Number/Name	Semester/Section
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Objective:

- To demonstrate the input and output relationship of 2 input AND, OR, NOT, NAND, NOR,XOR gates.
- To implement these logic gates in an electronic workbench.
- To write observations.

Lab Tasks:

1. Make a truth table for each of the logic gate given above and fill it with all possible combinations.

AND

A	B	F (Output)
0	0	**0**
0	1	**0**
1	0	**0**
1	1	**1**

OR

A	B	F (Output)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

NOT

A	F (Output)
0	**1**
1	**0**

NAND

A	B	F (Output)
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

NOR

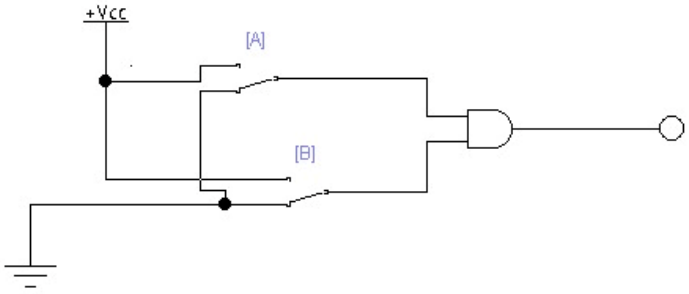
A	B	F (Output)
0	0	**1**
0	1	**0**
1	0	**0**
1	1	**0**

XOR

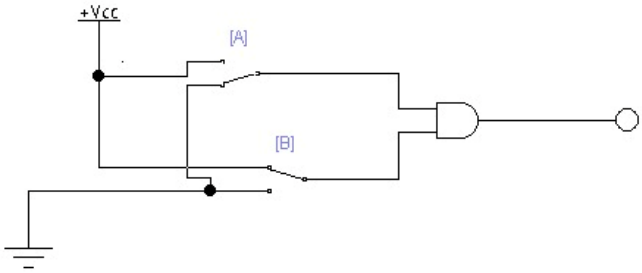
A	B	F (Output)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

2.Implement all the above, give logic gates on electronic workbench and verify your output by giving all possible combinations. Insert the output screenshots in your lab reports.

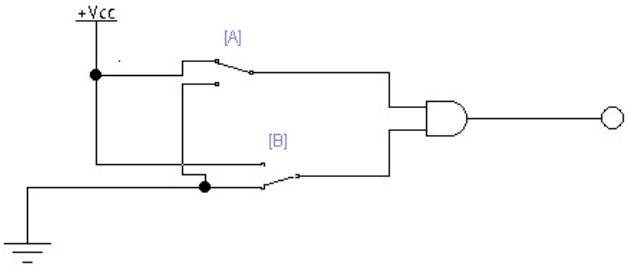
AND GATE:



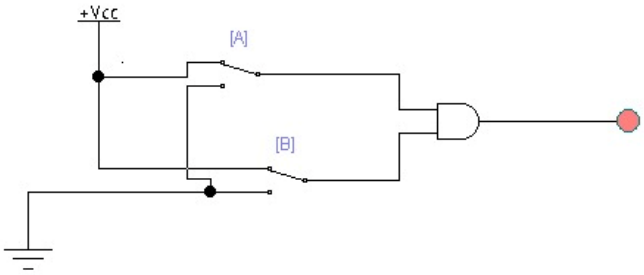
A	B	Output
0	0	0



A	B	Output
0	1	0

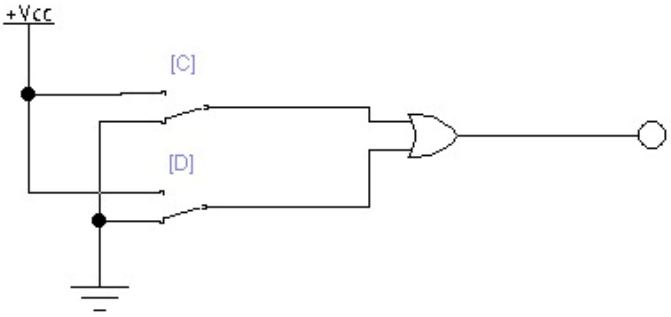


A	B	Output
1	0	0

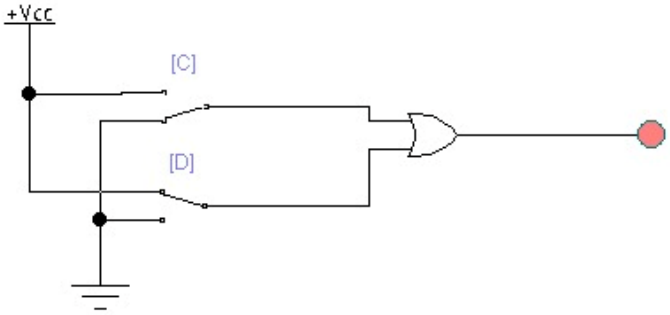


A	B	Output
1	1	1

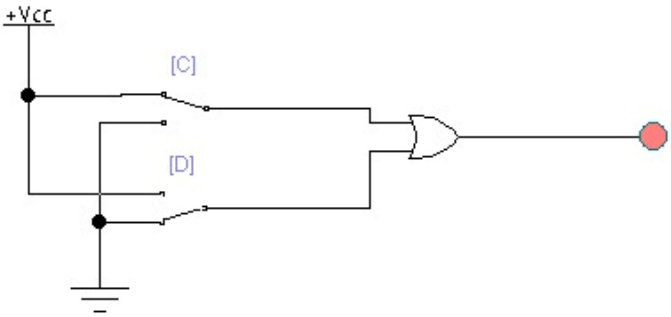
OR GATE



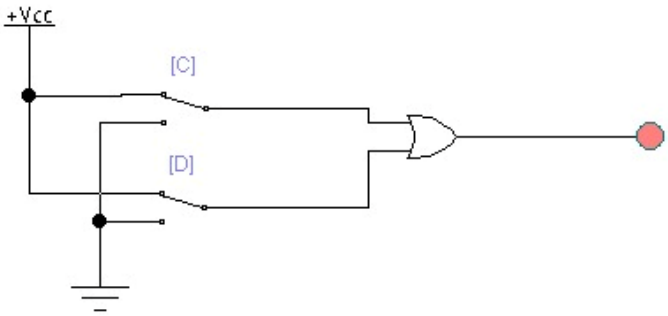
A	B	Output
0	0	0



A	B	Output
0	1	1

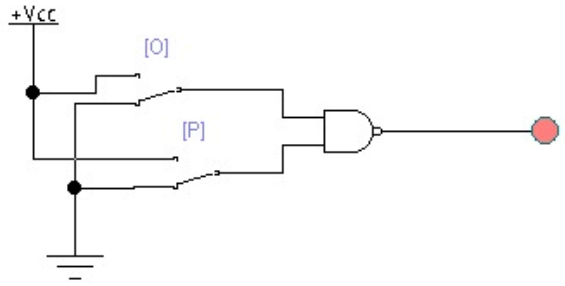


A	B	Output
1	0	1

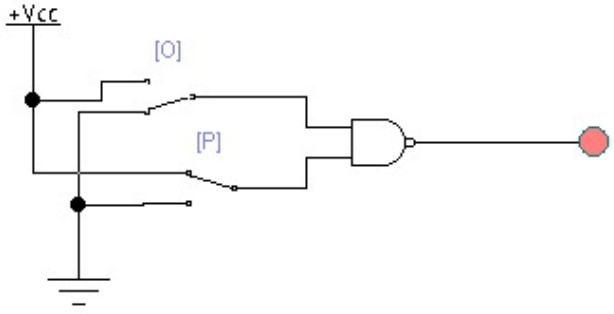


A	B	Output
1	1	1

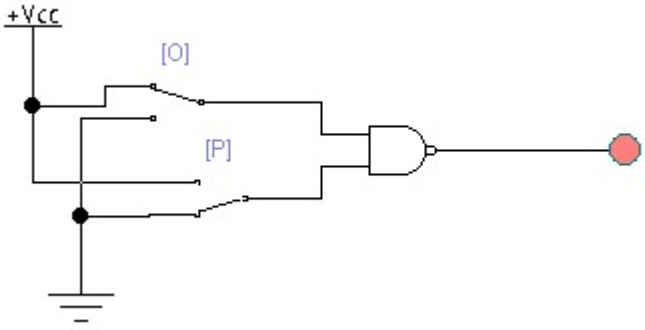
NAND GATE



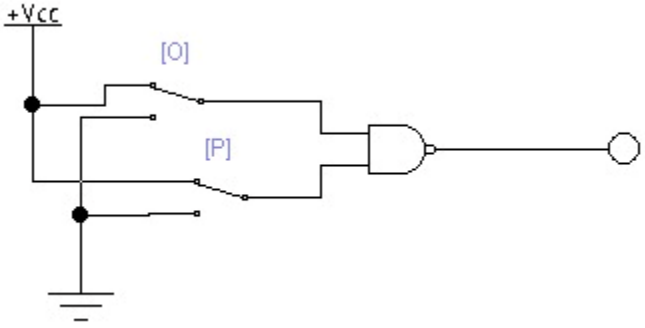
A	B	Output
0	0	1



A	B	Output
0	1	1

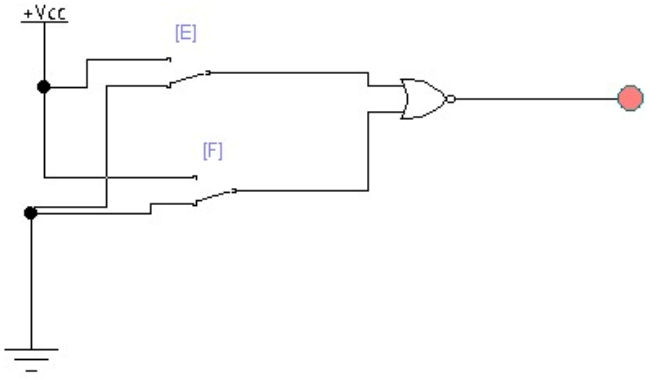


A	B	Output
1	0	1

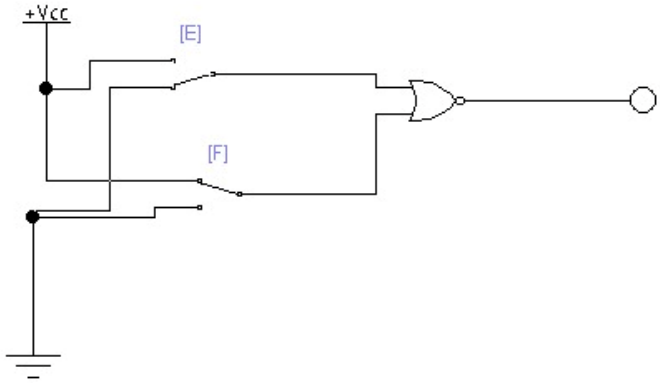


A	B	Output
1	1	0

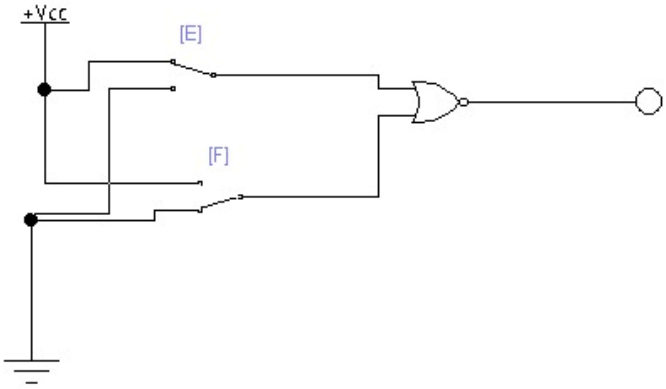
NOR GATE



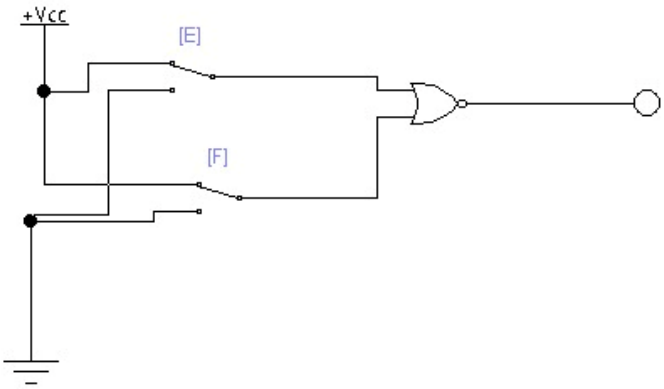
A	B	Output
0	0	1



A	B	Output
0	1	0

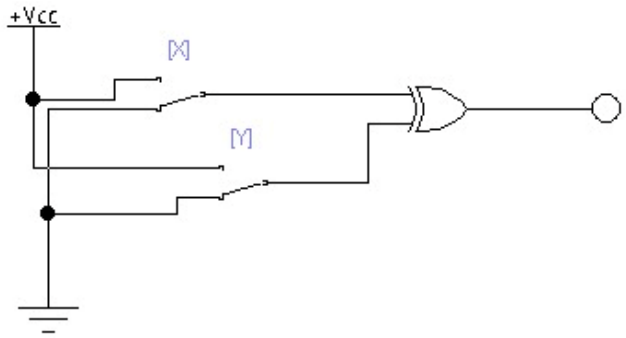


A	B	Output
1	0	0

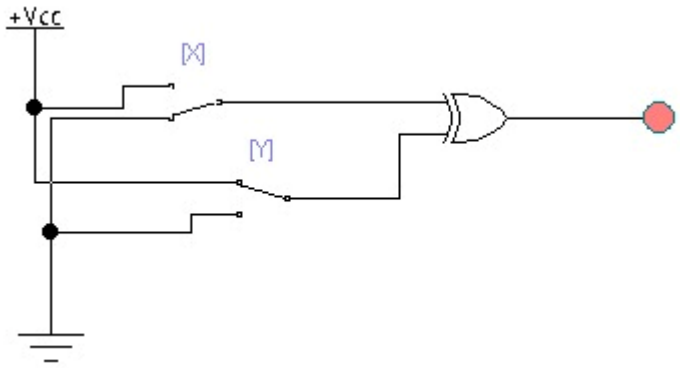


A	B	Output
1	1	0

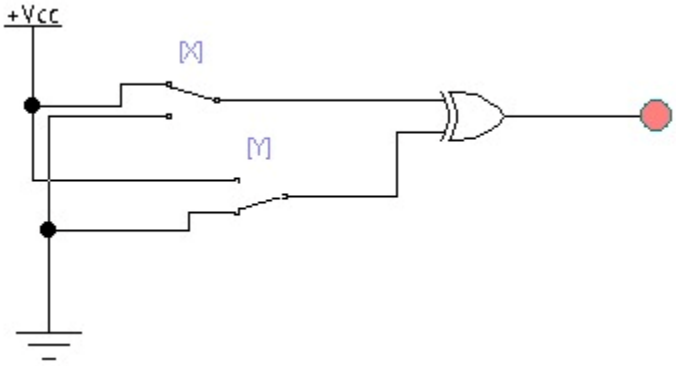
XOR GATE



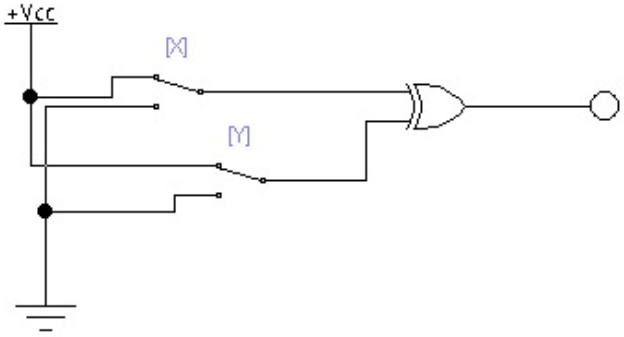
A	B	Output
0	0	0



A	B	Output
0	1	1

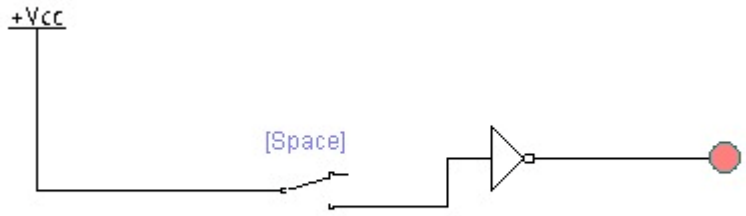


A	B	Output
1	0	1

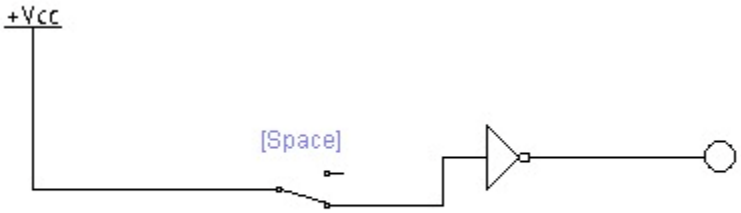


A	B	Output
1	1	0

NOT GATE



A	Output
0	1



A	Output
1	0

Conclusion:

Observations: -

- **AND Gate:** Output is HIGH only when both inputs are HIGH, confirming correct functionality.
- **OR Gate:** Output is HIGH if at least one input is HIGH, matching the truth table.
- **NOT Gate:** Output inverts the input, verified for both HIGH and LOW states.
- **NAND Gate:** Output is LOW only when both inputs are HIGH, as expected.
- **NOR Gate:** Output is HIGH only when both inputs are LOW, functioning correctly.
- **XOR Gate:** Output is HIGH when inputs differ, confirmed for all cases.

All circuits behaved as expected, verified in the electronic workbench. Observed outputs matched theoretical logic for all gates. The experiment successfully demonstrated the input-output relationship of basic logic gates.