

Work Log

Journal:

Date	Tasks	Attendees
Sun, March 6th	Discussed project breakdown	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Fri, March 25th	System Design update and Description/Cohort Information update	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Mon, March 28th	Top Level diagram, State Machine and Verilog Programming	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Tues, March 29th	Verilog Programming continued and State Machine	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Wed, March 30th	Verilog Programming + Bonus Finalizing	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Thurs, March 31st	Debugging and formatting	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Fri, April 1st	Finalizing project and submitting	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)

Affirmations:

Fri, April 1st: Full group (Hamzah, Mariam, Ruchit, Michael, Motalib) got the final Verilog code pushed to GitHub. Each member was able to run it on their own system shortly thereafter. Each member was able to finalize the project.