Work Log

Journal:

Date	Tasks	Attendees
Wed, Feb 16	Project part 2 planning and discussion	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Sun, Feb 20	Worked on: 2.2.2.1 List of inputs, 2.2.2.2 List of outputs, 2.2.2.3 List of interfaces	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Fri, Feb 25	Worked on 2.2.2.4 The List of Parts & Started working on the Verilog code.	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Sun, Feb 27	Worked on: 2.2.2.5 The Top-Level Circuit Diagram, Verilog code, and updated part 1.	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Fri, March 04	Worked on the Verilog Code and Top-Level Diagram	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Sun, March 06	Finalized the project for submission	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)

Affirmations:

Sun, March 6: Full group (Hamzah, Mariam, Ruchit, Michael, Motalib) got the final Verilog code pushed to GitHub. Each member was able to run it on their own system shortly thereafter. Each member was able to finalize the project.