System Design

2.2.2 System Design Description

The System Design description has five tasks that need to be completed. The list of inputs, the list of outputs, the list of interfaces, the list of parts, and the top-level circuit diagram.

2.2.2.1 The List of Inputs

The description in section 2.2.1 gives three inputs. The cohort needs to assign identifier names to these inputs, and list them, including their bit-size and a basic description.

- “A” is a 16-bit integer that will represent the first integer passed to the functional operator.
- “B” is a 16-bit integer that will represent the second integer passed to the functional operator.
- “Op” is a 4-bit code that will determine the operation applied on the two values A and B.

2.2.2.2 The List of Outputs

The description in section 2.2.1 gives two outputs. The cohort needs to assign identifier names to these outputs, and list them, including their bit-size and a basic description.

- “Result” is a 32-bit integer that will represent the output value of the selected operation on inputs A and B.
- “Error” is a 2-bit code that will determine the presence of an error and its type (overflow or division by 0).

2.2.2.3 The List of Interfaces

The description in section 2.2.1 has modules and components that connect to each other. Math modules connect to the multiplexor, the Decoder to the channel select of the multiplexor. These internal connection lines are called interfaces. The cohort needs to assign identifier names to these interfaces, and list them, including their bit-size and a basic description.

- “Mode” is a 1-bit line that determines whether the adder-subtractor does addition or subtraction.
- “Sum” is a 16-bit line that contains the output value from the adder-subtractor module for an addition or subtraction operation that will feed into multiplexor input channel #1 for addition and channel #2 for subtraction (determined by mode).

- “Product” is a 32-bit line that contains the output value from the multiplication module that will feed into multiplexor channel #3.
- “Quotient” is a 16-bit line that contains the output from the division module that will feed into multiplexor channel #4.
- “Remainder” is a 16-bit line that contains the output from the modulo module for a modulo operation that will feed into multiplexor channel #5.
- “Onehot” is a 16-bit one-hot line that contains the channel selection from the 4-bit operational code that will feed into the multiplexor input channels.
- “Mod0Err” is a 2-bit line that contains the error output for the modulus by 0 case which leads from the Modulo module into the Error-Handler module.
- “Div0Err” is a 2-bit line that contains the error output for the division by 0 case which leads from the Divisor module into the Error-Handler module.
- “OFErr” is a 2-bit line that contains the error output for overflow which leads from the Adder-Subtractor module to the Error-Handler module.

2.2.2.4 The List of Parts

The description in section 2.2.1 lists out an adder-subtractor module, a multiplier, a divisor, a modulo, a multiplexor, and a decoder. Each of these is a combinational logic component. The cohort needs to assign identifier names to these components, and list them, including what type of component and a basic description.

- “AdderSubtractor” is the adder-subtractor component in the ALU that is capable of performing addition and subtraction of binary numbers.
- “Multiplier” is the multiplier component in the ALU that is capable of performing multiplication on binary numbers.
- “Divider” is the divisor component in the ALU that is capable of performing integer division on binary numbers.
- “Modulus” is the modulo component in the ALU that is capable of performing the modulus operation on binary numbers (finding the remainder).
- “Mux” is the multiplexor component used in the ALU that handles mutual exclusion among the channels of the ALU.
- “Decoder” is the decoder component used in the ALU that converts the operational code into a one-hot selection for use in the multiplexor.

2.2.2.5 The Top-Level Circuit Diagram

Only the top-level circuit diagram is needed for this portion of the project. The interior workings of the arithmetic modules, the decoder, and the multiplexor are not required. The overall layout of the circuit begins with the inputs far left, next the arithmetic modules near left, then the multiplexor and decoder near right, and finally the output on the far right. Each line should be connected to the correct component, labeled with their

identifiers, and marked with a bus-size shown as a slash on the line, with the size beneath.