

## Work Log

### Journal:

Date	Tasks	Attendees
Wed, April 13th	Discussed project part 4 breakdown	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Sat, April 16th	Verilog programming + Bonus discussion	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Sun, April 16th	Verilog programming + Bonus discussion	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)
Thurs, April 21	Finalizing system design, project update, and verilog programming.	Full group (Hamzah, Mariam, Ruchit, Michael, Motalib)

### Affirmations:

Thurs, April 21: Full group (Hamzah, Mariam, Ruchit, Michael, Motalib) got the final Verilog code pushed to GitHub. Each member was able to run it on their own system shortly thereafter. Each member was able to finalize the project.