
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32N6570-DK
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	03/07/2025

1.2. MCU

MCU Series	STM32N6
MCU Line	STM32N6x7
MCU name	STM32N657X0HxQ
MCU Package	VFBGA264
MCU Pin number	264

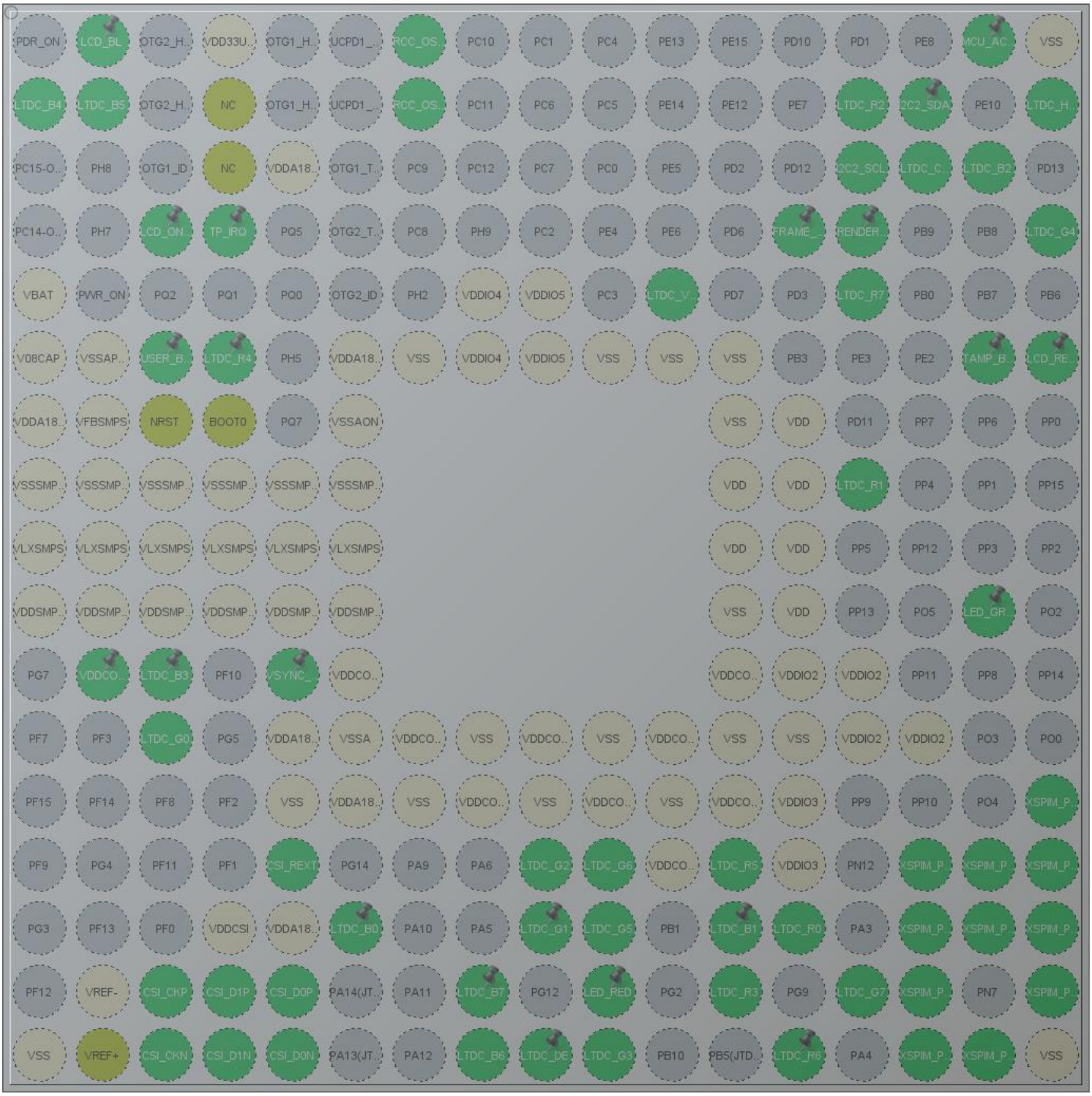
1.3. Core(s) information

Core(s)	ARM Cortex-M55

1.4. Caution

The report was generated although the configuration was in a modified state. It may be not accurate

2. Pinout Configuration



VFBGA264 (Top view)

3. Pins Configuration

Pin Number VFBGA264	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A2	PQ6 *	I/O	GPIO_Output	LCD_BL
A4	VDD33USB	Power		
A7	PH0-OSC_IN(PH0)	I/O	RCC_OSC_IN	
A16	PE9 *	I/O	GPIO_Output	MCU_ACTIVE
A17	VSS	Power		
B1	PH3	I/O	LTDC_B4	
B2	PH6	I/O	LTDC_B5	
B4	NC	NC		
B7	PH1-OSC_OUT(PH1)	I/O	RCC_OSC_OUT	
B14	PD15	I/O	LTDC_R2	
B15	PD4	I/O	I2C2_SDA	
B17	PB14	I/O	LTDC_HSYNC	
C4	NC	NC		
C5	VDDA18USB	Power		
C14	PD14	I/O	I2C2_SCL	
C15	PB13	I/O	LTDC_CLK	
C16	PB2	I/O	LTDC_B2	
D3	PQ3 *	I/O	GPIO_Output	LCD_ON_OFF
D4	PQ4	I/O	GPIO_EXTI4	TP_IRQ
D13	PD0 *	I/O	GPIO_Output	FRAME_RATE
D14	PD5 *	I/O	GPIO_Output	RENDER_TIME
D17	PB15	I/O	LTDC_G4	
E1	VBAT	Power		
E8	VDDIO4	Power		
E9	VDDIO5	Power		
E11	PE11	I/O	LTDC_VSYNC	
E14	PD8	I/O	LTDC_R7	
F1	V08CAP	Power		
F2	VSSAPMU	Power		
F3	PC13 *	I/O	GPIO_Input	USER_BUTTON_1
F4	PH4	I/O	LTDC_R4	
F6	VDDA18AON	Power		
F7	VSS	Power		
F8	VDDIO4	Power		
F9	VDDIO5	Power		
F10	VSS	Power		

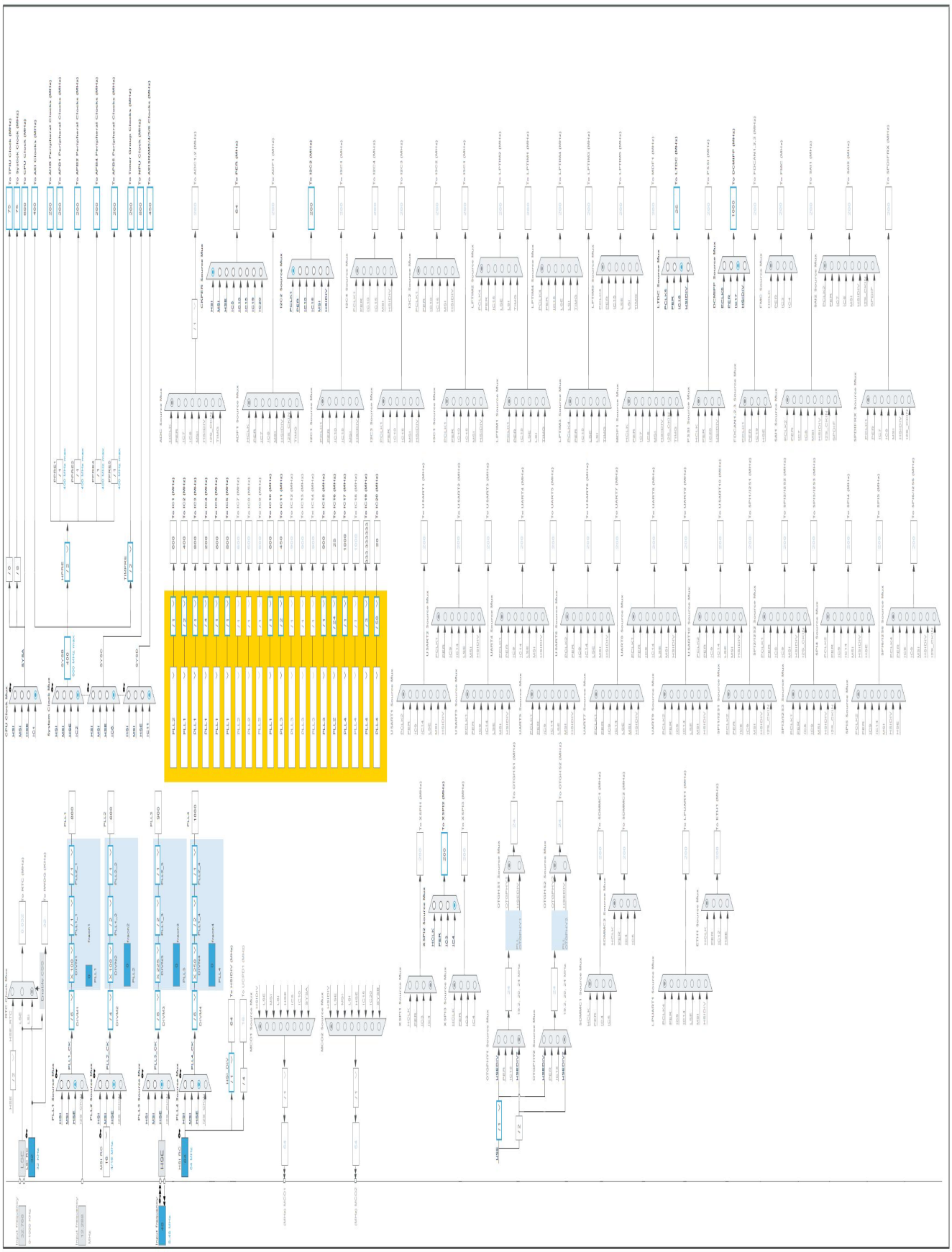
Pin Number VFBGA264	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F11	VSS	Power		
F12	VSS	Power		
F16	PE0 *	I/O	GPIO_Input	TAMP_BUTTON
F17	PE1 *	I/O	GPIO_Output	LCD_RESET
G1	VDDA18PMU	Power		
G2	VFBSMPS	Power		
G3	NRST	Reset		
G4	BOOT0	Boot		
G6	VSSAON	Power		
G12	VSS	Power		
G13	VDD	Power		
H1	VSSSMPS	Power		
H2	VSSSMPS	Power		
H3	VSSSMPS	Power		
H4	VSSSMPS	Power		
H5	VSSSMPS	Power		
H6	VSSSMPS	Power		
H12	VDD	Power		
H13	VDD	Power		
H14	PD9	I/O	LTDC_R1	
J1	VLXSMPS	Power		
J2	VLXSMPS	Power		
J3	VLXSMPS	Power		
J4	VLXSMPS	Power		
J5	VLXSMPS	Power		
J6	VLXSMPS	Power		
J12	VDD	Power		
J13	VDD	Power		
K1	VDDSMPS	Power		
K2	VDDSMPS	Power		
K3	VDDSMPS	Power		
K4	VDDSMPS	Power		
K5	VDDSMPS	Power		
K6	VDDSMPS	Power		
K12	VSS	Power		
K13	VDD	Power		
K16	PO1 *	I/O	GPIO_Output	LED_GREEN
L2	PF4 *	I/O	GPIO_Output	VDDCORE_OVERDRIVE
L3	PG6	I/O	LTDC_B3	

Pin Number VFBGA264	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L5	PF6 *	I/O	GPIO_Output	VSYNC_FREQ
L6	VDDCORE	Power		
L12	VDDCORE	Power		
L13	VDDIO2	Power		
L14	VDDIO2	Power		
M3	PF5	I/O	LTDC_G0	
M5	VDDA18PLL	Power		
M6	VSSA	Power		
M7	VDDCORE	Power		
M8	VSS	Power		
M9	VDDCORE	Power		
M10	VSS	Power		
M11	VDDCORE	Power		
M12	VSS	Power		
M13	VSS	Power		
M14	VDDIO2	Power		
M15	VDDIO2	Power		
N5	VSS	Power		
N6	VDDA18ADC	Power		
N7	VSS	Power		
N8	VDDCORE	Power		
N9	VSS	Power		
N10	VDDCORE	Power		
N11	VSS	Power		
N12	VDDCORE	Power		
N13	VDDIO3	Power		
N17	PN4	I/O	XSPIM_P2_IO2	
P5	CSI_REXT	I/O	CSI_REXT	
P9	PA1	I/O	LTDC_G2	
P10	PB11	I/O	LTDC_G6	
P11	VDDCORE	Power		
P12	PA15(JTDI)	I/O	LTDC_R5	
P13	VDDIO3	Power		
P15	PN6	I/O	XSPIM_P2_CLK	
P16	PN8	I/O	XSPIM_P2_IO4	
P17	PN0	I/O	XSPIM_P2_DQS0	
R4	VDDCSI	Power		
R5	VDDA18CSI	Power		
R6	PG15	I/O	LTDC_B0	

Pin Number VFBGA264	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R9	PG1	I/O	LTDC_G1	
R10	PB12	I/O	LTDC_G5	
R12	PA7	I/O	LTDC_B1	
R13	PG0	I/O	LTDC_R0	
R15	PN3	I/O	XSPIM_P2_IO1	
R16	PN5	I/O	XSPIM_P2_IO3	
R17	PN1	I/O	XSPIM_P2_NCS1	
T2	VREF-	Power		
T3	CSI_CKP	I/O	CSI_CKP	
T4	CSI_D1P	I/O	CSI_D1P	
T5	CSI_D0P	I/O	CSI_D0P	
T8	PA2	I/O	LTDC_B7	
T10	PG10 *	I/O	GPIO_Output	LED_RED
T12	PB4(NJTRST)	I/O	LTDC_R3	
T14	PG8	I/O	LTDC_G7	
T15	PN9	I/O	XSPIM_P2_IO5	
T17	PN2	I/O	XSPIM_P2_IO0	
U1	VSS	Power		
U2	VREF+	MonoIO		
U3	CSI_CKN	I/O	CSI_CKN	
U4	CSI_D1N	I/O	CSI_D1N	
U5	CSI_D0N	I/O	CSI_D0N	
U8	PA8	I/O	LTDC_B6	
U9	PG13	I/O	LTDC_DE	
U10	PA0	I/O	LTDC_G3	
U13	PG11	I/O	LTDC_R6	
U15	PN10	I/O	XSPIM_P2_IO6	
U16	PN11	I/O	XSPIM_P2_IO7	
U17	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Software Project

1.1. Project Settings

Name	Value
Project Name	STM32N6570-DK
Project Folder	C:\Users\HANS\STM32N6570-DK
Toolchain / IDE	EWARM V9.40
Firmware Package Name and Version	STM32Cube FW_N6 V1.0.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	FSBL-0x800
Minimum Stack Size	FSBL-0x800

1.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

1.3. Advanced Settings - Generated Function Calls FSBL

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_HPDMA1_Init	HPDMA1
4	MX_XSPI2_Init	XSPI2
5	MX_XSPIM_Init	XSPIM
6	MX_EXTMEM_MANAGER_Init	EXTMEM_MANAGER

1.4. Advanced Settings - Generated Function Calls Appli

Rank	Function Name	Peripheral Instance Name

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_HPDMA1_Init	HPDMA1
3	MX_JPEG_Init	JPEG
4	MX_DMA2D_Init	DMA2D
5	MX_GPU2D_Init	GPU2D
6	MX_I2C2_Init	I2C2
7	MX_ICACHE_Init	ICACHE
8	MX_LTDC_Init	LTDC
9	MX_CRC_Init	CRC
10	MX_CSI_Init	CSI
11	MX_DCMIPP_Init	DCMIPP
12	MX_CACHEAXI_Init	CACHEAXI
15	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.24.2_Appli
16	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.24.2_Appli
17	MX_RIF_Init	RIF

1.5. Advanced Settings - Generated Function Calls ExtMemLoader

Rank	Function Name	Peripheral Instance Name
1	MX_EXTMEM_MANAGER_Init	EXTMEM_MANAGER

2. Peripherals and Middlewares Configuration

2.1. CACHEAXI

mode: Activated

2.1.1. Core(s) Settings:

Context(s):	Application

2.2. CORTEX_M55_FSBL

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	First Stage Boot Loader

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

2.3. CORTEX_M55_S

2.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
Region Base Address	**0x34100000 ***
Region Limit Address	**0x34248FFF ***
MPU Attributes Number	ATTRIBUTE 0

MPU Access Permission	**ALL READS\WRITES Permissions ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Device	**MPU DEVICE GRE ***

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
Region Base Address	**0x34249000 ***
Region Limit Address	**0x343BFFFF ***
MPU Attributes Number	ATTRIBUTE 1
MPU Access Permission	**ALL READS\WRITES Permissions ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Device	**MPU DEVICE nGnRnE ***

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	**Enabled ***
Region Base Address	**0x70100400 ***
Region Limit Address	**0x701FFFFF ***
MPU Attributes Number	ATTRIBUTE 2
MPU Access Permission	**ALL READS Permissions ***
MPU Instruction Access	ENABLE
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**MPU WRITE BACK ***
MPU Transient Permission	**MPU NOT TRANSIENT ***
MPU Allocate Permission	**MPU R ALLOCATE ***
MPU Device	NONE

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	**Enabled ***
Region Base Address	**0x70200000 ***
Region Limit Address	**0x73FFFFFF ***
MPU Attributes Number	ATTRIBUTE 3
MPU Access Permission	**ALL READS Permissions ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**MPU WRITE BACK ***
MPU Transient Permission	MPU TRANSIENT
MPU Allocate Permission	**MPU R ALLOCATE ***
MPU Device	NONE

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

2.4. CRC

mode: Activated

2.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

2.5. CSI

Mode: double data lanes D1_D0

2.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Lane Merger:

Physical Lane 0 Status	Enabled
Physical Lane 0 Mapping	0
Physical Lane 1 Status	Disabled
Physical Lane 1 Mapping	1

Physical Bitrate:

Physical Bitrate	80 Mhz

2.6. DCMIPP

DCMIPP: Camera Serial Interface

mode: Pipe 1

2.6.1. PIPE1:

Core(s) Settings:

Context(s):	Application

Mode Config:

FrameRate	All frames captured
Pixel Pipe Format	RGB888 or YUV422 1-buffer
Pixel Pipe Pitch	10

Serial Interface Config:

Virtual Channel ID	Channel 0
Data Type Mode	Only flow DTIDA from the selected VC is forwaded in the pipe
Data Type ID-A	YUV420 8bit
Data Type ID-B	YUV420 8bit

2.7. DMA2D

mode: Activated

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

2.8. GPU2D

mode: Activated

2.8.1. Core(s) Settings:

Context(s):	Application

2.9. I2C2

I2C: I2C

2.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x109035B7 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

2.10. ICACHE

Mode: 2-ways set associative cache

Secure Attribute: secured

2.10.1. Core(s) Settings:

Context(s):	Application

2.11. JPEG

mode: Activated

2.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Version:

JPEG version	jpeg1_v1_0

JPEG Software options:

ENCODE	**Disabled ***
DECODE	Enabled
RGB_FORMAT	**JPEG_RGB565 ***
JPEG_SWAP_RG	0

2.12. LTDC

Display Type: RGB888 (24 bits)

2.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application

Synchronization for Width:

Horizontal Synchronization Width	**5 ***
Horizontal Back Porch	**8 ***
Active Width	**800 ***
Horizontal Front Porch	**8 ***
HSync Width	4
Accumulated Horizontal Back Porch Width	12
Accumulated Active Width	812
Total Width	820

Synchronization for Height:

Vertical Synchronization Height	**5 ***
Vertical Back Porch	**8 ***
Active Height	480
Vertical Front Porch	**14 ***
VSync Height	4
Accumulated Vertical Back Porch Height	12
Accumulated Active Height	492
Total Height	506

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

2.12.2. Layer Settings:

Core(s) Settings:

Context(s):	Application

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Number of Layers:

Number of Layers	**1 layer ***

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**800 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**480 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB565 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Line Length (Image Width)	**800 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**480 ***

Flexible YUV:

Layer 1 - Color Converter	0

2.13. PWR

mode: I/O voltage range selection

mode: Dead Battery Signals disabled

mode: Power saving mode

mode: Security and Privilege attributes

2.13.1. Parameter Settings:

Core(s) Settings:

Context(s):	First Stage Boot Loader

I/O voltage range selection:

VDDIO2	**(1.8) ***
VDDIO3	**(1.8) ***
VDDIO4	(3.3)
VDDIO5	(3.3)

2.13.2. PWR Privilege :

Core(s) Settings:

Context(s):	First Stage Boot Loader

Privilege PWR:

Privilege of PWR Secure Items	Disable
Privilege of PWR Non-Secure Items	Disable

2.13.3. PWR Security:

Core(s) Settings:

Context(s):	First Stage Boot Loader

Secure PWR:

Wake-Up 1 secure protection	Disable
Wake-Up 2 secure protection	Disable
Wake-Up 3 secure protection	Disable
Wake-Up 4 secure protection	Disable
Low power modes secure protection	Disable
Backup domain secure protection	Disable
Retention secure protection	Disable
Supply configuration and monitoring secure protection	Disable
Voltage USB Secure Protection	Disable

2.14. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	First Stage Boot Loader Application External Memory Loader

Power Parameters:

SupplySource	PWR_EXTERNAL_SOURCE_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Spread spectrum mode:

PLL1 CSG mode	Disabled
PLL2 CSG mode	Disabled
PLL3 CSG mode	Disabled
PLL4 CSG mode	Disabled

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	16
TIM Group1 Prescaler Selection	Disabled
TIM Group2 Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

System Parameters:

VDD voltage (V)	3.3

2.15. RIF

mode: RISUP

2.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Application
0	
SPI1/I2S1	false
	false
	-
	false
1	
SPI2/I2S2	false
	false
	-
	false
2	
SPI3/I2S3	false
	false
	-
	false
3	
SPI4	false
	false
	-
	false
4	
SPI5	false
	false
	-
	false

5	
SPI6/I2S6	false
	false
	-
	false
6	
SAI1	false
	false
	-
	false
8	
SAI2	false
	false
	-
	false
9	
I2C1	false
	false
	-
	false
10	
I2C2	false
	false
	-
	false
11	
I2C3	false
	false
	-
	false
12	
I2C4	false
	false
	-
	false
13	
I3C1	false
	false
	-
	false
14	
I3C2	false
	false

	-
	false
15	
USART1	false
	false
	-
	false
16	
USART2	false
	false
	-
	false
17	
USART3	false
	false
	-
	false
18	
UART4	false
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	false
19	
UART5	false
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20	
USART6	false
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	false
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UART7	false
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UART8	false
	false
	-
	false
23	

UART9	false
	false
	-
	false
24	
USART10	false
	false
	-
	false
25	
LPUART1	false
	false
	-
	false
26	
FDCAN1	false
	false
	-
	false
27	
TIM1	false
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	-
	false
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TIM2	false
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TIM3	false
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TIM4	false
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TIM5	false
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TIM6	false
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TIM7	false
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TIM9	false
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TIM11	false
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TIM12	false
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39	
TIM13	false
	false
	-
	false
40	
TIM14	false

	false
	-
	false
41	
TIM15	false
	false
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	false
42	
TIM16	false
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	-
	false
43	
TIM17	false
	false
	-
	false
44	
TIM18	false
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	false
45	
GFXTIM	false
	false
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46	
LPTIM1	false
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47	
LPTIM2	false
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	-
	false
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LPTIM3	false
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	-
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LPTIM4	false
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ADF1	false
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WWDG	false
	false
	-
	false
76	
RNG	false
	false
	-
	false
77	
PKA	false
	false
	-
	false
78	
SAES	false
	false
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	false
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HASH	false
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CRYP1	false
	false
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	false
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MCE1	false
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MCE2	false
	false
	-
	false
83	
MCE3	false
	false
	-

	false
84	
MCE4	false
	false
	-
	false
86	
XSPI1	false
	false
	-
	false
87	
XSPI2	false
	false
	-
	false
88	
XSPI3	false
	false
	-
	false
89	
XSPIM	false
	false
	-
	false
90	
FMC	false
	false
	-
	false
92	
CSI2HOST	false
	false
	-
	false
93	
DCMIPP	false
	false
	-
	false
94	
DCMI	false

	false
	-
	false
96	
JPEG	false
	false
	-
	false
97	
VENC	false
	false
	-
	false
98	
ICACHE	false
	false
	-
	false
99	
GPU	false
	false
	-
	false
100	
GFXMMU	false
	false
	-
	false
101	
DMA2D	false
	false
	-
	false
102	
LTDC_CMN	false
	false
	-
	false
103	
LTDC_L1	false
	false
	-
	false

104	
LTDC_L2	false
	false
	-
	false
106	
NPU	false
	false
	-
	false

2.16. SYS_S

Timebase Source: TIM2

2.16.1. Core(s) Settings:

Context(s):	Application

2.17. XSPI2

Mode: Octo SPI

Port: Port2 Octo

Chip Select Override: NCS1 -- Port2 --

2.17.1. Parameter Settings:

Core(s) Settings:

Context(s):	First Stage Boot Loader

Generic:

Fifo Threshold	**4 ***
Memory Mode	Disable
Memory Type	**Macronix ***
Memory Size	**1 GBits ***
Chip Select High Time Cycle	**2 ***
Free Running Clock	Disable
Clock Mode	Low
Wrap Size	Not Supported
Clock Prescaler	0
Sample Shifting	None

Delay Hold Quarter Cycle	**Enable ***
Chip Select Boundary	Disabled
Maximum Transfer	0
Refresh Rate	0
Memory Select	NCS1
Switching Duration Clock Number	1

2.18. XSPIM

mode: Direct (XSPI1 to Port1, XSPI2 to Port2, XSPI3 not used)

2.18.1. Core(s) Settings:

Context(s):	First Stage Boot Loader

2.19. EXTMEM_MANAGER

mode: Activate External Memory Manager

2.19.1. Boot usecase:

Core(s) Settings:

Context(s):	First Stage Boot Loader External Memory Loader

Boot:

Select boot code generation	**true ***
Selection of the boot system	Execute In Place

XIP:

select the memory	Memory 1
Application offset	**0x100000 ***
Header size	**0x400 ***

2.19.2. Memory 1:

Core(s) Settings:

Context(s):	First Stage Boot Loader External Memory Loader

Select driver:

Select the memory driver	EXTMEM_NOR_SFDP

Configuration:

Memory Instance	XSPI2
Number of memory data line	**EXTMEM_LINK_CONFIG_8LINES ***

2.19.3. Memory 2:

Core(s) Settings:

Context(s):	First Stage Boot Loader External Memory Loader

Select driver:

Select the memory driver	NONE

2.20. STMicroelectronics.X-CUBE-AI.10.0.0_Appli

2.21. STMicroelectronics.X-CUBE-TOUCHGFX.4.24.2_Appli

mode: GraphicsJjApplication

2.21.1. TouchGFX Generator:

Core(s) Settings:

Context(s):	Application

Display:

Interface	**Parallel RGB (LTDC) ***
Framebuffer Pixel Format (LTDC)	RGB565
Width (LTDC)	800
Height (LTDC)	480
Use Larger Framebuffer Stride	No
Framebuffer Strategy	**Double Buffer ***
Buffer Location	By Allocation

Driver:

Application Tick Source	**LTDC ***
Use DMA2D Accelerator (ChromART)	**Yes ***
Use GPU2D Accelerator (NeoChrom)	**Yes ***
Real-Time Operating System	**ThreadX ***
Memory Pool Allocation	Static
Memory Pool Size	4096
Memory Stack Size	4080

Additional Features:

External Data Reader	Disabled
Vector Rendering	**Hardware ***
Vector Font Rendering	**Enabled ***

GPU2D Driver:

GPU2D Command List Size	8192

Video Decoding:

Type	**Hardware ***
Concurrent videos	1
Strategy	Direct to Framebuffer

2.22. THREADX

mode: Core

2.22.1. ThreadX:

Core(s) Settings:

Context(s):	Application

Core:

TX_MINIMUM_STACK	200
TX_THREAD_USER_EXTENSION	
TX_DISABLE_STACK_FILLING	Disabled
TX_ENABLE_STACK_CHECKING	Disabled
TX_DISABLE_PREEMPTION_THRESHOLD	Enabled
TX_DISABLE_REDUNDANT_CLEARING	Disabled
TX_DISABLE_NOTIFY_CALLBACKS	Enabled
TX_INLINE_THREAD_RESUME_SUSPEND	Disabled
TX_NOT_INTERRUPTABLE	Disabled
TX_MAX_PRIORITIES	32
TX_TIMER_TICKS_PER_SECOND	**1000 ***
TX_NO_FILEX_POINTER	Disabled
TX_THREAD_SECURE_STACK_MINIMUM	256
TX_THREAD_SECURE_STACK_MAXIMUM	**2048 ***
Enable BASEPRI support	Disabled
TX_DISABLE_ERROR_CHECKING	Disabled

Timer:

TX_TIMER_PROCESS_IN_ISR	Disabled
TX_REACTIVATE_INLINE	Disabled
TX_TIMER_THREAD_STACK_SIZE	**2048 ***

TX_TIMER_THREAD_PRIORITY	0
Version:	
ThreadX version	6.4.0
ThreadX App Init:	
Generate App Init Code	false
Memory Configuration:	
ThreadX memory pool size	**8192 ***
Memory Pool Allocation	Use Static Allocation
ThreadX MemPool Name	tx_app_byte_pool

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context
CSI	CSI_REXT	CSI_REXT	n/a	n/a	n/a		Application
	CSI_CKP	CSI_CKP	n/a	n/a	n/a		Application
	CSI_D1P	CSI_D1P	n/a	n/a	n/a		Application
	CSI_D0P	CSI_D0P	n/a	n/a	n/a		Application
	CSI_CKN	CSI_CKN	n/a	n/a	n/a		Application
	CSI_D1N	CSI_D1N	n/a	n/a	n/a		Application
	CSI_D0N	CSI_D0N	n/a	n/a	n/a		Application
I2C2	PD4	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low		Application
	PD14	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low		Application
LTDC	PH3	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PH6	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PD15	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB14	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB13	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB2	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PE11	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PD8	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PH4	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PD9	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG6	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PF5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA1	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context
	PB11	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA15(JTDI)	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG15	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG1	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB12	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA7	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG0	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA2	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PB4(NJTRST)	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG8	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG13	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PA0	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
	PG11	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low		Application
RCC	PH0-OSC_IN(PH0)	RCC_OSC_IN	n/a	n/a	n/a		First Stage Boot Loader Application
	PH1-OSC_OUT(PH1)	RCC_OSC_OUT	n/a	n/a	n/a		First Stage Boot Loader Application
XSPI2	PN4	XSPIM_P2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN6	XSPIM_P2_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN8	XSPIM_P2_IO4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN0	XSPIM_P2_DQS0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN3	XSPIM_P2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN5	XSPIM_P2_IO	Alternate Function Push	No pull-up and no pull-down	Very High		First Stage Boot

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context
		3	Pull				Loader
	PN1	XSPIM_P2_NCS1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN9	XSPIM_P2_IO5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN2	XSPIM_P2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN10	XSPIM_P2_IO6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
	PN11	XSPIM_P2_IO7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		First Stage Boot Loader
GPIO	PQ6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL	First Stage Boot Loader* Application
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MCU_ACTIVE	First Stage Boot Loader* Application
	PQ3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_ON_OFF	First Stage Boot Loader* Application
	PQ4	GPIO_EXTI4	**External Interrupt Mode with Falling edge trigger**	No pull-up and no pull-down	n/a	TP_IRQ	First Stage Boot Loader* Application
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	FRAME_RATE	First Stage Boot Loader* Application
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RENDER_TIME	First Stage Boot Loader* Application
	PC13	GPIO_Input	Input mode	**Pull-down ***	n/a	USER_BUTTON_1	First Stage Boot Loader* Application
	PE0	GPIO_Input	Input mode	**Pull-down ***	n/a	TAMP_BUTTON	First Stage Boot Loader* Application
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RESET	First Stage Boot Loader* Application
	PO1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN	First Stage Boot Loader* Application
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VDDCORE_OVERDRIVE	First Stage Boot Loader* Application
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	VSYNC_FREQ	First Stage Boot

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context
							Loader* Application
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED	First Stage Boot Loader* Application

* Initialized context

3.2. GPDMA1

3.2.1. Core(s) Settings:

Context(s):	First Stage Boot Loader Application

3.3. HPDMA1

Channel 1 - 4 Words Internal FIFO : Standard Request Mode

Channel 0 - 4 Words Internal FIFO : Standard Request Mode

3.3.1. All Channels:

Core(s) Settings:

Context(s):	First Stage Boot Loader Application
Channel 0:	
Request	HPDMA1_REQUEST_JPEG_RX
Channel 1:	
Request	HPDMA1_REQUEST_JPEG_TX

3.3.2. SECURITY:

Core(s) Settings:

Context(s):	First Stage Boot Loader Application
CH1:	
Enable Isolation	**STATIC_ISOLATION_ON ***
CID	Static CID: 1

Enable Channel as Privileged	PRIVILEDGED
Enable Channel as Secured	SECURE
Enable Source as Secured	SECURE
Enable Destination as Secured	SECURE

CH0:

Enable Isolation	**STATIC_ISOLATION_ON ***
CID	Static CID: 1
Enable Channel as Privileged	PRIVILEDGED
Enable Channel as Secured	SECURE
Enable Source as Secured	SECURE
Enable Destination as Secured	SECURE

3.3.3. CH1:

Core(s) Settings:

Context(s):	First Stage Boot Loader Application

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**JPEG_TX ***
DMA Handle in IP Structure	hdmaout
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**Very High ***
Transaction Mode	Normal
Direction	Peripheral To Memory

Source Data Setting:

Source Address Increment After Transfer	Disabled
Data Width	**Word ***
Burst Length	**8 ***
Allocated Port for Transfer	**Port 1 ***

Destination Data Setting:

Destination Address Increment After Transfer	**Enabled ***
Data Width	**Word ***
Burst Length	**8 ***
Allocated Port for Transfer	Port 0

Data Handling:

Data Handling Configuration	Disable

Trigger:

Trigger Configuration	Disable
Trigger Selection	HPDMA CH0 TCF

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

3.3.4. CH0:

Core(s) Settings:

Context(s):	First Stage Boot Loader Application

Circular configuration:

Circular Mode	Disable

Request Configuration:

Request	**JPEG_RX ***
DMA Handle in IP Structure	hdmain
Block HW request protocol	Single/Burst Level

Channel configuration:

Priority	**Very High ***
Transaction Mode	Normal
Direction	**Memory To Peripheral ***

Source Data Setting:

Source Address Increment After Transfer	**Enabled ***
Data Width	Byte
Burst Length	**8 ***
Allocated Port for Transfer	Port 0

Destination Data Setting:

Destination Address Increment After Transfer	Disabled
Data Width	**Word ***
Burst Length	**8 ***
Allocated Port for Transfer	**Port 1 ***

Data Handling:

Data Handling Configuration	**Enable ***
Data exchange	NONE
Data Alignment	**Packed at the destination data width when src data width smaller than dest data width ***

Trigger:

Trigger Configuration	Disable
Trigger Selection	HPDMA CH0 TCF

Transfer Event Configuration:

Transfer Event Generation	The TC (and the HT) event is generated at the (respectively half) end of each block

3.4. LINKEDLIST

3.4.1. Core(s) Settings:

Context(s):	First Stage Boot Loader Application

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
Secure fault	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	14	0
EXTI Line4 interrupt	true	0	0
DMA2D global interrupt	true	0	0
JPEG global interrupt	true	8	0
GPU2D global interrupt	true	0	0
GPU2D Error interrupt	true	0	0
GPU2D cache interrupt	true	0	0
HPDMA1 Channel 0 global interrupt	true	6	0
HPDMA1 Channel 1 global interrupt	true	7	0
TIM2 global interrupt	true	5	0
LTDC global interrupt	true	5	0
LTDC error interrupt	true	5	0
FPU global interrupt	unused		
DCMIPP global interrupt	unused		
I2C2 Event interrupt	unused		
I2C2 Error interrupt	unused		

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
Secure fault	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pendable request for system service	false	false	false
System tick timer	false	false	true
EXTI Line4 interrupt	false	true	true
DMA2D global interrupt	false	true	true
JPEG global interrupt	false	true	true
GPU2D global interrupt	false	true	true
GPU2D Error interrupt	false	true	true
GPU2D cache interrupt	false	true	true
HPDMA1 Channel 0 global interrupt	false	true	true
HPDMA1 Channel 1 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
LTDC global interrupt	false	true	true
LTDC error interrupt	false	true	true

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
Secure fault	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
FPU global interrupt	unused		
XSPI2 global interrupt	unused		

3.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
Secure fault	false	true	false
System service call via SWI instruction	false	true	false

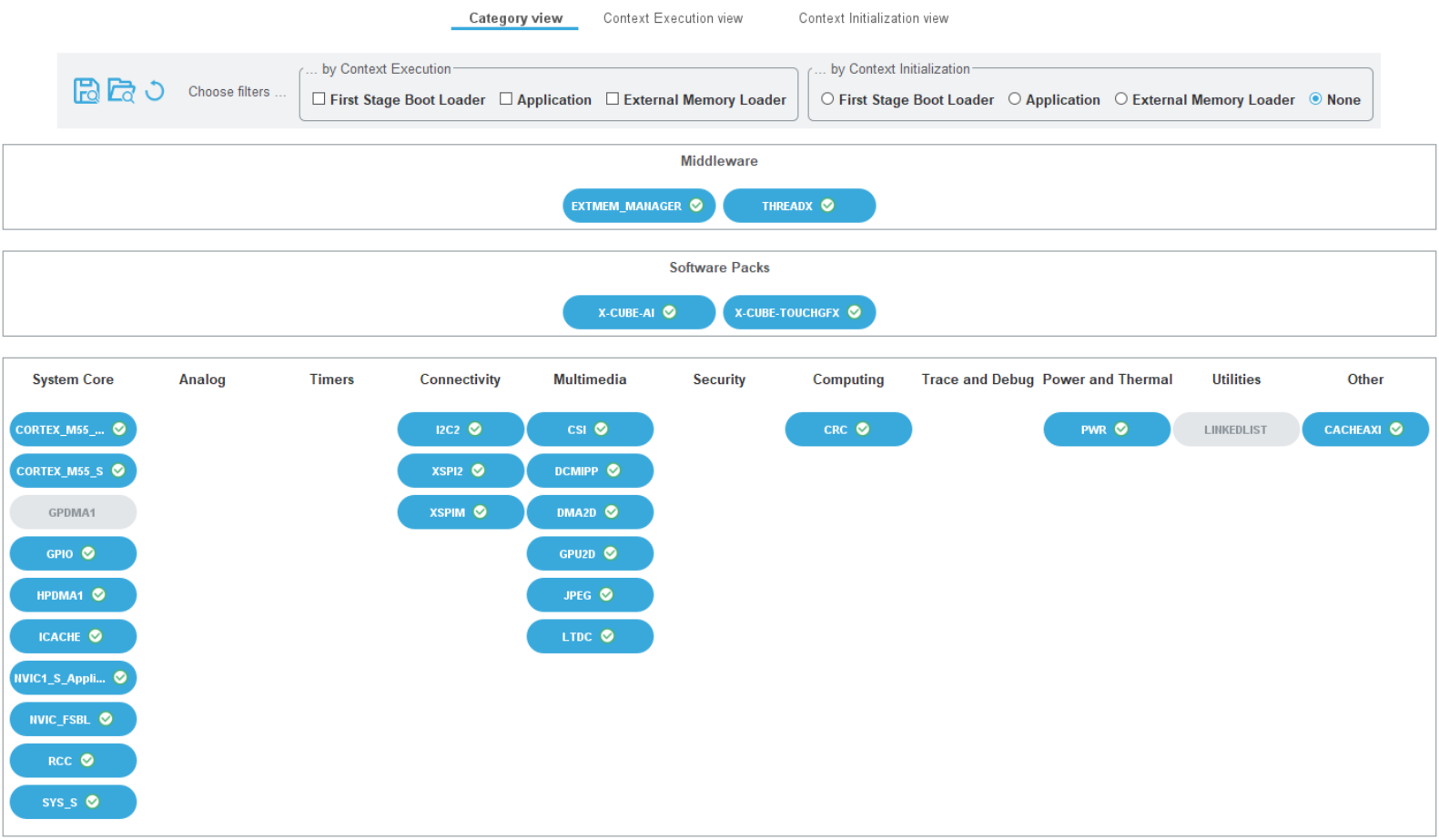
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

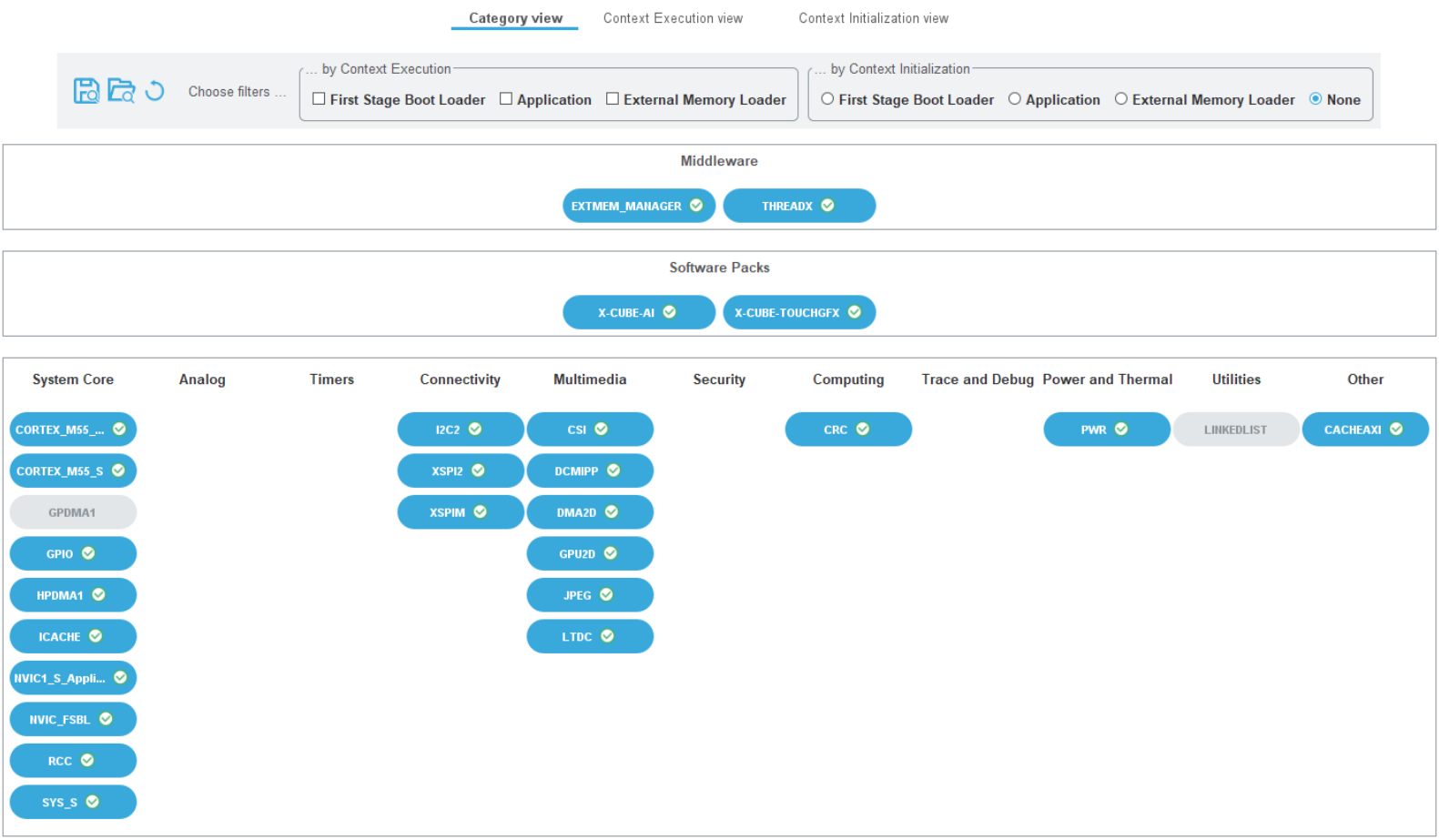
4. System Views

4.1. Category view

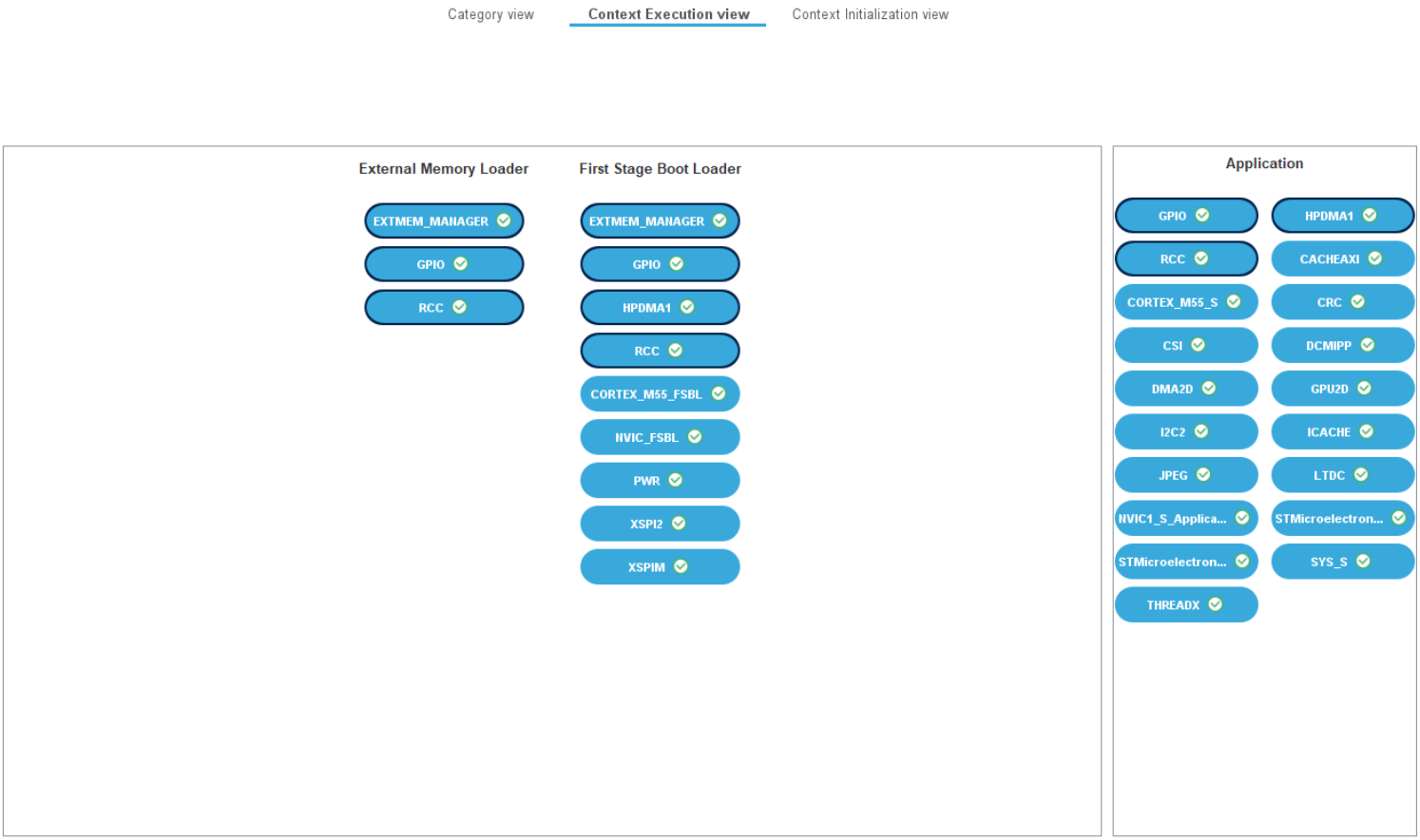
4.1.1. Current



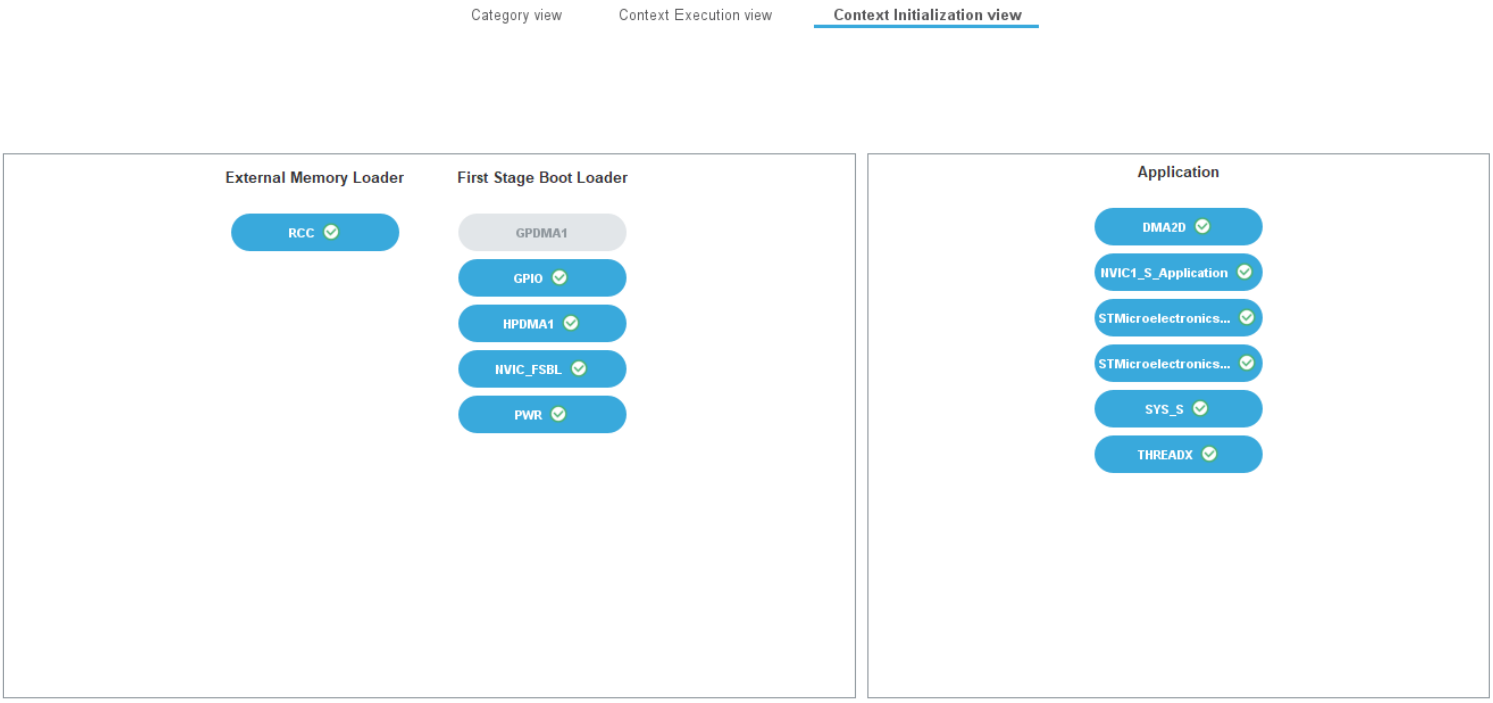
4.1.2. Without filters



4.2. Context Execution view



4.3. Context Initialization view



5. Software Pack Report

5.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.24.2	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.24.2
STMicroelectronics	X-CUBE-AI	10.0.0	Class : Artificial Intelligence Group : Core Version : 10.0.0

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32n6-bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32n6-ibis.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32cubeai_press_pres.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/presentation-st-edge-ai-suite.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32n6-series-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/st-neural-art-accelerator-introduction.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32n6.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-

	increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4991-how-to-wake-up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4879-introduction-to-usb-hardware-and-pcb-guidelines-using-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcusmpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-introduction-to-

	timers-for-stm32-mcus-stmicroelectronics.pdf
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