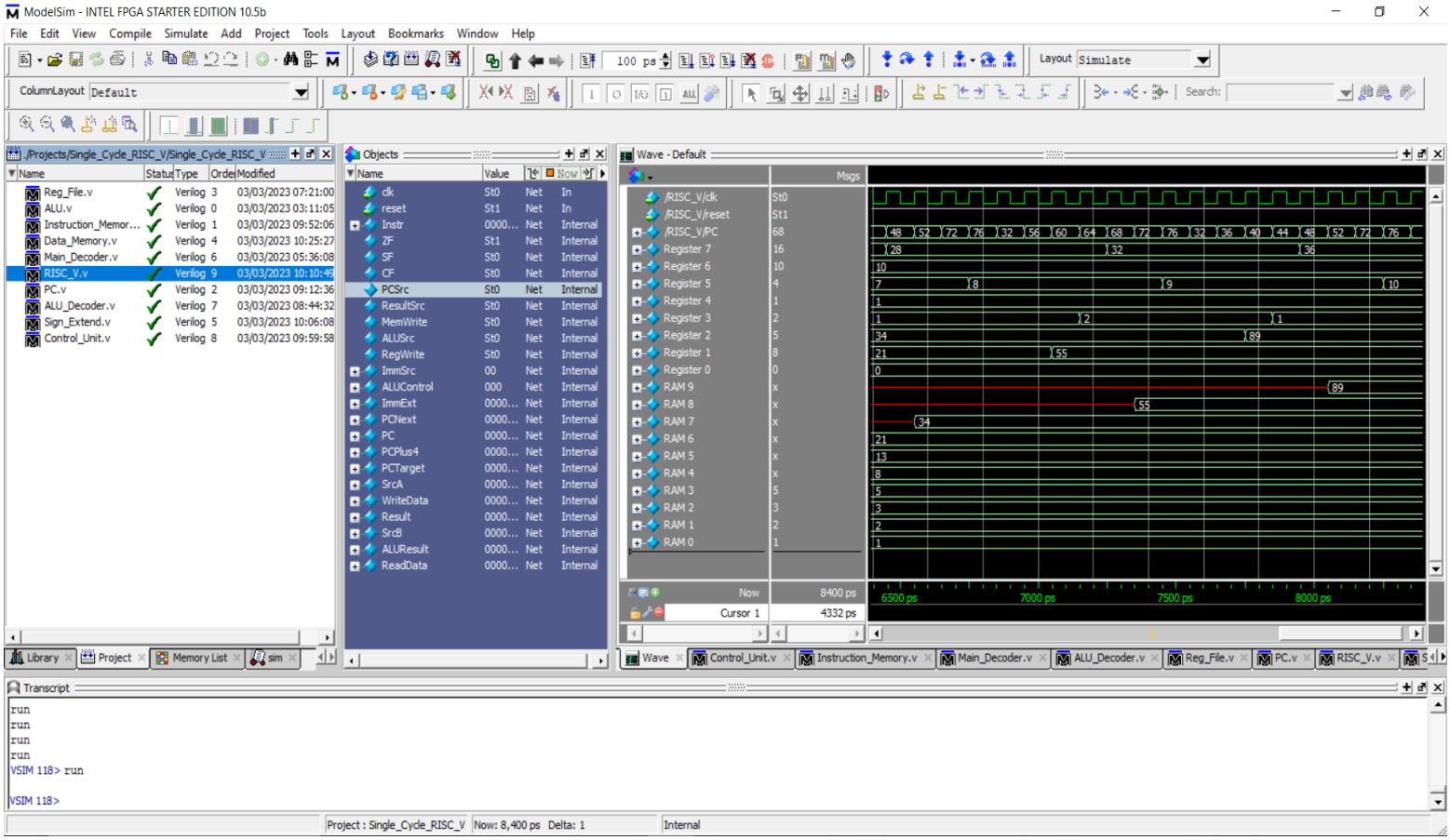
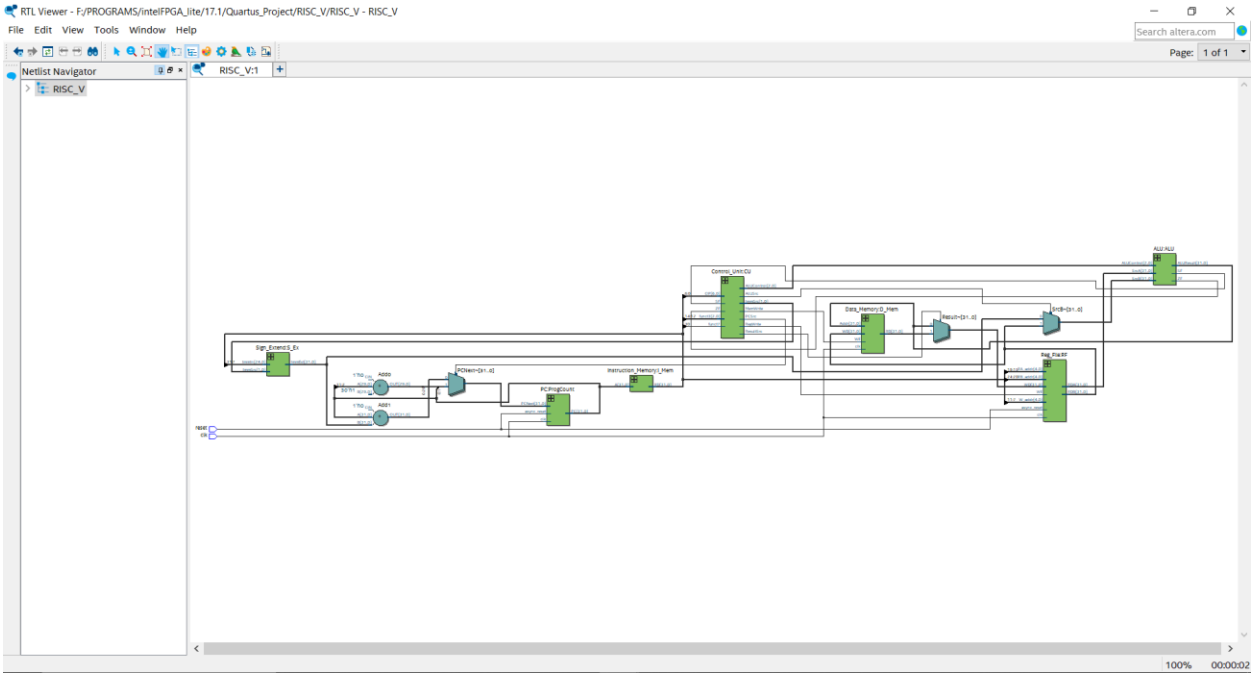
Simulation:

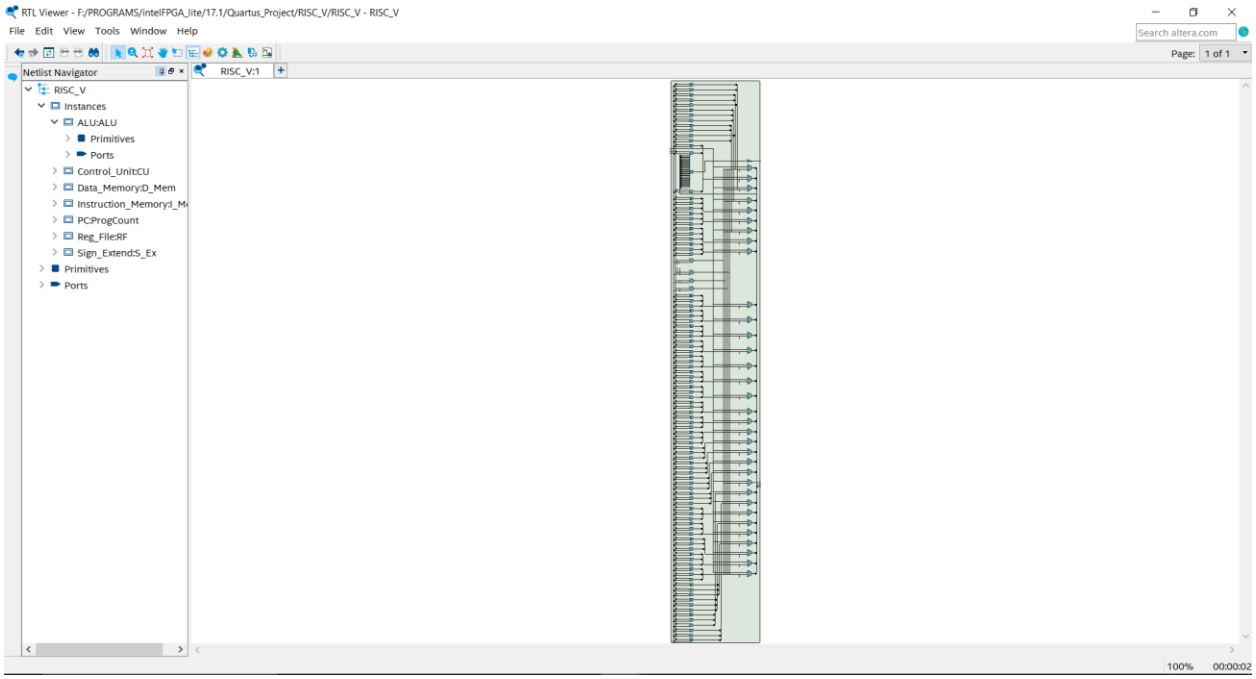

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Wave - Default
Objects
Transcript
run
run
run
run
VSIM 118> run
VSIM 118>
Project : Single_Cycle_RISC_V
Now: 8,400 ps Delta: 1
Internal

RTL Viewer:

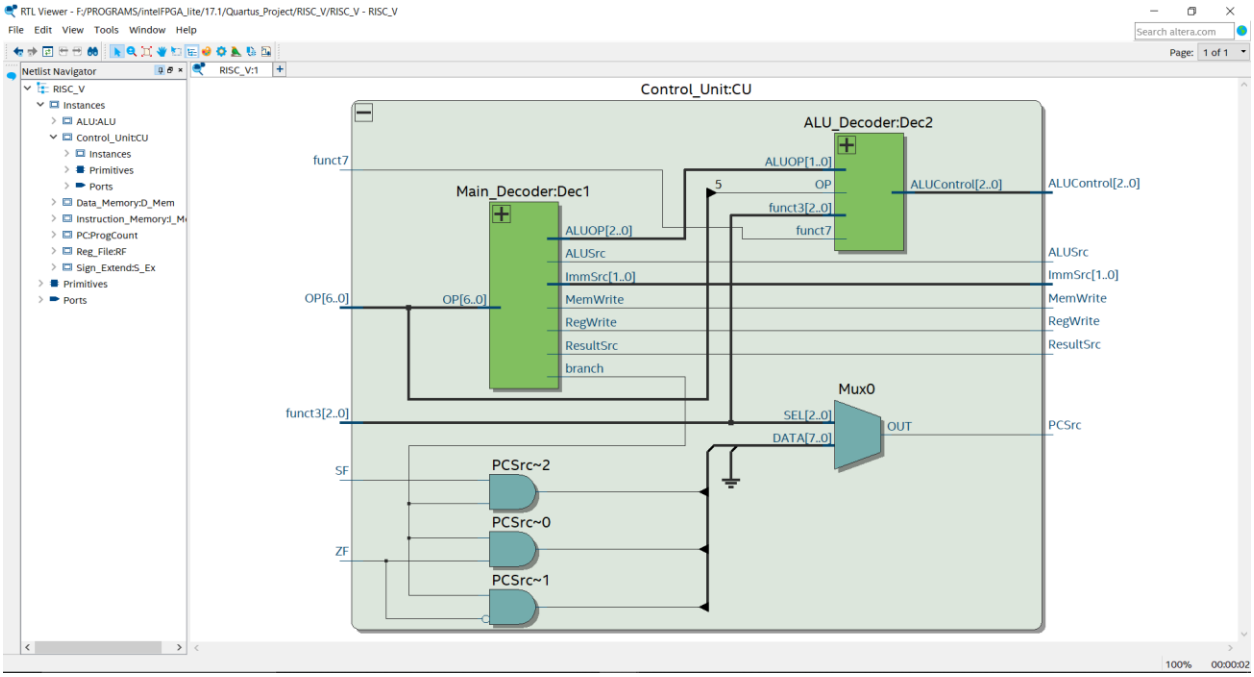
1- The RISC_V Processor



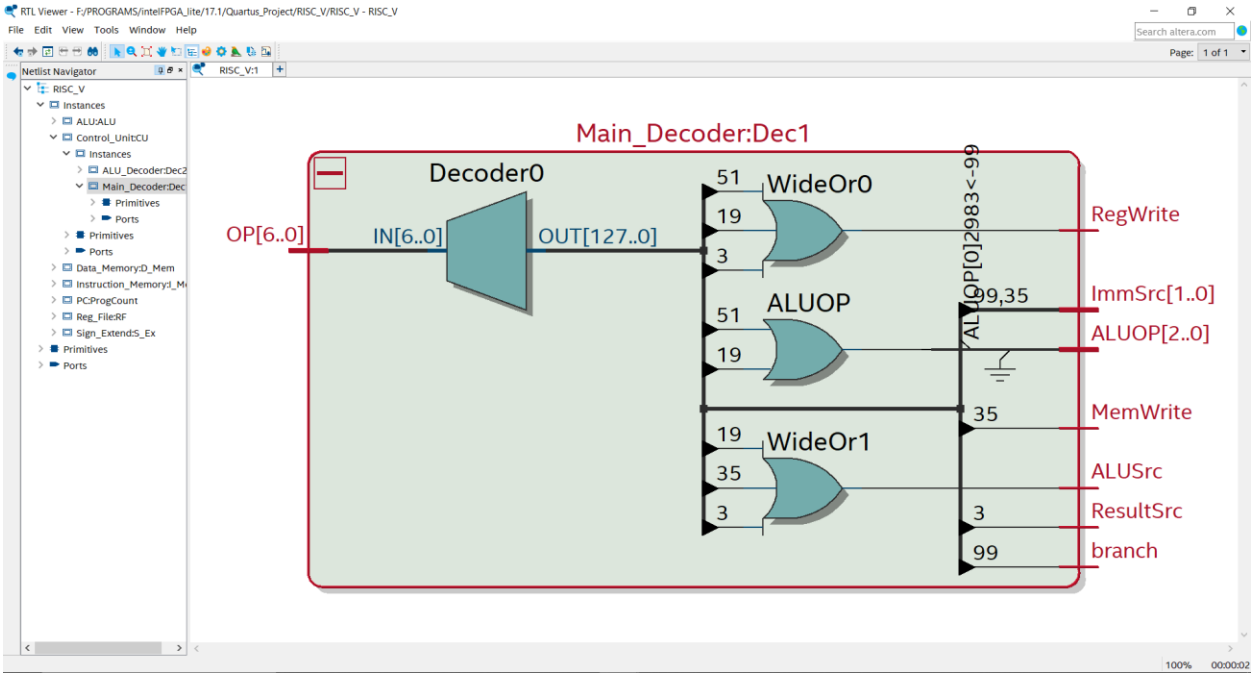
2- ALU



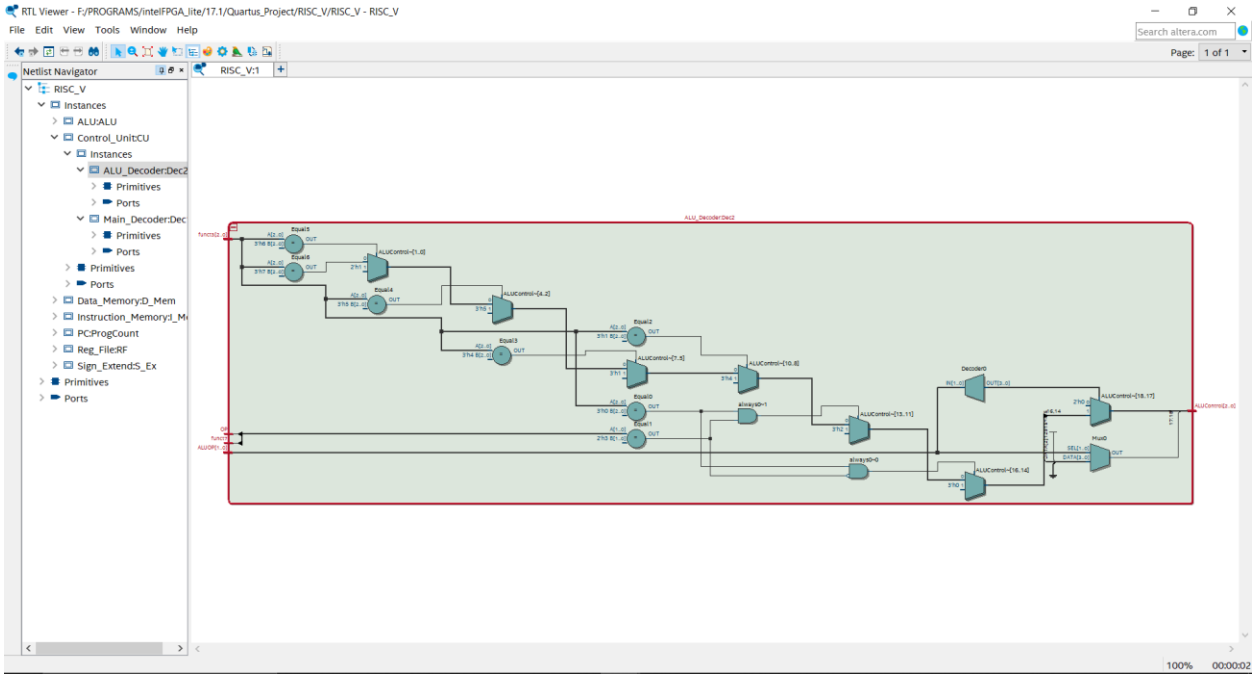
3- Control Unit



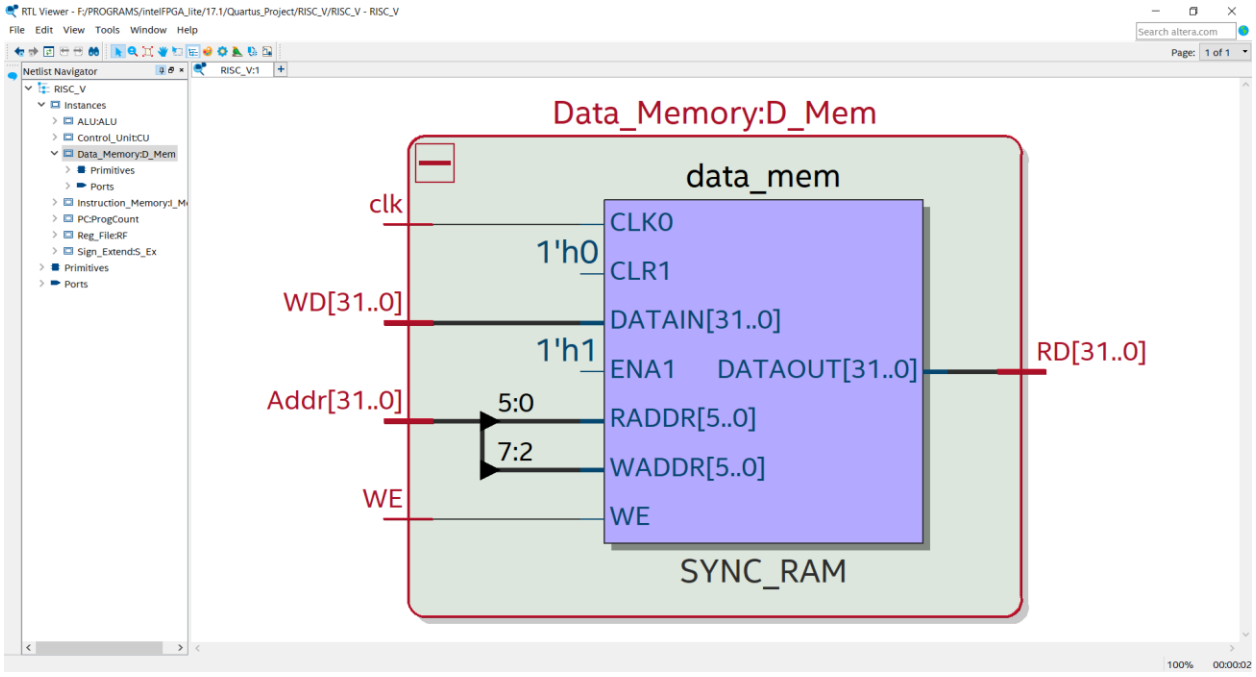
4- Main Decoder



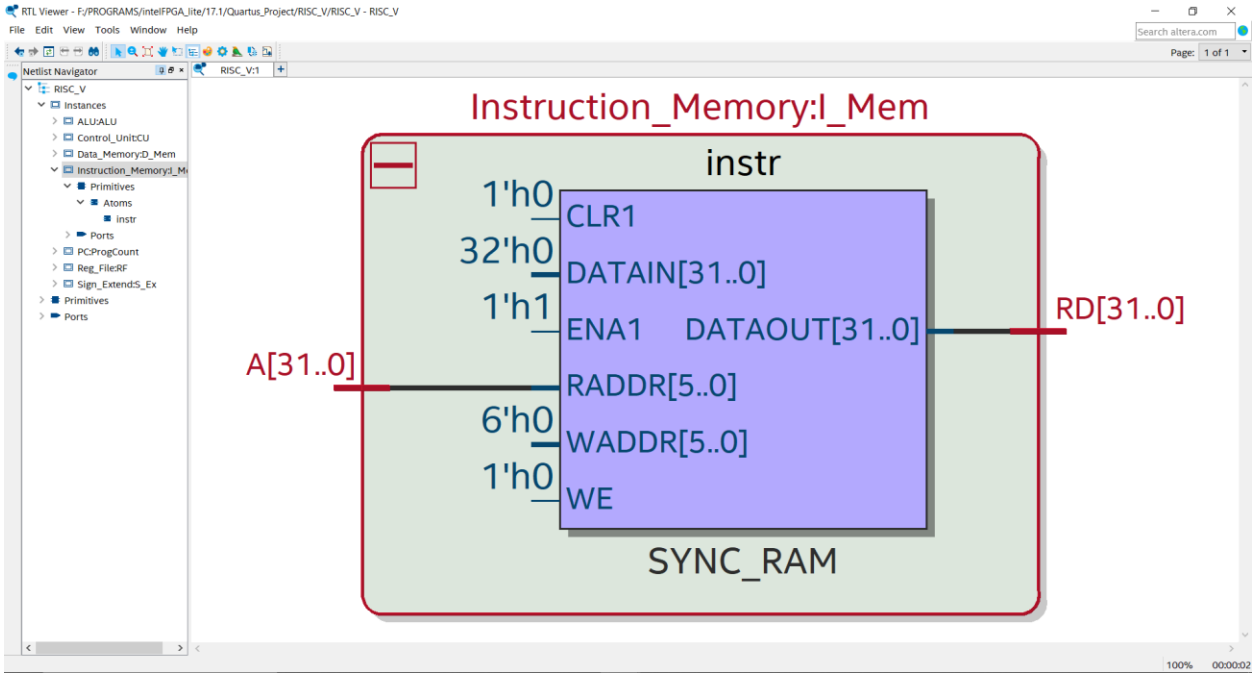
5- ALU Decoder



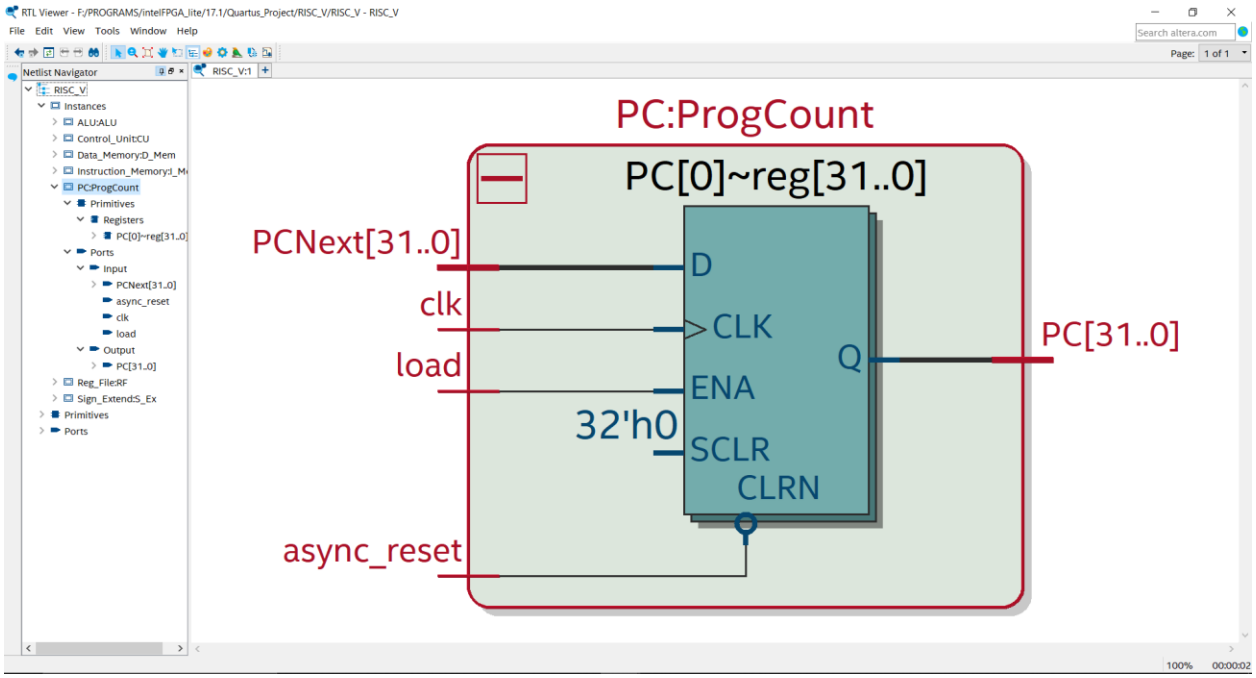
6- Data Memory



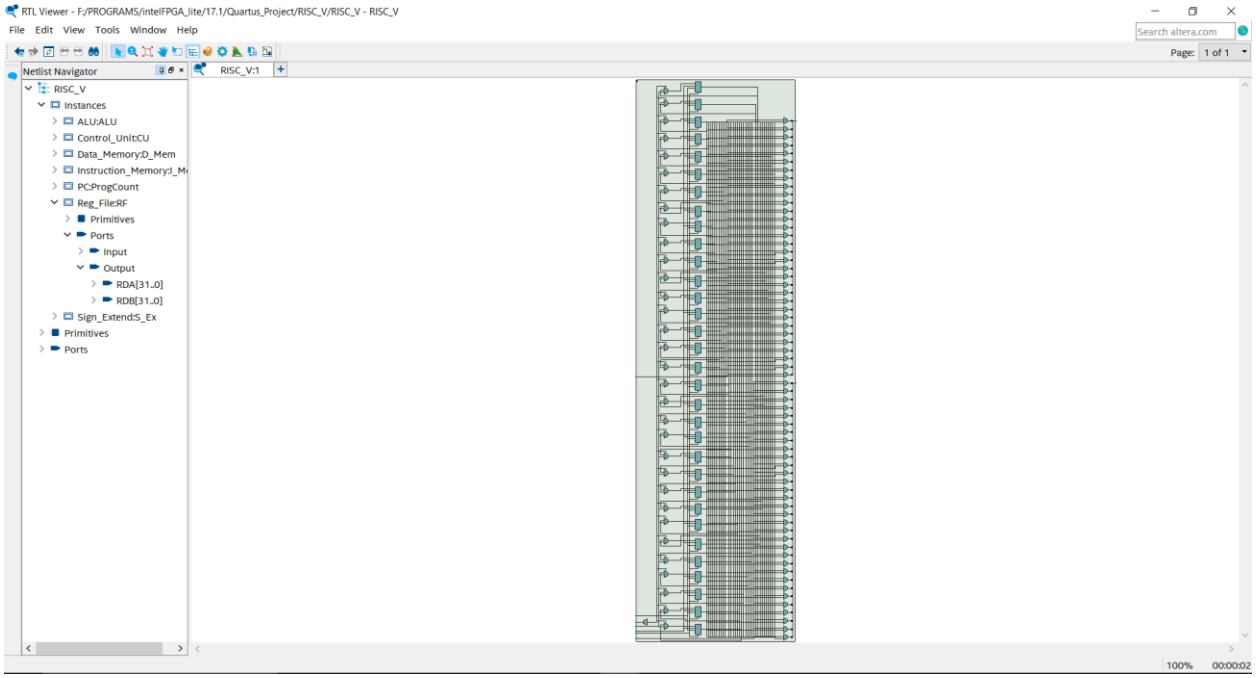
7- Instruction Memory



8- Program Counter



9- Register File



10-Sign Extend