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MEng Honours Project Phase 2 Report
An EEG Signal Band Sigma Delta Modulator With CIFF topology
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Mission Statement

Project Definition

A block level design of an EEG signal band sigma delta modulator by Simulink. The design aims to minimise power consumption , while guaranteeing excellent data conversion performance and system robustness.

Main Tasks

The project includes following tasks:

- Simulink design of sub-blocks (including integrators, quantizers etc.)
- Simulink design of the completed modulator model.
- Simulation on designed model, focused on modulator's performance.
- Estimations of theoretical power consumption and noise caused by non-linearity.
- Estimations of different noise power, including circuit noise.

For the second phase:

- A Circuit-level model for the modelled modulator.
- Simulation on circuit model on modulator's performance.
- Completed noise analysis with circuit model.
- Completed power consumption analysis with circuit performance.
- Transistor level modelling for certain circuit components

This final project is expected to be completed within 51 weeks (08/Jan/2024 – 13/Jan/2025)

Introduction

In rapidly evolving neuroscience and cognitive science fields, electroencephalogram (EEG) could be essential for many tasks and applications. Aiming to achieve desired performance, advance analogue-to-digital converter should be applied, and due to this specific purpose, sigma-delta modulator with CIFF (Chain of Integrators with Feed-forward) topology is one of the most popular design choices.

Sigma-delta modulator with CIFF design could offer low power consumption while realising same noise transfer function as CIFB (Chain of Integrators with Feed-backward). It also could be implemented with less capacitor area and easier dynamic range scaling, since the integrators' outputs only contains quantization noise, capacitor could be dedicated to noise filtering .

Background Knowledge

Signal Processing, Sigma-Delta Modulator, MATLAB Coding, Simulink Modelling, Cadence Suite for Circuit Level design.

Declarations

The supervisor and student are satisfied that this project is suitable for performance and assessment in accordance with the guidelines of the course documentation.

Abstract

This study presents the design, simulation and analysis of a high-performance Sigma-Delta modulator ($\Sigma\Delta$M) for Electroencephalography (EEG) system, focusing on challenges in low-noise, high-resolution, and low power consumption analogue front-end (AFE) applications. By employing a 3rd-order Cascade of Integrators with Feed-forward (CIFF) topology, the proposed modulator achieved achieves optimal noise shaping and stability. A refined design workflow is proposed. By incorporating block-level design with circuit-level non-linearity factors, transition from block-level modelling to circuit implementation can be smoothed, and minimize iterations in the later design stages. Comprehensive simulations are performed to validate the design's performance, achieving a signal-to-noise ratio (SNR) of 119.33 dB and a dynamic range (DR) of 119.9 dB. Stability are tested, confirming the modulator's robustness.

This $\Sigma\Delta$M design demonstrates significant potential for advanced EEG systems for supporting high resolution signal acquisition in applications such as neuroscience, medical diagnostics, and brain–computer interface (BCI), while the proposed workflow can potentially reduce design cost, leading to a more efficient and predictable design.

Declaration of Originality

I declare that this thesis is my
original work except where stated.

.....

Statement of Achievement

I confirm that I was the only contributor to this study on Sigma-Delta modulator modelling and simulating, while my supervisor Dr. Shiwei Wang and Dr. Istvan Gyongy providing me valuable consultations and supports to this subject. The key achievements at this stage include: (1) The objectives of this design is well-discussed, while the state-of-art studies are reviewed; (2) A model level Sigma-Delta modulator with completed defined block parameters; (3) A refined workflow is proposed, aiming on assess the modulator performance in early stage and reduce iterations; (4) Simulations on model behaviour at various conditions, which shows the model is capable to perform required A/D conversion at expected frequency range; (5) noise analysis is conducted, gives a performance reference for further works and provides design specification for transistor-level design.

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List of Symbols

A_v Gain of OTA.

B_w Signal bandwidth.

FoM_S The Schreier FoM.

L The order of the sigma-delta modulator.

N Bit-length of quantizer.

PDF Probability distribution function.

P_s Power of signal.

$S_{E,q}$ Quantization noise power spectral density.

T Sampling period of the system; defined as the reciprocal of the sampling frequency f_s.

T Temperature in Kelvin.

Δ Step of quantization.

γ Thermal noise coefficient of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET).

ω Angular frequency of the signal; expressed in radians per second.

τ Settling time of OTA.

$\mathbf{IBN}_q$ In-band noise power caused by quantization.

OSR Oversampling ratio.

e_q Quantization error.

f_N Nyquist frequency; defined as half of the sampling frequency.

f_s Sampling frequency.

g_m Transconductance.

k Boltzmann constant $1.381 \times 10^{-23} JK^{-1}$.

Glossary

ΣΔM Sigma-Delta modulator.

AAF anti-aliasing filter.

ADC analogue-to-digital converter.

AFE analogue front-end.

BCI brain–computer interface.

CIFB Cascade of Integrators with Feedback.

CIFF Cascade of Integrators with Feed-forward.

CMOS Complementary Metal Oxide Semiconductor.

CMRR Common-Mode Rejection Ratio.

codec coder/decoder.

CRFB Cascade of Resonators with Feedback.

CRFF Cascade of Resonators with Feedforward.

CT Continuous-Time.

DAC digital-to-analogue converter.

DR dynamic range.

DSP digital signal processing.

DT Discrete-Time.

ECG electrocardiogram.

EDA Electronic Design Automation.

EEG Electroencephalography .

EMG electromyographic.

ENOB Effective number of bits.

FFT Fast Fourier Transform.

GBW Gain-Bandwidth Product.

IA instrumentation amplifier.

IBN in-band noise.

MASH Multi-Stage Modulators.

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor.

MSA Maximum Stable Amplitude.

NTF noise transfer function.

OTA Operational transconductance amplifier.

PDM Pulse-density Modulation.

PSD Power Spectral Density.

S-C Switched-capacitor.

S/H Sample-and-hold.

SAR successive approximation register.

SFDR Spurious-Free Dynamic Range.

SNDR signal-to-noise-and-distortion ratio.

SNR signal-to-noise ratio.

SQNR signal-to-quantization-noise ratio.

STF signal transfer function.

Chapter 1

Introduction

Electroencephalography (EEG) is the most commonly applied method for detecting and recording electrical signals from the brain, which could reflect various physiological behaviour and activity of the subject. Beyond being used for medical diagnosis, EEG signal with high fidelity is highly demanded by advanced neuroscience and cognitive science, such as brain–computer interface (BCI) and other applications involving brain-controlling concept [1]. Considering the EEG signal is an extremely weak raw electric signal with amplitude of 1-100 μV, a specific system is required to perform analogue to digital conversion for data collection and further analysis. This system, defined as analogue front-end (AFE), is required to achieve high signal-to-noise ratio (SNR) in order to avoid impact on signal detection accuracy[2], and this would lead the design emphasis of AFE to analogue-to-digital converter (ADC) design.

Normally, EEG signal can be decomposed into different components at particular frequency band: delta ($\leq$4 Hz), theta (4-8 Hz), alpha (8-12 Hz), beta (12-30 Hz), gamma (30-80 Hz) and other activity signal at higher frequency [3]. Recent research and studies have proved that EEG signal at high frequency, or "spike" signal, is related to learning and recognition [4]. To detect delicate EEG signal such as spiking activity, the desired operating bandwidth of ADC is 0.5 Hz - 1 kHz [5], with high SNRs provide resolution above 12 bits [6]–[8]. Moreover, due to the weakness of EEG signal, it could be easily affected by noises and interferences, like electromyographic (EMG) signal, electrocardiogram (ECG) signal, power noise, voltage offset and artifacts caused by motion. This requires the ADC to have a wide dynamic range (DR) to avoid circuit saturation. Other design considerations that are commonly found in state-of-art studies, such as low power consumption, also contributes to EEG signal acquisition circuit.

The performance of AFE in EEG systems is largely determined by quality of the ADC. Rencent research has proposed various high-performance ADCs. Given the requirements of achieving high resolution at a relatively low-speed, successive approximation register (SAR) ADCs and

sigma-delta ADCs are widely used for EEG AFEs due to their ability to balance precision, noise, and power efficiency. SAR ADC simply applies the idea of binary search algorithm to compare the input voltage to a given voltage reference by high-speed comparator, while the SAR logic and digital-to-analogue converter (DAC) adjust the reference voltage. This operating principle leads to the resolution of the SAR ADC is mainly determined by the step of the reference voltages [9]. Recent studies indicate SAR ADCs could perform a satisfying resolution with ultra-low power consumption. In [10], the proposed SAR ADC achieved Effective number of bits (ENOB) of 12 bits with power consumption of only 455 nW. However, the accuracy of SAR ADC is limited by capacitance mismatch introduced in fabrication process. Though, many techniques can be applied to counteract capacitance mismatch, the ENOB of SAR ADC is hardly exceed 16 bits due to the limitation on component noise [11]. Meanwhile, as more complex architectures and higher power consumption are applied to achieve higher solution, the power and area efficiency advantages of SAR ADCs are diminished.

In case of seeking higher resolution, sigma-delta ADCs are regarded as a better option. Benefited from oversampling technique, sigma-delta ADCs can provide higher signal-to-noise-and-distortion ratio (SNDR), and for some specific applications such as audio coder/decoder (codec) and industrial instrumentation, sigma-delta ADCs with over 20 bits ENOB are widely used.[12], [13]. Numbers of sigma-delta ADC studies have proved its capability of operates as a practical AFE component, however, there is still design challenges remain to be addressed. In some research such as [14], stability is ensured by carefully turning the coefficients in its noise transfer function (NTF), but this also introduced additional complexity, and reduced SNR.

This work addressed on a block-level EEG propose Sigma-Delta modulator ($\Sigma\Delta$M) design, while providing additional circuit-level non-linearity to give a better view of the modulator's performance. The proposed modulator employs a 3-order, 1-bit quantizer design with Cascade of Integrators with Feed-forward (CIFF) topology. Simulations are performed with calculations of various noise, conversely, based on desired performance, specific requirements for modulator components can be obtained. By applying these simulations with parameters reinforced, the actual performance and stability of the modulator can be foreseen, and simplifying the design to component circuit engineering. The proposed modulator is assumed to be implemented in 0.35μm CMOS technology, with power supply of 1 V. Simulations are conducted, showing the proposed modulator can achieve SNR of 119.33 dB and DR of 119.9 dB.

The remainder of this paper is organized as follows: Chapter 2 discusses the background of $\Sigma\Delta$M and motivation of this work. In Chapter 3, the design of the proposed modulator is introduced, with calculation and estimation given. Simulation results with comments are shown in Chapter 4. The conclusion is presented in Chapter 5. Chapter 6 discusses how the design could be further improved, and the impact from the proposed design is also discussed.

Chapter 2

Background

The acquisition and processing of Electroencephalography (EEG) signal offers unique requirements and challenges due to its signal characteristic, such as low amplitude, diverse frequency components and sensitivity to various noise and offsets. These challenges highlights the demand to a highly specialized signal acquisition system in order to maintain resolution of the signal and minimize all sorts of interference. In this chapter, necessary background is given for understanding the context and motivation behind the Sigma-Delta modulator ($\Sigma\Delta$M) proposed.

Section 2.1 provides the basic technical background to the proposed design, outlined as follows: Section 2.1.1 gives the characteristic of of EEG signal, with its frequency bands, significance on neuroscience and cognitive science, and challenges of acquisition raised by interference. Section 2.1.2 discusses the role of analogue front-end (AFE) in EEG acquisition system with its composition, focusing on the critical contribution of the analogue-to-digital converter (ADC). Commonly used ADC architectures are compared, which highlights the advantage of $\Sigma\Delta$Ms for its high resolution, low power consumption. Section 2.1.3 provides an in-depth illustration of the mechanisms of $\Sigma\Delta$Ms, with attention to their architectures, topologies, performance metrics and design.

Number of recent studies are given in Section 2.2 to provide a general understanding of $\Sigma\Delta$Ms proposed with similar application to this work. In Section 2.3, motivation of this design and the previous work are presented, highlighting the background leads to this specific research focus, and the progress made since the phase one of this project.

2.1 Technical Background

2.1.1 Characteristics and Challenges in EEG Signals

Electroencephalography, EEG is a widely used method for measuring and analysing human brain's electrical activity. EEG signal can provide valuable insights to help medical diagnosis, and understanding of physiological processes and cognitive states. The first brain electrical signal detected was succeeded in 1924 by Hans Berger [15], in the after 100 years, EEG has be broadly adopted by clinicians and researchers. The brain electrical signal exists as an extracellular voltage fluctuations, which can be measured and recorded by EEG with scalp or subdural electrodes on the measure subject [3]. Typically EEG signal can be considered as composed by signals in different amplitudes and frequency bands (figure 2.1), these are: (1) Delta(δ) in frequency range of 0.1-4 Hz, exhibits sleep and unconscious state. (2) Theta (θ) in frequency range of 4-8 Hz, revealing part of sleeping state, and creativeness, intuitiveness, recalling, fantasy, imaginary and dream . (3) Alpha (α) in frequency range of 8-13 Hz showing the activity when waking and relaxed with conscious. (4) Beta (β) in frequency range of 13-30 Hz indicating the brain cortex is activated, and the subject is focused, thinking with alertness of surroundings. (5) Gamma (γ) typically in frequency range of 30-80 Hz [3], exhibits activities such as movement and mental function [16]. In recent researches, it is proved that, EEG signal detected at higher frequency is correlated to high-level cognition such as learning and creation [3], [4], [17]. Usually, to record the high frequency signal, called "neuron spikes" as mentioned before (figure 2.2), EEG device is often required to have bandwidth of no less than 1 kHz in order to record delicate spike signal, which only sustains for less than 1 ms [5], [18].

Another characteristic of brain electrical signal is its weak amplitude ($\sim$50 μV for brain wave, $\sim$200 μV for spikes), as shown in figure 2.2. This low amplitude makes it a challenge for EEG system to acquire the desired signal without interference. Since the electrodes are placed on scalp, or subdural, it is difficult to completely eliminate other bio-signal such as electrocardiogram (ECG) signal or electromyographic (EMG) signal. Meanwhile, EEG signal can be easily biased with DC offset caused by uncontrollable such as electrode polarization and skin conditions if electrodes are on scalp. This offset could lead to signal baseline drift, which overlaps with low frequency brain signal as a noise source. In severe cases, excessive offset can saturate the circuitry of the system, further impairing signal acquisition. These characteristics of EEG signal impose strict requirements to EEG system. The low amplitude and various bio-signals necessitate high resolution to acquire and digitalize small signal variations. The presence of overlapping interferences such as low frequency bio-signals and DC offsets require a robust filtering, and high dynamic range (DR) to prevent saturation. Moreover, to capture both slow waves and fast spikes, a wide frequency range is demanded for EEG system [19].

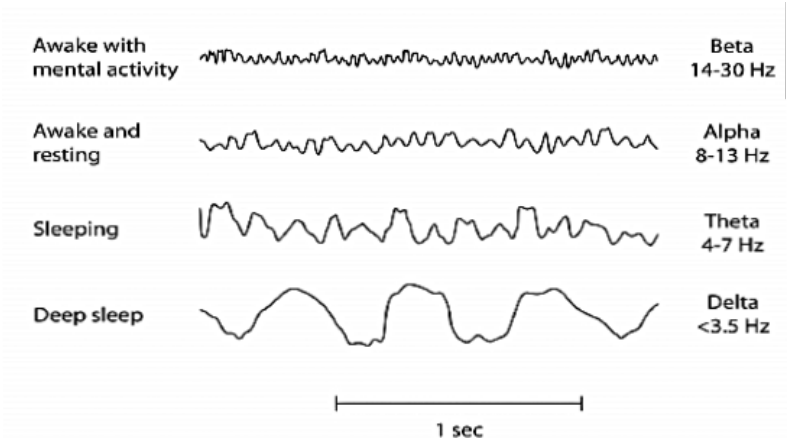

Figure 2.1: EEG waveforms for different signals (Source: [20]), Beta, Alpha, Theta and Delta

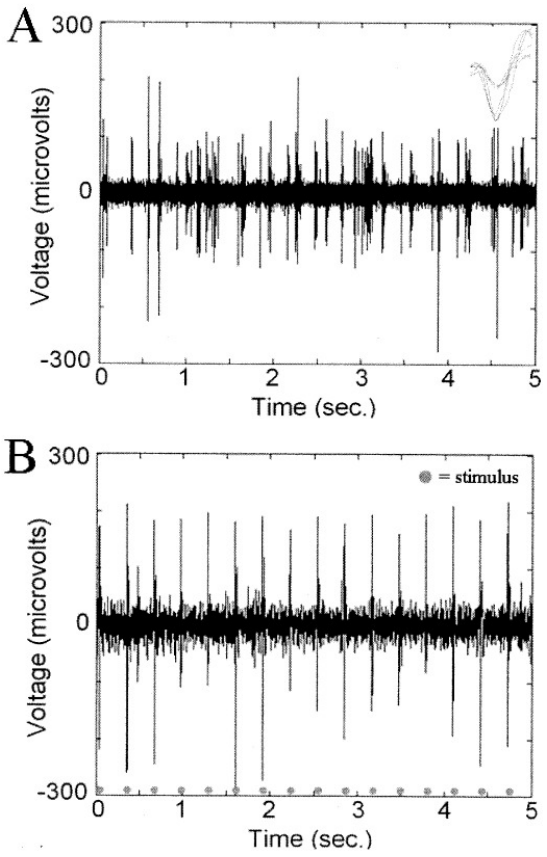

Figure 2.2: EEG signal recordings (Source: [21]). A and B are recordings at A: Postoperative Day, B: 45 Days after. The signal spikes are presented.

2.1.2 AFE and Sigma-Delta ADCs

As the concept of brain–computer interface (BCI) continues to develop rapidly, the demand of high performance EEG system is increased. BCI systems rely heavily correctly acquired and processed brain signal to enable interact between human and external device. Moreover, for clinician, accurate acquired signal is required to diagnose neurological disorders such as epilepsy, sleep disorders, and brain injuries. However, the weak amplitude and highly vulnerable to noise of EEG signals have posed significant challenges for their acquisition as discussed before. These challenges leads to the importance of a robust analogue front-end (AFE) system, which plays a critical role as the input port of EEG system, ensuring the weak EEG signals are filtered, amplified, and digitized with high fidelity and proper amplitude for follow-up applications [22].

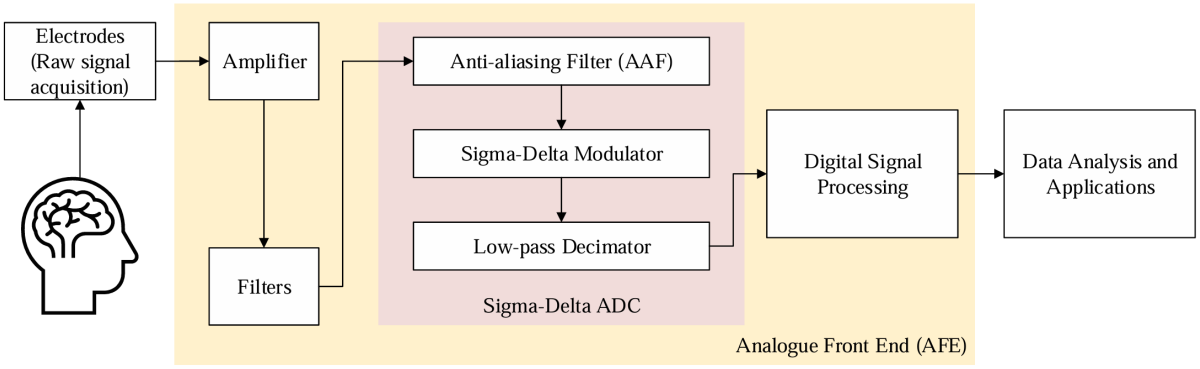

Figure 2.3: Block diagram of EEG system for brain–computer interface (BCI) purpose

Figure 2.3 shows the signal processing pathway of an EEG system, with AFE illustrated in detail. The amplifier block, typically implemented with instrumentation amplifier (IA). Instrumentation amplifiers are designed to perform high input impedance and low output impedance, which helps the IA prevents loading effect and draws most of the signal current from the electrodes, and send the well amplified signal to filters without significant voltage drops or distortion. Additionally, IA has excellent Common-Mode Rejection Ratio (CMRR) to mitigate the DC offset problem mentioned before. Filters and digital signal processing (DSP) unit present in figure 2.3 remove noise in analogue and digital stages. For the filter stage after amplifiers, it could attenuate unwanted signals such as powerline noise, EMG and ECG signal, in some specific applications the bandwidth and gain are adjustable for different target signals [23]. The DSP stage offers digital signal filtering and other signal processing for different interests, such as amplitude measurement, Fourier transforms and wavelet analysis.

In the central of the AFE, the Sigma-Delta ADC plays the crucial role of analogue to digital

conversion. A typical Sigma-Delta ADC includes an anti-aliasing filter (AAF), a Sigma-Delta modulator (ΣΔM) and Low-pass decimator. The AAF is used to prevent any input signal higher than the target bandwidth pass on to Sigma-Delta modulator (ΣΔM) and interferes output. As an oversampling ADC, Sigma-delta ADC operates at higher sampling frequency (f_s) as the Nyquist frequency (f_N) will be much higher the target signal.

In a standard Nyquist-rate ADC, quantization noise power is evenly distributed across the frequency range of $\pm f_s/2$. Therefore, as f_s is significantly increased and the quantization noise power remains constant, the power density of quantization noise power is reduced as 2.4 shown. With lower quantization noise power density, noise in signal band of interest is reduced as filter can be applied to cut-of any out-band signal.

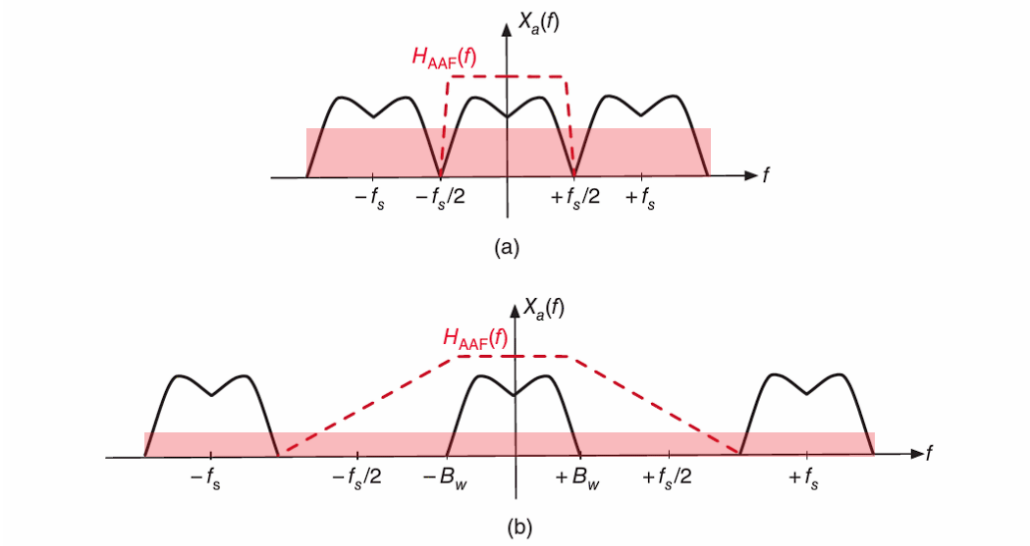

Figure 2.4: Uniformly distributed quantization noise power is re-distributed as f_s increased, lead to a lower noise power density. X_f is noise power density

2.1.3 Principles and Topologies of Sigma-Delta Modulators

The Sigma-Delta modulator (ΣΔM) is the key component in Sigma-Delta ADC to achieve high resolution and low-noise signal conversion. By employing oversampling and noise shaping, quantization noise can be pushed out of the signal band to enhance signal-to-quantization-noise ratio (SQNR) in desired signal band.

As discussed near the end of the section 2.1.2, oversampling contributes to reduce in-band noise (IBN) by re-distribute quantization noise across a wider bandwidth. Ideally, the effect of employing oversampling can be estimated mathematically. Assume an N-bit quantizer, its step

of quantization (the difference between 2 adjacent output level), Δ can be expressed as Eq.(2.1), as R refers to the output range of the quantizer.

$$\Delta = \frac{R}{2^N - 1} \tag{2.1}$$

Consider the input has enough length and the quantization error e_q is uniform, this leads to a constant probability distribution as express in Eq.(2.2). As this quantization error is distributed in the bandwidth of quantizer, the quantization noise power spectral density, $S_{E,q}$ can be calculated as Eq.(2.3). Therefore, the IBN from quantization IBN_q can be obtained by integrating $S_{E,q}$ through the signal bandwidth B_w Eq.(2.4), which suggests that the IBN from quantization can be significantly reduced by increasing oversampling ratio OSR.

$$\overline{{e_q}^2} = \int_{-\infty}^{+\infty} {e_q}^2 PDF(e_q)\, de_q = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} {e_q}^2\, de_q = \frac{\Delta^2}{12} \tag{2.2}$$

$$S_{E,q} = \frac{\overline{{e_q}^2}}{f_s} = \frac{\Delta^2}{12 f_s} \tag{2.3}$$

$$\text{IBN}_q = \int_{-B_w}^{+B_w} S_{E,q}(f) df = \int_{-B_w}^{+B_w} \frac{\Delta^2}{12 f_s} df = \frac{\Delta^2}{12\text{OSR}} \tag{2.4}$$

Exception of oversampling, $\Sigma\Delta$M implies noise shaping by integrators. An integrator accumulates input signal over time while functioning as a low-pass filter to average the signal, thus enables noise shaping. Quantization noise will be shaped by a transfer function which only affect on this noise, commonly referred as noise transfer function (NTF). Figure 2.5 shows a simple $\Sigma\Delta$M with one delaying integrator, if the integrator is assumed to have a transfer function $H(z)$, the output in z-domain, $V(z)$, can be expressed in Eq.(2.5). Meanwhile, by Figure 2.5, Eq.(2.6) is established.

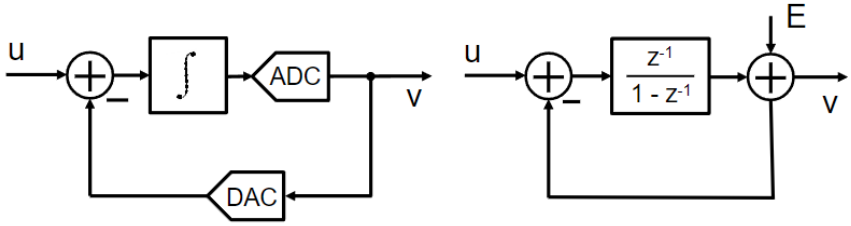

Figure 2.5: Block diagram and flow chart of a $\Sigma\Delta$M with one integrator

$$\begin{aligned} V(z) &= H(z)(U(z) - V(z)) + E(z) \\ V(z) &= \frac{H(z)}{1 + H(z)}U(z) + \frac{1}{1 + H(z)}E(z) \end{aligned} \tag{2.5}$$

$$\begin{aligned} v &= \frac{z^{-1}}{1 - z^{-1}}(u - v) + E \\ V(z) &= z^{-1}U(z) + (1 - z^{-1})E(z) \end{aligned} \tag{2.6}$$

From Eq.(2.5) and Eq.(2.6), the signal transfer function (STF) and NTF can be express as in Eq.(2.7), and the mechanism of noise shaping is revealed. Take square of STF and NTF which reflect the signal power, shown in Eq.(2.8). The square of STF suggest the signal is not affected by the integrator, while the square of NTF, illustrated in figure 2.6, indicates the quantization noise is pushed to higher frequency.

$$\begin{aligned} STF(z) &= \frac{V(z)}{U(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \\ NTF(z) &= \frac{E(z)}{U(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} = (1 - z^{-1})^L \end{aligned} \tag{2.7}$$

$$\begin{aligned} |NTF|^2 = |1 - z^{-1}|^2 = |1 - e^{-j\omega T}|^2 = (2\sin(\frac{\omega T}{2}))^2 \\ |STF|^2 = |z^{-1}|^2 = 1 \end{aligned} \tag{2.8}$$

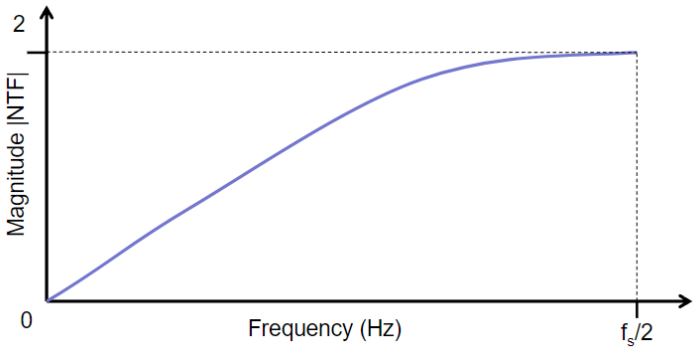

Figure 2.6: Magnitude of |NTF| versus frequency

Combining the affects of oversampling and noise shaping in Eq.(2.3) and Eq.(2.8), the total IBN by quantization can be estimated. As shown in Eq.(2.9), increasing OSR exponentially reduces IBN_q, highlighting OSR a crucial design parameter. Similarly, the order of modulator L determines steepness of noise shaping, quantified by 20 dB/decade per order. However, high OSR and L could raise challenges against system stability, energy-efficiency and other performance metrics, leads to requirements of balancing these parameters in order to achieve optimal performance based on the application's requirements.

$$\text{IBN}_q = \int_{-B_w}^{+B_w} S_{E,q}(f)|\text{NTF}(f)|^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}} \tag{2.9}$$

The trade-offs on OSR and modulator order L indicate the need for choosing parameters carefully in ΣΔM design. However, to achieve optimal performance requires not only well-designed parameters, an appropriate topology could also affect the performance of the modulator to a large extent. Commonly used ΣΔM topologies higher orders includes Cascade of Integrators with Feedback (CIFB), Cascade of Integrators with Feed-forward (CIFF), Cascade of Resonators with Feedback (CRFB) and Cascade of Resonators with Feedforward (CRFF), with their unique design in integrators/resonators and loops to feedback or feed-forward, while Multi-Stage Modulators (MASH) design and single-stage (one integrator) modulator design can also be found in some design [24]–[27]. Comparison between these ΣΔM designs is listed in Table 2.2. The implementation of ΣΔM in time domain can be categorized to Discrete-Time (DT) and Continuous-Time (CT). DT ΣΔMs rely on Sample-and-hold (S/H) of Switched-capacitor (S-C) circuits with integration and feedback while CT ΣΔMs direct process continuous signals with CT integrator. Comparison between DT and CT is given in Table 2.1. Later chapter provides a detailed analysis of the topology and the trade-offs between DT and CT to justifies the design choice.

Table 2.1: Comparison Between Discrete-Time and Continuous-Time Sigma-Delta Modulators

Feature	**Discrete-Time (DT)**	**Continuous-Time (CT)**
Sampling	Sampled using switched-capacitor circuits	Operates directly on continuous signals
Speed	Limited by clock jetter	High
Power Efficiency	Higher power consumption due to switched-capacitor circuits	More power-efficient at high frequencies
Linearity	Better control over coefficients	Requires carefully coefficient tuning
Clock Jitter Sensitivity	Highly sensitive to clock jitter	Robust to clock jitter as only DAC is affected
Design Complexity	Simple, well-established	Complex, especially in higher-order designs

Table 2.2: Comparison of Sigma-Delta Modulator Designs

Feature	**Single-Stage**	**Multi-Order (CIFF, CIFB, etc.)**	**MASH (Multi-Stage)**
Noise Shaping	Low, +20db/*dec*	+20db/*dec* for each order	+20db/*dec* for each order for each modulator
Resolution	Very limited	High resolution can be achieved with higher orders	High resolution with multiple stages and cascaded modulators
Complexity	Simple	Depends on order and feedback/feed-forward structure	High, due to coordination for cascaded stages
Stability	Stable	Stability decreases with increasing order	Stable, as stages operates independently and easier pole optimization
Power Consumption	Ultra low	Increases with higher order and larger signal swings	Similar to multi-order, power consumption depends on stage design
Challenges	Performance is limited	Stability for high order design, signal saturation, component mismatch	High design complexity, very sensitive to component mismatch
Use case	Wearable devices	Commonly used for various purpose	Resolution-sensitive e.g., clinical diagnostics, BCI

2.2 State-of-the-Art Studies

To understand advanced progress in ΣΔM designs, it is crucial to review recent state-of-the-art researches. These studies emphasizes the evolution of modulator design, with various topologies and significant improvements in power efficiency, noise performance, and stability. In EEG purpose design, the development on topologies such as CIFB and CIFF provides a simple and practical solution for most application due to the generality and scalability of multi-order modulator, while MASH designs further help to lessen the challenge on system stability and harmonic distortion when designing multi-order modulator [28], [29]. Table 2.3 summarizes a number of recent studies on EEG ΣΔM with their key performance metrics. As seen in Table 2.3, DT ΣΔMs are the most favoured design option due to their simplicity on well-established design method and high-resolution capabilities. However, CT ΣΔMs have unique advantages on noise reduction [30] and low power consumption [31].

While these studies demonstrate significant progress, challenges remain in when designing a low-power consumption ΣΔM for EEG applications as problems with topology, stability and noise performance are usually discovered in circuit-level design stage. Motivated by the limitation of simulating in block-level, this work proposes a novel ΣΔM design in block-level with detailed

simulation focused on noise and stability, which could further simplify the process of designing ΣΔMs.

Table 2.3: Recent researches on ΣΔM for EEG purpose

Metrics	Architecture	Process [μm]	f_s [kHz]	B_w [Hz]	DR [dB]	SNDR [dB]	Power [μW]	FoM_S [dB]
Sensors'23[32]	DT ΣΔM	0.18	1024	1500	126	110	1600	177.8
Electronics'23 [30]	CT ΣΔM	0.05	102.4	100	137	136*	2310	188
Sci. China'22[33]	DT ΣΔM	0.18	1024	125	124	82.6	2750	170.6
IEEE'21[34]	DT ΣΔM	0.11	512	2000	96.3	94*	62.43	171
IEEE'21(2) [35]	DT ΣΔM	0.18	12800	25000	-	100.5	1280	163.4
IEEE'14[31]	CT ΣΔM	0.18	256	200	-	57.9	1.614	-
IEEE'09[36]	DT ΣΔM	0.18	2000	16000	-	63.4*	18.1	171

*SNR is presented instead of SNDR

2.3 Motivation and Previous Work

As the process of designing ΣΔMs tend to be more systemic with proven procedures, simulations at block-level and circuit-level could provide valuable insight of actual modulator which help to avoid repeated iterations and revisions after silicon prototypes are found to be deficient. In circuit-level simulations, it is possible to estimate detailed noise power from different sources including Operational transconductance amplifier (OTA) noise, integrator's noise and other noise due to non-linearity of circuit. In additional of quantization noise caused by DAC non-linearity, noise from these sources dominate the power of noise floor, while it is not modulated by noise shaping [37]. This part of noise from circuit non-linearity contributes significantly to eventual noise performance of the modulator, however, as circuit non-linearity is intrinsic, once the parameters and topology used are determined, limited effect from circuit optimization can be obtained. This leads to 2 methods for achieving desired performance when circuit is proven to be unsatisfying: Iterative redesign on block-level parameters, such as increasing modulator order; Or re-engineering on subsystem such as OTA.

As discussed in previous parts, increasing L and OSR significantly reduces in-band quantization noise, which help to improve overall noise performance. However, modifications on block-level requires redesign circuit, and additional integrators are considered as extra noise sources thus iteration on noise analysis is demanded. Though block-level simulation could give a good insight of the effect of noise shaping and system's stability, due to the sensitivity of modulator to

mismatch and component variation [38], it is difficult to design modulator based on existing data and cases that is highly reliable to fulfil noise performance requirements. Meanwhile, increasing L and OSR also increases power consumption and circuit design complexity, which is difficult to be capture in block-level simulation. Nonetheless, despite all the limitation on block-level simulation, it is still the most appropriate starting point of $\Sigma\Delta$M design.

The other approach of circuit supplement is to improve or rework circuit component, especially OTA design on transistor-level. By increasing Gain-Band-width(GBW) and stew rate, reducing settling time, OTA can handle rapid changes signal input while provide enough amplification, thus allow higher OSR, meanwhile, increasing large transistor dimension can reduce flicker noise, and improve overall integrator performance. Additionally, enhanced CMRR can further improve circuit's resistance to common-mode noise such as powerline noise discussed before. Nonetheless, improved OTA performance come with trad-offs, leading to increased power consumption and complexity, therefore parameter of OTA must be carefully considered in practical to ensure desired performance while avoid over-engineering. In following chapter, these trad-offs and design justifications will be discussed.

In order to prevent repetitive iteration and optimization, and improve methodologies and workflows for $\Sigma\Delta$M design, this study proposed a refined design workflow in Figure 2.7 (b). In previous phase of this study [39], a standard development method for $\Sigma\Delta$M, shown in Figure 2.7 (a) is used referring to Schreier [37]. limited by project timeline and experience, phase one work only achieved a block-level simulation, and proved the proposed modulator is functional with good stability and satisfying SQNR. Phase on study also provided some rough estimation on modulator SNR but the focus of phase one work is to build a operable model with proposed topology as a test-bench. In this study, though CIFF topology is still the key work, a new method of design, Figure 2.7 (b), is adopt which intend to work both on block-level design and component requirement assumption in parallel. This aims to simplify design process by using block-level simulation result to infer required performance of components such as OTA, then iterate component parameter with more realistic simulation as the performance of component is obtained. Once the simulation shows the metrics of modulator could fulfil the requirement of signal acquisition and conversion, more straightforward and manageable circuit-level and transistor-level design can be performed. Detailed explanation of this proposed workflow is provided in later chapters, and a comparison between work for phase one and phase two is given is Table 2.4.

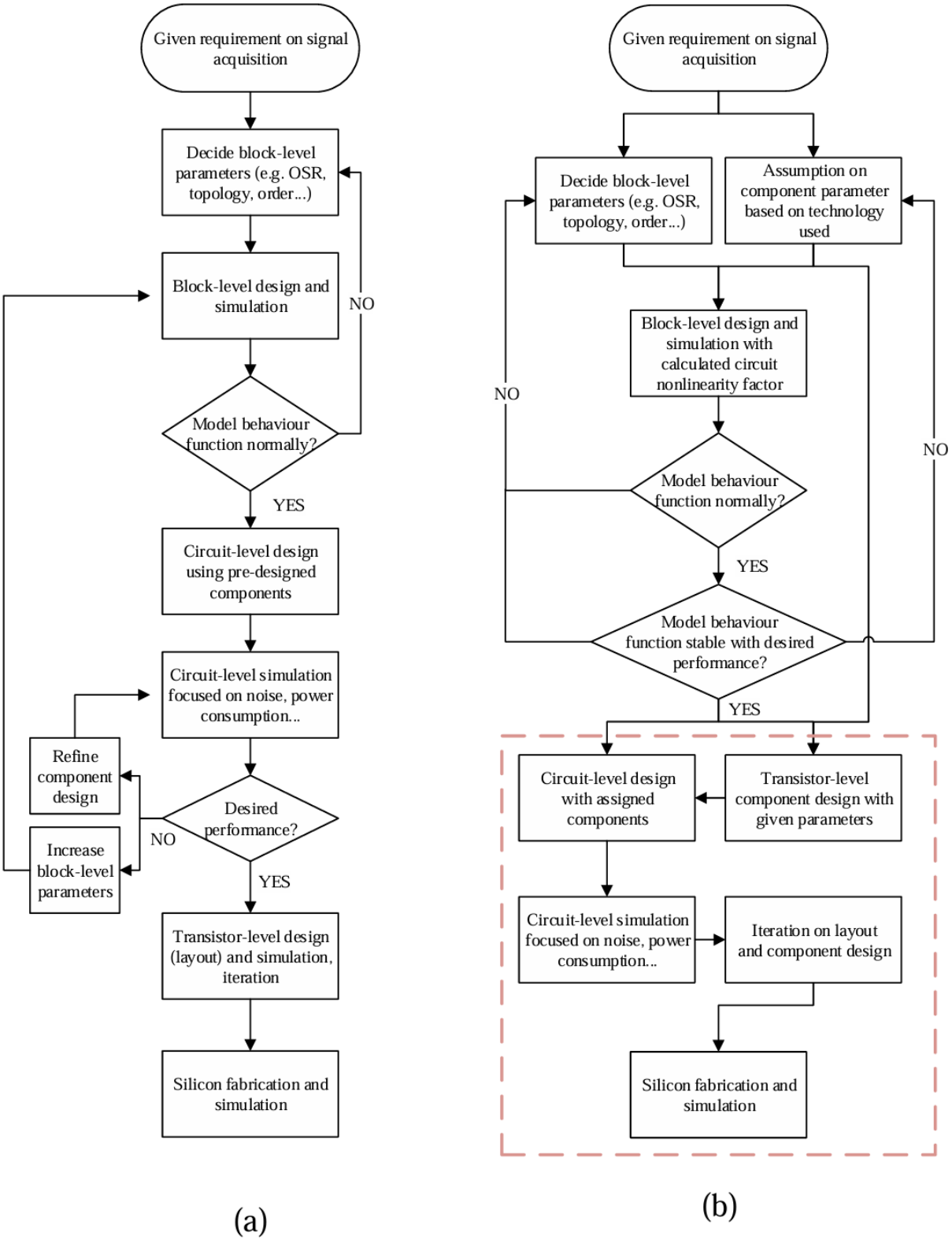

Figure 2.7: Design workflow of ΣΔM, (a) Standard design workflow (b) Proposed design workflow

Table 2.4: Summary on comparison between phase one and phase two work

	Phase One	Phase Two
Block-level design	✓	✓
Block-level simulation	✓	✓
Topology	CIFF	CIFF
Order	4	3
f_s	2.048MHz	1.024MHz
OSR	1024	512
SQNR calculation	✓	✓
Amplitude/DC gain sweep	✓	✓
Stability with different inputs		✓
Circuit non-linearity noise		✓
Guiding parameter for OTA		✓
SNR estimation		✓

2.4 Summary

In this chapter, a comprehensive review of the theoretical background and technical challenges to ΣΔM design is provided. Introduction on EEG signal, equipment such as BCI and AFE are given with discussion on their characteristics and connections between. The chapter delved into the principles of ΣΔM with key concepts such as oversampling, noise shaping, and the significance of STF and noise transfer function (NTF) with their affect on quantization noise. Various types of modulator topologies are reviewed with advantages and trade-offs highlighted.

State-of-the-art studies are reviewed, providing insight of advancements in modulator design, power efficiency, and noise performance in current studies. Trends such as CT ΣΔM, MASH design and ultra-low power designs are discussed with their limitations, while traditional high order ΣΔM with CIFF or CIFB design still being the most popular design choice.

Finally, the inefficiency of standard ΣΔM design workflow is explained, which leads to the motivation for this study, providing a refined workflow to reduce iteration in late design stage like circuit-level and transistor-level stage. Previous work in phase one is addressed to be limited with lack of detailed analysis in non-linearity noise and as this work adopted the proposed workflow, a more completed and realistic simulation could be provided.

Chapter 3

System Design

In previous chapter, the significance of Sigma-Delta modulator ($\Sigma\Delta$M) in developing an efficient analogue front-end (AFE) for Electroencephalography (EEG) signal acquisition systems is discussed, and key challenges in EEG system design, such as achieving high resolution, stability, and low power consumption with minimized power consumption and noise are addressed. Building on the insights from literature review, this chapter provides approach to the proposed design in a systematic way with a refined workflow. In preliminary stage, modulator parameters are defined refer to well-established calculations and empirical charts, meanwhile, Cascade of Integrators with Feed-forward (CIFF) is adopted as its outstanding performance at current application. Subsequently, synthesis of block-level is provide with the help from software toolbox, and the block-level model is implemented as test-bench. As the block-level design progresses, the focus shifts to simulating non-linearities introduced by the circuit components, especially by Operational transconductance amplifier (OTA). Combining requirement on system performance and Complementary Metal Oxide Semiconductor (CMOS) technology parameters, OTA design requirement is established.

The structure of this chapter is outlined as follows: Section 3.1 presents the preliminary design, including proposed workflow, the selection of modulator parameters and topology. Section 3.2 focuses on the synthesis of the NTF and model implementation. Section 3.3 evaluates the affect of non-linearities through calculations with CMOS parameters, and provide OTA design parameters. Finally, Section 3.4 summarizes the design findings and highlights the outcomes.

3.1 Preliminary Design

3.1.1 Design workflow

The design of ΣΔM involves refinement and iteration on different levels and stages, each aimed at providing the desired performance for signal acquisition. Figure 2.7 presents two distinct ΣΔM design workflows: the conventional design workflow (a) and the refined workflow (b) proposed in this work.

- Conventional Workflow

  As illustrated in Figure 2.7 (b), traditional design flow begins with defining the block-level parameters such as oversampling ratio (OSR), topology, and order. This can be completed with calculations based on Sigma-Delta modulation such as Eq. 2.9, and with more efforts mathematics derivation, it is possible to use dynamic range (DR) to make presumptions on modulator parameters. After modulator parameters is defined, block-level simulation can be performed in software tool, as MATLAB in this case. Once the model behaves as expected, circuit-level design design is processed. As in this stage, metrics such as noise, power consumption, and linearity is not ready as no circuit-level simulation is done, pre-designed components are utilized to complete circuit model and process circuit-level simulation. Commonly, as previous assumptions and designs do not take circuit non-linearity into account, the performance of modulator is often below expectation. As the desired performance is not met, adjustments are made by refining the component design or increasing block-level parameters as performed before, and this cycle repeats until all performance requirements are satisfied. Subsequently, design moves to transistor-level engineering for layout with simulation, once the design is proved to be robust and fully-completed, design work advances to silicon fabrication and validation.

  This approach, while it is comprehensive and follows a intuitive flow, is prone to inefficiencies due to the lack of integration between block-level and circuit-level design presumption. Design iterations at later stages (e.g., circuit and transistor levels) are frequently encountered as performance is not met, result in significant delays and increased complexity.

- Proposed Workflow

  The refined workflow focuses the inefficiencies of the conventional process discussed, and to reduce iterations at later stages, integration of circuit-level nonlinearity factors during the block-level design stage is introduced. In this approach:

1. Block-level parameters are defined with calculations and assumptions about circuit components based on the CMOS chosen technology and other circuit parameters.
2. Block-level simulations incorporate these nonlinearity factors into account, providing a more accurate behavioural model with more realistic simulation result.
3. Block-level simulation results lead to iterations on circuit component parameters, eventually to technical requirements for component design.
4. This ensures that the performance and functional stability of the model is tested earlier in the process, reducing the risk of major revisions and limit the complexity of refinement at later stages.

Once the block-level design is validated, the workflow transitions into circuit and transistor-level simulations, with pre-assigned components and calculated parameters. With benefits from modern design technique, such as adopting Electronic Design Automation (EDA) tools, the red dashed area in Figure 2.7 can be simplified to streamline design. For example, as requirements for OTA is given, g_m/I_D method can be deployed with EDA assisted. This approach enables a rapid exploration of transistor dimensions, biasing conditions, and process variations, which reduces resources and complexity while providing satisfying performance metrics [40]. This refinement minimizes unnecessary iterations and optimizes the overall design process, leading to a more efficient and predictable design.

In comparison, the proposed workflow significantly reduces the iteration cycles in block-level and circuit-level design stage by incorporating realistic circuit-level factors earlier in the process. This not only shortens the design timeline and reduces design cost, but also improves the likelihood of meeting performance targets in the first pass at each stage.

3.1.2 Defining modulator parameters

The performance of a ΣΔM is fundamentally limited by by the constraints of block-level design and parameters, these includes Oversampling Ratio (OSR), modulator level (L), quantizer bit-length (N) and signal bandwidth (B_w). In the initial stage of design, parameter selection is guided by theoretical calculations and charts to ensure the design satisfies application's requirements. Based on the mechanism of oversampling and noise shaping, a peak signal-to-quantization-noise ratio (SQNR) can be calculated with specified OSR, L, and N, as seen from Eq. 3.1 with detailed derivations given in Appendix A.

$$SQNR_{peak} = 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}(\text{OSR})^{2N+1}\right) \tag{3.1}$$

Instead of selecting parameter by directly calculate expect SQNR, empirical chart and figure can assist design better as other negative factors are included. For example, Figure 3.1 is empirical SQNR limits for ΣΔM with 1-bit quantizer presented by Schreier and Temes [37], which gives expectations of SQNR lower than calculation result as a number of non-linearity factors are considered such as components mismatch.

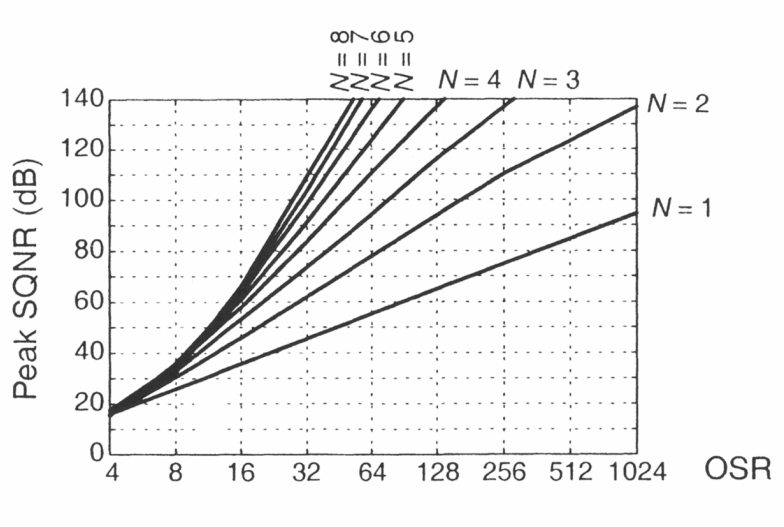

Figure 3.1: Empirical SQNR performance with 1-bit quantizer [37]

As the proposed design is aimed to operate at low frequency band, it is reasonable to take increasing OSR as the main approach to increase SQNR, with crystal oscillators providing sampling clock. In this case, lower order and 1-bit quantizer are adopted as low order modulator tends to have better stability and lower power consumption, and 1-bit quantizer significantly reduces system complexity, while providing immunity to digital-to-analogue converter (DAC) capacitor mismatch. Overall, the parameter specification is given in Table 3.1.

Table 3.1: Pre-designed specifications of the ΣΔADC

Specification	
Architecture	CIFF (modified)
Modulator Order	3
Quantizer Bits	1
Oversampling Ratio (OSR)	512
Sampling Frequency (F_s)	1.024 MHz
Input Bandwidth	1000

3.1.3 CIFF topology

When employing a high-order ΣΔM, selecting an appropriate topology is essential to ensure system stability and efficiency. In this section, different topologies are compared and discussed, including Cascade of Integrators with Feedback (CIFB), Cascade of Integrators with Feed-forward (CIFF), Cascade of Resonators with Feedback (CRFB) and Cascade of Resonators with Feed-forward (CRFF), finally, CIFF is selected as the proper topology for the proposed system.

- Comparison between integrator-based structures and resonator-based structures

  Integrator-based structures, including CIFB and CIFF, are commonly preferred in EEG ΣΔM design compare to resonator-based structures such as CRFB and CRFF, due to their built-in limitations.

  The noise shaping mechanism of resonator-based structures rely on resonance phenomena, and the transfer functions of resonator typically exhibit bandpass characteristics. Therefore, in resonator-based design, resonant frequencies are placed out of signal band at noise transfer function (NTF), acting low-pass filters and push quantization noise out of signal band. However, due to the bandpass characteristics, when input (noise) frequency is low, the resonators need to be designed with very low resonant frequencies, which leads to design with high capacitance or inductance and increased silicon area and power consumption. Meanwhile, by comparing NTFs between resonator and integrator, it is found that in lower frequency, resonator is not effective as integrator, which is proved in Figure 3.4, as NTFs of resonator and integrator are sketched.

- Comparison between feedback and feed-forward structures

  In feed-forward structures, as shown in Figure 3.2, integrator on each stages contribute to the input signal of quantizer by assigned feed-forward paths with independent gain block on each path. In CIFF topology, by carefully optimize gain of each block, the output swing of the each integrator can be distributed and balanced, then sum to full-scale signal swing as input of the quantizer. In CIFB, as the quantizer only receive signal from the last integrator, all the integrator one the chain must operate at full-scale output swing to achieve a maximum dynamic range (DR). By adopting CIFF, power consumption of the modulator is reduced by lower output swings, and the risk of integrator saturation is also reduced.

  Additionally, to obtain the quantization error, output signal from quantizer is converted back to analogue signal by DAC in feedback loop. Instead of having multiple feedback loops to each integrator as CIFB structure shown in Figure 3.3, CIFF structure only have one feedback loop. Reduction on feedback loop can further cut power consumption, and for multi-bits quantizer

case (see in Further work), reduction on number of DACs can improve system immunity to DAC component mismatch.

To further improve the ΣΔM performance, the proposed CIFF topology is refined with an additional feed-forward loop, which directly transmit the input signal to the quantizer as shown in Figure 3.2. As Schreier and Temes [37] discussed, by subtracting $v(n)$ from the input, extracted quantization noise is sent to integrators instead of the input signal. Therefore, the input of the first integrator only consists shaped quantization noise, thus less harmonic distortion can be achieved.

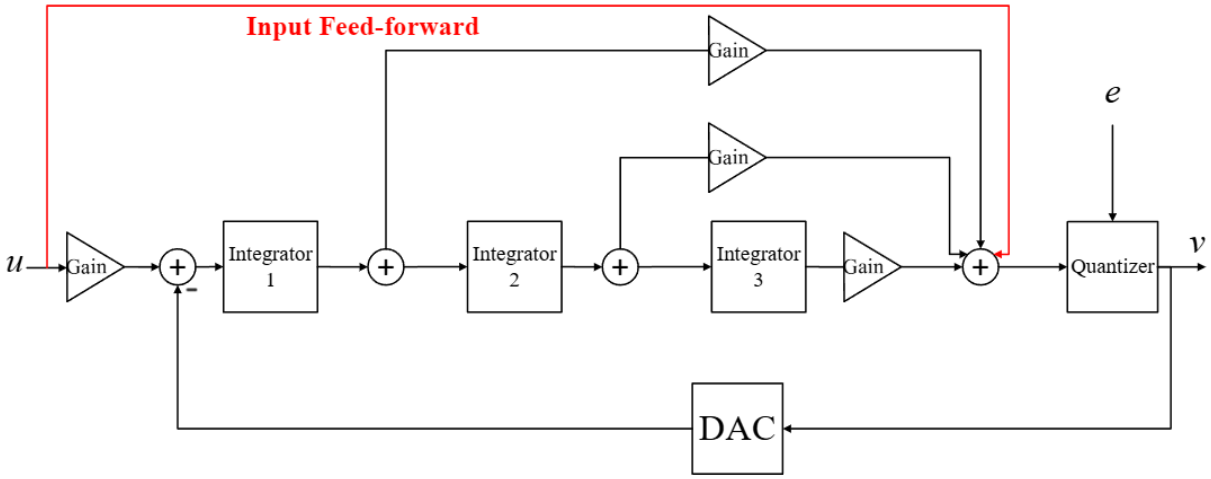

Figure 3.2: Proposed CIFF topology

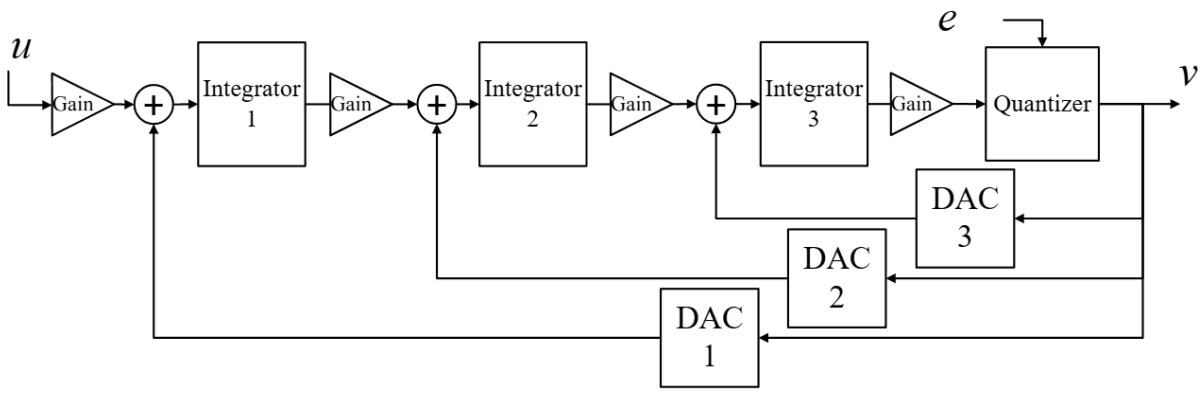

Figure 3.3: Conventional CIFB topology

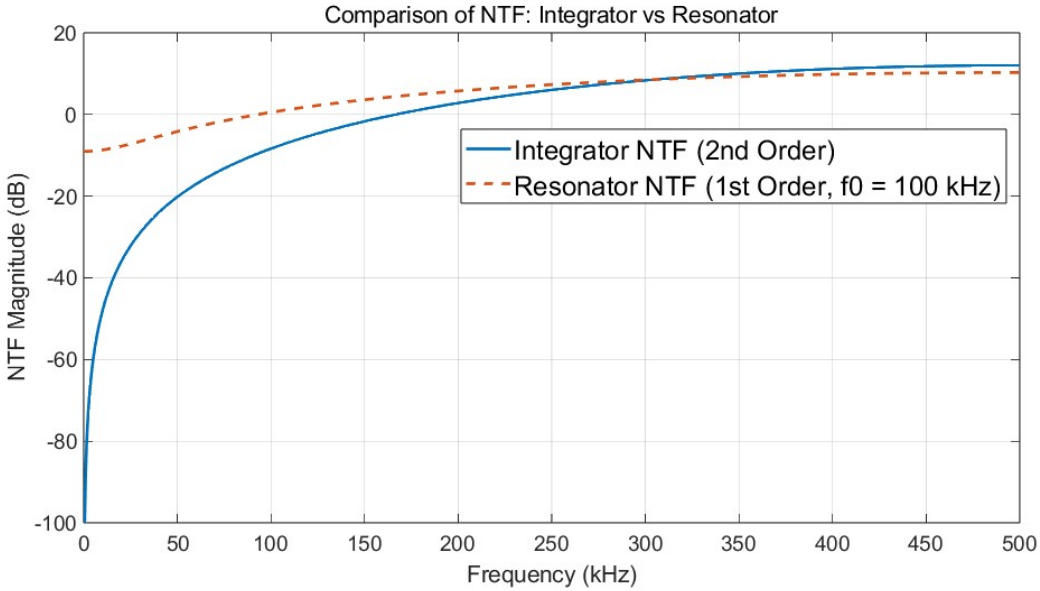

Figure 3.4: NTFs of resonator and integrator

3.2 Design synthesis

3.2.1 NTF synthesis and calculation

With previous design parameters, the NTF of proposed ΣΔM is obtained with MATLAB Simulink, Delta-Sigma Toolbox by Schreier and Temes [37], as presented in Eq. 3.2. And the ratio of NTF is given in Eq. 3.3. By evaluating NTF ratio at DC level, the result, -13.57 dB suggest the simulated SQNR will be 13.57 dB lower than calculated peak SQNR by Eq. 3.1. Figure 3.5 presents the frequency response of NTF, indicating the ΣΔM exhibits a 60 db/dec.slope for noise shaping. Furthermore, by integrating the square of NTF in modulator bandwidth, the calculated total quantization noise in-band is -140.2 dB, and as operation frequency increases indefinitely, NTF's frequency response is stabilized at 3.52 dB.

$$H_{\mathrm{NTF}}(z) = \frac{(z-1)(z^2-2z+1)}{(z-0.6694)(z^2-1.531z+0.6639)} \tag{3.2}$$

$$r(z) = \frac{(z-0.6694)(z^2-1.531z+0.6639)}{z^3} \tag{3.3}$$

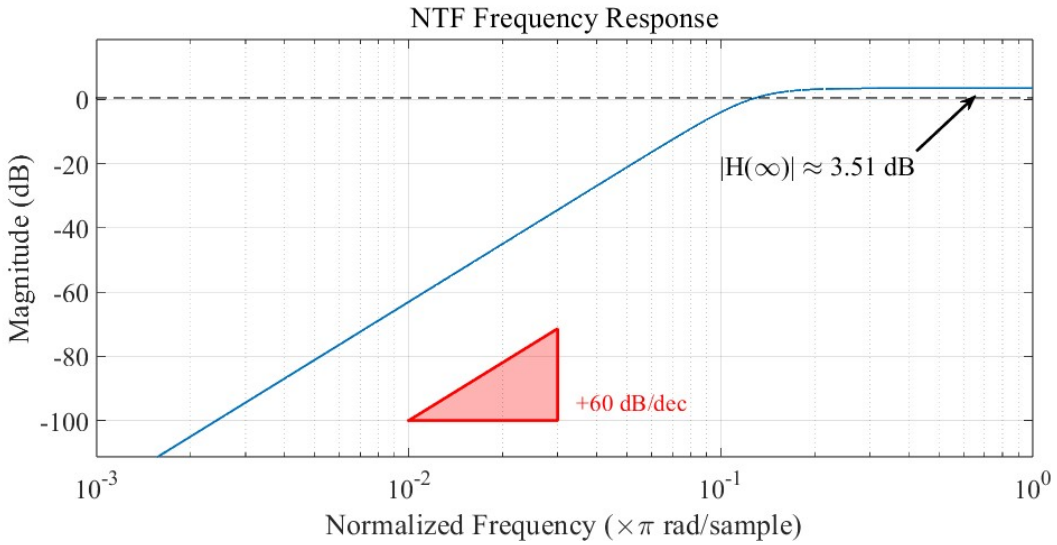

Figure 3.5: Frequency response of NTF

3.2.2 Model implementation

Based on the given specifications, a modified CIFF architecture is adopted, as the Simulink model illustrated in Figure 3.6. The coefficients for each gain block are calculated with Schreier's Delta-Sigma Toolbox [41], the resulting values listed in Table 3.2. To clarify, gain coefficients with a value of 0 indicate the corresponding connection is absent.

Table 3.2: Results of gain block coefficients: a, b, c, and g

Coefficient	1	2	3	4
a	2.0667	2.5914	2.5426	-
b	0.3870	0	0	1
c	0.3870	0.2873	0.1555	-
g	0	-	-	-

In order to fully test the performance of the model, other blocks to support simulation are not included in Figure 3.6, these includes signal input selection block, integrator non-linearity noise block, dither block and output capture block. These blocks with corresponding features are discussed later.

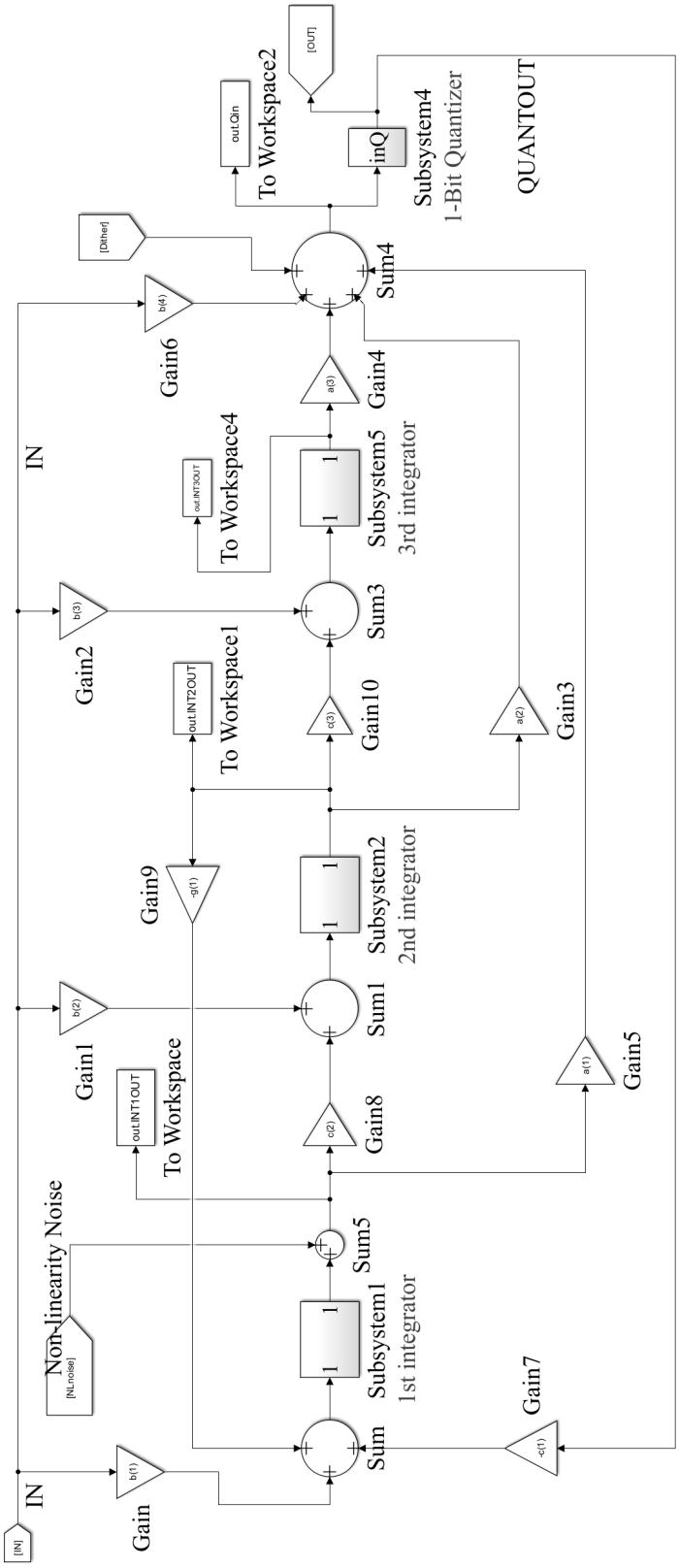

Figure 3.6: Simulink model of proposed design

3.3 Non-linearity simulation

3.3.1 CMOS technology and OTA parameter

The choice of CMOS is crucial in determining the performance and feasibility of OTA in integrators. In this study, CMOS technology defines the noise performance of the OTA and more important, CMOS process parameters including transistor dimension and oxide thickness can directly affect on basic performance of the OTA, including Gain-Band-width(GBW), slew rate, power consumption and chip area. These parameters must align with the ΣΔM design principles, ensuring enough signal amplification while minimizing non-linearity noise and distortion that could degrade the modulator's resolution.

Non-linearity in OTA and CMOS components are often resulted from transistor-level mismatches and intrinsic characteristics due to process variations such as Random Dopant Fluctuations (RDF) and Line-Edge Roughness (LER). These non-linearities significantly impacts the ΣΔM performance, and since these non-linearities are introduced fabrication by process variations, it is not possible to be fully controlled. Simulating these non-linearities with parameters from realistic CMOS process can enable more accurate estimation of their effects on integrator noise, gain, stability, and noise shaping, therefore refines design parameters to avoid iterations.

3.3.2 Integrator non-linearity simulations and performance trade-offs

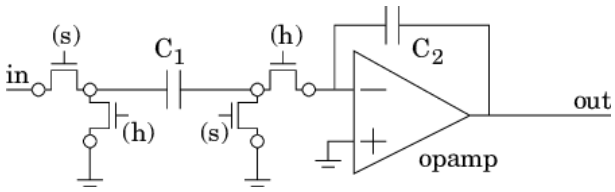

Figure 3.7: Switched-capacitor (S-C) based integrator

As the proposed modulator adopted a Discrete-Time (DT) design, integrators are implemented with S-C circuits as Figure 3.7 shown. The S-C integrator operates in two phases: (a) In sampling phase, switches (s) is closed to for C_1 Charing thus allow sampling, while switches (h) are open. (b) In integration phase, switches (h) are closed, charge transferred from C_1 to C_2, the OTA would adjust the negative input equal to positive input to ensure charge is transferred completely. In this circuit, the output voltage is proportional to the input voltage, scaled by the ratio of C_1 over C_2. As the input signal is continuous, and the circuit operates on clock-controlled switches while behaving characteristic of delay, the circuit is considered as integrator, its discrete-time difference equation is given in Eq. 3.4.

$$V_{out}[n] = V_{out}[n-1] + \frac{C_1}{C_2} \cdot V_{in}[n] \tag{3.4}$$

The analysis above are based on the assumption of an ideal integrator, in this work, circuit noise and OTA limited gain are consider. In this part, circuit noise is analysed as follows.

The gain of an OTA, A_v, as a fundamental performance metric, is mainly dictated by the transconductance g_m. Therefore, optimizing g_m is essential for both achieve enough gain and avoiding increased noise. To further discuss g_m, Eq. 3.5 gives expression of GBW, C_L represents load capacitance of OTA.

$$\text{GBW} = \frac{g_m}{2\pi C_L} \tag{3.5}$$

Meanwhile, settling time τ (Eq. 3.6) is also affected by transconductance and load capacitor. The settling time is defined as the time for OTA output to be stable, Conventionally, the settling time is less than 10% of a time period of clock signal.

$$\tau = \frac{C_L}{g_m} \tag{3.6}$$

Furthermore, the thermal noise of integrator in given by Eq. 3.7. In practical circuit, Flicker noise also affect on integrator noise, especially in lower frequency band. However, in this case, as the OSR is relatively high, noise power contributed by OTA flicker noise is ignored.

$$\begin{aligned} v^2_{Thermal,OTA} &= \frac{4kT\gamma}{g_m} \\ v^2_{Thermal,C_L} &= \frac{1}{\text{OSR}}\frac{kT}{C_L} \\ v^2_{Flicker} &= \frac{K_f}{C_{ox}WLf} \end{aligned} \tag{3.7}$$

By former calculation on total in-band quantization noise, which is -140.2 dB, it is proven that in proposed design, the quantization noise is not the primary contributor to the total noise floor. If desired Effective number of bits (ENOB) is 12-bits, or signal-to-noise ratio (SNR) of 74 dB, the noise power is $1.76 \times 10^{-8}V^2$ with full-scale output assumed to be 1 V. And with a design redundancy of 20%, this gives us a total noise power budget of $2.11 \times 10^{-8}V^2$. In order to achieve lower power consumption, 60% noise power budget is dedicated to OTA noise for lower transconductance, while thermal noise from C_L is 40% of the total noise. By Eq. 3.7, the minimum required C_L calculated below, which is a very low value and easy to achieve. In practice, 2 pF is used due to fabrication process and unavoidable parasitic capacitance, and

corresponding noise power is given.

$$C_{L,min} = \frac{1}{\text{OSR}} \frac{kT}{2.11 \times 10^{-8} V^2 \times 40\%} = 9.580 \times 10^{-16} F \tag{3.8}$$

$$v^2_{Thermal,C_L} = \frac{1}{\text{OSR}} \frac{kT}{2p\text{F}} = 1.617 \times 10^{-12} V^2 \tag{3.9}$$

By settling time in Eq. 3.6, and f_s of 1.024 MHz, the minimum transconductance required is given below, with related OTA thermal noise power calculated. The parameter γ refer to thermal noise coefficient of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). According to research by Re, Manghisoni, Ratti *et al.* [42], γ is assumed to be 2/3 as the transistors in OTA aim to operate in strong inversion mode.

$$g_m = \frac{C_L}{\tau} = \frac{C_L}{10\% \times \frac{1}{f_s}} = 20.48 \mu A/V \tag{3.10}$$

$$v^2_{Thermal,OTA} = \frac{4kT\gamma}{g_m} = 5.395 \times 10^{-16} V^2 \tag{3.11}$$

With transconductance and load capacitance, the GBW can be calculted with Eq. 3.5. The OTA's GBW in this specification is 1.630 Hz, consider the input bandwidth of 1 kHz, the OTA can provide gain $A_v = 64.24$ dB, this limitation on gain can be simulated in block-level.

Overall, with previous analysis, the non-linearities of integrator is listed in Table 3.3. These non-linearities are take into account for block-simulation after, and specifications for OTA is provided for transistor-level engineering.

Table 3.3: Non-linearities of integrator and design specifications for OTA

Non-linearities	
OTA thermal noise $v^2_{Thermal,OTA}$	$5.395 \times 10^{-16} V^2$
Load capacitance thermal noise $v^2_{Thermal,C_L}$	$1.617 \times 10^{-12} V^2$
OTA finite gain	64.24 dB @ 1 kHz
Design Specifications for OTA	
GBW	$\geq$ 1.630 MHz
Transconductance g_m (F_s)	$\geq$ 20.48 μA/V
Load capacitance (input + parastic)	2 pF
Settling time	$\leq$ 97.66 ns
Output swing	1 V
Stew rate	$\geq$ 10.24 V/μs

In the previous analysis, trade-offs between transconductance g_m, load capacitance C_L and noise were noticed. Designing OTA for ΣΔM requires carefully balancing these parameters in order to fulfil performance demands. Higher g_m can increase GBW and reduce OTA thermal noise ($v^2_{Thermal,OTA}$), but it also raises power consumption and reduces phase margin, which has major impact on system stability at higher frequency [43]. Conversely, by increasing C_L, load capacitance thermal noise ($v^2_{Thermal,C_L}$) is reduced, but it also extends settling time and reduces GBW, which results in compensating a higher g_m to ensure gain. In the proposed design, in order to provide low noise and power consumption in relatively low speed application, moderate g_m and load capacitance are adopted to offer an optimal performance.

3.4 Summary

In this chapter, the systematic design and discussion on system non-linearities of proposed ΣΔM are presented, emphasizing three key design aspects: refined workflow, CIFF topology, and non-linearity analysis.

Firstly, a refined workflow was introduced to streamline the design process. By incorporating block-level design with circuit-level non-linearity factors, performance of the model can be tested earlier in the design process, thus minimized iterations in the later design stages such as circuit and transistor layout development. Furthermore, with verified design specifications, the proposed workflow enables a rapid implementation of circuit components, and allows parallel processing of design on block-level and transistor-level.

Secondly, the proposed model employs a modified CIFF topology to optimize performance. With feed-forward structure, the output swing of integrators is reduced, thereby lowering power consumption. Gain coefficients were calculated with Schreier's toolbox, and Simulink model was implemented. Furthermore, the plots of NTF is examined and total in-band quantization noise is calculated by integration.

Lastly, a detailed non-linearity analysis was conducted in order to address critical circuit-level challenges. Integrator non-linearities including OTA thermal noise, load capacitance thermal noise and finite OTA gain were quantified for further simulation, and corresponding design specifications for OTA were provided. Trade-offs between transconductance, load capacitance, noise, power consumption and stability were evaluated to highlight the importance of optimizing design for high resolution low power application with low speed.

By integrating these design elements systematically, a solid foundation for block-level test-bench is laid, in the following chapter, the design's capability to meet EEG signal acquisition requirements will be tested and discussed.

Chapter 4

Simulation and Discussion

In previous chapter, Sigma-Delta modulator ($\Sigma\Delta$M) model with non-linearity elements were established, providing a reasonable and comprehensive expectation of the modulator performance. Building upon these model and analyses, this chapter delves into the simulation and evaluation of the model's functionality, noise performance, and stability, ensuring the proposed modulator's capability of signal acquisition. By implying MATLAB Simulink, theoretical assumptions are validated, and performance characteristics are explored.

The chapter is structured as follows: Section 4.1 focuses on the basic functionality of the model, providing simulation results of crucial operation process of the modulator. Section 4.2 investigates the noise characteristics, providing the system's performance with its signal-to-quantization-noise ratio (SQNR), signal-to-noise ratio (SNR), dynamic range (DR) signal-to-noise-and-distortion ratio (SNDR), analysing how different noise sources affects on system resolution. Section 4.3 addresses stability concerns by simulating system with extreme input signals to ensure model's ability to maintain a reliable operation under dynamic input conditions. Finally, Section 4.5 summarizes key founding in simulations with corresponding discussions and comments, thus leads to a evaluation of the modulator's performance.

4.1 Model functionality

To verify the basic operation of proposed $\Sigma\Delta$M, the primary objective is simulate modulator and focus on if desired output is obtained. A sine wave input of 100 Hz with 0.707 amplitude is applied to the modulator, the output records are given in Figure 4.1 and Figure 4.2. Figure 4.1 shows the time-domain output of the first integrator in proposed $\Sigma\Delta$M, demonstrating stable oscillations within expected integrator output swing, confirming effective signal accumulation. Figure 4.2 presents the output of the quantizer, which shows a solid output of Pulse-density

Modulation (PDM) signal. Together, these figures validate the expected behaviour of integrator and quantizer, ensuring the ΣΔM is functioning properly.

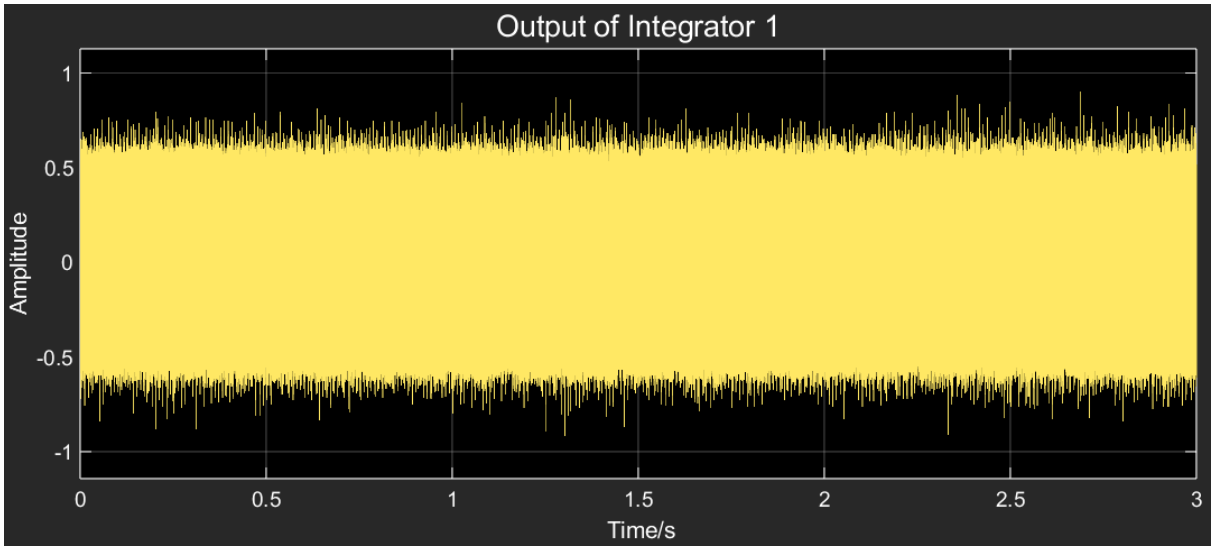

Figure 4.1: Output of integrator 1

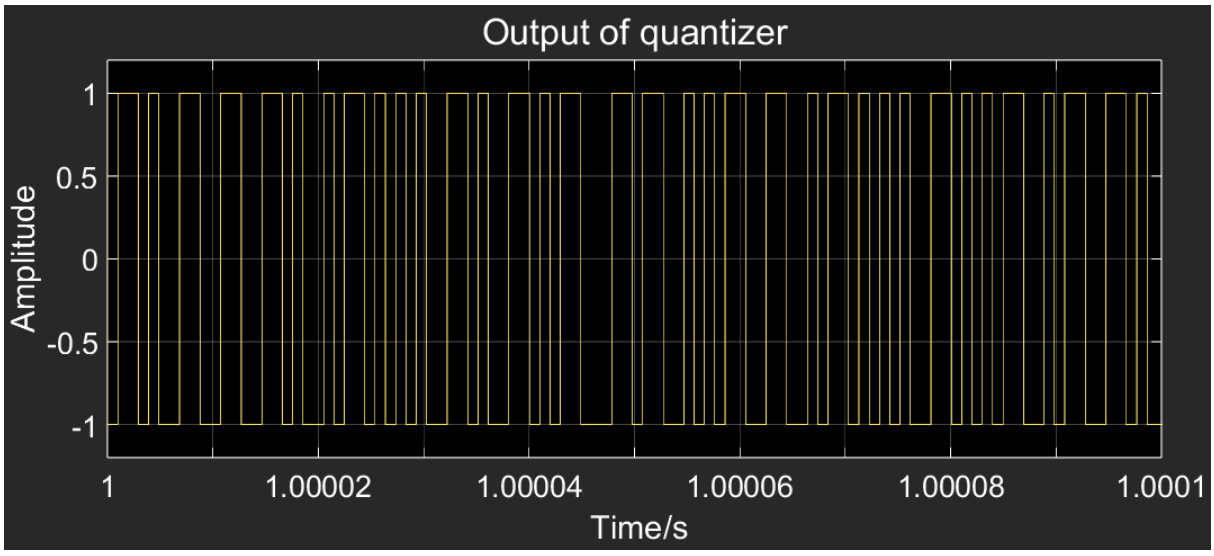

Figure 4.2: Output of quantizer (partial)

Subsequently, the output is demodulated as Figure 4.3 illustrated. This output waveform accurately replicates the input's amplitude and frequency, indicating a successful signal acquisition and reconstruction after decimation and filtering, confirming the modulator's capability of

processing low-frequency signals, while achieving minimal distortion. Figure 4.4 illustrates the Power Spectral Density (PSD) of the modulator output, showing the quantization noise shaping behaviour of 3rd order ΣΔM. The signal peak clearly represents the input signal of 100 Hz. Furthermore, a strong SQNR of 136.78 dB is calculated at the signal frequency. The red triangle illustrated in Figure 4.4 is a reference for 60 dB per decade slope, indicating the noise shaping effect of proposed ΣΔM meets the theoretical expectation for a third-order modulator.

The simulated signal-to-quantization-noise ratio (SQNR) of 136.78 dB showcases the system's resolution performance, with quantization noise effectively pushed outside the signal band. Comparing to the previous work [39], the designed fourth-order ΣΔM with oversampling ratio (OSR) of 512 and 3-bit quantizer achieved SQNR of 151.76 dB with same input signal. This suggest at current configuration, quantization is not the significant noise source that contribute to SNR, and the effect of noise shaping exceeds the actual need for over 12-bits. Additionally, Spurious-Free Dynamic Range (SFDR) is measured to be 138.66 dB, this is defined as the power difference between signal and the strongest spurious signal, representing the limitation of the dynamic range (DR) between the maximum and the minimum signal the system is capable to distinguish.

In current and simulations after, Fast Fourier Transform (FFT) frame size is set as 1,048,576 to provide a high resolution for monitoring low frequency, The sovler of Simulink is set as ODE5 (Dormand-Prince 5th Order) with fixed step size of 9.766×10^{-8}s ($\frac{1}{10f_s}$), providing a high-precision system monitoring. The simulation times is set to be 3 seconds to ensure a precise FFT resolution and smoothed noise floor to fully validate the model's performance, this duration can be reduced to improve computational efficiency if needed.

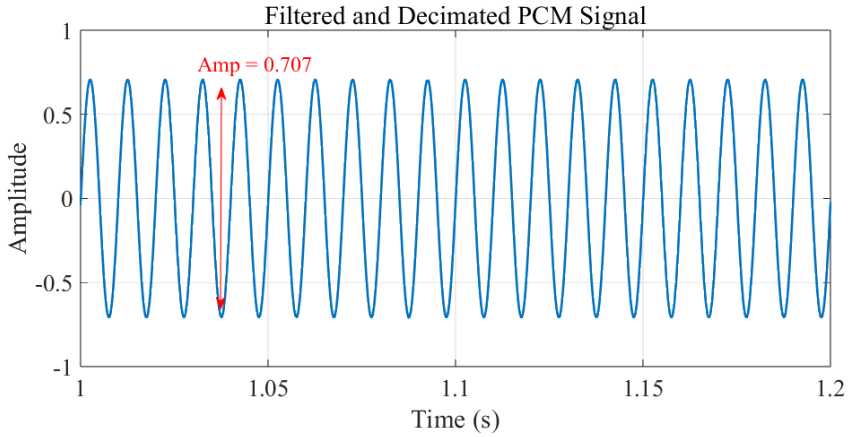

Figure 4.3: Demodulated output signal, when input is 0.707 amplitude at 100 Hz

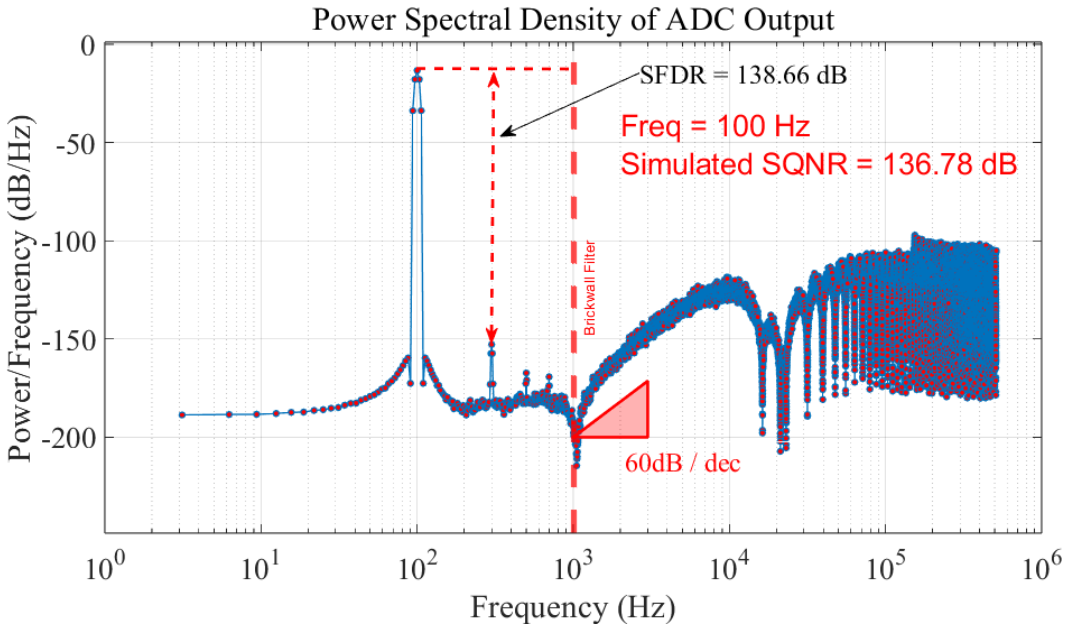

Figure 4.4: Power spectral density of the output

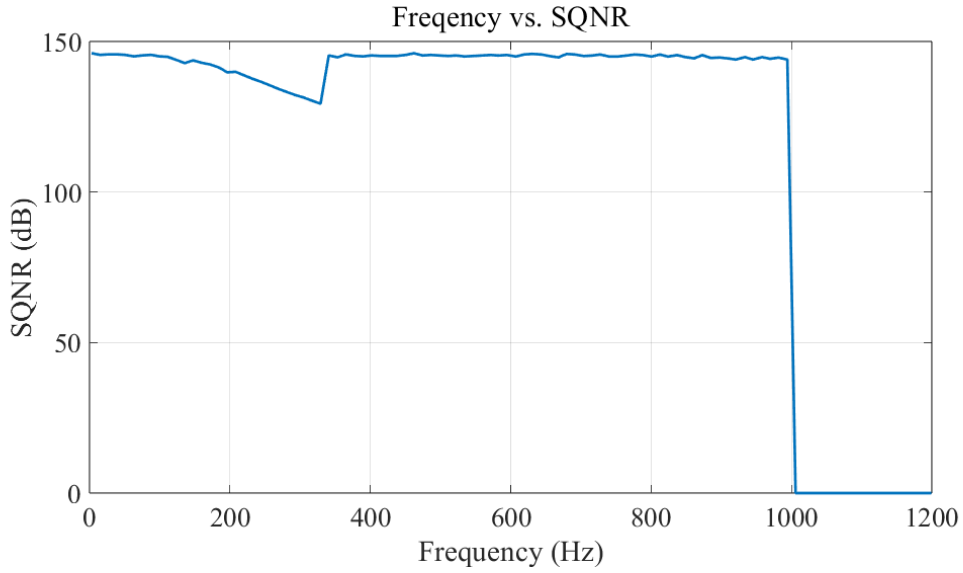

Figure 4.5: Frequency sweep at amplitude of 0.707

In order to fully prove the proposed ΣΔM is capable for processing input signal within the aimed signal band, a frequency sweep test is performed with frequency range of 1 - 1200 Hz, the result is presented in Figure 4.5. The frequency sweep result indicates the modulator's SQNR

across the operational frequency range, demonstrating good consistency on quantization noise shaping.

4.2 Noise simulation

n the previous chapter, noise sources created by non-linearity circuit-level factors, such as Operational transconductance amplifier (OTA) thermal noise, load capacitance noise, and finite gain effects were analysed in detail. Based on the calculations, these non-linearity noise is proved to be the dominative noise to cause system resolution degeneration. Though theoretical analysis have provided an estimation of these noise sources, it is still insufficient to determine the system signal-to-noise-and-distortion ratio (SNDR) and SNR. Therefore, noise simulation serves as an essential step to integrate theoretical prediction to block-level performance, providing reference to validation of the design and guidance for further optimization.

Figure 4.6 illustrates the PSD of the ΣΔM output with calculated OTA thermal noise and load capacitance noise added (blue curve), and the previous output which only consist the quantization noise (grey curve). The input signal remains unchanged as sine wave with amplitude of 0.707 at 100 Hz, and the simulated SNR is calculated as 119.33 dB.

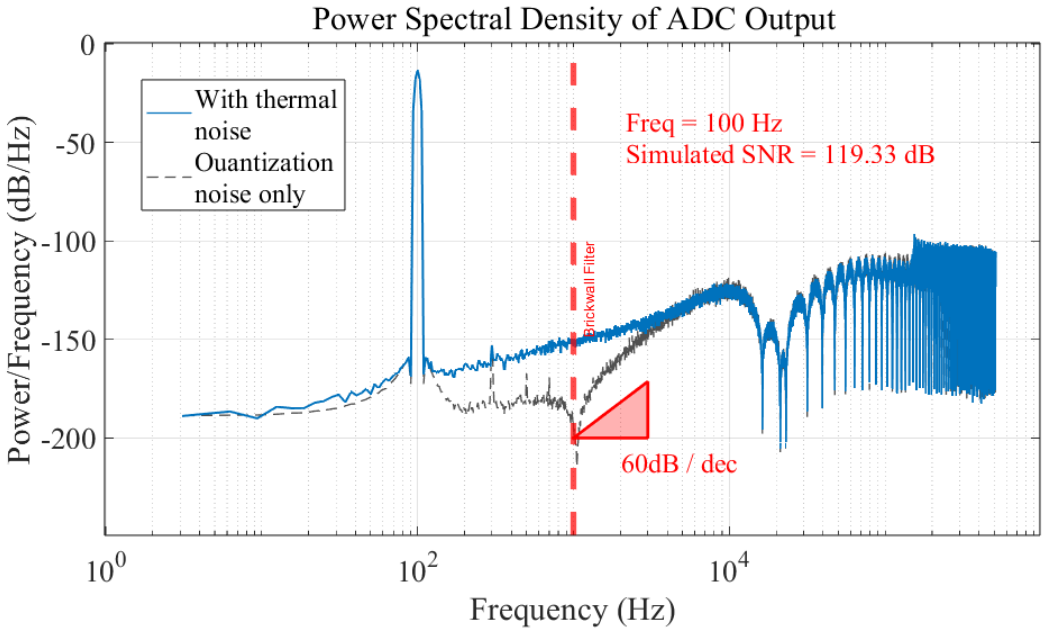

Figure 4.6: Power spectral density of the ΣΔM output, with thermal noise added

Similar to previous result, a clear effect of noise shaping is observed, though it failed to follow

the 60 dB per decade slope due to raised noise floor. Comparing two curves, the contribution from thermal noise is significant within the signal band as the simulated PSD deviates from the pure quantization noise curve. In actual simulated model, OTA thermal noise and load capacitance noise are applied on the first integrator only. As due to noise shaping, noise from the second and the third integrator are divided by the transfer function of the first stage integrator, contributing less to the total thermal noise in the signal band [44]. It is also noticed that most of the spurious signals found in previous simulation are now covered by noise floor, and the noise power at 1000 Hz is measured to be higher than than the previous strongest spurious signal.

4.3 Stability simulation

4.3.1 Amplitude sweep and dynamic range

To evaluate the Sigma-Delta modulator's performance with varying input conditions, an amplitude sweep test is performed to examine how the modulator processes different signal amplitudes. This test is crucial for determining the modulator's linearity, dynamic range (DR), and overall robustness against saturation for overwhelming large signal input. The result of amplitude sweep test is given by Figure 4.7.

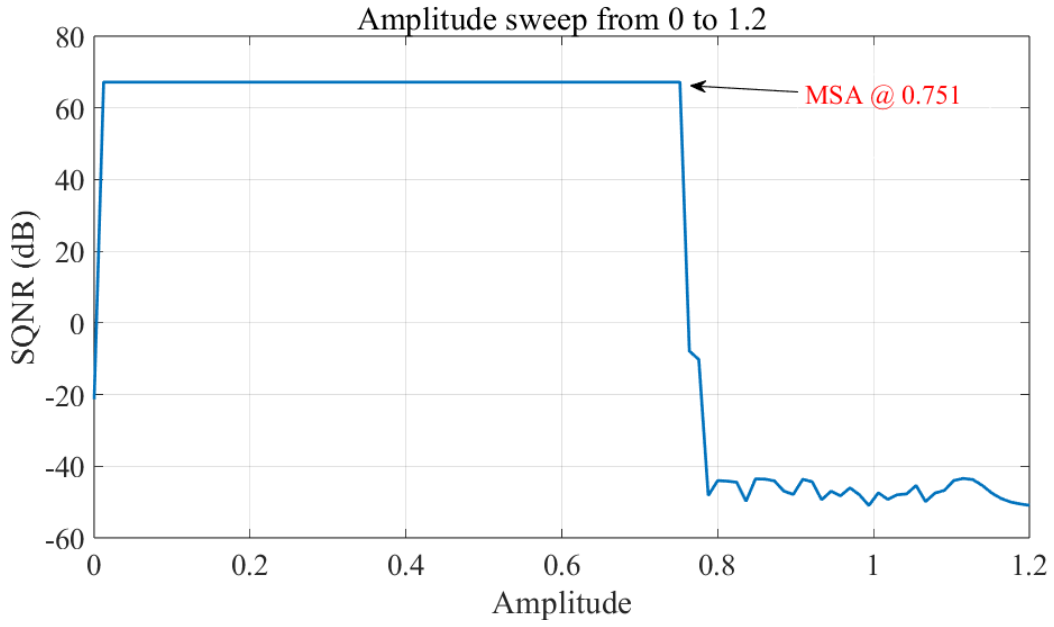

Figure 4.7: Amplitude sweep from 0 to 1.2

From the test result, the Maximum Stable Amplitude (MSA) is determined to be 0.751,

which identifies the highest input amplitude the modulator can process without causing unrecoverable self-oscillation. Comparing to the previous work, the fourth-order modulator design with oversampling ratio of 1024, which has achieved a MSA of 0.93, the proposed modulator significantly suffer from input saturation. In general, MSA is affected by the 1-bit quantizer as the limitation of output bit-width, DR is significantly reduced, and this also effect on the feedback loop. With MSA given, the DR is calculated with in-band total noise power of $2.855 \times 10^{-}13$, the DR is given by Eq, 4.1, which is 119.9 dB. The calculated DR indicates the $\Sigma\Delta$M is able to process signals with a wide range of amplitudes, which is essential for Electroencephalography (EEG) applications as discussed in Chapter 2.

$$DR = 10 \cdot \log_{10}(\frac{P_{max}}{P_{min}}) = 10 \cdot \log_{10}(\frac{P_{max,sig}}{P_{noise}}) = 119.9 \text{ dB} \tag{4.1}$$

4.3.2 Stress test with extreme input conditions

To evaluate the system's stability under extreme input conditions, stress tests are conducted with following input signals, including: (a) DC input, (b)DC input sweep, (c) step input, (d) high frequency perturbation test.

DC input test is one of the fundamental method to evaluate the system's stability under steady-state conditions. By testing the system with constant input signals, the test focuses on the response to low-frequency or zero-frequency inputs, ensuring that transient effects are minimized. The results obtained from the DC input test provided in following figures: (a) Zero input by Figure 4.8, (b) DC input at level of 0.5 by Figure 4.9.

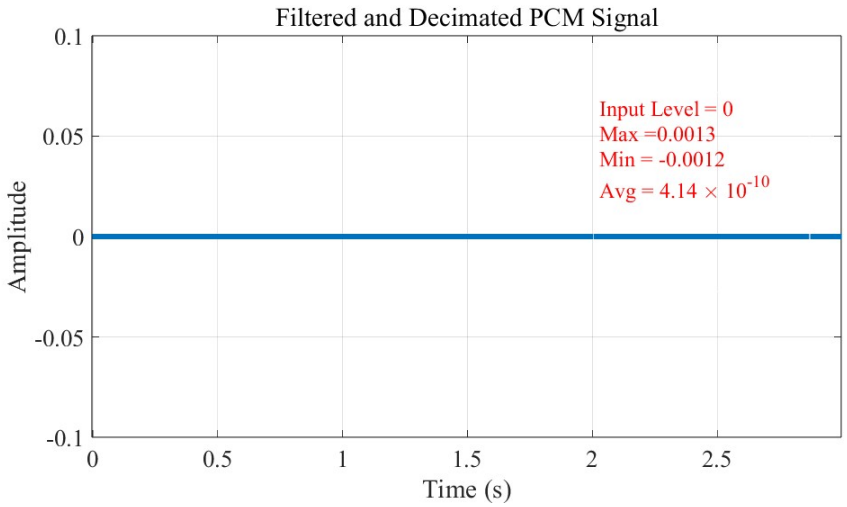

Figure 4.8: DC response with zero input

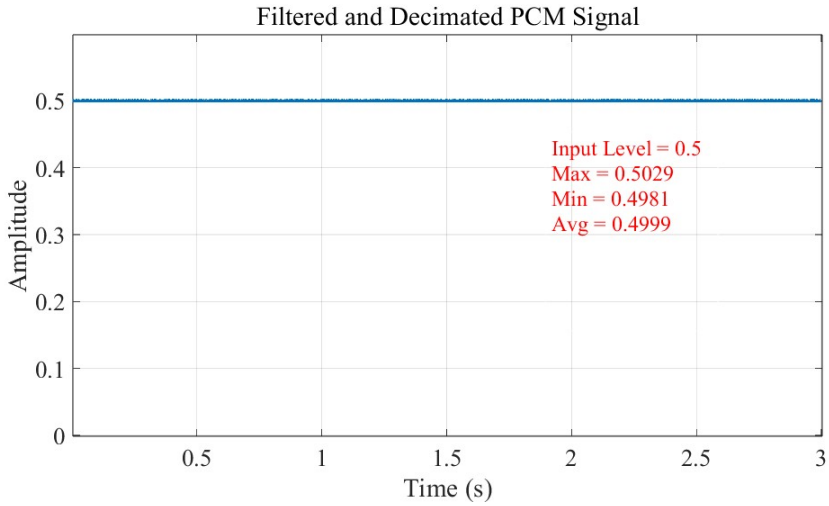

Figure 4.9: DC response with input level of 0.5

Both result show the system's stability under steady-state conditions and no DC offset is found. These results validate the system's ability to process static signals with a stable output, which is crucial for high precision and low-speed application, such as in EEG signal baselines detection. In order to further examine the linearity of the proposed ΣΔM with different DC inputs, a sweep test is conducted with the input DC level varys from -1 to 1, the result is given in Figure 4.10. The result indicates the modulator performs a linear input-output behaviour in range of ±0.960

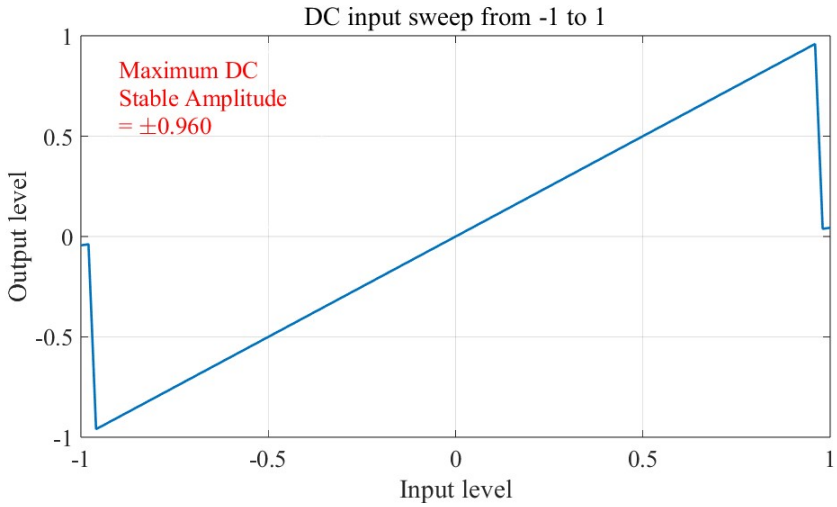

Figure 4.10: DC input level sweep from -1 to 1

The step input test is another critical method to evaluate the dynamic performance and stability of a system under sudden changes. By introducing an abrupt change in the input signal, the test examine the system's transition from one state to another, revealing its response characteristics, such as overshoot and settling time This assesses the system's ability to adapt to rapid input change while maintaining stability. The results from the step input test is provide in Figure 4.11. The settling time is measured as 7×10^{-5}s, reflecting the time required for the output to stabilize within a 10% to 90% range of the final value after the input step. This ensures system's rapid response capability, which is crucial to neuron spikes signal that are often encountered in real-time applications such as EEG signal processing.

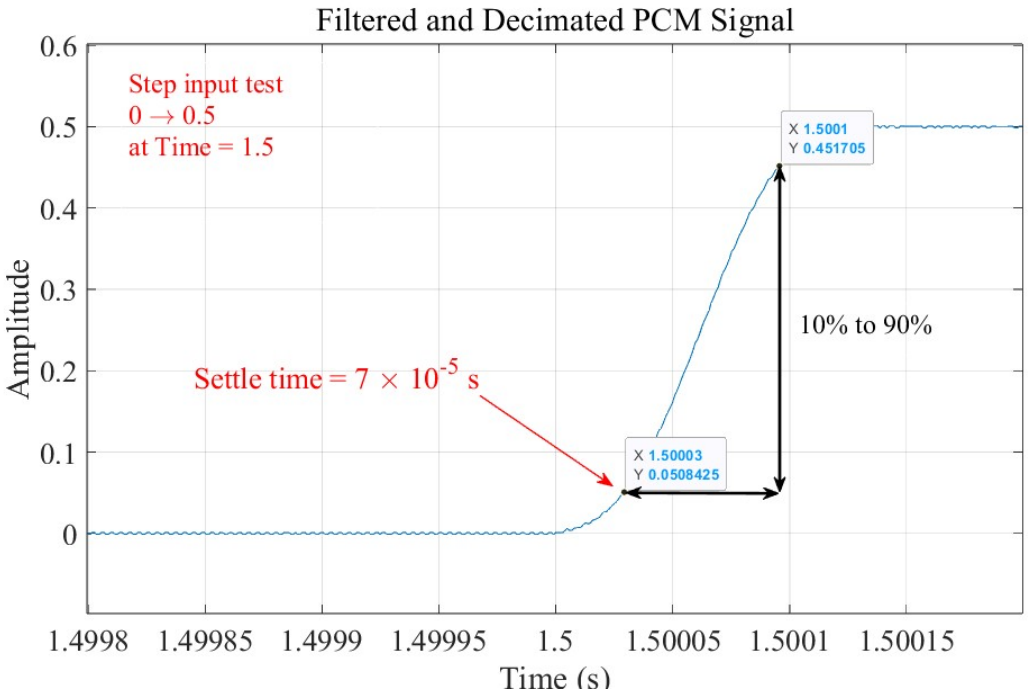

Figure 4.11: Step input from 0 to 0.5 at time of 1.5 s

To further evaluate the robustness and stability of the Sigma-Delta modulator under high-frequency perturbations, a dedicated perturbation test was performed by introducing a sinusoidal noise signal at high frequency significantly beyond the signal band of interest. The test employs a target input signal at around 100 Hz with amplitude of 0.707, while a high frequency noise signal at 50 kHz with amplitude of 20% of the target signal is introduced. The result is presented in Figure 4.12, which indicates the performance of the modulator is not affected by high-frequency perturbations. However, high amplitude perturbations can still saturate the modulator, highlighting the necessary of low-pass filters and chopper circuit before modulator input. This will

be further analysed in the next chapter.

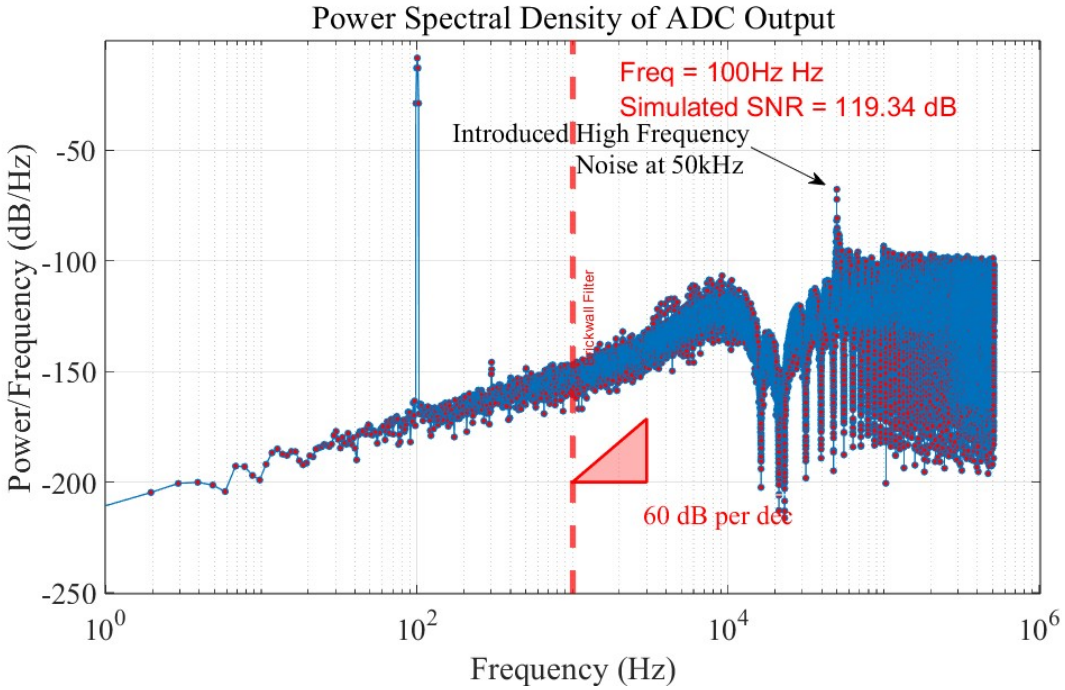

Figure 4.12: FFT of output signal with high frequency noise at 50 kHz

4.4 Finite integrator gain

In Section 3.3, the specification of OTA is presented with OTA gain at 1 kHz to be 64.24 dB. In practice, finite integrator gain significantly can affects on integration process, weakening noise shaping effect and introduces quantization noise leakage. Therefore, simulation with limited integrator gain is crucial for inspecting whether the specification of OTA sufficient for supporting expecting integrator operation.

Figure 4.13 presents the output SNR results with increasing integrator gain from 1 dB to 120 dB, with the target OTA gain in OTA design specifications labelled. The curve clearly shows that to achieve an expected performance on SNR, OTA gain more than 30 dB is required to avoid incomplete integration. This result is also gives reference to transistor-level design as the target OTA gain can be less than 64.24 dB to achieve better power consumption performance while maintaining same resolution.

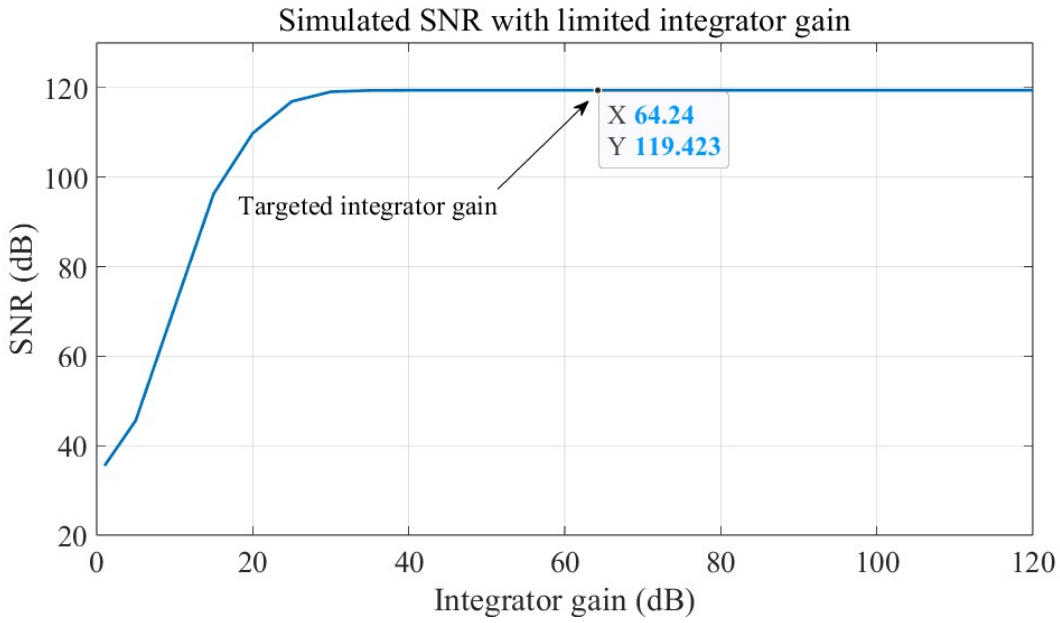

Figure 4.13: Output SNR with finite integrator gain from 1 dB to 120 dB

4.5 Summary

In this section, simulations are conducted for the proposed ΣΔM design, with analysis in depth, focusing several key areas: model functionality, noise characteristics, stability analysis, and system stability and responses under different input conditions.

Initial simulations are aimed to verify the modulator's functionality by examining the output behaviour of each integrator stage and the quantizer. Results indicated proper signal processing within the modulator, with integrator outputs maintaining expected dynamic ranges and the quantizer accurately generating discrete-level signals, representing the input signal with PDM. SQNR or the proposed modulator is calculated to be 136.78 dB with good consistency in the targent input signal range. This established a solid foundation for subsequent noise and stability analysis.

The noise simulations revealed the quantization noise and thermal noise, highlighting the impact of thermal noise from OTA and load capacitance. Results presents an effective noise shaping, achieving a simulated SNR of 119.33 dB and confirming the modulator's ability to suppress noise within the signal band. The simulation result with thermal noise is compared to previous simulation with pure quantization noise, indicating the thermal noise contributed the most to total noise in-band. Deviations from the ideal 60 dB per decade noise shaping effect slope were observed, which is caused by raised noise floors.

Additionally, amplitude sweep tests are conducted to provide insights into the modulator's dynamic range, with a calculated DR of 119.9 dB, the design's ability to handle variations in input amplitude is confirmed. It is noticed that the MSA of the modulator is significantly reduced by 1-bit quantizer, decreased to 0.751 from 0.93 in previous work. The DC response tests further verified the modulator's precision and low offset in steady-state conditions.

Finally, stability simulations tested the system under extreme input conditions, such as high-frequency perturbations and step input responses. The results confirmed the system's robustness and reliability with no significant deviation or instability observed at outputs. The effect of limited OTA gain is considered and simulated, confirming the target OTA gain is sufficient for expected noise shaping.

Overall, the chapter demonstrated the performance and robustness of the proposed $\Sigma\Delta$M design, providing a detailed validation of its performance metrics including noise suppression, stability, and linearity performance. These results prepare a good reference and foundation for further designs and refinements in the circuit-level design and silicon implementation.

Chapter 5

Impact and Exploitation

5.1 Product development cycle

In order to trace the progress been made, and summarize experiences in engineering and development of this project, it is crucial to align the actual project routine with the product development cycle. The product development cycle aims to provide a systematic view of how individual steps contribute to the overarching goal, thus result in a functional and impactful final product. In this project, the conducted work can be aligned to the product development cycle with several stages, summarized as follows:

- **Concept Generation**: This project started with a specific design of analogue-to-digital converter (ADC) of Electroencephalography (EEG) signal processing. Through literature review and interview with researchers in related fields, key challenges such as noise reduction, power efficiency, and high-resolution are focused. Meanwhile, number of commercial product are reviewed, which ensuring the proposed design's uniqueness and the demand on the market. The adoption of Cascade of Integrators with Feed-forward (CIFF) topology is confirmed in early stage.

- **Research and Development**: In this project, a refined workflow is proposed to achieve better work efficiency. The final design has been iterated for multiple versions in Simulink, and non-linearity are well-discussed. This work also provided a design specification for transistor-level implementation, which assists to examine the manufacturability. Complementary Metal Oxide Semiconductor (CMOS) technology was also addressed in consideration of manufacture cost and availability.

- **Validation**: Numbers of simulations focused on noise performance, stability and power efficiency simulation and analysis were integrated at the block level. The result indicated the

proposed design achieved predefined performance benchmarks, leading the design to be able to proceed to practical application.

- **Potential Production**: Through the project only consists theoretical analysis and block-level simulation, the outcomes can provide a robust foundation for transitioning to circuit-level design and eventual silicon fabrication. By pre-defining critical metrics of the modulator parameter and Operational transconductance amplifier (OTA) specifications, an efficient engineering work has been laid.

Additional, the improved efficiency of the refined workflow compared to conventional workflows. The key point of the proposed design methodology is incorporating circuit-level insights during the early stages, this leads to:

- **Reduced Iterations**: Early incorporation of non-linearity factors streamlines subsequent design phases.
- **Cost and Time Savings**: The workflow reduces redundancies, minimizing resource waste.

Overall, the project process is aligned to the product development cycle through initial researching and background study to pre-production stage, offering a good efficiency and reproducibility.

5.2 Impacts analysis

This project demonstrates potential for societal and economic impact, by contributing to:

- **Medical Applications**: The proposed Sigma-Delta modulator enhances EEG system performance, benefiting fields like neuroscience, brain–computer interface (BCI), and medical diagnostics. Meanwhile, reduced power consumption enables the mobility of related equipment, providing better monitoring for medical diagnostics purpose. This has potential to significantly improve the quality of life.
- **Industry Growth**: By proposing a low-power, high-resolution design, the project supports advancements in wearable health monitoring devices and clinical diagnostic equipment. Further, this assist the development in brain-controlling concept.
- **Economic Viability**: The refined workflow and low-power design contribute to cost-effective manufacturing and energy efficiency, which can lead to broad adoption in commercial and healthcare sectors.

- **Human Resource**: The proposed workflow streamlined the design process, loosen the requirement for ΣΔM designer, and allowed related designer to achieve a better efficiency. This design also potentially creating employment in related areas including medical service and brain-controlling equipment development.
- **Scientific researches**: The proposed workflow and design advance the field of ΣΔM development, improve the smoothness of design flow and support future researches.

The advantage of this fully analogue design should also be addressed. Design in this work adopts a 0.35 μm CMOS technology for a complete analogue design, and other digital components and devices, such as the decimation filter and clock can be provided with a more advanced process. This contributes to reduce waste and cost by repurposing outdated fabrication technology, while the proposed design can receive performance upgraded by swapping advanced digital components without discarding the entire device.

5.3 Future works

Despite the design and simulations conducted in this work, improvements and additional studies are expected in future works. This including the refinement and tuning on existing design, more simulation arranged for comprehensive verification on performance, additional features on current design, development in next design level, and other devices at input or output.

The current system employs optimized parameter to balance noise suppuration and stability. However, as result shown in Ch. 4, the modulator design can lean more to stability side. This can specifically draw by re-tuning the noise transfer function (NTF) pole location and adopt multi-bit quantizer. The current simulations are focused on the existing design, and more simulations can be performed focusing on the impact of design factors, such as the order of integrator and multi-bit quantizer. Other technique focused on improving modulator performance, such as dynamic element matching for multi-bit quantizer can be apply to minimize the affect by component mismatch.

To achieve a complete development cycle, circuit-level and transistor-level design needs to be continued after this work, and tests in corresponding level should be performed. This is specifically important as some block-level components, such as "sum block", quantizer, "gain block" are not fully defined in this work. Additionally, circuit chopper and other component can be introduced at this stage.

Finally, to achieve a fully functional analogue front-end (AFE), other devices including () and decimation filter should be included, from this, a completed analogue-to-digital conversion process can be simulated.

Chapter 6

Conclusion

6.1 Summary of achievements

This project aimed to design a high resolution Sigma-Delta modulator (ΣΔM) for Electroencephalography (EEG) signal acquisition, the key achievements and milestones of this work is summarized as follows:

- **Literature review on EEG system and EEG purpose ΣΔM**:

  This project established a literature review on EEG system, focusing on EEG signal characteristics, EEG system and analogue front-end (AFE) requirements. A summary of the state-of-the-art studies on EEG purpose ΣΔM is provided to give insights of related works and establish a proper target performance metrics for this work.

  In early stage, a number of current researches have been studied, focusing on advanced ΣΔM design, including Multi-Stage Modulators (MASH) design and hybrid Continuous-Time (CT)/Discrete-Time (DT) integrator design. Meanwhile, information on EEG technology with related hardware studies are explored to outline a preliminary aimed design specifications. As the process advances, the work subsequently focused on detailed design metrics, such as comparison between different topologies, especially for Cascade of Integrators with Feed-forward (CIFF) and Cascade of Integrators with Feedback (CIFB), which are commonly found in similar applications. Design parameters from different works are listed together and compared, aiming to quantify the influence of parameters on performance. As the design proceed to circuit-level non-linearity analysis, study by Hunter and Poole [44] was review in depth for non-linear factor in design.

- **Refined workflow**:

  A refined workflow is established in this project, providing a systematic approach for the design and evaluation of ΣΔM. This refined approach ensured reliability, mitigated the design complexity in circuit-level and transistor-level and minimize the possibility of iteration.

  The design workflow began with analyses on system requirements, and defining key system parameters through calculations, then followed by block-level model design. In parallel, non-linearity factors integrated early into the process with block-level design, using theoretical calculations and simulation tools in order to assist block-level simulation. Subsequently, block-level refinement and tests are performed with non-linearity information, and simulation result for performance metrics are obtained. Then, the design proceeds to circuit-level design and transistor-level implementation, the work load can be reduced with previous block-level validation and design specifications

- **Block-level design and Simulink validation**:

  The proposed modulator was modelled and validated with Simulink simulation. The result confirmed the proposed modulator's functionality, with expected behaviours at each stage. CIFF topology is applied to the proposed design for its stability and power efficiency with detailed analysis. This provides a solid foundation for further simulations and higher level designs.

- **Performance verification on proposed design**:

  The performance of the proposed ΣΔM design was thoroughly verified through a series of simulations and analyses, with performance metrics were evaluated under various operating conditions.

  The resolution of the modulator obtained a signal-to-noise ratio (SNR) of 119.63 dB and a dynamic range (DR) of 119.9 dB, fully achieved the expected noise suppression requirement, proving the proposed ΣΔM is suitable for high-precision signal acquisition with minimized noise and distortion. Moving forward, stress tests with extreme input conditions including step input, DC input and amplitude sweep are performed, result in no obvious degenerations and interference found at output. Therefore, good robustness and stability of the proposed ΣΔM are proven.

Overall, this work provide an in-depth research on state-of-the-art ΣΔM studies focusing on advanced design. A refined workflow has significantly improve the coherence and efficiency of ΣΔM design process. The proposed ΣΔM achieved predefined performance benchmarks, demonstrated applicability for high-precision, low-power EEG system.

6.2 Reflections on design and workflow

During this study, possible improvements on workflow and design are found. However, due to the limitations on foundational knowledge, time and experience, these improvements are not put into practice. Upon reviewing the entire project, areas to be improved are summarized as follows:

- **Workflow**: In this project, workflow can be improved to have more areas for foresight on design process. Firstly, the design process began with no sufficient study on different $\Sigma\Delta$M design choices, which have caused ineffective model design and iterations on early stage. Meanwhile, the process of gathering relevant research resources cannot be considered as comprehensive and efficient. The reviewed studies are not sorted with a clear timeline and priority on contents, numbers of outdated design or irrelevant studies are brought in early literature review.

  During block-level design, iterations on design parameter lacked a systematic and incremental approach, causing redundant evaluations and simulations. Meanwhile, the design process utilized a relatively outdated platform and optimizing tool which failed to leverage design efficiency from newer techniques. The non-linearity analysis lacked validation, and circuit simulation in parallel with block-level design can be introduced to ensure the reliability of non-linearity analysis. Most importantly, time cost on refining model and simulation parameters exceeded the expectation, result in some scheduled design not implemented.

- **Design**: To simulate all performance metrics as possible, in final design model, sub-blocks for test are introduced with disorganized placing and insufficient notes. In actual operation, this lead to uncertainty of variables that are applied, result in unnecessary repetition in tests. Due to modular design the from sub-blocks, different design should be also modelled and simulated to provided reference to variation on performance. In detail, during the design process, dynamic element matching technique for digital-to-analogue converter (DAC) component mismatch are studied and well evaluated with functioning model, However, as the final design adopts a 1-bit quantizer design, this feature is not added to the final design.

Overall, insufficient planning, outdated resources, redundant testing, and wasted resources degraded the quality of the final output from this work. This requires the future projects must adopt better structured workflows and sufficient preliminary researches, the proposed analysis should be well-verified in simulations. Resources and achievement must be fully utilized and demonstrated in the final outcome.

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Appendix A

Derivation of theoretical peek SQNR

As given in section 2.1.3, the noise transfer function (NTF) is given by Eq. A.1.

$$\begin{aligned} \mathrm{NTF}(z) &= (1 - z^{-1})^N \\ \textbf{with } z &= e^{j2\pi \frac{f}{f_s}} \\ |\mathrm{NTF}(f)| &= (2\sin(\frac{\pi f}{f_s}))^N \end{aligned} \tag{A.1}$$

The signal-to-quantization-noise ratio (SQNR) is given by Eq. A.2.

$$SQNR = 10\log_{10}\frac{P_s}{\mathrm{IBN}_q} \tag{A.2}$$

The power of signal, P_s depends on the bit-length of quantizer, N, given by Eq. A.3.

$$P_s = \frac{\Delta^2}{4} \cdot 2^{2N} \tag{A.3}$$

Substitute Eq. 2.9 and Eq. A.3 to Eq. A.2, the SQNR is derived as Eq. A.4.

$$\begin{aligned} SQNR_{peak} &= 10\log_1 0\frac{P_s}{\mathrm{IBN}_q} \\ &= 10\log_{10}(\frac{\Delta^2}{4} \cdot 2^{2N}) - 10\log_{10}(\frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)\mathrm{OSR}^{2L+1}}) \\ &= 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}(\mathrm{OSR})^{2N+1}\right) \end{aligned} \tag{A.4}$$

Appendix B

MATLAB codes

PSD and SQNR calculation

```
decimation_factor = OSR;
fs_new = Fs / decimation_factor;
f_cutoff = BW;
fs_pcm = fs_new;
filter_order = 128;
Qout = out.Qout;

d = designfilt('lowpassfir', 'FilterOrder', filter_order, ...
               'CutoffFrequency', f_cutoff, 'SampleRate', Fs);
pcm_signal = filter(d, Qout);
t_pcm = (0:length(pcm_signal)-1) / Fs;

if plotflag == 1
    figure;
    subplot(2, 1, 1)
    plot(t_pcm, pcm_signal);
    title('Filtered and Decimated PCM Signal');
    xlabel('Time (s)');
    ylabel('Amplitude');
    grid on;
end

% Parameters for pwelch
frame_size  = psdctrl.framesize; % Length of each segment
window = blackman(frame_size);
overlap = round(frame_size / h.OverlapPercent) ; % 50% overlap
nfft = frame_size; % Number of FFT points

% Compute the Power Spectral Density using pwelch
```

```
[pxx, f] = pwelch(pcm_signal, window, overlap, nfft, Fs);

if plotflag == 1
    subplot(2, 1, 2);
    plot(f, 10*log10(pxx)); % Convert to dB scale
    title('Power Spectral Density of ADC Output');
    xlabel('Frequency (Hz)');
    ylabel('Power/Frequency (dB/Hz)');
    grid on;
end

% Calculate the signal power (integrate over the signal band)
main_lobe_bins = 6; % Main lobe width in bins for Blackman window
main_lobe_width_hz = main_lobe_bins * (Fs / nfft);

signal_band = [sinfreq - main_lobe_width_hz/2, sinfreq + main_lobe_width_hz/2];

in_band = [0 , BW];

signal_indices = f >= signal_band(1) & f <= signal_band(2);
signal_power = bandpower(pxx, f, signal_band, 'psd');
signal_power

total_power = bandpower(pxx, f, in_band, 'psd');
total_power

noise_power = total_power - signal_power;
noise_power

SQNR = 10 * log10(signal_power / noise_power);
SQNR
```

Sweep test on variable

In order to obtain better computational efficiency, MATLAB Parallel Computing Toolbox is applied. The code listed below is a sweep test on input sine wave amplitude, test on different variable can be performed based on this code.

```
amplab = (linspace(0, 1.2, 100))

% Initialize an array to store SQNR values
SQNR_values = zeros(size(amplab));

% Define the frequency of the input sine wave
swpctrl.trantime = 3;
```

```
Ptr = 0;
plotflag = 0;
% Loop over each sine wave amplitude
parfor i = 1:length(amplab)


    simIn = Simulink.SimulationInput(target_modulator);
    simIn = simIn.setVariable('Fs', Fs);
    simIn = simIn.setVariable('DACctrl', DACctrl);
    simIn = simIn.setVariable('input_dc', input_dc);
    simIn = simIn.setVariable('intNoise', intNoise);
    simIn = simIn.setVariable('modctrl', modctrl);
    simIn = simIn.setVariable('noisectrl', noisectrl);
    simIn = simIn.setVariable('swpctrl', swpctrl);
    simIn = simIn.setVariable('a', a);
    simIn = simIn.setVariable('b', b);
    simIn = simIn.setVariable('c', c);
    simIn = simIn.setVariable('g', g);
    %simIn = simIn.setVariable('', );


    sinamp = amplab(i);
    simIn = simIn.setVariable('sinfreq', sinfreq);
    simIn = simIn.setVariable('sinamp', sinamp);
    % Run the Simulink model

    simOut = sim(simIn)

    % Extract Qout from Simulink output


    % Decimation and filtering parameters

    decimation_factor = OSR;
    fs_new = Fs / decimation_factor;
    f_cutoff = BW;
    fs_pcm = fs_new;
    filter_order = 128;
    Qout = simOut.Qout;
    d = designfilt('lowpassfir', 'FilterOrder', filter_order, ...
              'CutoffFrequency', f_cutoff, 'SampleRate', Fs);
    pcm_signal = filter(d, Qout);
    t_pcm = (0:length(pcm_signal)-1) / Fs;
    frame_size  = psdctrl.framesize; % Length of each segment
```

```
    window = blackman(frame_size);
    overlap = round(frame_size / h.OverlapPercent) ; % 50% overlap
    nfft = frame_size; % Number of FFT points

    % Compute the Power Spectral Density using pwelch
    [pxx, f] = pwelch(pcm_signal, window, overlap, nfft, Fs);
    % Calculate the signal power (integrate over the signal band)
    main_lobe_bins = 6; % Main lobe width in bins for Blackman window
    main_lobe_width_hz = main_lobe_bins * (Fs / nfft);

    signal_band = [sinfreq - main_lobe_width_hz/2, sinfreq +
        main_lobe_width_hz/2];

    in_band = [0 , BW];

    signal_indices = f >= signal_band(1) & f <= signal_band(2);
    signal_power = bandpower(pxx, f, signal_band, 'psd');
    signal_power

    total_power = bandpower(pxx, f, in_band, 'psd');
    total_power;

    noise_power = total_power - signal_power;
    noise_power;

    SQNR = 10 * log10(signal_power / noise_power);
    SQNR


    % Calculate SQNR
    SQNR_values(i) = SQNR;

end
```

Model initialization

```
    format short g
psdctrl.win = 'blackman-harris';
psdctrl.winbw = 3;
modctrl.igain1 = inf;
modctrl.igain3 = inf;
modctrl.isat1= inf;
modctrl.isat2= inf;
modctrl.isat3= inf;
modctrl.qsatin1 = inf;
```

```
modctrl.qsatin2 = inf;
modctrl.qlev1=2;
modctrl.qlev2=2;
modctrl.qlev3=2;
modctrl.dgain1 = 0;
modctrl.dgain2 = 0;
modctrl.mgain1 = 1; .
modctrl.mgain2 = 1;
modctrl.mgain3 = 1;
modctrl.nlg1 = 10;
modctrl.nlg2 = 10;
modctrl.nlg3 = 10;
modctrl.ngain1 = 0;
modctrl.ngain2 = 0;
modctrl.ngain3 = 0;
Order = 3;
nLev = 2;
OSR = 512;
form = 'CIFF';
BW = 1000;
target_modulator = 'MEngPrjPH2';
Fs = BW *2 *OSR;
H = synthesizeNTF(Order,OSR,1) ;
[a g b c] = realizeNTF(H,form);
ABCD = stuffABCD(a,g,b,c,form);
[ABCDscaled umax] = scaleABCD(ABCD,nLev)
[a g b c] = mapABCD(ABCDscaled,form);
swpctrl.select = 1;
swpctrl.trantime = 3;
psdctrl.framesize = 2^20;
Cpara = 100;
sinfreq = Cpara * Fs/psdctrl.framesize;
noisectrl.select = 1;
sinamp = 0.707;
intNoise = 1;
```

Appendix C

Simulink Sub-model

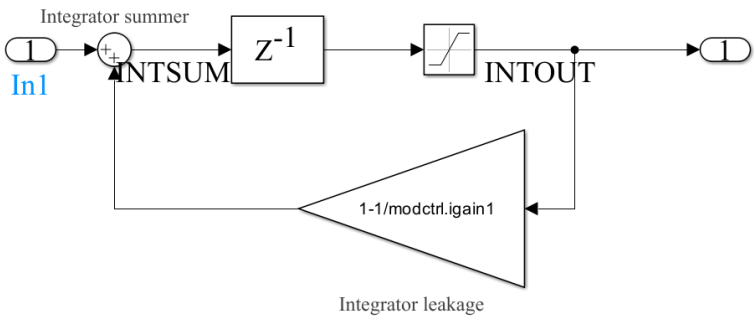

Figure C.1: Sub-block for integrator

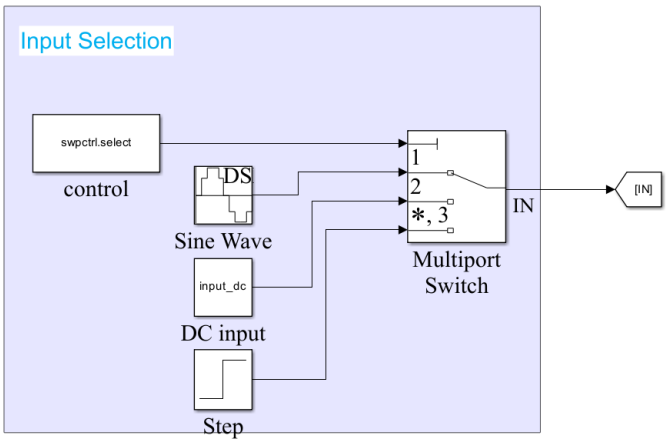

Figure C.2: Sub-block for Input signal selection

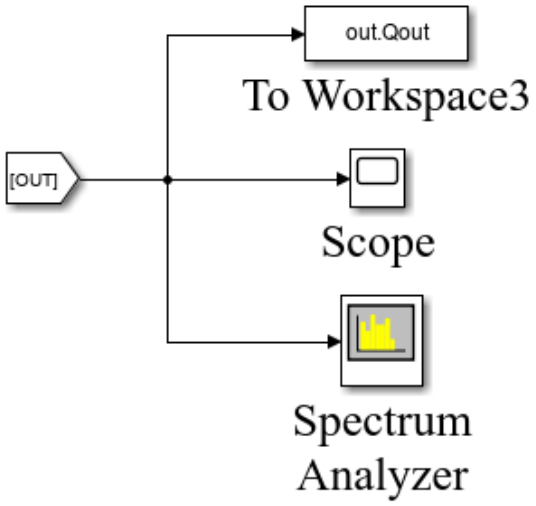

Figure C.3: Sub-block for output monitoring

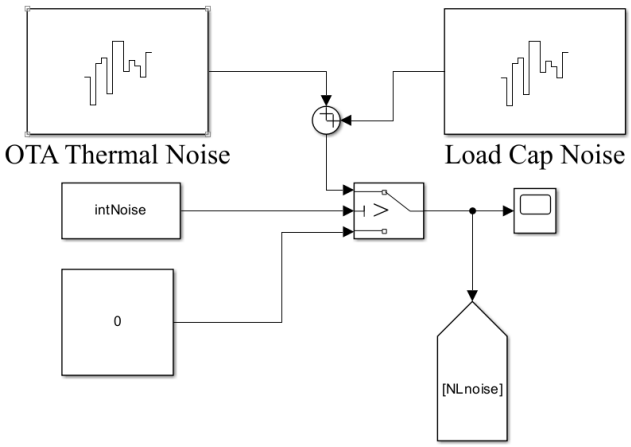

Figure C.4: Sub-block for thermal noises