

Hanryck Brar

Canadian Citizen

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𝕏 @ItsHB17

✉ Hanryck Brar

👤 Hanbrar

📍 Vancouver, BC

Education

University of British Columbia (UBC)

Bachelor of Applied Science (BASc) in Electrical Engineering

Vancouver, BC

Sep 2024 – Present

Relevant Coursework: Embedded Systems, Digital Design, Software Engineering, Control Systems

Technical Skills

Programming: Python, C, Java, TypeScript, SystemVerilog, Verilog, MATLAB

Web & Cloud: Next.js, React, Tailwind CSS, Supabase (PostgreSQL, Auth), Vercel, SSE Streaming

Tools & Platforms: Git, Quartus, ModelSim, Pandas, Matplotlib, Jupyter, Hugging Face, Excel, Claude Code

Design & Product: Product Design, UI/UX Design, Landing Page Design

Engineering: Embedded Systems, Robotics, Control Systems, ARM Microcontrollers, FPGA Design

Lab Skills: Circuit Design, PCB Layout, Soldering, Oscilloscopes, Multimeters, Data Analysis

Experience

UBC Smart City Design Team

Vancouver, BC

Transportation Sub-Team – PCB Engineer

Sep 2025 – Present

- Designing flight controller PCB with sensor interfaces and power management for an autonomous medicine-delivery drone, collaborating cross-functionally with electrical and mechanical sub-teams.

Projects

DeepConverge – Multi-Agentic AI Debate Platform ([deepconverge.ai](#))

Feb 2026

- Built a full-stack multi-agentic debate platform featuring three AI agents (Advocate, Critic, Judge) that reason collaboratively via real-time SSE streaming using NVIDIA Nemotron 30B.
- Designed and shipped end-to-end product including Next.js 14 frontend, Supabase Auth (Google OAuth), PostgreSQL database for conversation history, and toggleable convergent thinking mode with collapsible reasoning blocks.
- Implemented waitlist-gated access control, debate history replay, and PDF export with LaTeX-to-Unicode math rendering, delivering a polished production-grade application deployed on Vercel.

ARC4 Hardware Cracker – Parallel Verilog Key-Search Engine (FPGA)

Dec 2025

- Designed a high-throughput ARC4 key-cracking pipeline in Verilog with custom parallel processing module, achieving search performance exceeding 15 million keys in approximately 2 seconds.
- Implemented multi-core cracking units with on-chip memory buffering and timing-aware RTL optimization, maximizing throughput and FPGA resource efficiency.

Autonomous Coin-Picking Robot – Project Lead

May 2025

- Led 6-person team to build STM32/PIC32-based robot with JDY-40 wireless communication and inductive sensing, achieving autonomous coin detection and retrieval.
- Programmed PWM-based motor and servo control with dual-mode navigation, enabling precise movement and object manipulation in competitive environment.