CPU所用部件及数据来源

	PC	NPC	IMEM	RegFile	ALU		Ext16 Ext5		Ext18	ADD		II		DMEM	
				Rd/Rt	A	В				A	В	Α	В	Addr	Data
Add	NPC	PC	PC	ALU	Rs	Rt									
Addu	NPC	PC	PC	ALU	Rs	Rt									
Sub	NPC	PC	PC	ALU	Rs	Rt									
Subu	NPC	PC	PC	ALU	Rs	Rt									
And	NPC	PC	PC	ALU	Rs	Rt									
Or	NPC	PC	PC	ALU	Rs	Rt									
Xor	NPC	PC	PC	ALU	Rs	Rt									
Nor	NPC	PC	PC	ALU	Rs	Rt									
Sit	NPC	PC	PC	ALU	Rs	Rt									
Sltu	NPC	PC	PC	ALU	Rs	Rt									
SII	NPC	PC	PC	ALU	Ext5	Rt		sa							
Srl	NPC	PC	PC	ALU	Ext5	Rt		sa							
Sra	NPC	PC	PC	ALU	Ext5	Rt		sa							
SIIv	NPC	PC	PC	ALU	Rs	Rt									
Srlv	NPC	PC	PC	ALU	Rs	Rt									
Srav	NPC	PC	PC	ALU	Rs	Rt									
Jr	Rs		PC												
Addi	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Addiu	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Andi	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Ori	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Xori	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Lw	NPC	PC	PC	DMEM(Data)	Rs	Ext16	offset							ALU	
Sw	NPC	PC	PC		Rs	Ext16	offset							ALU	Rt
Beq	ADD	PC	PC		Rs	Rt			offset	NPC	Ext18				
Bne	ADD	PC	PC		Rs	Rt			offset	NPC	Ext18				
SIti	NPC	PC	PC	ALU	Rs	Ext16	imm16								
SItiu	NPC	PC	PC	ALU	Rs	Ext16	imm16								
Lui	NPC	PC	PC	ALU	16	Ext16	imm16								
J	II	PC	PC									PC(31-28)	IMEM(25-0)		
Jal	II	PC	PC	PC								PC(31-28)	IMEM(25-0)		

	3126	2521	2016	1511	106	50			
521	ор	rs	rt	rd	sa	func			
	ор	rs	rt	immediate					
3335	ор			Index					
Add	000000	rs	rt	rd	0	100000			
Addu	000000	rs	rt	rd	0	100001			
Sub	000000	rs	rt	rd	0	100010			
Subu	000000	rs	rt	rd	0	100011			
And	000000	rs	rt	rd	0	100100			
Or	000000	rs	rt	rd	0	100101			
Xor	000000	rs	rt	rd	0	100110			
Nor	000000	rs	rt	rd	0	100111			
SIt	000000	rs	rt	rd	0	101010			
SItu	000000	rs	rt	rd	0	101011			
SII	000000	0	rt	rd	sa	000000			
Srl	000000	0	rt	rd	sa	000010			
Sra	000000	0	rt	rd	sa	000011			
SIIv	000000	rs	rt	rd	0	000100			
Srlv	000000	rs	rt	rd	0	000110			
Srav	000000	rs	rt	rd	0	000111			
Jr	000000	rs	0	0	0	001000			
Addi	001000	rs	rt		immediate(- ~ +)				
Addiu	001001	rs	rt		immediate(- ~ +)				
Andi	001100	rs	rt	immediate(0 ~ +)					
Ori	001101	rs	rt	immediate(0 ~ +)					
Xori	001110	rs	rt		immediate(0 ~ +)				
Lw	100011	rs	rt	immediate(- ~ +)					
Sw	101011	rs	rt		immediate(- ~ +)				
Beq	000100	rs	rt	immediate(- ~ +)					
Bne	000101	rs	rt	immediate(- ~ +)					
SIti	001010	rs	rt	immediate(- ~ +)					
SItiu	001011	rs	rt		immediate(- \sim +)				
Lui	001111	00000	rt		immediate(- ~ +)				
J	000010			address					
Jal	000011			address					

	z	wreg	regrt	jal	m2reg	shift	aluimm	sext	aluc[3:0]	wmem	pcs[1:0
Add	Х	1	0	0	0	0	0	х	0010	0	00
Addu	х	1	0	0	0	0	0	х	0000	0	00
Sub	х	1	0	0	0	0	0	х	0011	0	00
Subu	х	1	0	0	0	0	0	х	0001	0	00
And	х	1	0	0	0	0	0	х	0100	0	00
Or	х	1	0	0	0	0	0	х	0101	0	00
Xor	х	1	0	0	0	0	0	х	0110	0	00
Nor	х	1	0	0	0	0	0	х	0111	0	00
SIt	х	1	0	0	0	0	0	х	1011	0	00
Sltu	х	1	0	0	0	0	0	х	1010	0	00
SII	х	1	0	0	0	1	0	х	111x	0	00
Srl	Х	1	0	0	0	1	0	х	1101	0	00
Sra	Х	1	0	0	0	1	0	х	1100	0	00
SIIv	х	1	0	0	0	0	0	х	111x	0	00
Srlv	х	1	0	0	0	0	0	х	1101	0	00
Srav	х	1	0	0	0	0	0	х	1100	0	00
Jr	х	0	x	x	х	X	X	х	xxxx	0	10
Addi	х	1	1	0	0	0	1	1	0010	0	00
Addiu	х	1	1	0	0	0	1	1	0000	0	00
Andi	х	1	1	0	0	0	1	0	0100	0	00
Ori	х	1	1	0	0	0	1	0	0101	0	00
Xori	х	1	1	0	0	0	1	0	0110	0	00
Lw	х	1	1	0	1	0	1	1	0010	0	00
Sw	x	0	X	Х	Х	0	1	1	0010	1	00
Beq	0	0	X	x	X	0	1	1	0010	0	00
Beq	1	0	X	X	X	0	1	1	0010	0	01
Bne	0	0	X	X	X	0	1	1	0010	0	01
Bne	1	0	X	X	X	0	1	1	0010	0	00
SIti	X	1	1	0	0	0	1	1	1011	0	00
Sltiu	X	1	1	0	0	0	1	1	1010	0	00
Lui	X	1	1	0	0	X	1	X	100x	0	00
J	X	0	X	X	X	x	X	X	xxxx	0	11
Jal	X	1	X	1	X	x	X	X	XXXX	0	11