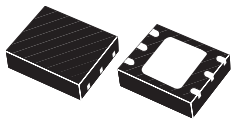
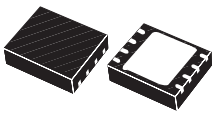
ST1L05

Very low quiescent current BiCMOS voltage regulator

Datasheet - production data



DFN6 (3x3 mm)



DFN8 (4x4 mm)

Features

- Fixed output voltage: 1.8 V, 2.5 V, 3.3 V and ADJ
- Output voltage tolerance: ± 2% at 25 °C
- Output current capability: 1.3 A
- Very low quiescent current: max. 650 µA
- Typ. dropout 0.3 V (@ I_O = 1.3 A)
- Enable function for B, C and D versions
- Power Good function for B and D versions
- Stable with low ESR ceramic capacitors
- Thermal shutdown protection with hysteresis
- Overcurrent protection
- Operating junction temperature range: from 0 to 125 °C

Description

The ST1L05 is a low drop linear voltage regulator, which supplies up to 1.3 A output current.

The output voltage is fixed at 1.8 V, 2.5 V, 3.3 V and it is adjustable. It is available in three different versions with different pinouts.

Thanks to BiCMOS technology, the quiescent current is controlled and maintained below 650 µA over the entire allowed junction temperature range. The ST1L05 is stable with low ESR output ceramic capacitors.

Internal protection circuitry includes thermal protection with hysteresis and overcurrent limiting.

The ST1L05 is suitable for data storage applications such as HDDs, where it can supply 3.3 V required by read channel and memory chips.

The regulator is available in the small and thin DFN6 (3x3 mm) and DFN8 (4x4 mm) packages.

Table 1. Device summary

Order codes	Package	Output voltage
ST1L05PU25R	DFN6 (3x3 mm)	2.5 V
ST1L05APU33R	DFN6 (3x3 mm)	3.3 V
ST1L05BPUR	DFN6 (3x3 mm)	ADJ
ST1L05CPU33R	DFN6 (3x3 mm)	3.3 V
ST1L05DPUR	DFN8 (4x4 mm)	ADJ

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Figure 1. ST1L05 schematic diagram

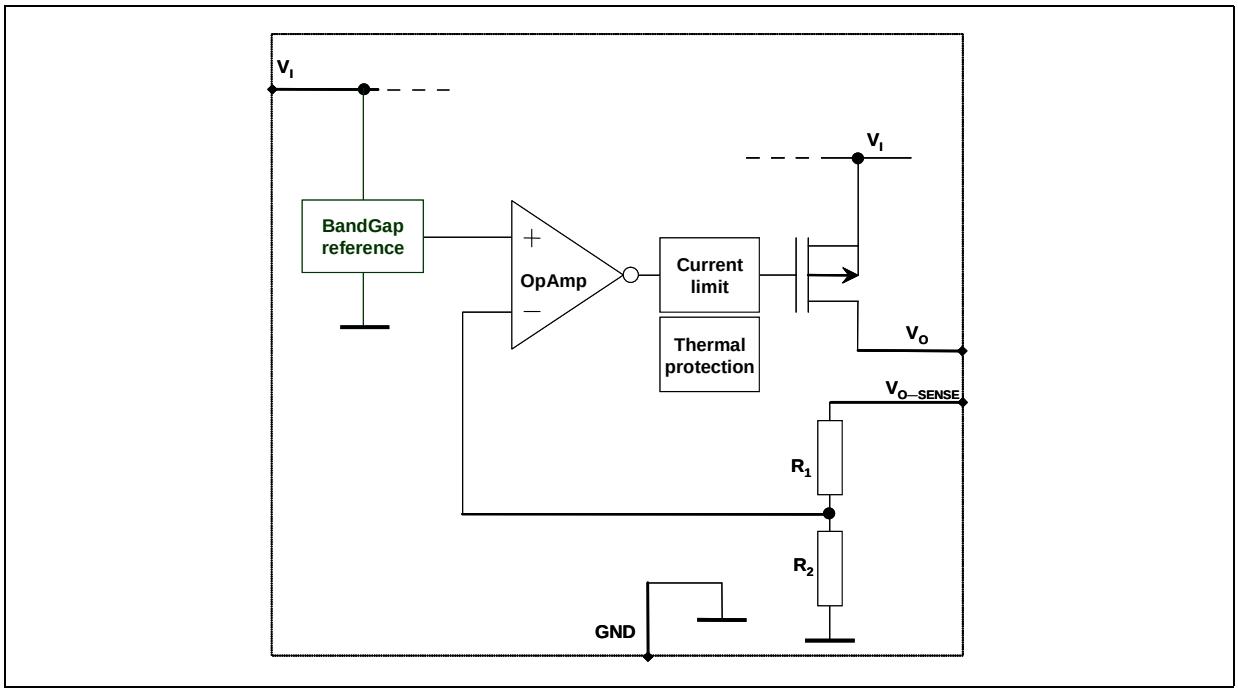


Figure 2. ST1L05A schematic diagram

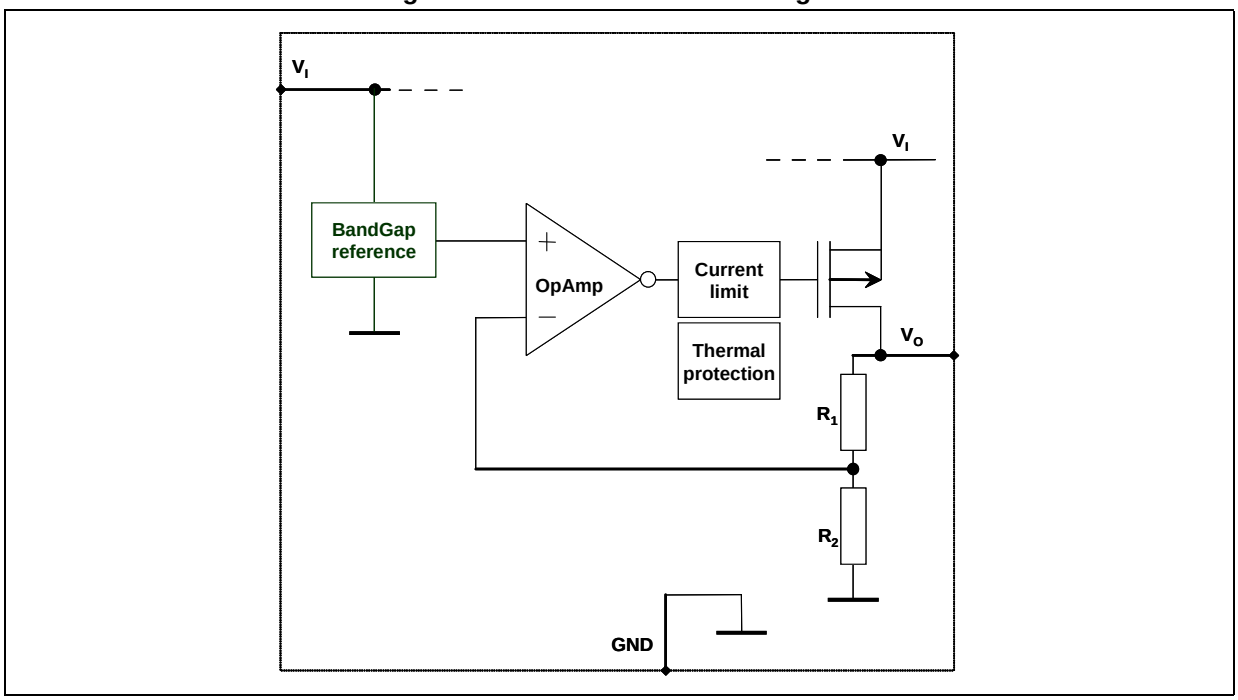


Figure 3. ST1L05B and ST1L05D schematic diagram

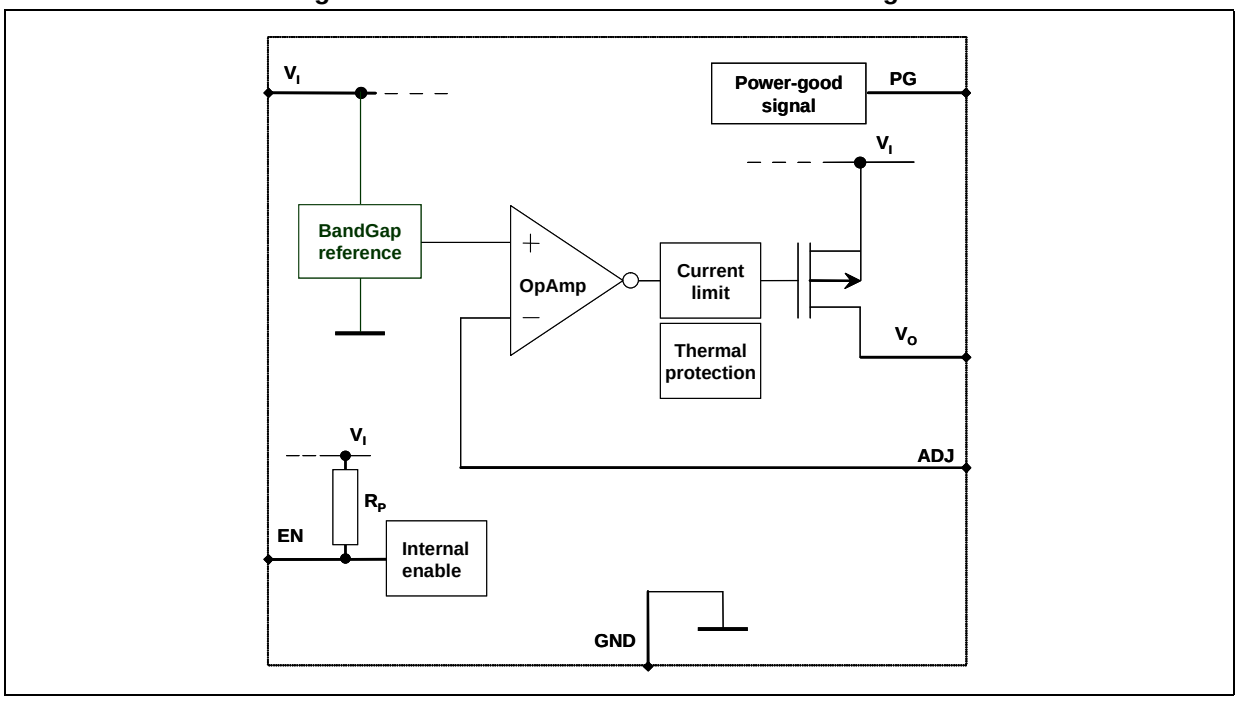
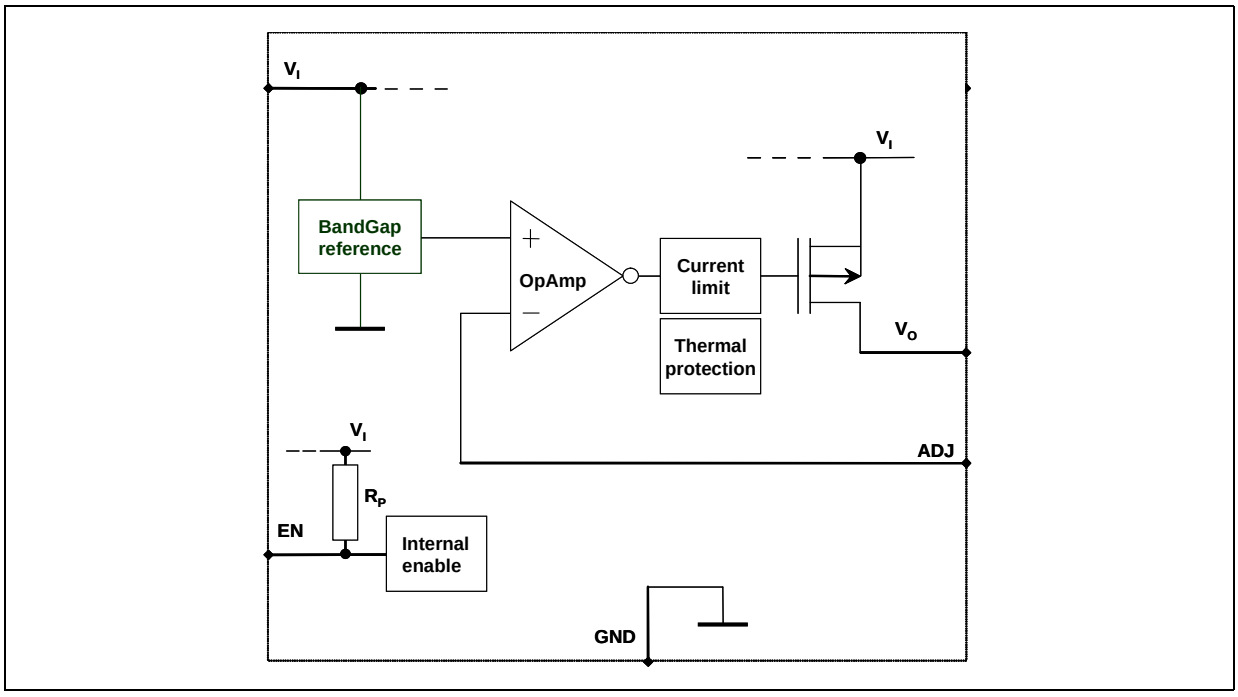


Figure 4. ST1L05C schematic diagram



2 Pin configuration

Figure 5. Pin connections (top view)

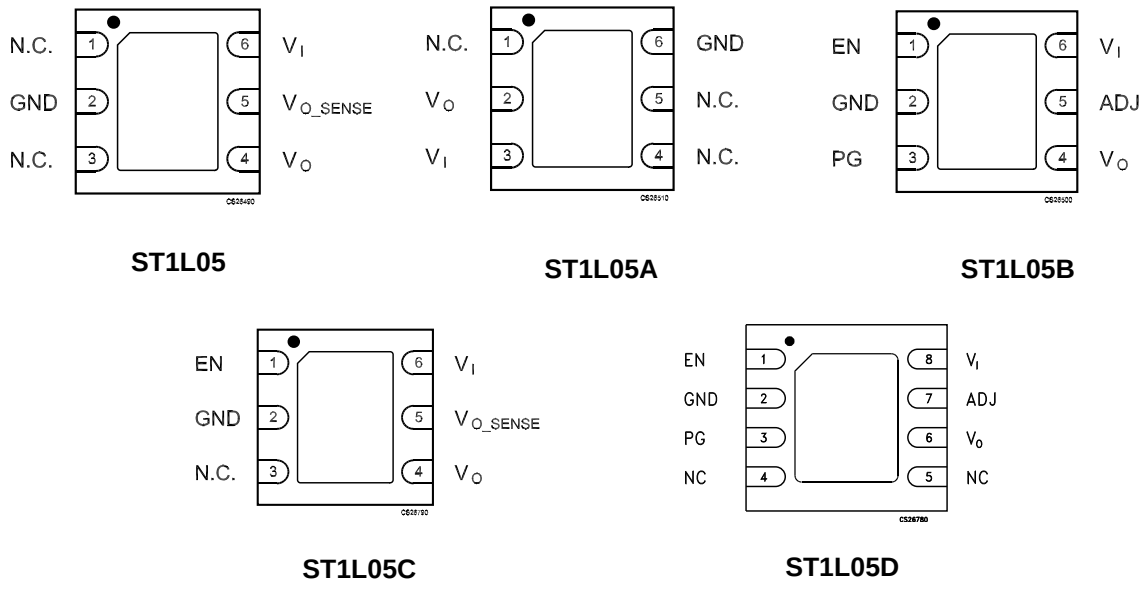


Table 2. Pin description

Symbol	Pin					Function
	ST1L05	ST1L05A	ST1L05B	ST1L05C	ST1L05D	
V_I	6	3	6	6	8	Supply voltage input pin. Bypass with a 4.7 µF capacitor to GND
V_O	4	2	4	4	6	Output voltage pin. Bypass with a 4.7 µF capacitor to GND
GND	2	6	2	2	2	Ground pin
ADJ	-	-	5	-	7	Adjust pin
V_{O_SENSE}	5	-	-	5	-	V_O sense
PG	-	-	3	-	3	Power Good pin
EN	-	-	1	1	1	Enable pin. Internal pull-up to V_I
N.C.	1-3	1-4-5	-	3	4-5	Not connected
GND	Exposed					Exposed pad has to be connected to GND

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC supply voltage	-0.3 to 7	V
V_O	DC output voltage	-0.3 to 7	V
PG	Power Good	-0.3 to 7	V
EN	Enable pin	-0.3 to 7	V
ADJ/V_{OUT_SENSE}	Adjust pin or V_O sense	4	V
P_D	Power dissipation	Internally limited	W
I_O	Output current	Internally limited	A
T_{OP}	Operating junction temperature range	0 to 150	°C
T_{STG}	Storage temperature range(1)	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 seconds	260	°C

1. Storage temperature > 125 °C is acceptable only if the regulator is soldered to a PCBA.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	DFN6	DFN8	Unit
R_{thJC}	Thermal resistance junction-case	10	4	°C/W
R_{thJA}	Thermal resistance junction-ambient	55	40	°C/W

Table 5. ESD data

Symbol	Parameter	Value	Unit
HBM	Human body model	2	kV
MM	Machine model	150	V

4 Electrical characteristics

Refer to the typical application schematic, V_I = 3.3 V to 4.5 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Intended typical value is T_J = 25 °C unless otherwise specified.

Table 6. ST1L05PU25R electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 3.3 V to 5.25 V, T = 25 °C	2.45	2.5	2.55	V
V_O	Output voltage	V_I = 3.3 V to 5.25 V	2.4375	2.5	2.5625	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1.3 A		15	30	mV
I_S	Output current limit	V_I = 5.5 V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8 A		0.2	0.4	V
		I_O = 1 A		0.25	0.45	V
		I_O = 1.3 A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1.3 A, T = 25 °C		350	500	µA
		V_I = 5.5 V, I_O = 2 mA to 1.3 A		350	650	
SVR	Supply voltage rejection(1)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	68		dB
eN	RMS output noise(1)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising)(1)(2)	V_I = 5 V, any 200 mA step from 100 mA to 1.3 A, $t_R \geq 1$ µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling)(1)(2)	V_I = 5 V, I_O = 1.3 A to 10 mA, $t_F \geq 1$ µs			2.75	V
$\Delta V_O/\Delta V_I$	Start-up transient(1)(2)	V_I = 0 V to 5 V, I_O = 10 mA to 1.3 A, $t_R \geq 1$ µs			2.75	V
$\Delta V_O/\Delta I_O$	Short-circuit removal response(1)(2)	V_I = 5 V, I_O = short to 10 mA			2.75	V
T_{SH}	Thermal shutdown trip point(1)	V_I = 5 V		165		°C

1. Guaranteed by design. Not tested in production.
2. C_I = 10 µF, C_O = 10 µF, all X7R ceramic capacitors.

Refer to the typical application schematic, V_I = 4.5 V to 5.5 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Intended typical value is T_J = 25 °C unless otherwise specified.

Table 7. ST1L05APU33R electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25 °C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1.3 A		15	30	mV
I_S	Output current limit	V_I = 5.5 V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8 A		0.2	0.4	V
		I_O = 1 A		0.25	0.45	V
		I_O = 1.3 A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1.3 A, T = 25 °C		350	500	µA
		V_I = 5.5 V, I_O = 2 mA to 1.3 A		350	650	
SVR	Supply voltage rejection(1)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	65		dB
eN	RMS output noise(1)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising)(1)(2)	V_I = 5 V, any 200 mA step from 100 mA to 1.3 A, $t_R \geq 1$ µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling)(1)(2)	V_I = 5 V, I_O = 1.3 A to 10 mA, $t_F \geq 1$ µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient(1)(2)	V_I = 0 V to 5 V, I_O = 10 mA to 1.3 A, $t_R \geq 1$ µs			3.5	V
$\Delta V_O/\Delta I_O$	Short-circuit removal response (1)(2)	V_I = 5 V, I_O = short to 10 mA			3.5	V
T_{SH}	Thermal shutdown trip point(1)	V_I = 5 V		165		°C

1. Guaranteed by design. Not tested in production.
2. C_I = 10µF, C_O = 10µF, all X7R ceramic capacitors.

Refer to the typical application schematic, V_I = 4.5 V to 5.5 V, V_{EN} = 2 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Intended typical value is T_J = 25 °C unless otherwise specified.

Table 8. ST1L05CPU33R electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 4.75 V to 5.25 V, T = 25 °C	3.234	3.3	3.366	V
V_O	Output voltage	V_I = 4.75 V to 5.25 V	3.2175	3.3	3.3825	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1.3 A		15	30	mV
I_S	Output current limit	V_I = 5.5 V	1.3			A
I_{OMIN}	Minimum output current for regulation				0	mA
V_d	Dropout voltage	I_O = 0.8 A		0.2	0.4	V
		I_O = 1 A		0.25	0.45	V
		I_O = 1.3 A		0.3	0.5	V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1.3 A, T = 25 °C		350	500	µA
		V_I = 5.5 V, I_O = 2 mA to 1.3 A		350	650	
V_{EN_H}	Enable threshold high	V_I = 4.5 V to 5.25, I_O = 50 mA	2			V
V_{EN_L}	Enable threshold low	V_I = 4.5 V to 5.25, I_O = 50 mA			0.8	
I_{EN}	Enable pin current	$V_{EN} = V_I$ = 5 V			2	µA
SVR	Supply voltage rejection(1)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	65		dB
eN	RMS output noise(1)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising) (1)(2)	V_I = 5 V, any 200 mA step from 100 mA to 1.3 A, $t_R \geq 1$ µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling)(1)(2)	V_I = 5 V, I_O = 1.3 A to 10 mA, $t_F \geq 1$ µs			3.6	V
$\Delta V_O/\Delta V_I$	Start-up transient (1)(2)	V_I = 0 V to 5 V, I_O = 10 mA to 1.3 A, $t_R \geq 1$ µs			3.5	V
$\Delta V_O/\Delta I_O$	Short-circuit removal response (1)(2)	V_I = 5 V, I_O = short to 10 mA			3.5	V
T_{SH}	Thermal shutdown trip point(1)	V_I = 5 V		165		°C

1. Guaranteed by design. Not tested in production.
2. C_I =10 µF, C_O =10 µF, all X7R ceramic capacitors.

Refer to the typical application schematic, V_I = 3 V to 5.5 V, V_{EN} = 2 V, I_O = 5 mA to 1.3 A, $C_I = C_O$ = 4.7 µF, T_J = 0 to 125 °C, unless otherwise specified. Intended typical value is T_J = 25 °C unless otherwise specified.

Table 9. ST1L05BPUR and ST1L05DPUR electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	V_I = 3 V to 5.25 V, T = 25 °C	1.195	1.22	1.245	V
V_O	Output voltage	V_I = 3 V to 5.25 V	1.18	1.22	1.256	V
ΔV_O	Line regulation	V_I = 4.75 V to 5.25 V			15	mV
ΔV_O	Load regulation	V_I = 4.75 V, I_O = 10 mA to 1.3 A		15	30	mV
I_{ADJ}	Adjust pin current	V_I = 3 V to 5.25 V		1		nA
I_S	Output current limit	V_I = 5.5 V	1.3			A
I_{OMIN}	Minimum output current for regulation				1	mA
V_d	Dropout voltage (1)	I_O = 0.8 A, V_O = 3.3 V		0.2		V
		I_O = 1 A, V_O = 3.3 V		0.25		V
		I_O = 1.3 A, V_O = 3.3 V		0.3		V
I_Q	Quiescent current	V_I = 5 V, I_O = 2 mA to 1.3 A, T = 25 °C		300	500	µA
		V_I = 5.5 V, I_O = 2 mA to 1.3 A		350	650	
		Device OFF(2)			1	
V_{EN_H}	Enable threshold high	V_I = 3 V to 5.25, I_O = 50 mA	2			V
V_{EN_L}	Enable threshold low	V_I = 3 V to 5.25, I_O= 50 mA			0.8	
I_{EN}	Enable pin current	$V_{EN} = V_I$ = 5 V			2	µA
PG	Power Good output threshold	Rising edge		0.92 V_O		V
		Falling edge		0.8 V_O		
	Power Good output voltage low(3)	I_{SINK} = 6 mA open drain output			0.4	V
SVR	Supply voltage rejection(3)	V_I = 5 ± 0.5 V, I_O = 5 mA, f = 120 Hz	50	72		dB
eN	RMS output noise(3)	B = 10 Hz to 10 kHz, V_I = 5 V, I_O = 5 mA		0.003		$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (rising)(3)(4)	V_I = 5 V, any 200 mA step from 100 mA to 1.3 A, $t_R \geq 1$ µs			5	$\%V_O$
$\Delta V_O/\Delta I_O$	Load transient (falling)(3)(4)	V_I = 5 V, I_O = 1.3 A to 10 mA, $t_F \geq 1$ µs			1.38	V
$\Delta V_O/\Delta V_I$	Start-up transient(3)(4)	V_I = 0 V to 5 V, I_O = 10 mA to 1 A, $t_R \geq 1$ µs			1.38	V

Table 9. ST1L05BPUR and ST1L05DPUR electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta V_O/\Delta I_O$	Short-circuit removal response(3)(4)	V_I = 5 V, I_O = short to 10 mA			1.38	V
T_{SH}	Thermal shutdown trip point (3)	V_I = 5 V		165		°C

1. See minimum start-up voltage, V_I = 2.9 V.
2. PG pin floating.
3. Guaranteed by design. Not tested in production.
4. C_I = 10 µF, C_O = 10 µF, all X7R ceramic capacitors.

5 Typical characteristics

Figure 6. Output voltage vs temperature V_O = 1.22 V, I_O = 10 mA

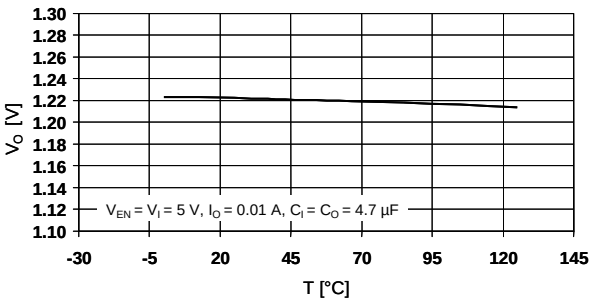


Figure 7. Output voltage vs temperature V_O = 1.22 V, I_O = 1.3 A

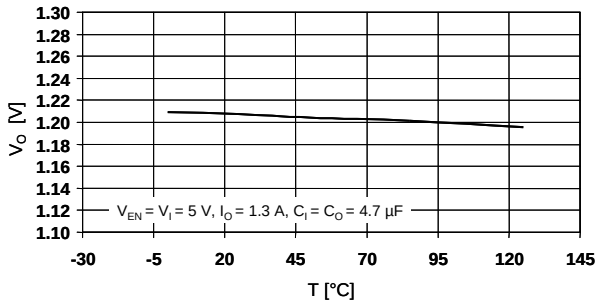


Figure 8. Output voltage vs temperature V_O = 2.5 V, I_O = 10 mA

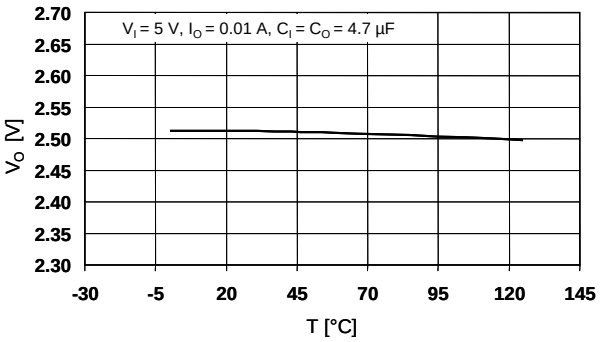


Figure 9. Output voltage vs temperature V_O = 2.5 V, I_O = 1.3 A

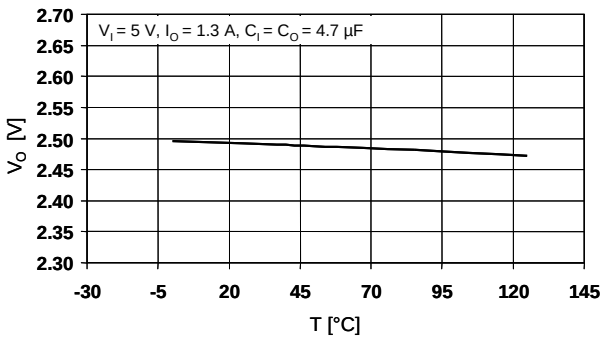


Figure 10. Line regulation vs temperature

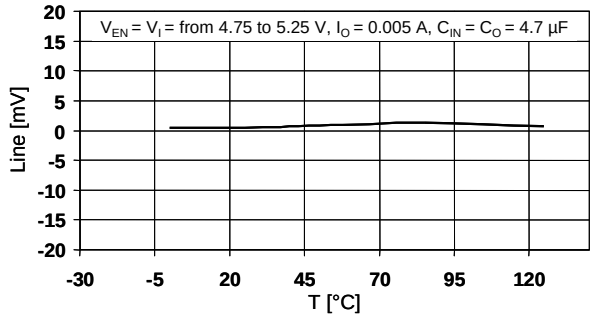


Figure 11. Load regulation vs temperature

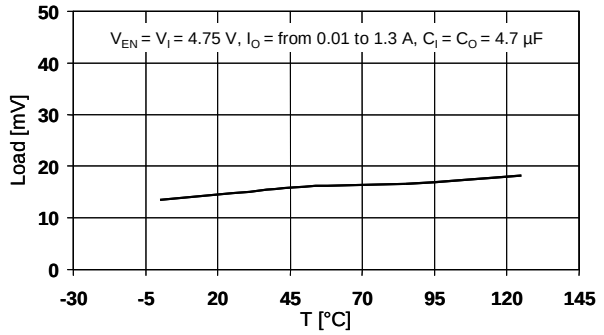


Figure 12. Dropout voltage vs temperature

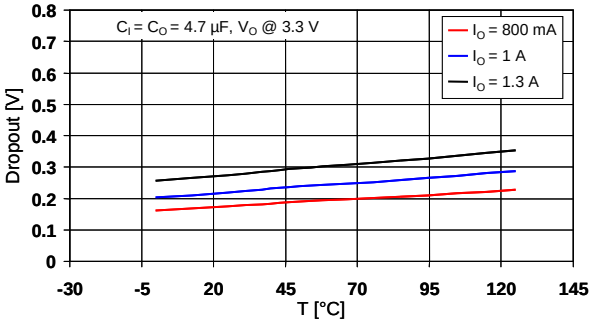


Figure 13. ESR required for stability with ceramic capacitors

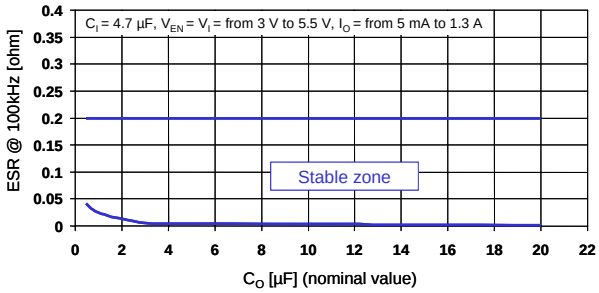


Figure 14. Quiescent current vs temperature

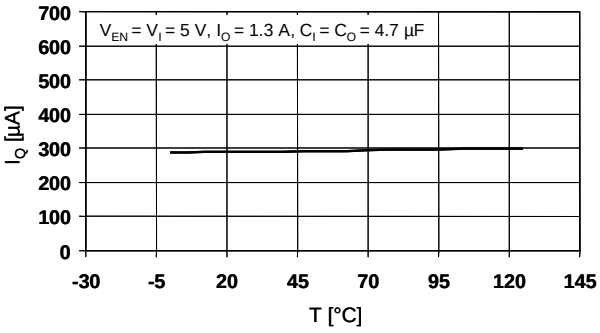


Figure 15. Quiescent current vs output current

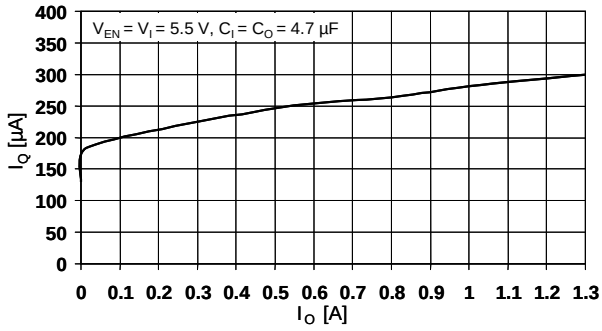


Figure 16. Enable voltage vs temperature V_I = 3 V

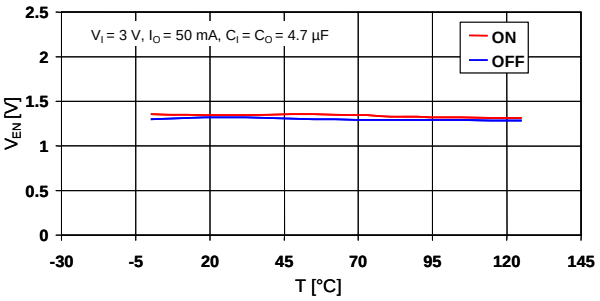


Figure 17. Enable voltage vs temperature V_I = 5.25 V

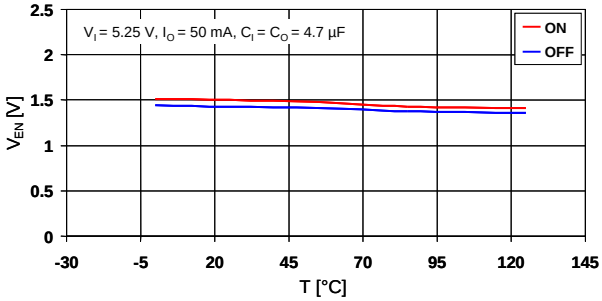


Figure 18. Supply voltage rejection vs temperature

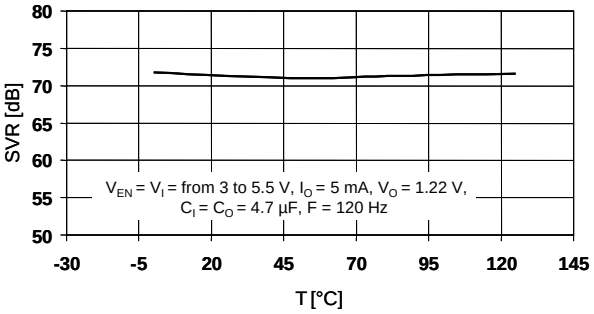


Figure 19. Supply voltage rejection vs frequency

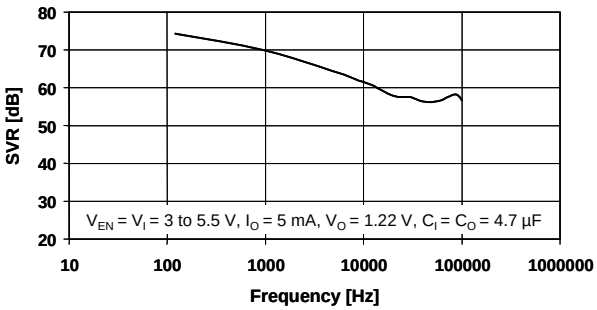
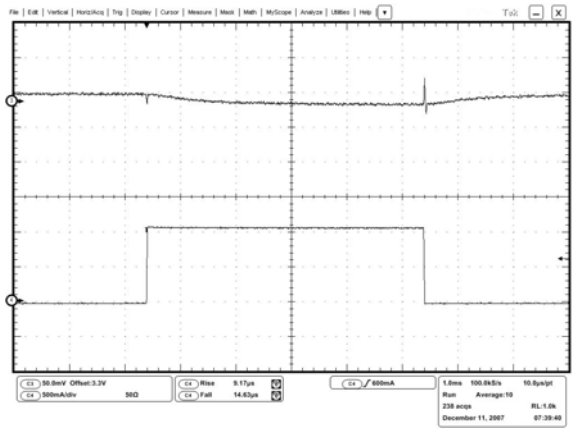
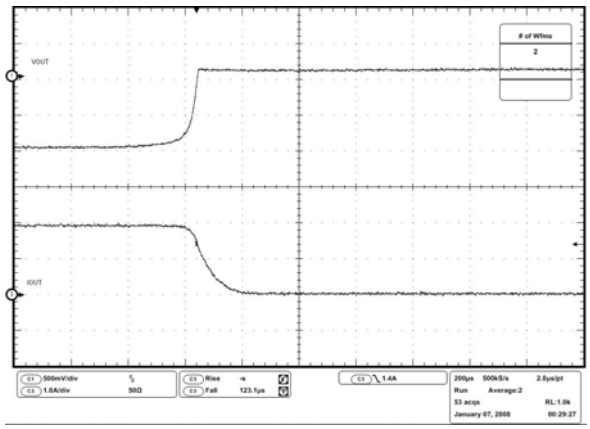


Figure 20. Load transient



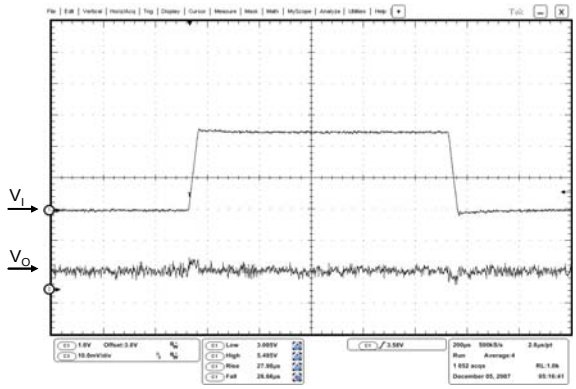
I_O=10 mA to 1.3 A, C_I=C_O=10 µF, V_{EN}=V_I=5 V, V_O@3.3 V

Figure 21. Short-circuit removal transient



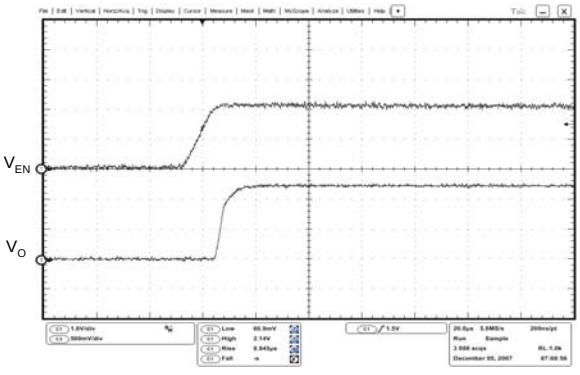
I_O=10 mA to short, C_I=C_O=10 µF, V_{EN}=V_I=5.5 V

Figure 22. Line transient



C_I=C_O=4.7 µF, V_I=3 to 5.5V, I_O=5 mA

Figure 23. Enable transient



C_O=C_I=4.7 µF, V_{EN}=0 to 2 V, V_I=5.5 V, I_O=5 mA

6 Application information

The ST1L05 is a low-dropout linear regulator. It provides up to 1.3 A with a low 300 mV dropout. The input voltage range is from 3 V to 5.5 V. The device is available in fixed and adjustable output versions.

The regulator is equipped with internal protection circuitry, such as short-circuit current limiting and thermal protection.

The regulator is designed to be stable with ceramic capacitors on the input and the output. The expected values of the input and output ceramic capacitors are from 1 µF to 22 µF with 4.7 µF typical. The input capacitor has to be connected within 1 cm from V_I terminal. The output capacitor has also to be connected 1 cm far from output pin. There isn't any upper limit to the value of the input capacitor.

Figure 24, *Figure 25*, *Figure 26* and *Figure 27* illustrate the typical application schematics:

Figure 24. ST1L05 application schematic

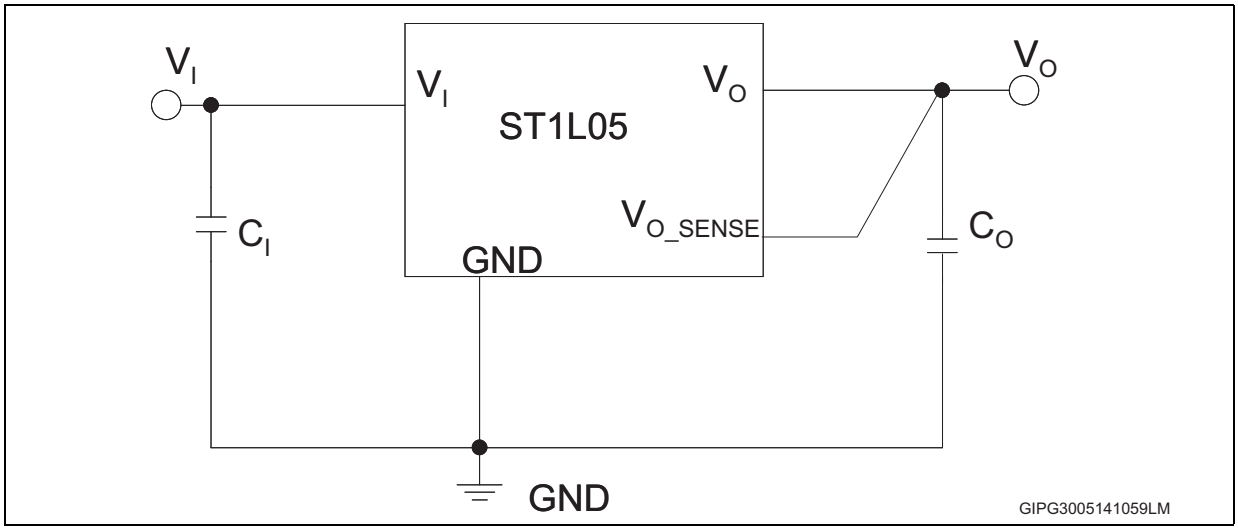


Figure 25. ST1L05A application schematic

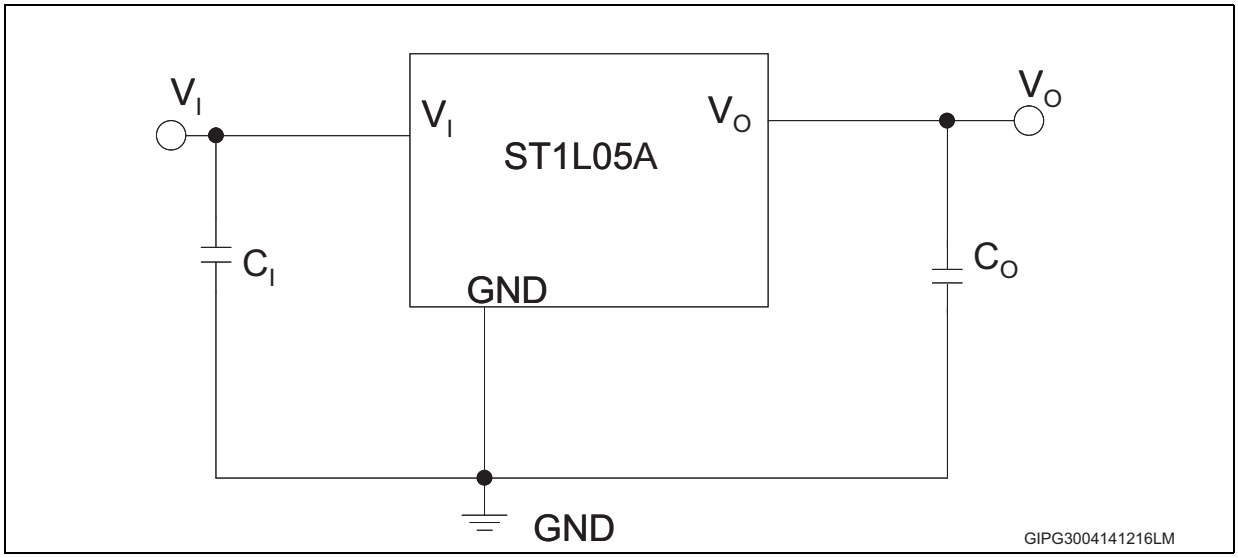


Figure 26. ST1L05B and ST1L05D application schematic

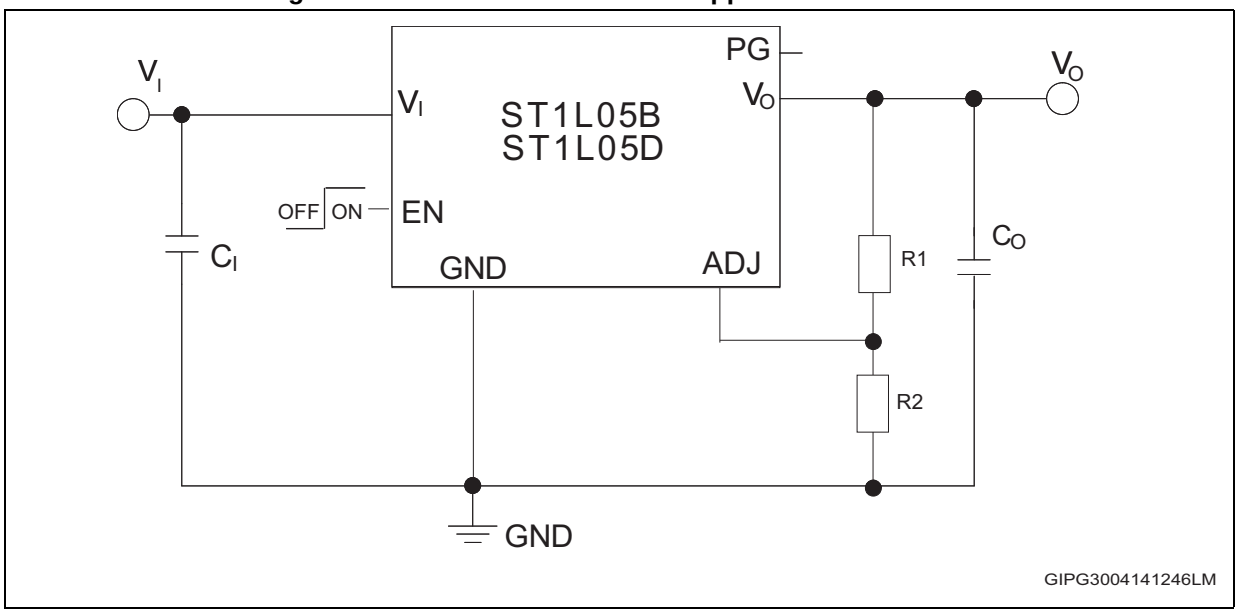
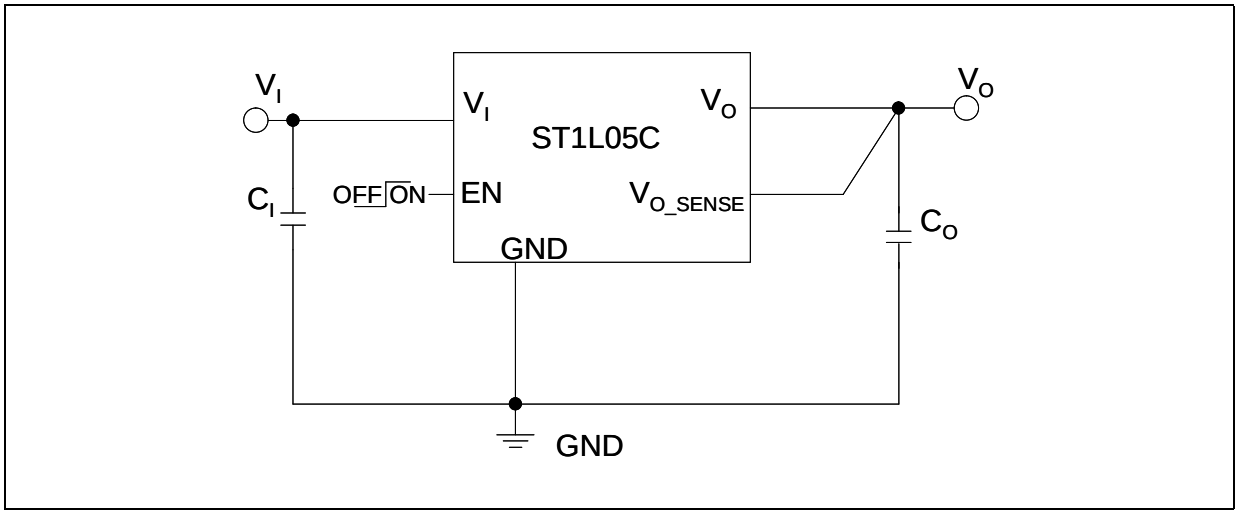


Figure 27. ST1L05C application schematic



Regarding to the adjustable version, the output voltage can be adjusted from 1.22 V up to the input voltage, minus the voltage drop across PMOS (dropout voltage), by connecting a resistor divider between ADJ pin and the output, thus allowing remote voltage sensing. The resistor divider should be selected according to the following equation:

Equation 1

$V_O = V_{ADJ} (1 + R_1 / R_2)$ with $V_{ADJ} = 1.22$ V (typ.)

Resistors should be used with values in the range from 10 kΩ to 100 kΩ. Lower values can also be suitable, but they increase current consumption.

6.1 Power dissipation

An internal thermal feedback loop disables the output voltage if the die temperature rises to approximately 165 °C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device.

A good PC board layout should be used to maximize the power dissipation. Thermal path goes from the die to the copper lead frame through the package leads and exposed pad to the PC board copper. The PC board copper works as a heatsink. Footprint copper pads should be as wider as possible to spread and dissipate the heat to the surrounding ambient. Feed-through vias to inner or backside copper layers are also useful to improve the overall thermal performance of the device.

Power dissipation of the device depends on the input voltage, output voltage and output current, and is given by:

Equation 2

$P_D = (V_I - V_O) I_O$

The junction temperature of the device is:

$T_{J\_MAX} = T_A + R_{thJA} \times P_D$

where:

T_{J_MAX} is the maximum junction of the die, 125 °C

T_A is the ambient temperature

R_{thJA} is the thermal resistance junction-to-ambient

6.2 Enable function (ST1L05B, ST1L05C and ST1L05D only)

The ST1L05 features the enable function. When EN voltage is higher than 2 V the device is ON, and if it is lower than 0.8 V the device is OFF. In shutdown mode, consumption is lower than 1 µA. EN pin has an internal pull-up, so it can be left floating if it is not used.

6.3 Power Good function (ST1L05B and ST1L05D only)

Most applications require a flag showing that the output voltage is in the correct range.

Power Good threshold depends on the adjust voltage. When the adjust is higher than $0.92*V_{ADJ}$, Power Good (PG) pin goes to high impedance. If the adjust is below $0.92*V_{ADJ}$ PG pin goes to low impedance. If the device works correctly, Power Good pin is at high impedance.

If the output voltage is fixed using an external or internal resistor divider, Power Good threshold is $0.92*V_O$.

To use Power Good function, an external pull-up resistor is required, and it has to be connected between PG pin and V_I or V_O. PG pin typical current capability is up to 6 mA. A pull-up resistor in the range of 100 kΩ to 1 MΩ is recommended. If Power Good function is not used, PG pin has to remain floating.

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 28. DFN6 (3x3 mm) drawings

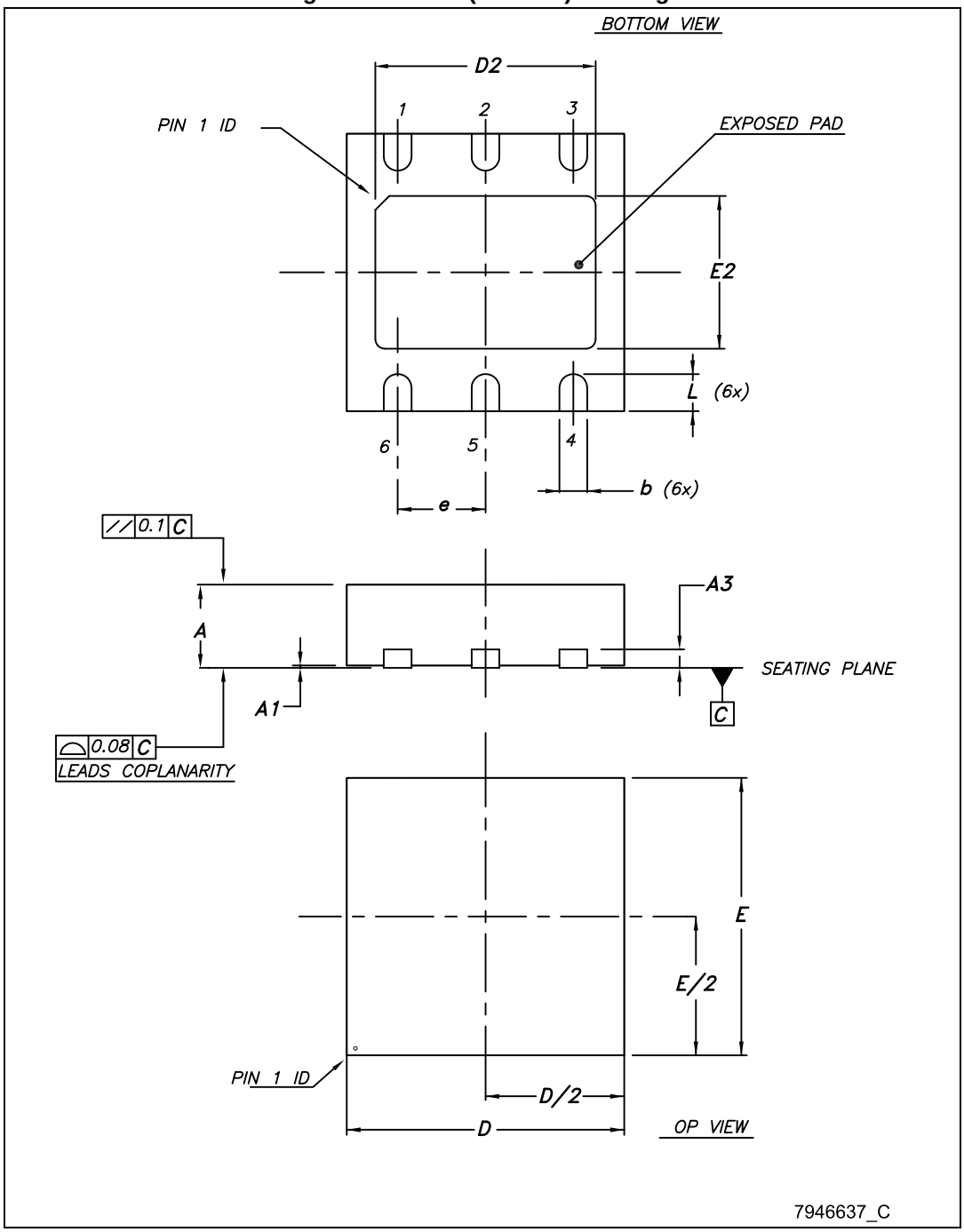


Table 10. DFN6 (3x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
		0.95	
L	0.30	0.40	0.50

Figure 29. DFN6 (3x3 mm) recommended footprint

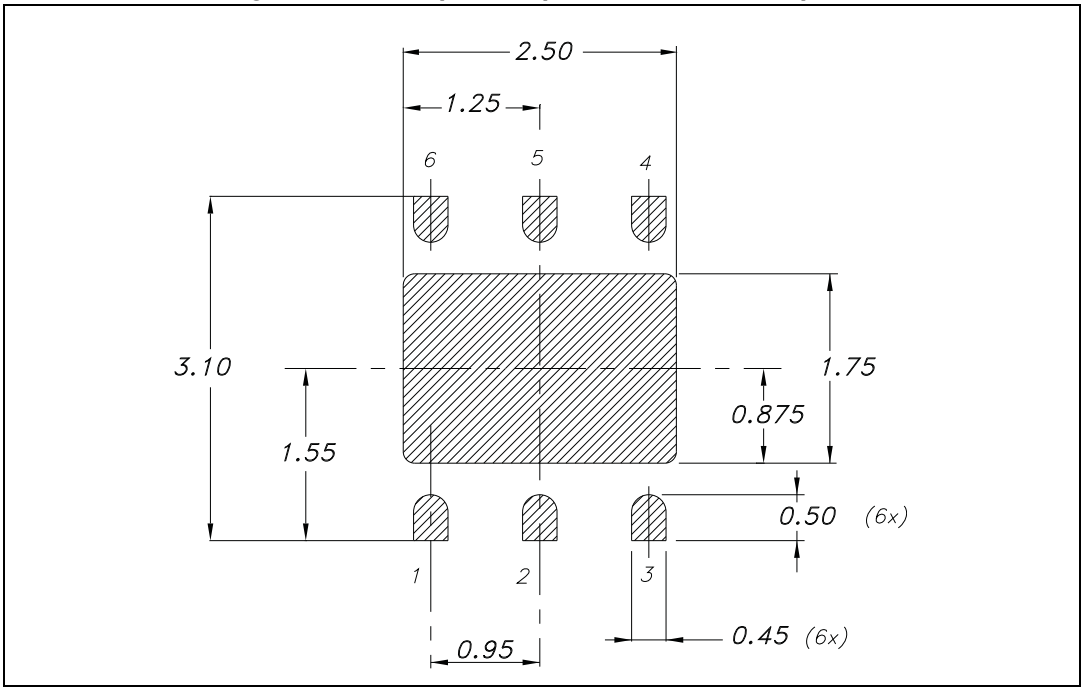


Figure 30. DFN8 (4x4 mm) drawings

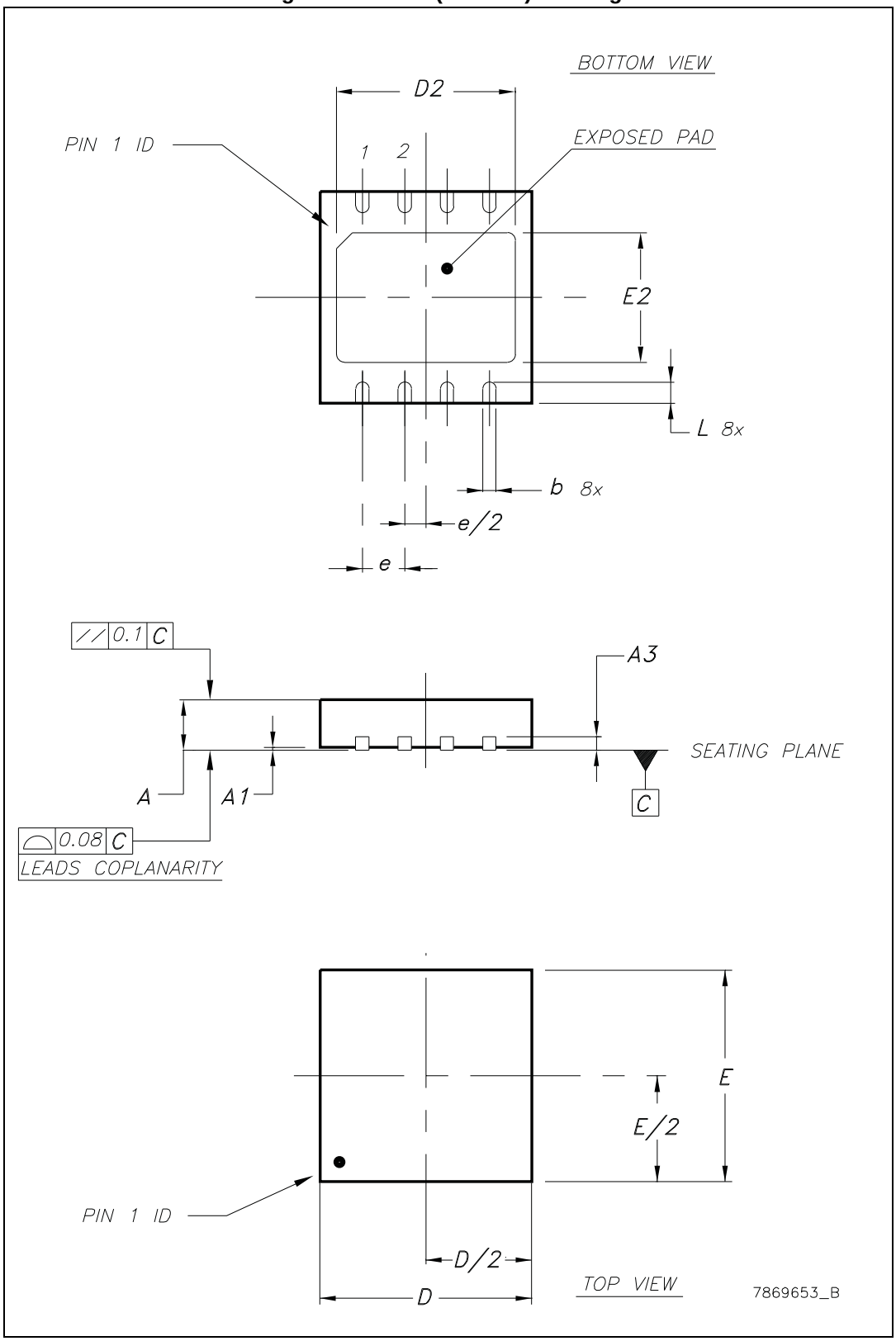
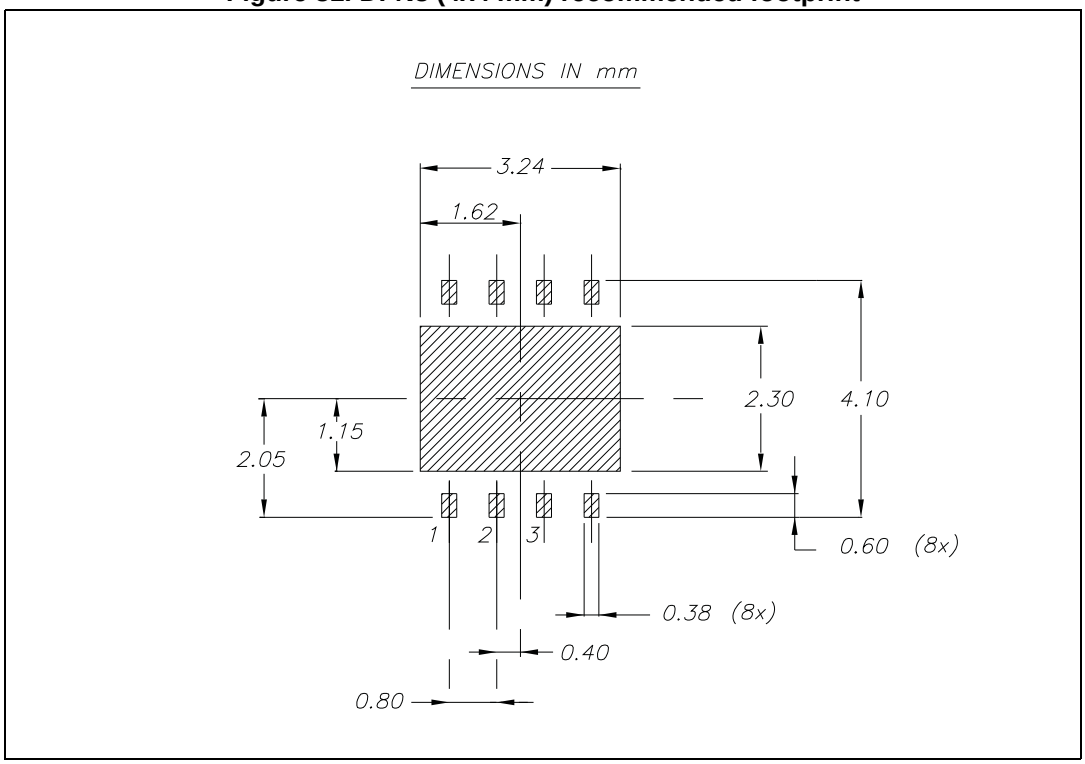


Table 11.DFN8 (4x4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0	0.02	0.05
A3		0,20	
b	0.23	0.30	0.38
D	3.90	4	4.10
D2	2.82	3	3.23
E	3.90	4	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 31. DFN8 (4x4 mm) recommended footprint



8 Packaging mechanical data

Figure 32. DFN6 (3x3 mm) tape

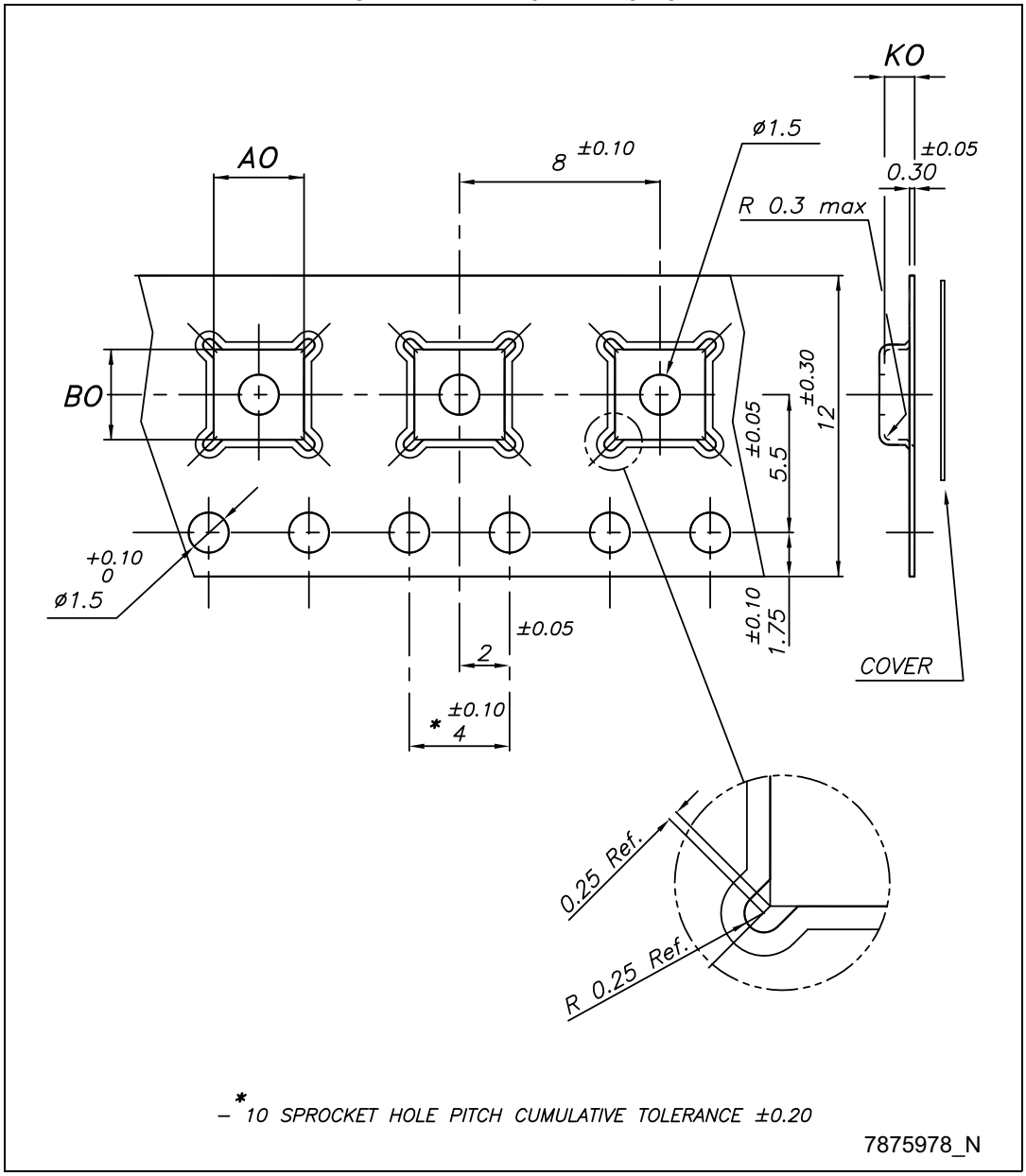


Figure 33. DFN6 (3x3 mm) reel

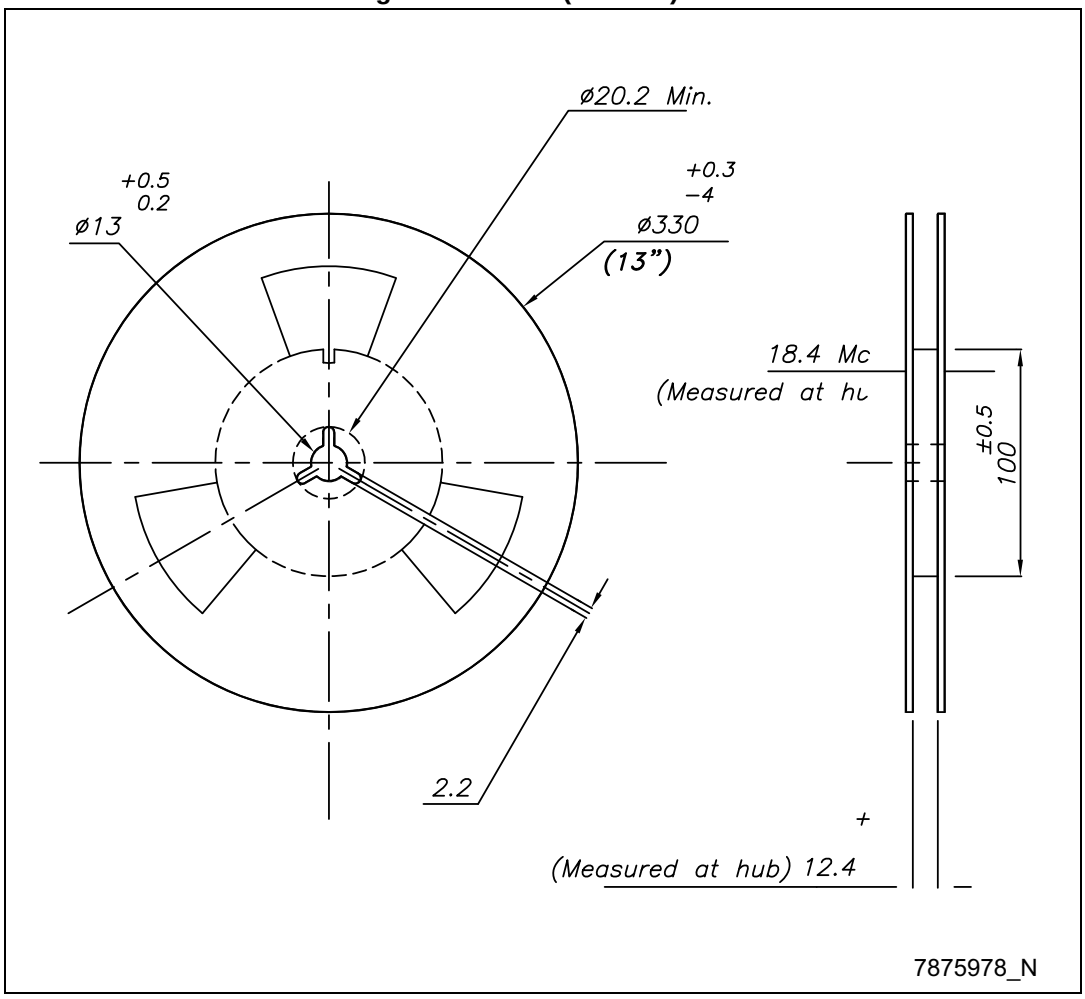
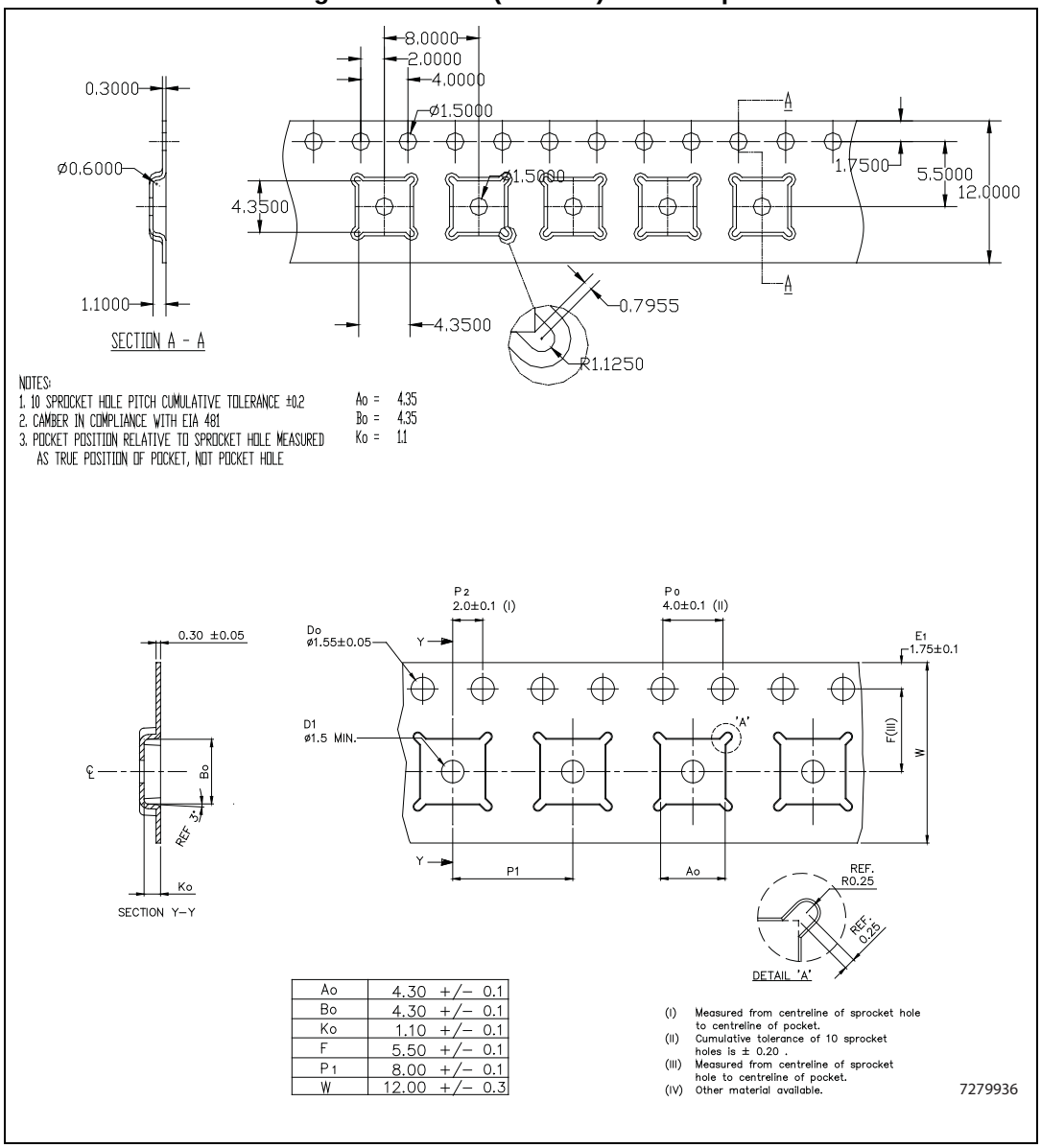


Table 12. DFN6 (3x3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

Figure 34. DFN8 (4x4 mm) carrier tape



Ao	4.30 +/- 0.1
Bo	4.30 +/- 0.1
Ko	1.10 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

Figure 35. DFN8 (4x4 mm) reel

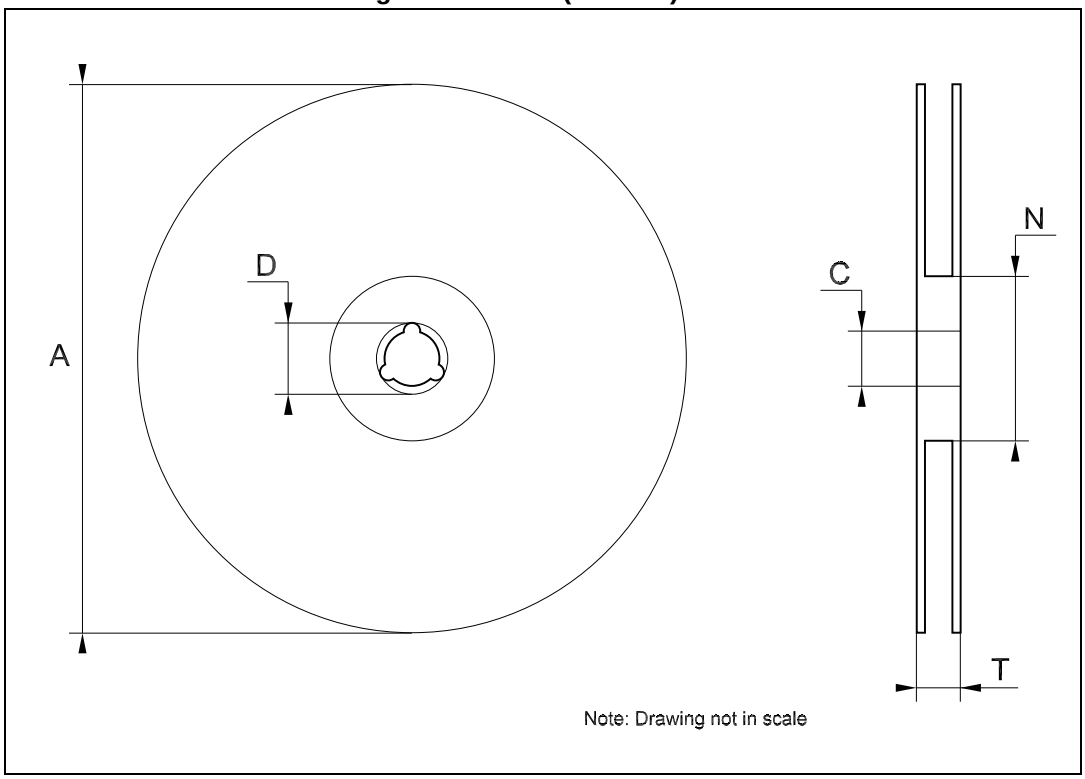


Table 13. DFN8 (4x4 mm) reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8	13.0	13.2
D	20.2		
N	60		
T			22.4

9 Revision history

Table 14. Document revision history

Date	Revision	Changes
29-Feb-2008	1	First release.
07-Jul-2009	2	Added: package DFN8 (4 x 4 mm).
05-May-2014	3	Part numbers: ST1L05A, ST1L05B, ST1L05C, ST1L05D have been included in the ST1L05 for product rationalization. Changed title of *Figure 6*, *Figure 7*, *Figure 8*, *Figure 9*, *Figure 16* and *Figure 17*. Updated package mechanical data. Added *Section 8*.

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