

Implementation of A Neuron Using Sigmoid Activation Function with CMOS

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Abstract—A multi-input neuron circuit with high-precision Sigmoid activation function (AF) is presented in this paper. The proposed circuit composed of input signal weighting circuit, current-voltage conversion circuit, and Sigmoid AF fitting circuit. Designed circuit can fit Sigmoid function based on the current-voltage relationship of differential pairs. The circuit is simulated in TSMC 0.18 μm CMOS technology. The post-simulation shows that the error between the output of Sigmoid AF fitting circuit and the ideal Sigmoid function is 1.76%. The area of the layout is 375 $\mu\text{m} \times 238 \mu\text{m}$. The maximum error caused by noise in the output of the circuit is 80 $\text{pA}/\sqrt{\text{Hz}}$.

Keywords-artificial neural networks; neuron circuit; sigmoid; activation function; CMOS

I. INTRODUCTION

In the last decade, the interest to emulate of the functionality and structure of the human brain to solve the problems related to pattern recognition, classification, optimization, signal processing and control systems, especially using Artificial Neural Networks (ANNs), has significantly increased [1]. The capability of ANNs to perform at highspeed has been proven to be very useful for various large-scale problems. Ability and performance to make decision of ANNs mostly depend on the type of AF and network structure. Therefore, to simplify the structure of the network, accelerate the time of convergence and the learning outcome of ANNs, it is necessary to design a high-precision AF neuron that will meet these properties. Variety of neuron AFs have been proposed in last decades, such as the step, identity, rectified-linear unit (ReLU), and Sigmoid. The Sigmoid function with the nonlinear ability and performance of its derivative become a commonly used AF in ANNs [2]. Most of the work in this field consist of software simulations, investigating capabilities of ANN models or new algorithms. However, hardware implementations are also essential for applicability and for taking the advantage of neural network's inherent parallelism [3], [4]. The hardware implementations of the AFs involve complicated circuit and a considerable amount of power dissipation [5], [6], [7]. Thus, it is necessary to design a high-precision, simple structure Sigmoid AF neuron circuit by hardware technology.

In this paper, a high-precision Sigmoid AF neuron for the ANNs is presented [8], [9]. Compared with the traditional Sigmoid circuits, the design of the current-voltage conversion (I-V) circuit can provide a simplified circuit structure, small chip area and a large input range [10]. As the most basic unit

of ANNs, ANNs circuit can be composed by multiple neural circuit directly and reduce the design time.

The rest of the paper is organized as follows. Section II and Section III introduce the background of neuron and the introduction of proposed neuron circuit. the simulation results are presented in Section IV followed by the conclusions in Section V.

II. BACKGROUND OF NEURON

Fig.1 illustrates the transfer characteristics of the Sigmoid function and these characteristics described in equation (1).

$$f(x) = \frac{1}{1+e^{-x}} \quad (1)$$

The simplest model of a neuron is illustrated in Fig.2.

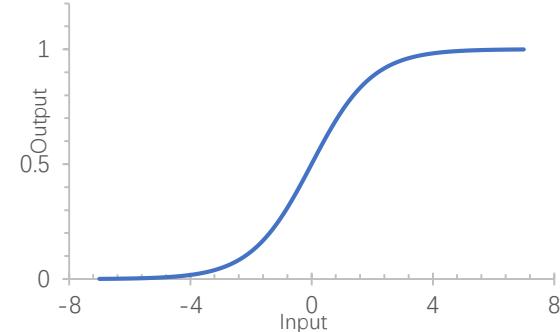


Figure 1. Sigmoid function.

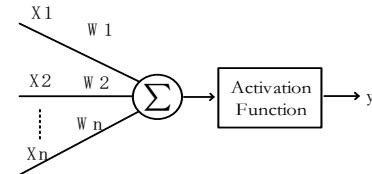


Figure 2. Basic model of neuron.

The output of the simplest neuron can be written in the form given in equation (2).

$$y = f(\sum_{i=1}^{i=n} X_i * W_i) \quad (2)$$

where X_i and W_i are the input and weight of the neuron, respectively and the function f is AF.

III. PROPOSED CIRCUIT

The schematic of high-precision Sigmoid AF neuron circuit is shown in Fig. 3. The circuit composed of three parts:

input signal weighting circuits, I-V circuit, and Sigmoid AF fitting circuit.

A. Input Signal Weighting Circuit

The signal weighting circuit is composed of M1-M10, which is used to linearly weight the input signal to the adder.

$$\frac{W}{L}(M7) \cdot \frac{W}{L}(M9) = \frac{W}{L}(M8) \cdot \frac{W}{L}(M10) = 1:w_1 \quad (3)$$

The designed weighting circuit can both weigh the positive and negative input current signal. The CMOS switch and the signal transmission path are determined by the

property of input signal. When the input signal X_1 is positive (the current flow into the circuit), the PMOS M7 and M9 are on, and the NMOS M8 and M10 are off.

When the input signal X_1 is negative (the current flow out of the circuit), the PMOS M7 and M9 are off, and the NMOS M8 and M10 are on, so

$$I_1 = X_1 * W_1 \quad (4)$$

The simulation of signal weighting circuit (Fig. 4) shows that the circuit can linearly weigh the input current signal without distortion.

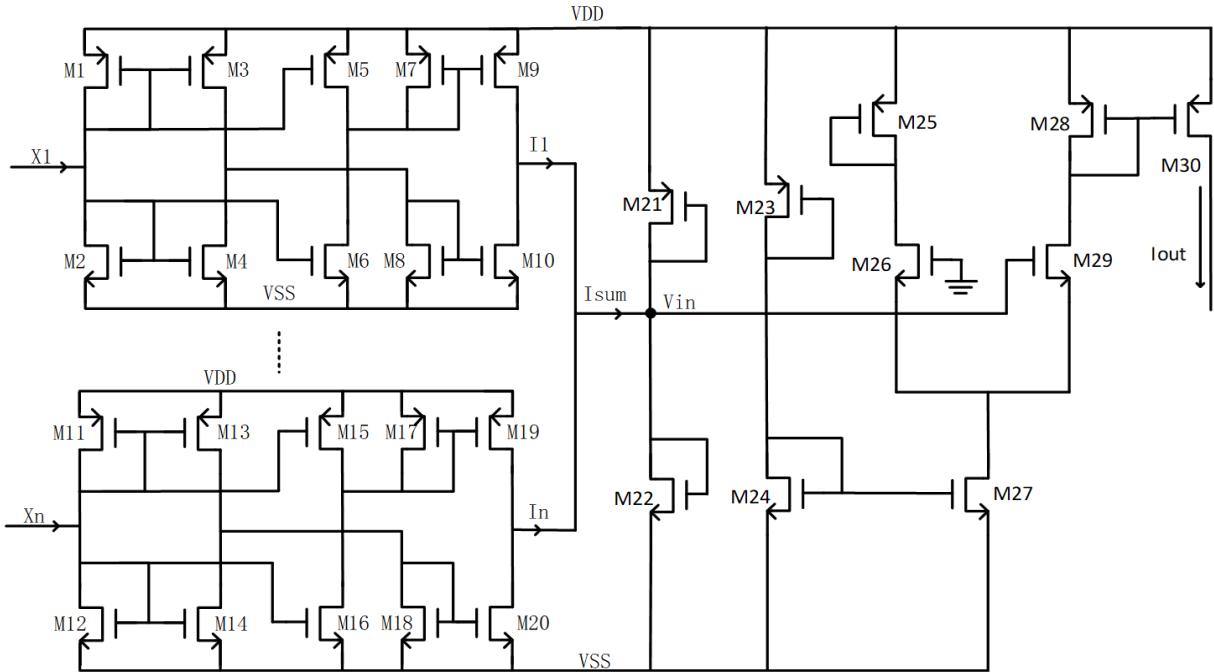


Figure 3. The schematic of the proposed neuron circuit.

In practice, most of neurons have n input signals, and the designer can construct the input module through n signal weighting circuits directly.

$$I_{sum} = \sum_{i=1}^{i=n} X_i * W_i \quad (5)$$

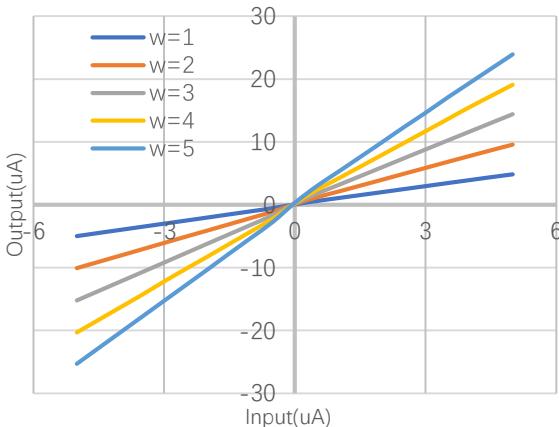


Figure 4. The simulation of signal weighting circuit.

B. I-V Circuit

The signal of ANNs circuit is transmitted by current, while the input signal of Sigmoid AF circuit is voltage. Therefore, it is necessary to design a I-V circuit (Fig.5) composed of M21 and M22 that convert the current of input signal to voltage. Concerned with the ideal relationship between the current and voltage of this circuit. The behavior for the current-voltage relationship of CMOS transistor in saturation is

$$I_d = K(V_{GS} - V_{TH})^2 \quad (6)$$

Consider the circuit of Fig.5, consisting of two CMOS transistors M21 and M22. The gate-source voltage of M21 is equal to $V_{in} - VDD$ and the gate-source voltage of M22 is equal to $V_{in} - VSS$. Using (6) we may write the circuit equations as

$$I1 = K_P(V_{in} - VDD - V_{TP})^2 \quad (7)$$

$$I2 = K_N(V_{in} - VSS - V_{TN})^2 \quad (8)$$

$$VDD = -VSS \quad (9)$$

$$In = I2 - I1 \quad (10)$$

where K_P and K_N are the conductivity parameters of the PMOS M21 and NMOS M22, respectively and V_T is the threshold voltage of CMOS. The parameters of M21 and M22 are matched, $K_N = K_P, V_{TN} = -V_{TP}$.

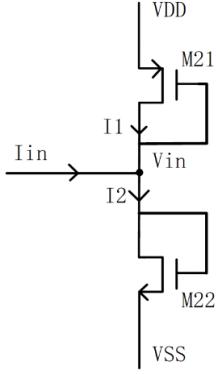


Figure 5. Current-Voltage conversion circuit.

With (7) - (10), the V_{in} may be written as

$$V_{in} = \frac{I_{in}}{4K_N(V_{DD}-V_{TN})} = k * I_{in} \quad (11)$$

where, $k = \frac{1}{4K_N(V_{DD}-V_{TN})}$.

C. Sigmoid AF Fitting Circuit

Sigmoid AF fitting circuit which consists of a current bias circuit and a differential pairs [11]. M23, M24 and M27 constitute the current bias circuit which provides a stable bias current (I_{bias}) for the differential pairs.

To prove this circuit can fit Sigmoid function, we can use (6) to write the circuit equations as

$$I_{DM26} = K_N(V_{GSM26} - V_{TH})^2 \quad (12)$$

$$I_{DM29} = K_N(V_{GSM29} - V_{TH})^2 \quad (13)$$

$$I_{DM26} + I_{DM29} = I_{bias} \quad (14)$$

With (12) -(14), the I_{DM29} may be written as

$$I_{DM29} = \frac{1}{2}I_{bias} + \frac{1}{2}K_NV_{in}\sqrt{\frac{2I_{bias}}{K_N}} - V_{in}^2 \quad (15)$$

where K_N is the conductivity parameter of M26 and M29.

I_{DM29} derivative to V_{in}

$$\frac{\partial I_{DM29}}{\partial V_{in}} = K_N \frac{\frac{I_{bias}-V_{in}^2}{K_N}}{\sqrt{\frac{2I_{bias}-V_{in}^2}{K_N}}} \quad (16)$$

From (16), When $V_{in} \leq -\sqrt{\frac{I_{bias}}{K_N}}$, the transconductance of M29 approaches zero, the drain current of M29 remains unchanged as the gate voltage of M29 decreasing, and then reaches the minimum value of zero; When $-\sqrt{\frac{I_{bias}}{K_N}} \leq V_{in} \leq \sqrt{\frac{I_{bias}}{K_N}}$, the transconductance of M29 is greater than zero and increases slowly, the drain current of M29 augments rapidly with the increasing of the gate voltage of M29. Especially,

when $V_{in} = 0$, the drain current of M29 is $\frac{1}{2}I_{bias}$; When $V_{in} \geq \sqrt{\frac{I_{bias}}{K_N}}$, the transconductance of M29 approaches zero, and the drain current of M29 remains unchanged as the gate voltage of M29 increasing, and then reaches the maximum value of I_{bias} .

With the above analysis, it can be seen that the drain current of M29 in this circuit is approximate to the ideal Sigmoid function, and the error between the fitting function and the ideal function is related to the CMOS parameters.

IV. SIMULATION RESULTS

Fig.6 shows the layout of the proposed two-inputs and one-output high-precision Sigmoid AF neuron circuit. It was designed in TSMC 0.18 μm CMOS technology and costs 375 $\mu m \times 238 \mu m$ area.

The post-simulation (Fig.7) of the Sigmoid AF fitting circuit shows that the maximum error between the output of proposed circuit and the ideal Sigmoid function is 1.76%. The form of Current Input-Current Output is proximity to biological neuron and the signal of current is transmitted in the neuron circuit, so there is no need of extra I-V or V-I conversion unit and reduce circuit complexity. The comparison of this work with references is shows in Table I.

$$Error = \frac{|I_{out}-Sigmoid_{ideal}|}{Amplitude} \quad (17)$$

It is always preferred to check the proposed circuit for error that can be caused by noise. The proposed Sigmoid AF neuron circuit was simulated for noise. The simulation (Fig.8) shows that the noise effect is 0.43 pA/ \sqrt{Hz} to 80 pA/ \sqrt{Hz} in the region of frequency from 1 Hz to 100 MHz. The maximum error caused by noise in the output of the circuit is 80 pA/ \sqrt{Hz} , which can be considered as negligible impact.

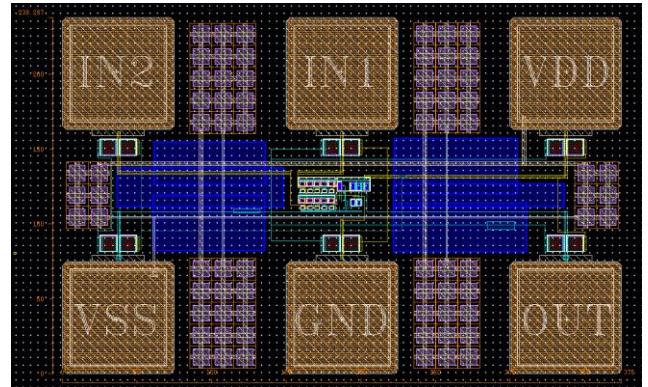


Figure 6. Layout of high-precision Sigmoid AF neuron circuit.

TABLE I. COMPARISON OF THIS WORK WITH REFERENCES

Ref	Tech [nm]	Supply Voltage [V]	Power Consumption [uW]	CMOS Number of function circuit	Error [%]	Form of Input-Output
[11]	350	3.3	0.23	15	6.5	V-I
[12]	90	1.2	21.6	6	7.67	I-V
[13]	350	3.3	N/A	12	5	V-I
[14]	90	1.2	8.4	6	3	V-V
This work	180	1.8	8.02	9	1.76	I-I

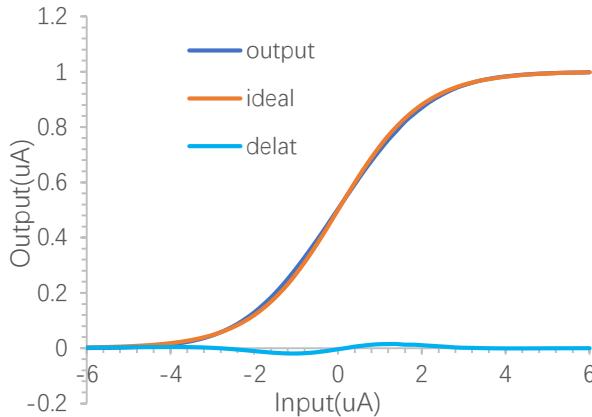


Figure 7. The post-simulation of sigmoid AF fitting circuit.

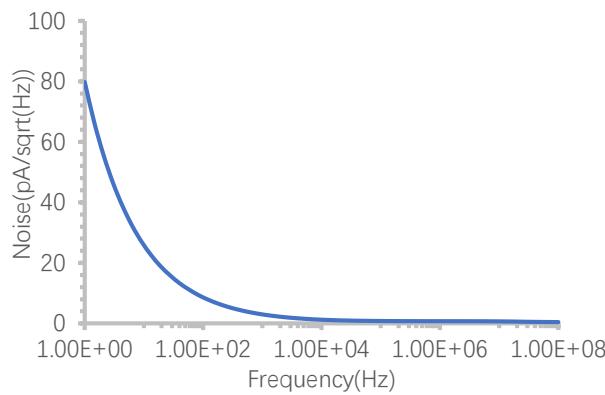


Figure 8. Effect of noise on circuit.

V. CONCLUSIONS

Sigmoid function is widely used in ANNs due to its fast convergence and proximity to biological neuron. In this paper, a high-precision Sigmoid AF neuron circuit is presented, the proposed circuit fitting the Sigmoid function is based on the transfer characteristics of the CMOS differential pairs. The circuit was simulated in TSMC 0.18 μ m CMOS technology. The post-simulation shows that the error between the output of Sigmoid AF fitting circuit and the ideal Sigmoid function is 1.76%. The total area of the layout is 375 μ m *238 μ m. The noise effect of the designed circuit was tested in the region of frequency from 1 Hz to 100 MHz. It can be concluded that the proposed neuron circuit is able to withstand the influence of noise. The future work is to ensure that the designed circuit can be used for large-scale systems.

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