

ECE6217

Lab 2: Current Mirror Circuit

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Examine Fig. 20.2. In this figure we show a current mirror and the equivalent circuit representation of a current source. Looking at M1, we can write

$$I_{REF} = I_{D1} = \frac{KP_n W_1}{2 L_1} (V_{GS1} - V_{THN})^2 (1 + \lambda(V_{DS1} - V_{DS1,sat})) \tag{20.1}$$

knowing $V_{DS1} = V_{GS1}$ and $V_{DS1,sat} = V_{GS1} - V_{THN}$. For M2, we write

$$I_O = I_{D2} = \frac{KP_n W_2}{2 L_2} (V_{GS1} - V_{THN})^2 (1 + \lambda(V_O - V_{DS1,sat})) \tag{20.2}$$

noting $V_{GS1} = V_{GS2}$, $V_{DS1,sat} = V_{DS2,sat}$, and V_O is the voltage across the current source. Looking at the ratio of the drain currents, we get

$$\frac{I_O}{I_{REF}} = \frac{W_2/L_2}{W_1/L_1} \cdot \frac{1 + \lambda(V_O - V_{DS1,sat})}{1 + \lambda(V_{DS1} - V_{DS1,sat})} \tag{20.3}$$

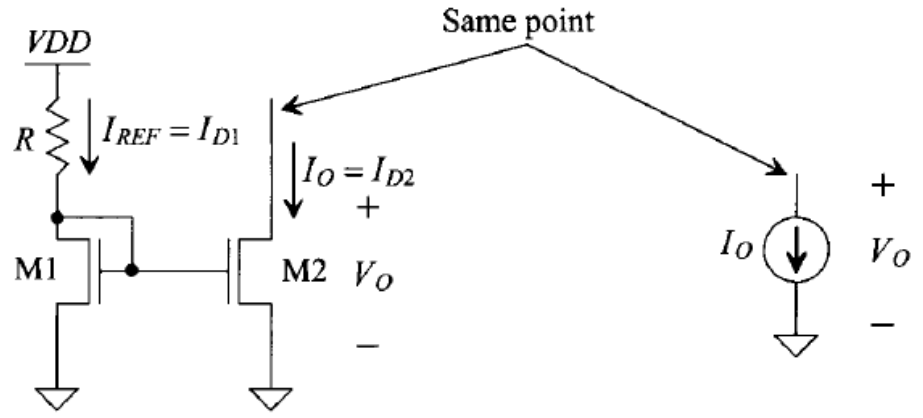


Figure 20.2 The current mirror and how we think about it.

Generally, the lengths of the devices in the current mirror are equal (let's assume they are for the moment). If, also at this time, we don't concern ourselves with channel-length modulation ($\lambda = 0$), we get a very useful result, that is,

$$\frac{I_O}{I_{REF}} = \frac{W_2}{W_1} \tag{20.4}$$

Process and Design Parameters

$K = \mu_e C'_{ox}$
 $\beta = K \frac{W}{L}$

$$I_D = \mu_e C'_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH})^2 - \frac{1}{2} (V_{GS} - V_{TH})^2 \right] = \frac{1}{2} \mu_e C'_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$I_D = \begin{cases} K \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & \text{triode} \\ \frac{K}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\beta}{2} (V_{GS} - V_{TH})^2 & \text{saturation} \end{cases}$$

CHANNEL LENGTH MODULATION IN SATURATION

- Modified Saturation-region drain current in presence of CLM

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_{TH})^2$$

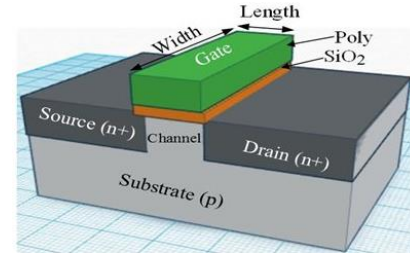
- Assuming incremental change ΔL is much less than L

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\Delta L}{L} \right)$$

$\frac{\Delta L}{L} \alpha V_{DS} = \lambda V_{DS}$ λ is a process technology parameter it accounts for how a certain semiconductor process technology responds to changes in the drain to source voltage

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{V_{DS}}{V_A} \right) \quad V_A = \frac{1}{\lambda}$$

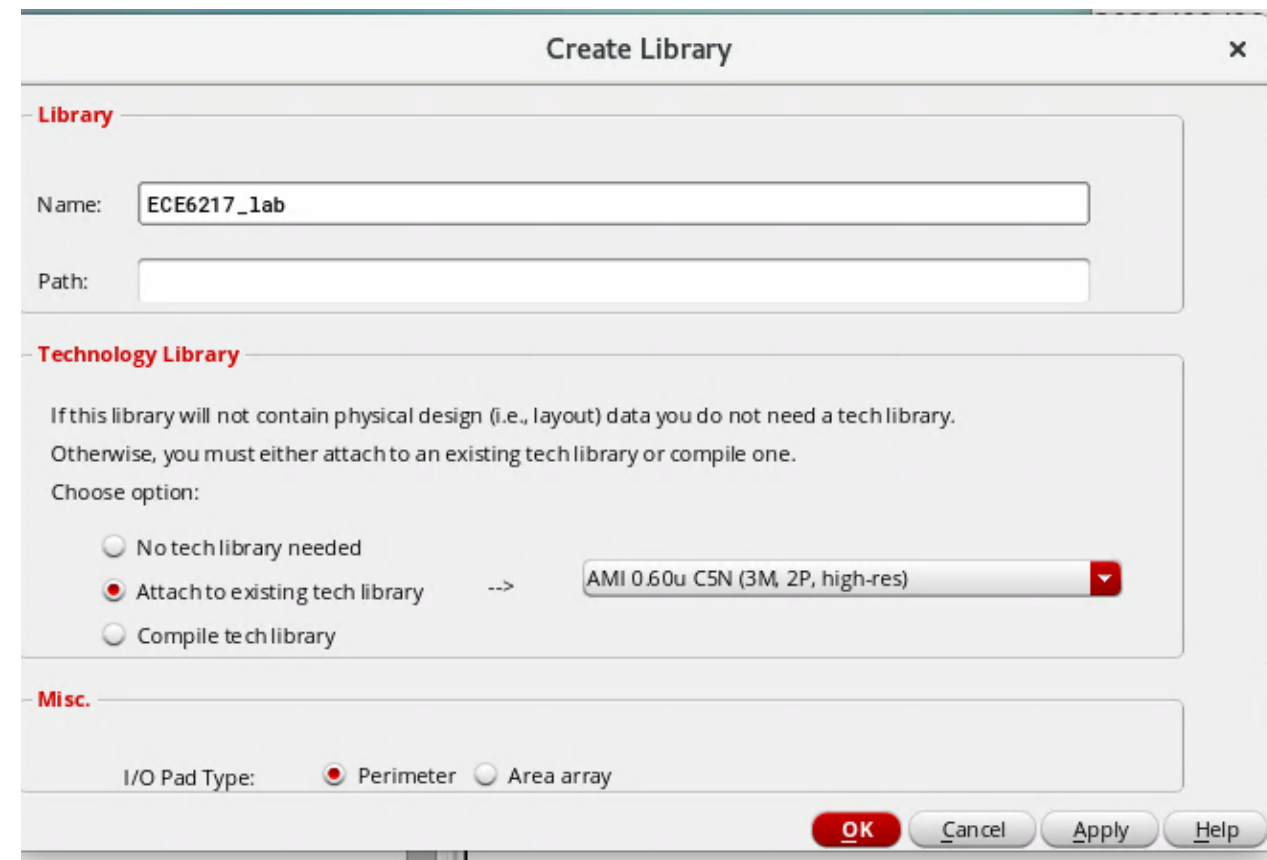


Create a new Library for ECE6217

- Go to Library manager window
- From the menu, select File ->New ->Library
- You will see a dialog like this
- NAME: ECE6217_lab
- *Attach to existing tech library* section, select: **AMI 0.60u C5N (3M, 2P, high-res)**

Press OK

Ensure no errors



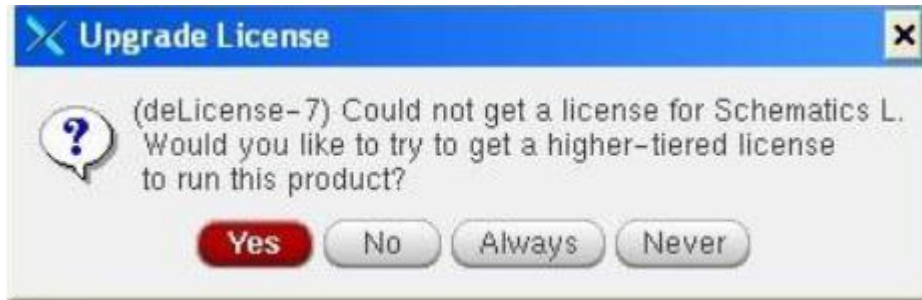
The screenshot shows the 'Create Library' dialog box with the following fields and options:

- Library** section:
 - Name: ECE6217_lab
 - Path: (empty field)
- Technology Library** section:
 - Text: "If this library will not contain physical design (i.e., layout) data you do not need a tech library. Otherwise, you must either attach to an existing tech library or compile one."
 - Text: "Choose option:"
 - Options:
 - ☐ No tech library needed
 - ☒ Attach to existing tech library --> AMI 0.60u C5N (3M, 2P, high-res) [dropdown arrow]
 - ☐ Compile tech library
- Misc.** section:
 - I/O Pad Type: ☒ Perimeter ☐ Area array

Buttons at the bottom: OK, Cancel, Apply, Help.

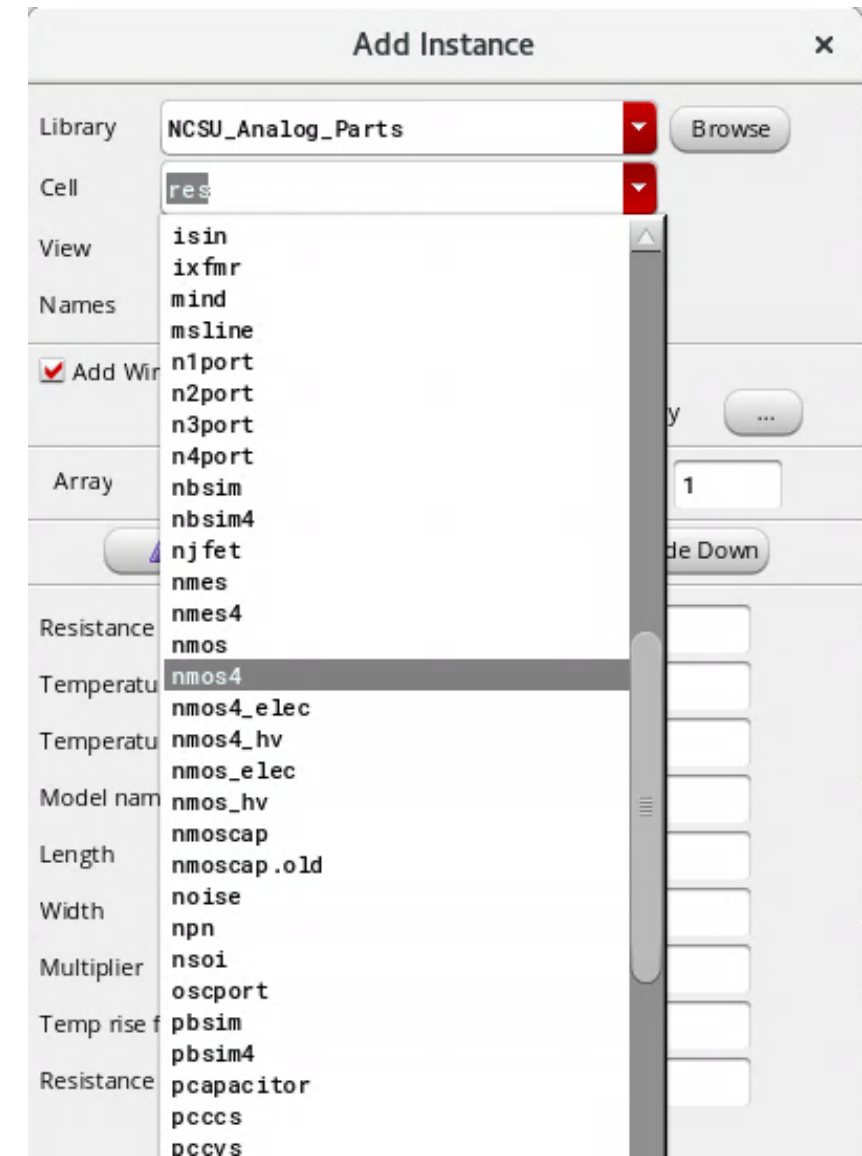
Create a New design

- From the Library Manager, click on the “ECE6217_lab” library you just created.
- From the menu, choose File->New->Cellview, and fill in the form as shown below.
- In the cell Field, type “Current_mirror”
- Click always when you see “Upgrade License”



Instantiating parts to create the Current Mirror circuit

- From the Menu choose: Create -> Instance
- Choose “nmos4”
- The default size for this “nmos” is
- $W/L = 1.5\mu\text{m}/0.6\mu\text{m}$
- Then create another nmos with the same parameters

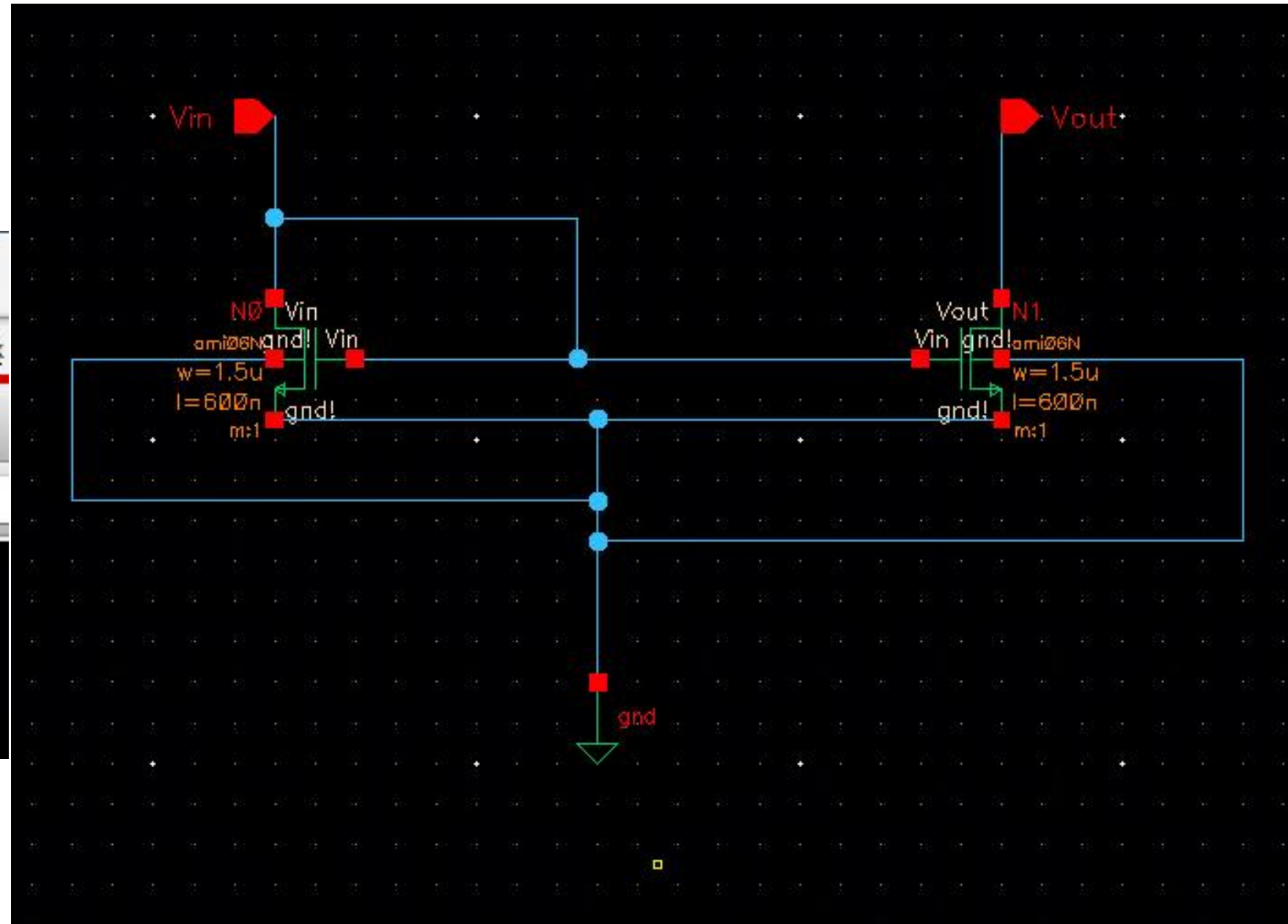
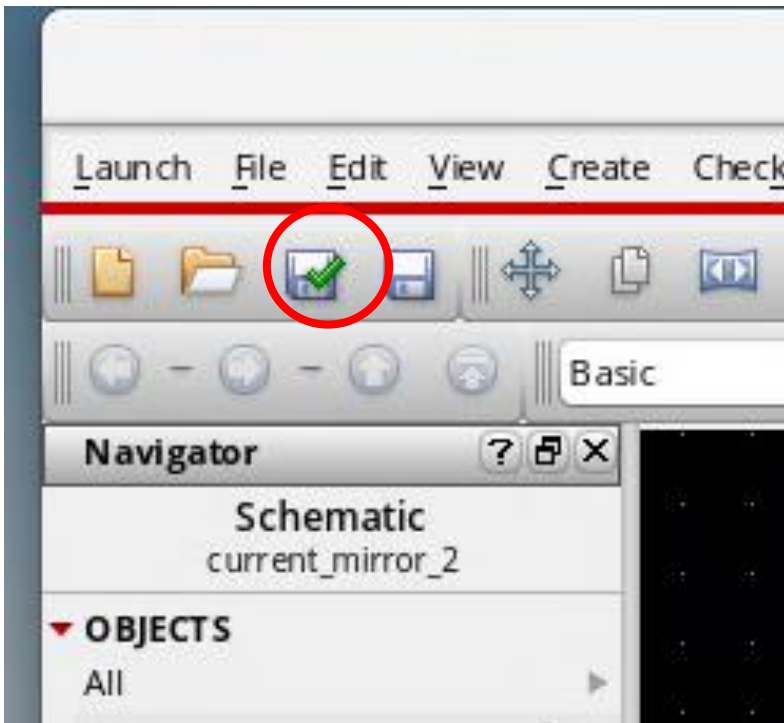


Build mirror current circuit

- From the instance menu, choose “gnd” and place it under the the transistors.
- Adding I/O Pins, press P to add “Vin” and “Vout” as input signal and output signal.
- Then connect the Pins and electronic components with wires.

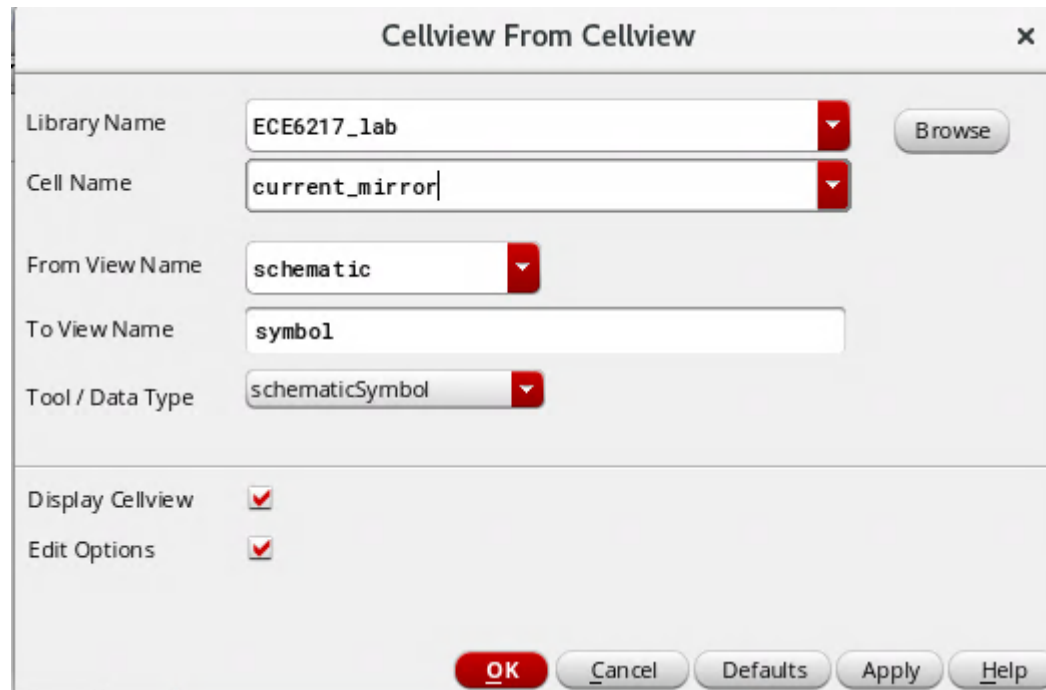
Build mirror current circuit

Click check and save after you build this circuit to see if there are any errors.



Make a symbol

Create -> Cellview -> From Cellview



The image shows a software dialog box titled "Cellview From Cellview" with a close button (X) in the top right corner. The dialog contains several input fields and checkboxes. The "Library Name" field is set to "ECE6217_lab" and has a "Browse" button to its right. The "Cell Name" field is set to "current_mirror". The "From View Name" field is a dropdown menu set to "schematic". The "To View Name" field is a text box set to "symbol". The "Tool / Data Type" field is a dropdown menu set to "schematicSymbol". At the bottom, there are two checked checkboxes: "Display Cellview" and "Edit Options". The bottom of the dialog features a row of buttons: "OK" (highlighted in red), "Cancel", "Defaults", "Apply", and "Help".

Library Name	ECE6217_lab	Browse
Cell Name	current_mirror	
From View Name	schematic	
To View Name	symbol	
Tool / Data Type	schematicSymbol	
Display Cellview	<input checked="" type="checkbox"/>	
Edit Options	<input checked="" type="checkbox"/>	

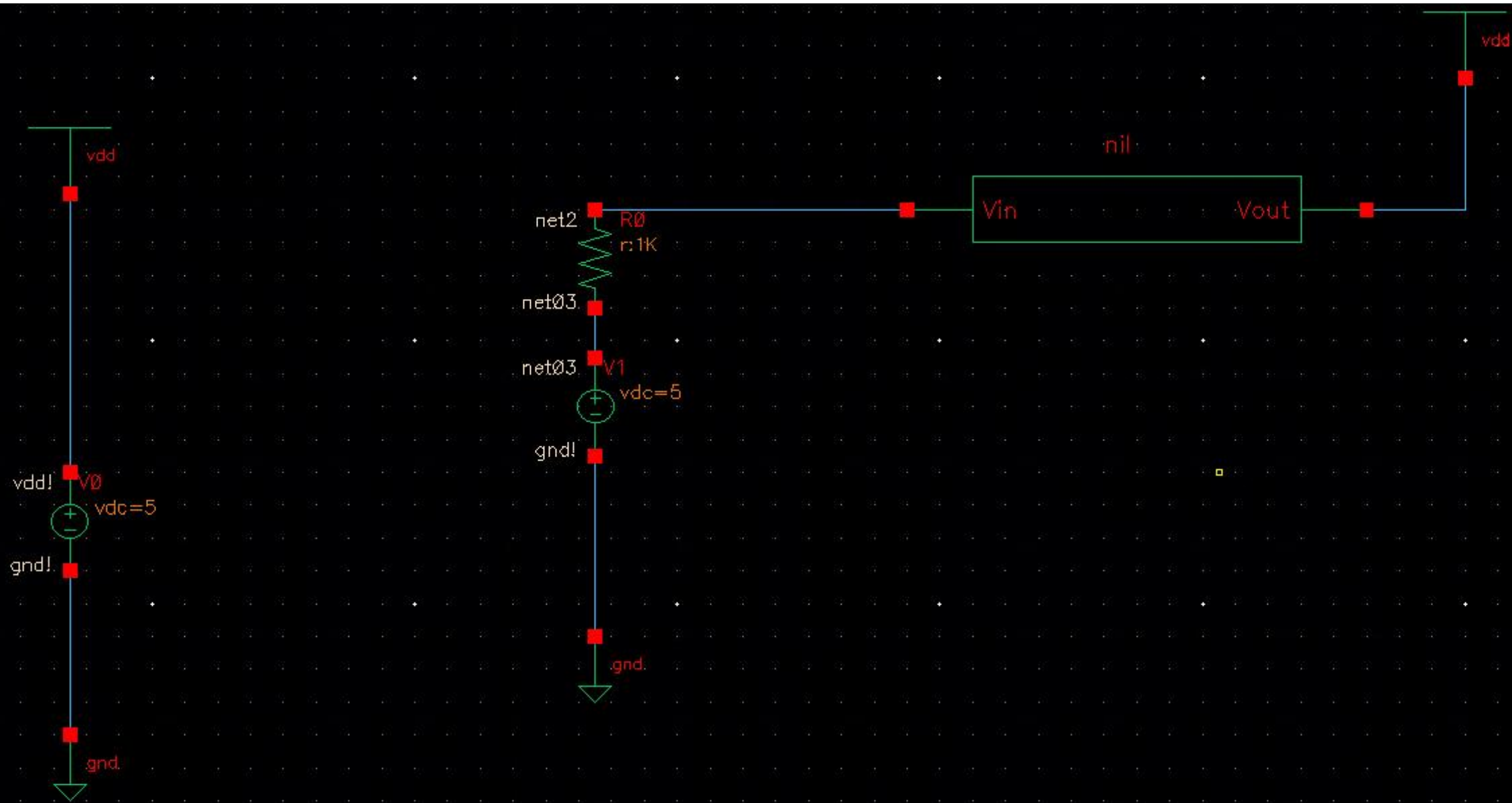
OK Cancel Defaults Apply Help

Create a Testbench

In the Library Manager, click on your “**ECE6217_lab**” Library.

- From the Library Manager Menu choose: **File-> New-> Cellview...**
- Fill it as shown below, to create a new cell called: **current_mirror_tb**
- Click Ok. A new Composer-Schematic window appears.
- Create -> Instance:
- Vdd X2
- vdc: 5V DC voltage X2
- res: 1 K ohm
- gnd
- Create -> ECE6217_lab -> current mirror
- Connect the power source component with the current mirror circuit
- Save and check if there are any errors

Testbench



Simulation

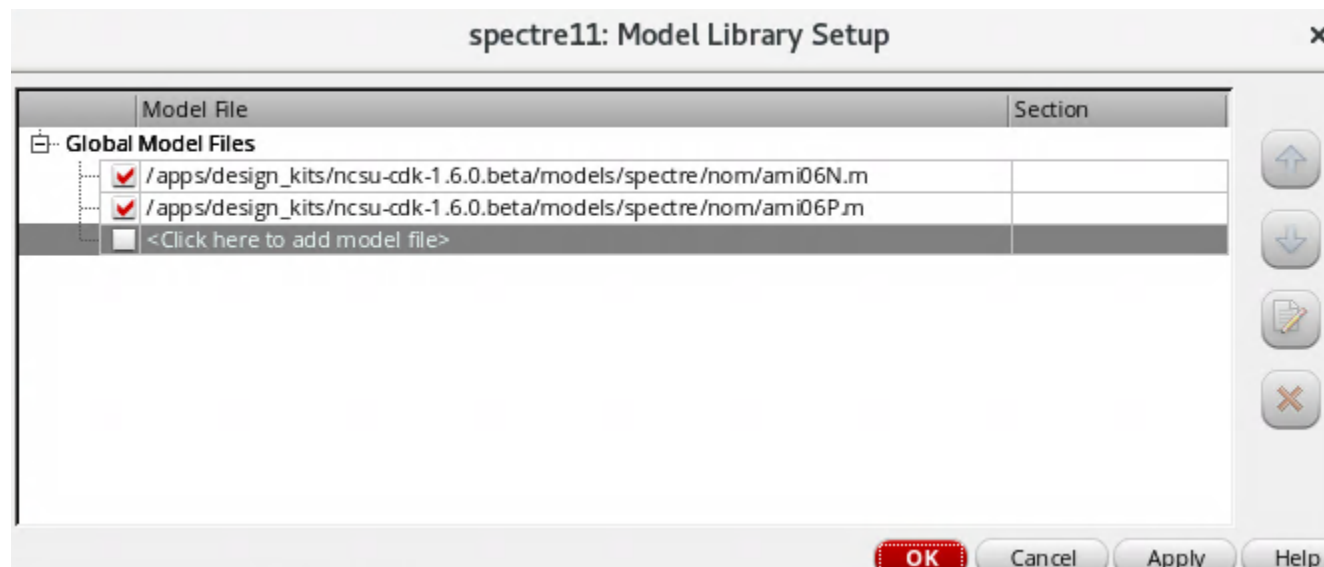
- Launch -> ADE L

In the Simulation window, select **Setup -> Simulator/Directory/Host**

Ensure the Simulator cyclic field is reading **Spectre**. Leave other fields to default.

In the simulation window, select **Setup -> Model Libraries...**

Ensure that the files shown below are in the list, if not, browse for the following files using the <...> icon



Choosing Analyses

- From the menu choose Analysis -> Choose...
- The form appears.
- Select the “**trans**” analysis or “**dc**”
- Set stop time = 150u as shown in the figure

Choosing Analyses -- ADE L (12) x

Analysis	<input checked="" type="radio"/> tran	<input type="radio"/> dc	<input type="radio"/> ac	<input type="radio"/> noise
	<input type="radio"/> xf	<input type="radio"/> sens	<input type="radio"/> dcmatch	<input type="radio"/> acmatch
	<input type="radio"/> stb	<input type="radio"/> pz	<input type="radio"/> lf	<input type="radio"/> sp
	<input type="radio"/> envlp	<input type="radio"/> pss	<input type="radio"/> pac	<input type="radio"/> pstb
	<input type="radio"/> pnoise	<input type="radio"/> pxf	<input type="radio"/> psp	<input type="radio"/> qpss
	<input type="radio"/> qpac	<input type="radio"/> qpnoise	<input type="radio"/> qpxf	<input type="radio"/> qpsp
	<input type="radio"/> hb	<input type="radio"/> hbac	<input type="radio"/> hbstb	<input type="radio"/> hbnoise
	<input type="radio"/> hbsp	<input type="radio"/> hbxf		

Transient Analysis

Stop Time

Accuracy Defaults (errpreset)

☐ conservative ☐ moderate ☐ liberal

☐ Transient Noise

Dynamic Parameter ☐

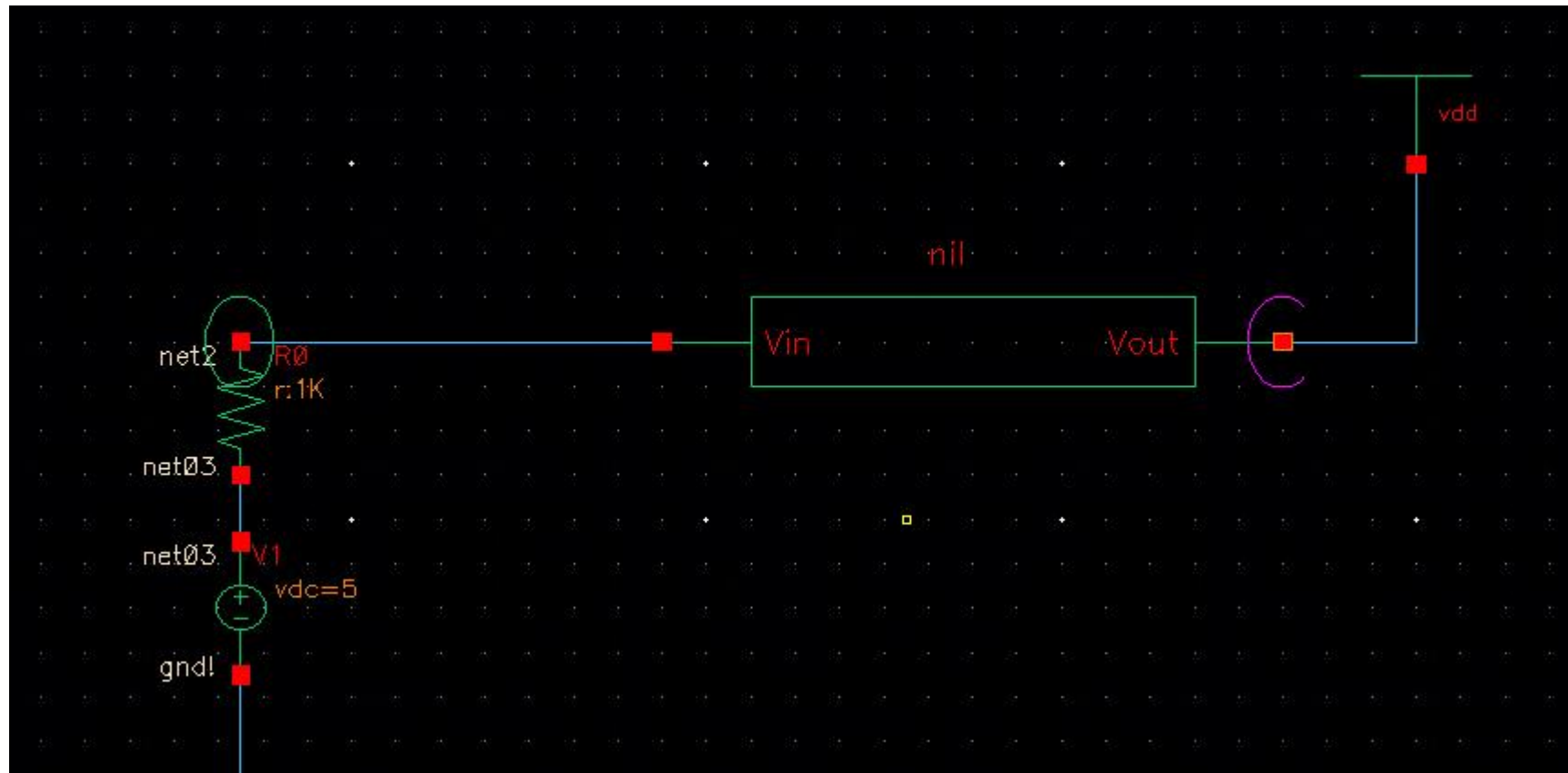
Enabled ☒

Options...

OK Cancel Defaults Apply Help

Choose the simulation node

- Outputs -> to be plotted -> from schematic
- Click on the nodes as shown below.(do not choose wire)



Run simulation



Assignment

- Finish the Layout of current mirror circuit
- Change the width (w) of the nmos close to the output Pin from 1.5 μm to 3 μm and see what will happen.