Mini Project Three

ELEC 301

University of British Columbia

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Content

1. Introduction

This project involves understanding and testing various amplifier circuits, including cascode, common-base/common-collector, operational amplifiers, and AM modulators. This project consists in designing, simulating, and analyzing the performance of these circuits.

2. The Cascode Amplifier.

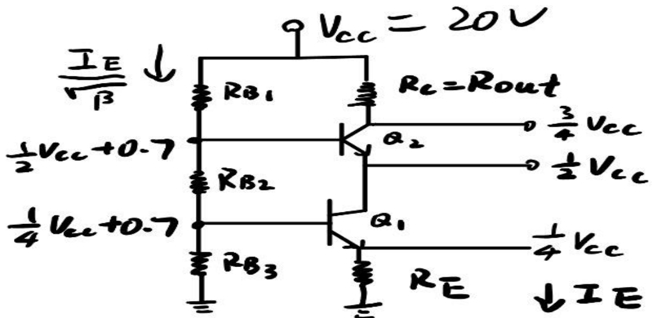


Figure 1 Cascode bias circuit

From the specification, $R_{out}(value\ at\ midband)\ is\ 2.5k\Omega \pm 250\Omega$ and use the closest commonly available resistance values which is $2.4k\Omega$. $R_{out} = \boldsymbol{R_C = 2.4k\Omega}$ because current source can be set to zero.

Apply the $\frac{1}{4}$ rule to bias the circuit as shown above. From mini project two, $\boldsymbol{\beta_{2N3904} = 117}$. $V_{cc} = 20V, V_{BE} = 0.7V$. $V_{C2} = \frac{3}{4}V_{CC} = 15V, V_{C1} = \frac{1}{2}V_{CC} = 10V, V_{E1} = \frac{1}{4}V_{CC} = 5V$.

$V_{B2} = 10.7V, V_{B1} = 5.7V\ R_L = 50k\Omega$.

$I_{C2} = \frac{V_{CC}-V_{C2}}{R_C} = 2.08333mA \approx I_{C1} = I_{E2} \approx I_{E1}$.$\boldsymbol{R_E} = \frac{\boldsymbol{V_{E1}}}{\boldsymbol{I_{E1}}} = \boldsymbol{2.4k\Omega}$.$I_{B1} = \frac{I_{C1}}{\beta} = 17.8\mu A \approx I_{B1}$. $I_1 = \frac{I_{E1}}{\sqrt{\beta}} = 0.1926mA, R_{B1} = \frac{V_{CC}-V_{B2}}{I_1} = 48.285k\Omega$.

$I_2 = I_1 - I_{E2} = 0.174798mA,$ $I_3 = I_1 - I_{E2} - I_{E1} = 0.15699mA$.

$\boldsymbol{R_{B3} = \frac{V_{B1}}{I_3} = 36.307k\Omega, R_{B2} = \frac{V_{B2}-V_{B1}}{I_2} = 28.604k\Omega, R_{B1} = \frac{V_{CC}-V_{B2}}{I_1} = 48.285k\Omega}$.

Use the closest commonly available resistance values:

$\boxed{\boldsymbol{R_{B3} = 36k\Omega, R_{B2} = 30k\Omega, R_{B1} = 47k\Omega, R_C = R_E = 2.4k\Omega}}$.

Since two transistors are identical, $\boxed{\boldsymbol{g_m = \frac{I_C}{V_T} = 0.0833℧, r_\pi = \frac{\beta}{g_m} = 1404\Omega}}$.

Since R_{in} need to be larger than 3500Ω at mid band, $R_{in} = R_{B2}||R_{B2}||r_\pi = \mathbf{1293}\Omega$ before adding extra resistor, need to add an additional resistor $\boxed{R_{ad} = 2.4k\Omega}$ in series with R_s to meet this requirement.

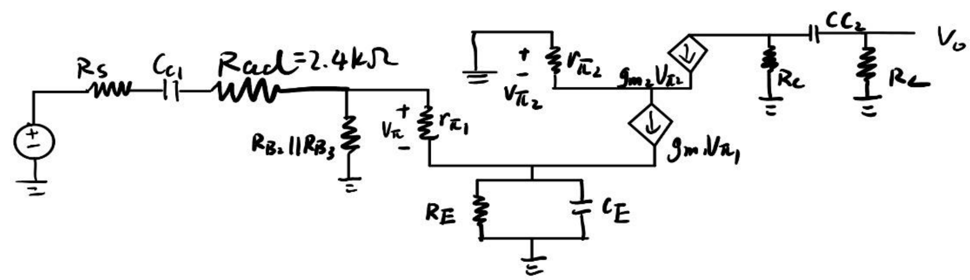


Figure 2 Low-frequency small signal model

C_B is comparatively large so can be considered as a short circuit. C_{C2} is decoupled, $\boldsymbol{\omega_{C_{C2}} = \frac{1}{(R_C+R_L)*C_{C2}} = \frac{1}{52400C_{C2}}}$.

Mentioned in class, C_{C1} is for open circuit test and C_{CE} is for short circuit test to be cost-effective. $\boldsymbol{\omega_{C_{C1}}^{OC} = \frac{1}{(R_s+R_{ad}+R_{B2}||R_{B3}||(r_\pi+R_E*(1+\beta)))*C_{C1}} = \frac{1}{17923.944*C_{C1}}}$.

$$\boldsymbol{\omega_{C_E}^{SC} = \frac{1}{\left(R_E||\left(\frac{r_\pi+R_{B2}||R_{B3}||(R_S+R_{ad})}{1+\beta}\right)*C_E\right.} = \frac{1}{29.28788*C_E}}.$$

$$\boxed{\omega_{LZ1} = \omega_{LZ2} = 0, \boldsymbol{\omega_{LZ3} = \omega_{LZ(C_E)} = \frac{1}{C_E*R_E} = \frac{1}{2400*C_E}}}.$$

Since $\omega_{C_E}^{SC}$ is the dominant pole for calculating L3dB frequency,

$$\omega_{L3dB} = \sqrt{{\omega_{C_E}^{SC}}^2 - 2*\omega_{LZ(C_E)}^2} = 1200. \text{ Solve to get } \boldsymbol{C_E = 28.4489\mu F}.$$

To be more cost effective, make all capacitors to be the same.

The final design is $\boxed{\boldsymbol{C_E = 33\mu F}}$. $\boxed{\boldsymbol{C_{C1} = C_E = 33\mu F}}$, $\boxed{\boldsymbol{C_{C2} = 33\mu F = C_E}}$.

R_{B3}	R_{B2}	R_{B1}	$R_C = R_E$	$C_{C1} = C_{C2} = C_E$	R_{ad}
$36k\Omega$	$30k\Omega$	$47k\Omega$	$2.4k\Omega$	$33\mu F$	$2.4k\Omega$

Table 1 Resistors and capacitors

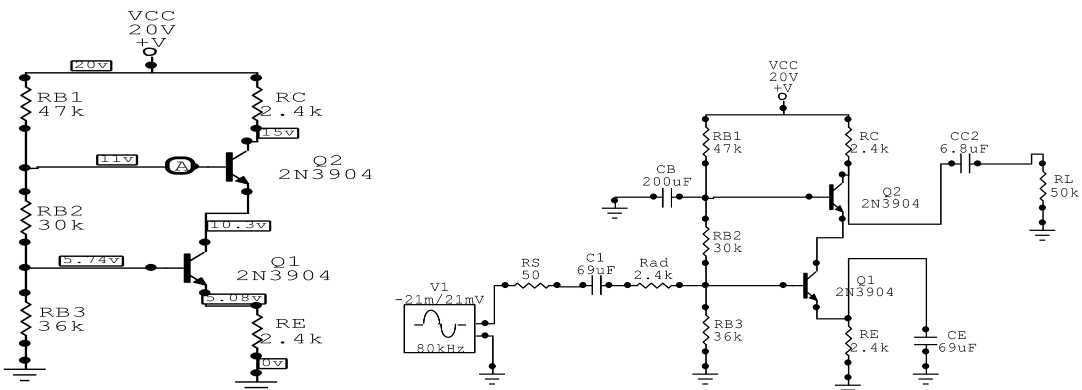


Figure 3 Bias circuit and full circuit

A

Draw the circuit diagram of the bias circuit and amplifier circuit on CircuitMaker. Measure the DC operating point:

	V_C	V_B	V_E	I_C	I_B	I_E
Q_2	15V	11V	10.3V	2.085mA	15.87μA	2.101mA
Q_1	10.3V	5.74V	5.08V	2.101mA	15.89 μA	2.116mA

Table 2 DC operating point

B

For calculated low-frequency poles and zeros as shown above:

$$\omega_{C_{C2}} = \frac{1}{(R_C+R_L)*C_{C2}} = 0.5783\,\frac{1}{sec},$$

$$\omega_{C_{C1}} = \frac{1}{(R_S+R_{ad}+R_{B2}||R_{B3}||(r_\pi+R_E*(1+\beta)))*C_{C1}} = 1.6906\,\frac{1}{sec},$$

$$\omega_{CE} = \frac{1}{\left(R_E||\left(\frac{r_\pi+R_{B2}||R_{B3}||(R_S+R_{ad})}{1+\beta}\right)*C_E\right.} = 1024.17\,\frac{1}{sec}, \quad \omega_{LZ(C_E)} = \frac{1}{C_E*R_E} = 12.6263\,\frac{1}{sec}.$$

$$\boxed{\omega_{L3dB} = \sqrt{{\omega_{C_{C2}}}^2 + {\omega_{C_{C1}}}^2 + {\omega_{CE}}^2 - 2*{\omega_{LZ(C_E)}}^2} = \mathbf{1024.02}\,\frac{\mathbf{1}}{\mathbf{sec}}}.$$

For High-frequency poles, use the high-frequency small-signal model and its Miller equivalence. As shown in class, it is easy to get $V_{\pi 1} = V_{\pi 2}$, and Miller gain **k=-1**. Use the same approach as previous Mini project two to get $\boldsymbol{C_{\mu 1} \approx C_{\mu 2} = 1.8pF, C_{\pi 1} \approx C_{\pi 2} = 42.3pF}$

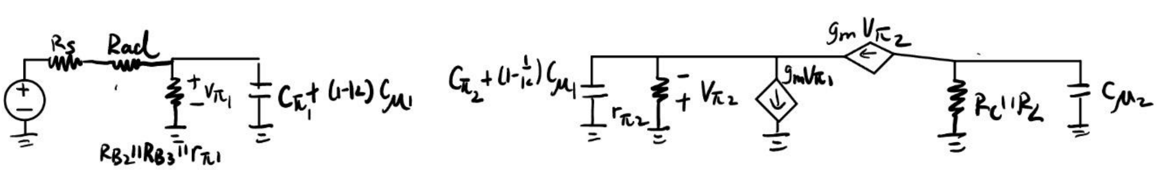


Figure 4 High-frequency small signal circuit

Calculate the time constant from left to right of the graph above. The first current source will be an open circuit.

$$\tau_{Hp1} = (C_{\pi1} + 2C_{\mu1}) * ((R_S + R_{ad})||R_{B2}||R_{B3}||r_{\pi1}) = 38.848ns,$$

$$\tau_{Hp2} = \frac{r_{\pi2}}{1+\beta_2} * (C_{\pi1} + 2C_{\mu1}) = 0.546ns,\ \tau_{Hp3} = C_{\mu2} * (R_C||R_L) = 4.122ns.$$

$$\boxed{\omega_{H3dB} = \frac{1}{\sqrt{\tau_{Hp1}{}^2+\tau_{Hp2}{}^2+\tau_{Hp3}{}^2}} = \mathbf{25.595 * 10^6}\,\frac{1}{s}}.$$

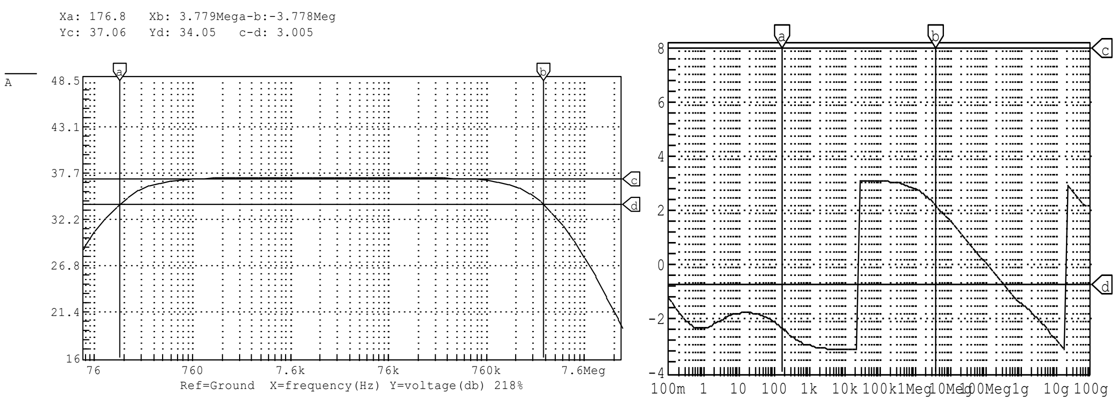


Figure 5 Magnitude and phase bode plots

Simulate the above circuit on CircuitMaker and plot the magnitude and phase bode plots. Make use of cursors to find out $\boxed{\omega_{L3dB} = 176.8Hz = 1110.867\frac{1}{s}}$.

$\boxed{\omega_{H3dB} = 3.779MHz = 23.744 * 10^6\frac{1}{s}}$.

	Calculated values	Simulated values	Error
$\omega_{L3dB}\ \frac{1}{s}$	1024.02	1110.867	7.8175%
$\omega_{H3dB}\ \frac{1}{s}$	$25.595 * 10^6$	$23.744 * 10^6$	7.78%

Table 3 Calculated and simulated frequency

Discussion: Compare the calculated and simulated values and find out the error is small. H3dB frequency is as accurate as L3dB frequency, and L3dB frequency meets the requirement of smaller than $1200\frac{1}{s}$.

C

Pick 25kHz as a mid-band frequency and adjust the input voltage from 1 mV until the output signal becomes not linear.

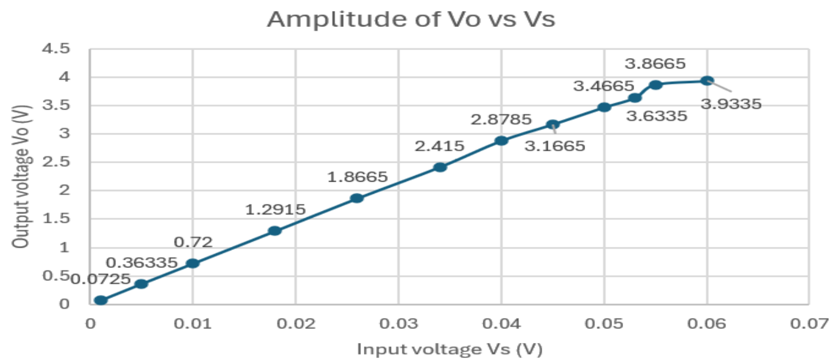


Figure 6 Vo vs Vs

When the amplitude of the input signal is about $\boxed{\mathbf{55mV}}$**,** the output signal becomes not linear. The slope of this linear line is $\boldsymbol{k = A_m = 68.5625\frac{V}{V} > 50(required)\frac{V}{V}}$.

D

The designed input resistance at midband $R_{in(calc)} = R_{ad} + R_{B2}||R_{B2}||r_\pi =$ $\boxed{\mathbf{3693\Omega}}$>3500 Ω. Remove the R_S, simulate the circuit on CircuitMaker and measure the input voltage and input current. $R_{in(simulation)} = \frac{V_{test}}{I_{test}} = \frac{39.91mV}{9.565\mu A} = \boxed{\mathbf{4.172k\Omega}} >$ 3500 Ω.The error is 11.49%, and both values meet the requirements.

3. Cascaded Amplifiers

A.

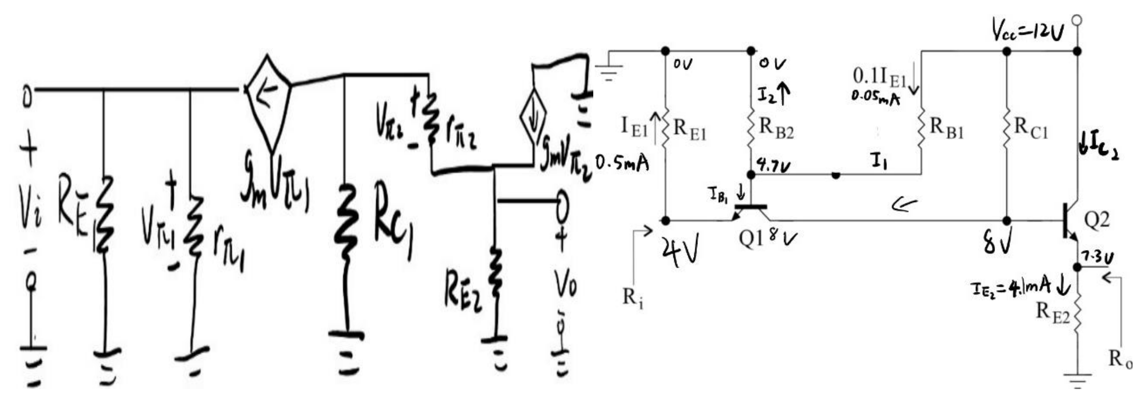


Figure 7 Mid-band circuit and bias circuit

As shown above is the small signal at midband. V_T (25mv) is much smaller than V_{E1}.

$R_i = R_{E1}||\frac{r_\pi}{1+\beta} = R_{E1}||\frac{\beta * V_T}{(1+\beta)*I_C} = \frac{V_{E1}}{I_{E1}}||\frac{V_T}{I_{E1}} \approx \frac{V_T}{I_{E1}} = 50\Omega$. Get $\boldsymbol{I_{E1}}$**=0.5mA**.

$I_{C1} \approx 0.5mA, I_{B1} = \frac{I_{C1}}{\beta} = 3\mu A, I_1 = 0.1I_{E1} = 0.05mA, I_2 = I_1 - I_{B1} = 47\mu A.$

$V_{E1} = 4V, V_{B1} = 4.7V, V_{C1} = 8V, V_{CC} = 12V, V_{E2} = 7.3V.$

Finally, get: $\boxed{R_{E1} = \frac{V_{E1}}{I_{E1}} = 8k\Omega, R_{B2} = \frac{V_{B1}}{I_2} = 100k\Omega, R_{B1} = \frac{V_{CC}-V_{B1}}{I_1} = 146k\Omega}$.

β is 166.7 from Mini project 2. Then solve resistors at Q2:

$$\begin{cases} R_{E2} = \frac{7.3V}{I_{E2}} (bias\ circuit) \\ R_{C1} = \frac{12V-8V}{I_{C1}+\frac{I_{E2}}{1+\beta}} (bias\ circuit) \\ R_o = 50\Omega = R_{E2}|| \frac{r_{\pi2}+R_1}{1+\beta} = R_{E2}||(\frac{V_T}{I_{E2}} + \frac{R_{c1}}{1+\beta})(small\ signal\ circuit) \end{cases}.$$

Solve to get $\boxed{I_{E2} = 4.1568\text{mA}}$, $\boxed{R_{E2} = 1.756k\Omega}$, $\boxed{R_{C1} = 7.622k\Omega}$.

$I_{C2} \approx 4.1568mA, g_{m1} = \frac{I_{C1}}{V_T} = 0.02℧, g_{m2} = 0.166℧, r_{\pi1} = 8.33k\Omega, r_{\pi1} = 1k\Omega$.

Then, determine the low frequency poles for C_{C1} and C_{C2}. $R_S = R_L = 50\Omega$, which is source resistor and load resistor. $R_i = R_o = 50\Omega$

$\omega_{C_{C1}} = \frac{1}{(R_S+R_i)C_{C1}} = \frac{1}{100*C_{C1}}, \omega_{C_{C2}} = \frac{1}{(R_L+R_o)C_{C2}} = \frac{1}{100*C_{C2}}$.

They are symmetric, and both contribute ω_{L3dB} while C_B will not be considered for calculating the low frequency cut-in. Set $C_{C1} = C_{C2}$. The zeros' frequencies for C_{C1} and C_{C2} are at zero. $\omega_{L3dB} = \sqrt{\omega_{C_{C1}}{}^2 + \omega_{C_{C2}}{}^2} = 1000Hz = 6283\frac{1}{s}$.

Solve to get, $\boxed{C_{C1} = C_{C2} = 2.25\mu F}$.

Do short circuit test for C_B which is the common-base capacitor.

$\omega_{C_B} = \frac{1}{(R_{B1}||R_{B2}||(r_\pi+R_{E1}(1+\beta)))*C_B} = \frac{1}{56850.178*C_B}$, ω_{C_B} has to be 1 decade smaller than $\omega_{C_{C1}}$ to not influence L3dB frequency much. $\frac{1}{49623.598*C_B} = 444.44\frac{1}{s}$.

Solve to get $\boxed{C_B = 39.5777nF}$.

B.

Using available resistors. Run the circuit simulation on CircuitMaker to test input and output resistance. Replace R_s and find out $R_{in} = \frac{V_{test}}{I_{test}} = 55.476\Omega$ does not meet the requirement. When decrease R_{E1} from $8.2k\Omega$ to$7.5\ k\Omega$, $R_{in} = \boxed{51.28}\Omega < 55\Omega$. $R_{out} = 43.77\Omega$, so increase $R_{C1}\ from\ 7.5k\Omega\ to\ 9.1k\Omega$. $R_{out} = \boxed{51.46}\Omega < 55\Omega$. Then both resistance values meet the requirement.

R_{E1}	R_{B2}	R_{B1}	R_{E2}	R_{C1}	C_B	C_{C1}, C_{C2}
$7.5k\Omega$	$100k\Omega$	$150k\Omega$	$1.8k\Omega$	$9.1k\Omega$	$39nF$	$2.2\mu F$

Table 4 Final resistors and capacitors

Remove R_s and R_L and plot the bode plot to measure $A_m = \frac{V_o}{V_s} = \boxed{\mathbf{164.7}}\frac{V}{V}$.

C

Run the circuit simulation on CircuitMaker, sweeping from 10mHz to 100GHz to draw the bode plots. Without changing the capacitors, the $\omega_{L3dB} = 1325Hz$,which does not meet the requirement. So increase $\boldsymbol{C_{C1}}, \boldsymbol{C_{C2}}$ capacitance to $\boxed{\mathbf{3.3uF}}$ to get $\boldsymbol{\omega_{L3dB(simulated)}} = 950.1Hz = \boxed{\mathbf{5969}}\frac{1}{s}$ which meet the requirements. Then, find the high frequency cut-off points $\boldsymbol{\omega_{H3dB(simultaed)}} = 1.053MHz = \boxed{\mathbf{6.616 * 10^6}}\frac{1}{s}$ on the magnitude bode plots.

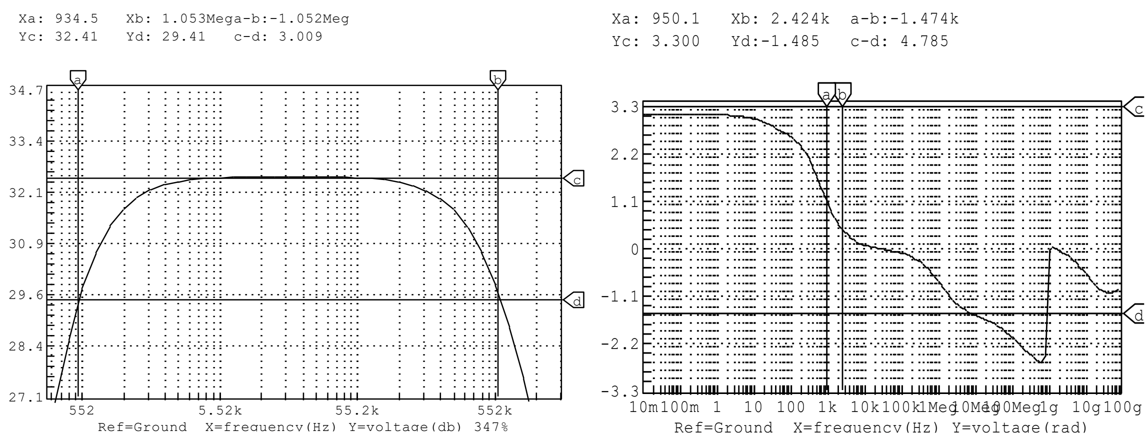


Figure 8 Magnitude and phase bode plots

4. The Operational Amplifier

A

i) Run the circuit simulation of the opamp on CircuitMaker, sweeping from 10mHz to 100GHz to plot the bode plot for magnitude response.

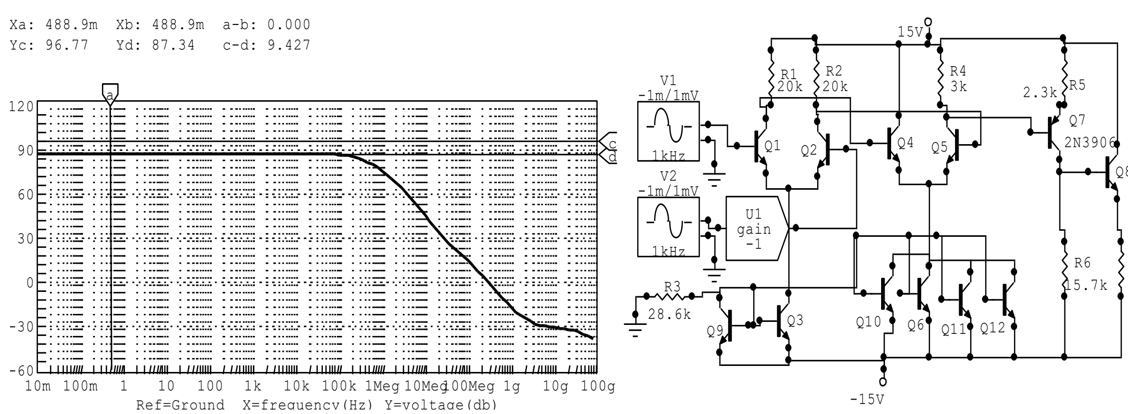


Figure 9 Magnitude bode plots and circuit diagram

ii) As shown in i), the gain of the circuit at 1kHz is $A_{m,diff} = 87.34dB = \boxed{\mathbf{23280}}\frac{V}{V}$.

B

i)(Check appendix 1 for detailed plots for i) and ii)). Simulate 1kHz and set one input voltage as a reference to measure another input voltage. Use transient analysis, plot and measure the peak-to-peak voltage $V_{test} = \mathbf{4mV}$**.**Then measure one of the input current peak-to-peak value $I_{test} = \mathbf{175.5nA}$. Differential input impedance is $\boxed{\boldsymbol{R_{in} = 22.792k\Omega}}$.

ii) Using a similar approach, using V_{test}, and I_{test} at the output to get single-ended output impedance and short the input, $R_{out} = \frac{V_{test}}{I_{test}} = \frac{1.414mV}{9.582\mu A} = \boxed{\mathbf{147.568\Omega}}$

C

i)Increase $20k\Omega$ by 0.1% to get 20.02kΩ, and decrease by 0.1% to get 19.98kΩ. Then, draw the common-mode circuit diagram on CircuitMaker to plot the bode plot. Sweep the frequency from 10mHz to 100GHz and apply small-signal to the input.

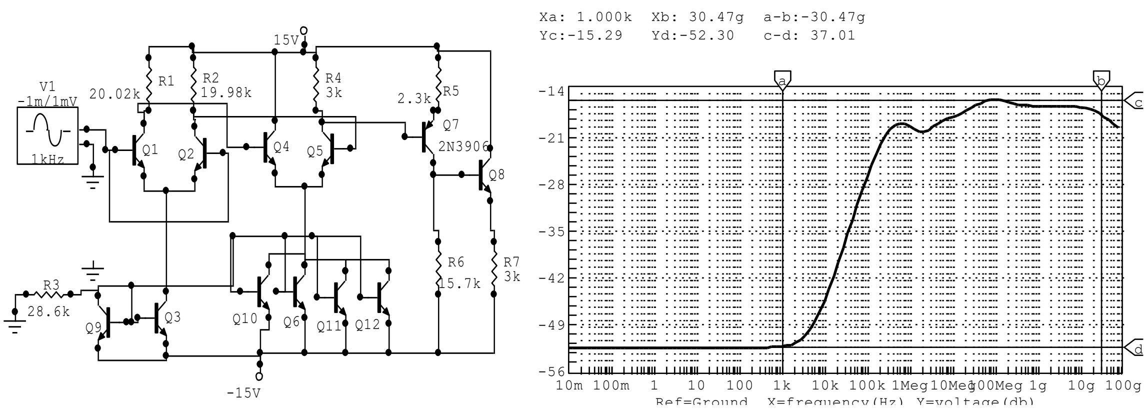


Figure 10 Common mode circuit and magnitude bode plot

ii) As shown on the bode plot, at 1kHz, $A_{CM} = -52.3dB = \boxed{\mathbf{2.4266 * 10^{-3}}}\frac{V}{V}$. At A),I have measured $A_{m,diff} = \boxed{\mathbf{23280}}\frac{V}{V}$, so CMRR=$20log\frac{|A_{m,diff}|}{|A_{CM}|} = \boxed{\mathbf{139.64}}dB$.

D

As mentioned by the professor, change resistors back to 20kΩ. Apply a small signal $\pm 1mV$ at 1kHz to the input and sweep from 10mHz to 100GHz.

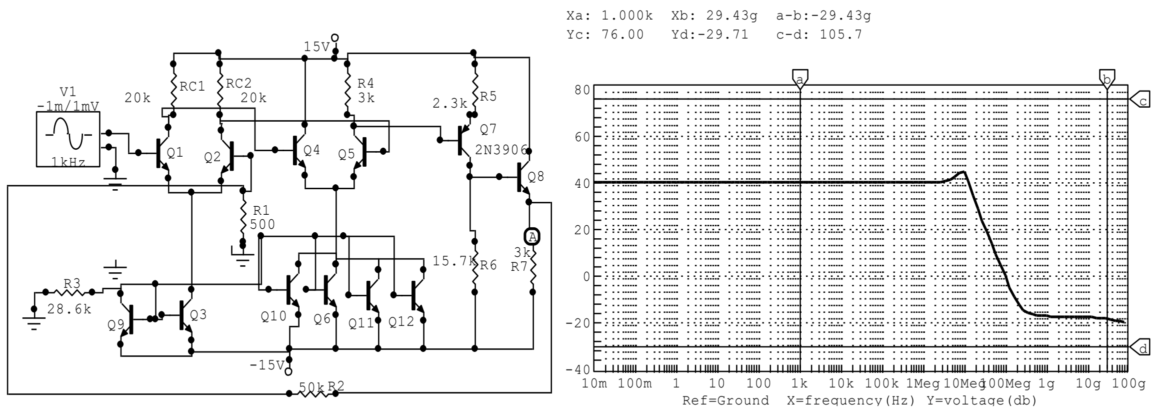


Figure 11Circuit diagram and magnitude bode plot

To measure the gain in the time domain, get $V_o = 70.7mV(RMS)$, and $V_S = 706.2\mu V$(RMS). The gain is $\boxed{\boldsymbol{A_{measured}} = \frac{\boldsymbol{V_o}}{\boldsymbol{V_S}} = \mathbf{100.14}\frac{\boldsymbol{V}}{\boldsymbol{V}}}$. Also, $A_{calculated} = 1 + \frac{R_2}{R_1} = \mathbf{101}\frac{V}{V}$, which agrees with the measured value.

E

At 1kHz, sweep the input source from 1mV until the output voltage becomes not linear.

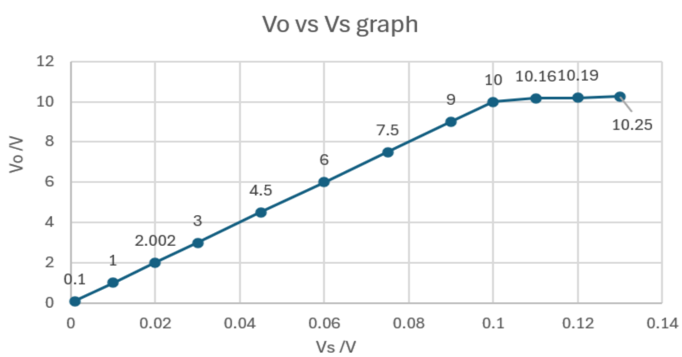


Figure 12 Non-inverting amplifier Vo vs Vs plot

Save the output data when increasing the input and plot the graph using Excel. The turning point is around $\boxed{\boldsymbol{V_S} = \mathbf{100}\boldsymbol{mV}}$ and V_o becomes not linear.

F

Use similar approach as B.

i) Use test voltage at the input side to measure the single-sided input impedance.

$$R_{in} = \frac{V_{in}(RMS)}{I_{in}(RMS)} = \frac{702.9\mu V}{281.8pA} = \boxed{\mathbf{2.494}}M\Omega.$$

ii)Then measure single-ended output impedance $R_{out} = \frac{V_{out}(RMS)}{I_{out}(RMS)} = \frac{702.9\mu V}{196.5uA} = \boxed{\mathbf{3.577}}\Omega$.

5. The AM Modulator.

A

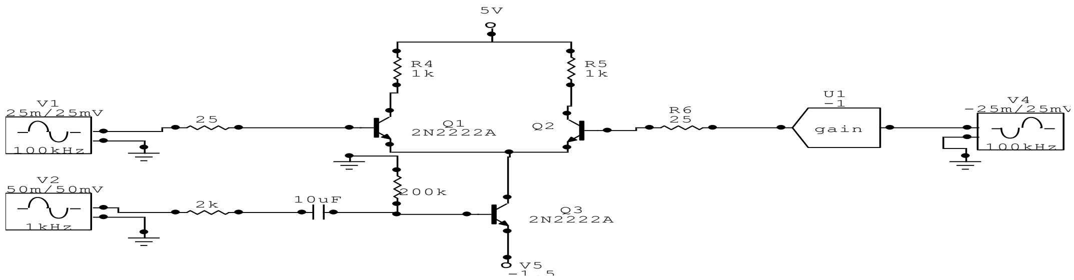


Figure 13 AM modulator

Apply a 50mVp, 1kHz sine wave to the input of the modulator and simulate 500ms to 502ms to observe the differential output. The high-frequency component visible in the waveform is consistent with the 100kHz carrier signal, while the envelope follows the lower 1kHz modulation signal. In this case, the troughs of the sine wave appear **flattened**, leading to a distortion.

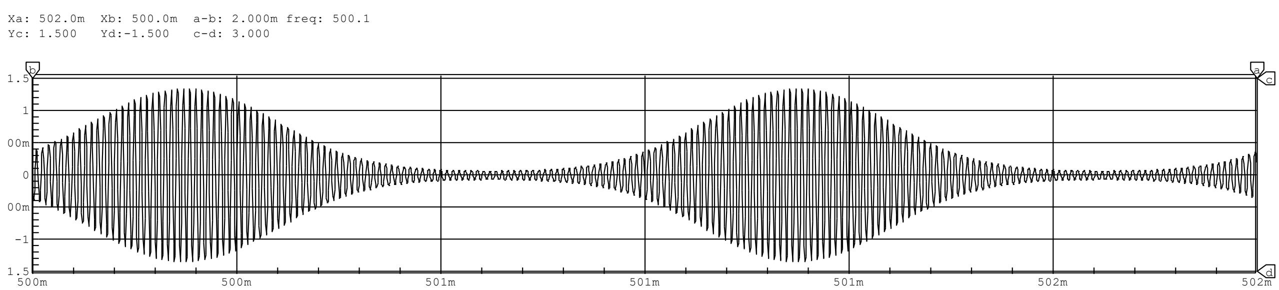
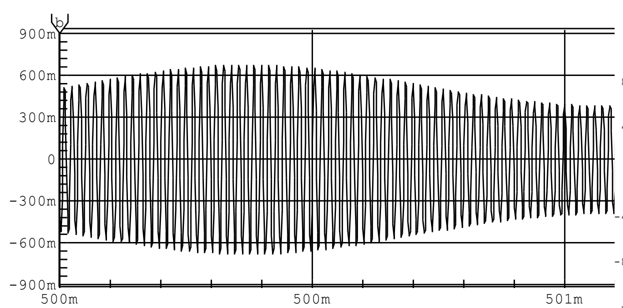
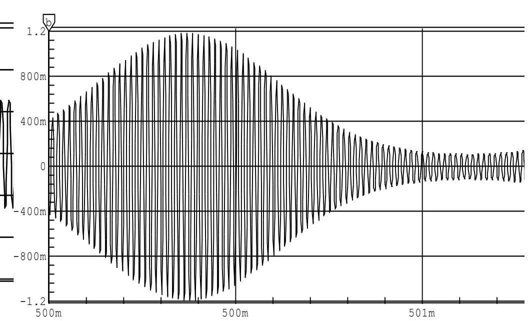


Figure 14 AM modulator output, 50mVp

B

For the least distortion, the modulation depth needs to be around 70% to 100%. Avoid clipping at the peaks and maintaining symmetry in the envelope.





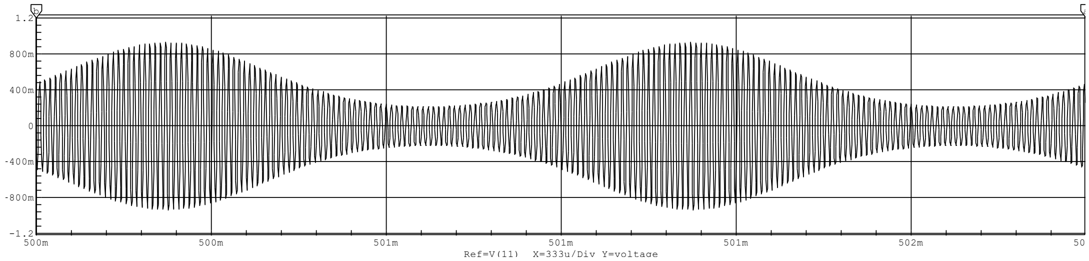


Figure 15 AM modulator output, 10mVp, 40mVp, 25mVp

The first graph is 10mVp input and the modulation depth is not enough. The second graph shows that when the input is 40mVp, the troughs of the sine wave appear flattened, which leads to distortion. The third graph shows when the input is 25mVp. The envelope of the AM signal is smooth and symmetrical(sin wave), with no signs of flattening and clipping. The depth is optimal. **25mVp** results in the least distorted envelope.

C

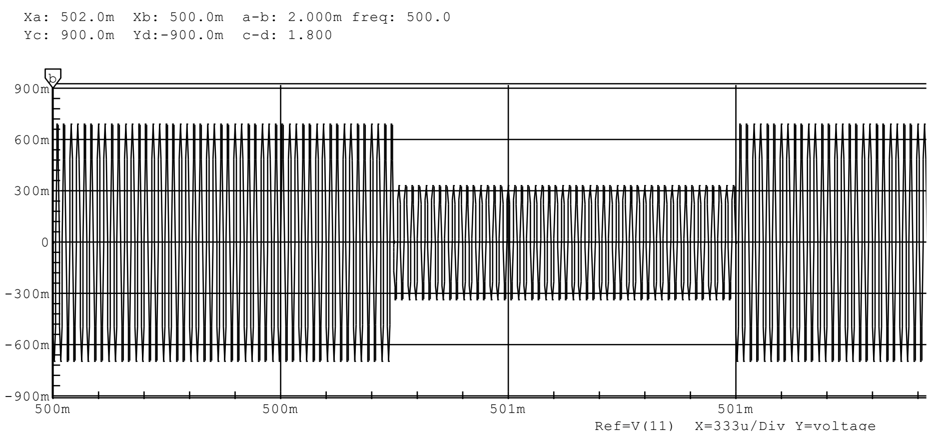


Figure 16 25mVp square wave input

Change the input signal to a square wave and vary amplitude from 10mVp to 100mVp. The output signal showed a stepped envelope. The depth is shallow for lower amplitude, and overmodulation is observed for higher amplitude. The least distorted envelope appeared at an intermediate amplitude(around **25mVp**), where the transitions are distinct and sharp without excessive distortion.

Discussion

An AM modulator varies the amplitude of a high-frequency carrier signal in proportion to a lower-frequency modulating signal, allowing information to be transmitted. The envelope's frequency and amplitude vary according to the modulating signal. $m = \frac{V_m(\,amplitude\ of\ input\ signal)}{V_C(amplitude\ of\ carrier\ signal)}$. When "m" is larger than 1, overmodulation occurs, leading to waveform distortion. When m=1, (in this case **25mVp**), the carrier amplitude varies fully with the modulating signal, achieving maximum efficiency without distortion. When m is too small the depth is not enough.

Conclusion

This project explored various amplifier types and an AM modulator, focusing on design, simulation, and performance analysis. Key findings include the cascode amplifier's high bandwidth and cascaded amplifiers' increased gain. The AM modulator demonstrated optimal modulation depth and highlighted distortion challenges with overmodulation.

References

ELEC 301 Course notes.

The Attached Standard/Commonly Available Values List.

A. Sedra and K. Smith, "Microelectronic Circuits," 5th, 6th, or 7th Ed., Oxford University Press, New York.

Appendix:

Appendix 1: