Implementation of the control signal logic

state	HALT	PC write	M src	M write	IR write	MDR write	LW	LI	RFwd		RF write	SorL	RD1 write	RD2 write	ALU1		ALU2		SUB	NOR	BN	BE	ALUout write	JAL
0	?	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1												1	1	1	0	0	1	0					1	
2															1	0	0	0					1	
3									1	1	1				0	0	0	0						
4															1	0	0	0	1				1	
5															1	0	0	0		1			1	
6															1	0	0	0	1	1			1	
7								1	0	0	1				0		0	0						
8									0	0	1						0							
9		1													0	1	0	0				1	1	
10		1													0	1	0	0			1		1	
11							1								1	0	1	0					1	
12			1			1											0							
13									1	0	1						0							
14															1	0	1	0					1	
15			1	1													0	0						
16		1							0	1	1				0	0	0	0						1