WILLIAM V.S. TUBMAN UNIVERSITY
College Of Engineering and Technology
Department: Computer Science Engineering

SYLLABUS
2nd Semester- AY 2024 - 2025

COURSE CODE	**: CSENG 406**	
COURSE TITLE	**: Digital Computer Circuits**	
PRE-REQUISITE	**: CSE 101, CSE 102**	**CO-REQUISITE: CSENG 306**
DURATION	**:** 1.5 hours a day, twice a week	

Instructor's Name: **Duah Jeremiah Leakpor**	email address: djleakpor@tubmanu.edu.lr
Mobile Number: **0770135920 / 0555353438**	Consultation Schedule: **10 Hours, Weekly**

Final Semester Project Specification

Project Title: Smart Traffic Intersection Controller with Emergency Override and Adaptive Timing

Duration: 3 Weeks

Project Type: Advanced Digital Systems Design

Objective

Design, implement, and test a smart traffic control system for a 4-way intersection that:

- Uses real-time inputs to dynamically adjust signal timing.
- Includes pedestrian crossing support.
- Prioritizes emergency vehicles.
- Simulates night mode (reduced functionality).
- Is modular and scalable.

System Requirements

Functional Requirements:

1. **Basic Traffic Signal Control**
   - ✓ 4-way traffic light system: North, South, East, West.
   - ✓ Standard Red-Yellow-Green light cycle.
2. **Vehicle Detection (Simulated)**
   - ✓ Use switches to simulate vehicle presence on each lane.

- ✓ Dynamically adjust green light duration based on density.

3. **Pedestrian Crossing**
   - ✓ Buttons to request crossing.
   - ✓ Countdown timer (7-segment) display during crossing phase.
4. **Emergency Vehicle Override**
   - ✓ Manual override input to simulate emergency vehicle presence.
   - ✓ Immediately switches to allow priority direction.
5. **Night Mode**
   - ✓ Blinking Yellow (main road) / Red (side roads) using a toggle switch.

Non-Functional Requirements:

- Modular circuit design (block-based approach).
- Fully documented FSMs, logic equations, truth tables.
- Simulated using Logisim or HDL tools (Verilog/VHDL).

Development Timeline

Week 1: Planning & Architecture

- Define inputs/outputs.
- Draft truth tables and initial FSMs.
- Choose simulation platform (Logisim / Verilog / VHDL).

Week 2: Base Traffic Logic + Timers

- Implement core FSM.
- Design and test timer subsystem.
- Begin 7-segment decoder for pedestrian timer.

Emergency Logic + Pedestrian Logic

- Integrate override logic and test transitions.
- Debounce pedestrian buttons and integrate countdown display.

Week 3: Full System Integration & Testing

- Simulate full system behavior.
- Test all input conditions.
- Record demo video.
- Final documentation and report.

Deliverables

- Complete circuit design or HDL source code.
- FSM diagrams.
- Truth tables and logic expressions.
- Simulated test cases.
- Demo video (2-5 minutes).
- Final report (PDF).
- GitHub Repository with all source files, simulation results, and documentation.
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- GitHub Submission Instructions
- Each team must create a public GitHub repository named:
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- smart-traffic-controller
- The repository should include:
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- README.md with project description, authors, and setup instructions.
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- Folder structure:
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- /docs # Reports, FSM diagrams, truth tables
- /src # HDL or Logisim files
- /simulation # Screenshots, testbenches, outputs
- /demo # Final demo video
- Share the GitHub repo link via this email: djleakpor@tubmanu.edu.lr
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- Bonus marks for professional commit history and use of GitHub Issues or Projects.

FSM Diagrams: (Starter outline)

1. **Traffic Light FSM**: States - NS_Green, NS_Yellow, EW_Green, EW_Yellow
2. **Pedestrian FSM**: States - Idle, Wait, Cross, Reset
3. **Emergency FSM**: States - Normal, Emergency_Override, Resume

Due Date: May 7, 2025