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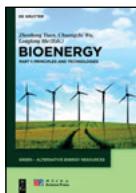
Satish Kumar Peddapelli

PULSE WIDTH MODULATION

ANALYSIS AND PERFORMANCE
IN MULTILEVEL INVERTERS

Satish Kumar Peddapelli
Pulse Width Modulation

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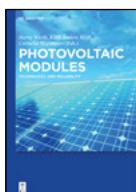
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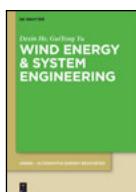
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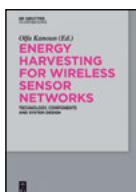
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Satish Kumar Peddapelli

Pulse Width Modulation

Analysis and Performance in Multilevel Inverters

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OLDENBOURG

Author

Dr. Satish Kumar Peddapelli

Department of Electrical Engineering
University College of Engineering
Osmania University, Hyderabad
Telangana State, India
satish_8020@yahoo.co.in

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Preface

The output voltage of a power inverter is a pure sinusoidal waveform with minimum distortion. However, for practical inverters, the output voltage is a series of rectangular waveforms. The major issue for the control of the power inverters is obtaining suitable modulation methods to control the output rectangular waveforms in order to synthesize the desired waveforms. Therefore, a modulation control method is required to get a desired fundamental frequency voltage and to eliminate higher-order harmonics as much as possible.

Higher frequencies are employed in traditional pulse width modulation (PWM) methods because the undesirable harmonics present at higher frequencies, which can be filtered easily and several kilohertz, is well above the acoustic noise level. However, the traditional PWM methods cause electromagnetic interference (EMI). The rapid change in voltage (dv/dt) is the cause of EMI. A high dv/dt produces common-mode voltages across the windings of motor and leads to damage it.

In multilevel inverters, as the switching involves several small voltages, the rapid change in voltage is smaller. Further, switching at the fundamental frequency will also result in a decrease in the number of times these voltage changes occur per fundamental cycle. However, harmonic elimination is a major issue for multilevel inverters. The harmonic elimination in multilevel inverters has been proposed in this book for the following reasons:

- i. Harmonics in output voltage create power losses in equipments.
- ii. Harmonics are the source of EMI. Protecting devices like snubber circuits and filters have to be incorporated in the designed circuits to eliminate harmonics. Hence, the cost of the circuits increases.
- iii. EMI can interfere with signals used to control power electronic devices and radio signals.
- iv. Harmonics can create losses in power equipments. Harmonic currents in an induction motor will dissipate the power in the stator and motor windings.
- v. Harmonics can lower the load power factor.

As mentioned earlier, multilevel inverters result in a better approximation of the sinusoidal waveform because of the increased number of DC voltage levels. The increased number of DC voltage levels provides an opportunity to eliminate more harmonic contents. The remaining harmonic content can be easily eliminated by less expensive smaller filters; because of large number of DC voltages used in multilevel inverters to block smaller voltages, several switches are needed. Since switch stress is reduced and lower switch ratings are used, if any component fails in the inverter, it will be still usable at reduced power level. In a multilevel inverter, there will be more than one way to generate the desired voltages due to switching redundancies. This will allow for the utilization of smaller and more reliable components. One disadvantage

of multilevel inverters is that they require more devices than traditional inverters. The system cost may increase. The probability of system failure increases and the control of the switches is also more complicated because of more devices.

There are four kinds of control methods for multilevel inverters: traditional PWM control method, selective harmonic elimination method, space vector control method, and space vector PWM method. Space vector PWM is considered a better technique of PWM implementation owing to its associated advantages such as better fundamental output voltage, better harmonic performance, and easier implementation in digital signal processor and microcontrollers.

For these reasons, in this book, space vector PWM-based algorithms are proposed and implemented for neutral point-clamped multilevel inverter fed induction motor. These space vector-based algorithms generate not only the desired fundamental frequency voltages, but also eliminate the harmonics up to the maximum possible extent and results in reduces total harmonic distortion (THD).

The work presented in this book offers a general approach for PWM techniques and multilevel inverter topologies. The main objective of this book is to provide detailed analysis and implementation of space vector PWM technique applied to neutral point-clamped multilevel inverter. This book is extremely useful for undergraduate students, postgraduate students, industry people, and especially for research scholars working in the area of multilevel inverters.

This book presented various space vector PWM-based algorithms for multilevel neutral point-clamped inverter fed induction motor. The performance of these algorithms are evaluated in terms of inverter output voltage, current waveforms, THD, speed of induction motor, and torque ripples, and the results have been analyzed and presented.

Chapter organization of the book

This book is organized in the following manner:

Chapter 1 discusses pulse width modulation, various basic pulse width modulation techniques, advanced modulation techniques, space vector pulse width modulation technique, and the advantages of pulse width modulation techniques.

Chapter 2 presents the features of space vector pulse width modulation, space vector concept, and the two-level inverter. The implementation of space vector pulse width modulation technique is explained in detail and is applied to a two-level inverter.

Chapter 3 presents the introduction to multilevel inverter, multilevel inverter topologies, and their working principles. The advantages and disadvantages of various topologies are discussed in detail.

Chapter 4 presents the space vector pulse width modulation (SVPWM) algorithm for a three-level inverter fed induction motor. This SVPWM algorithm provides high-safety voltages with fewer harmonic components compared with two-level structures. The results and analysis of this method have been presented and analyzed in this chapter.

Chapter 5 presents a method for the generation of space vector PWM for multilevel inverters based on fractal approach for three- and five-level inverters. The fractal approach reduces algorithm complexity and execution time. The results and analysis of this method have been presented and analyzed in this chapter.

Chapter 6 explains a qualitative space vector pulse width modulation algorithm for neutral point-clamped multilevel inverter. In this method, the duty cycles of reference voltage vectors are corrected accordingly to identify the location of the reference voltage vector in each region. The appropriate switching sequence of the region and calculation of the switching ON times for each state are estimated. The results of this qualitative space vector pulse width modulation method have been presented and analyzed in this chapter.

Chapter 7 describes a space vector pulse width modulation algorithm using the decomposition method for seven-level inverter. In this method, the space vector diagram of the seven-level inverter is decomposed into six space vector diagrams of four-level inverters. In turn, each four-level inverter is decomposed into three-level inverters, and finally, the three-level inverter is decomposed into six space vector diagrams of two-level inverters. The proposed method reduces algorithm complexity and execution time. It can also be applied to the multilevel inverters above the seven-level.

Chapter 8 presents an analytical space vector pulse width modulation for multilevel inverters, which improves inverter performance. This method is based on the intrinsic relation between multilevel and two-level space vector pulse width modulation, and the dwelling time of vector calculation is derived from a two-level inverter. This method is applied up to the eleven-level inverter, which can be extended to the n-level inverter as well. The results have been presented and analyzed.

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To my parents Shankar and Aruna,
my wife Roja Rani, and
my Children Sudhamsh and Sudheshna

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Nomenclature and Abbreviations

Nomenclature

V_{dc}	DC link voltage
M	Modulation index
f	Frequency
f_s	Switching frequency
f_1	Fundamental frequency
V_{ref}	Reference Voltage
n	Level inverter
S_L	Lower switch
S_U	Upper switch
C_1, C_2, C_3	Capacitors
V_{ao}, V_{bo}, V_{co}	Pole voltages
V_{ab}, V_{bc}, V_{ca}	Line-to-line voltages
V_a, V_b, V_c	Line voltages
V_{an}, V_{bn}, V_{cn}	Phase voltages
V_{no}	Common mode voltage
I_{ga}, I_{gb}, I_{gc}	Gate currents
I_a, I_b, I_c	Stator currents of induction motor
I_d, I_q	d- and q-axis stator currents
I_{rms}	RMS current
ω	Angular speed
ω_m	Rotor speed of induction motor
\emptyset	Flux
m_a	Amplitude modulation ratio
m_f	Frequency modulation ratio
dv/dt	Change in voltage
T_a, T_b, T_c	Switching times
T_s	Sampling time
P, O, N	Switching states of three-level inverter
A_{00}, A_{01}, A_{02}	Vertices of two-level space vector diagram
$(\alpha_{00}, \beta_{00}), (\alpha_{01}, \beta_{01}), (\alpha_{02}, \beta_{02})$	Co-ordinates of the vertices
$(a_0 b_0 c_0), (a_1 b_1 c_1), (a_2 b_2 c_2)$	Switching states of two-level inverter
R_1, R_2, R_3	Triangular regions of three-level inverter
$A_{00}P$	Reference space vector
m_1, m_2	Duty cycles of reference voltage vector
V_1	Fundamental voltage
$V_{carrier}$	Carrier voltage
(α, β)	Direct and quadrature axis

V_d	Reference voltage vector d-axis component
V_q	Reference voltage vector q-axis component
$V_1, V_2, V_3, V_4, V_5, V_6$	Voltage vectors
T_0, T_1, T_2	Switching times
α	Reference angle
T_L	Load torque
d_1, d_2, d_3	Duty cycles of nearest voltage vectors
θ	Angle of reference vector with zero axis
V^*	Reference voltage vector
V'_0, V'_1, V'_2	Voltage vectors of two-level inverter
$V_{1,N}, V_{2,N}, V_{3,N}$	Voltage vectors of N-level inverter
t'_0, t'_1, t'_2	Switching times of two-level inverter
$t_{1,N}, t_{2,N}, t_{3,N}$	Switching times of N-level inverter
T	Sampling time
A_2, A_3, A_4	Regions of three-level inverter
X, Y	Classification of voltage vectors
$\lambda_1, \lambda_2, \lambda_0$	Three dimension array
N	Level of inverter
T_{a1}, T_{a2}, T_{a3}	Switching devices
S	Hexagon number
V^7*	Reference vector of seven-level inverter
V_d^{7*}	d-axis component of seven-level voltage vector
V_q^{7*}	q-axis component of seven-level voltage vector
V^{4*}	Reference vector of four-level inverter
V_d^{4*}	d-axis component of four-level voltage vector
V_q^{4*}	q-axis component of four-level voltage vector
V^{3*}	Reference vector of seven-level inverter
V_d^{3*}	d-axis component of three-level voltage vector
V_q^{3*}	q-axis component of three-level voltage vector
V^{2*}	Reference voltage vector of two-level inverter

Abbreviations

ac	Alternating current
dc	Direct current
PWM	Pulse width modulation
SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
VSI	Voltage source inverter
NPC	Neutral point-clamped

DCMLI	Diode-clamped multilevel inverter
NPCMLI	Neutral point-clamped multilevel inverter
FCMLI	Flying capacitor multilevel inverter
CCMLI	Cascaded cell multilevel inverter
IGBT	Insulated gate bipolar transistor
ANN	Artificial neural network
FFT	Fast Fourier transformation
THD	Total harmonic distortion
ZVV	Zero-voltage vectors
LSVV	Lower small-voltage vectors
USVV	Upper small-voltage vectors
SVV	Small-voltage vectors
MVV	Middle-voltage vectors
LVV	Large-voltage vectors

1 Pulse width modulation techniques

In power electronic converters, the electrical energy from one level of voltage/current/frequency is converted into another using semiconductor-based electronic switch. The essential characteristic of these types of circuits is that the switches are operated only in one of two states – either fully ON or fully OFF – unlike other types of electrical circuits where the control elements are operated in a linear active region.

As the power electronics industry developed, various families of power electronic converters have evolved, often linked by power level, switching devices, and topological origins [3]. Application areas of power converters improved vastly in semiconductor technology, which offer higher voltage and current ratings as well as better switching characteristics. Meanwhile, the main advantages of modern power electronic converters are high efficiency, low weight, small dimensions, fast operation, and high-power densities.

The process of switching the electronic devices in a power electronic converter from one state to another is called ‘modulation’. Each family of power converters has preferred modulation strategies associated with it that aim to optimize the circuit operation for the target criteria most appropriate for that family. Parameters such as switching frequency, distortion, losses, harmonic generation, and speed of response are typical of the issues that must be considered when developing modulation strategies for a particular family of converters. The output voltage of power inverter should be a pure sinusoidal waveform with minimum distortion. However, for practical inverters, the output voltage is a series of rectangular waveforms. The major issues for the control of the power inverters are to get suitable modulation methods to control the output rectangular waveforms to synthesize the desired waveforms. Therefore, a modulation control method is required to get a desired fundamental frequency voltage and to eliminate higher-order harmonics as much as possible.

In modern converters, pulse width modulation (PWM) is a high-speed process ranging depending on the rated power from a few kilohertz (motor control) up to several megahertz (resonant converters for power supply). Therefore, first, we discuss about the principle and different topologies regarding PWM.

1.1 Pulse width modulation

The PWM technique is one of the most widely used strategies for controlling the ac output of power electronic converter. In this technique, the duty cycle of converter switches can be varied at a high frequency to achieve a target average low frequency output voltage or current. Modulation theory has been a major research area in power electronics for over three decades and continues to attract considerable attention and interest.

In principle, all modulation schemes aim to create trains of switching pulses that have the same fundamental volt-second average as a target reference waveform at any instant. The major difficulty with these trains of switched pulses is that they also contain unwanted harmonic components that should be minimized. Hence, for any PWM scheme, the primary objective can be identified, which is to calculate the converter switching ON times, which creates the desired (low-frequency) target output voltage or current. Having satisfied this primary objective, the secondary objective for a PWM strategy is to determine the most effective way of arranging the switching process to minimize unwanted harmonic distortion, switching losses, or any other specific performance criterion [7].

The dc input to the inverter is chopped by switching devices in the inverter. The amplitude and harmonic content of the ac waveform is controlled by varying the duty cycle of the switches. The fundamental voltage V_1 has a maximum amplitude of $4 V_d/\pi$ for a square wave output, but by creating notches, the amplitude of V_1 is reduced.

Usually, the power switches in one inverter leg are always either in ON or OFF state. Therefore, the inverter circuit can be simplified into 3 two-position switches. Either the positive or the negative dc bus voltage is applied to one of the motor phases for a short time. PWM is a method whereby the switched voltage pulses are produced for different output frequencies and voltages. A typical modulator produces an average voltage value, equal to the reference voltage within each PWM period. Considering a very short PWM period, the reference voltage is reflected by the fundamental of the switched pulse pattern. The concept of pulse width modulation is shown in Fig. 1.1.

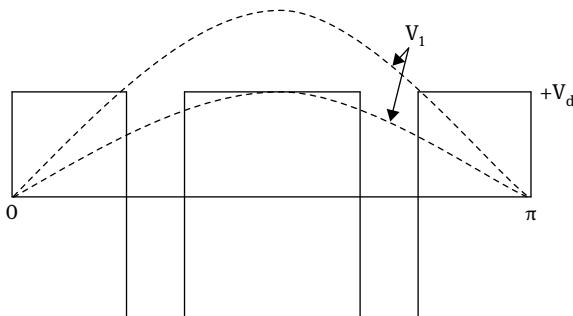


Fig. 1.1: Principle of pulse width modulation.

There are several different PWM techniques, differing in their methods of implementation. However, in all these techniques, the aim is to generate an output voltage, which after some filtering, would result in a good-quality sinusoidal output voltage waveform of desired fundamental frequency and magnitude. However, in the case of inverters, it may not be possible to reduce the overall voltage distortion due to harmonics, but by proper switching control, the magnitudes of lower-order harmonic

voltages can be reduced, often at the cost of increasing the magnitudes of higher order harmonic voltages. Such a situation is acceptable in most cases, as the harmonic voltages of higher frequencies can be satisfactorily filtered using lower sizes of filters and capacitors. Many of the loads, like motor loads, have an inherent quality to suppress high-frequency harmonic currents, and hence, an external filter may not be necessary. To judge the quality of voltage produced by a PWM inverter, a detailed harmonic analysis of the voltage waveform needs to be done.

In fact, after removing a third and multiples of third harmonics from the pole voltage waveform one obtains the corresponding load phase voltage waveform. The pole voltage waveforms of three-phase inverter are simpler to visualize and analyze, and hence, the harmonic analysis of load phase and line voltage waveforms is done via the harmonic analysis of the pole voltages. It is implicit that the load phase and line voltages will not be affected by the third and multiples of third-harmonic components that may be present in the pole voltage waveforms.

1.2 Basic pulse width modulation techniques

1.2.1 Single pulse width modulation

In single PWM control, the width of the pulse is varied to control the inverter output voltage, and there is only one pulse half per cycle. By comparing the rectangular reference signal with the triangular carrier wave the gating signals are generated, as shown in Fig. 1.2. The frequency of reference signal determines fundamental frequency of the output voltage.

The advantages of this technique are that the even harmonics are absent due to the symmetry of the output voltage along the x-axis and that the Nth harmonics can be eliminated from inverter output voltage if the pulse width is made equal to $2\pi/n$. However, the disadvantages are that the output voltage introduces a great deal of harmonic content and that at a low output voltage, the distortion factors increases significantly.

1.2.2 Multiple pulse width modulation

In multiple PWM, several equidistant pulses per half cycle are generated, as shown in Fig. 1.3. Using several pulses in each half cycle of the output voltage, the harmonic content can be reduced.

In this technique, the amplitudes of lower-order harmonics are reduced and the derating factor is reduced significantly. However, the fundamental component of the output voltage is less, the amplitudes of higher-order harmonics increases significantly, and switching losses are increased.

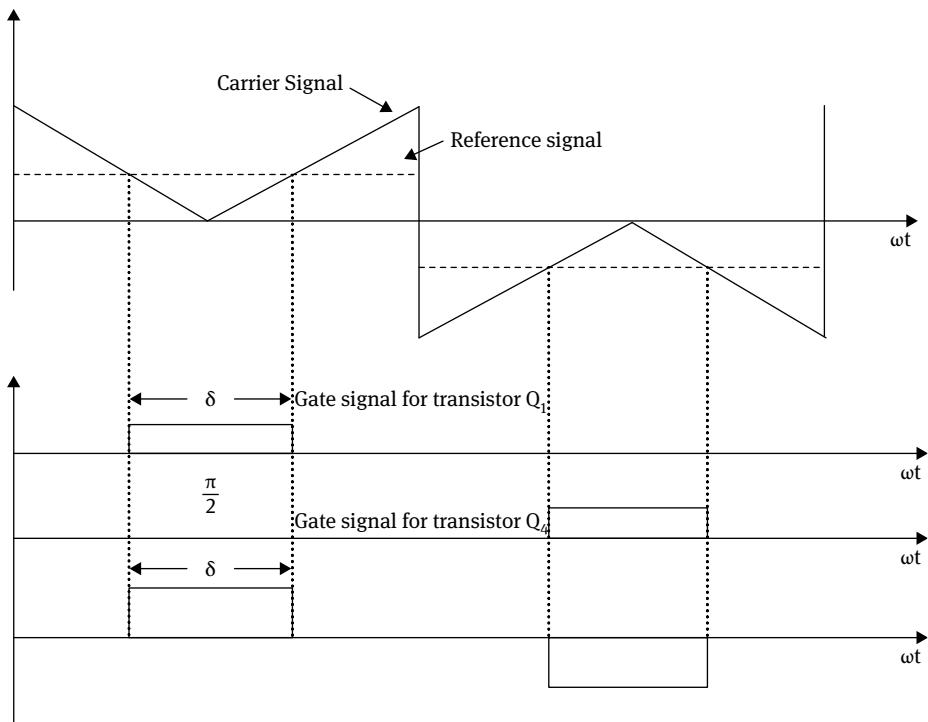


Fig. 1.2: Single pulse width modulation.

1.2.3 Sinusoidal pulse width modulation

In many industrial applications, to control the inverter output voltage sinusoidal PWM (SPWM) is used. SPWM provides good performance of the drive in entire range of operation between 0 and 78% of the value that would be reached by square wave operation. If the modulation index exceeds this value, the linear relationship between the modulation index and the output voltage is not maintained, and over-modulation methods are required. The SPWM refers to the generation of PWM outputs with sine wave as the modulating signal. In this modulation method, the ON and OFF instances of the PWM signals can be determined by comparing a reference signal with a high-frequency triangular wave, as shown in Fig. 1.4. The frequency of the output voltage can be determined by the frequency of the modulation wave. The peak amplitude of the modulating wave determines the modulation index and in turn controls the RMS value of the output voltage. When the modulation index is changed, the RMS value of the output voltage also changes. This technique improves the distortion factor significantly compared to other ways of multiphase modulation. It eliminates all harmonics less than or equal to $(2n - 1)$, where n is defined as the

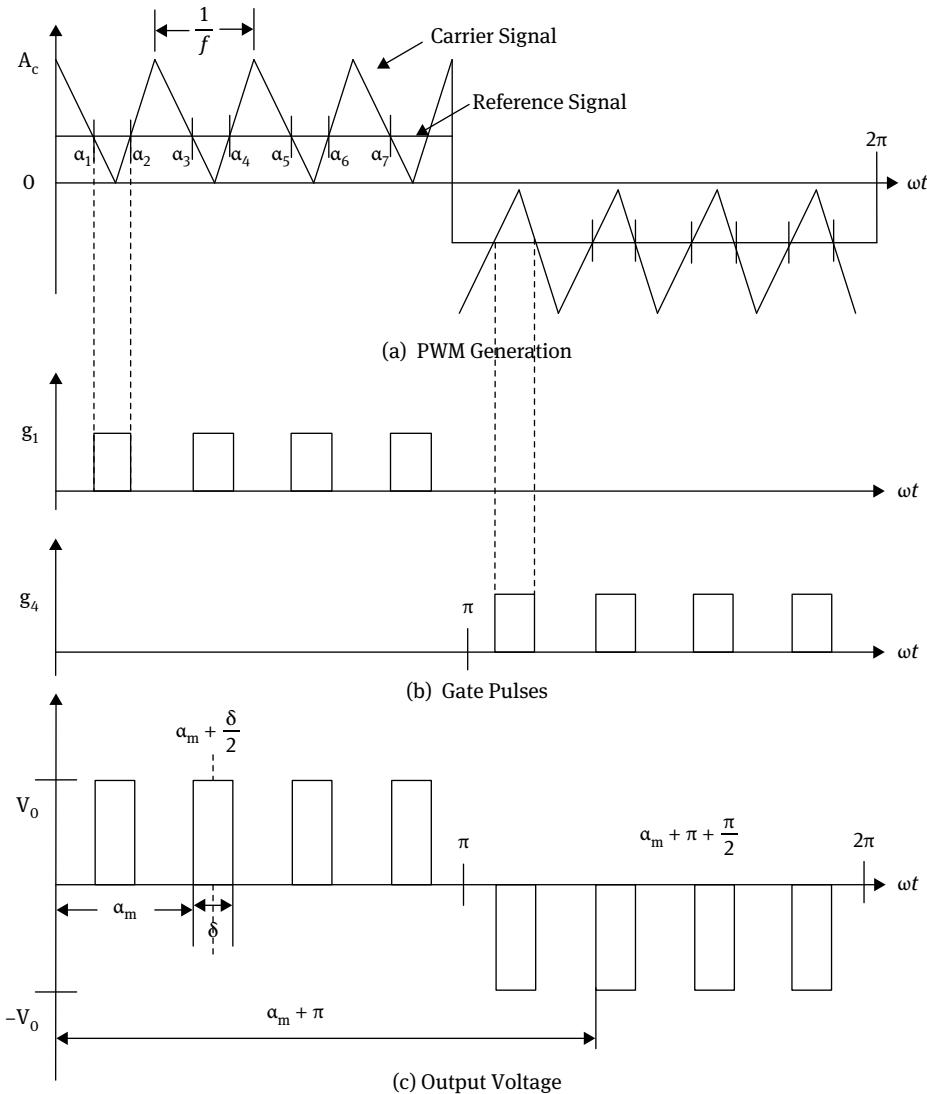


Fig. 1.3: Multiple pulse width modulation.

number of pulses per half cycle of the sine wave. The output voltage of the inverter contains harmonics. However, the harmonics are pushed to the range around the carrier frequency and its multiples.

$$\text{Amplitude modulation ratio: } m_a = \frac{\text{peak amplitude of } V_{\text{control}}}{\text{amplitude of } V_{\text{carrier}}} = \frac{\text{Peak value of } (V_{A0})_1}{V_{dc}/2},$$

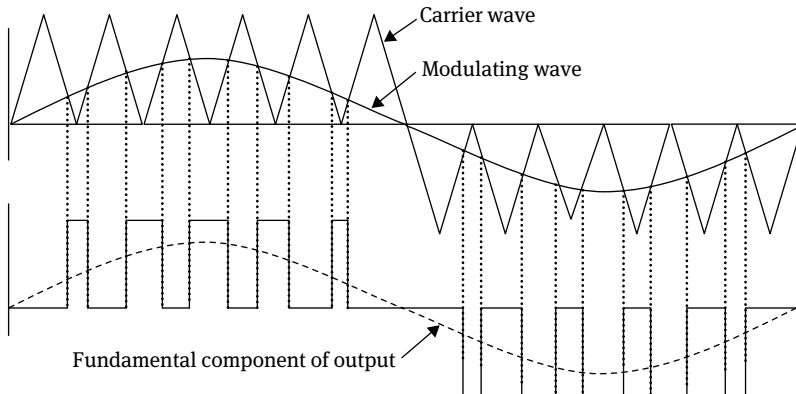


Fig. 1.4: Sinusoidal pulse width modulation.

where $(V_{AO})_1$ is the fundamental frequency component of the pole voltage V_{AO} . The frequency modulation ratio (m_f), which should be an odd integer, is the ratio between the PWM frequency and the fundamental frequency.

- i. If m_f is not an integer, subharmonics may exist at output voltage.
- ii. If m_f is not odd, dc component may exist and even harmonics are present at output voltage.
- iii. m_f should be a multiple of 3 for three-phase PWM inverter.
- iv. An odd multiple of three and even harmonics are suppressed.

1.3 Advanced modulation techniques

1.3.1 Trapezoidal modulation

By comparing a triangular carrier wave (V_c) with a reference trapezoidal wave (V_r), the switching instance to semiconductor devices are generated as shown in Fig.1.5. This type of modulation increases the peak fundamental output voltage up to $1.05 V_d$, but output voltage contains lower-order harmonics.

1.3.2 Staircase modulation

In staircase PWM, the modulated wave eliminates specific harmonics. To obtain the desired quality of the output voltage, the modulation frequency ratio m_f and the number of steps are chosen as shown in Fig. 1.6. If the number of pulses is less than 15 per half cycle, this is optimized PWM.

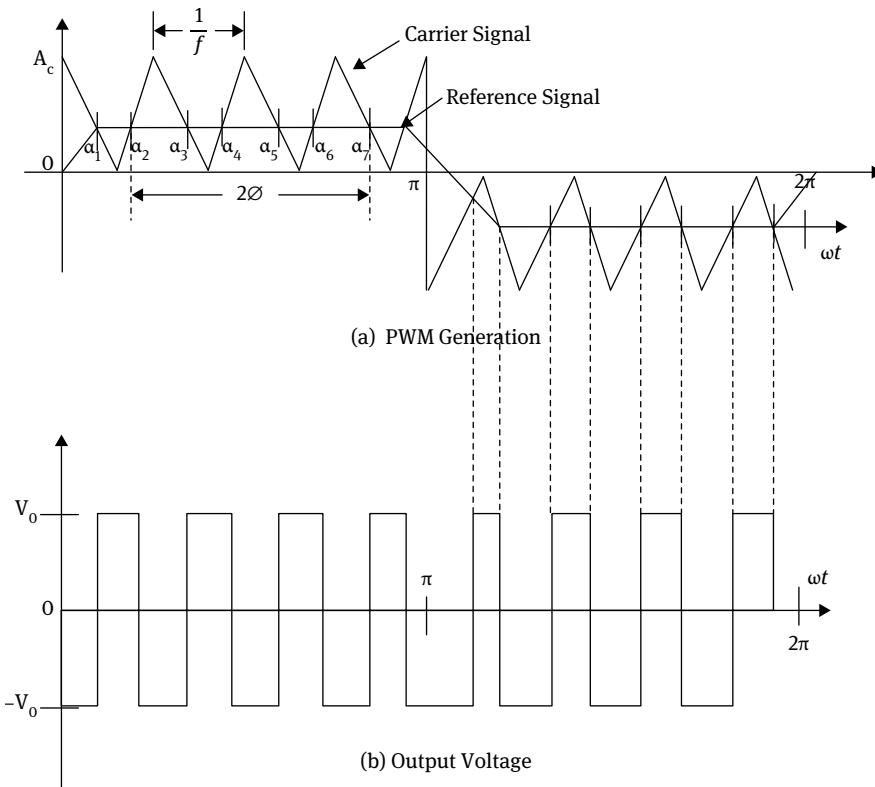


Fig. 1.5: Trapezoidal modulation.

1.3.3 Stepped modulation

In this modulation, the signal is stepped wave. To control the magnitude of the fundamental component and to eliminate specific harmonics, this wave is divided into specific intervals, with each interval being controlled individually as shown in Fig. 1.7. When compared to that of normal PWM control, this type of control gives low distortion but higher fundamental amplitude.

1.3.4 Harmonic-injected modulation

In this modulation, the signal is generated by injecting harmonics to the sine wave as shown in Fig. 1.8. The result is a flat topped wave form and it reduces the amount of over modulation. A higher fundamental amplitude and low distortion of the output voltage is provided. The amplitude of fundamental components is approximately 15% more than that of normal SPWM.

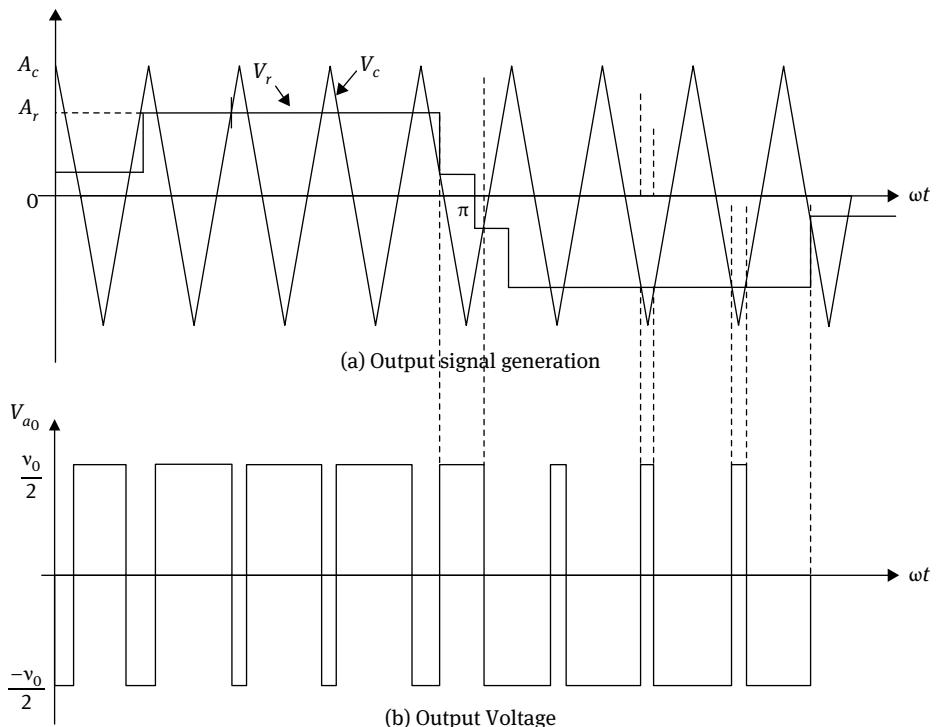


Fig. 1.6: Staircase modulation.

1.3.5 Delta modulation

In this modulation, a triangular wave is allowed to oscillate within a defined window ΔV above and below the reference wave V_r . From the vertices of the triangular wave V_c , the output voltage is generated as shown in Fig. 1.9. This type of modulation is also known as hysteresis modulation. If the frequency of modulating wave is changed while keeping the slope of the triangular wave constant, the number of pulses and pulse widths of modulated wave would change. The fundamental output voltage can be up to V_s and is dependent on peak amplitude A_r and frequency f_r of the reference voltage. This modulation can control the ratio of voltage to frequency. Depending on the permissible harmonic content in the inverter output voltage, machine type, power level, and semiconductor switching devices employed for a particular application, the particular PWM is chosen.

1.3.6 Space vector pulse width modulation

This modulation is a relatively new and popular technique in controlling motor devices. In the space vector PWM (SVPWM) method, the output voltage is approximated using the nearest three output vectors that the nodes of the triangle containing the

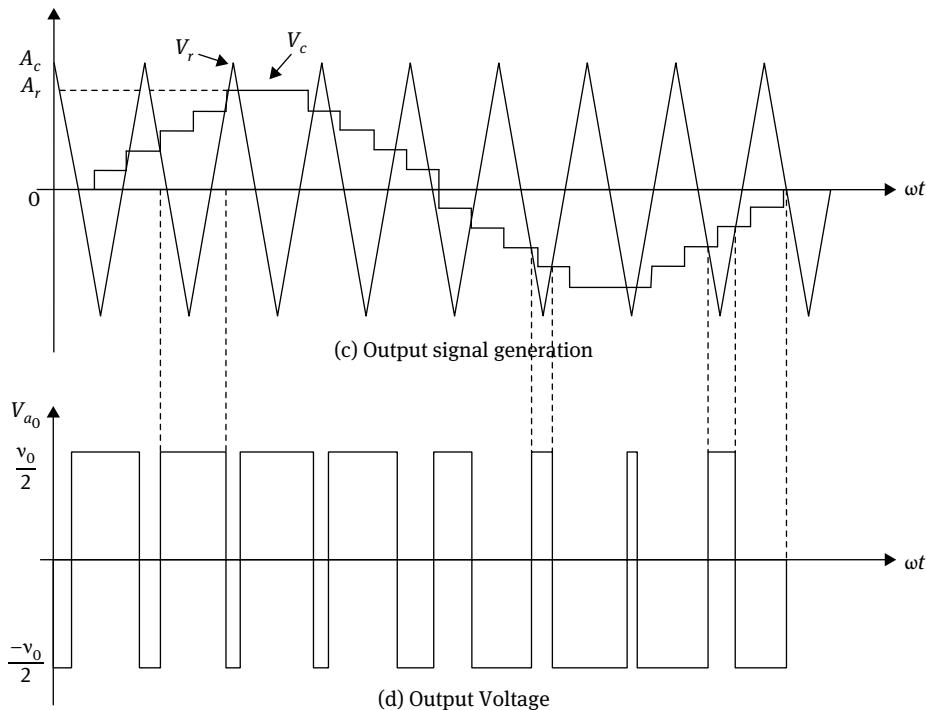
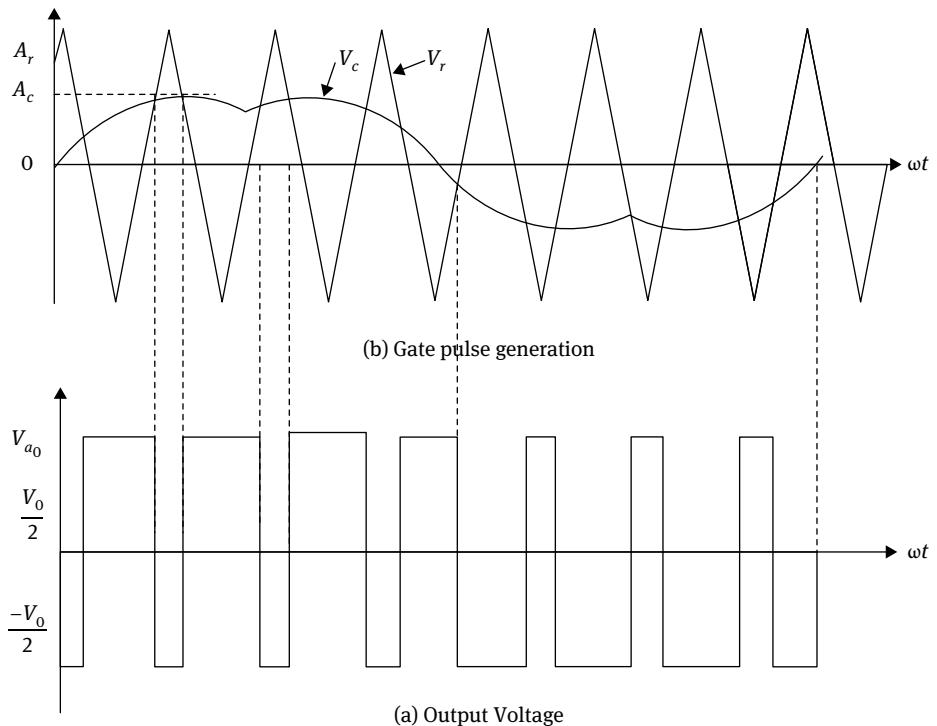


Fig. 1.7: Stepped modulation.

reference vector in the space vector diagram of the inverter. When the reference vector changes from one region to another, it may induce an abrupt change in the output vector. In addition we need to calculate the switching sequences and switching time of the states at every change of the reference voltage location.

1.4 Advantages of pulse width modulation techniques

- i. Using PWM techniques, lower-order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are also minimized.
- ii. Both output voltage control and frequency control are possible in a single power stage of the inverter without any additional components.
- iii. The presence of constant dc supply permits the parallel operation of several independent PWM inverters on the same rectifier power supply. The PWM inverter has a transient response that is much better than that of a quasi-square wave rectifier.
- iv. The commutative ability of PWM inverters remains substantially constant compared to variable dc-link inverter, irrespective of the voltage and frequency settings.

**Fig. 1.8:** Harmonic-injected modulation.

- v. The power factor of the system is good, as a diode rectifier can be employed on the line side.
- vi. With constant dc supply used in PWM, we can obtain commutation even at low voltage, whereas a six-step inverter needs an auxiliary dc supply for commutating thyristors at low output voltages.
- vii. The amplitude of the torque pulsations are minimized even at low speeds.
- viii. A sophisticated PWM technique eliminates lower-order harmonics in the motor current, low-speed torque pulsations, and cogging effects.

1.5 Conclusions

In this chapter, the necessity of PWM in various power electronic converters is presented in detail as well as the basic and advanced PWM techniques. The advanced modulation techniques such as trapezoidal modulation, staircase modulation, stepped, harmonic-injected modulation, delta modulation, and SVPWM are specially recommended for multilevel inverters of various topologies to reduce the THD, dv/dt

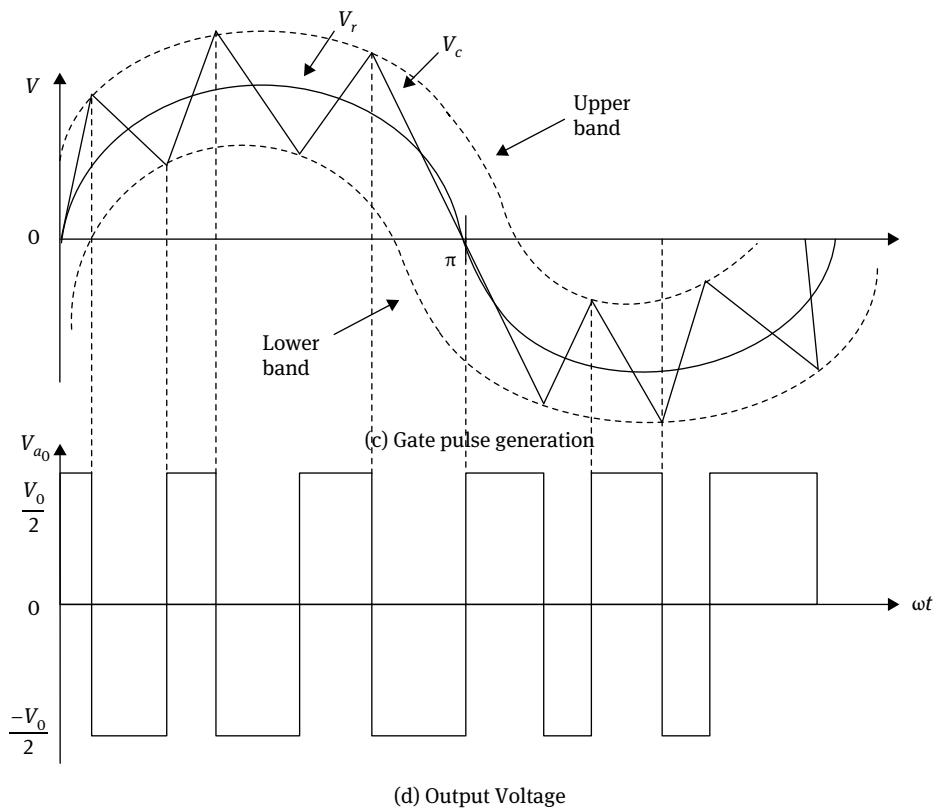


Fig. 1.9: Delta modulation.

effect, switching frequency, and switching losses. SVPWM is more robust than THD because of its flexibility in redundant state selection in case of higher levels. Finally, the advantages of PWM techniques have been discussed to give a clear idea of PWM.

2 Space vector pulse width modulation technique

One of the most popular modulation approaches for two-level converters is space vector pulse width modulation (SVPWM), which is increasingly being used in the control of multilevel converters. This is an advanced and computation-intensive PWM technique. The SVPWM increases the output capability of sinusoidal PWM without distorting the line-to-line output voltage waveform.

The concept of space voltage vectors corresponding to various switching states has been applied in the study of impact of various switching states on the capacitor charge balancing. An advantage of the SVPWM is the instantaneous control of switching states and the freedom to select vectors in order to balance the NP. Additionally, one can realize output voltages with almost any average value using the nearest three vectors, which is the method that results in the best spectral performance. The SVPWM method is an advanced, computation-intensive PWM method and is possibly the best among all the PWM techniques for variable frequency drive applications. Because of its superior performance characteristics, it has been finding widespread application in recent years. If the switching frequency is high enough, the losses due to the harmonics can be almost neglected, and the SVPWM is a better solution in terms of inverter output voltage, harmonic losses, and number of switching per cycle [13].

2.1 Features of SVPWM

The SVPWM technique is more popular than conventional technique because of the following excellent features:

- i. It achieves the wide linear modulation range associated with PWM, third-harmonic injection automatically.
- ii. It has lower base band harmonics than regular PWM or other sine-based modulation methods, or otherwise optimizes harmonics.
- iii. 15% more output voltage than conventional modulation, i.e. better dc-link utilization.
- iv. More efficient use of dc supply voltage.
- v. Advanced and computation-intensive PWM technique.
- vi. Higher efficiency.
- vii. Prevent unnecessary switching hence less commutation losses.
- viii. A different approach to PWM modulation based on space vector representation of the voltages in the $\alpha\text{-}\beta$ plane.

2.2 Space vector concept

The space vector concept is derived from the rotating field of ac machine that is used for modulating the inverter output voltage. In this modulation technique, the three-phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame or in stationary frame. From this two-phase component, the magnitude of the reference vector can be found and is used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame.

Let the three-phase sinusoidal voltage component be

$$\begin{aligned} V_a &= V_m \sin \omega t \\ V_b &= V_m \sin \left(\omega t - \frac{2\pi}{3} \right) \\ V_c &= V_m \sin \left(\omega t + \frac{2\pi}{3} \right). \end{aligned} \quad (2.1)$$

When this three-phase voltage is applied to the ac machine, it produces a rotating flux in the air gap of the ac machine. This rotating flux component can be represented as single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's transformation as explained below in the stationary reference frame. The representation of rotating vector in complex plane is shown in Fig. 2.1.

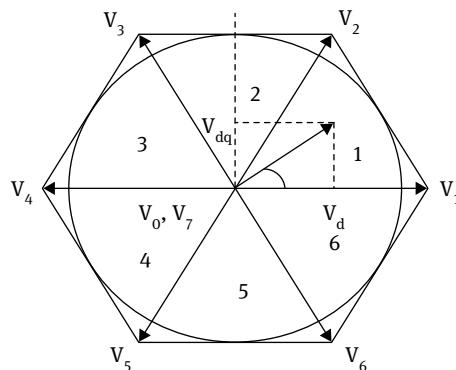


Fig. 2.1: Representation of the rotating vector in a complex plane space vector representation of the three-phase quantity.

$$\overline{V^*} = V_d + jV_q = \frac{2}{3} (V_a + aV_b + a^2V_c), \quad (2.2)$$

where $a = e^{j2\pi/3}$.

$$\overline{|V|} = \sqrt{V_d^2 + V_q^2}; \quad a = \tan^{-1} \left(\frac{V_q}{V_d} \right) \quad (2.3)$$

$$V_d + jV_q = \frac{2}{3} \left(V_a + e^{j\frac{2\pi}{3}} V_b + e^{-j\frac{2\pi}{3}} V_c \right) \quad (2.4)$$

$$V_d + jV_q = \frac{2}{3} \left(V_a + \cos \frac{2\pi}{3} V_b + \cos \frac{2\pi}{3} V_c \right) + j \frac{2}{3} \left(\sin \frac{2\pi}{3} V_b - \sin \frac{2\pi}{3} V_c \right)$$

Equating real and imaginary parts:

$$V_d = \frac{2}{3} \left(V_a + \cos \frac{2\pi}{3} V_b + \cos \frac{2\pi}{3} V_c \right) \quad (2.5)$$

$$V_q = \frac{2}{3} \left(0 \cdot V_a + \sin \frac{2\pi}{3} V_b - \sin \frac{2\pi}{3} V_c \right) \quad (2.6)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \cos \frac{2\pi}{3} & \cos \frac{2\pi}{3} \\ 0 & \sin \frac{2\pi}{3} & -\sin \frac{2\pi}{3} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2.7)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2.8)$$

2.2.1 Principle of SVPWM

The SVPWM treats the sinusoidal voltage as a constant amplitude vector rotating at a constant frequency. This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns. A three-phase voltage vector is transformed into a vector in the stationary d-q coordinate frame, which represents the spatial vector sum of the three-phase voltage.

2.2.2 Definition of space vector

The space vector V_{sr} constituted by the pole voltages V_{ao} , V_{bo} , and V_{co} is defined as

$$V_{sr} = V_{ao} + V_{bo} \cdot e^{j\frac{2\pi}{3}} + V_{co} \cdot e^{j\frac{4\pi}{3}}. \quad (2.9)$$

The relationship between the phase voltages V_{an} , V_{bn} , and V_{cn} and the pole voltages V_{ao} , V_{bo} , and V_{co} is given by

$$V_{ao} = V_{an} + V_{no}; V_{bo} = V_{bn} + V_{no}; V_{co} = V_{cn} + V_{no}. \quad (2.10)$$

Since $V_{an} + V_{bn} + V_{cn} = 0$,

$$V_{no} = \frac{V_{ao} + V_{bo} + V_{co}}{3}, \quad (2.11)$$

where V_{no} is the common mode voltage. From Eqs. (2.9) and (2.10), it is evident that the phase voltages V_{an} , V_{bn} , and V_{cn} also result in the same space vector V_{sr} . The space vector V_{sr} can also be resolved into two rectangular components, namely V_d and V_q . It is customary to place the d-axis along the A-phase axis of the induction motor.

Hence,

$$V_{sr} = V_d + jV_q. \quad (2.12)$$

2.2.3 Advantages of SVPWM

SVPWM is considered a better technique of PWM implementation owing to its associated advantages mentioned below:

- i. Better fundamental output voltage.
- ii. Better harmonic performance.
- iii. Easier implementation in digital signal processor and microcontrollers.

2.3 SVPWM for the two-level inverter

2.3.1 Three-phase voltage source inverter

A three-phase two-level inverter with a star connected load can be represented, as shown in Fig. 2.2, where V_{ao} , V_{bo} , and V_{co} are the inverter output voltages with respect to their return terminal of the dc source marked as 'O'. These voltages are called pole voltages and V_{an} , V_{bn} , and V_{cn} are the load phase voltages with respect to neutral (n). Each switching circuit configuration generates three independent pole voltages V_{ao} , V_{bo} , and V_{co} . There are eight possible switching configurations, called the operating states or inverter states.

2.3.2 Determination of switching states

The possible pole voltages that can be produced at any time are $+0.5 V_{dc}$ and $-0.5 V_{dc}$. For example, when switches S_1 , S_6 , and S_5 are closed then a-phase and c-phase are

connected to the positive dc bus and b-phase is connected to negative dc bus, the corresponding pole voltages are:

$$V_{ao} = +0.5 V_{dc}$$

$$V_{bo} = -0.5 V_{dc}$$

$$V_{co} = +0.5 V_{dc}$$

Using this procedure, the inverter state in the above equation is represented by the notation (+ - +) or 1 0 1 and the corresponding switching state is denoted by V_6 . Thus, every phase of a three-phase voltage source inverter (VSI) can be connected either to the positive or the negative dc bus. The switching states are shown in Fig. 2.3, which are designated using the code numbers 0 to 7.

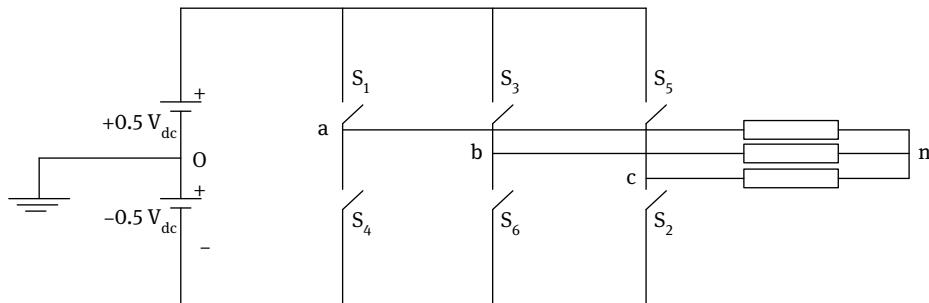


Fig. 2.2: Three-phase two-level inverter.

In case of switching states V_0 and V_7 , all the three poles are connected to the same dc bus, effectively shorting the load and there will be no power transfer between source and load. These two states are called ‘null states’ or ‘zero states’. In case of other switching states, power transfers between source and load. Hence, these states (V_1, V_2, \dots, V_6) are called ‘active voltage vectors’ or ‘active states’.

In terms of phase voltages of inverter, the voltage space vector can be written as shown below:

$$V_{sr} = V_{an} + V_{bn}e^{j\frac{2\pi}{3}} + V_{cn}e^{j\frac{4\pi}{3}}. \quad (2.13)$$

In terms of the pole voltages of the inverter, the voltage space vector can be written as

$$V_{sr} = V_{ao} + V_{bo}e^{j\frac{2\pi}{3}} + V_{co}e^{j\frac{4\pi}{3}}. \quad (2.14)$$

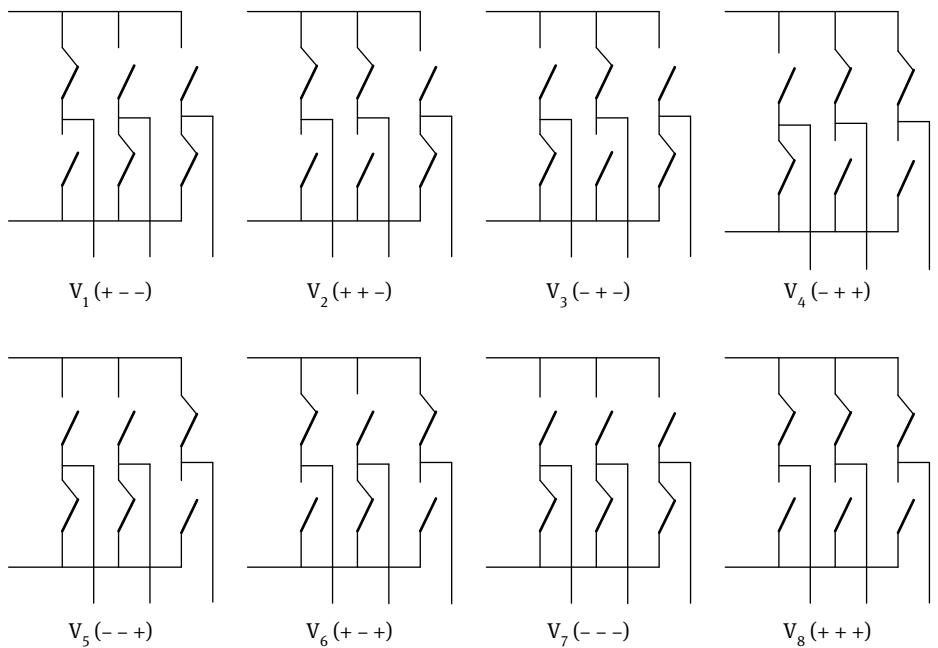


Fig. 2.3: Possible switching states of the two-level inverter.

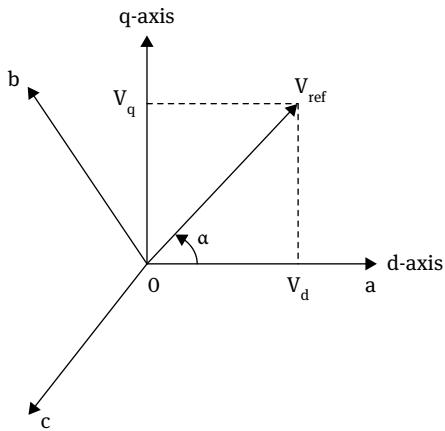


Fig. 2.4: Three-phase (a, b, c) to two-phase (d, q) transformation.

In the implementation of SVPWM, the (a, b, c) reference frame voltage equations are transformed into the d-q reference frame, which is a stationary reference frame, as depicted in Fig. 2.4. As described in Fig. 2.4, this transformation is equivalent to an orthogonal projection of [a, b, c] onto the two dimensions perpendicular to the vector [1, 1, 1] (the equivalent d-q plane) in a three-dimensional coordinate system. The desired reference voltage vector V_{ref} is obtained in the d-q plane by applying the similar

transformation to the desired output voltage. The approximation of the reference vector from the eight switching states is the primary objective of SVPWM technique. The space vector diagram of two-level inverter is as shown in Fig. 2.5.

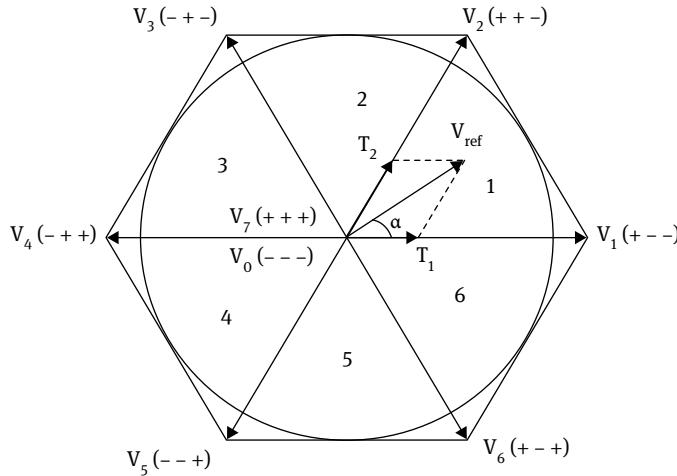


Fig. 2.5: Space vector diagram of the two-level inverter.

2.3.3 Calculation of switching times

The switching times of the SVPWM-based inverter can be calculated using the volt-second relation. Figure 2.6 represents the calculation of switching times based on the voltage-second relation of the reference vector V_{sr} . The volt-second produced by vectors V_1 , V_2 , and V_7 or V_0 along the d and q axes are the same as those produced by the reference vector V_{ref} .

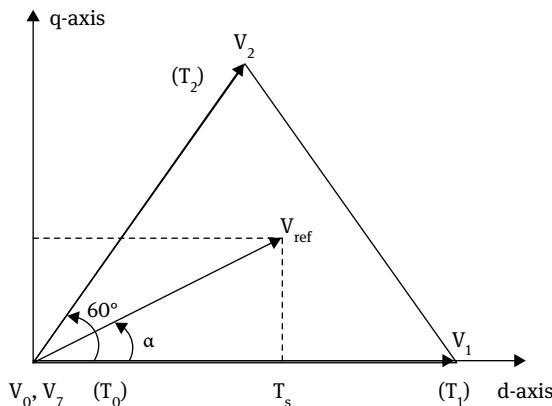


Fig. 2.6: Representation of the reference vector in terms of the volt-second relation.

$$V_{dc} \cdot T_1 + V_{dc} \cos 60^\circ \cdot T_2 = |V_{sr}^*| \cos \alpha \cdot T_s \quad (2.15)$$

$$V_{dc} \sin 60^\circ \cdot T_2 = |V_{sr}^*| \sin \alpha \cdot T_s \quad (2.16)$$

After simplifying, we will get the expressions as

$$T_1 = \frac{(m \times \sin(60^\circ - \alpha))}{\sin(60^\circ)} \quad (2.17)$$

$$T_2 = \frac{(m \times \sin(\alpha))}{\sin(60^\circ)} \quad (2.18)$$

$$T_o = T_s - T_1 - T_2, \quad (2.19)$$

where

$$m = \frac{V_{sr}}{\left(\frac{2}{3}\right)V_{dc}}. \quad (2.20)$$

2.3.4 Optimized switching sequence

The aim of SVPWM is to approximate the reference voltage vector (V_{ref}) in a sampling period by time averaging the three voltage vectors. In the SVPWM strategy, the total zero voltage vector time is equally distributed between V_0 and V_7 . Further, the zero voltage vector time is equally distributed symmetrically at the start and at the end of the subcycle in a symmetrical manner. Moreover, to minimize the switching frequency and reduce the number of commutations, it is desirable that the switching sequence between the three voltage vectors involves only one commutation when there is a transfer from one state to the other. This requires the use of both zero vectors (V_7 and V_0) in a given sector and a reversal of the switching sequence every subcycle.

Thus, SVPWM uses $V_0-V_1-V_2-V_7-V_7-V_2-V_1-V_0$ in sector I, $V_0-V_3-V_2-V_7-V_7-V_2-V_3-V_0$ in sector II, and so on. Table 2.1 depicts the switching sequence for all sectors. The switching times of the two-level inverter at each sector are shown in Tab. 2.2.

The two-level inverters have certain drawbacks:

- i. These are not suitable for high-power levels.
- ii. High-dc-link voltage requires series connection of devices.
- iii. Difficulty in dynamic voltage during switching.
- iv. Multilevel topology has been applied in several situations, such as high-voltage ac drive, FaCTS, SVC, and so on.

Tab. 2.1: Switching sequence of the two-level inverter.

Sector number	ON sequence	OFF sequence
1	$V_0-V_1-V_2-V_7$	$V_7-V_2-V_1-V_0$
2	$V_0-V_3-V_2-V_7$	$V_7-V_2-V_3-V_0$
3	$V_0-V_3-V_4-V_7$	$V_7-V_4-V_3-V_0$
4	$V_0-V_5-V_4-V_7$	$V_7-V_4-V_5-V_0$
5	$V_0-V_5-V_6-V_7$	$V_7-V_6-V_5-V_0$
6	$V_0-V_1-V_6-V_7$	$V_7-V_6-V_1-V_0$

Tab. 2.2: Switching times of the two-level inverter.

Sector	Upper switches	Lower switches
1	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_2 + T_0/2$	$S_6 = T_1 + T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
2	$S_1 = T_1 + T_0/2$	$S_4 = T_2 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
3	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_2 + T_0/2$	$S_2 = T_1 + T_0/2$
4	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_1 + T_0/2$	$S_6 = T_2 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
5	$S_1 = T_2 + T_0/2$	$S_4 = T_1 + T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
6	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_1 + T_0/2$	$S_2 = T_2 + T_0/2$

Multilevel topology has the following advantages over traditional two-level topology:

- The voltage blocked by the power device is decreased tremendously.
- Multilevel inverters produce low harmonic distortion for ac currents even for moderate switching frequency operation and the switch losses are lower than two-level inverters.

2.4 Conclusions

In this chapter, the most recommended PWM technique applied to power electronic inverters has been discussed in detail as well as the features of the space vector modulation technique, concept of space vector with principle of operation, theoretical analysis of SVPWM, pros and cons, and finally, analysis of space vector modulation to two-level inverter. The analysis of VPWM, including the determination of switching states and calculation of switching times and optimized switching sequence when applied to a two-level VSI, has been presented with operation state diagrams. The main objective of this chapter is to help the reader understand how space vector modulation is implemented in case of a two-level VSI. To enrich the analysis, the simulation results of space vector pulse width-modulated two-level inverter are furnished at the end.

3 Multilevel inverter topologies

Recently, the multilevel inverter technology has emerged as a very important alternative in the area of medium-voltage, high-power applications. As the name indicates, multilevel inverters can produce more than two levels at its output phases. Multilevel inverters also provide benefits such as improved output voltage spectrum. Multilevel inverters offer many benefits for higher-power applications. In particular, these include the ability to synthesize voltage waveform with lower harmonic content than two-level inverters and operation at higher dc voltages using series-connected semiconductor switches. Multilevel inverters with neutral point-clamped (NPC) or diode-clamped technology were introduced in 1980. In the 1990s, new multilevel inverter topologies were introduced. Some important multilevel inverter topologies are NPC multilevel inverter, flying-capacitor multilevel inverter, and cascaded H-bridge multilevel inverter. However, due to simple construction features and other advantages, the NPC topology is widely used.

Higher frequencies are employed in traditional pulse width modulation (PWM) methods because of the undesirable harmonics occurring at higher frequencies, which can be filtered easily and several kilohertz well above the acoustic noise level. However, the traditional PWM methods cause electromagnetic interference (EMI). The rapid change in voltage (dv/dt) is the cause of EMI. A high dv/dt produces common-mode voltages across the windings of motor and leads to damage.

In multilevel inverters, as the switching involves several small voltages, the rapid change in voltage is smaller. Further, switching at the fundamental frequency will also result in the decrease of the number of times these voltage changes occur per fundamental cycle. However, harmonic elimination is the major issue for multilevel inverters. For the following reasons, harmonic elimination in multilevel inverters has been proposed in this book.

- i. Harmonics in output voltage create power losses in equipments.
- ii. Harmonics are the source of EMI.
- iii. Protecting devices such as snubber circuits and filters have to be incorporated in the designed circuits for the elimination of harmonics. Hence, the cost of the circuits increases.
- iv. EMI can interfere with control signals used to control power electronic devices and radio signals.
- v. Harmonics can create losses in power equipments. Harmonic currents in an induction motor will dissipate power in stator and motor windings.
- vi. Harmonics can lower the load power factor.

As mentioned earlier, the use of multilevel inverters results in a better approximation to a sinusoidal waveform because of increased number of dc voltages. These increased number of dc voltages provides the opportunity to eliminate more harmonic contents.

The remaining harmonic content can be easily eliminated by less expensive, smaller filters. Because of the large number of dc voltages used in multilevel inverters, several switches are needed to block smaller voltages. Since switch stress is reduced and lower switch ratings are used, if any component fails in the inverter, it will be still usable at reduced power level. In a multilevel inverter, there will be more than one way to generate the desired voltages due to switching redundancies [20]. This will allow for the utilization of smaller and more reliable components. One disadvantage of multilevel inverters is that they require more devices than traditional inverters. Hence, system cost may increase. The probability of system failure increases and control of the switches is also more complicated due to more devices.

There are four kinds of control methods for multilevel inverters. They are traditional PWM control method, selective harmonic elimination method, space vector control method, and SVPWM method. SVPWM is considered a better technique of PWM implementation owing to its associated advantages such as better fundamental output voltage, better harmonic performance, and easier implementation in digital signal processor and microcontrollers.

The main features of multilevel inverter are:

1. Ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the dc bus.
2. Important when a high-dc side voltage is imposed by an application (e.g. traction systems).
3. Even at low switching frequencies, a small distortion in the multilevel inverter ac side waveform can be achieved (with stepped modulation technique).

3.1 Diode-clamped multilevel inverter

The diode-clamped multilevel inverter (dcMI) or NPC multilevel inverter is based on the concept of using diodes to limit power devices voltage stress. The structure and basic operating principle consists of series-connected capacitors that divide the dc bus voltage into a set of capacitor voltages.

- i. A DCMI with n number of levels typically comprises $(N - 1)$ capacitors on the dc bus.
- ii. Voltage across each capacitor is $V_{dc}/(N - 1)$.
- iii. Output phase voltage can assume any voltage level by selecting any of the nodes.
- iv. The DCMI is considered a type of multiplexer that attaches the output to one of the available nodes.
- v. It consists of main power devices in series with their respective main diodes connected in parallel and clamping diodes.

- vi. Main diodes conduct only when most upper or lower node is selected.
- vii. Although the main diodes have the same voltage rating as main power devices, much lower current rating is allowable.
- viii. In each phase leg, the forward voltage across each main power device is clamped by the connection of diodes between the main power devices and the nodes.
- ix. The number of power devices in the ON state for any selection of node is always equal to $(N - 1)$.

The three-phase six-level diode-clamped inverter is shown in Fig. 3.1. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc} and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Table 3.1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage V_0 as a reference. State condition 1 means the switch is ON, and 0 means the switch is OFF. Each phase has five complementary switch pairs, such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg 'a' are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, and $(S_{a5}, S_{a'5})$. Table 3.1 also shows that in a diode-clamped inverter, the switches that are ON for particular phase legs are always adjacent and in series. For a six-level inverter, a set of five switches is ON at any given time.

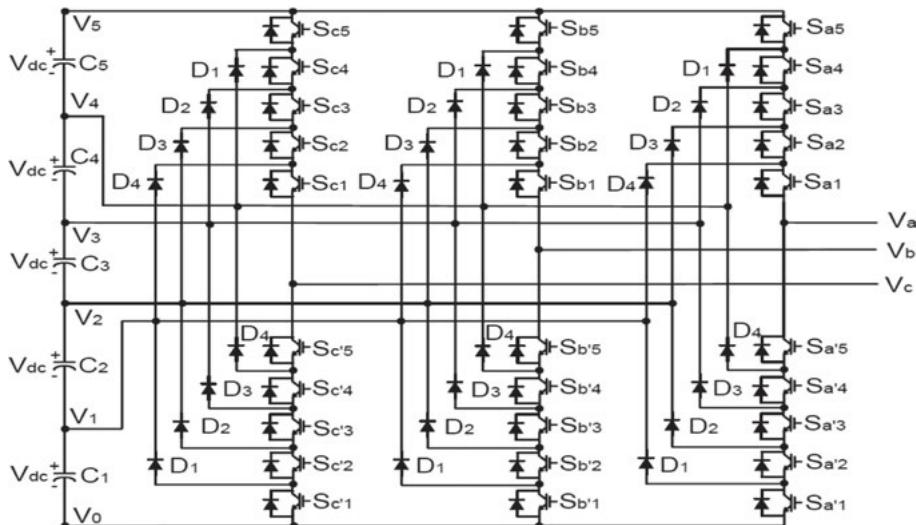


Fig. 3.1: Three-phase six-level diode-clamped inverter.

Tab. 3.1: Switching states of the six-level diode-clamped inverter.

Voltage V_{ao}	Switching states									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5 V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4 V_{dc}$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3 V_{dc}$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2 V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_1 = 1 V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_o = 0$	0	0	0	0	0	1	1	1	1	1

3.1.1 General features

- i. For three-phase dcMI, the capacitors need to filter only the high-order harmonics of the clamping diodes currents, low-order components intrinsically cancel each other.
- ii. For dcMI employing step modulation strategy, if n is sufficiently high, filters may not be required at all due to the significantly low harmonic content.
- iii. If each clamping diode has same voltage rating as power devices, for n -level dcMI.
- iv. Number of clamping diodes/phase = $(N - 1) \times (N - 2)$.
- v. Each power device blocks only a capacitor voltage.

3.1.2 Advantages

- i. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
- ii. The capacitors can be precharged as a group.
- iii. Efficiency is high for fundamental frequency switching.

3.1.3 Disadvantages

- i. Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- ii. The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

3.2 Flying capacitor multilevel inverter

Flying capacitor multilevel inverter is capable of solving capacitor voltage unbalance problem and excessive diode count requirement in diode capacitor multilevel inverter

and it is also known as flying capacitor multilevel inverter (capacitors are arranged to float with respect to earth). The structure and basic operating principle of flying capacitor multilevel inverter are the following:

- i. Employs separate capacitors precharged to

$$\left[\frac{(N-1)}{(N-1)} \times V_{dc} \right], \left[\frac{(N-2)}{(N-1)} \times V_{dc} \right], \dots \left\{ \frac{N-(N-1)}{[N-1]} \times V_{dc} \right\}.$$

- ii. The size of voltage increment between two capacitors defines the size of voltage steps in flying capacitor multilevel inverter output voltage waveform.
- iii. N-level flying capacitor multilevel inverter has n-level output phase voltage and $(2N - 1)$ -level output line voltage.
- iv. The output voltage is produced by switching the right combinations of power devices to allow adding or subtracting of capacitor voltages.

For example, the three-phase six-level flying capacitor multilevel inverter is shown in Fig. 3.2. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor.

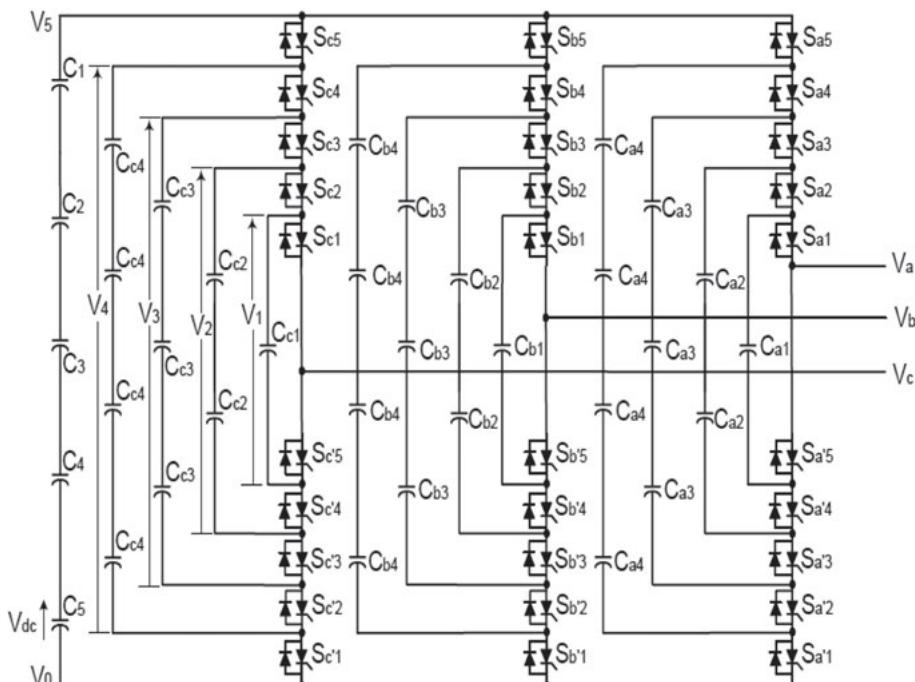


Fig. 3.2: Three-phase six-level flying capacitor inverter.

3.2.1 General features

- i. With step modulation strategy, with sufficiently high n, harmonic content can be low enough to avoid the need for filters.
- ii. Advantage of inner voltage-level redundancies: allows preferential charging or discharging of individual capacitors and facilitates manipulation of capacitor voltages so that their proper values are maintained.
- iii. Active and reactive power flow can be controlled.
- iv. Additional circuit required for initial charging of capacitors.

3.2.2 Advantages

- i. Phase redundancies are available for balancing the voltage levels of the capacitors.
- ii. Real and reactive power flow can be controlled.
- iii. The large number of capacitors enables the inverter to ride through short-duration outages and deep voltage sags.

3.2.3 Disadvantages

- i. Control in tracking the voltage levels for all of the capacitors is complicated. Also, precharging all the capacitors to the same voltage level and startup are complex.
- ii. Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

3.3 Cascade H-bridge multilevel inverter

This refers to modular structured multilevel inverter (MSMI) or series-connected H-bridge inverters. The structure and basic operating principle of cascade H-bridge multilevel inverter consists of $(N - 1)/2$ or h number of single-phase H-bridge inverters (MSMI modules). The MSMI output phase voltage is

$$V_0 = V_{m1} + V_{m2} + \dots + V_{mh}$$

V_{m1} : output voltage of module 1

V_{m2} : output voltage of module 2

V_{mh} : output voltage of module h

A single-phase structure of an m-level cascaded inverter is illustrated in Fig. 3.3. Each separate dc source ($SdcS$) is connected to a single-phase full-bridge or H-bridge

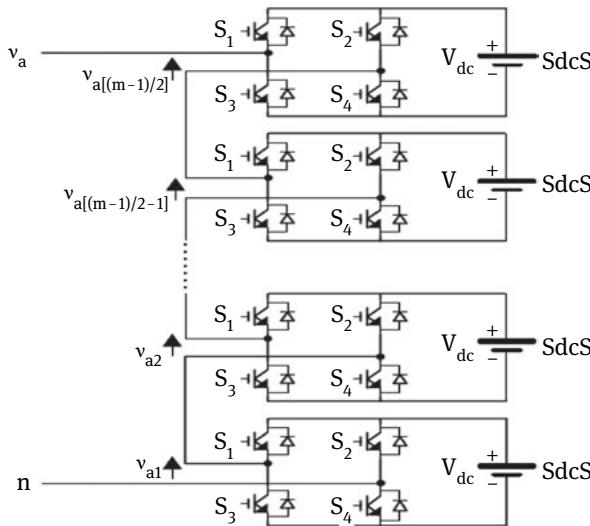


Fig. 3.3: Single-phase structure of cascaded H-bridge inverter.

inverter. Each inverter level can generate three different voltage outputs $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches S_1 , S_2 , S_3 , and S_4 . To obtain $+V_{dc}$, switches S_1 and S_4 are turned ON, whereas $-V_{dc}$ can be obtained by turning ON switches S_2 and S_3 . By turning ON S_1 and S_2 or S_3 and S_4 , the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output-phase voltage levels m in a cascade inverter is defined by $m = 2s + 1$, where s is the number of separate dc sources.

3.3.1 Advantages

- The number of possible output voltage levels is more than twice the number of dc sources ($m = 2s + 1$).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

3.3.2 Disadvantage

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple $SdcSs$ readily available.
- As the level of the output voltage produced increases, the switch count will also increase.

3.4 Conclusions

In this chapter, the state of the art of different multilevel inverters, which have potential applications in the area of medium-voltage and high-power applications, has been discussed. The fundamental multilevel inverter topology, principle of operation, and its features with advantages and disadvantages have been explained in detail for the three basic topologies. The limitations of the two-level inverters in terms of switching frequency, switching losses, and dv/dt issues have been resolved with multilevel inverters. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc-link capacitors for N-level has been described. The main objective of this chapter was to provide a general idea to readers interested in multilevel inverters and the pros and cons of their real-time implementation.

4 Space vector pulse width modulation algorithm for the three-level inverter

Three-level inverter topology is widely used in high-voltage/high-power applications with currently available power devices because of its high-voltage handling and good harmonic rejection capabilities. In the previous chapters, the space vector pulse width modulation (SVPWM) scheme for the two-level inverter is described in detail. However, the three-level inverter roughly has four times better harmonic content compared with two-level topology. The harmonic contents of the output voltage are fewer than those of the two-level inverter at the same switching frequency. In addition, the blocking voltage of each switching device is a half of the dc-link voltage and is thus an easy-to-realize high-voltage and large-capacity inverter system.

In this chapter, the SVPWM algorithm for a three-level inverter fed induction motor is presented and analyzed. This SVPWM algorithm provides high-safety voltages with less harmonic components compared to two-level structures and reduces the switching losses by limiting the switching to two thirds of the pulse duty cycle. The voltage vector selection procedure, switching time calculation, and switching pattern generation for the three-level inverter are described in detail. This SVPWM algorithm contributed to the reduction of switching power losses and has the advantages of a three-level inverter that carry out voltage with contents of less harmonic injection than two-level inverter. The proposed method can be applied to multilevel inverters above the three-level inverters. However, as the level of inverter increases, the sector identification, switching vector determination, and dwelling time calculation become more complex. The computational complexity and the execution time increase.

The implementation of SVPWM involves:

- i. Identification of the sector where the tip of the reference vector lies.
- ii. Determination of the three nearest voltage space vectors.
- iii. Determination of the duration of each of these switching voltage space vectors.
- iv. Choosing an optimized switching sequence.

Sector identification can be done using coordinate transformation of the reference vector into a two-dimensional coordinate system. The sector can also be determined by resolving the reference phase vector along the a-, b-, and c-axes and by repeated comparison with discrete phase voltages. After identifying the sector, the voltage vectors at the vertices of the sector are determined. Once the switching voltage space vectors are determined, the switching sequences can be obtained. The calculation of the duration of the voltage vectors can be simplified by mapping the identified sector to the sector corresponding to the two-level inverter. To obtain optimum switching, the voltage vectors are to be switched for their respective durations, in a sequence such that only one switching occurs as the inverter moves from one switching state

to another. Conventional techniques involve look-up tables to achieve this optimum switching sequence [50].

4.1 SVPWM for the three-level inverter

4.1.1 Three-level inverter topology and switching states

The schematic diagram of a three-level inverter is shown in Fig. 4.1. Each phase of the inverter consists of two clamping diodes, four IGBTs, and four freewheeling diodes. Since three kinds of switching states and terminal voltages exist in each phase, the three-level inverter has 27 (3^3) switching states. Figure 4.2 shows the representation of the space voltage vectors for output voltage and the space vector diagram of all switching states, where P, O, and N represent the terminal voltage, respectively, that is $V_{dc}/2$, 0, $-V_{dc}/2$ (Tab. 4.1). According to the magnitude of the voltage vectors, we divide them into four groups: zero-voltage vector (ZVV; V_0), small-voltage vectors (SVVs; V_1 , V_4 , V_7 , V_{10} , V_{13} , V_{16}), middle-voltage vectors (MVs; V_3 , V_6 , V_9 , V_{12} , V_{15} , V_{18}), and large-voltage vector (LVV; V_2 , V_5 , V_8 , V_{11} , V_{14} , V_{17}). The ZVV has three switching states; SVV, two switching states; and the MV and LV have only one switching state.

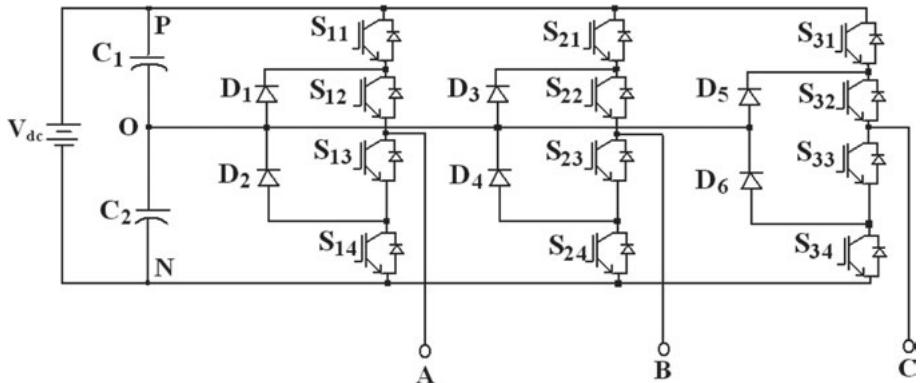


Fig. 4.1: Schematic diagram of the three-level inverter.

Tab. 4.1: Switching states of the three-level inverter.

Switching symbols	Switching conditions				Output voltage (V_{ao})
	S_{11}	S_{12}	S_{13}	S_{14}	
P	ON	ON	OFF	OFF	$+V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

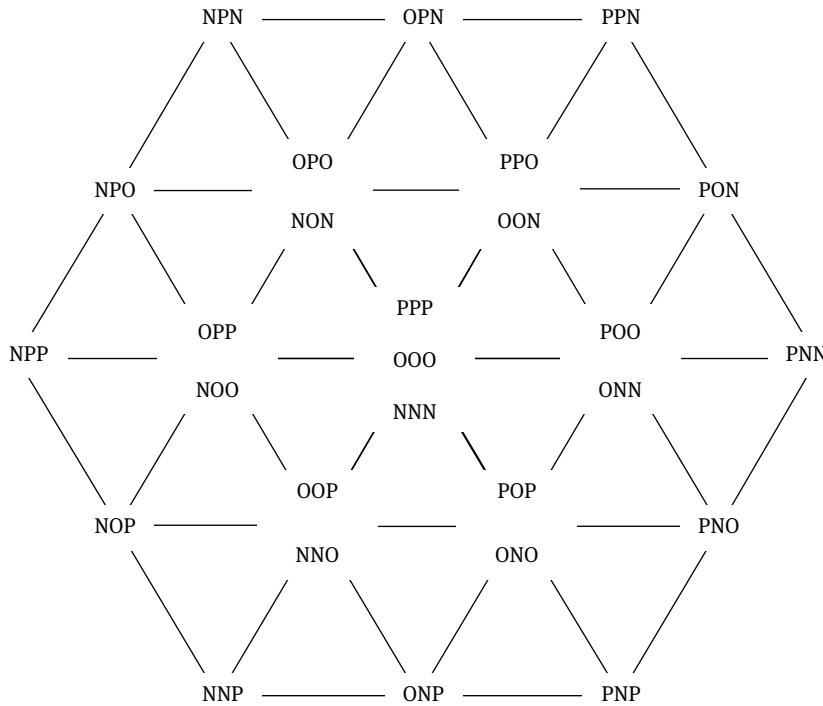


Fig. 4.2: Space vector diagram of the three-level inverter.

4.1.2 Voltage vectors and calculation of switching times

Figure 4.3 shows the triangle formed by the voltage vectors V_0 , V_2 , and V_5 . This triangle is divided into four small triangles 1, 2, 3, and 4. In the space voltage vector PWM, generally, output voltage vector is formed by its nearest three vectors to minimize the harmonic components of the output voltage and the current. The duration of each vector can be calculated by vector calculation. For instance, if the reference voltage vector falls into triangle 3, the duration of each voltage vector can be calculated by the following equations:

$$V_1 T_a + V_3 T_b + V_4 T_c = V^* T_S \quad (4.1)$$

$$T_a + T_b + T_c = T_S \quad (4.2)$$

$$V_1 = \frac{1}{2}V; \quad V_3 = \frac{\sqrt{3}}{2}Ve^{j\frac{\pi}{6}}; \quad V_4 = \frac{1}{2}Ve^{j\frac{\pi}{3}}; \quad V^* = Ve^{j\theta} \quad (4.3)$$

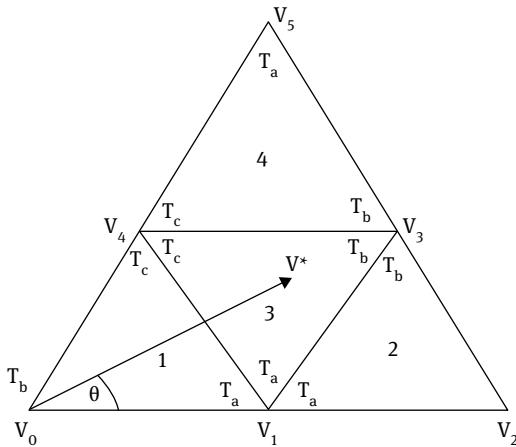


Fig. 4.3: Voltage vectors of the three-level inverter in sector I.

Substituting Eq. (4.3) in Eq. (4.1) and changing into trigonometric form

$$\frac{1}{2}V \cdot T_a + \frac{\sqrt{3}}{2}V \cdot \left(\cos \frac{\pi}{6} + j \sin \frac{\pi}{6} \right) \cdot T_b + \frac{1}{2}V \left(\cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) \cdot T_c = V(\cos \theta + j \sin \theta) \cdot T_s. \quad (4.4)$$

Separating the real and imaginary parts from Eq. (4.4),

$$\frac{1}{2} \cdot T_a + \frac{\sqrt{3}}{2} \left(\cos \frac{\pi}{6} \right) \cdot T_b + \frac{1}{2} \left(\cos \frac{\pi}{3} \right) \cdot T_c = V(\cos \theta) \cdot T_s \quad (4.5)$$

$$\frac{\sqrt{3}}{2} \left(\sin \frac{\pi}{6} \right) \cdot T_b + \frac{1}{2} \left(\sin \frac{\pi}{3} \right) \cdot T_c = V(\sin \theta) \cdot T_s. \quad (4.6)$$

By solving Eq. (4.2), Eq. (4.5), and Eq. (4.6), the values of T_a , T_b , and T_c are

$$T_a = T_s[1 - 2k\sin(\theta)] \quad (4.7)$$

$$T_b = T_s[2k\sin(\theta + 60) - 1] \quad (4.8)$$

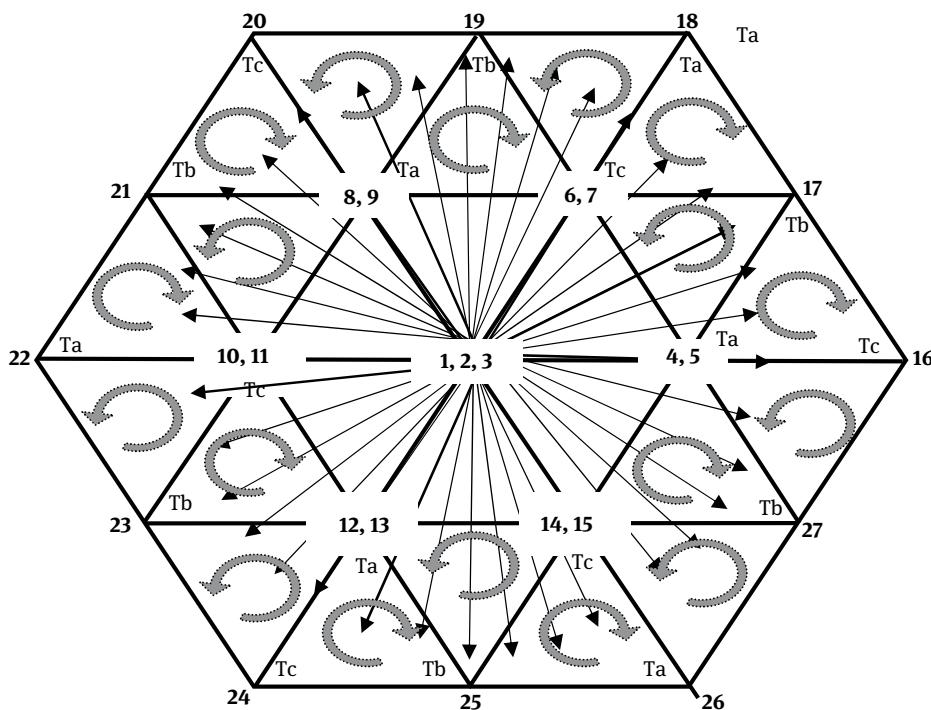
$$T_c = T_s[2k\sin(\theta - 60) + 1], \quad (4.9)$$

$$\text{Where } k = \frac{2}{\sqrt{3}}V \cdot$$

In other regions (1, 2, 4), the duration for each voltage vector can be calculated in the same way. Table 4.2 shows the switching times of voltage vector in sector I. The switching pattern of the three-level inverter is shown in Fig. 4.4 and corresponding switching states are shown in Tab. 4.3.

Tab. 4.2: Switching times of the three-level inverter.

Region	T_a	T_b	T_c
1	$2kT_s \sin(60 - \theta)$	$T_s[1 - 2k\sin(\theta + 60)]$	$2kT_s \sin(60 - \theta)$
2	$2T_s[1 - k\sin(\theta + 60)]$	$2kT_s \sin\theta$	$T_s[2k\sin(60 - \theta) - 1]$
3	$T_s[1 - 2k\sin\theta]$	$T_s[2k\sin(\theta + 60) - 1]$	$T_s[2k\sin(\theta - 60) + 1]$
4	$T_s[2k\sin\theta - 1]$	$2kT_s \sin(60 - \theta)$	$2T_s[1 - k\sin(\theta + 60)]$

4.1.3 Optimized switching sequence**Fig. 4.4:** Switching pattern of the three-level inverter.**Tab. 4.3:** Switching states of the three-level inverter.

Section	Samples	States	Switching states
1.2	1	5-17-16-4	POO-PON-PNN-ONN
	2	4-16-17-5	ONN-PNN-PON-POO
	3	5-17-16-4	POO-PON-PNN-ONN
1.3	4	4-7-17-5	ONN-OON-PON-POO

Tab. 4.3 (continued)

Section	Samples	States	Switching states
1.4	5	6-18-17-7	PPO-PPN-PON-OON
	6	7-17-18-6	OON-PON-PPN-PPO
	7	6-18-17-7	PPO-PPN-PON-OON
	8	7-17-18-6	OON-PON-PPN-PPO
2.2	9	6-18-19-7	PPO-PPN-OPN-OON
	10	7-19-18-6	OON-OPN-PPN-PPO
	11	6-18-19-7	PPO-PPN-OPN-OON
2.3	12	9-19-7-8	OPO-OPN-OON-NON
2.4	13	9-19-20-8	OPO-OPN-NPN-NON
	14	8-20-19-9	NON-NPN-OPN-OPO
	15	9-19-20-8	OPO-OPN-NPN-NON
	16	8-20-19-9	NON-NPN-OPN-OPO
3.2	17	9-21-20-8	OPO-NPO-NPN-NON
	18	8-20-21-9	NON-NPN-NPO-OPO
	19	9-21-20-8	OPO-NPO-NPN-NON
3.3	20	11-8-21-10	NOO-NON-NPO-OPP
3.4	21	5-17-16-4	OPP-NPP-NPO-NOO
	22	4-16-17-5	NOO-NPO-NPP-OPP
	23	5-17-16-4	OPP-NPP-NPO-NOO
	24	4-16-17-5	NOO-NPO-NPP-OPP
4.2	25	10-22-23-11	OPP-NPP-NOP-NOO
	26	11-23-22-10	NOO-NOP-NNP-OPP
	27	10-22-23-11	OPP-NPP-NOP-NOO
4.3	28	12-23-11-13	OPP-NOP-NOO-NNO
4.4	29	12-23-24-13	OPP-NOP-NNP-NNO
	30	13-24-23-12	NNO-NNP-NOP-OPP
	31	12-23-24-13	OPP-NOP-NNP-NNO
	32	13-24-23-12	NNO-NNP-NOP-OPP
5.2	33	12-25-24-13	OOP-ONP-NNP-NNO
	34	13-24-25-12	NNO-NNP-ONP-OOP
	35	12-25-24-13	OOP-ONP-NNP-NNO
5.3	36	12-25-15-13	OOP-ONP-ONO-NNO
5.4	37	14-26-25-15	POP-PNP-ONP-ONO
	38	15-25-26-14	ONO-ONP-PNP-POP
	39	14-26-25-15	POP-PNP-ONP-ONO
	40	15-25-26-14	ONO-ONP-PNP-POP
6.2	41	14-26-27-15	POP-PNP-PNO-ONO
	42	15-27-26-14	ONO-PNO-PNP-POP
	43	14-26-27-15	POP-PNP-PNO-ONO
6.3	44	5-27-15-4	POO-PNO-ONO-ONN
6.4	45	5-27-16-4	POO-PNO-NPO-NOO
	46	4-16-27-5	NOO-NPO-PNO-POO
	47	5-27-16-4	POO-PNO-NPO-NOO
	48	4-16-27-5	NOO-NPO-PNO-POO

4.2 Results and discussions

To verify the proposed SVPWM algorithm, simulation studies have been carried out for the two- and three-level inverter fed induction motor. The simulation parameters of induction motor used in this method are given in Appendix I. The simulation results for the two-level inverter are shown in Figs. 4.5 to 4.11. The gate currents and pole voltages of the two-level inverter are shown in Figs. 4.5 and 4.6, respectively. The phase voltage and line voltages of the two-level inverter are shown in Figs. 4.7 and 4.8, respectively. The d-axis and q-axis stator currents of the two-level inverter fed induction motor are shown in Fig. 4.9. The torque, speed, and flux of the two-level inverter fed induction motor are shown in Fig. 4.10 for a load torque (T_L) of 10.32 N-m. The harmonic spectrum of the inverter output voltage and total harmonic distortion (THD) are shown in Fig. 4.11.

For the same conditions, Figs. 4.12 to 4.18 give the results for the three-level inverter fed induction motor. Figures 4.12 and 4.13 show the gate currents and pole voltages, respectively, of the three-level inverter. The phase voltages and line voltages of the three-level inverter are shown in Figs. 4.14 and 4.15, respectively. The d- and q-axes stator currents of the three-level inverter fed induction motor are shown in Fig. 4.16.

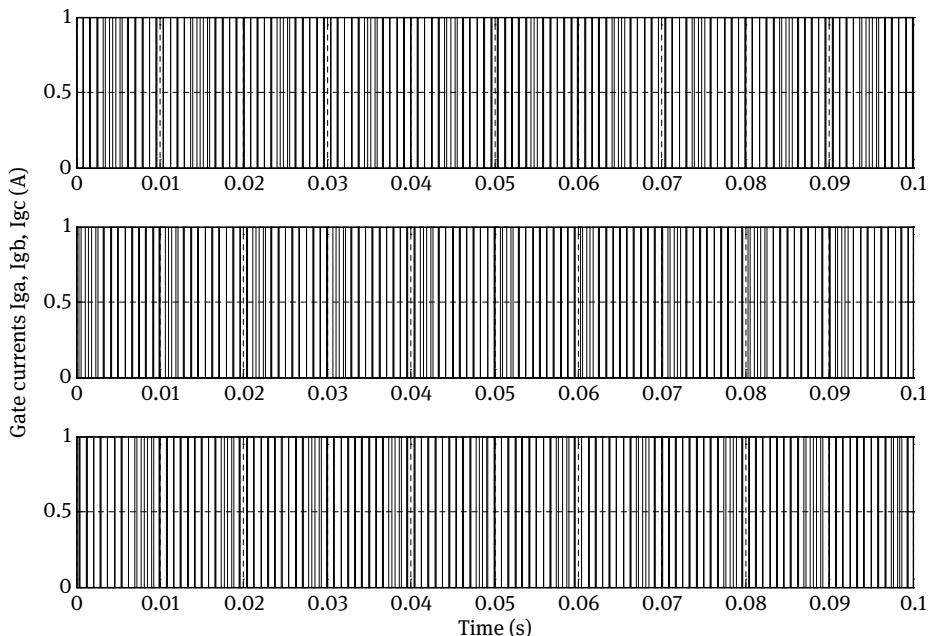


Fig. 4.5: Gate currents of the two-level inverter.

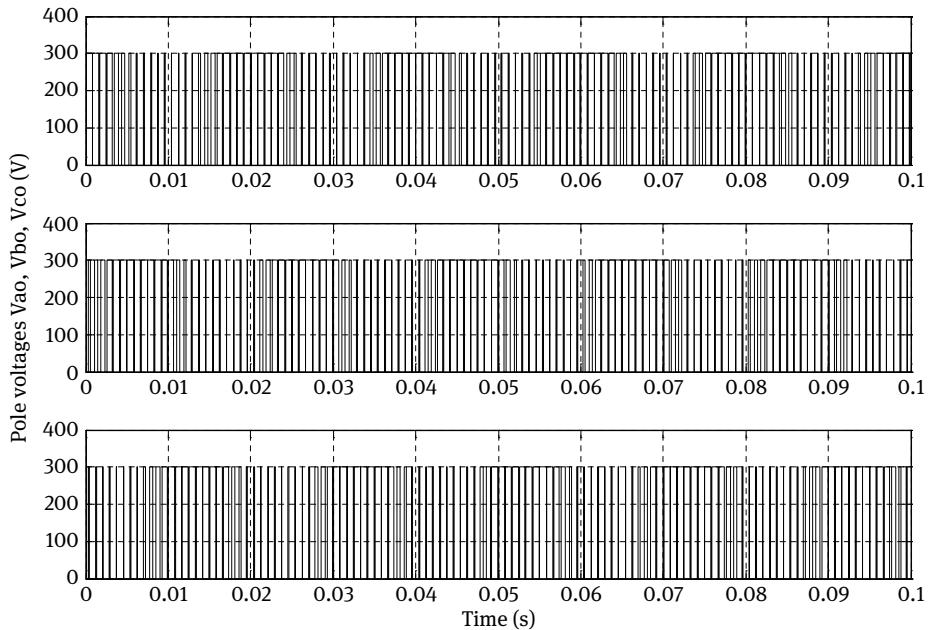


Fig. 4.6: Pole voltages of the two-level inverter.

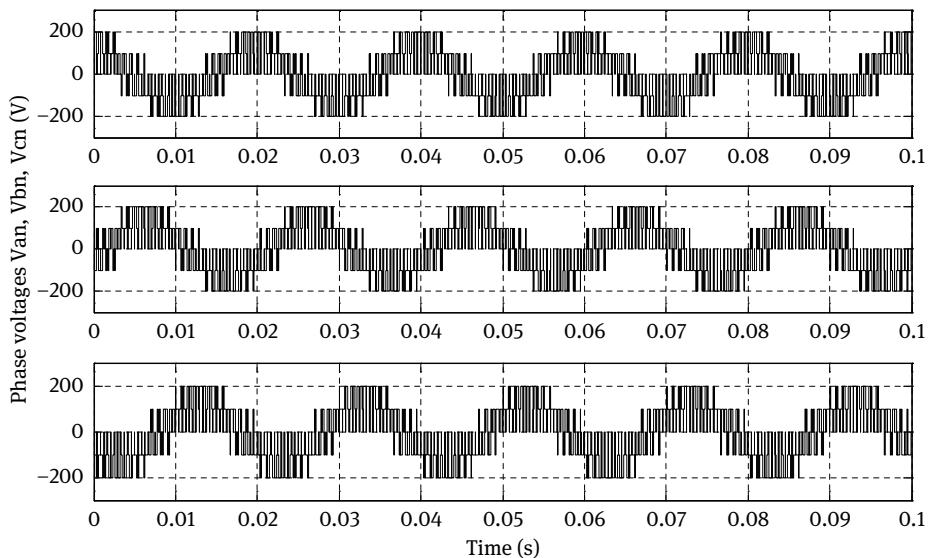


Fig. 4.7: Phase voltages of the two-level inverter.

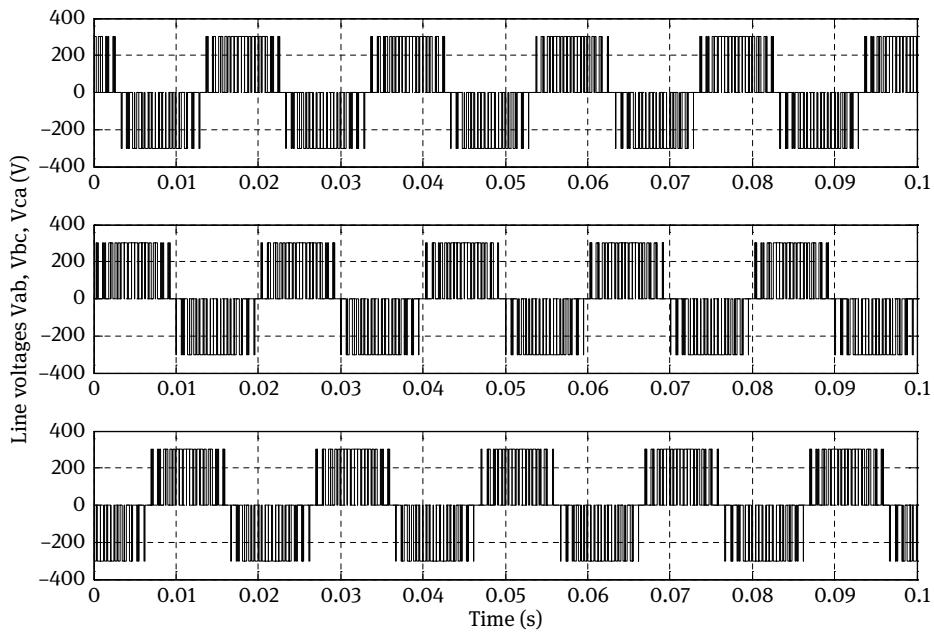


Fig. 4.8: Line-to-line voltages of the two-level inverter.

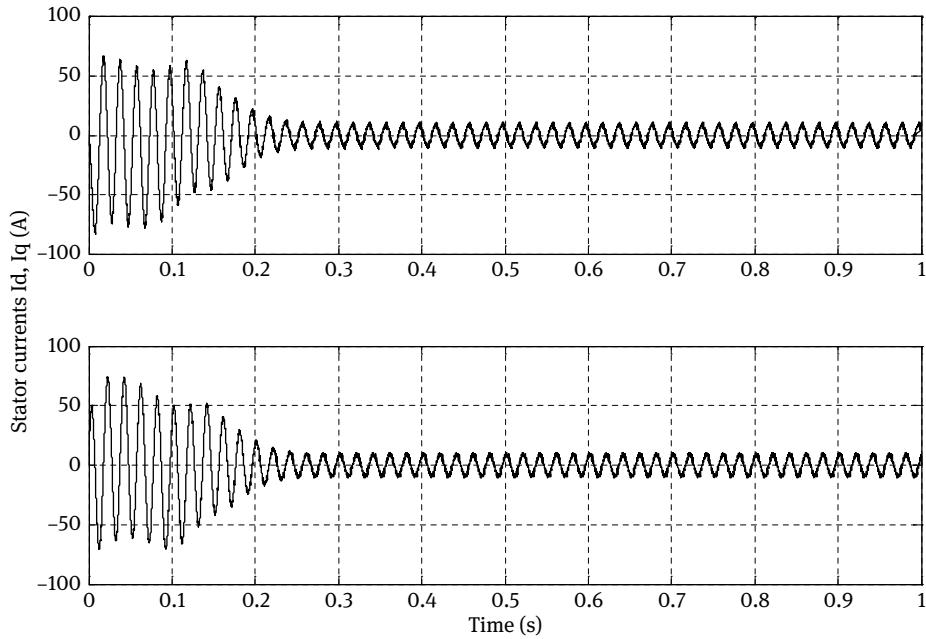


Fig. 4.9: Stator currents of the two-level inverter fed induction motor.

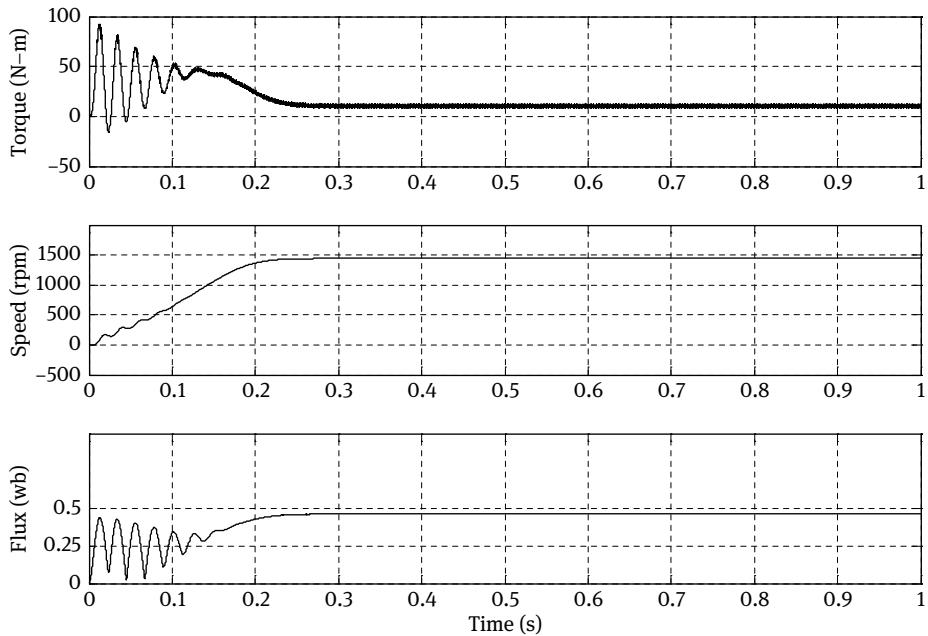


Fig. 4.10: Torque, speed, and flux responses of the two-level inverter fed induction motor for load torque (T_L) of 10.32 N·m.

The torque, speed, and flux of the three-level inverter fed induction motor are shown in Fig. 4.17 for a load torque (T_L) of 10.32 N·m. The harmonic spectrum of the inverter output voltage and the THD are shown in Fig. 4.18. Tables 4.4 and 4.5 show the comparison between two- and three-level inverter performances. The interpretation of all the results shows that in case of the three-level inverter, the output voltage, speed, and torque response considerably improves and that the torque ripples and the THD reduce.

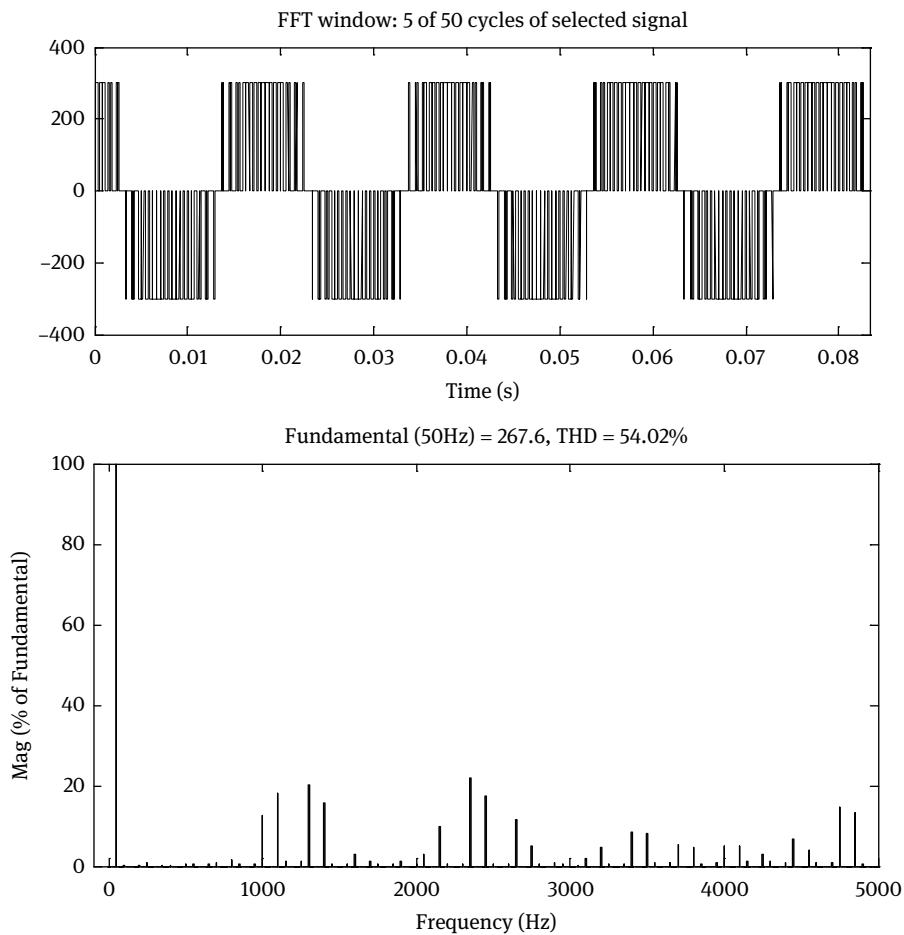


Fig. 4.11: Output line voltage (and its harmonic spectrum) of the two-level inverter.

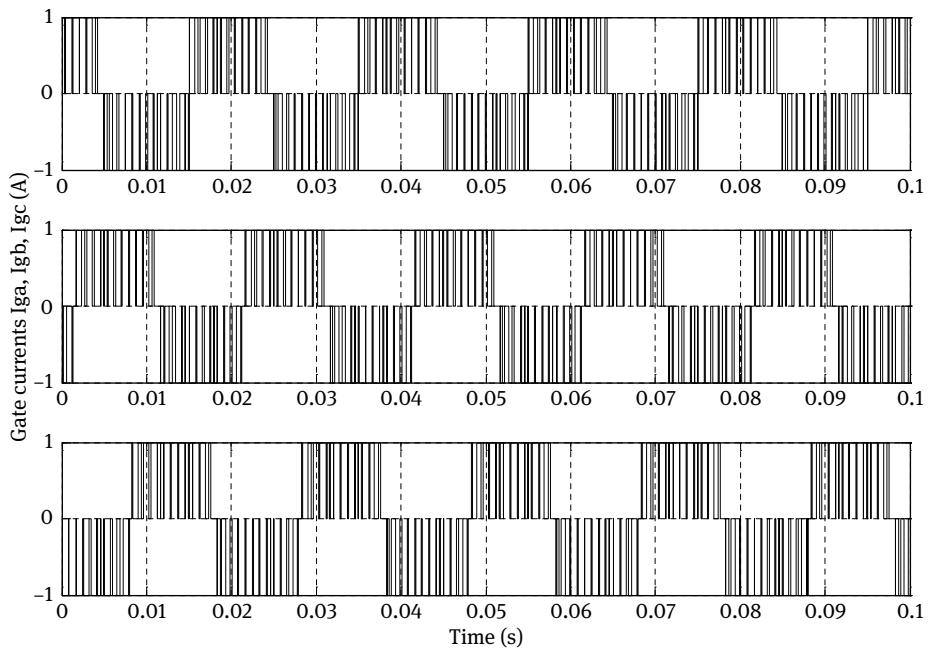


Fig. 4.12: Gate currents of the three-level inverter.

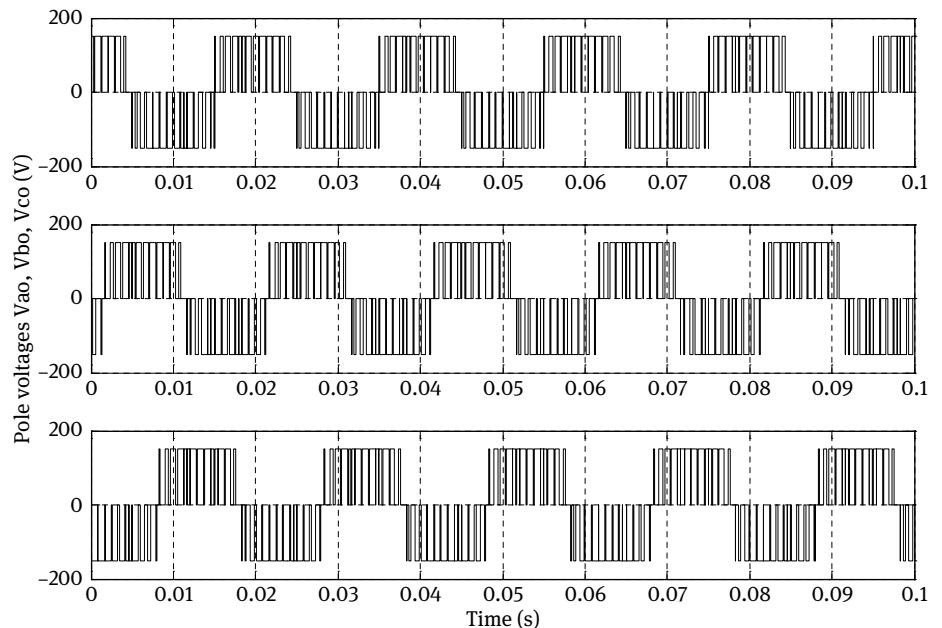


Fig. 4.13: Pole voltages of the three-level inverter.

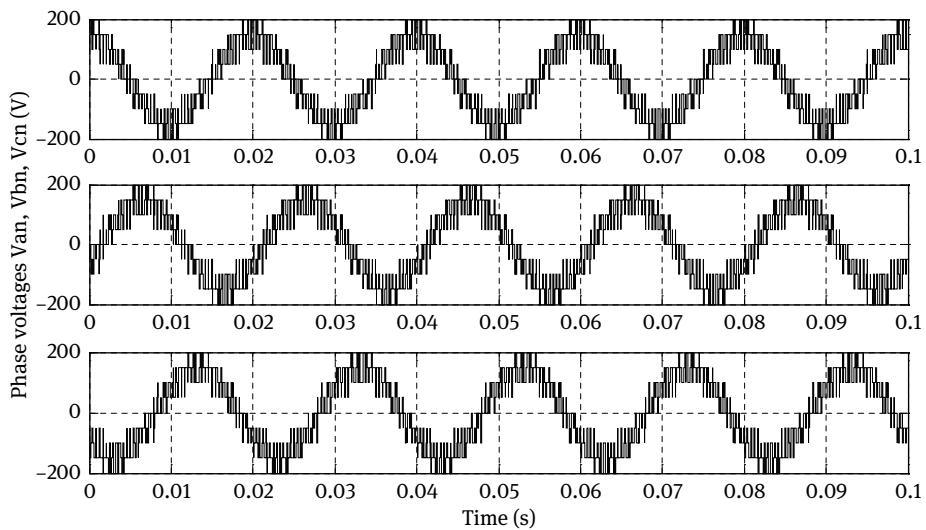


Fig. 4.14: Phase voltages of the three-level inverter.

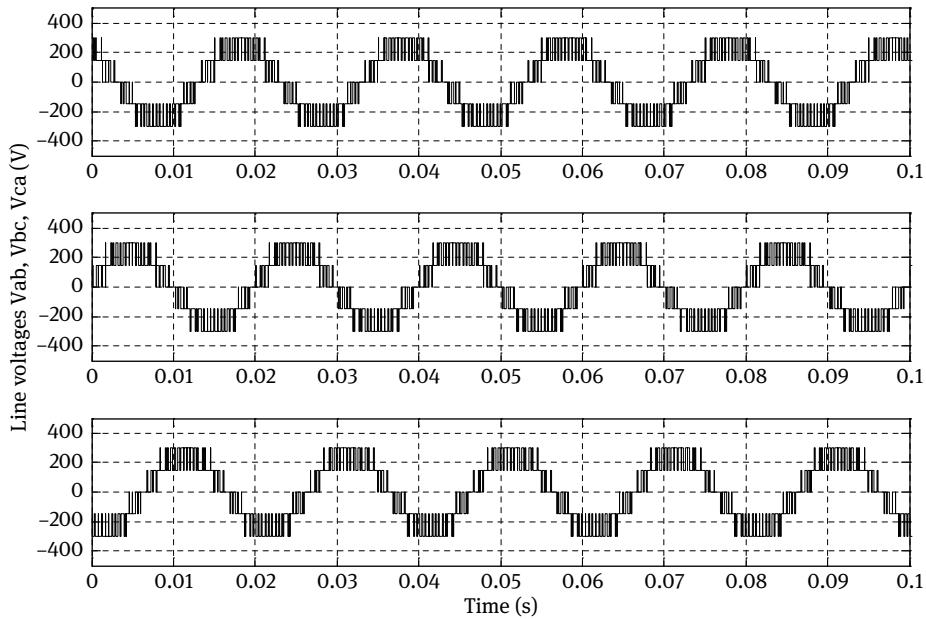


Fig. 4.15: Line-to-line voltages of the three-level inverter.

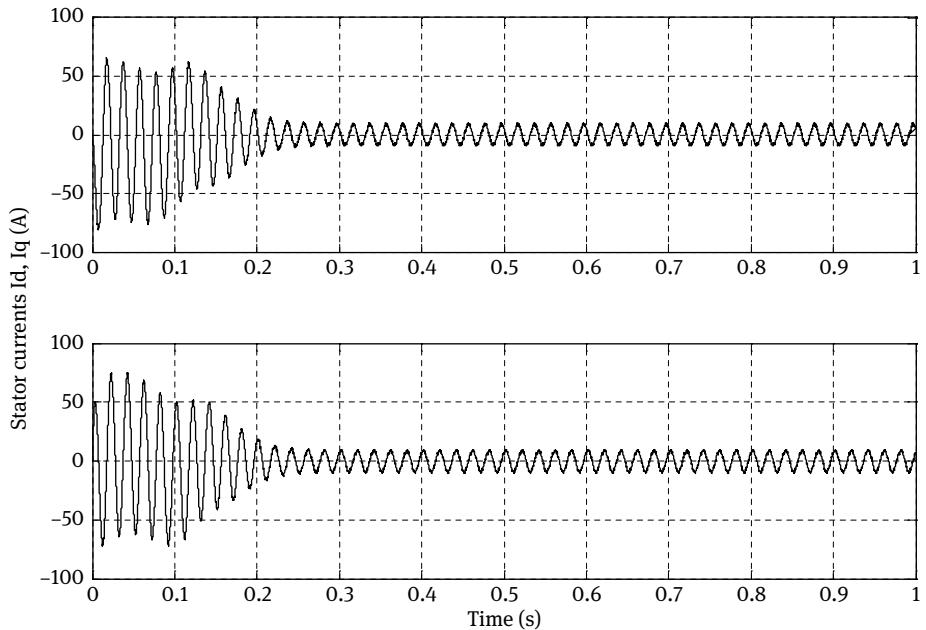


Fig. 4.16: Stator currents of the three-level inverter fed induction motor.

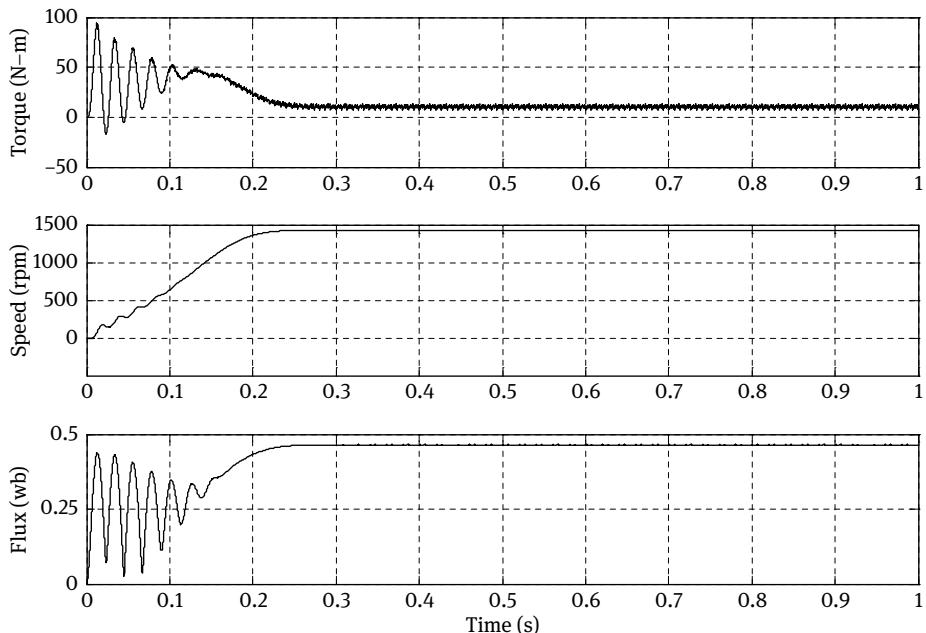


Fig. 4.17: Torque, speed, and flux responses of the three-level inverter fed induction motor for load torque (TL) of 10.32 N-m.

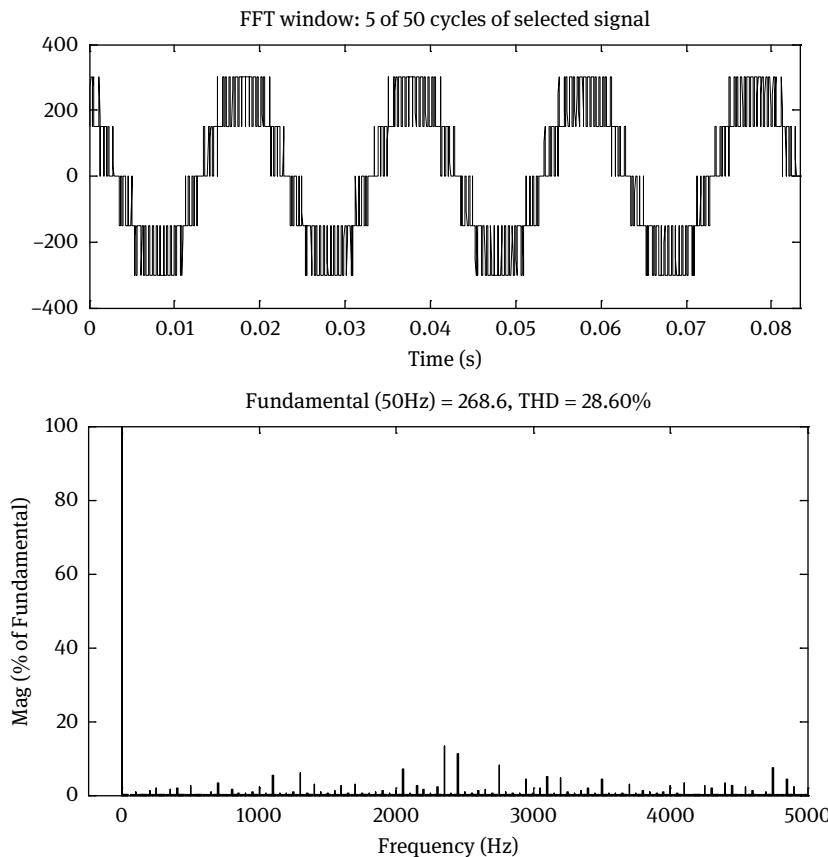


Fig. 4.18: Output line voltage (and its harmonic spectrum) of the three-level inverter.

From simulation results, the performance of the two- and three-level inverters has been analyzed. It shows that the three-level inverter is more effective than the two-level inverter in terms of rotor speed of the induction motor and the THD (Tab. 4.4). Table 4.5 shows that as the modulation index increases, the THD decreases.

Tab. 4.4: Performance of the two- and three-level inverters.

Parameters	Two-Level inverter	Three-Level inverter
Input dc voltage (V)	300	300
Speed (rpm)	1442	1443
THD (%)	54.02	28.60
Peak value of fundamental harmonic (V)	267.6	268.6
Switching frequency (Hz)	2400	2400

Tab. 4.5: Performance of inverters with respect to modulation index.

Modulation index (m)	Two-Level voltage source inverter		Three-Level voltage source inverter		
	Fundamental peak voltage (V)	THD%	Fundamental peak voltage (V)	THD%	
0.7	236.3	73.47	237	33.88	
0.75	251.9	67.09	253.7	31.34	
0.8	267.6	54.02	268.6	28.60	
0.86	269	51.52	270.7	26.51	

4.3 Conclusions

In the field of high-power, high-performance applications, multilevel inverters seem to be the most promising alternative. In this chapter, the application of SVPWM control strategy on three-level inverter has been proposed and analyzed. The proposed SVPWM algorithm provides high-safety voltages with less harmonic components compared to two-level structures and reduces the switching losses by limiting the switching to two thirds of the pulse duty cycle. On the one hand, the latter aimed to prove the effectiveness of SVPWM in the contribution of switching power losses reduction and to show the advantage of the three-level inverter that carry out voltages with contents of less harmonic injection than the two-level inverter. On the other hand, the simulation results show that as modulation index increases, the THD decreases and the fundamental RMS value increases linearly. In the first proposed method, the obtained THD for the two- and three-level inverters are 54.02% and 28.60%, respectively.

5 Space vector pulse width modulation for multilevel inverters using fractal approach

In this chapter, the space vector pulse width modulation (SVPWM) for multilevel inverters using fractal approach has been proposed and implemented for three- and five-level inverters. This method is mainly based on the fact that the switching vector representation of any multilevel inverter has an inherent fractal structure, which is the basic unit of this structure, being a triangle made of the vertices of three adjacent inverter voltage space vectors. The proposed method uses simple arithmetic for determining the sector and does not require look-up tables; hence, the fractal approach is applied for multilevel inverters using SVPWM. The results have been presented and analyzed. The complexity and feasibility of this algorithm have been discussed.

The space vector representation of a higher-level inverter can be conceived as generated from the space vector representation of the two-level inverter, wherein the sectors of the two-level inverter get progressively divided and subdivided. The basic structure, a triangle (sector), is transformed by further dividing itself into smaller triangles. A basic structure that evolves by dividing itself into structures similar to it has an associated fractal. The switching voltage space vector representation of multilevel inverters also has an associated fractal. In fractal theory, the basic triangle is divided into four smaller triangular regions, joined by the midpoints of the sides of the triangle [101].

5.1 Inherent fractal structure of multilevel inverter

The voltage space vectors of the two-level inverter are shown in Fig. 5.1. The voltage space vector locations for a three-level inverter are shown in Fig. 5.2, where A_{00} , A_{01} , A_{02} , A_{03} , A_{04} , A_{05} , and A_{06} are same as the locations of the voltage space vectors of the two-level inverter. Consider the region marked 1 in the case of the two-level inverter, formed by the vectors located at A_{00} , A_{01} , and A_{02} . In the case of the three-level inverter, this region has three additional voltage space vectors, as shown in Fig. 5.2.

It can be observed that the three additional voltage space vectors are located at the midpoints of each side of the sector of equivalent two-level inverter. The three additional switching voltage space vectors together with switching voltage space vectors located at A_{00} , A_{01} , and A_{02} results in four sectors within (sector 1) A_{00} , A_{01} , A_{02} of the three-level inverter. Considering the triangular region formed by the space vectors

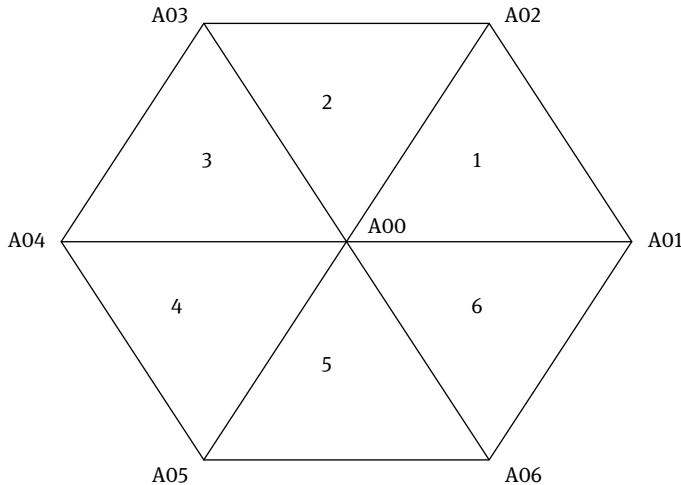


Fig. 5.1: Voltage space vectors of the two-level inverter.

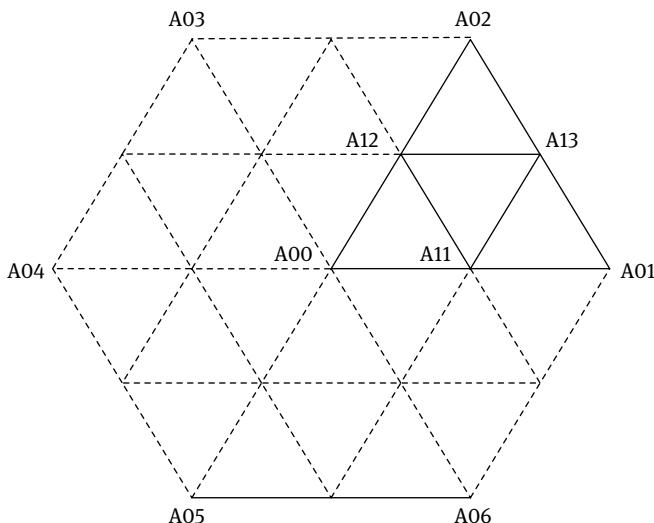


Fig. 5.2: Voltage space vectors of the three-level inverter.

located at A_{00} , A_{01} , and A_{02} , besides the voltage space vectors of the three-level inverter, nine additional voltage space vectors are present, as shown in Fig. 5.3. The nine additional vectors are located at A_{21} , A_{22} , A_{23} , A_{24} , A_{25} , A_{26} , A_{27} , A_{28} , and A_{29} . It can be clearly observed that the nine additional vectors are located at the midpoints of the sides of sectors of the three-level inverter. The nine additional vectors together with the voltage space vectors of the three-level inverter results in 16 sectors within

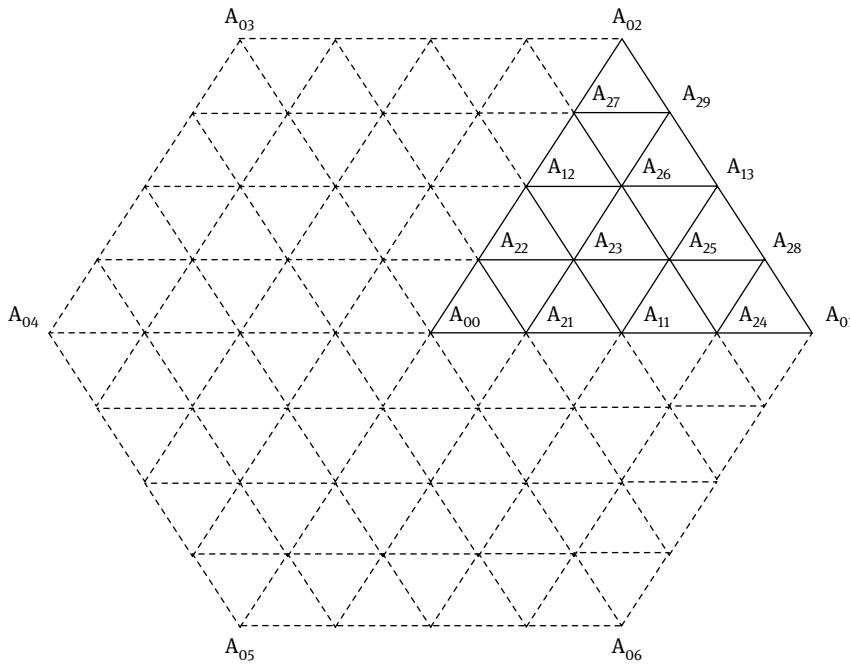


Fig. 5.3: Voltage space vectors of the five-level inverter by inherent fractal structure.

(sector I) $\Delta A_{00}A_{01}A_{02}$ of the five-level inverter. In this manner each sector in the voltage space vector representation of an equivalent two-level inverter is divided into four smaller sectors, resulting in voltage space vector locations of the three-level inverter. Each of the sectors of the three-level inverter is further divided into four smaller sectors resulting in switching space vectors of the five-level inverter. This process gets repeated for generation of space vectors of higher-level inverters.

5.2 SVPWM algorithm using the fractal approach

This algorithm explains the procedure to adopt the SVPWM for multilevel inverters using the fractal approach.

- i. Three-phase (a, b, c) to two-phase (d, q) transformation.
- ii. Identify the sector where the tip of the reference vector is located.
- iii. Determine the three nearest voltage vectors.
- iv. Perform the triangularization algorithm.
- v. Calculate and compare the centroids of each triangle with the reference vector.
- vi. For the higher-level implementation of the fractal approach, perform the triangularization algorithm until the reference vector is nearer to the centroids of respective triangle where the triangularization is to be performed using Eqs. (5.12) to (5.14).

- vii. Switching states are obtained using Eqs. (5.15) to (5.17).
- viii. Switching time durations are calculated, taking the basic two-level timings into consideration.
- ix. Optimized switching sequence is calculated by (a) taking the virtual zero vectors, (b) eliminating the redundant switching states, and (c) considering optimum switching where only one switching is involved as the inverter changes from one state to another.

5.2.1 Three-phase (a, b, c) to two-phase (d, q) transformation

The three phase quantities can be transformed to their equivalent two phase quantities either in synchronously rotating frame or stationary frame. From this two-phase component the reference vector magnitude can be found and used for modulating the inverter output.

The three phase sinusoidal voltage components are

$$\begin{aligned} V_a &= V_m \sin \omega t \\ V_b &= V_m \sin \left(\omega t - \frac{2\pi}{3} \right) \\ V_c &= V_m \sin \left(\omega t + \frac{2\pi}{3} \right) \end{aligned} \quad (5.10)$$

The magnitude and angle of the rotating vector can be found by means of Clark's transformation. Then, the (d, q) coordinates of the corresponding space vector can be obtained as

$$\begin{aligned} V_d &= \frac{3}{2} (V_a) \\ V_q &= \frac{3}{2} (V_b - V_c). \end{aligned} \quad (5.11)$$

5.2.2 Location of the reference voltage vector

The identification of sector where the tip of the reference vector lies can be done using coordinate transformation of the reference vector into a two dimensional coordinate system. The sector can also be determined by resolving the reference phase vector along a, b and c axes and by repeated comparison with discrete phase voltages.

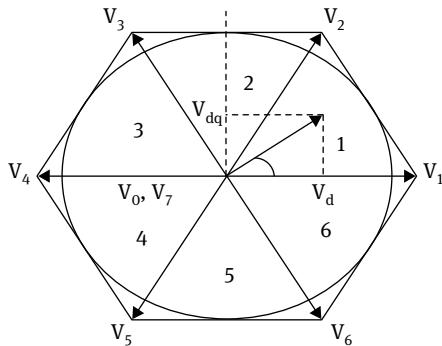


Fig. 5.4: Location of the reference vector in the two-level inverter.

After identifying the sector, the voltage vectors at the vertices of the sector are to be determined. This can be done by the comparison of reference angle with sector angle; Fig. 5.4 depicts SVPWM with six sectors in (d, q) reference frame with α as the reference angle.

If the reference angle

$0^\circ < \alpha < 60^\circ$, reference vector is in sector 1

$60^\circ < \alpha < 120^\circ$, reference vector is in sector 2

$120^\circ < \alpha < 180^\circ$ reference vector is in sector 3

$180^\circ < \alpha < 240^\circ$ reference vector is in sector 4

$240^\circ < \alpha < 300^\circ$ reference vector is in sector 5

$300^\circ < \alpha < 360^\circ$ reference vector is in sector 6

The location of tip of reference frame passing through different layers can be found in Fig. 5.5. If the reference vector is in layer 1, it represents the two-level inverter operation and the reference vector in layer 2 represents the three-level inverter, the reference vector in layer 3 represents the four-level inverter, and the reference vector in layer 4 represents the five-level inverter.

After identifying the sector, the voltage vectors at the vertices of the sector are to be determined. The nearest three voltage vectors of the reference vector are the vertices of the sector.

5.2.3 Determination of nearest three voltage vectors

The space vector voltage is located in a hexagon surrounded by different states of the inverter that gives different voltage magnitudes of the output voltage. These inverter

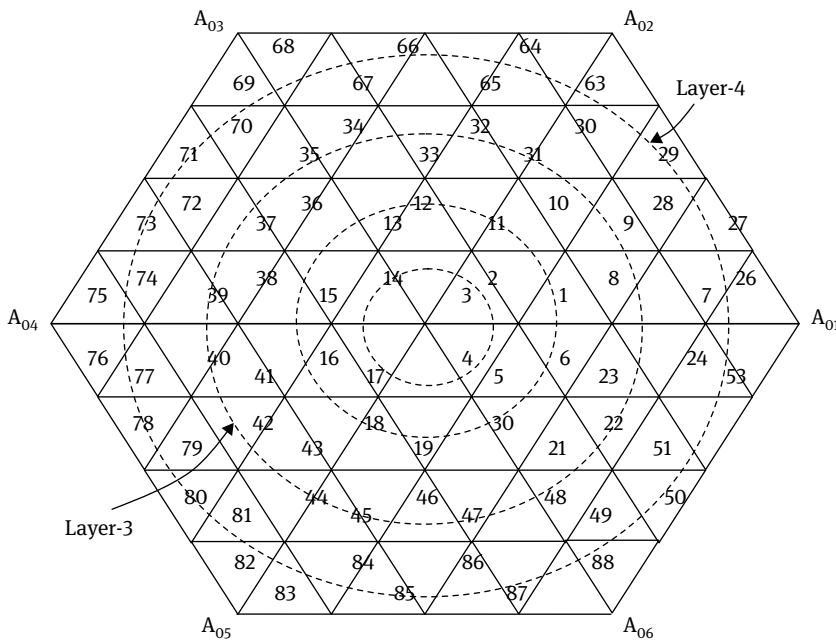


Fig. 5.5: Locus of the tip of the reference vector passing through different layers of the five-level inverter.

states are nothing but the ON/OFF states of the devices. After identifying the sector where the tip of the reference vector is located, the voltage vectors of this sector are determined to find out the three nearest voltage vectors of space vector voltage V_{sr} . To obtain these three nearest voltage vectors, the region where the space vector voltage lies should be determined.

If the reference vector lies in sector 1, the three nearest vectors are determined by the comparison of the reference angle. If reference angle $\alpha < 60^\circ$, it lies in the first sector, and hence, three nearest voltage vectors are V_0 , V_1 , and V_2 . For example, if the reference angle lies in sector 4, the nearest three vectors are V_0 , V_4 , V_5 or V_4 , V_5 , V_7 .

5.2.4 Triangularization algorithm

As explained earlier, due to the inherent fractal structure associated with multilevel inverter, the voltage space vector representation of the two-level inverter grows to that of higher-level inverters by repeated division of each sector. At every stage, the triangular region is divided into four smaller triangular regions, due to the presence of the additional voltage vectors as shown in Fig. 5.6. The three additional voltage vectors

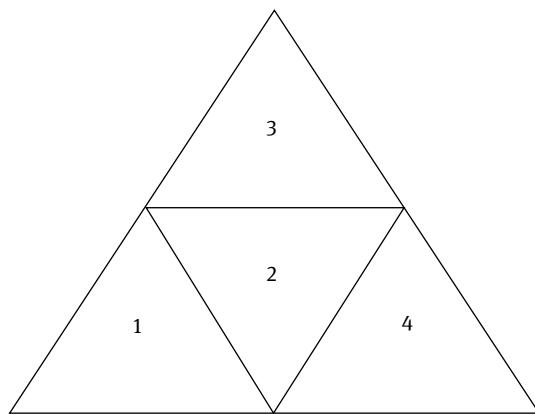


Fig. 5.6: Triangularization of the two-level inverter in sector I.

are located at the midpoint of each side of sector. The sectors of higher-level inverter can therefore be generated by such repeated triangularization.

- The following steps are involved to perform the triangularization
- Determine the sector where the triangularization is to be performed.
 - Determine the midpoints of each side of the sector using Eqs. (5.12) to (5.14). These are the coordinates of the three new vectors that will divide the sector into four smaller, but similar, triangular regions.
 - Determine the inverter states corresponding to these vectors using Eqs. (5.15) to (5.17).

For example, consider region I of the two-level inverter formed by vertices A_{00} , A_{01} , and A_{02} . The coordinates of three vertices are $(\alpha_{00}, \beta_{00})$, $(\alpha_{01}, \beta_{01})$, and $(\alpha_{02}, \beta_{02})$, respectively. The coordinates of the three new voltage space vectors located at A_{11} , A_{12} , and A_{13} as shown in Fig. 5.7 can be obtained from the coordinates of A_{00} , A_{01} , and A_{02} .

Coordinates of A_{11} are

$$V_q = \frac{3}{2} (V_b - V_c)$$

$$\beta_{11} = \frac{1}{2}(\beta_{00} + \beta_{01}). \quad (5.12)$$

Coordinates of A_{12} are

$$\alpha_{12} = \frac{1}{2}(\alpha_{00} + \alpha_{02})$$

$$\beta_{12} = \frac{1}{2}(\beta_{00} + \beta_{02}). \quad (5.13)$$

Coordinates of A_{13} are

$$\alpha_{13} = \frac{1}{2}(\alpha_{01} + \alpha_{02})$$

$$\beta_{13} = \frac{1}{2}(\beta_{01} + \beta_{02}). \quad (5.14)$$

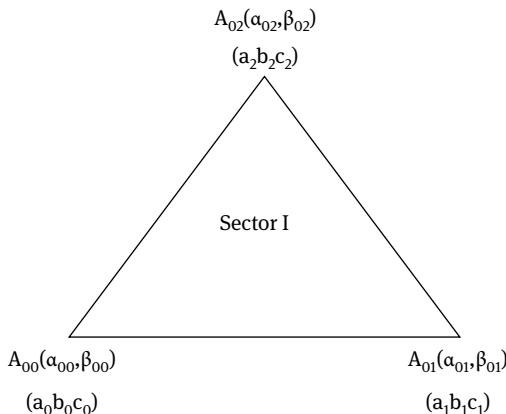


Fig. 5.7: Sector I of the two-level inverter.

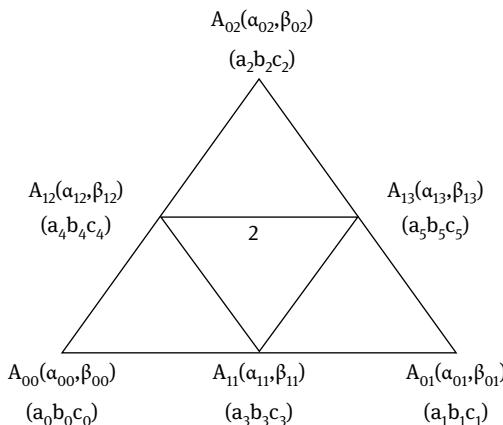


Fig. 5.8: First triangulation of the two-level inverter.

The associated switching vector states can also be determined in a similar manner. The inverter switching states corresponding to the voltage space vector located at A_{00} , A_{01} , and A_{02} are $(a_0 b_0 c_0)$, $(a_1 b_1 c_1)$, and $(a_2 b_2 c_2)$, respectively. The switching states of the new voltage space vectors as shown in Fig. 5.8 at A_{11} ($a_3 b_3 c_3$), A_{12} ($a_4 b_4 c_4$), and A_{13} ($a_5 b_5 c_5$) can be obtained as

$$X_3 = \frac{1}{2}(X_0 + X_1) \quad (5.15)$$

$$X_4 = \frac{1}{2}(X_0 + X_2) \quad (5.16)$$

$$X_5 = \frac{1}{2}(X_2 + X_1) \quad (5.17)$$

where X takes a , b , and c for the respective phases.

Eqs. (5.12) to (5.14) represent the arithmetic procedure used in the proposed method for dividing a triangular region (sector) into four similar regions by generating three additional vectors situated at the midpoints of the sides forming the original triangular region. This is referred as the triangularization algorithm. To generate sectors of higher-level inverter by progressively dividing sectors of the two-level inverter, the triangularization algorithm is repeatedly applied. In fractal theory, algorithms whose repeated iterations will result in the pattern to grow or evolve are referred as iterated function system, the repeated iteration of triangularization algorithm will grow the inherent fractal structure in space vector representation of multilevel inverters. Therefore, the triangularization algorithm can be viewed as the iterated function system for this fractal structure.

5.2.5 Comparison of the reference vector with the centroid

The location of the tip of the reference voltage space vector from among these four triangular regions is found by determining the region whose centroid is closest to the tip of the reference space vector. The coordinates of the centroid of an equilateral triangle can be determined as the average of coordinates of the three vertices. For an equilateral triangle with the coordinates of the vertices as (α_1, β_1) , (α_2, β_2) , (α_3, β_3) , the coordinates of the centroid $(\alpha_{\text{cent}}, \beta_{\text{cent}})$ is given by

$$\begin{aligned} \alpha_{\text{cent}} &= \frac{1}{3}(\alpha_1 + \alpha_2 + \alpha_3) \\ \beta_{\text{cent}} &= \frac{1}{3}(\beta_1 + \beta_2 + \beta_3). \end{aligned} \quad (5.18)$$

The triangle with the centroid closest to the tip of the reference space vector is $\Delta A_{11}A_{12}A_{13}$. The triangularization algorithm has to be applied again in case of the five-level inverter. The application of Eqs. (5.12) to (5.14) to $\Delta A_{11}A_{12}A_{13}$ will generate further three new voltage space vectors A_{23} , A_{25} , A_{26} and also the inverter states corresponding to these new voltage vectors. Thus, the three-level inverter space vector diagram is further divided into four smaller triangles for a five-level inverter space vector diagram, as shown in Fig. 5.9.

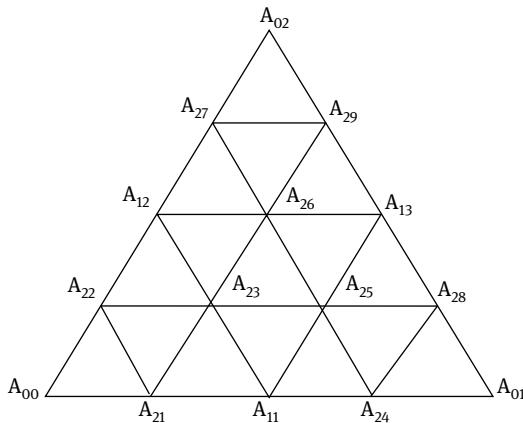


Fig. 5.9: Triangularization of sector I of equivalent three-level inverter.

From these four triangles, one triangle enclosing the reference space vector is chosen such that its centroid is closest to the tip of the reference space vector. The sector is identified and the inverter states corresponding to the switching vectors located at the vertices of the identified sector are also generated simultaneously.

5.2.6 Calculation of switching times

The switching time durations are calculated, taking the basic two-level timings into consideration, as these can be extended to the N-level. The switching voltage vectors approximate the volt-second of the reference space vector by operating for specific durations. The determination of duration of operation of the switching voltage space vectors is simplified by mapping the sector that is identified to enclose the reference space vector to a sector of the two-level inverter.

The switching time durations of the vectors can be determined using the following formulae from Eqs. (5.19) to (5.22).

$$T_1 = \frac{(m \times \sin(60 - \alpha))}{\sin(60)} \quad (5.19)$$

$$T_2 = \frac{(m \times \sin(60))}{\sin(60)} \quad (5.20)$$

$$T_0 = T_5 - T_1 - T_2, \quad (5.21)$$

where

$$m = \frac{V_{sr}}{\left(\frac{2}{3}\right)V_{dc}} \quad (5.22)$$

5.2.7 Concept of virtual zero

According to the magnitude of the voltage vectors, they are divided into four groups: zero-voltage vectors (ZVV), small-voltage vectors (SVVs), middle-voltage vectors (MVV), and large-voltage vectors (LVV). Both ZVVs and SVVs have redundant switching states. The mapping is done by choosing one of the three vectors of the identified sector to coincide with the actual zero vectors in the voltage space vector representation of the inverter. In the present work, the vector selected to coincide with the actual zero vector is referred to as the virtual zero vector. The vector with the minimum value for the sum of the magnitudes of the α and β coordinates is chosen to be the virtual zero vector for a particular sector. The sum of the magnitudes of the α and β coordinates represents the total offset of the vector from the actual zero vector. Therefore, in the present work, the virtual zero vectors chosen are at minimum offset from the zero vectors.

5.3 Algorithm implementation for the three-level inverter

This section explains the proposed method for generation of SVPWM for the three-level inverter using the inherent fractal structure associated with the switching space vector representation of multilevel inverter.

5.3.1 Determination of switching vectors

The process of obtaining the reference space vector includes the transformation of (a, b, c) to (d, q) coordinates. Sector identification determines the triangle that encloses the tip of the reference space vector. The vertices of the triangle represent the locations of switching voltage space vectors used to synthesize the reference space vector.

The (d, q) components of the space vector of an N -level inverter can be normalized through division by $V_{dc}/N - 1$, where V_{dc} is the dc-link voltage. In the case of a three-level inverter, the voltage V_{dc} , in the normalized space vector representation is therefore represented by a vector of length 2 as shown in Fig. 5.10.

For a three-level inverter, the switching vectors located at the six vertices of the hexagon forming the periphery are same as the vectors of equivalent two-level inverter, but they have the switching states as (200), (220), (020), (022), (002), (202).

The position of the reference space vector $A_{00}P$ for a three-level inverter is as shown in Fig. 5.11. The first step in the proposed sector identification method is to determine the location of the tip of the reference space vector $A_{00}P$ from among the six regions of the equivalent two-level inverter. This step is implemented by the comparison of the instantaneous reference phase voltages. In this case, the reference

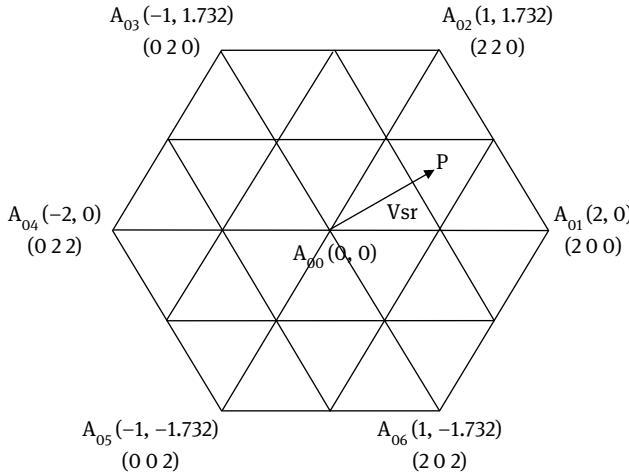


Fig. 5.10: Space vector representation of the three-level inverter.

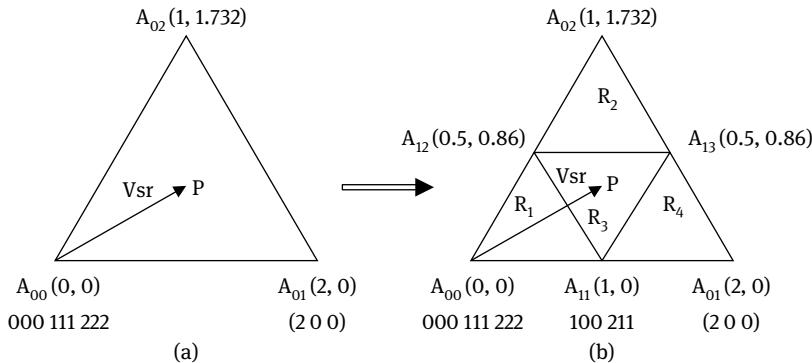


Fig. 5.11: Sector identification and switching vector determination of the three-level inverter.

space vector A_{00P} is located in region I of the equivalent two-level inverter. Region I is formed by the vertices A_{00} , A_{01} , and A_{02} . The coordinates of the vertices are $(0,0)$, $(2,0)$, and $(1,1.732)$, respectively. The switching states corresponding to the vectors located at A_{00} , A_{01} , and A_{02} are also shown in Fig. 5.11(a). The switching states of the vector located at A_{00} , A_{01} , and A_{02} are $(000, 111, 222)$, (200) , and (220) , respectively. The next step is to divide region I into four smaller triangular regions by applying the triangulation algorithm, which will generate the coordinates of the new voltage space vectors and the inverter states corresponding to these new switching vectors. The three new voltage space vectors divide region I into four smaller triangular regions marked R_1 , R_2 , R_3 , and R_4 as shown in Fig. 5.11(b). Thus, by determining the switching states through triangulation algorithm for the three-level inverter, 27 switching states and sectors are represented in Fig. 5.12.

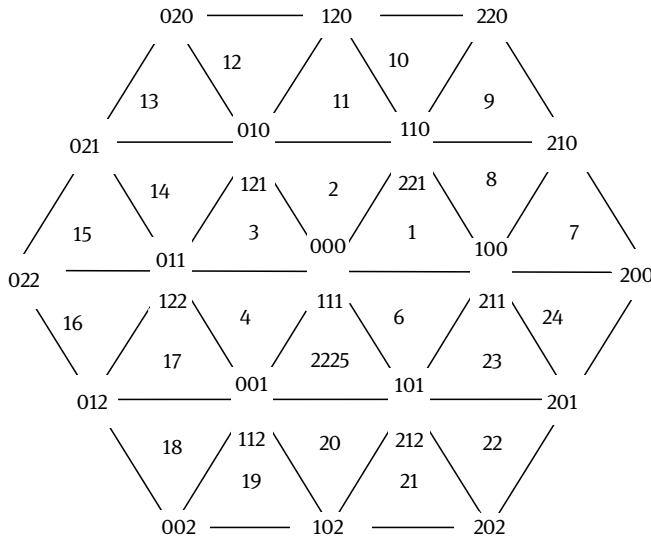


Fig. 5.12: Switching states and sectors of the three-level inverter.

5.3.2 Determination of centroid

The location of the tip of the reference voltage space vector $A_{00}P$ among these four triangular regions is found by determining the region whose centroid is closest to the tip of the reference space vector. The coordinates of the centroid of an equilateral triangle can be determined as the average of coordinates of the three vertices. For an equilateral triangle with the coordinates of the vertices as $(\alpha_1, \beta_1), (\alpha_2, \beta_2), (\alpha_3, \beta_3)$, the coordinates of the centroid $(\alpha_{\text{cent}}, \beta_{\text{cent}})$ can be obtained from Eq. (5.18).

The triangle with the centroid closest to the tip of the reference space vector is $\Delta A_{11}A_{12}A_{13}$. From among these four triangles, the triangle enclosing the reference space vector $A_{00}P$ is $\Delta A_{11}A_{12}A_{13}$, as its centroid is closest to the tip of the reference space vector. The $\Delta A_{11}, A_{12}, A_{13}$ corresponds to sector 8. The sector is identified and the inverter states corresponding to the switching vectors located at the vertices of the identified sector are also generated simultaneously.

5.3.3 Determination of switching times

The voltage reference vector $A_{00}P$ is identified in sector 8 as shown in Fig. 5.29(b). The voltage space vector with the tip located at A_{12} becomes the virtual zero vector for sector 8. Sector 8 thus gets mapped to sector 1 of the three-level inverter. The determination of duration now reduces to that of a two-level inverter, since after mapping, one of the vectors of the identified sector coincides with the

zero vectors. The durations of the vectors can be determined as in the case of the two-level inverter.

5.3.4 Determination of optimized switching sequence

Once the switching vectors are determined and their respective durations are calculated, the vectors are to be switched in an optimum sequence such that only one switching occurs when the inverter changes its state. In the SVPWM technique, optimum switching is achieved using the redundant states of the zero vector for alternate switching cycles. In this chapter, optimum switching is achieved using two redundant switching states of the respective virtual zero vector in the alternate cycles. The tip of the reference vector $A_{00}P$ is located in sector 8. The switching states corresponding to the switching vectors at the vertices of sector 8 with redundancies are A_{11} (100,211), A_{12} (110,221), and A_{13} (210). For sector 8, the virtual zero vector at A_{12} has two redundant switching states whereas the voltage vectors at A_{11} has two redundancies and A_{13} has one redundancy. If the redundancy of the virtual zero vector is greater than two, the last two redundant switching states are selected for the virtual zero vector. For the other two vectors, if redundant states are more than one, the last redundant state is selected. In case of the three-level inverter, as the zero vector at A_{12} has two redundant switching states, both of these are selected. As the space vector A_{11} has more than

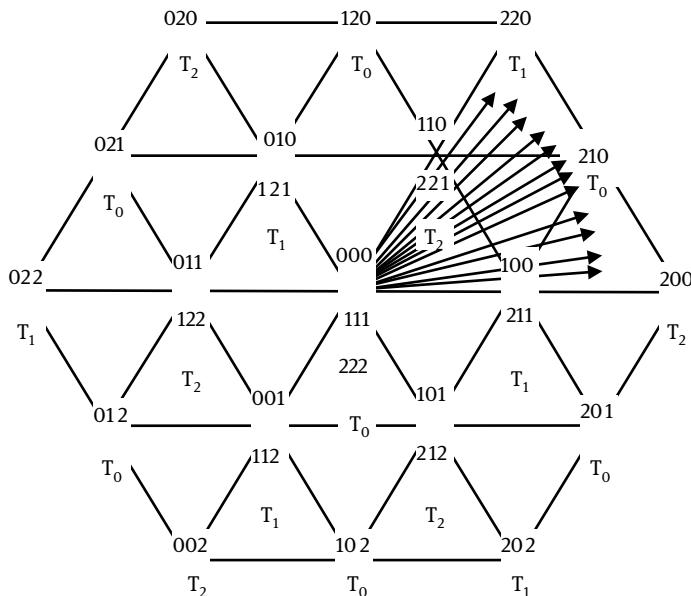


Fig. 5.13: Space vector diagram of the three-level inverter with rotating reference vector.

one redundant state, the last switching state is selected. As A_{13} has only one redundant state, it is selected. This strategy of choosing the last two redundant states for the virtual zero vector and the last redundant state for the other vectors will achieve optimum switching sequence. The selection will result in switching states 110-210-211-221 for the virtual zero vector. With this switching sequence, only one switching occurs as the inverter changes its state.

By following the above procedure of the fractal approach for the three-level inverter, the switching states and switching sequence of a reference vector is generated. Considering twelve samples of the reference vector in a single sector, as shown in Fig. 5.13, by rotating reference angle from 0° to 360° , a total of 72 samples are obtained. The optimized switching sequence for 72 samples is determined and presented in Tab. 5.1.

Tab. 5.1: Switching states of the three-level inverter.

Samples	States	Switching states
1	4-16-17-5	100-200-210-211
2	5-17-16-4	211-210-200-100
3	4-16-17-5	100-200-210-211
4	5-17-16-4	211-210-200-100
5	6-17-5-7	110-210-211-221
6	7-5-17-6	221-211-210-110
7	6-17-5-7	110-210-211-221
8	7-5-17-6	221-211-210-110
9	6-17-18-7	110-210-220-221
10	7-18-17-6	221-220-210-110
11	6-16-18-7	110-210-220-221
12	7-18-17-6	221-220-210-110
13	6-19-18-7	110-120-220-221
14	7-18-19-6	221-220-120-110
15	6-19-18-7	110-120-220-221
16	7-18-19-6	221-220-120-110
17	6-19-9-7	110-120-121-221
18	7-9-19-6	221-121-120-110
19	6-19-9-7	110-120-121-221
20	7-9-19-6	221-121-120-110
21	8-20-19-9	010-020-120-121
22	9-19-20-8	121-120-020-010
23	8-20-19-9	010-020-120-121
24	9-19-20-8	121-120-020-010
25	8-20-21-9	010-020-021-121
26	9-21-20-8	121-021-020-010
27	8-20-21-9	010-020-021-121
28	9-21-20-8	121-021-020-010
29	10-21-9-11	011-021-121-122
30	11-9-21-10	122-121-021-011

Tab. 5.1 (continued)

Samples	States	Switching states
31	10-21-9-11	011-021-121-122
32	11-9-21-10	122-121-021-011
33	10-21-22-11	011-021-022-122
34	11-22-21-10	122-022-021-011
35	10-21-22-11	011-021-022-122
36	11-22-21-10	122-022-021-011
37	10-23-22-11	011-012-022-122
38	11-22-23-10	122-022-012-011
39	10-23-22-11	011-012-022-122
40	11-22-23-10	122-022-012-011
41	10-23-13-11	011-012-112-122
42	11-13-23-10	122-112-012-011
43	10-23-13-11	011-012-112-122
44	11-13-23-10	122-112-012-011
45	12-24-23-11	001-002-012-112
46	13-23-24-12	112-012-002-001
47	12-24-23-11	001-002-012-112
48	13-23-24-12	112-012-002-001
49	12-24-25-13	001-002-102-112
50	13-25-24-12	112-102-002-001
51	12-24-25-13	001-002-102-112
52	13-25-24-12	112-102-002-001
53	14-25-13-15	101-102-112-212
54	15-13-25-14	212-112-102-101
55	14-25-13-15	101-102-112-212
56	15-13-25-14	212-112-102-101
57	14-25-26-15	101-102-202-212
58	15-26-25-14	212-202-102-101
59	14-25-26-15	101-102-202-212
60	15-26-25-14	212-202-102-101
61	14-27-26-15	101-201-202-212
62	15-26-27-14	212-202-201-101
63	14-27-26-15	101-201-202-212
64	15-26-27-14	212-202-201-101
65	14-27-5-15	101-201-211-212
66	15-5-27-14	212-211-201-101
67	14-27-5-15	101-201-211-212
68	15-5-27-14	212-211-201-101
69	4-16-27-5	100-200-201-211
70	5-27-16-4	211-201-200-100
71	4-16-27-5	100-200-201-211
72	5-27-16-4	211-201-200-100

5.4 Implementation of the algorithm for the five-level inverter

This section explains the proposed method for generation of SVPWM for the five-level inverter using the inherent fractal structure associated with the switching space vector representation of multilevel inverter. The schematic diagram of the five-level inverter is shown in Fig. 5.14.

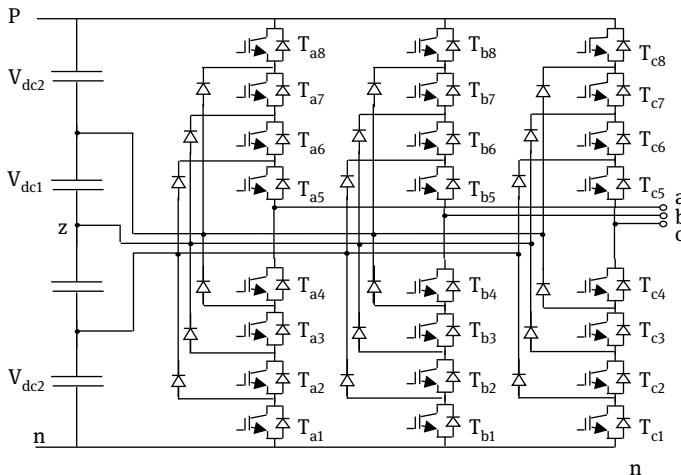


Fig. 5.14: Five-level diode-clamped inverter.

The dc bus voltage is split into five levels using four dc capacitors, C_1 , C_2 , C_3 , and C_4 . Each capacitor has $V_{dc}/4$ V each voltage stress will be limited to one capacitor level through clamping diodes. In the five-level inverter, clamping diodes clamped the bus voltage into three voltage levels, $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$. These states are defined as 4, 3, 2, 1, and 0, respectively. There are N^3 possible states, i.e. 125 states for the five-level inverter and it consists of $(5 - 1) = 4$ capacitors on the dc bus, $2(5 - 1) = 8$ switching devices per phase and $2(5 - 2) = 6$ clamping diodes per phase.

5.4.1 Determination of switching vectors

In the case of the five-level inverter, voltage V_{dc} , in the normalized space vector representation, is represented by a vector of length 4. The switching vectors located at the six vertices of the hexagon forming the periphery are the same as the vectors of the equivalent two-level inverter, but they have switching states (400), (440), (040), (044), (004), (404).

The position of the reference space vector $A_{00}P$ for the five-level inverter is as shown in Fig. 5.15. The switching states of five-level inverter are shown in Fig. 5.16. The first step in the proposed sector identification of this method is to determine the location of the tip of the reference space vector $A_{00}P$ from among the six regions of the equivalent two-level inverter. Region I is formed by the vertices A_{00} , A_{01} , and A_{02} . The coordinates of the vertices are $(0,0)$, $(4,0)$, and $(2, 2\sqrt{3})$, respectively, as shown in Fig. 5.17. The switching states of the vector located at A_{00} , A_{01} , and A_{02} are $(000, 111, 222, 333, 444)$, (400) , and (440) , respectively. The next step is to divide region I into four smaller triangular regions by applying the triangularization algorithm and generates the coordinates of the new voltage space vectors and the inverter states corresponding to these new switching vectors. The three new voltage space vectors divide region I into four smaller triangular regions marked as R_1 , R_2 , R_3 , and R_4 as shown in Fig. 5.17.

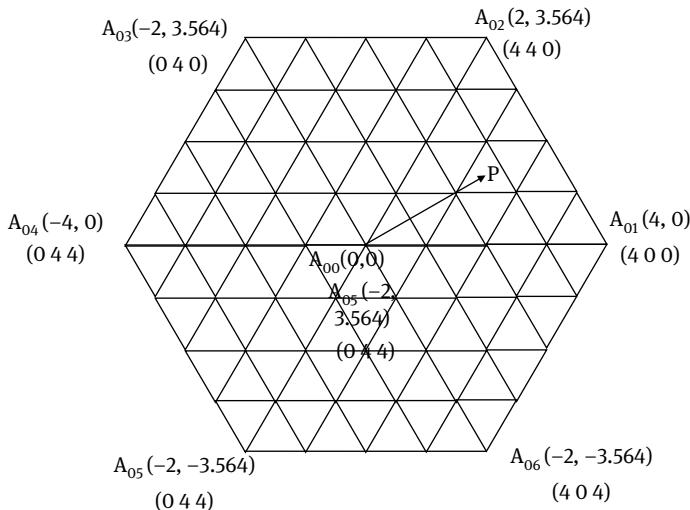


Fig. 5.15: Space vector representation of the five-level inverter.

5.4.2 Determination of centroids

The location of the tip of the reference voltage space vector $A_{00}P$ among these four triangular regions is found by determining the region whose centroid is closest to the tip of the reference space vector. The coordinates of the centroid of an equilateral triangle can be determined as the average of coordinates of the three vertices.

The triangle with the centroid closest to the tip of the reference space vector is $\Delta A_{11}A_{12}A_{13}$ for the five-level inverter, the triangularization algorithm has to be applied again, which generates further three new voltage space vectors and the inverter states corresponding to these new voltage vectors, thus dividing it into four smaller triangles, with $\Delta A_{23}A_{25}A_{26}$ as the triangle enclosing the reference space vector $A_{00}P$, as its

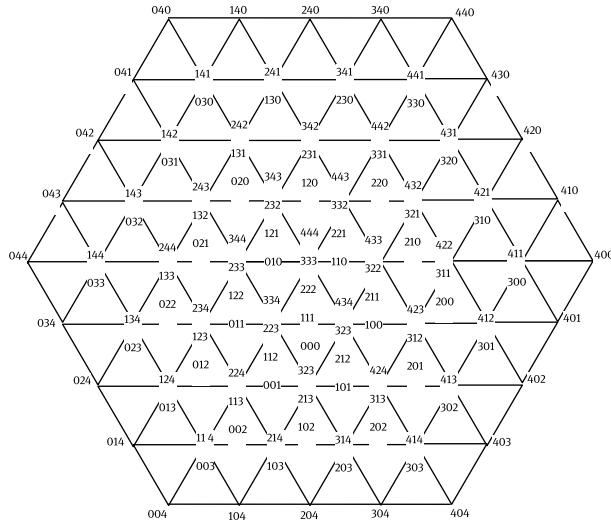


Fig. 5.16: Switching states of the five-level inverter.

centroid is closest to the tip of the reference space vector. The $\Delta A_{23}A_{25}A_{26}$ corresponds to sector 27 of the five-level inverter. The sector is identified and the inverter states corresponding to the switching vectors located at the vertices of the identified sector are also generated simultaneously.

5.4.3 Determination of switching times

For the voltage reference vector A_{00P} , the sector identified is sector 27. The voltage space vector with tip located at A_{23} becomes the virtual zero vector for sector 27. Sector 27 thus gets mapped to sector 1 of the five-level inverter. The determination of duration now reduces to that of a two-level inverter since after mapping one of the vectors of the identified sector coincides with the zero vectors. The durations of the vectors can be determined using the conventional two-level inverter.

5.4.4 Determination of optimized switching sequence

The tip of the reference vector A_{00P} is located in sector 27, as shown in Fig. 5.17. The switching states corresponding to the switching vectors at the vertices of sector 27 with redundancies are A_{23} (210, 321, 432), A_{25} (310, 421) and A_{26} (320, 431). For sector 27, the virtual zero vector at A_{23} has three redundant switching states while the voltage vectors at A_{25} and A_{26} has two redundancies each. In the present work, if the redundancy of the virtual zero vector is greater than two, the last two redundant switching

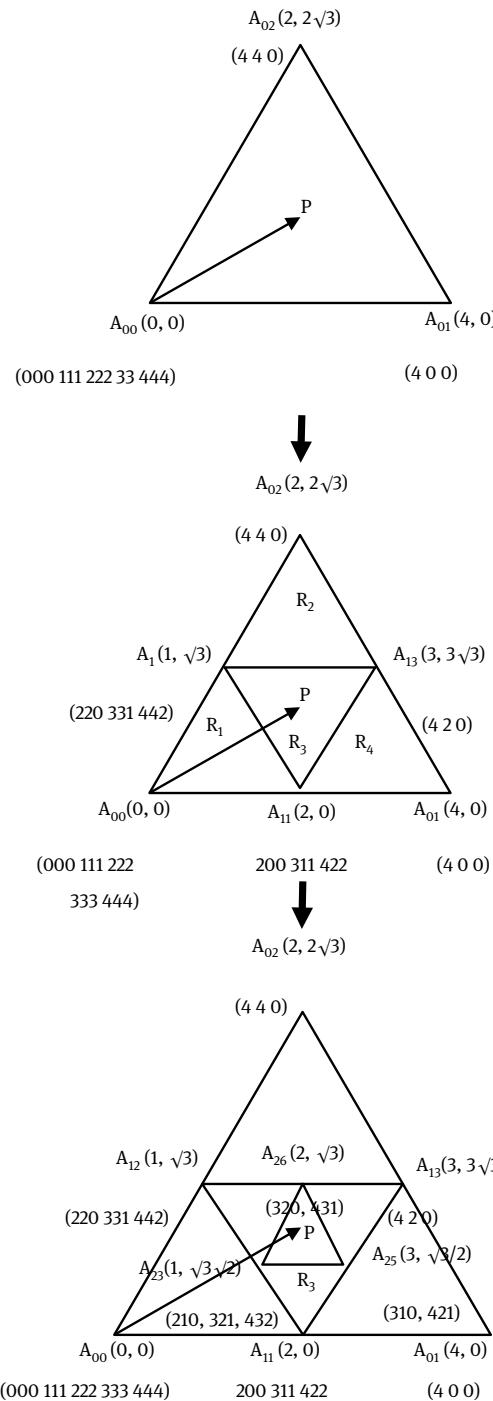


Fig. 5.17: Sector identification and switching vector determination of the five-level inverter.

states are selected for the virtual zero vector. For the other two vectors, if redundant states are more than one, the last redundant state is selected. This strategy of choosing the last two redundant states for the virtual zero vector and the last redundant state for the other vectors will achieve optimum switching sequence. The selection will result in switching states 321–432 for the virtual zero vector. The other vectors have switching states 421 and 431. With these states, the switching sequence of inverter for sector 27 is 321–421–431–432 during a sampling interval and 432–431–421–321 for the subsequent sampling interval. Note that only one switching occurs as the inverter changes state.

By following the above procedure of the fractal approach for the five-level inverter, the switching states and switching sequence of a reference vector are generated. Considering twelve samples of the reference vector in a single sector, as shown in Fig. 5.18 by rotating the reference angle from 0° to 360° , 72 samples are obtained. The optimum switching pattern for these 72 samples obtained through implementation of fractal approach for the five-level inverter is shown in Tab. 5.2.

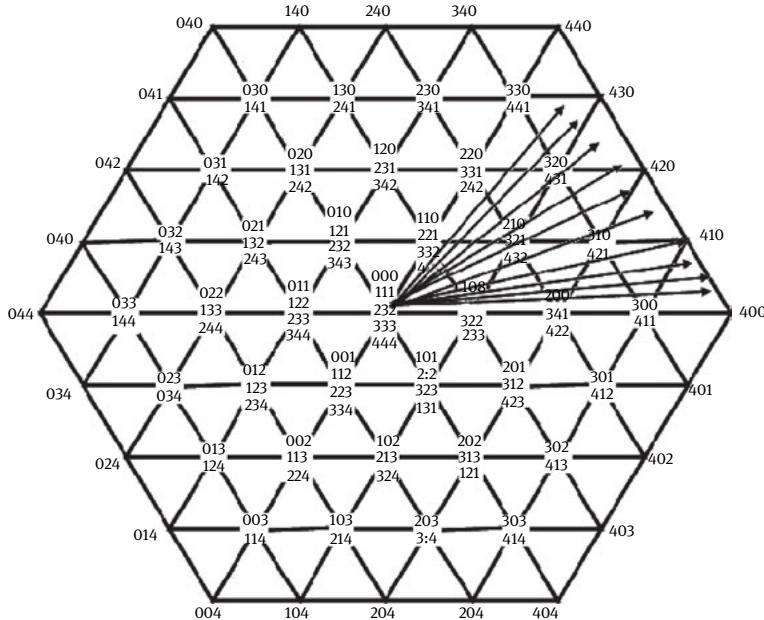


Fig. 5.18: Space vector diagram of the five-level inverter with rotating reference vector.

5.5 Results and discussions

To validate the proposed method of the generation of SVPWM for multilevel inverters using the fractal approach, simulation studies have been carried out with a dc-link voltage of 400 V and modulation index of 0.8. The simulation parameters

Tab. 5.2: Switching states of the five-level inverter.

Samples	States	Switching states
1	66-102-103-67	300-400-410-411
2	67-103-69-66	411-410-310-300
3	68-103-67-69	310-410-411-421
4	69-104-103-68	421-420-410-310
5	68-103-104-69	310-410-420-421
6	71-69-104-70	431-421-420-320
7	70-104-105-71	320-420-430-431
8	71-105-73-70	431-430-330-320
9	72-105-71-73	330-30-431-441
10	73-106-105-72	441-440-430-330
11	72-105-106-73	330-430-440-441
12	73-106-105-72	441-440-430-330
13	72-107-106-73	330-340-440-441
14	73-106-107-72	441-440-340-330
15	72-107-75-73	330-340-341-441
16	75-107-108-74	341-430-240-230
17	74-108-107-75	230-240-340-341
18	75-77-108-74	341-241-240-230
19	76-109-108-77	130-140-240-241
20	77-108-109-76	241-240-140-130
21	76-109-79-77	130-140-141-241
22	79-109-110-78	141-140-040-030
23	49-111-110-78	030-040-140-141
24	79-109-110-78	141-140-040-030
25	78-110-111-79	030-040-041-141
26	79-111-110-78	141-041-040-030
27	80-111-79-81	031-041-141-142
28	81-112-111-80	142-042-041-031
29	80-111-112-81	031-041-042-142
30	83-81-112-82	143-142-042-032
31	82-112-113-83	032-042-043-143
32	83-113-112-82	143-043-042-032
33	84-113-83-85	033-043-143-144
34	85-114-113-84	144-044-043-033
35	84-113-114-85	033-043-044-144
36	85-114-113-84	144-044-043-033
37	84-115-114-85	033-034-044-144
38	85-114-115-84	144-044-034-033
39	84-115-87-85	033-034-134-144
40	87-115-116-86	134-034-024-023
41	86-116-115-87	023-024-034-134
42	87-89-116-86	134-124-024-023
43	88-117-116-89	013-014-024-124
44	89-116-117-88	124-024-014-013
45	88-117-91-89	013-014-114-124

Tab. 5.2 (continued)

Samples	States	Switching states
46	91-117-118-90	114-014-004-003
47	90-118-117-91	003-004-014-114
48	91-117-118-90	114-014-004-003
49	90-118-119-91	003-004-104-114
50	91-119-118-90	114-104-004-003
51	92-119-91-93	103-104-114-214
52	93-120-119-92	214-204-104-103
53	92-119-120-93	103-104-204-214
54	95-93-120-94	314-214-204-203
55	94-120-121-95	203-204-304-314
56	95-121-120-94	314-304-204-203
57	96-121-95-97	303-304-314-414
58	97-120-121-96	414-404-304-303
59	96-121-120-97	303-304-404-414
60	97-120-121-96	414-404-304-303
61	96-123-122-97	303-403-404-414
62	97-122-123-96	414-404-403-303
63	96-123-99-97	303-403-413-414
64	99-123-124-98	413-403-402-302
65	98-125-123-99	302-402-403-413
66	99-101-124-98	413-412-402-302
67	100-125-124-100	301-401-402-412
68	101-124-125-100	412-402-401-301
69	100-125-67-101	301-401-411-412
70	67-125-102-66	411-401-400-300
71	66-102-125-67	300-400-401-411
72	67-125-102-66	411-401-400-300

used in this method are given in Appendix II. Figures 5.19 and 5.20 show the simulation results for the three-level inverter. Figures 5.19 and 5.20 show the process of triangularization and rotation of the reference voltage vector of the three-level inverter, respectively. Figure 5.19 shows the basic SVPWM where the first triangularization was done to locate the reference voltage vector. Figure 5.20 shows the rotation of the reference voltage vector through 0° to 360° in the d-q reference frame. From Fig. 5.20, it is clear that the reference vector is rotated from 0° to 360° , and by the proposed technique, the sectors are clearly identified, when the tip of the reference vector moved from sector 7 to sector 24. As the reference vector is changing from one sector to another, the simultaneous switching sequence is given to the multilevel inverter.

Figs. 5.21 and 5.22 show the pole voltages and line voltages of the three-level inverter, respectively. Figures 5.23 and 5.24 show the phase voltages and gate currents, respectively. Figure 5.25 shows the stator currents of the three-level inverter fed induction motor. The rotor speed and torque of the three-level inverter fed induction motor are shown in Figs. 5.26

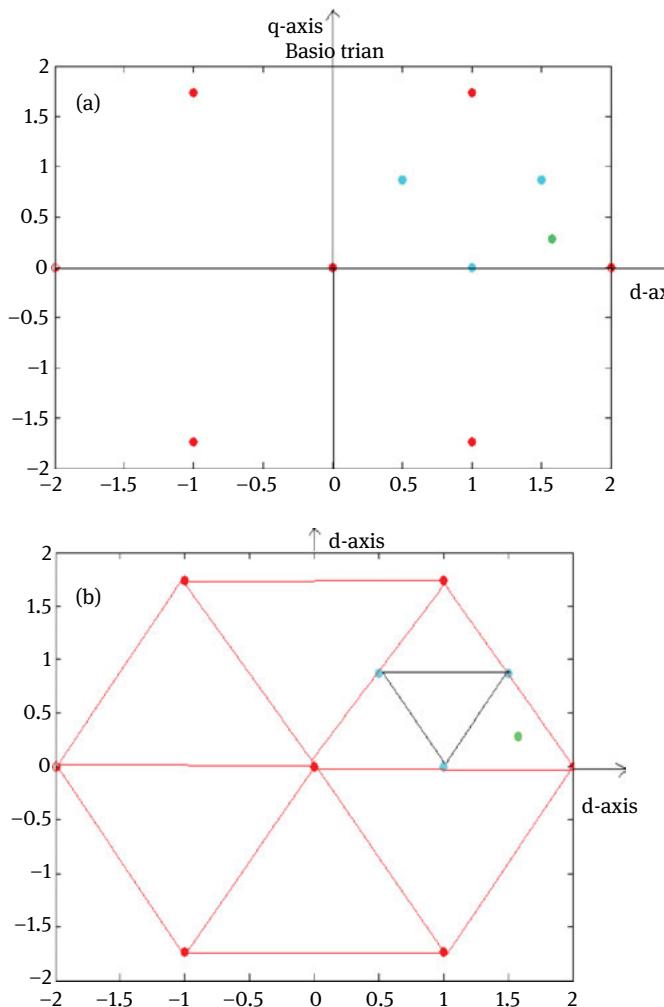


Fig. 5.19: Space vector diagram of the three-level inverter for a basic reference angle (a) of 6° .

and 5.27, respectively. The harmonic spectrum of the inverter output voltage and the total harmonic distortion (THD) are shown in Fig. 5.28.

Figs. 5.28 to 5.38 show the simulation results for the five-level inverter. Figures 5.28 and 5.29 show the process of triangularization and rotation of the reference voltage vector of the five-level inverter, respectively. Figure 5.28 shows the basic SVPWM where the triangularization was done to locate the reference voltage vector. Figure 5.29 shows the rotation of the reference voltage vector through 0° to 360° through sectors 25 to 54 in the d-q reference frame.

Figs. 5.30 and 5.31 show the pole voltages and line voltages of the five-level inverter, respectively. Figures 5.32 and 5.33 show the phase voltages and gate currents, respectively.

Figures 5.34 and 5.35 show the stator currents of the five-level inverter fed induction motor, respectively. The rotor speed and torque of the five-level inverter fed induction motor are shown in Figs. 5.36 and 5.37, respectively. The harmonic spectrum of the five-level inverter output voltage and the THD are shown in Fig. 5.38. The comparison between the three- and five-level inverters with the proposed algorithm is given in Tab. 5.3. These results show that the five-level inverter attains a steady-state response faster than the three-level inverter and that the torque ripple and the THD are reduced.

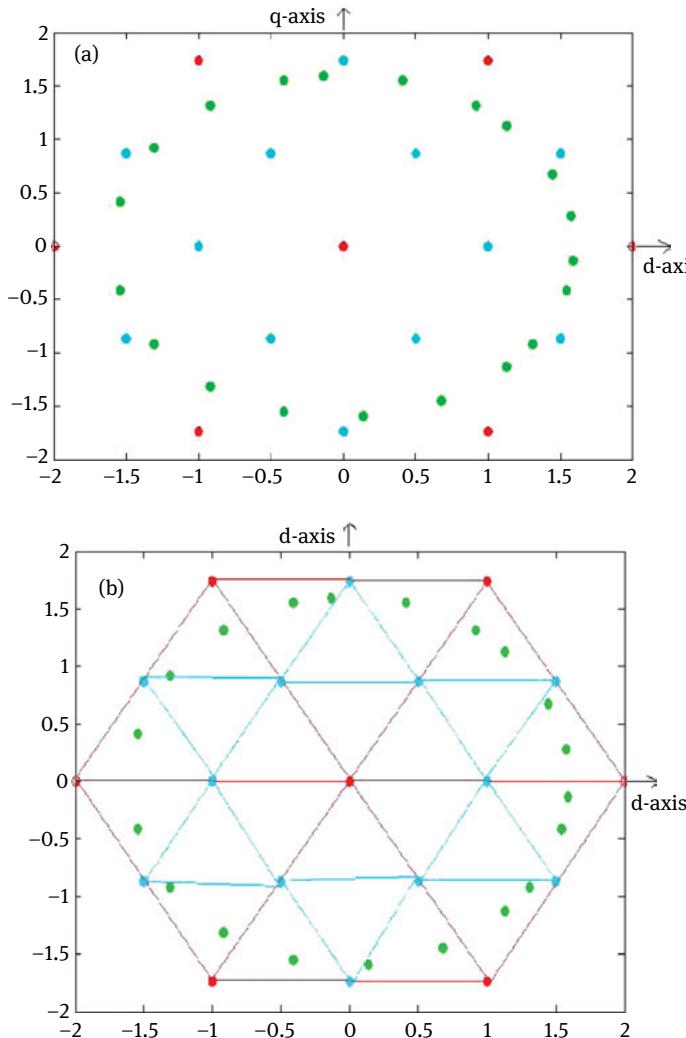


Fig. 5.20: Space vector diagram of the three-level inverter when reference angle (a) rotated through 360° .

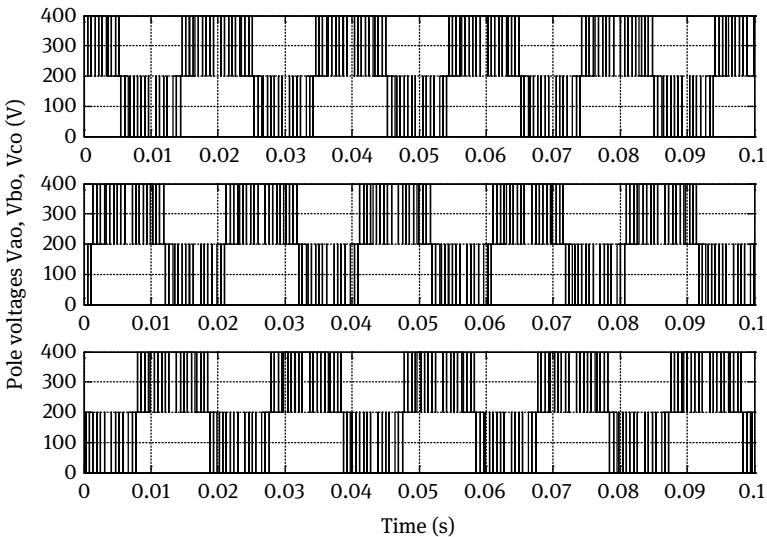


Fig. 5.21: Pole voltages of the three-level inverter.

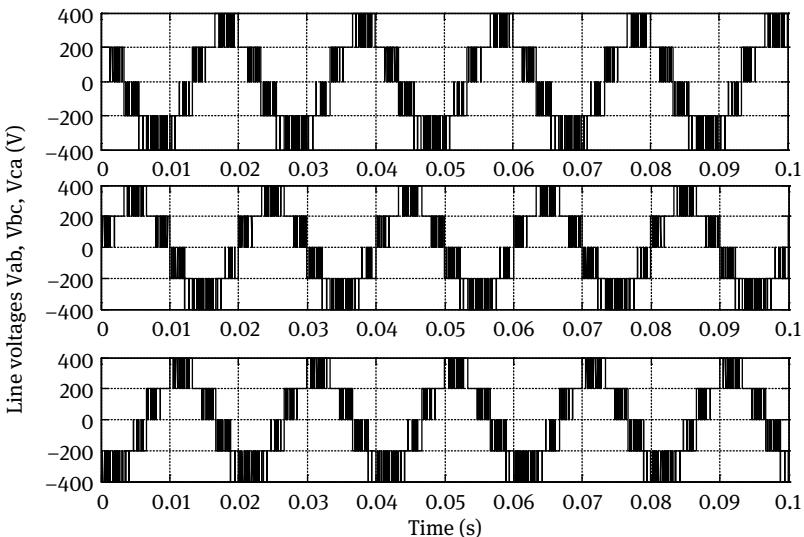


Fig. 5.22: Line-to-line voltages of the three-level inverter.

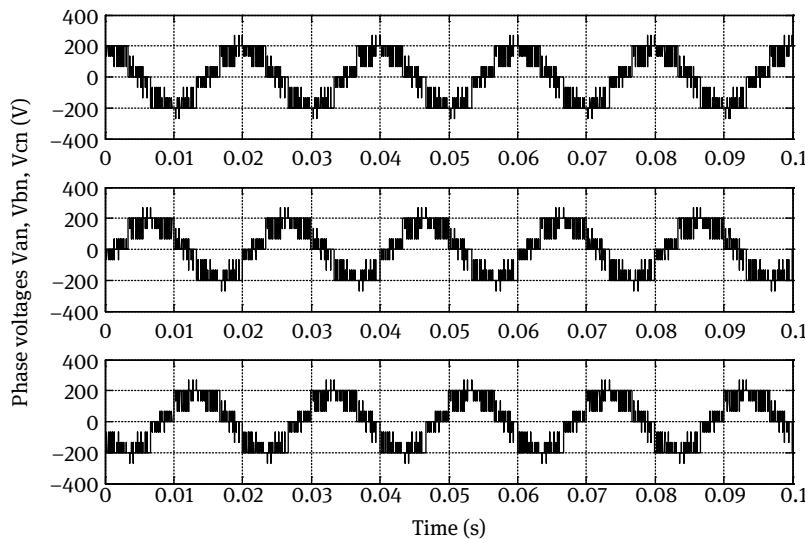


Fig. 5.23: Phase voltages of the three-level inverter.

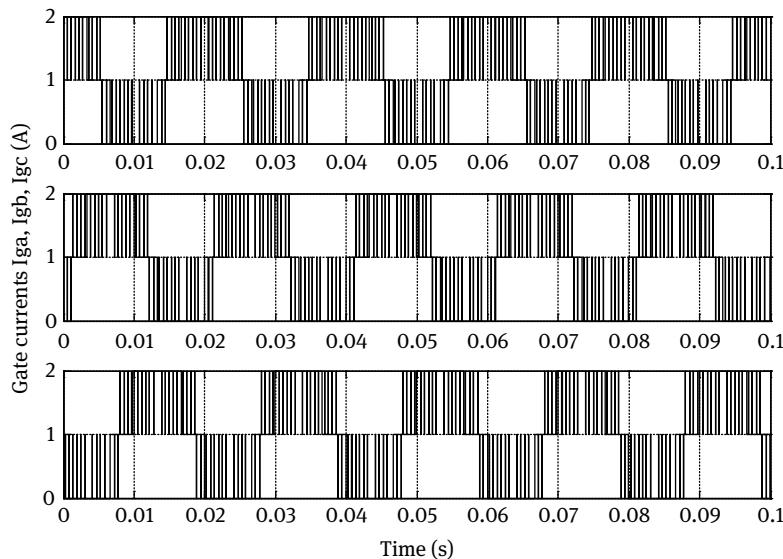


Fig. 5.24: Gate currents of the three-level inverter.

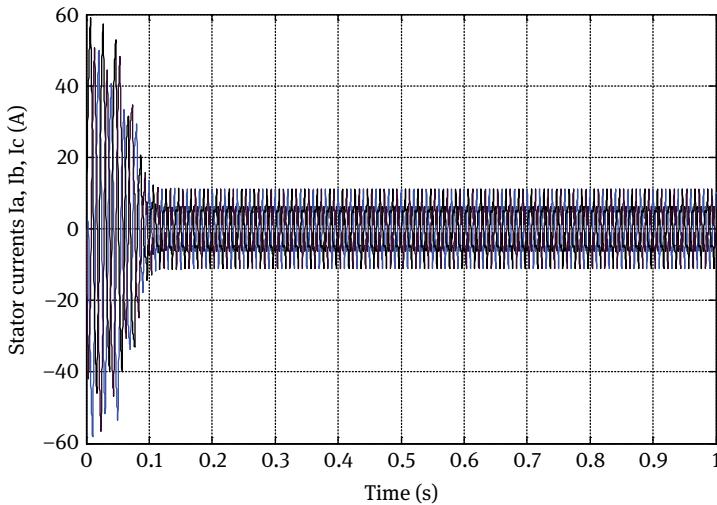


Fig. 5.25: Stator currents of the three-level inverter fed induction motor.

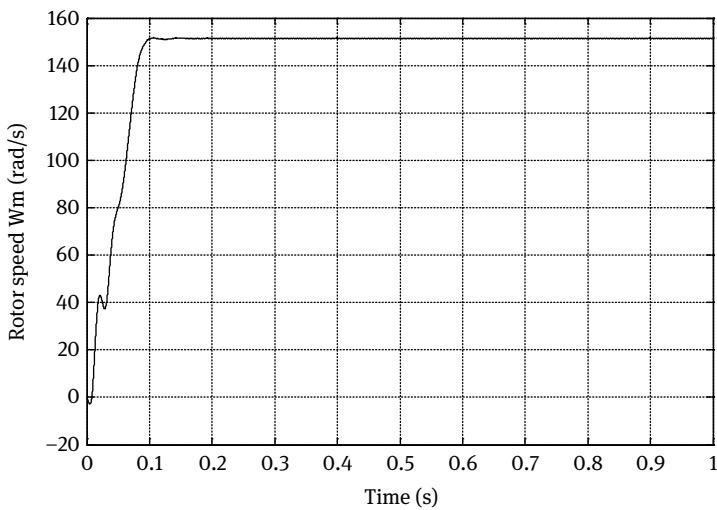


Fig. 5.26: Speed response of the three-level inverter fed induction motor.

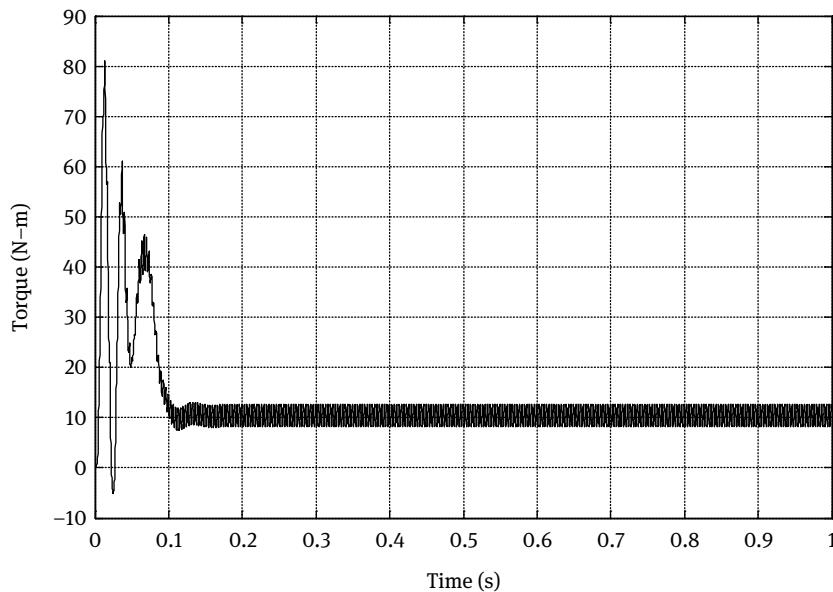


Fig. 5.27: Torque response of the three-level inverter fed induction motor.

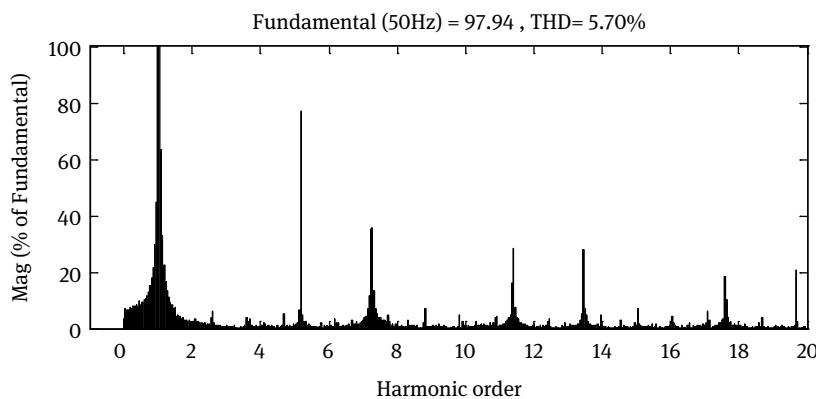


Fig. 5.28: Output line voltage harmonic spectrum of the three-level inverter.

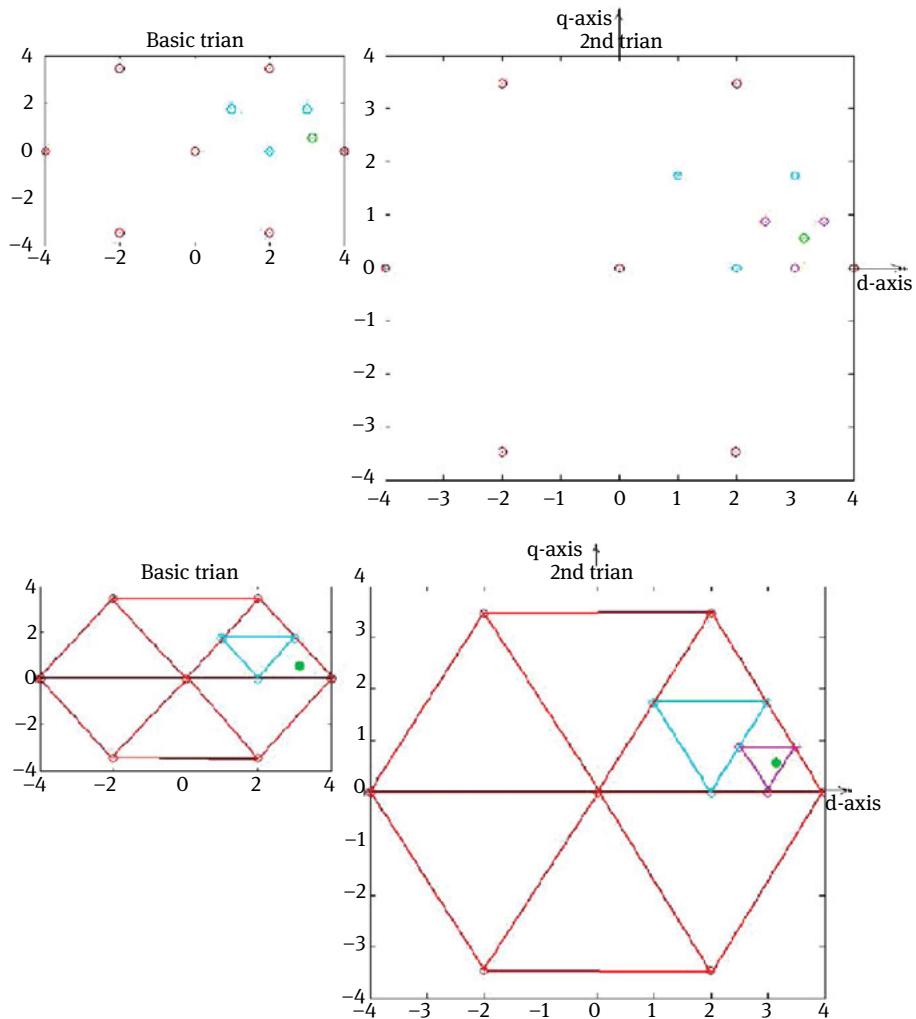


Fig. 5.29: Space vector diagram of the five-level inverter for a basic reference angle (α) of 6° .

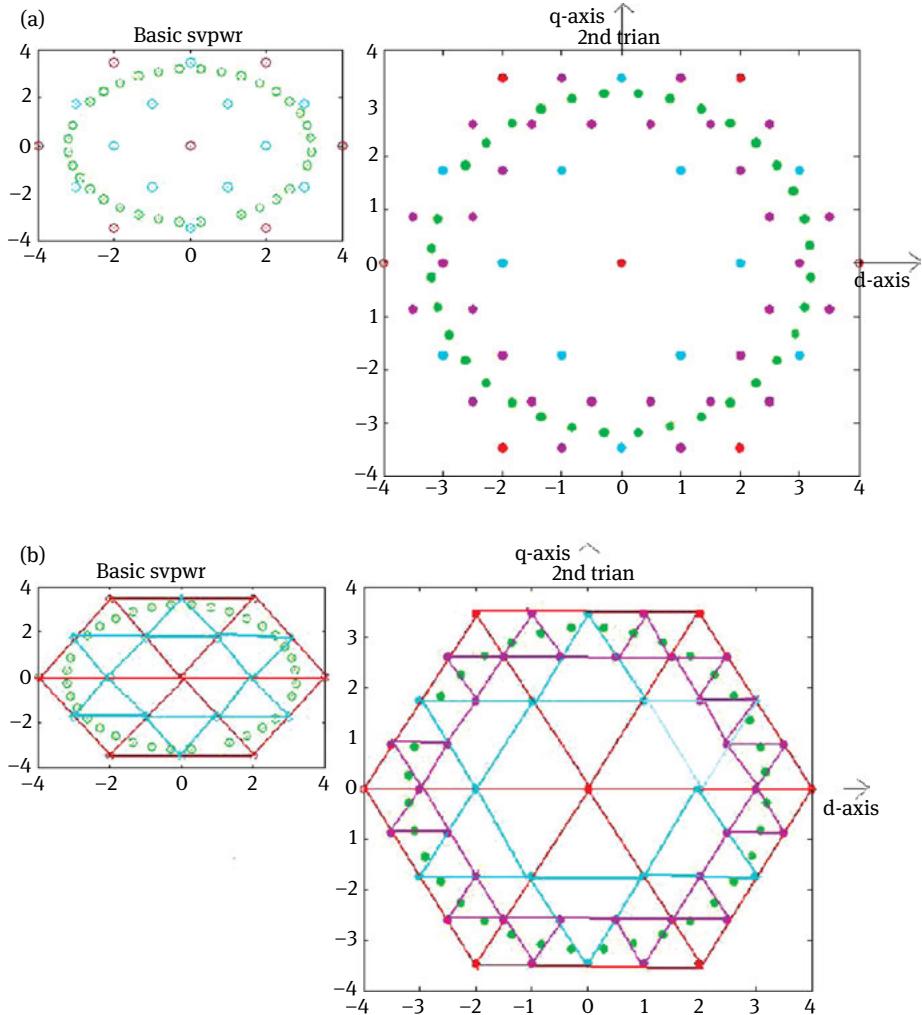


Fig. 5.30: Space vector diagram of the five-level inverter when reference angle (α) rotated through 360° .

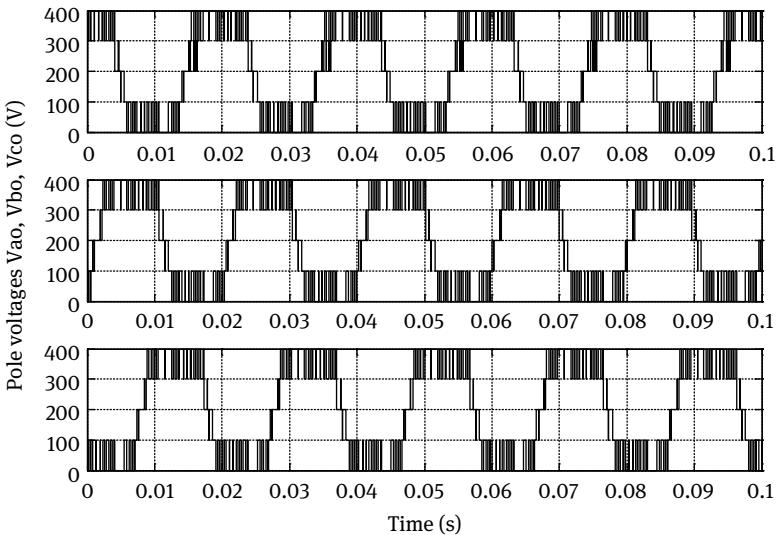


Fig. 5.31: Pole voltages of the five-level inverter.

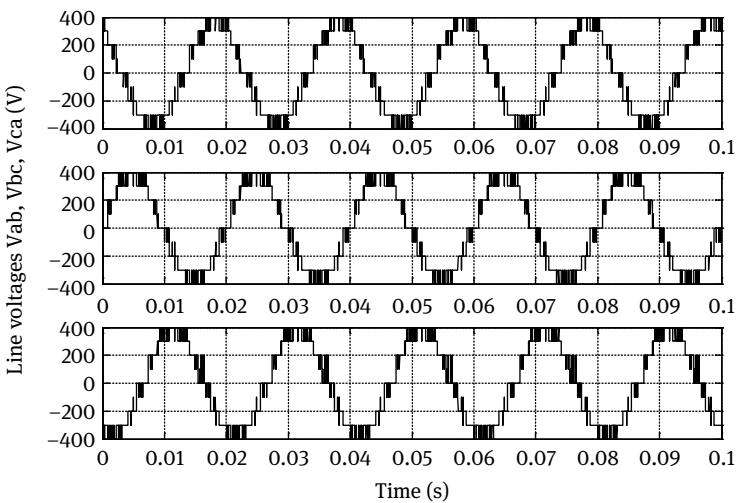


Fig. 5.32: Line-to-line voltages of the five-level inverter.

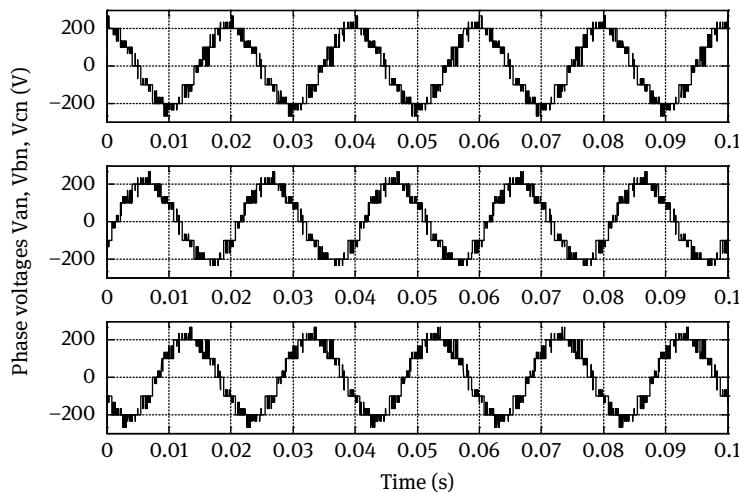


Fig. 5.33: Phase voltages of the five-level inverter.

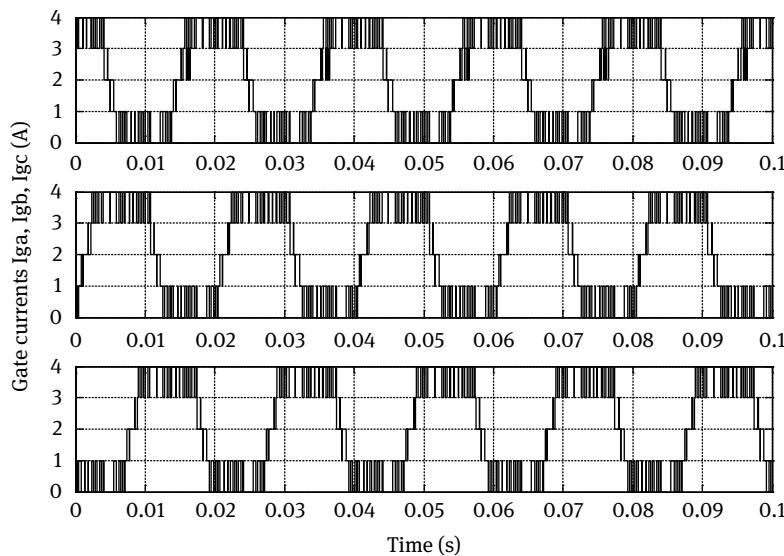


Fig. 5.34: Gate currents of the five-level inverter.

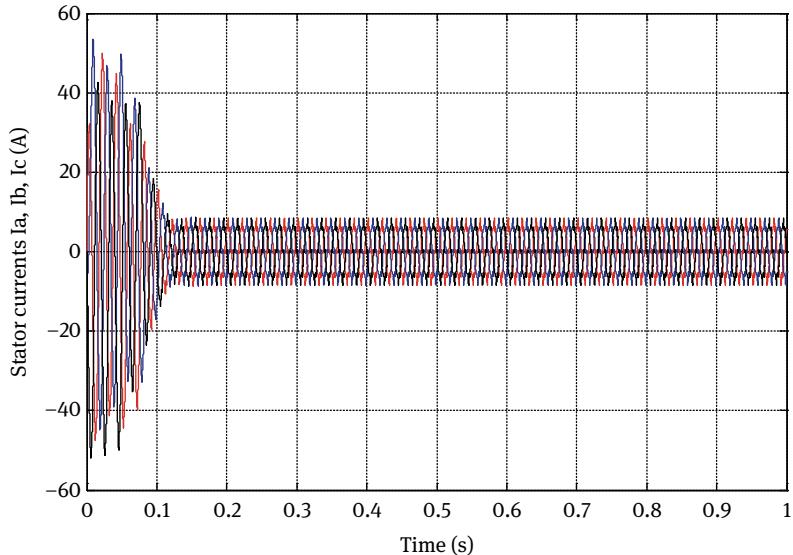


Fig. 5.35: Stator currents of the five-level inverter fed induction motor.

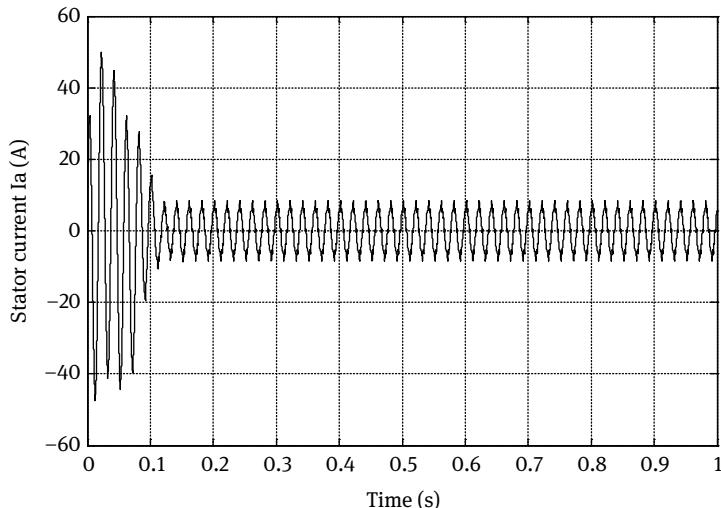


Fig. 5.36: Stator current of the five-level inverter fed induction motor.

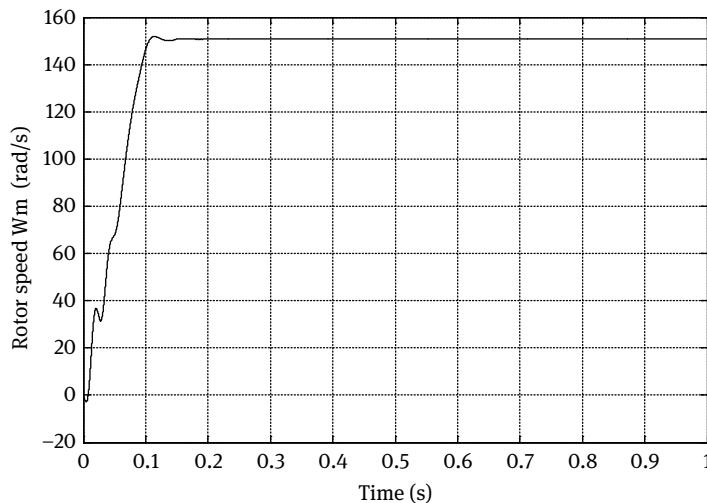


Fig. 5.37: Speed response of the five-level inverter fed induction motor.

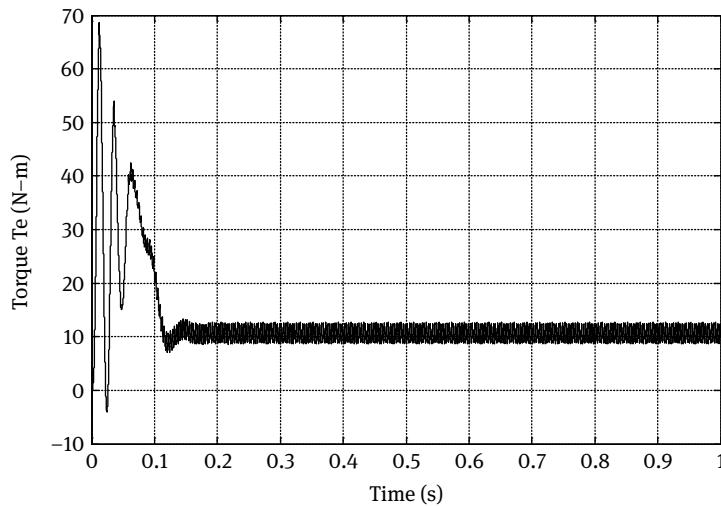


Fig. 5.38: Torque response of the three-level inverter fed induction motor.

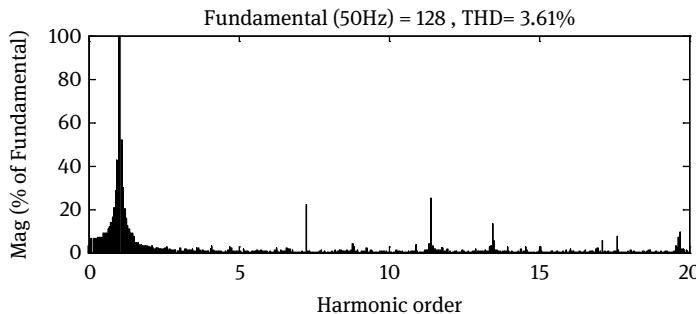


Fig. 5.39: Output voltage harmonic spectrum of the five-level inverter.

The results of three- and five-level inverters have been analyzed and shown in Tab. 5.3. The harmonic spectrum of five-level inverter output voltage is as shown in Fig. 5.39. The five-level inverter shows improved performance than the three-level inverter.

Tab. 5.3: Performance of the three- and five-level inverters.

S.No.	Parameters	Three-Level inverter	Five-Level inverter
01	Torque (N-m)	10.41	10.67
02	Speed (rad/s)	151.4	150.71
03	I_{rms} (A)	5.129	4.859
04	THD (%)	5.70	3.61

5.6 Conclusions

In the field of high-power, high-performance applications, multilevel inverters seem to be the most promising alternative. In this chapter, an algorithm for the generation of SVPWM for multilevel inverter based on fractals has been proposed and applied for three- and five-level inverters. In this method, the switching sequence is determined without using look-up tables, so the memory of the controller can be saved. The switching times of the voltage vectors are calculated at the same manner as two-level SVPWM. Thus, the proposed method reduces the execution time of the three- and five-level SVPWM. The triangularization algorithm is easy to implement, as basic arithmetic is used. It can also be applied to the SVPWM method for N-level. The obtained THDs for the three- and five-level inverters are 5.70% and 3.61%, respectively, which is much less, compared with the conventional SVPWM algorithm.

6 Qualitative space vector pulse width modulation algorithm for multilevel inverters

In this chapter, a qualitative space vector pulse width modulation (SVPWM) algorithm is proposed and implemented for neutral point-clamped (NPC) multilevel inverter. In this method, the duty cycles of the reference voltage vectors are corrected accordingly to identify the location of the reference voltage vector in each region. The appropriate switching sequence of the region and calculation of the switching ON times for each state are estimated. This scheme can be extended to high-level inverters as well. This algorithm has been discussed in detail, and results have been presented and analyzed for two, three, four, five, six and seven-level inverters. The total harmonic distortion (THD) has been calculated, and comparison with lower levels is also presented in this chapter.

The conventional SVPWM algorithm and a novel approach for the generation of SVPWM for multilevel inverters based on fractals are presented in the previous chapters. However, as the number of level increases, the location of the reference voltage vector, optimum switching sequence and dwelling time calculations, and the control algorithm become increasingly complex. To improve the performance of multilevel inverters, a qualitative SVPWM algorithm is proposed and analyzed in this chapter.

6.1 A qualitative SVPWM algorithm for multilevel inverters

Sector identification can be done using coordinate transformation of the reference vector into a two-dimensional coordinate system. The sector can also be determined by resolving the reference phase vector along the a, b and c-axes and by repeated comparison with discrete phase voltages. After identifying the sector, the voltage vectors at the vertices of the sector are to be determined. Once the switching voltage space vectors are determined, the switching sequences can be identified using lookup tables. The calculations of the duration of the voltage vectors can be simplified by mapping the identified sector corresponding to a sector of the two-level inverter. To obtain optimum switching, the voltage vectors are to be switched for their respective durations, in a sequence such that only one switching occurs as the inverter moves from one switching state to another [126].

The duty cycles of the reference voltage vector will be m_1 , m_2 , and $[1 - (m_1 + m_2)]$. The values of m_1 and m_2 are useful in identifying the region where reference vector is located, which is the major problem in the case of multilevel inverters.

In this method, a correction to the duty cycles of the reference vector is applied to identify the location of the reference vector easily in each region of a multilevel inverter. Once the region is identified, the appropriate switching sequence of the region can

be identified. The ON time period for each state can be calculated with the obtained duty cycles.

6.2 Seven-level NPC inverter

The circuit diagram and space vector diagram of seven-level NPC inverter are as shown in Figs. 6.1 and 6.2, respectively. In case of the seven-level inverter, six switches from each phase leg will be ON at any time point to produce predetermined output at phases. The possible switching combinations will be 343, with 216 redundant states. SVPWM is quite different from other PWM techniques. With other PWM techniques, the inverter can be thought of as three separate stages, which create each phase wave form separately. However, the SVPWM treats an inverter as a single unit, with each inverter in specific unique state. Modulation is achieved by switching the state of the inverter. The SVPWM is a digital modulating technique whose the objective is to generate PWM load line voltages that are, in average, equal to given (or reference) load line voltages. This is done in each sampling period by properly selecting the switching states of the inverter and calculating the appropriate time period for each state. The SVPWM is an advanced and computation-intensive PWM method.

The space vector (V_{sr}) constituted by the pole voltages of inverters V_{ao} , V_{bo} , and V_{co} with 120° phase displacement can be defined as

$$V_{sr} = V_{ao} + V_{bo} \exp[j(2\pi/3)] + V_{co} \exp[-j(2\pi/3)]. \quad (6.1)$$

The dwelling time periods T_1 , T_2 , and T_0 are

$$T_1 = \frac{V_{sr} \times T_s \times \sin(\pi/3 - \alpha)}{V_{dc} \times \sin(\pi/3)}. \quad (6.2)$$

$$T_2 = \frac{V_{sr} \times T_s \times \sin \alpha}{V_{dc} \times \sin(\pi/3)} \quad (6.3)$$

$$T_0 = T_s - (T_1 + T_2) \quad (6.4)$$

In multilevel inverters, the reference voltage vector can be reproduced in the average sense by switching among the inverter states situated at the vertices, which are in closest proximity to it. In the case of the two-level inverter, the identification of the reference vector location in a sector is straightforward. However, in a higher-level inverter, the existence of more than one region in the sector will require additional mathematical computation to identify the region where the reference vector is located. The duty cycles (ON time for each state) will be found by equating the volt-seconds of the reference voltage with the nearest three states.

$$m = d_1 V_1 + d_2 V_2 + d_3 V_3, \quad (6.5)$$

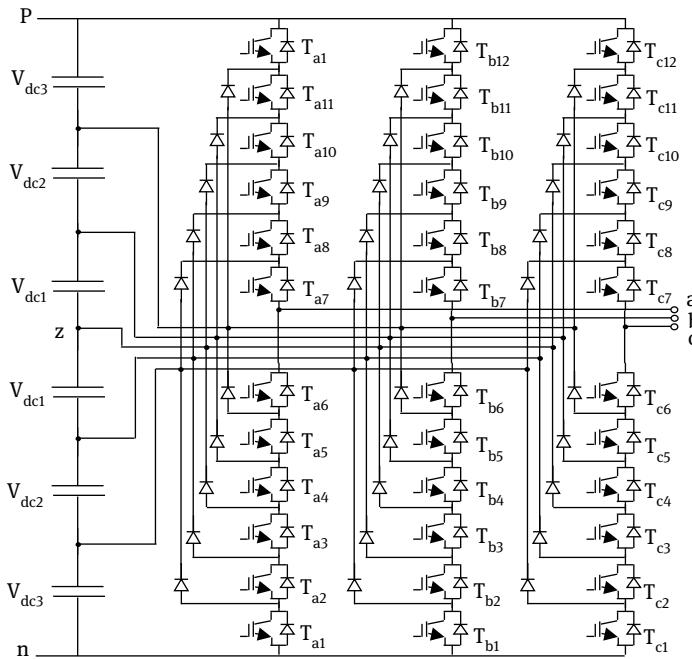


Fig. 6.1: Seven-level NPC inverter topology.

where d_1 , d_2 , and d_3 are the duty cycles of the nearest voltage vectors V_1 , V_2 , and V_3 and m is the voltage reference vector.

6.2.1 Calculation of duty cycles

The vector states at the vertices of each region can be identified from space vector diagrams. Consider the space vector diagram of sector 1 of the seven-level inverter, shown in Fig. 6.3. The reference vector m_3 is located in region 2 of the three-level inverter. m_6 and m_7 are the reference vectors located in region 21 of the six-level inverter and region 29 of the seven-level inverter, respectively. m_{x1} and m_{x2} ($x = 3$ or 6 or 7) are projections of the reference vectors onto zero axis and 60° axis (angle θ is made by the reference vector from the zero axes, i.e. start sector 1; noted that m_3 , m_6 , and m_7 have different angle θ values). The reference vector can be synthesized by sequential switching operation of the three nearest switching states (vertices of the region where the reference vector is located).

The lengths of new vectors can be found using

$$\begin{aligned} m_1 &= m \times (\cos \theta - \sin \theta / \sqrt{3}) \\ m_2 &= 2 \times m \times (\sin \theta / \sqrt{3}) \end{aligned} \quad (6.6)$$

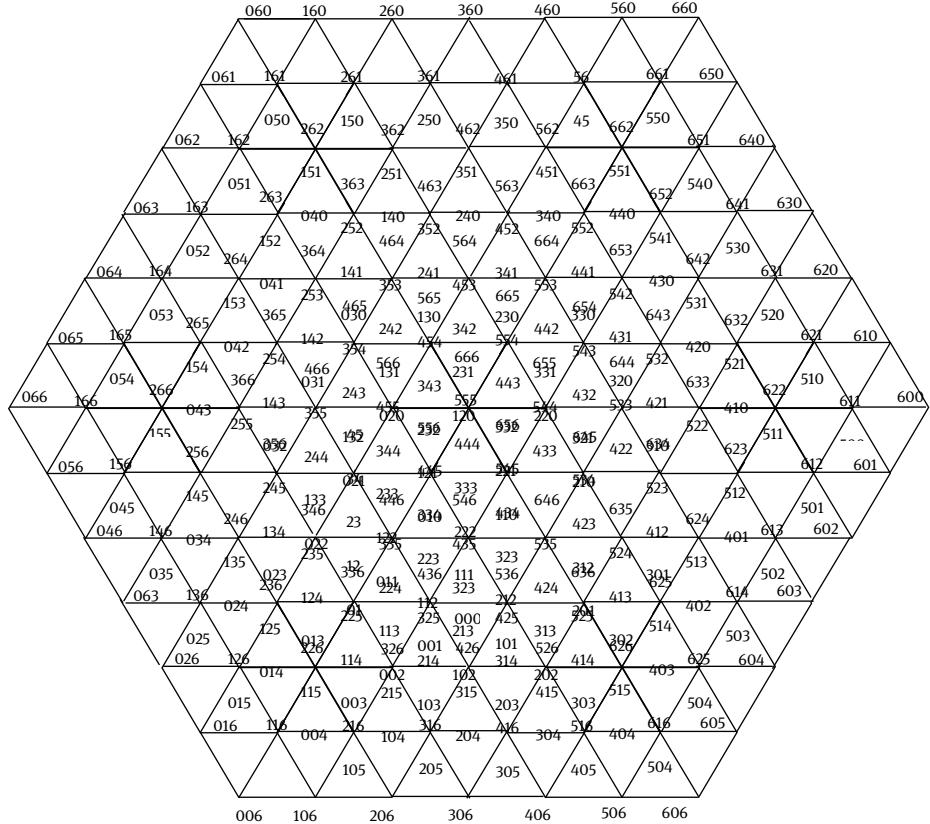


Fig. 6.2: Space vector diagram of the seven-level inverter.

The values of m_1 and m_2 for the reference vector in each region can be calculated using Eq. (6.6). The duty cycles of the vertices of the reference voltage will be m_1 , m_2 , and $[1 - (m_1 + m_2)]$. For example, with reference to m_3 (reference vector in region 2), the reference vector can be synthesized by switching vectors V_1 , V_2 , and V_3 . It is important to note that the duty cycle for switching state V_1 shall be the length of the vector joining V_3 and V_1 , whereas m_1 is the projection of reference vector m_3 from the origin. As such, the corrected duty cycle for switching state V_1 in the present case would be $(m_1 - 0.167)$. The length of the vector joining V_3 and V_2 is m_2 . As such, the corrected duty cycles for the switching states V_1 , V_2 , and V_3 would be $(m_1 - 0.167)$, m_2 , and $(0.833 - m_1 - m_2)$, respectively.

The values of m_1 and m_2 are useful in identifying the region where the reference vector is located, which is the major problem in multilevel inverters. The conditions for identifying the reference vector location in each region and the corrected duty cycles for each of the level of inverter are shown in Tab 6.1. Once

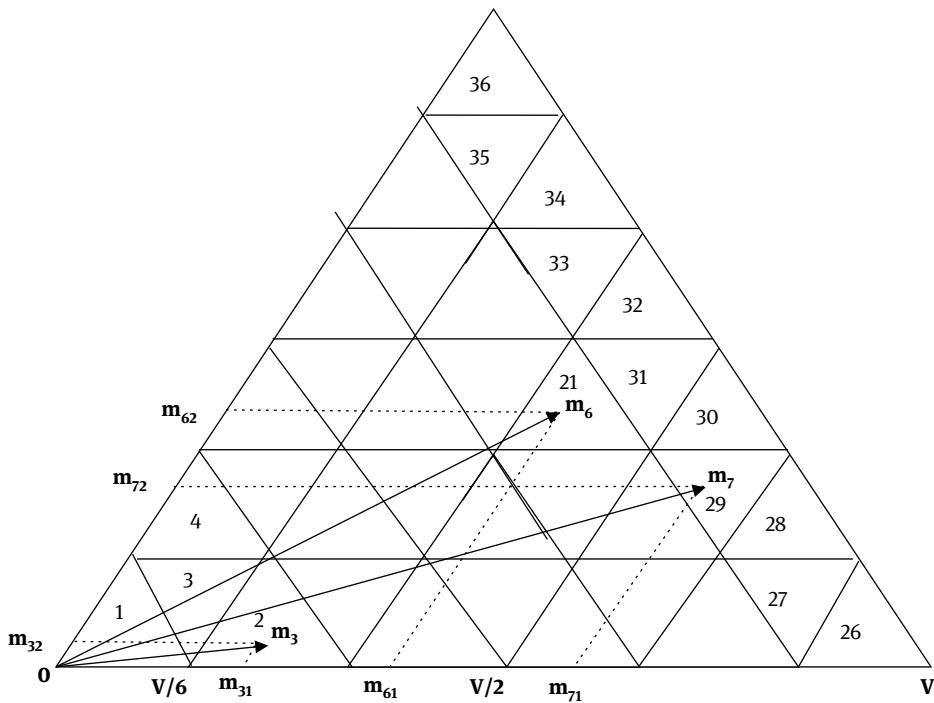


Fig. 6.3: Sector I of the seven-level inverter.

the region is identified, the appropriate switching sequence of a region can be identified.

The ON time period for each state can be calculated with the duty cycles obtained:

$$\begin{aligned}
 T_{ON} \text{ for state 1} &= Ts \times m_1 \\
 T_{ON} \text{ for state 2} &= Ts \times m_2 \\
 T_{ON} \text{ for state 3} &= Ts \times [1 - (m_1 + m_2)]. \tag{6.7}
 \end{aligned}$$

6.2.2 A qualitative SVPWM algorithm

1. Find the sector where V_{ref} lies.
2. Calculate m_1, m_2 from Eq. (6.6) and compute $(m_1 + m_2)$ of the reference voltage.
3. Find the region where V_{ref} is located.
4. Identify the nearest three vectors (vertices of region) to the V_{ref} .
5. Select appropriate switching sequences.
6. Compute ON time for each switching state.
7. Place the inverter states in the respective states for the calculated ON times.

6.2.3 Flowchart

The flowchart for the implementation of qualitative space vector pulse width modulation algorithm for multilevel inverters is as shown in Fig. 6.4.

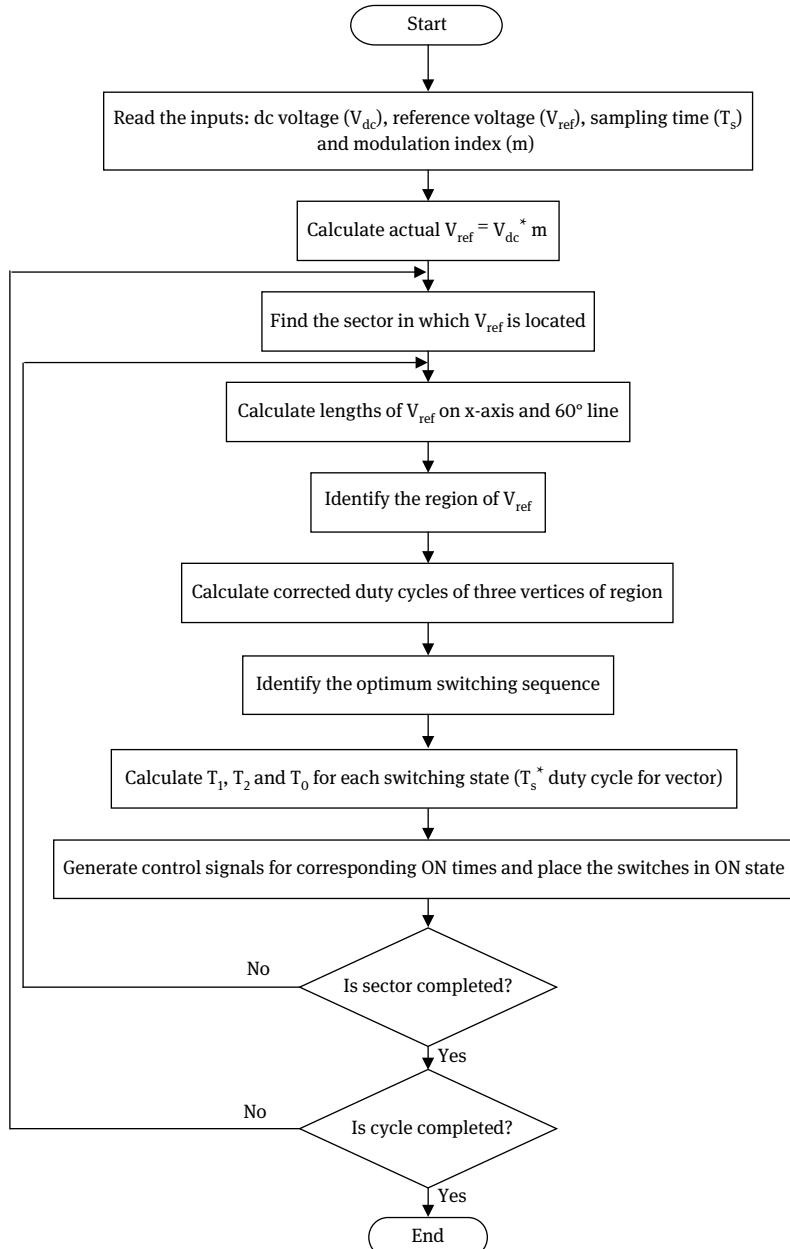


Fig. 6.4: Flowchart of qualitative SVPWM for multilevel inverter.

6.2.4 Location of the reference vector and correction of duty cycles

The conditions for identifying reference vector location in seven-level inverter and the corrections required for the duty cycles are indicated in Tab. 6.1. The switching ON and OFF sequences are as shown in Tab. 6.2.

Tab. 6.1: Location of the reference vector and corrected duty cycles.

Region	Condition for location of the reference vector	Corrected m_1 , m_2 , and m_3 for the switching states
26	$0.834 < m_1 < 1$ $m_2 < 0.167$ $(m_1 + m_2) < 1$	$m_1 = m_1 - 0.833$ $m_2 = m_2$ $m_3 = 1 - m_1 - m_2$
27	$0.667 < m_1 < 0.834$ $m_2 < 0.167$ $(m_1 + m_2) > 0.834$	$m_1 = 0.833 - m_1$ $m_2 = 0.167 - m_2$ $m_3 = m_1 + m_2 - 0.834$
28	$0.667 < m_1 < 0.834$ $0.167 < m_2 < 0.333$ $(m_1 + m_2) < 1$	$m_1 = m_1 - 0.667$ $m_2 = m_2 - 0.167$ $m_3 = 1 - m_1 - m_2$
29	$0.5 < m_1 < 0.667$ $0.167 < m_2 < 0.333$ $(m_1 + m_2) > 0.834$	$m_1 = 0.667 - m_1$ $m_2 = 0.333 - m_2$ $m_3 = m_1 + m_2 - 0.834$
30	$0.5 < m_1 < 0.667$ $0.333 < m_2 < 0.5$ $(m_1 + m_2) < 1$	$m_1 = m_1 - 0.5$ $m_2 = m_2 - 0.333$ $m_3 = 1 - m_1 - m_2$
31	$0.333 < m_1 < 0.5$ $0.333 < m_2 < 0.5$ $(m_1 + m_2) > 0.834$	$m_1 = 0.5 - m_1$ $m_2 = 0.5 - m_2$ $m_3 = m_1 + m_2 - 0.834$
32	$0.333 < m_1 < 0.5$ $0.5 < m_2 < 0.667$ $(m_1 + m_2) < 1$	$m_1 = m_1 - 0.333$ $m_2 = m_2 - 0.5$ $m_3 = 1 - m_1 - m_2$
33	$0.167 < m_1 < 0.333$ $0.5 < m_2 < 0.667$ $(m_1 + m_2) > 0.834$	$m_1 = 0.5 - m_1$ $m_2 = 0.667 - m_2$ $m_3 = m_1 + m_2 - 0.834$
34	$0.167 < m_1 < 0.333$ $0.667 < m_2 < 0.834$ $(m_1 + m_2) < 1$	$m_1 = m_1 - 0.167$ $m_2 = m_2 - 0.667$ $m_3 = 1 - m_1 - m_2$
35	$m_1 < 0.167$ $0.667 < m_2 < 0.834$ $(m_1 + m_2) > 0.834$	$m_1 = 0.167 - m_1$ $m_2 = 0.834 - m_2$ $m_3 = m_1 + m_2 - 0.834$
36	$m_1 < 0.167$ $0.834 < m_2 < 1$ $(m_1 + m_2) < 1$	$m_1 = m_1$ $m_2 = m_2 - 0.834$ $m_3 = 1 - m_1 - m_2$

Tab. 6.2 (continued)

Sector	Region	ON sequence					OFF sequence		
5	70	005	006	106	116	116	106	006	005
	71	005	105	106	116	116	106	105	005
	72	105	106	206	216	216	206	106	105
	73	105	205	206	216	216	206	205	105
	74	205	206	306	316	316	306	206	205
	75	205	305	306	316	316	306	305	205
	76	305	306	406	416	416	406	306	305
	77	305	405	406	416	416	406	405	305
	78	405	406	506	516	516	506	406	405
	79	405	505	506	516	516	506	505	405
	80	505	506	606	616	616	606	506	505
6	91	500	600	601	611	611	601	600	500
	90	500	501	601	611	611	601	501	500
	89	501	601	602	612	612	602	601	501
	88	501	502	602	612	612	602	502	501
	87	502	602	603	613	613	603	602	502
	86	502	503	603	613	613	603	503	502
	85	503	603	604	614	614	604	603	503
	84	503	504	604	614	614	604	504	503
	83	504	604	605	615	615	605	604	504
	82	504	505	605	615	615	605	505	504
	81	505	605	606	616	616	606	605	505

6.3 Results and discussions

To validate the proposed qualitative SVPWM algorithm for multilevel inverters, the simulation studies have been carried out for two, three, four, five, six and seven-level inverters. The simulation parameters and specifications of the induction motor used in this method are given in Appendix III. The results for the two-level inverter are shown in Figs. 6.5 to 6.10. The phase voltages and line voltages of the two-level inverter are shown in Figs. 6.5 and 6.6, respectively. The output voltage harmonic spectrum and the THD are shown in Fig. 6.7. The stator currents, rotor speed, and torque of the two-level inverter fed induction motor are shown in Figs. 6.8 to 6.10, respectively. The results for the three-level inverter are shown in Figs. 6.11 to 6.16. The phase and line voltages are shown in Figs. 6.11 and 6.12, respectively.

The harmonic spectrum of the output voltage and the THD are shown in Fig. 6.13. The stator currents, rotor speed, and torque of the three-level inverter fed induction motor are shown in Figs. 6.14 to 6.16, respectively. The results of the

four-level inverter are shown in Figs. 6.17 to 6.22. The phase voltages, line voltages, output voltage harmonic spectrum, and THD are shown in Figs. 6.17 to 6.19, respectively. The stator currents, rotor speed, and torque of the four-level inverter fed induction motor are shown in Figs. 6.20 to 6.22, respectively. The results of the five-level inverter are shown in Figs. 6.23 to 6.28. The phase voltages, line voltages, output voltage harmonic spectrum, and THD are shown in Figs. 6.23 to 6.25, respectively. The stator currents, rotor speed, and torque of the four-level inverter fed induction motor are shown in Figs. 6.26 to 6.28, respectively. The results of the six-level inverter are shown in Figs. 6.29 to 6.34. The phase voltages, line voltages, output voltage harmonic spectrum, and THD are shown in Figs. 6.29 to 6.31, respectively.

The stator currents, rotor speed, and torque of the four-level inverter fed induction motor are shown in Figs. 6.32 to 6.34, respectively. The results of the seven-level inverter are shown in Figs. 6.35 to 6.40. The phase voltages, line voltages, output voltage harmonic spectrum, and THD are shown in Figs. 6.35 to 6.37, respectively. The stator currents, rotor speed, and torque of the four-level inverter fed induction motor are shown in Figs. 6.38 to 6.40, respectively. From these results, it is observed that as the level of the inverter is increased, the THD is decreased, as shown in Tab. 6.3. and torque ripples are also greatly reduced.

6.3.1 Two-level inverter

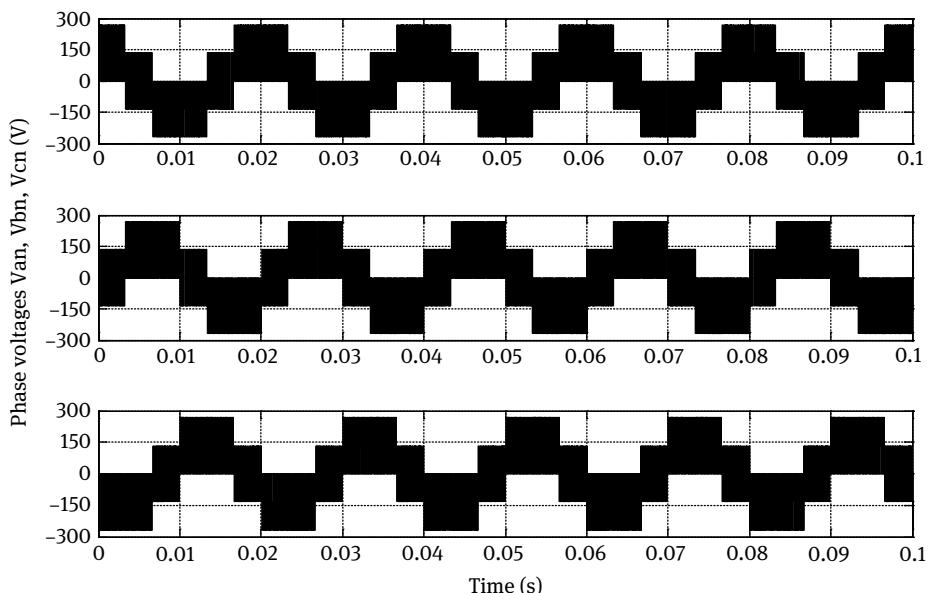


Fig. 6.5: Phase voltages of the two-level inverter.

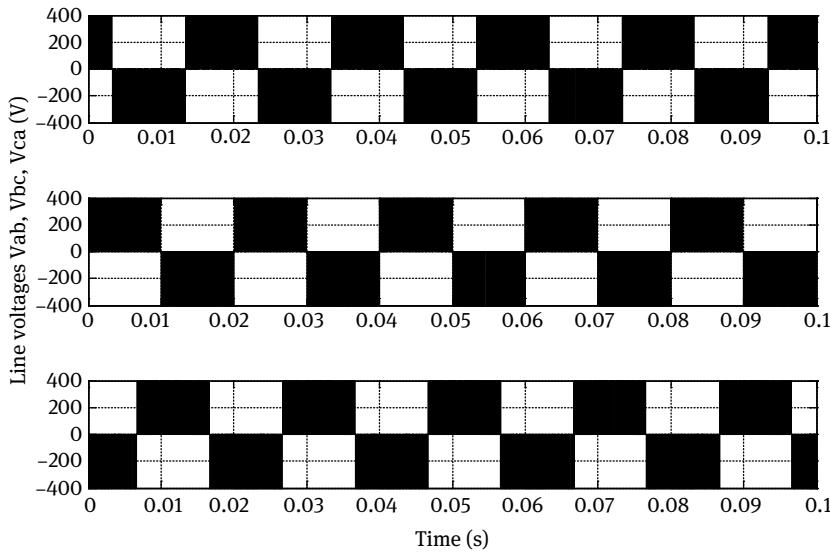


Fig. 6.6: Line-to-line voltages of the two-level inverter.

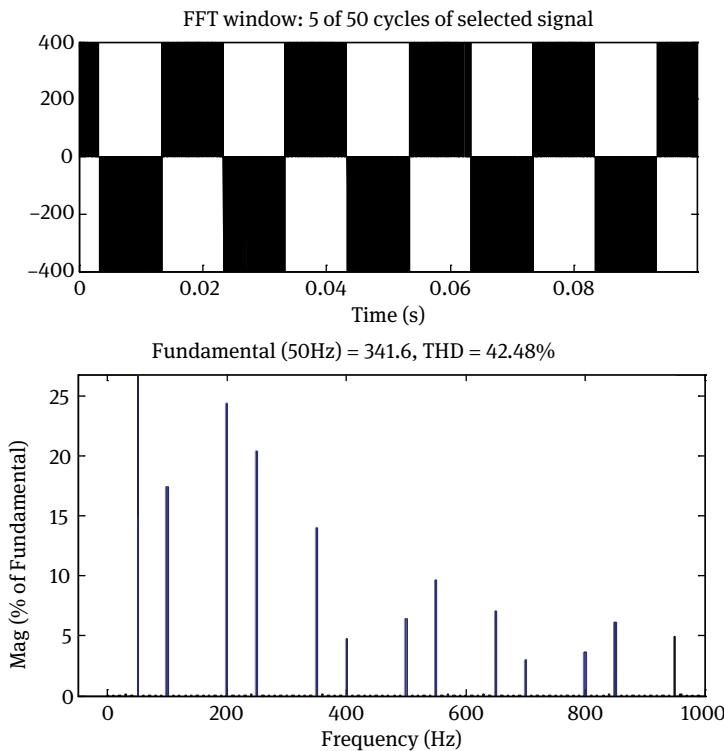


Fig. 6.7: Output line voltage (and its harmonic spectrum) of the two-level inverter.

Stator currents I_a, I_b, I_c (A)

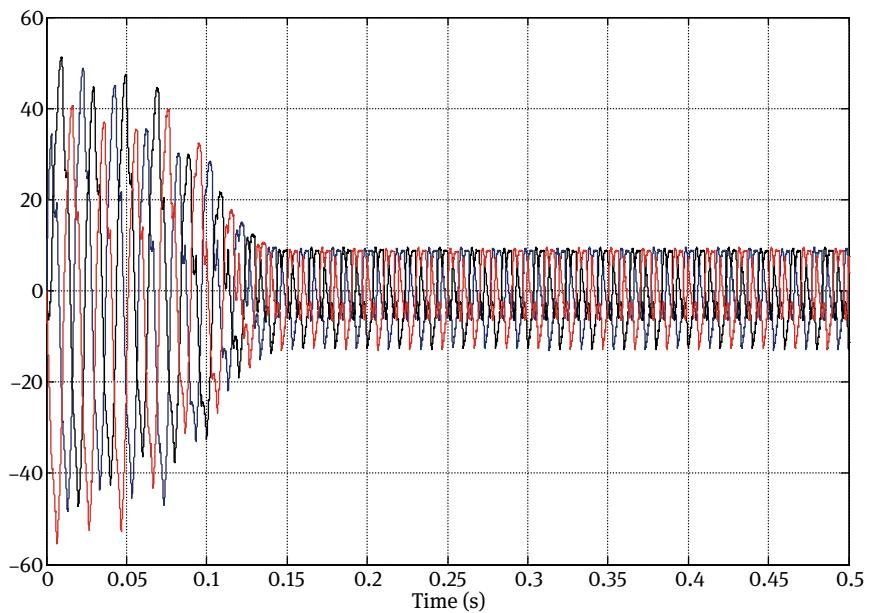


Fig. 6.8: Stator currents of the two-level inverter fed induction motor.

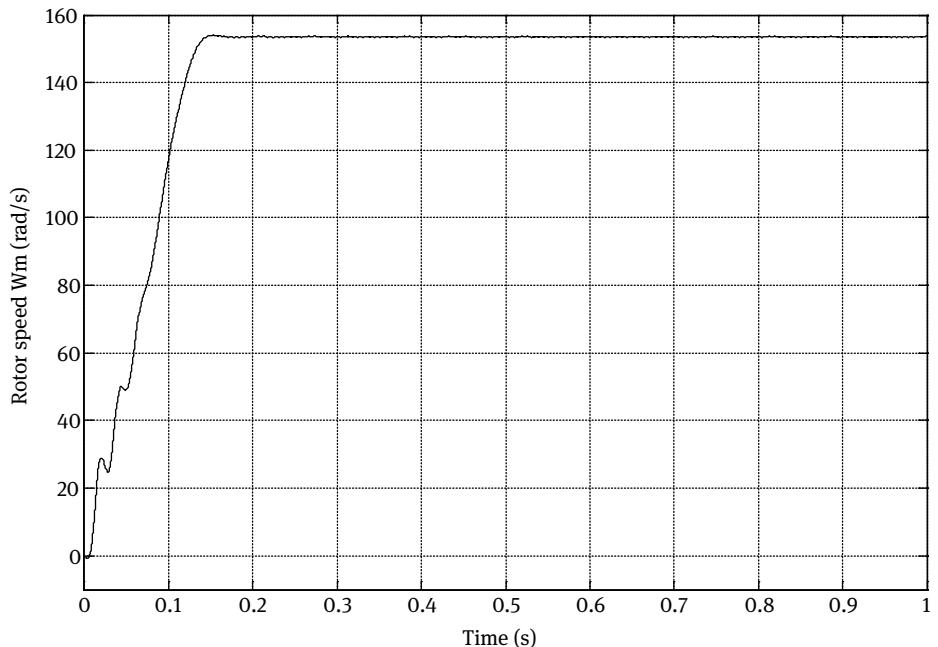


Fig. 6.9: Speed response of the two-level inverter fed induction motor.

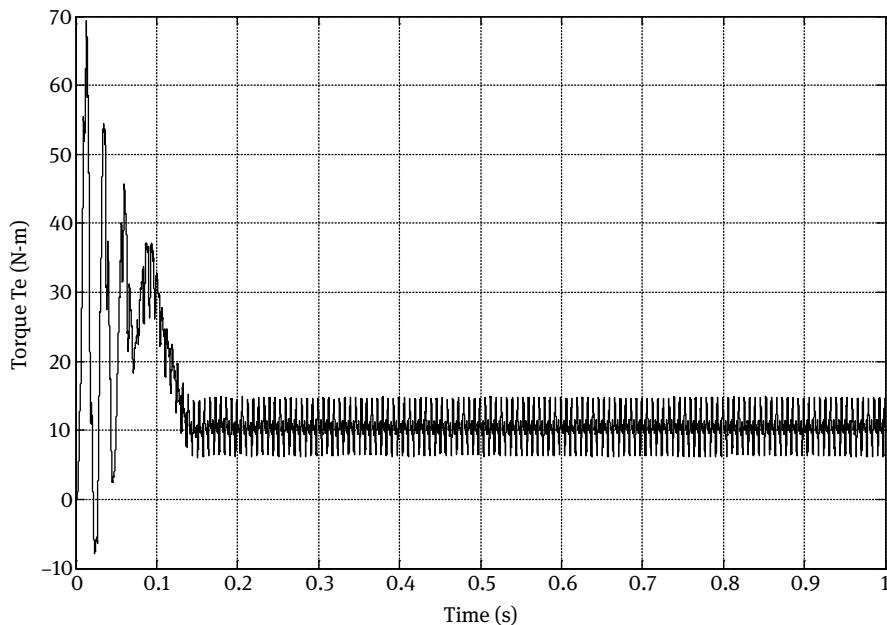


Fig. 6.10: Torque response of the two-level inverter fed induction motor.

6.3.2 Three-level inverter

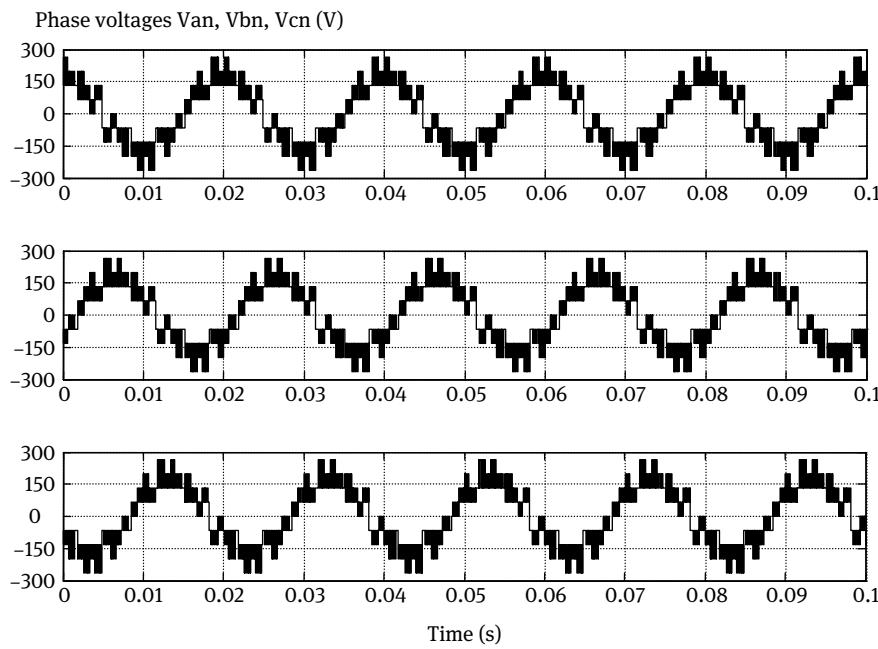


Fig. 6.11: Phase voltages of the three-level inverter.

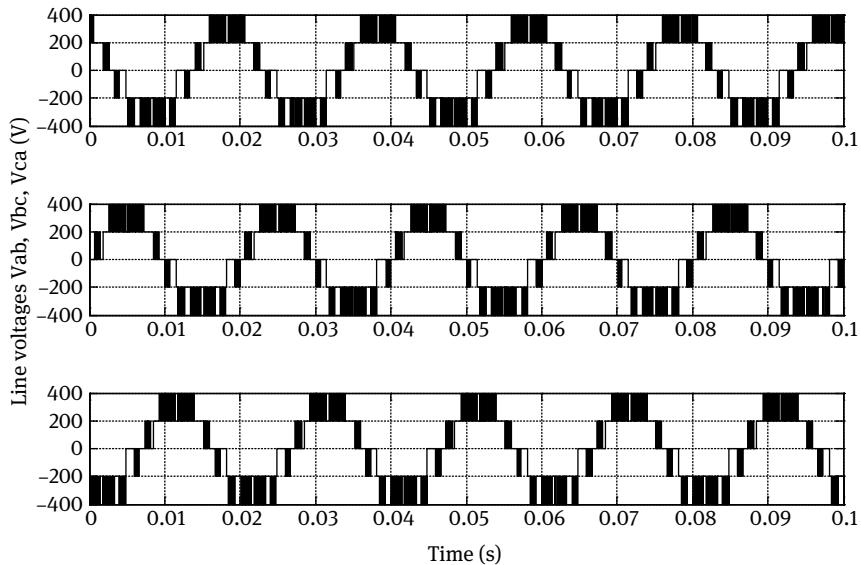


Fig. 6.12: Line-to-voltages of the three-level inverter.

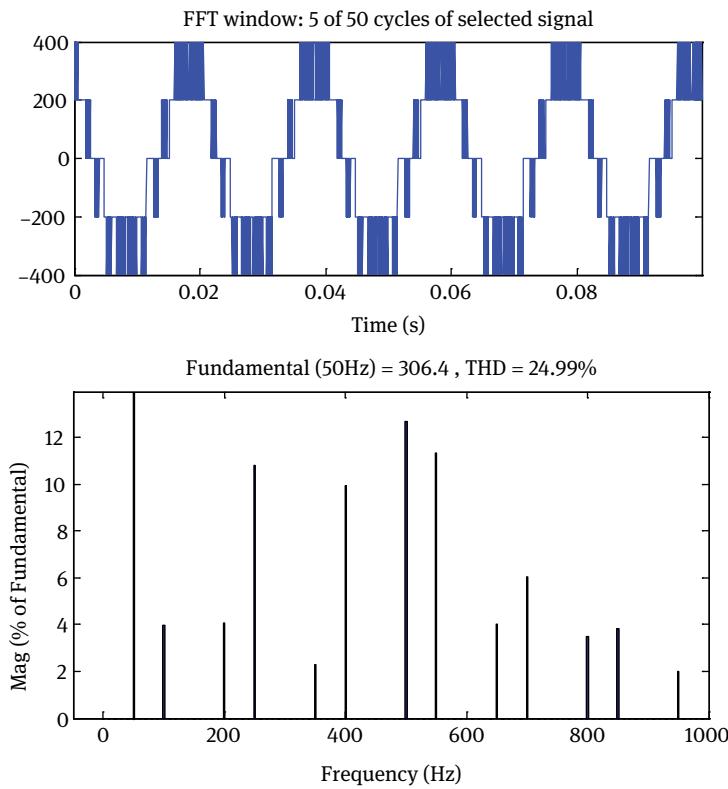


Fig. 6.13: Output line voltage (and its harmonic spectrum) of the three-level inverter.

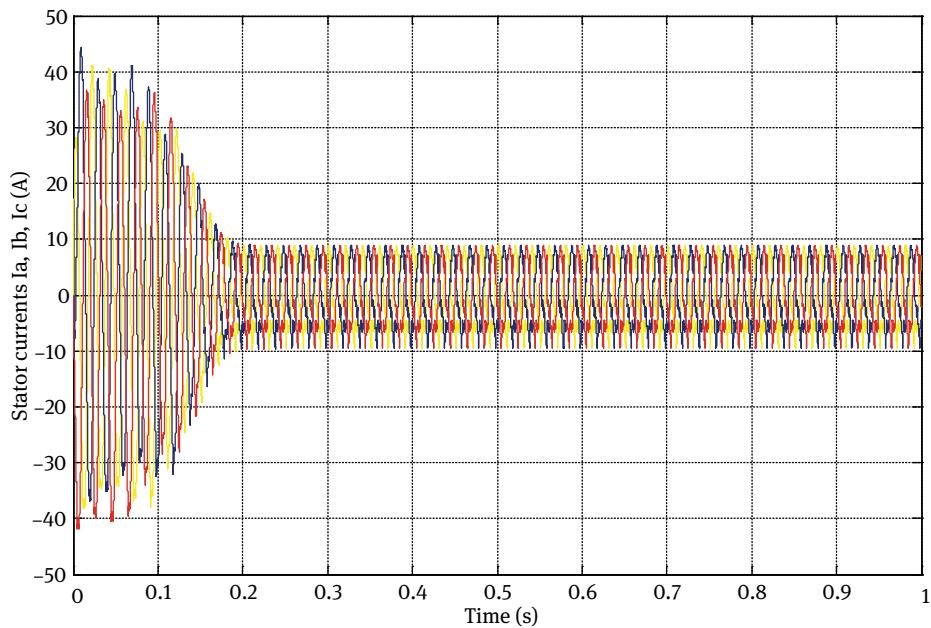


Fig. 6.14: Stator currents of the three-level inverter fed induction motor.

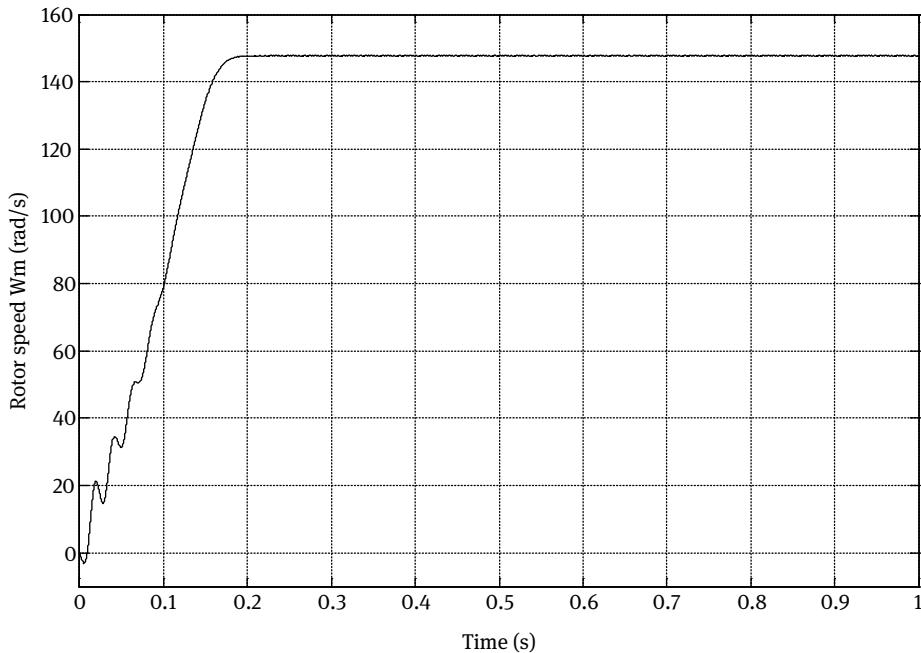


Fig. 6.15: Speed response of the three-level inverter fed induction motor.

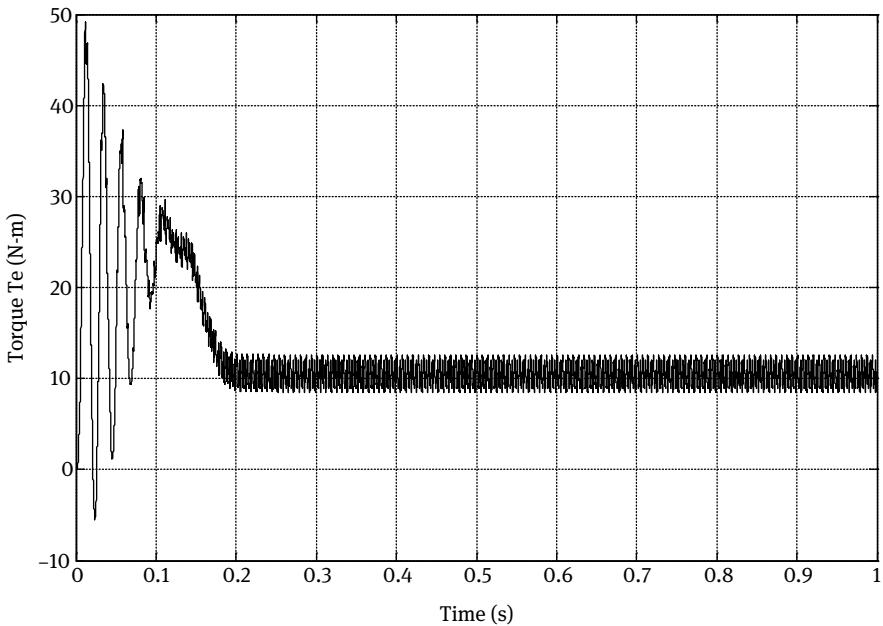


Fig. 6.16: Torque response of the three-level inverter fed induction motor.

6.3.3 Four-level inverter

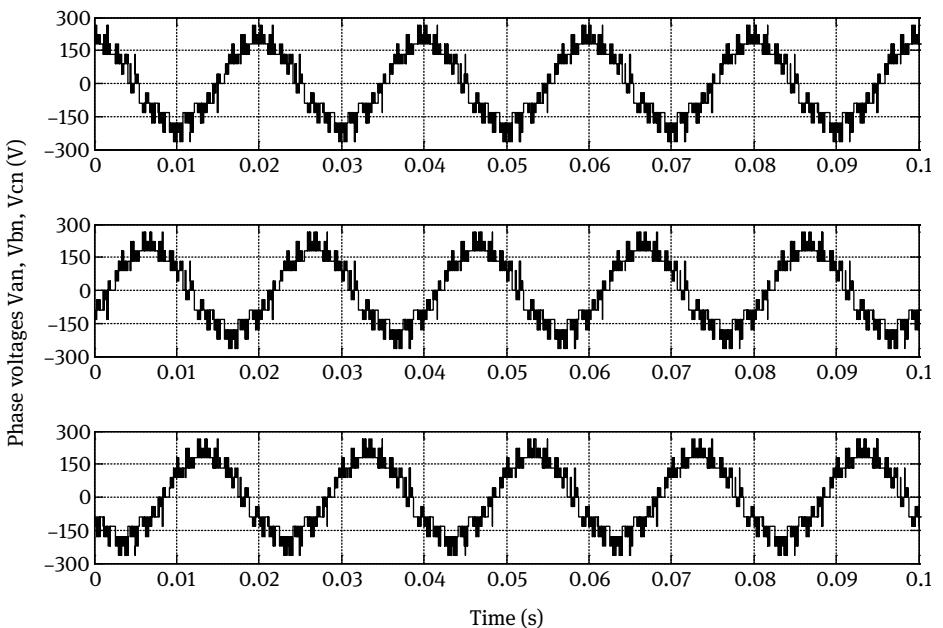


Fig. 6.17: Phase voltages of the four-level inverter.

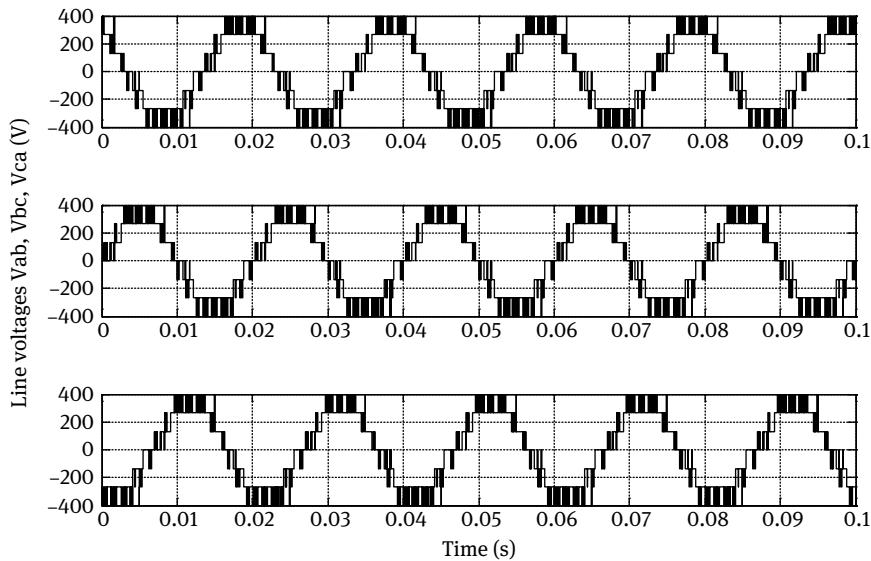


Fig. 6.18: Line-to-line voltages of the four-level inverter.

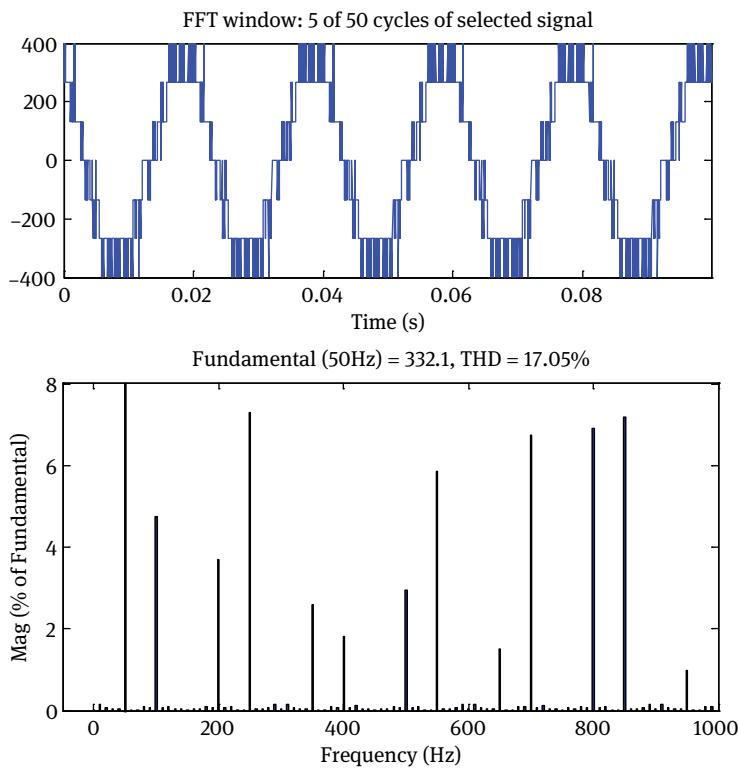


Fig. 6.19: Output line voltage (and its harmonic spectrum) of the four-level inverter.

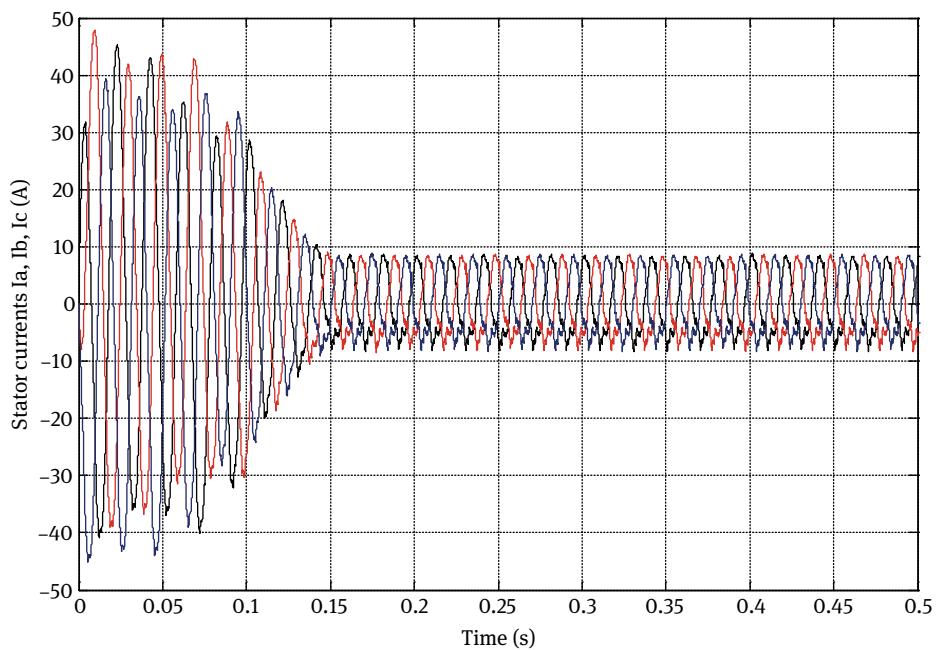


Fig. 6.20: Stator currents of the four-level inverter fed induction motor.

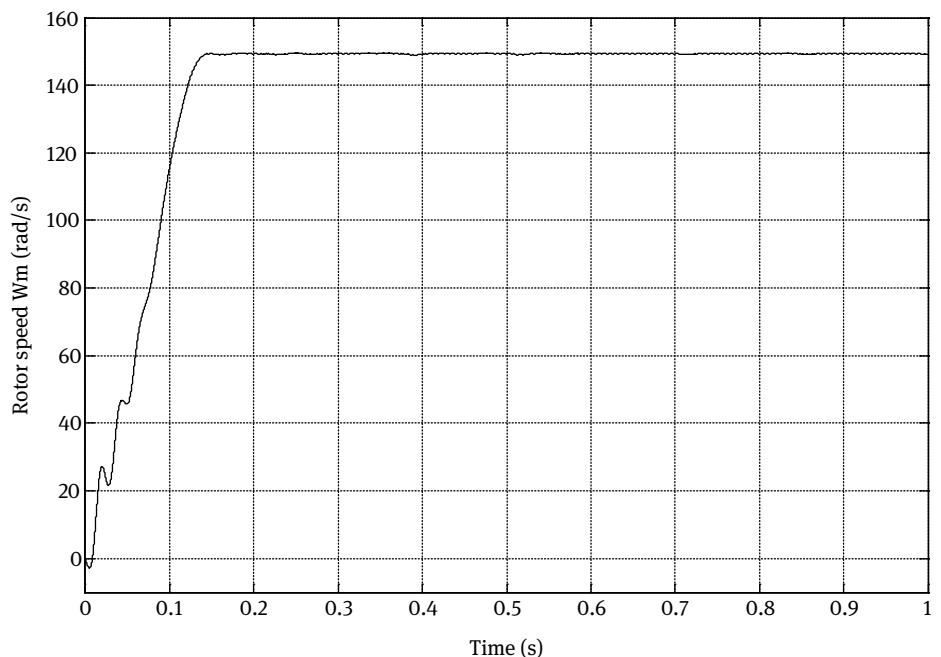


Fig. 6.21: Speed response of the four-level inverter fed induction motor.

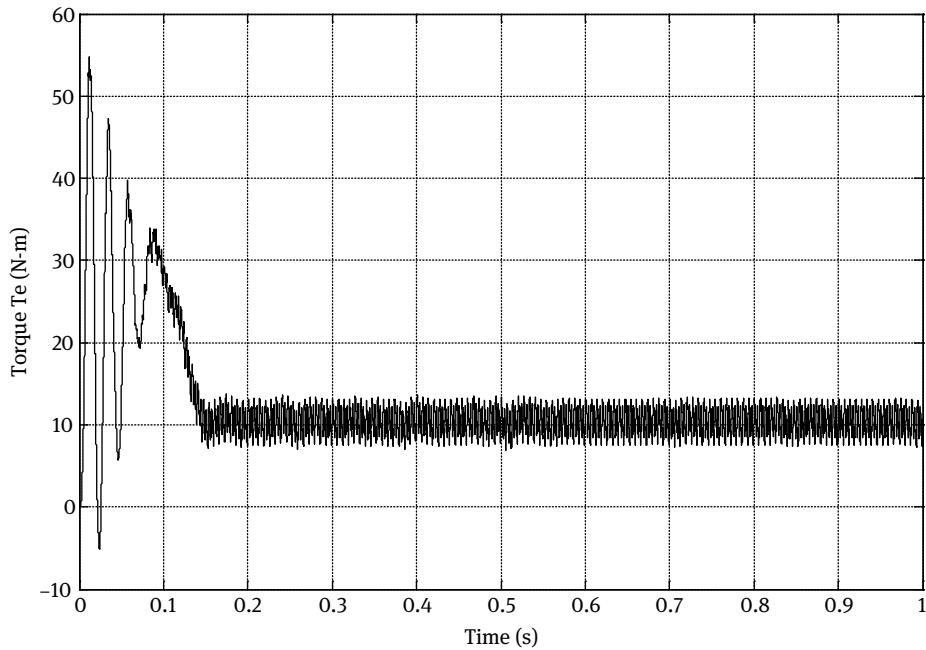


Fig. 6.22: Torque response of the four-level inverter fed induction motor.

6.3.4 Five-level inverter

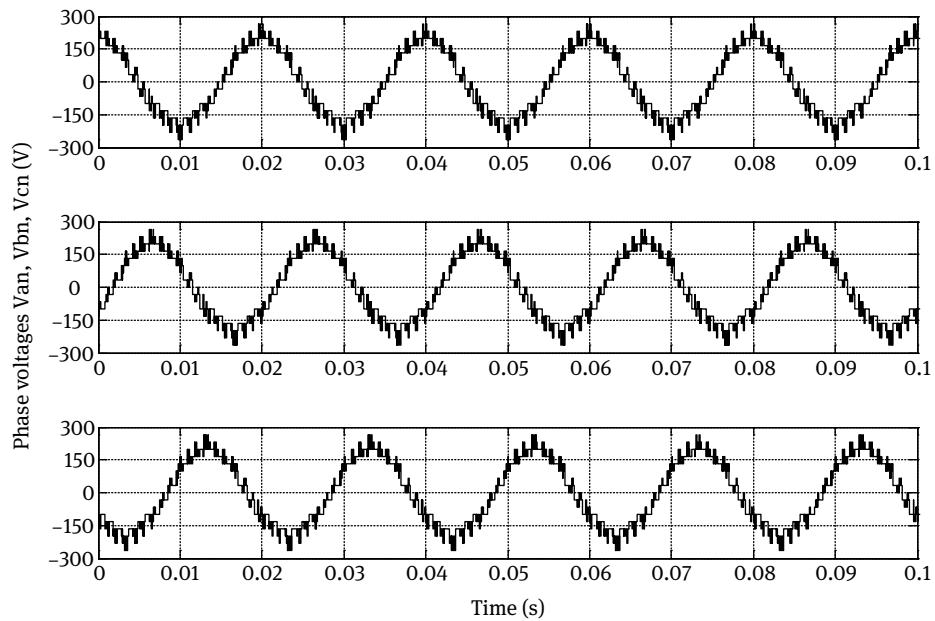


Fig. 6.23: Phase voltages of the five-level inverter.

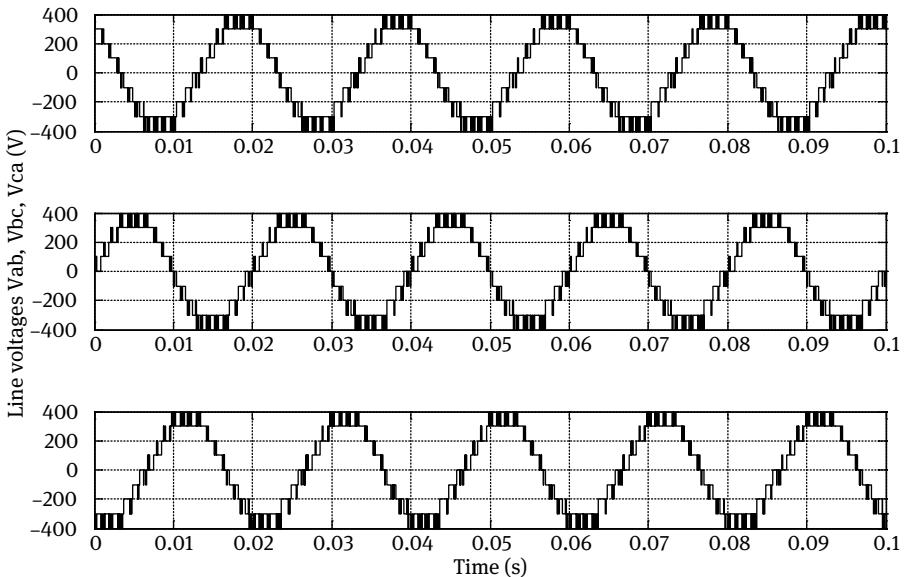


Fig. 6.24: Line-to-line voltages of the five-level inverter.

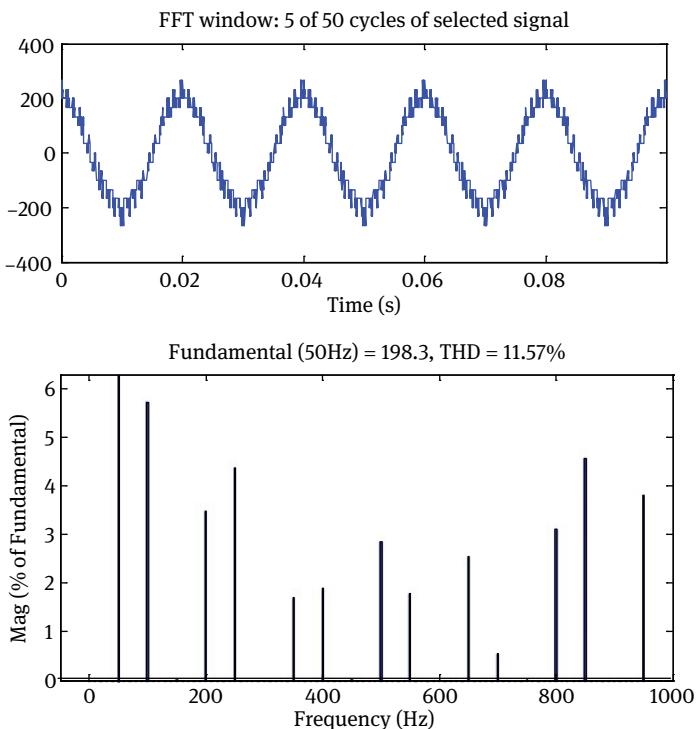


Fig. 6.25: Output line voltage (and its harmonic spectrum) of the five-level inverter.

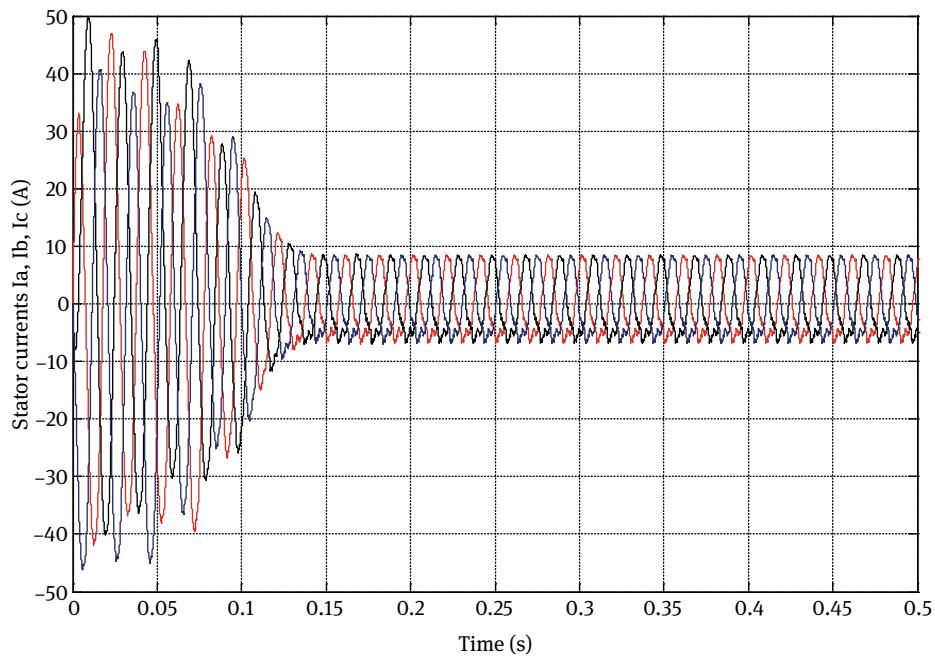


Fig. 6.26: Stator currents of the five-level inverter fed induction motor.

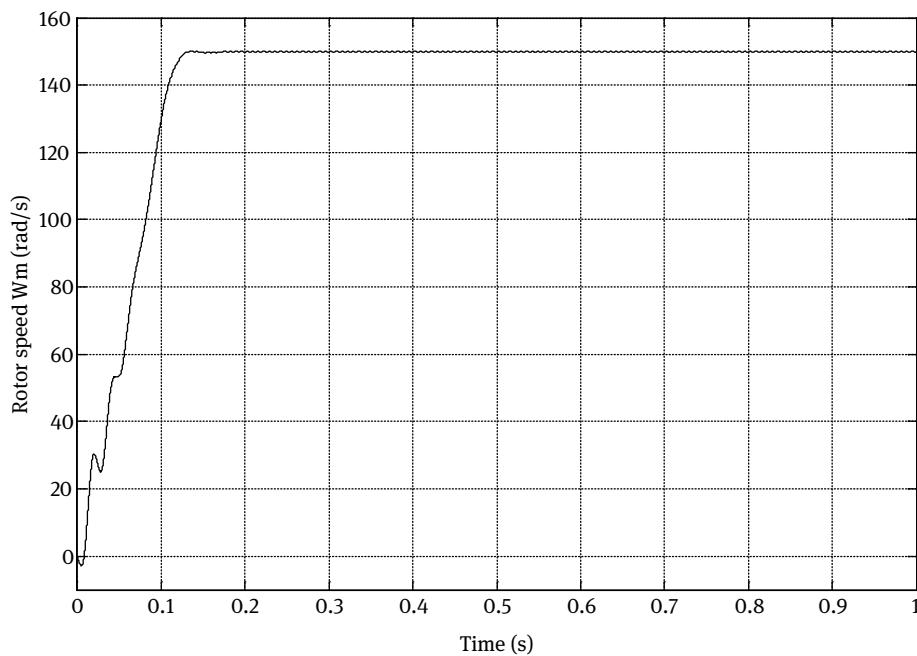


Fig. 6.27: Speed response of the five-level inverter fed induction motor.

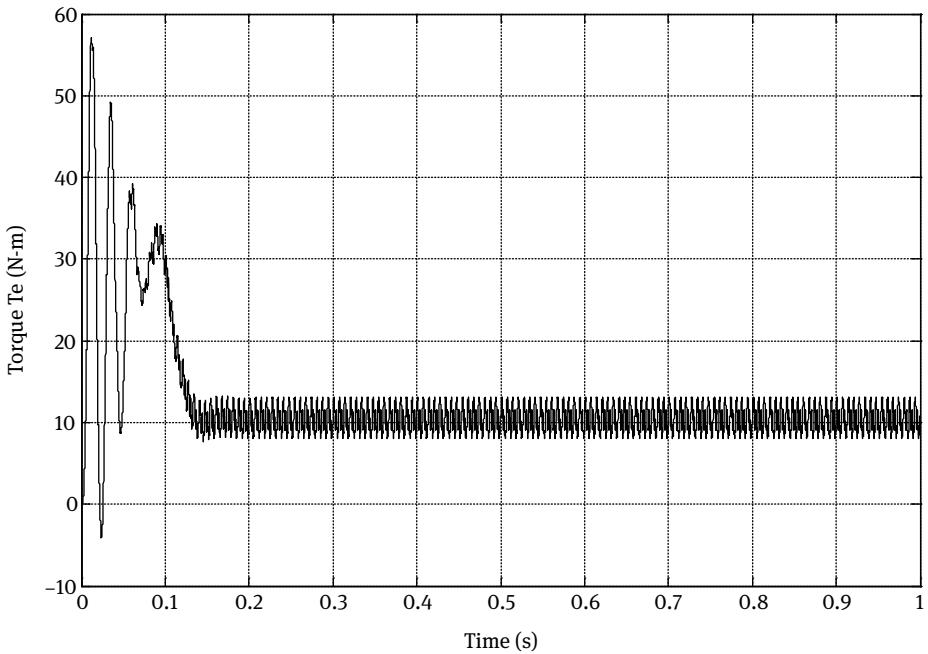


Fig. 6.28: Torque response of the five-level inverter fed induction motor.

6.3.5 Six-level inverter

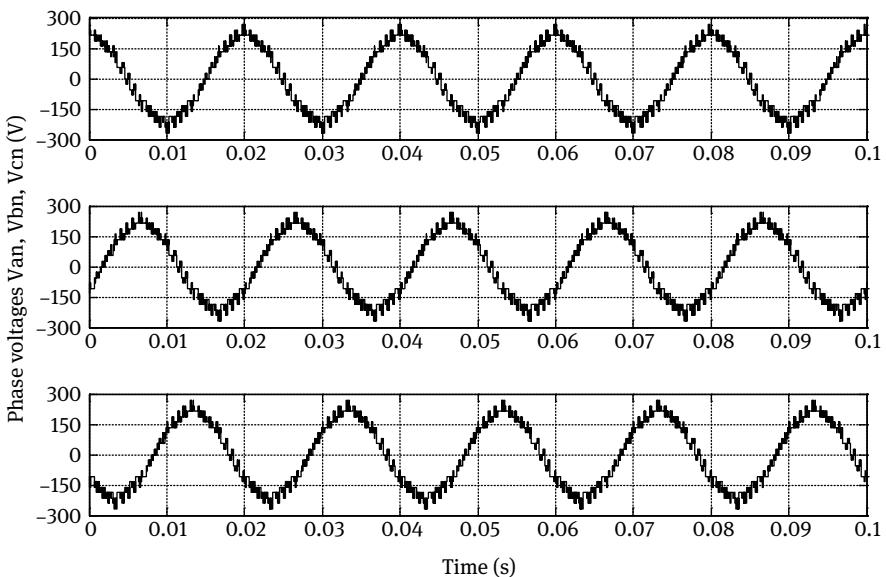


Fig. 6.29: Phase voltages of the six-level inverter.

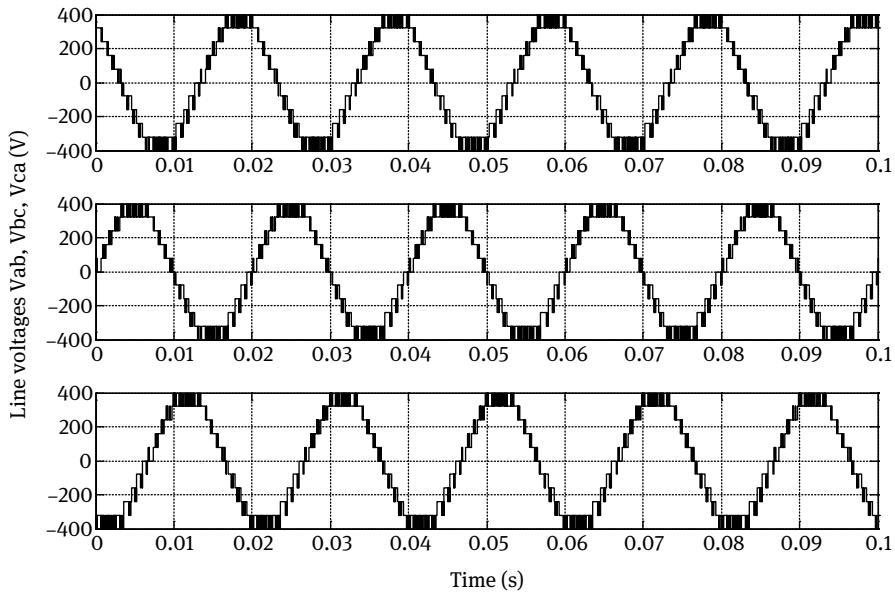


Fig. 6.30: Line-to-line voltages of the six-level inverter.

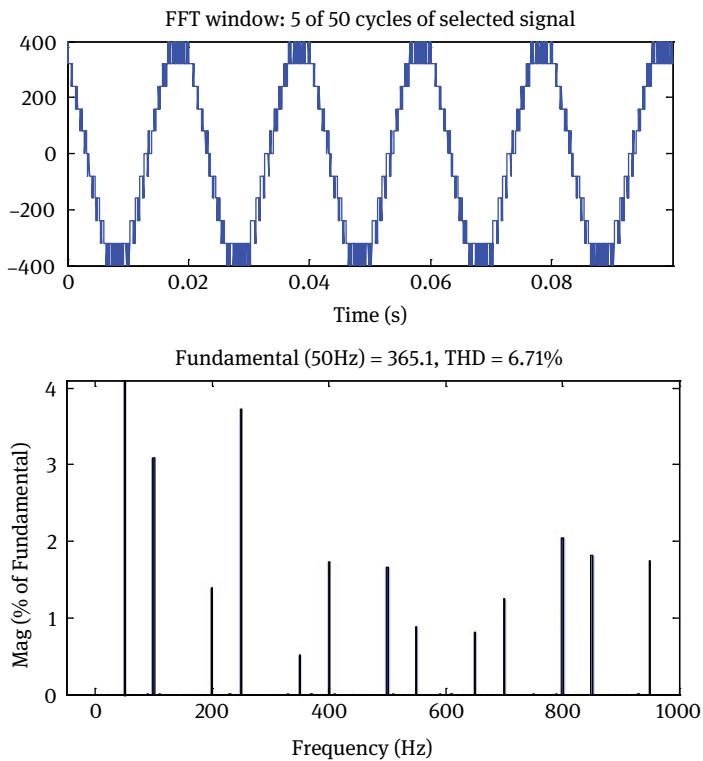


Fig. 6.31: Output line voltage (and its harmonic spectrum) of the six-level inverter.

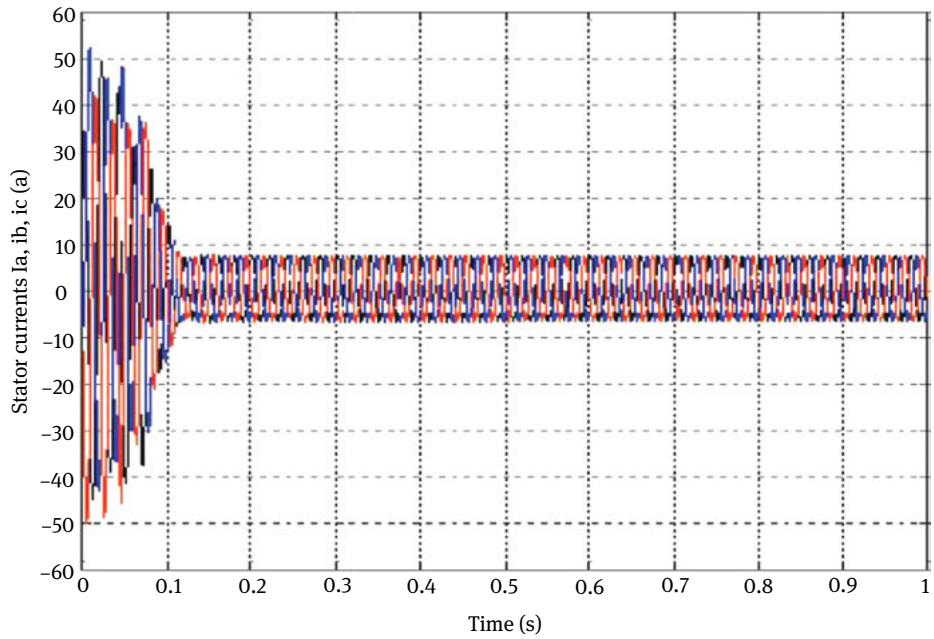


Fig. 6.32: Stator currents of the six-level inverter fed induction motor.

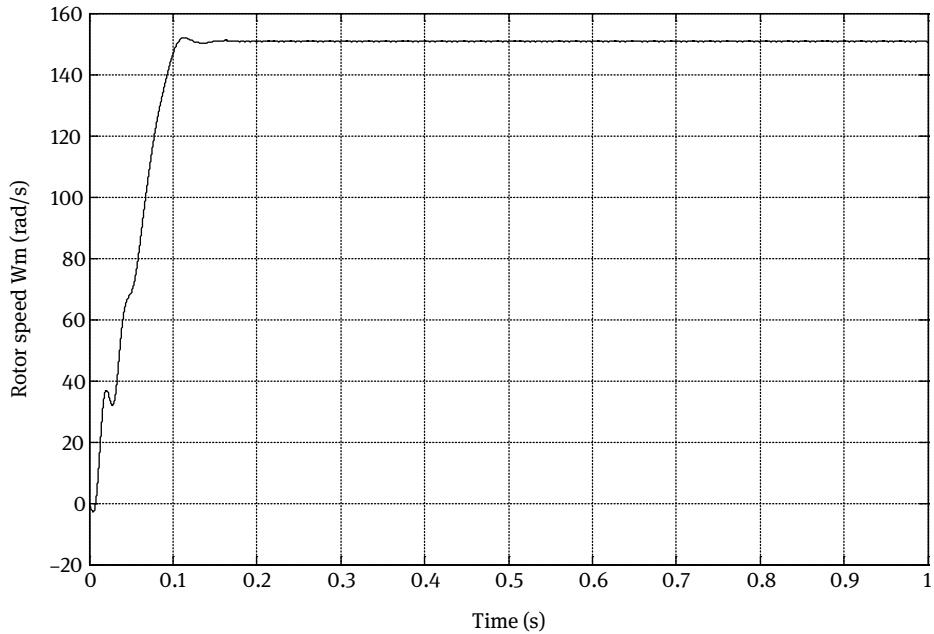


Fig. 6.33: Speed response of the six-level inverter fed induction motor.

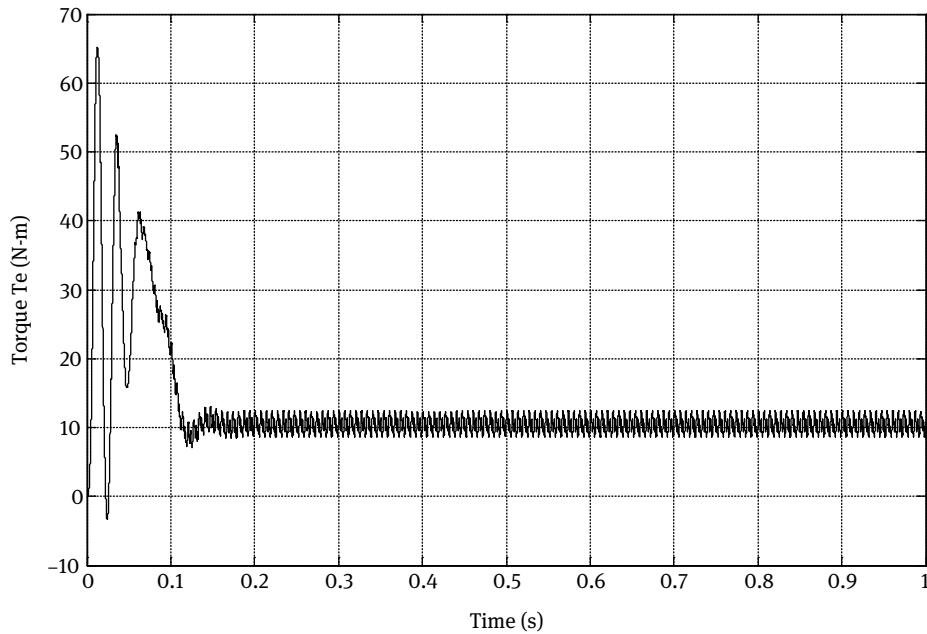


Fig. 6.34: Torque response of the six-level inverter fed induction motor.

6.3.6 Seven-level inverter

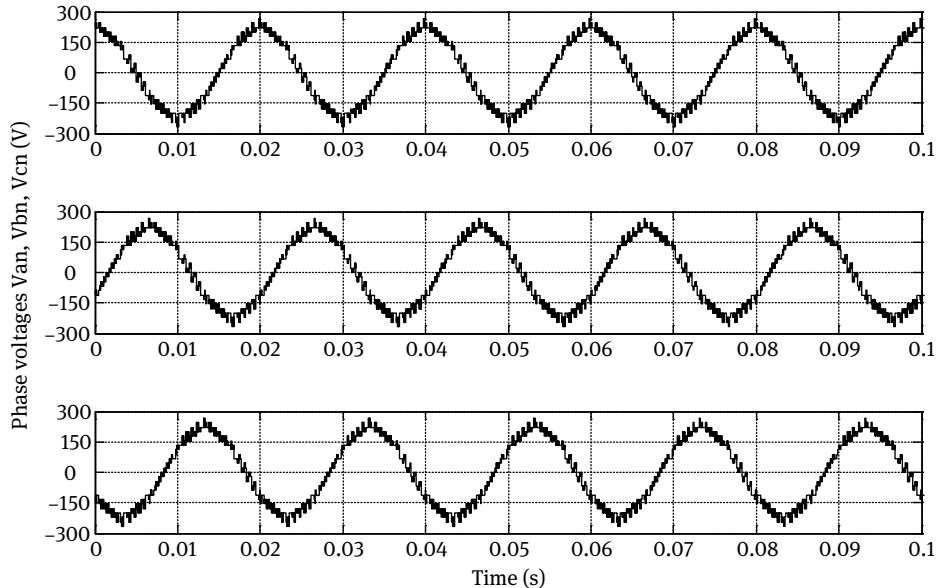


Fig. 6.35: Phase voltages of the seven-level inverter.

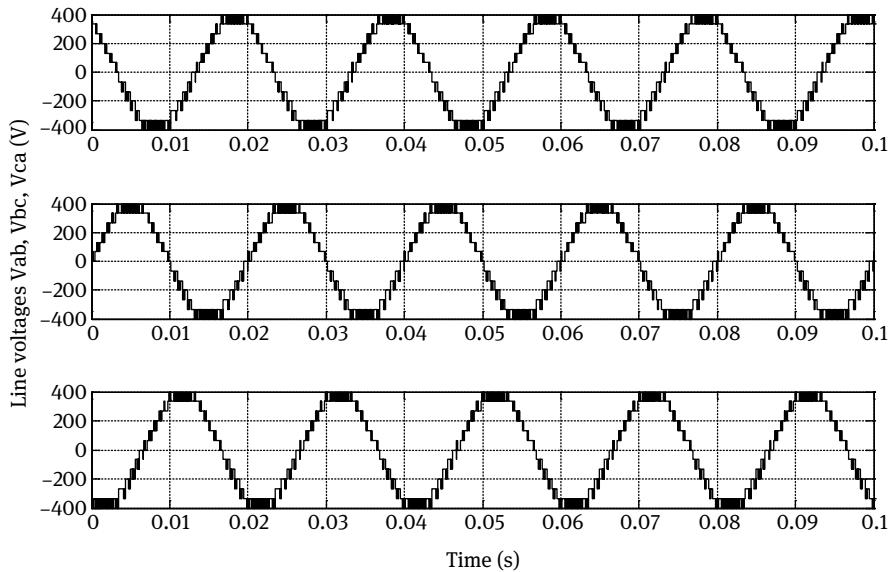


Fig. 6.36: Line-to-line voltages of the seven-level inverter.

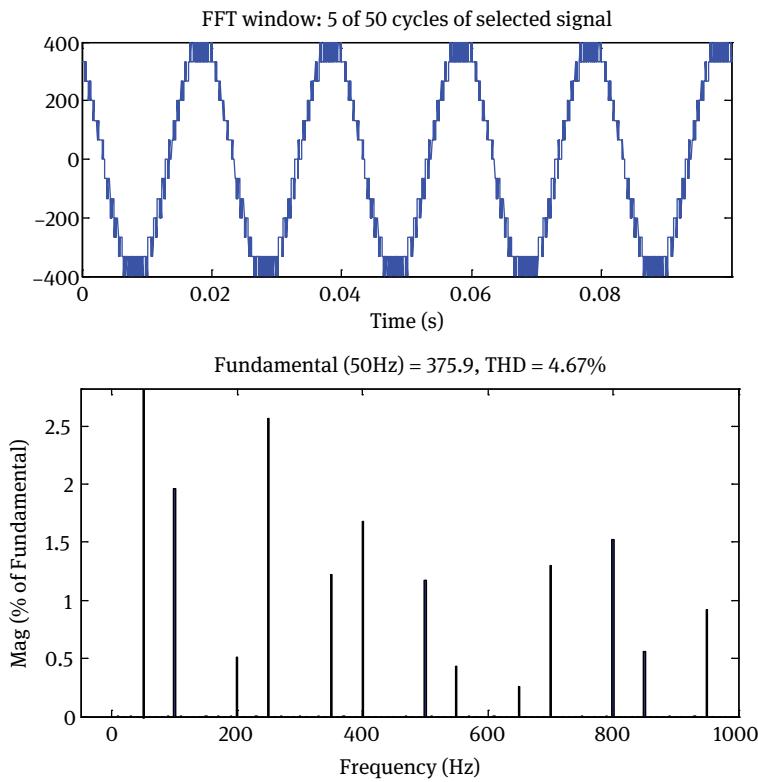


Fig. 6.37: Output line voltage (and its harmonic spectrum) of the seven-level inverter.

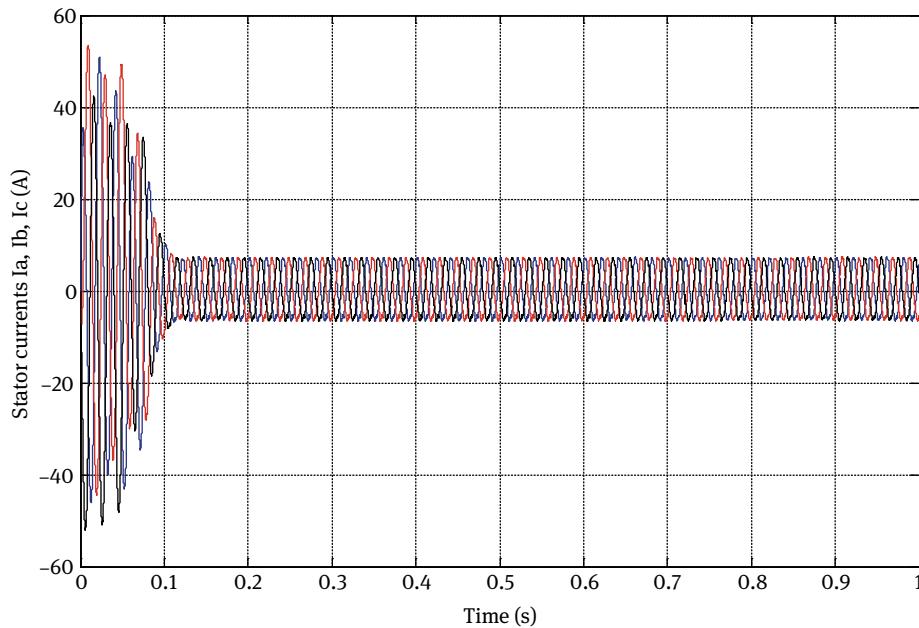


Fig. 6.38: Stator currents of the seven-level inverter fed induction motor.

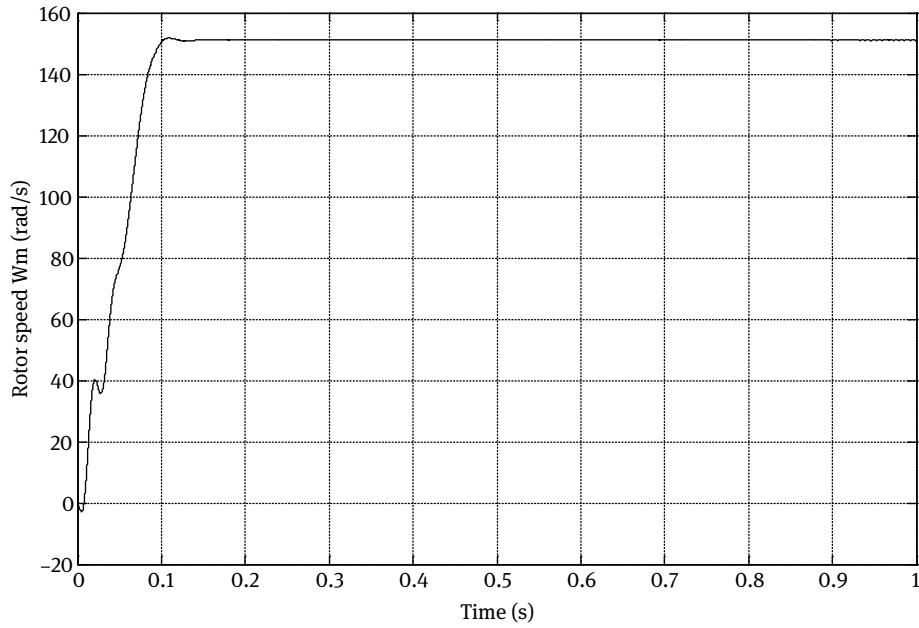


Fig. 6.39: Speed response of the seven-level inverter fed induction motor.

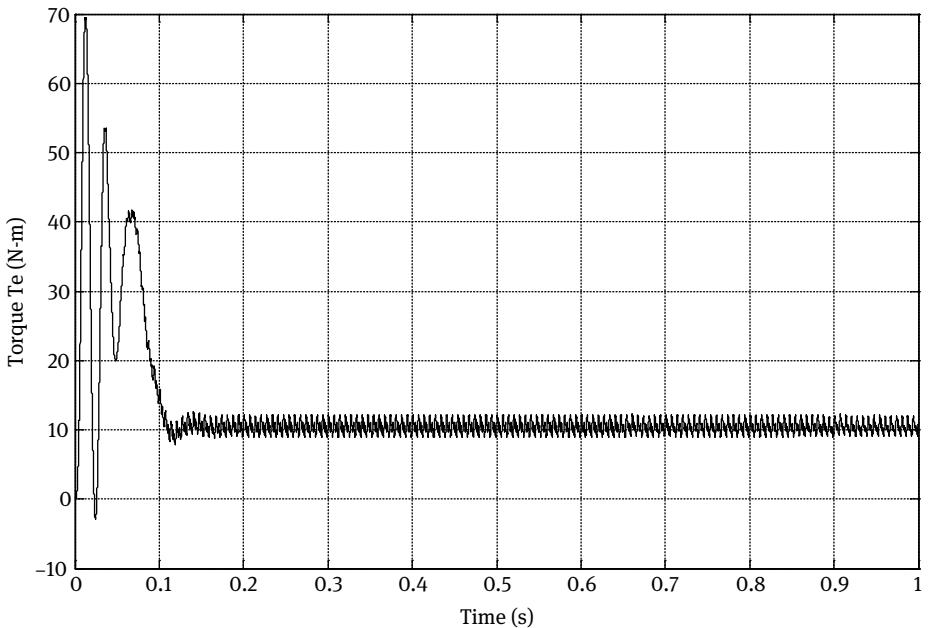


Fig. 6.40: Torque response of the seven-level inverter fed induction motor.

Tab. 6.3: THD of multilevel inverters.

Inverter	THD (%)
Two-level inverter	42.48
Three-level inverter	24.99
Four-level inverter	17.05
Five-level inverter	11.57
Six-level inverter	6.71
Seven-level inverter	4.67

6.4 Conclusions

In this chapter, a qualitative SVPWM algorithm has been proposed and described for the three, four, five, six and seven-level inverters. In this proposed scheme, the duty cycles of the reference voltage vectors are corrected to identify the location of the reference voltage vector easily in each region. The appropriate switching sequence of the region and dwelling time calculation are also proposed. The results have been presented and analyzed, which show that the generated voltage spectrum is very much

improved with the increase in the level of inverter. The THD is highly reduced as the level of inverter increases. The input current drawn by the induction motor is less distorted as the level of inverter increases. The output voltage THD for the three-, four-, five-, six-, and seven-level inverters is 42.48%, 24.99%, 17.05%, 11.57%, 6.71%, and 4.67%, respectively, which is considerably lower than that of the same inverter using the other modulation techniques.

7 Space vector pulse width modulation for multilevel inverters using the decomposition method

In this chapter, the space vector pulse width modulation (SVPWM) algorithm for multilevel inverters using the decomposition method is presented. In this method, the space vector diagram of the multilevel inverter is decomposed into several space vector diagrams of the two-level inverters. The SVPWM algorithm using the decomposition method is applied for the seven-level inverter. In this method, the space vector diagram of the seven-level inverter is decomposed into six space vector diagrams of the four-level inverters. In turn, each of these six space vector diagrams of the four-level inverter is decomposed into six space vector diagrams of the three-level inverters, and each of these six space vector diagrams of the three-level inverter is decomposed into six space vector diagrams of the two-level inverters. To proceed with the switching state determination, first, one of these hexagons is selected based on the location of the target voltage vector. Second, the original voltage reference vector is decremented by the voltage vector that locates the origin of the selected two-level hexagon. This then allows the determination of switching sequence and calculation of the voltage vector duration to be done in the same manner as for a conventional two-level inverter. The proposed method reduces the algorithm complexity and execution time. It can be applied to the multilevel inverters above the seven-level inverter as well. This method has been explained in detail, and results have been presented and analyzed for the three-level, five-level, and seven-level inverters.

7.1 Seven-level inverter

Figure 7.1 shows the space vector diagram of the seven-level inverter. The seven-level diode clamping inverter diagram is shown in Fig. 7.2. Each leg is composed of six upper and lower switches with anti-parallel diodes. Six series dc-link capacitors split the dc bus voltage in half, and 36 clamping diodes confine the voltages across the switches within the voltages of the capacitors. The necessary conditions for the switching states for the seven-level inverter are that the dc-link capacitors should not be shorted, and the output current should be continuous [98].

The three dc voltages are labeled as V_{dc1} , V_{dc2} , and V_{dc3} to distinguish them in the inverter output, although in most of the cases, $V_{dc1} = V_{dc2} = V_{dc3}$. The phase leg switch states required to achieve the seven output levels can be determined by connecting, for example, phase leg b to the negative dc bus by triggering all switches in the lower

portion of its phase leg. Then, the phase leg a output voltage with respect to the negative dc rail, V_{an} , can be identified for various switch combinations, as shown in Tab. 7.1.

Tab. 7.1: Switching states and current path for the seven-level inverter.

Switch state	Phase a voltage V_{an}	Devices tuned ON	Current path with I_a positive	Current path with I_a negative
1	$V_{an} = 0$	T_{a1} to T_{a6}	$T_{a6} > T_{a5} > T_{a4} > T_{a3} > T_{a2} > T_{a1}$	$T_{a6} > T_{a5} > T_{a4} > T_{a3} > T_{a2} > T_{a1}$
2	$V_{an} = V_{dc3}$	T_{a2} to T_{a7}	$D_{a7} > T_{a7}$	$T_{a6} > T_{a5} > T_{a4} > T_{a3} > T_{a2} > D_{a2}$
3	$V_{an} = V_{dc3} + V_{dc2}$	T_{a3} to T_{a8}	$D_{a8} > T_{a8} > T_{a7}$	$T_{a6} > T_{a5} > T_{a4} > T_{a3} > D_{a3}$
4	$V_{an} = V_{dc3} + V_{dc2} + V_{dc1}$	T_{a4} to T_{a9}	$D_{a9} > T_{a9} > T_{a8} > T_{a7}$	$T_{a6} > T_{a5} > T_{a4} > D_{a4}$
5	$V_{an} = V_{dc3} + V_{dc2} + 2V_{dc1}$	T_{a5} to T_{a10}	$D_{a10} > T_{a10} > T_{a9} > T_{a8} > T_{a7}$	$T_{a6} > T_{a5} > D_{a5}$
6	$V_{an} = V_{dc3} + 2(V_{dc2} + V_{dc1})$	T_{a6} to T_{a11}	$D_{a11} > T_{a11} > T_{a10} > T_{a9} > T_{a8} > T_{a7}$	$T_{a6} > D_{a6}$
7	$V_{an} = 2(V_{dc3} + V_{dc2} + V_{dc1})$	T_{a7} to T_{a12}	$T_{a12} > T_{a11} > T_{a10} > T_{a9} > T_{a8} > T_{a7}$	$T_{a7} > T_{a8} > T_{a9} > T_{a10} > T_{a11} > T_{a12}$

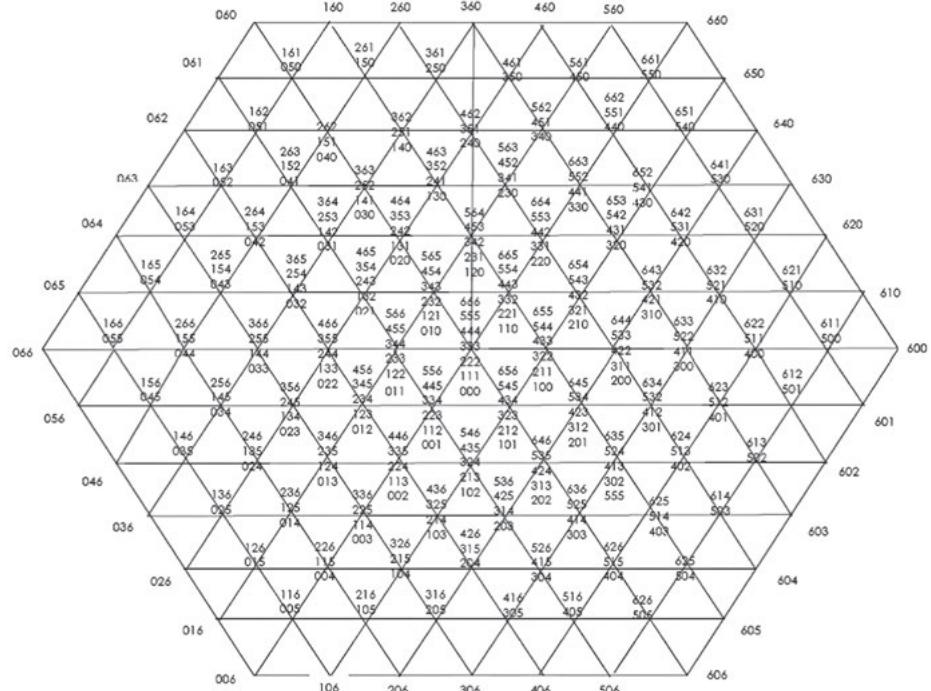


Fig. 7.1: Space vector diagram of the seven-level inverter.

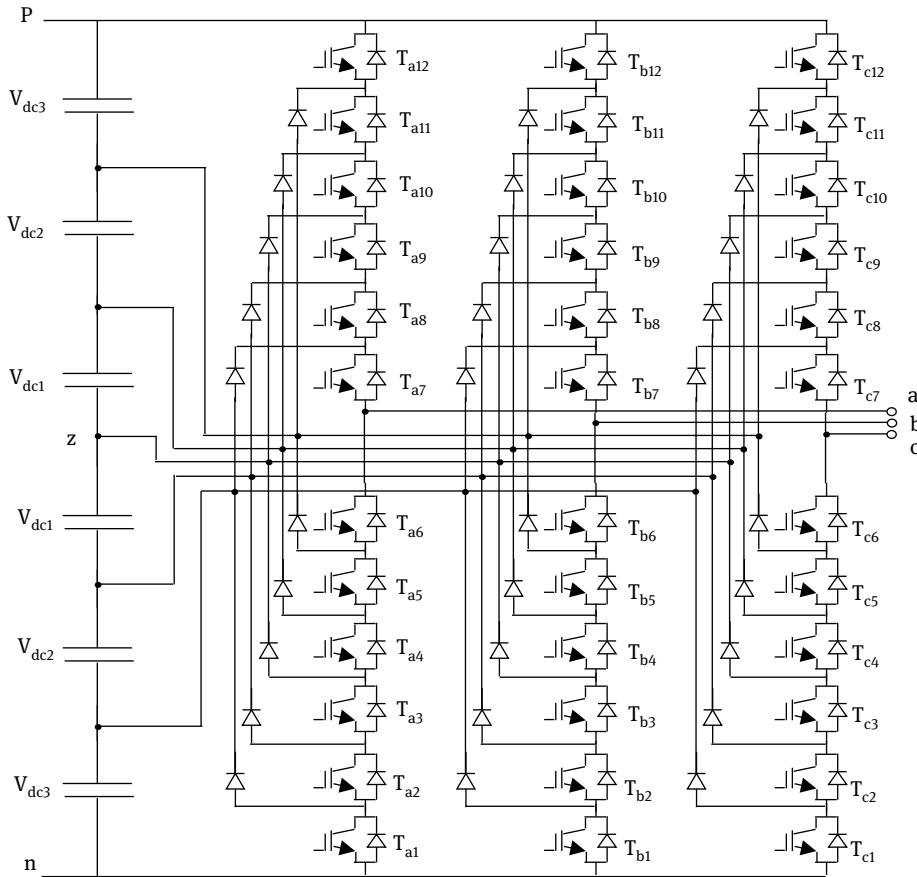


Fig. 7.2: Seven-level NPC inverter topology.

7.2 SVPWM algorithm using the decomposition method

7.2.1 Basic principle of the decomposition method

The space vector diagram of the multilevel inverter can be divided into different forms of subdiagrams in such a manner that the space vector modulation becomes simpler and easier to implement. The decomposition method is a simple and fast one that divides the space vector diagram of the seven-level inverter, within three steps, into several small hexagons, each hexagon being space vector diagram of the two-level inverter, as shown in Figs. 7.3 to 7.5. Thus, the space vector diagram

of the seven-level inverter becomes very simple and similar to that of conventional two-level space vector diagram. This simplification of multilevel space vector diagram into two-level space vector diagram can be done in two steps. At first, one

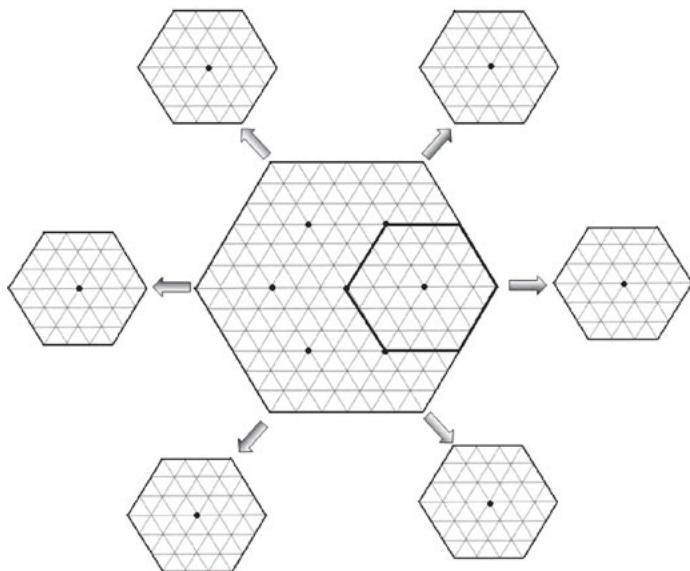


Fig. 7.3: Decomposition of the space vector diagram of the seven-level inverter into the space vector diagram of the four-level inverter.

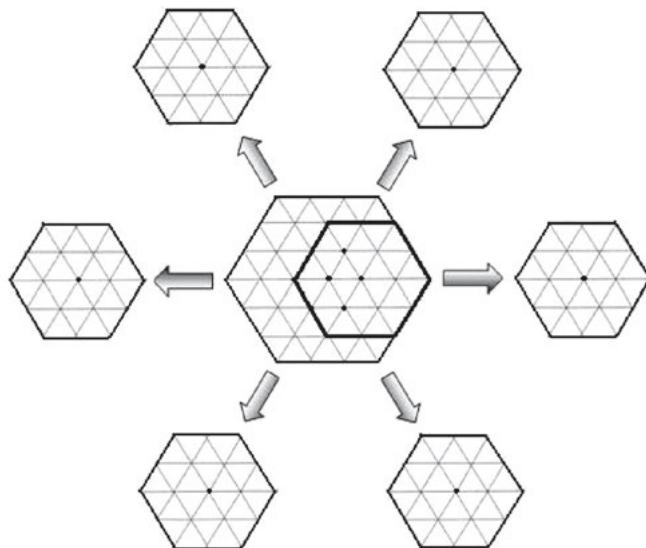


Fig. 7.4: Decomposition of the space vector diagram of the four-level inverter into the space vector diagram of the three-level inverter

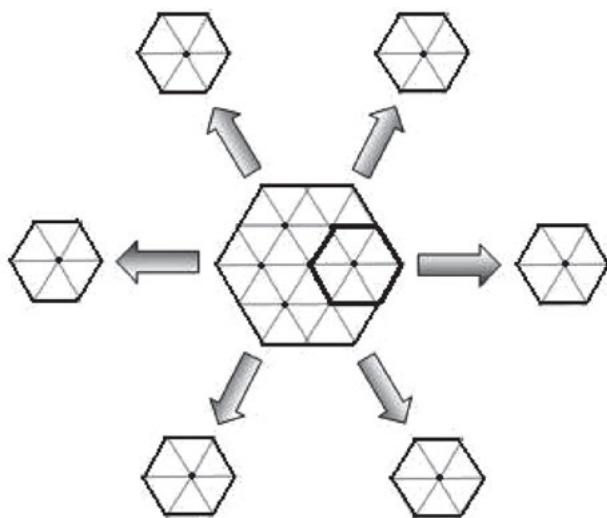


Fig. 7.5: Decomposition of the space vector diagram of the three-level inverter into the space vector diagram of the two-level inverter.

hexagon has to be selected based on the location of the reference voltage vector. Second, the translation of the origin of the reference voltage vector has to be done toward the center of the selected hexagon.

7.2.2 First correction of the reference voltage vector

After finding the location of a given reference voltage vector, one hexagon has to be selected among the six small hexagons that contain the seven-level space vector diagram, as shown in Fig. 7.3. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided equally between the two hexagons, as shown in Fig. 7.6. Each hexagon is identified by a number's' defined as given in Tab. 7.2.

Tab. 7.2: Selection of hexagon based on the reference angle (θ).

Hexagon S	Location of the reference voltage vector phase angle θ
1	$-\pi/6 < \theta < \pi/6$
2	$\pi/6 < \theta < \pi/2$
3	$\pi/2 < \theta < 5\pi/6$
4	$5\pi/6 < \theta < 7\pi/6$
5	$7\pi/6 < \theta < 3\pi/2$
6	$3\pi/2 < \theta < -\pi/6$

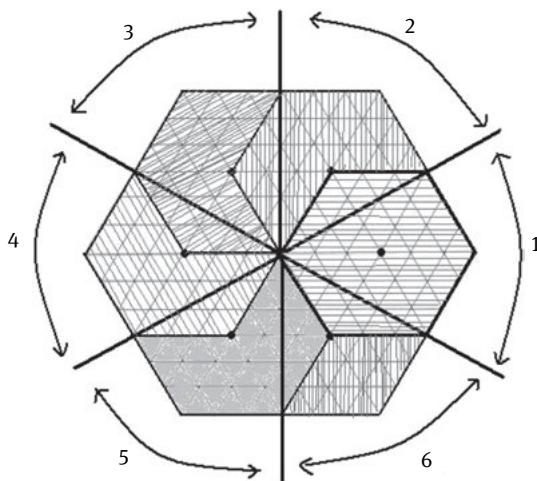


Fig. 7.6: Division of overlapped regions.

After selecting one hexagon, the translation of the reference vector V^{7*} has to be done toward the center of this hexagon, as indicated in Fig. 7.7. This translation is done by subtracting the center vector of the selected hexagon from the original reference

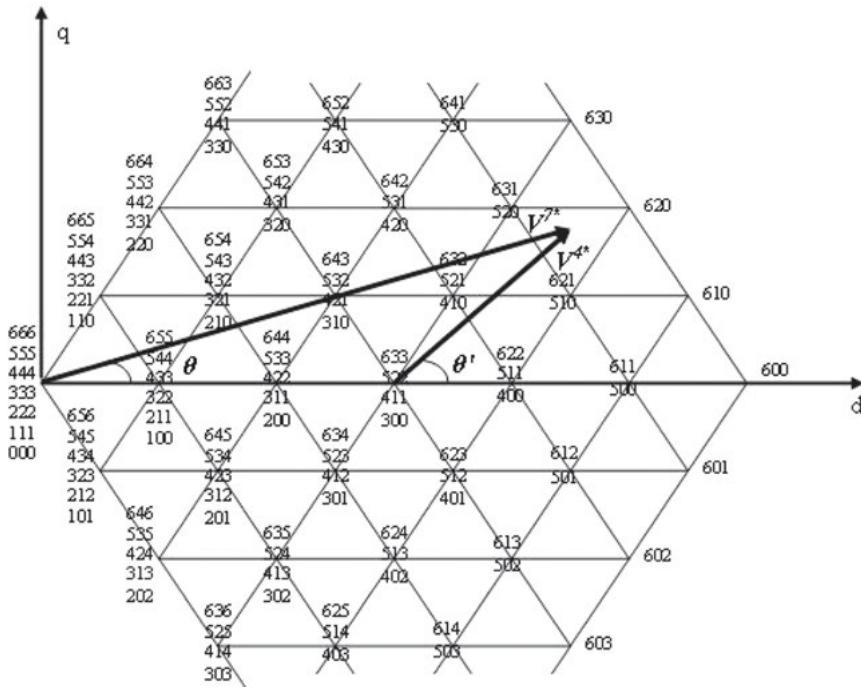


Fig. 7.7: First translation of the reference voltage vector.

vector. Table 7.3 gives the components d and q of the reference voltage V^{4*} after translation, for all the six hexagons. Index (3), (4), or (7) above the components indicate three-, four-, or seven-level cases, respectively.

Tab. 7.3: First correction of the reference voltage vector.

S	V_d^{4*}	V_q^{4*}
1	$V_d^{7*} - \frac{1}{2}\cos(0^0)$	$V_q^{7*} - \frac{1}{2}\sin(0^0)$
2	$V_d^{7*} - \frac{1}{2}\cos(\pi/3)$	$V_q^{7*} - \frac{1}{2}\sin(\pi/3)$
3	$V_d^{7*} - \frac{1}{2}\cos(2\pi/3)$	$V_d^{7*} - \frac{1}{2}\sin(2\pi/3)$
4	$V_d^{7*} - \frac{1}{2}\cos(\pi)$	$V_d^{7*} - \frac{1}{2}\sin(\pi)$
5	$V_d^{7*} - \frac{1}{2}\cos(4\pi/3)$	$V_d^{7*} - \frac{1}{2}\sin(4\pi/3)$
6	$V_d^{7*} - \frac{1}{2}\cos(5\pi/3)$	$V_d^{7*} - \frac{1}{2}\sin(5\pi/3)$

7.2.3 Second correction of the reference voltage vector

Having the selected four-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this four-level diagram, as shown in Fig. 7.4. Here, the overlapped regions are equally divided between the two hexagons. After the selection of one hexagon, we translate the reference vector V^{4*} toward the center of this hexagon, as indicated in Fig. 7.8.

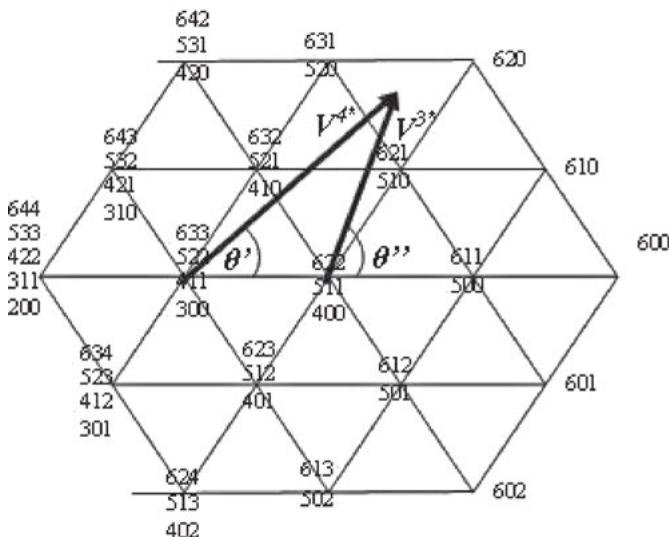


Fig. 7.8: Second translation of the reference voltage vector.

This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 7.4 gives the components d and q of the reference voltage V^{3*} after translation, for all the six hexagons.

Tab. 7.4: Second correction of the reference voltage vector.

S	V_d^{3*}	V_q^{3*}
1	$V_d^{4*} - \frac{1}{6}\cos(0^\circ)$	$V_q^{4*} - \frac{1}{6}\sin(0^\circ)$
2	$V_d^{4*} - \frac{1}{6}\cos(\pi/3)$	$V_q^{4*} - \frac{1}{6}\sin(\pi/3)$
3	$V_d^{4*} - \frac{1}{6}\cos(2\pi/3)$	$V_q^{4*} - \frac{1}{6}\sin(2\pi/3)$
4	$V_d^{4*} - \frac{1}{6}\cos(\pi)$	$V_q^{4*} - \frac{1}{6}\sin(\pi)$
5	$V_d^{4*} - \frac{1}{6}\cos(4\pi/3)$	$V_q^{4*} - \frac{1}{6}\sin(4\pi/3)$
6	$V_d^{4*} - \frac{1}{6}\cos(5\pi/3)$	$V_q^{4*} - \frac{1}{6}\sin(5\pi/3)$

7.2.4 Third correction of the reference voltage vector

After selection of the three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram, as shown in Fig. 7.5. Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, the translation of the reference vector V^{3*} has to be done toward the center of this hexagon, as indicated in Fig. 7.9.

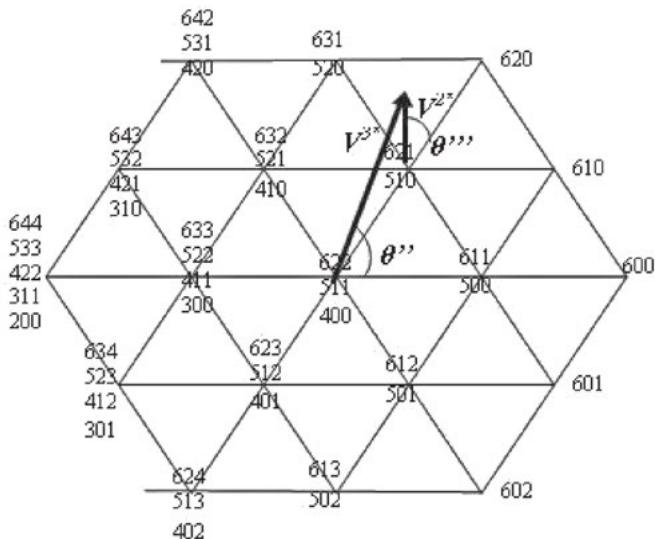


Fig. 7.9: Third translation of the reference voltage vector.

This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table 7.5 gives the components d and q of the reference voltage V^{2*} after translation, for all the six hexagons.

Tab. 7.5: Third correction of the reference voltage vector.

S	V_d^{2*}	V_q^{2*}
1	$V_d^{3*} - \frac{1}{6}\cos(0^\circ)$	$V_q^{3*} - \frac{1}{6}\sin(0^\circ)$
2	$V_d^{3*} - \frac{1}{6}\cos(\pi/3)$	$V_q^{3*} - \frac{1}{6}\sin(\pi/3)$
3	$V_d^{3*} - \frac{1}{6}\cos(2\pi/3)$	$V_q^{3*} - \frac{1}{6}\sin(2\pi/3)$
4	$V_d^{3*} - \frac{1}{6}\cos(\pi)$	$V_q^{3*} - \frac{1}{6}\sin(\pi)$
5	$V_d^{3*} - \frac{1}{6}\cos(4\pi/3)$	$V_q^{3*} - \frac{1}{6}\sin(4\pi/3)$
6	$V_d^{3*} - \frac{1}{6}\cos(5\pi/3)$	$V_q^{3*} - \frac{1}{6}\sin(5\pi/3)$

7.2.5 Determination of switching times

Once the corrected reference voltage V^{2*} and the corresponding hexagon are determined, we can apply the conventional two-level SVPWM method to calculate the dwelling times; the only difference between the two-level SVPWM and the five-level SVPWM is factor 6 appearing at the first two equations, as shown in Eq. (7.1). The remaining procedure is implemented like the conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

$$\begin{aligned}
 T_1 &= 6^* \left[\frac{\left| \vec{V}^{2*} \right| \cdot T_s \cdot \sin\left(\frac{\pi}{3} - \theta^{***}\right)}{\sin\left(\frac{\pi}{3}\right)} \right] \\
 T_2 &= 6^* \left[\frac{\left| \vec{V}^{2*} \right| \cdot T_s \cdot \sin(\theta^{***})}{\sin\left(\frac{\pi}{3}\right)} \right] \\
 T_0 &= T_s - T_1 - T_2
 \end{aligned} \tag{7.1}$$

7.2.6 Switching sequence

This process is implemented by first considering each four-level decomposed space vector diagram of seven-level space vector diagram based on the value of s. Second, each four-level space vector diagram is further decomposed into 6 three-level space vector diagrams. Finally, each three-level space vector diagram is further decomposed

into 6 two-level space vector diagrams, and the switching states of seven-level space vector diagram are changed into its equivalent two-level switching states. The optimum sequence of these three states is selected to minimize the total number of switching transitions and fully optimize the harmonic profile of the output voltage. Note that from the two-level space vector modulation theory, it is well known that these sequences should be reversed in the next switching interval for minimum harmonic impact.

7.3 Results and discussions

The SVPWM algorithm for multilevel inverters using the decomposition method is proposed. In this method, the space vector diagram of multilevel inverter is decomposed into several space vector diagrams of the two-level inverters. The validity of the proposed method is verified for the three-, five-, and seven-level inverters by simulation. The simulation parameters and specifications of induction motor used in this method are given in Appendix IV. The results of the three-level inverter are shown in Figs. 7.10 to 7.16. The pole voltages, phase voltages, and line voltages are shown in Figs. 7.10 to 7.12, respectively. The stator currents, rotor speed, and torque of the three-level inverter fed induction motor are shown in Figs. 7.13 to 7.15, respectively. The output voltage harmonic spectrum and total harmonic distortion (THD) of the three-level inverter are shown in Fig. 7.16.

The results of the five-level inverter are shown in Figs. 7.17 to 7.23. The pole voltages, phase voltages, and line voltages are shown in Figs. 7.17 to 7.19, respectively. The stator currents, rotor speed, and torque of the five-level inverter fed induction motor are shown in Figs. 7.20 to 7.22, respectively. The output voltage harmonic spectrum and the THD of the five-level inverter are shown in Fig. 7.23. The results of the seven-level inverter are shown in Figs. 7.24 to 7.30. The pole voltages, phase voltages, and line voltages are shown in Figs. 7.24 to 7.26, respectively. The stator currents, rotor speed, and torque of the seven-level inverter fed induction motor are shown in Figs. 7.27 to 7.29, respectively. The output voltage harmonic spectrum and the THD of the five-level inverter are shown in Fig. 7.30. The obtained THD for the three-, five-, and seven-level inverters is 5.93%, 2.79%, and 1.51%, respectively, which is much less as compared with other conventional SVPWM techniques.

7.3.1 Three-level inverter

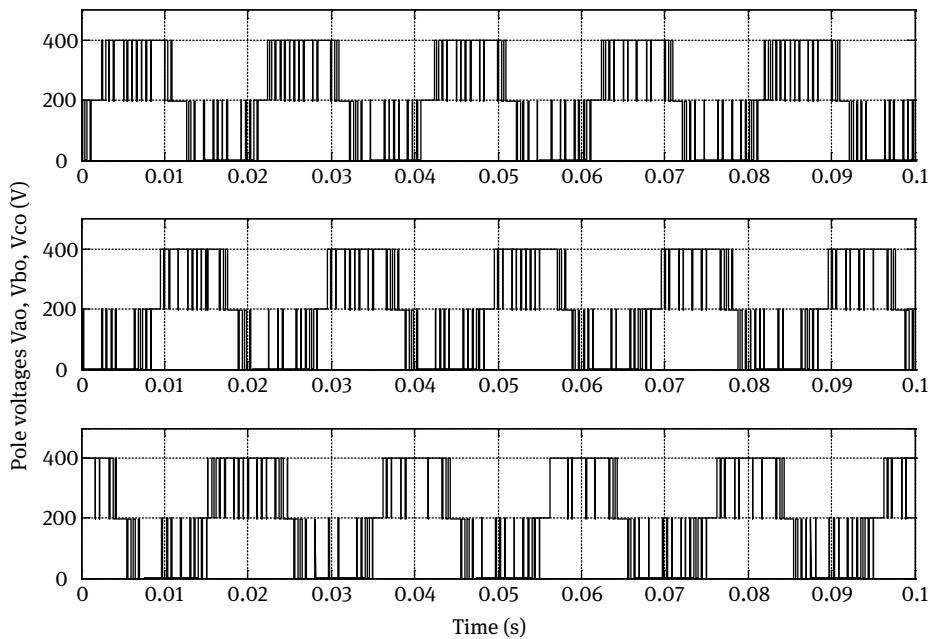


Fig. 7.10: Pole voltages of the three-level inverter.

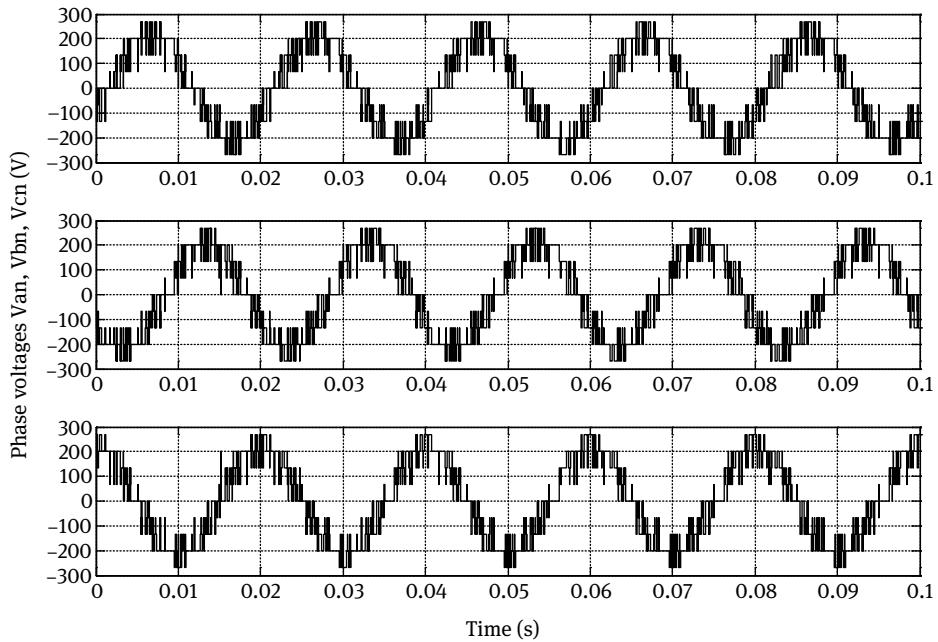


Fig. 7.11: Phase voltages of the three-level inverter.

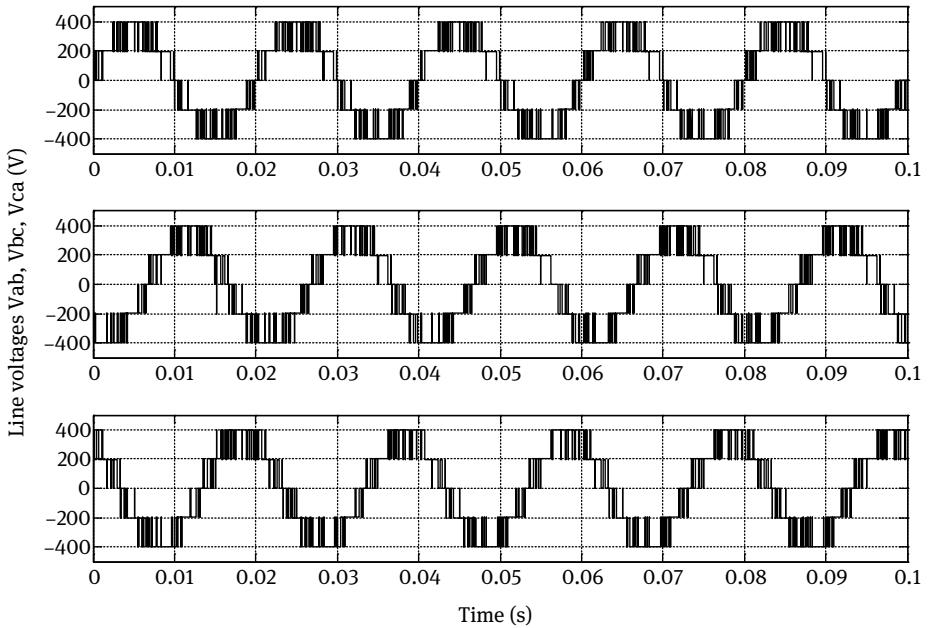


Fig. 7.12: Line-to-line voltages of the three-level inverter.

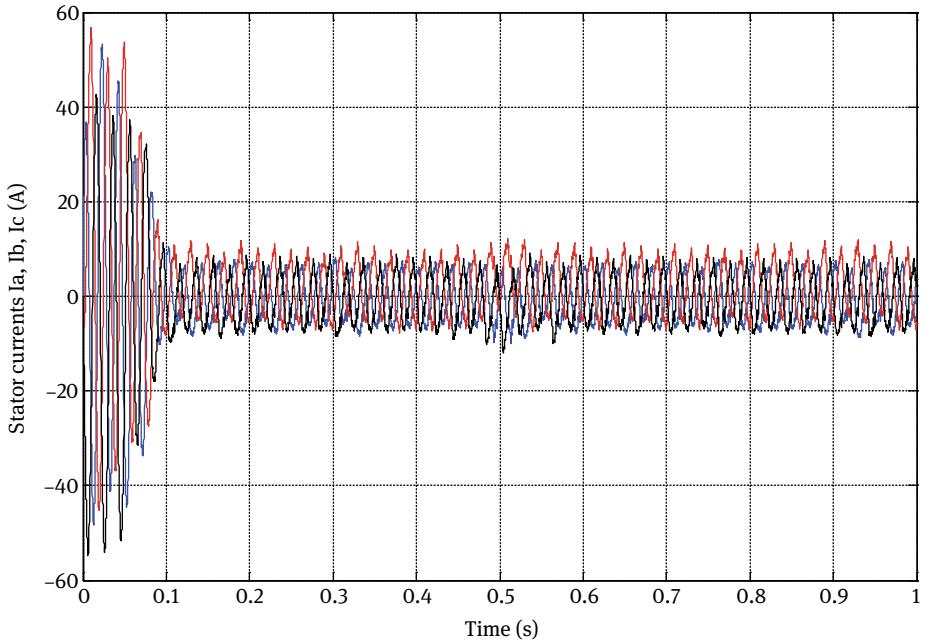


Fig. 7.13: Stator currents of the three-level inverter fed induction motor.

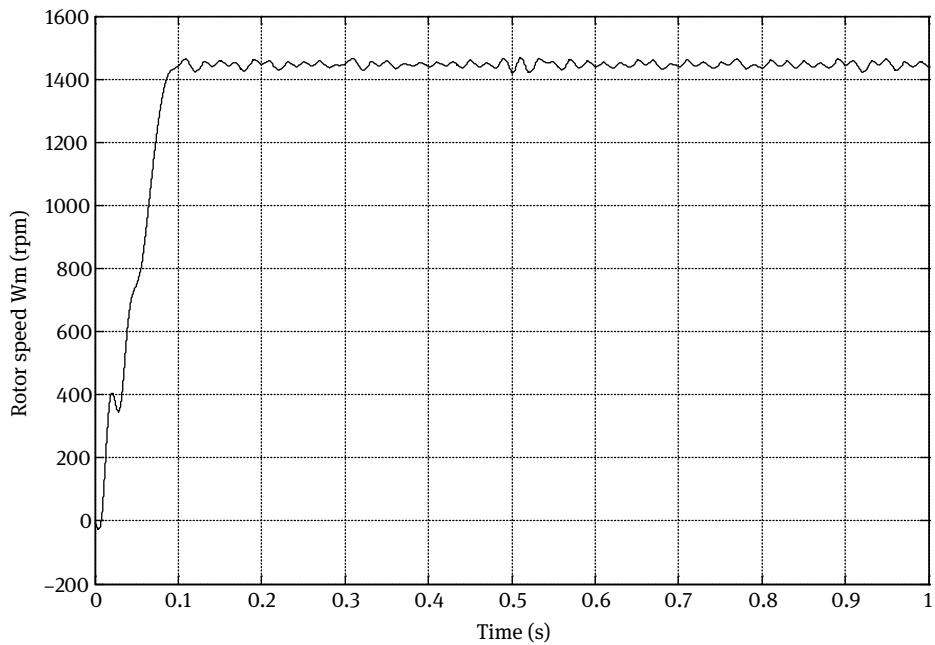


Fig. 7.14: Speed response of the three-level inverter fed induction motor.

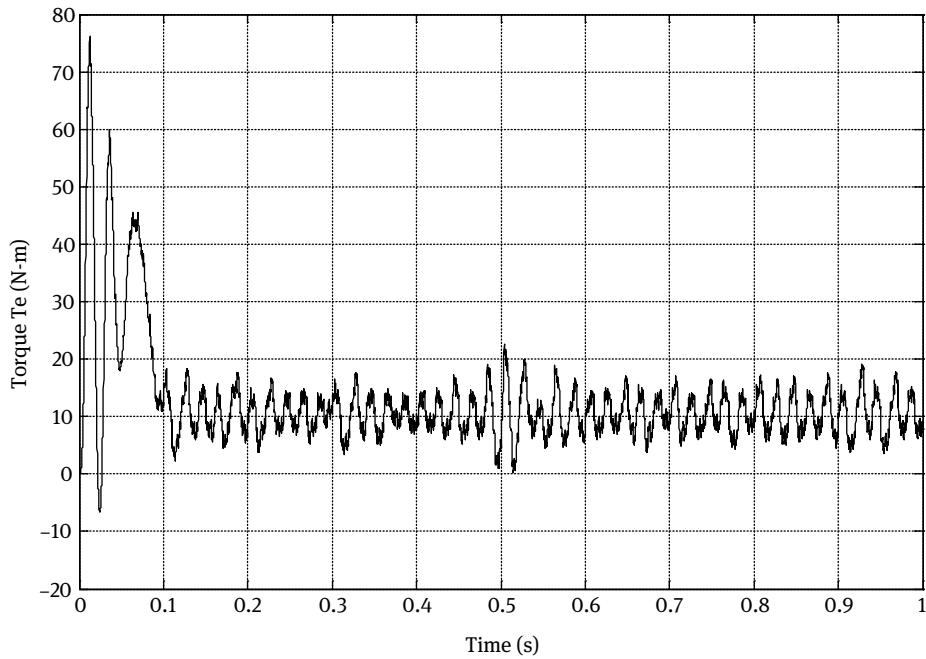


Fig. 7.15: Torque response of the three-level inverter fed induction motor.

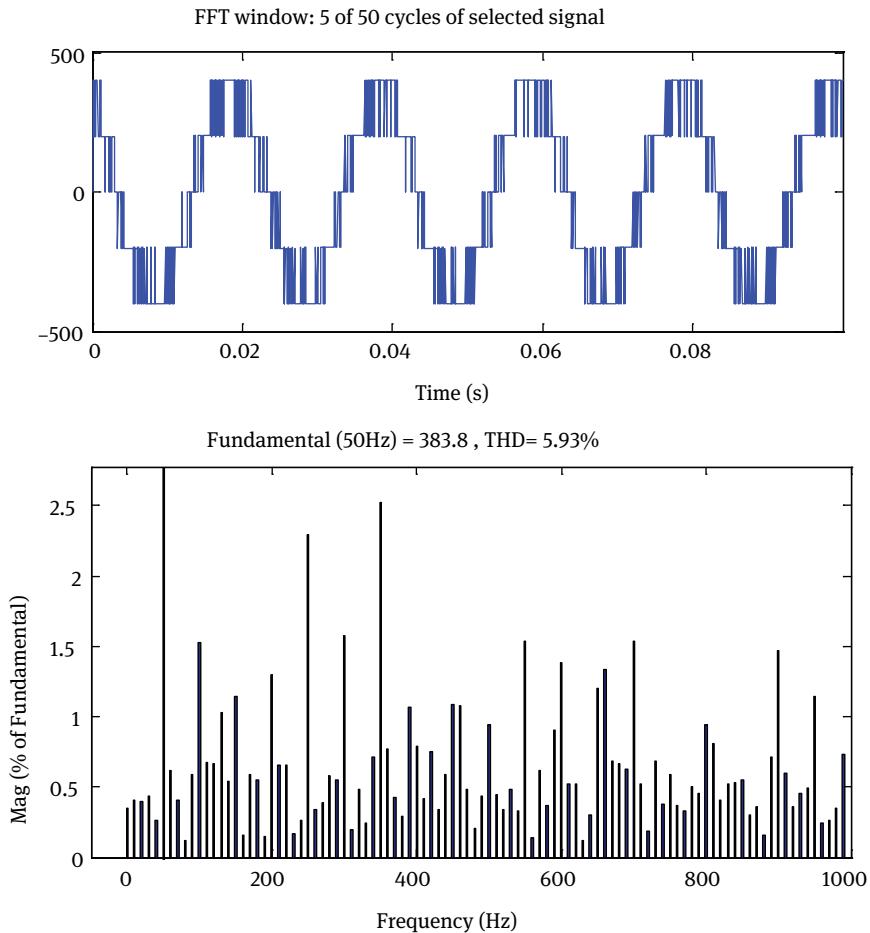


Fig. 7.16: Output line voltage (and its harmonic spectrum) of the three-level inverter.

7.3.2 Five-level inverter

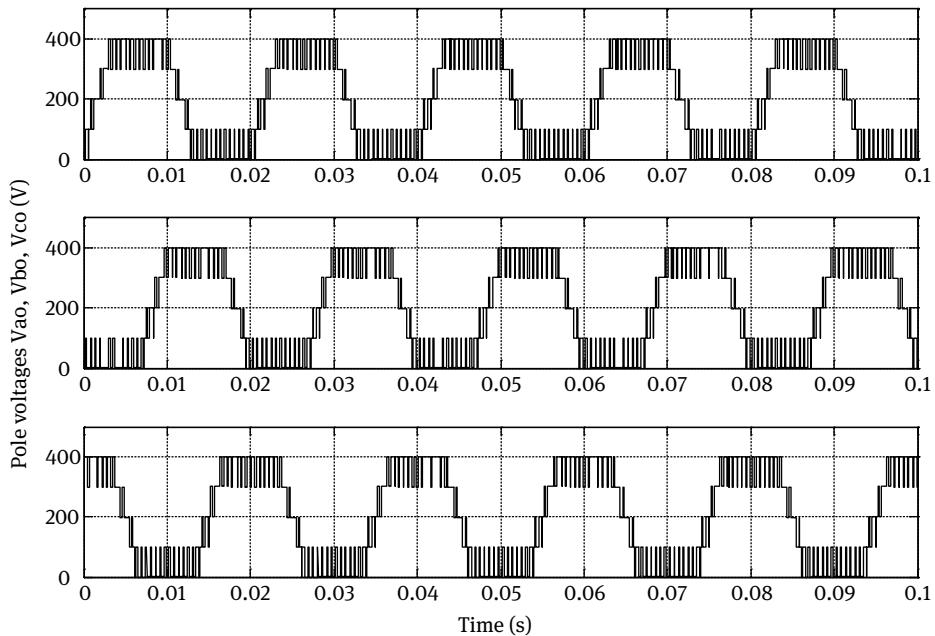


Fig. 7.17: Pole voltages of the five-level inverter.

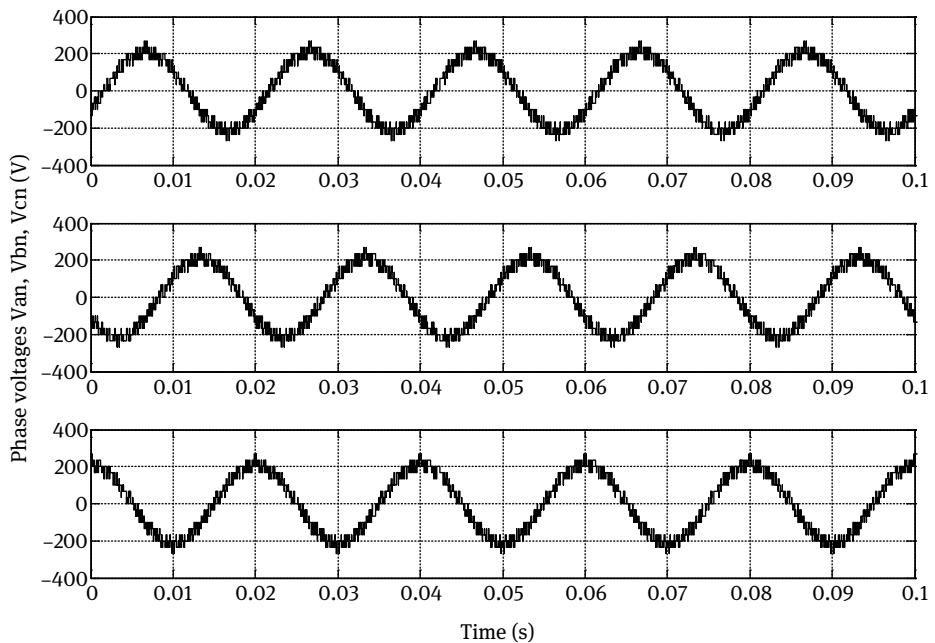


Fig. 7.18: Phase voltages of the five-level inverter.

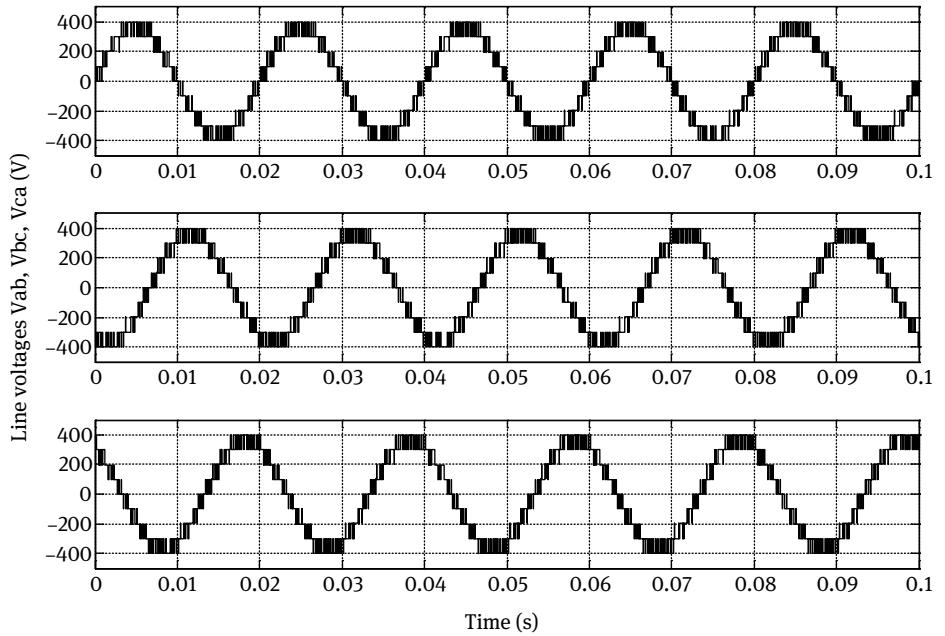


Fig. 7.19: Line-to-line voltages of the five-level inverter.

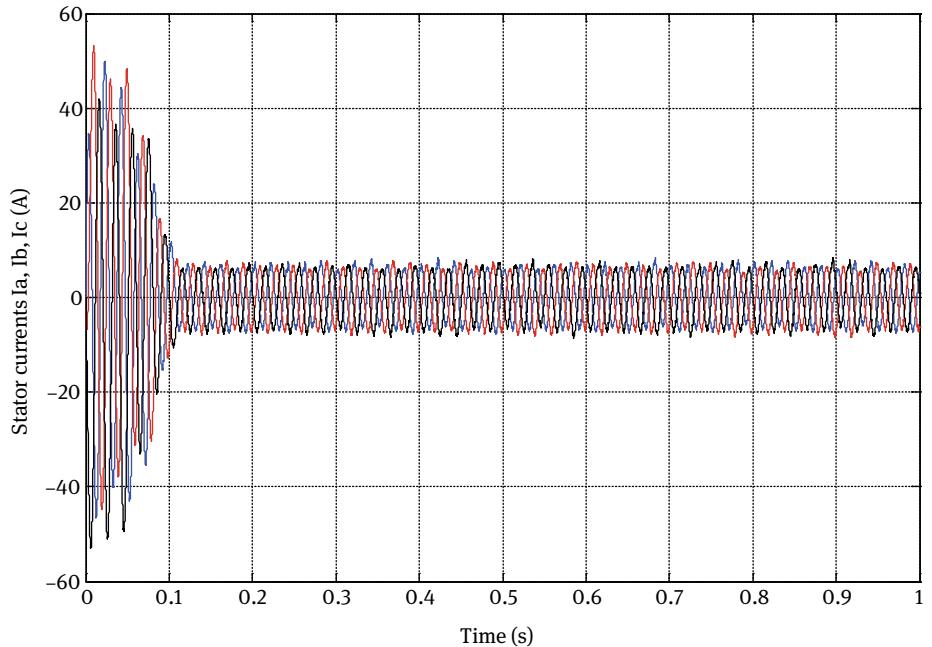


Fig. 7.20: Stator currents of the five-level inverter fed induction motor.

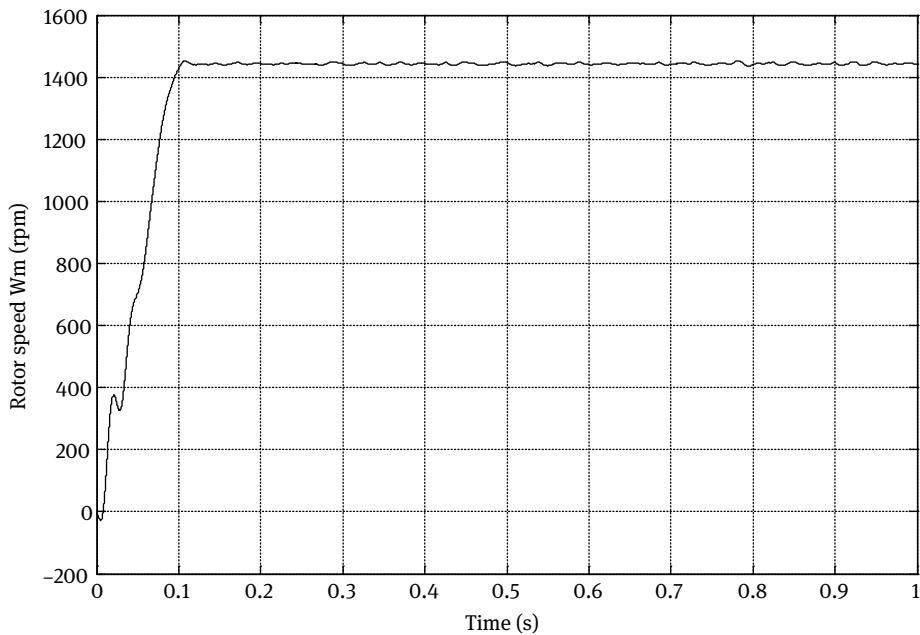


Fig. 7.21: Speed response of the five-level inverter fed induction motor.

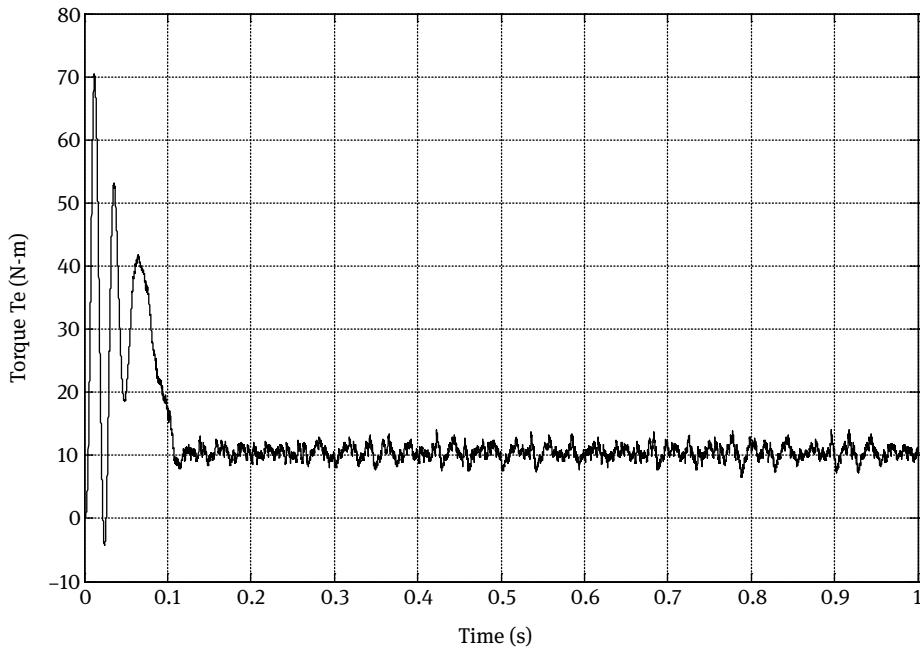


Fig. 7.22: Torque response of the five-level inverter fed induction motor.

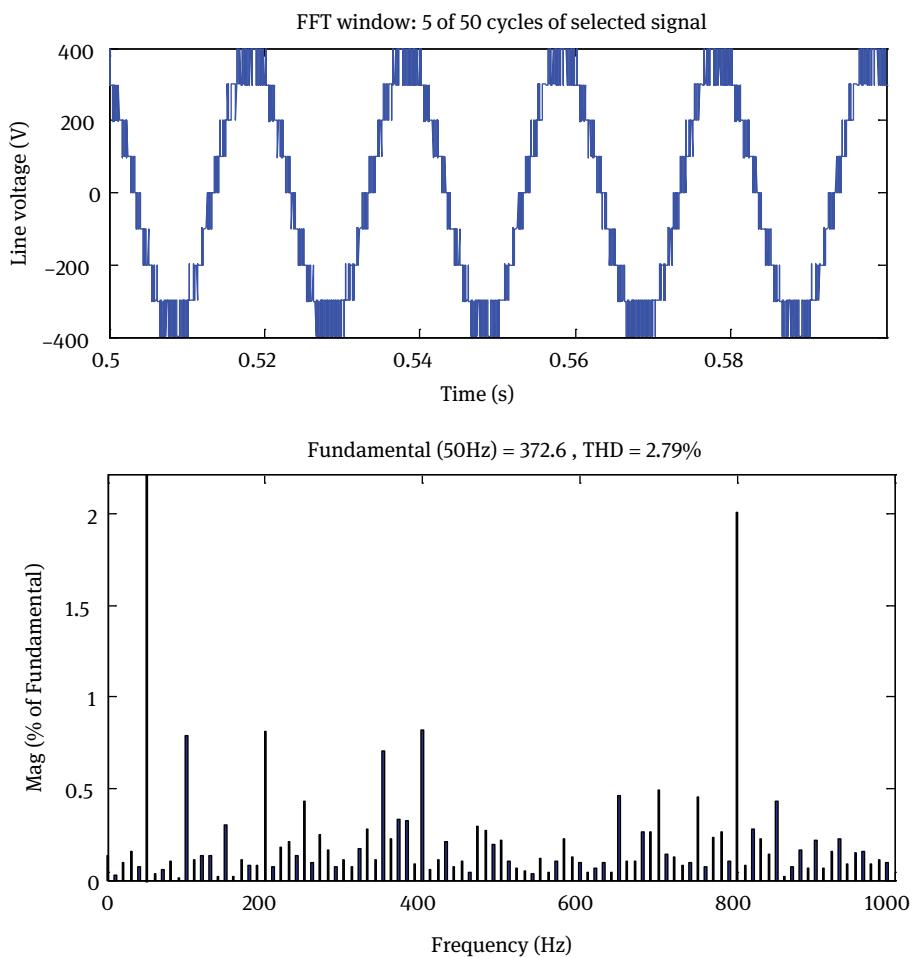


Fig. 7.23: Output line voltage (and its harmonic spectrum) of the five-level inverter.

7.3.3 Seven-level inverter

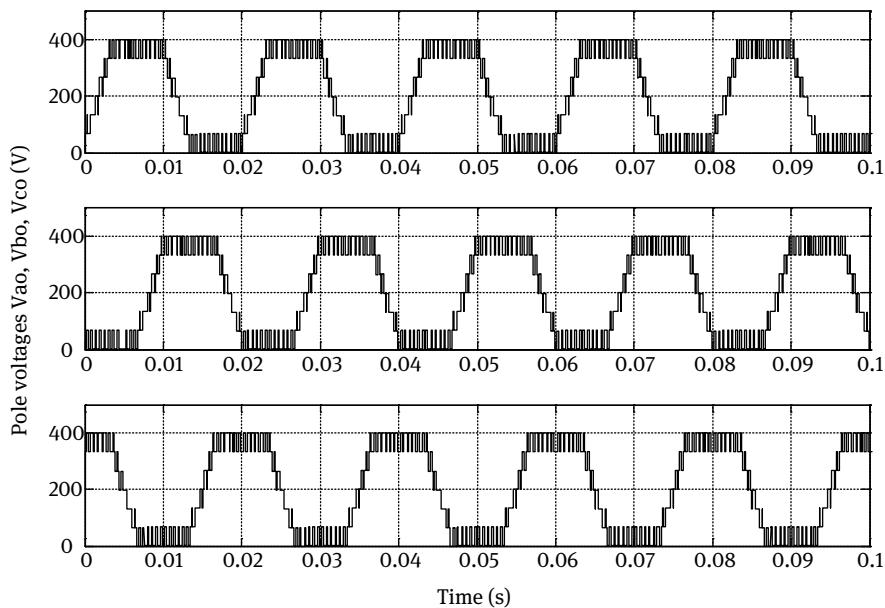


Fig. 7.24: Pole voltages of the seven-level inverter.

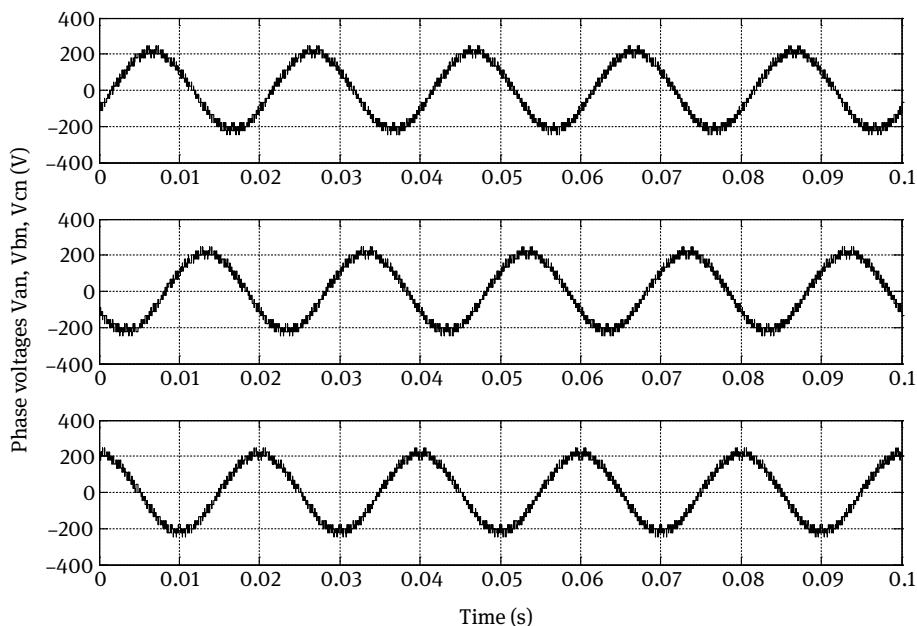


Fig. 7.25: Phase voltages of the seven-level inverter.

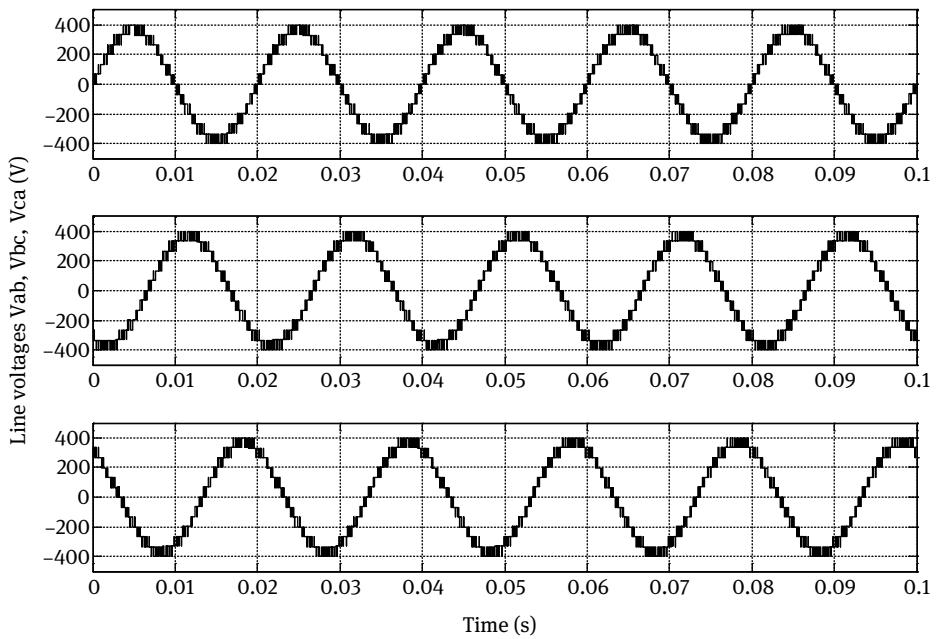


Fig. 7.26: Line-to-line voltages of the seven-level inverter.

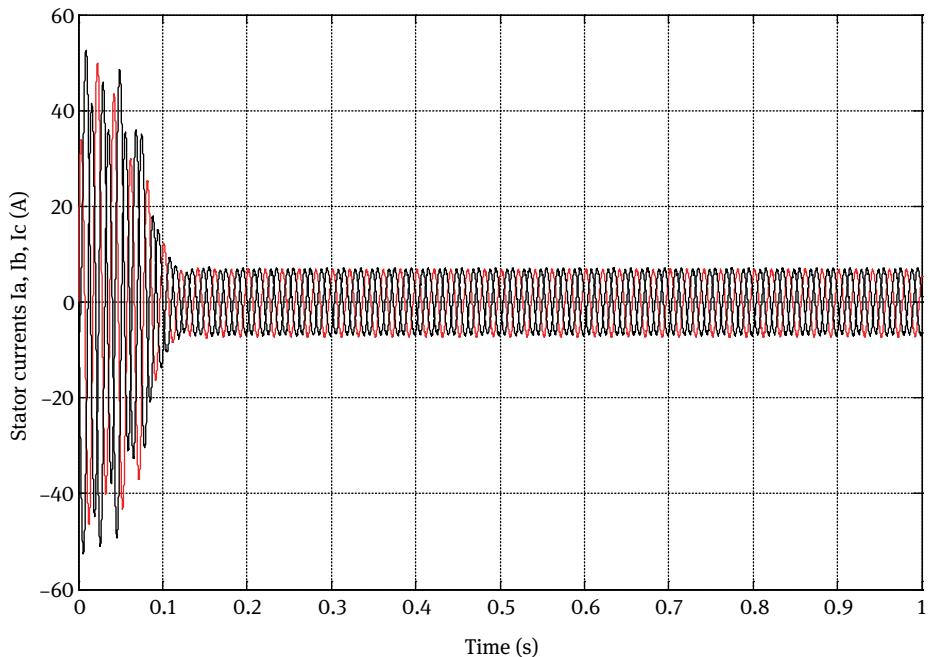


Fig. 7.27: Stator currents of the seven-level inverter fed induction motor.

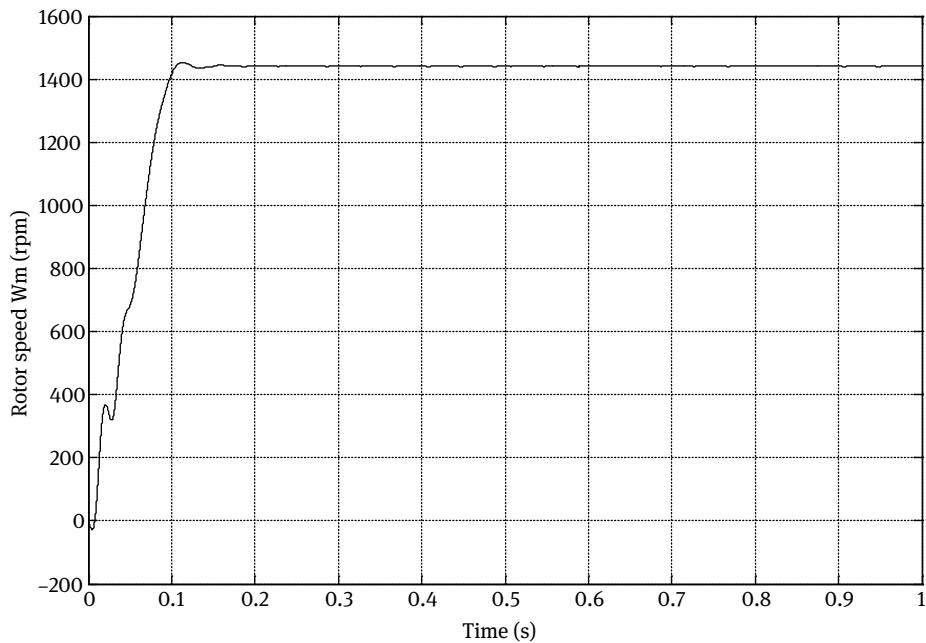


Fig. 7.28: Speed response of the seven-level inverter fed induction motor.

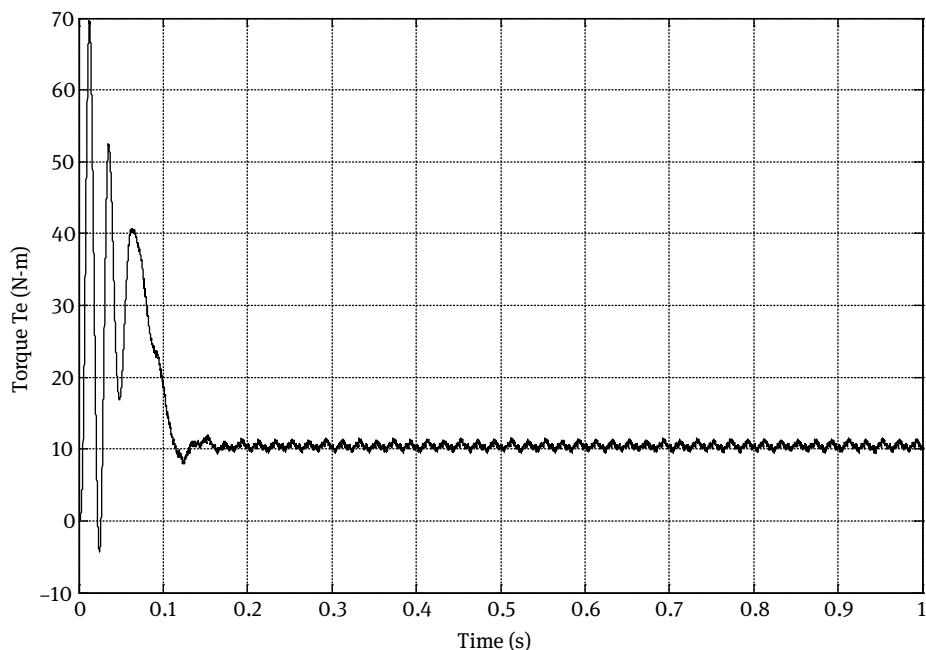


Fig. 7.29: Torque response of the seven-level inverter fed induction motor.

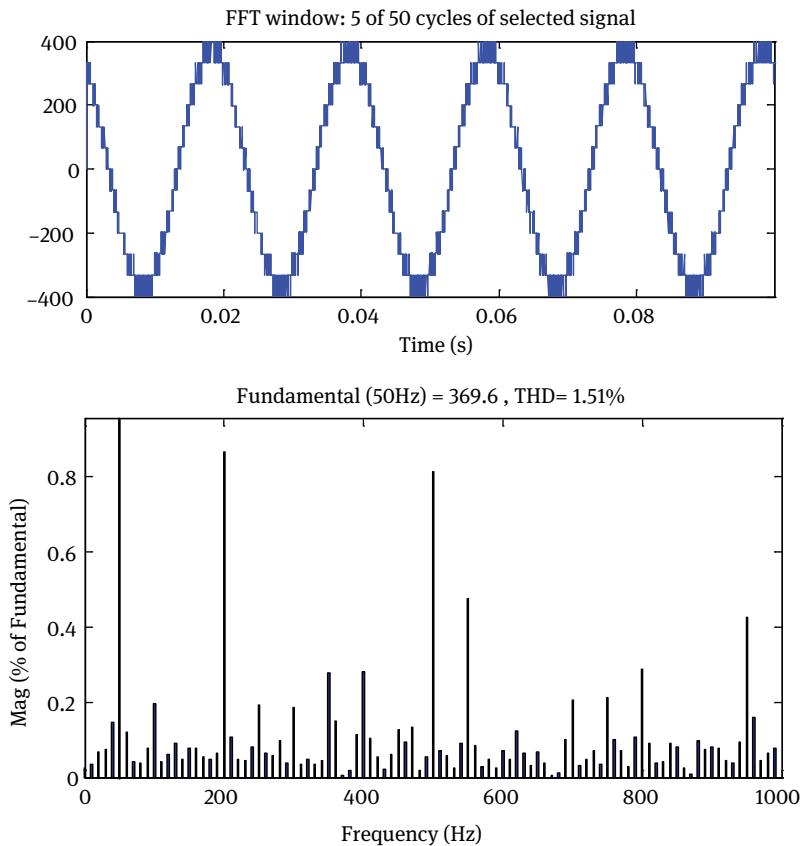


Fig. 7.30: Output line voltage (and its harmonic spectrum) of the seven-level inverter.

7.4 Conclusions

In this chapter, the SVPWM for the multilevel inverter using the decomposition method has been proposed and described for a seven-level inverter. In this method, the space vector diagram of the multilevel inverter is decomposed into several space vector diagrams of the two-level inverter. After decomposition, all the remaining necessary procedures for multilevel inverter are done like conventional two-level inverter. The dwelling times of the voltage vectors are calculated at the same manner as the two-level inverter. Thus, the proposed method reduces the algorithm complexity and execution time. The results are obtained for the three-, five-, and seven-level inverters. The obtained THD with the proposed method for the three-, five-, and seven-level inverters is 5.93%, 2.79%, and 1.51%, respectively. The phase voltage, torque, speed, and current responses are greatly improved.

8 An analytical space vector pulse width modulation method for multilevel inverters

In this chapter, an analytical space vector pulse width modulation (SVPWM) method for multilevel voltage source inverter (VSI) is proposed based on the intrinsic relation between multilevel and two-level SVPWM. In this method, the dwelling time of vector calculation is derived from the two-level inverter. Using linear transformation, the dwell time of vectors for two-level VSI can be transformed into multilevel VSI. A novel classification of voltage vectors is proposed to determine switching pattern of PWM sequence and used up to the eleven-level inverter, which can be extended to the n-level inverter as well.

8.1 Relation between three- and two-level SVPWMs

The first step of the nearest three vector algorithm is to determine the subsection where the reference vector is located, and the second step is to calculate the dwelling times of each vector. As the number of inverter levels increases, the subsection becomes very small. In this section, an analytical SVPWM algorithm for multilevel inverters is explained.

8.1.1 SVPWM for the two-level inverter

The two-level inverter space vector diagram is shown in Fig. 8.1. The reference voltage vector is described as

$$V^* = V_A + V_B e^{j\frac{2\pi}{3}} + V_C e^{j\frac{4\pi}{3}}. \quad (8.1)$$

The switching times of the SVPWM-based inverter can be calculated using volt-second relation. The volt-second balance equation in matrix form is

$$\begin{bmatrix} V'_{1x} & V'_{2x} & 0 \\ jV'_{1y} & jV'_{2y} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} t'_1 \\ t'_2 \\ T \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix} \quad (8.2)$$

The dwelling times of vectors are

$$\begin{aligned} t'_1 &= mT \sin(\frac{\pi}{3} - \theta) \\ t'_2 &= mT \sin(\theta) \\ t'_0 &= T - t'_1 - t'_2, \end{aligned} \quad (8.3)$$

where m is the modulation index, θ is the angle of rotation, t'_1 , t'_2 , and t'_0 are the dwell times of voltage vectors V'_1 , V'_2 , and V'_0 , respectively.

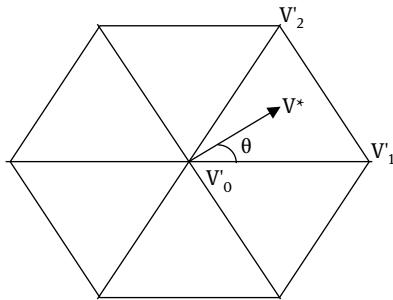


Fig. 8.1: Space vector diagram of the two-level inverter.

8.1.2 Switching times calculation for the three-level inverter

Figure 8.2 shows the space vector diagram of the three-level inverter. The relation between the switching times and the voltage vectors are given by

$$\begin{aligned} t_1 V_1 + t_2 V_2 + t_3 V_3 &= V^* T \\ t_1 + t_2 + t_3 &= T \end{aligned} \quad . \quad (8.4)$$

In matrix form

$$\begin{bmatrix} V_{1x} & V_{2x} & V_{3x} \\ jV_{1y} & jV_{2y} & jV_{3y} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix}. \quad (8.5)$$

The relation between two- and three-level voltage vectors is given by

$$\begin{aligned} V_1 &= a_1 V_1^1 + b_1 V_2^1 = (a_1 V_{1x}^1 + b_1 V_{2x}^1) + j(a_1 V_{1y}^1 + b_1 V_{2y}^1) \\ V_2 &= a_2 V_1^1 + b_2 V_2^1 = (a_2 V_{1x}^1 + b_2 V_{2x}^1) + j(a_2 V_{1y}^1 + b_2 V_{2y}^1) \\ V_3 &= a_3 V_1^1 + b_3 V_2^1 = (a_3 V_{1x}^1 + b_3 V_{2x}^1) + j(a_3 V_{1y}^1 + b_3 V_{2y}^1). \end{aligned} \quad (8.6)$$

Describing Eq. (8.6) in matrix form and substituting in Eq. (4.12) gives

$$\begin{bmatrix} V_{1x}^1 & V_{2x}^1 & 0 \\ jV_{1y}^1 & jV_{2y}^1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix}. \quad (8.7)$$

Comparing Eq. (8.7) with Eq. (8.1) and considering that the first left matrix is reversible, and then the switching times for the three-level inverter is described as

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} t'_1 \\ t'_2 \\ T \end{bmatrix}. \quad (8.8)$$

From Eq. (8.7), the switching times for the three-level inverter can be described as

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} t'_1 \\ t'_2 \\ T \end{bmatrix} = \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix}. \quad (8.9)$$

The switching times of the three-level inverter can be obtained from the solution of Eq. (8.8). Thus, from a linear transformation between two- and three-level inverters, the switching times of the three-level inverters can be derived. This method simply can be extended to the N-level inverter.

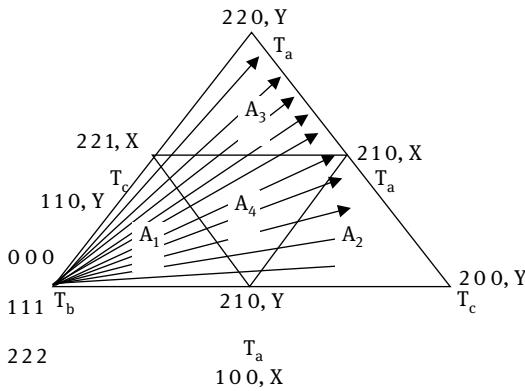
8.2 Switching states and switching sequence

8.2.1 Three-level inverter

The switching states of the three-level inverter can be classified into four groups based on their magnitudes and represented by a space vector diagram, as shown in Fig. 8.2. They can be classified into zero, small (vertices of inner hexagon), medium (mid-points of sides of outer hexagon), and large vectors (vertices of outer hexagon). Both the zero and small vectors have redundant switching states.

The space vector diagram of the three-level inverter is divided into six sextants, and each sextant is divided into four triangular regions in order to show the vectors nearest to the reference. The three-level inverter consists of zero voltage vectors (ZVV), lower small voltage vectors (LSVV), upper small voltage vectors (USVV), middle voltage vectors (MVV), and large voltage vectors (LVV), as shown in Tab. 8.1.

A new method is proposed for the generation of voltage vector switching pattern. The voltage vectors are divided into X and Y groups as shown in Tab. 8.2. If one vector belongs to the X group, then the vector with only one level changing in one phase belongs to the Y group. Thus, all middle voltage vectors belongs to the X group and all large voltage vectors belong to the Y group. The lower small voltage vectors and upper small voltage vectors belong to the X and Y groups, respectively. Thus, the output vector always alternates between X and Y groups. After odd times varying, the vector reaches the other group, and after even times varying, the vector reaches the same group. The switching sequence of sections A₂, A₃ and A₄ are shown in Tab. 8.3.

**Fig. 8.2:** Space vector diagram of the three-level inverter in sextant I.**Tab. 8.1:** Classification of voltage vectors.

Voltage vector	Symbols
ZVV	(000), (111), (222)
LSVV	(100), (010), (001), (110), (101), (011)
USVV	(211), (121), (112), (221), (212), (112)
MVV	(210), (120), (021), (012), (102), (201)
LVV	(200), (220), (020), (022), (002), (202)

Tab. 8.2: Classification of the three-level inverter switching states.

X	(111)	(100), (010), (001), (221), (212), (122)	(210), (120), (021), (012), (102), (201)
Y	(000), (222)	(110), (101), (011), (211), (121), (112)	(200), (220), (020), (022), (002), (202)

Tab. 8.3: Switching sequence of A_2 , A_3 , and A_4 regions.

Region	(ON sequence)	(OFF sequence)
A_2	211-210-200-100	100-200-210-211
A_3	221-220-210-110	110-210-220-221
A_4	211-210-110-100	110-210-211-221

8.2.2 Eleven-level inverter

The schematic diagram of the eleven-level inverter is shown in Fig. 8.3. The dc bus voltage is split into eleven levels using ten dc capacitors, C_1 , C_2 , C_3 , C_4 , C_5 , C_6 , C_7 , C_8 , C_9 , and C_{10} . Each capacitor has $V_{dc}/10$ V and each voltage stress will be limited to one capacitor level through clamping diodes.

The space vector diagram of the eleven-level inverter is divided into six sextants, and each sextant is divided into 100 triangular regions in order to show the vectors nearest to the reference voltage. The switching sequences of the three level inverter

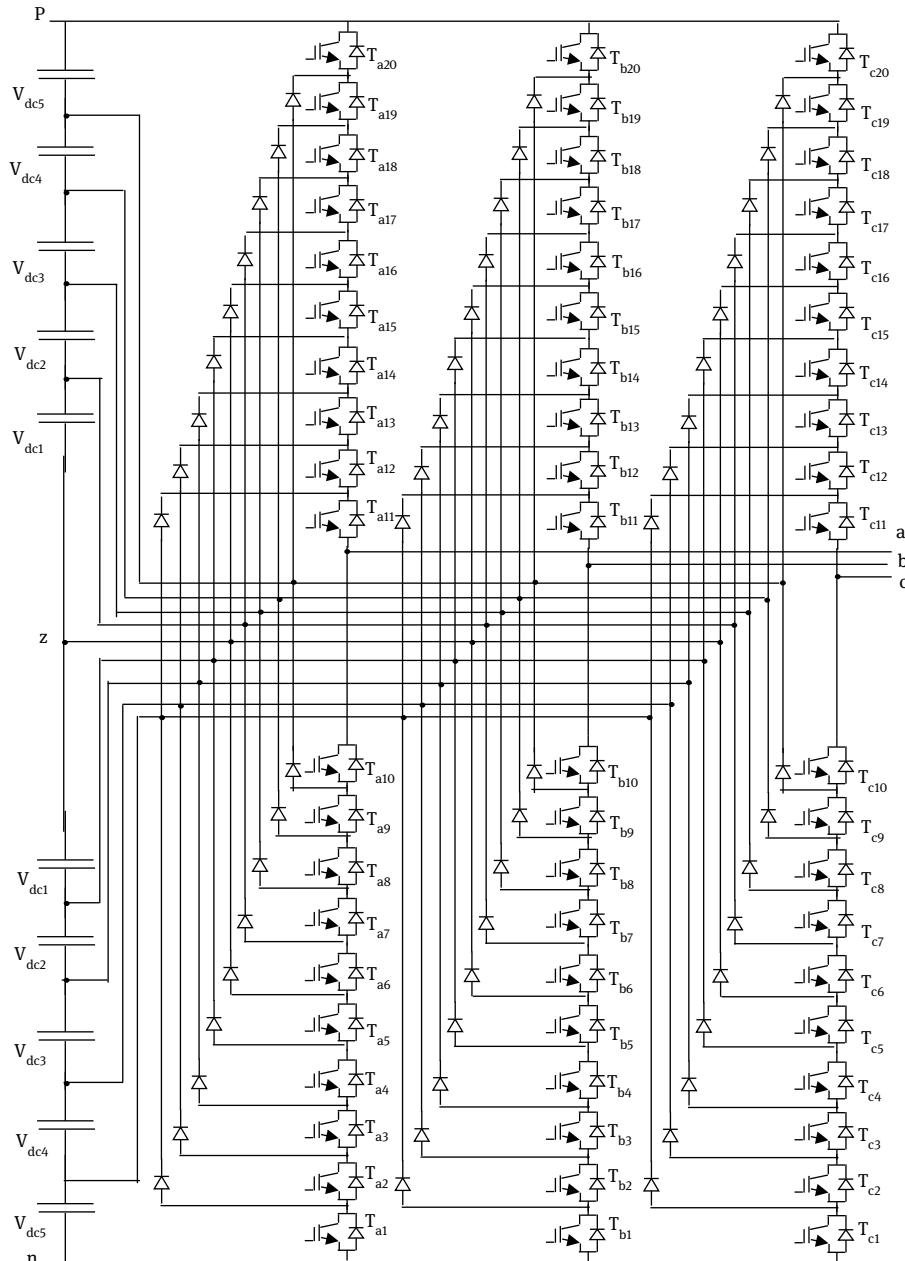


Fig. 8.3: Eleven-level NPC inverter topology.

in sector I are as shown in Tab 8.4. The voltage vectors of the eleven-level inverter are divided into X and Y groups, as shown in Tab. 8.5. The procedure of selecting the voltage vector of X and Y groups are similar to that of the three-level inverter. Table 8.6 shows the switching ON sequence and OFF sequence for all the regions of sextant I of the eleven-level inverter. The subsections of the eleven-level inverter in sextant-I are shown in Fig. 8.4.

Tab. 8.4: Switching sequence of the three-level inverter in sector I.

Samples	States	Switching
1	5-17-16-4	211-210-200-100
2	4-16-17-5	100-200-210-211
3	4-16-17-5	100-200-210-211
4	5-17-16-4	211-210-200-100
5	5-17-7-4	211-210-110-100
6	4-7-17-5	100-110-210-211
7	6-18-17-7	221-220-210-110
8	7-17-18-6	110-210-220-221
9	7-17-18-6	110-210-220-221
10	7-17-18-6	110-210-220-221
11	6-18-17-7	221-220-210-110

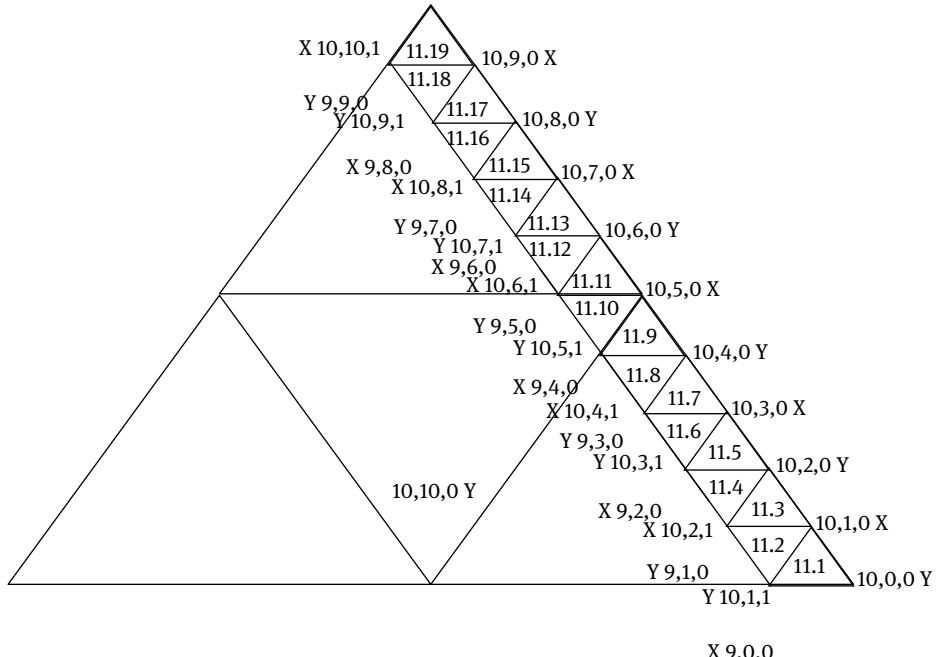


Fig. 8.4: Subsections of the eleven-level inverter in sextant I.

Tab. 8.5: Classification of the eleven-level inverter switching states.

X	(900) (1021) (920) (1041) (940) (1061) (960) (1081) (980) (10101) (890) (8101) (690) (6101) (490) (4101) (290) (2101) (090) (1102) (092) (1104) (094) (1106) (096) (1108) (098) (11010) (089) (1810) (069) (1610) (049) (1410) (029) (1210) (009) (2110) (209) (4110) (409) (6110) (609) (8110) (809) (10110) (908) (1018) (906) (1016) (904) (1014) (902) (1012) (1010) (1030) (1050) (1070) (1090) (9100) (7100) (5100) (3100) (1100) (0101) (0103) (0105) (0107) (0109) (0910) (0710) (0510) (0310) (0110) (1010) (3010) (5010) (7010) (9010) (1009) (1007) (1005) (1003) (1001)
Y	(1011) (910) (1031) (930) (1051) (950) (1071) (970) (1091) (990) (9101) (790) (7101) (590) (5101) (390) (3101) (190) (1101) (091) (1103) (093) (1105) (095) (1107) (097) (1109) (099) (1910) (079) (1710) (059) (1510) (039) (1310) (019) (1110) (109) (3110) (309) (5110) (509) (7110) (709) (9110) (909) (1019) (907) (1017) (905) (1015) (903) (1013) (901) (1000) (1020) (1040) (1060) (1080) (10100) (8100) (6100) (4100) (3100) (0100) (0102) (0104) (0106) (0108) (01010) (0810) (0610) (0410) (0210) (0010) (2010) (4010) (6010) (8010) (10010) (1008) (1006) (1004) (1002)

Tab. 8.6: Switching sequence of the eleven-level inverter in sector I.

Region	ON sequence and OFF sequence
11.1	10,1,1-10,1,0-10,0,0-9,0,0 9,0,0-10,0,0-10,1,0-10,1,1
11.2	10,1,1-10,1,0-9,1,0-9,0,0 9,1,0-10,1,0-10,1,1-10,2,1
11.3	10,2,1-10,2,0-10,1,0-9,1,0 9,1,0-10,1,0-10,2,0-10,2,1
11.4	10,2,1-10,2,0-9,2,0-10,2,1 9,2,0-10,2,0-10,2,1-10,3,1
11.5	10,3,1-10,3,0-10,2,0-9,2,0 9,2,0-10,2,0-10,3,0-10,3,1
11.6	10,3,1-10,3,0-9,3,0-9,2,0 9,3,0-10,3,0-10,3,1-10,4,1
11.7	10,4,1-10,4,0-10,3,0-9,3,0 9,3,0-10,3,0-10,4,0-10,4,1
11.8	9,3,0-10,4,0-10,5,1-10,4,1 9,4,0-10,4,0-10,4,1-10,5,1
11.9	9,4,0-10,4,0-10,5,0-10,5,1 10,5,1-10,5,0-10,4,0-9,4,0
11.10	10,5,1-10,5,0-9,5,0-9,4,0 9,5,0-10,5,0-10,5,0-10,6,1
11.11	10,6,1-10,6,0-10,5,0-9,5,0 9,5,0-10,5,0-10,6,0-10,6,1
11.12	10,6,1-10,6,0-10,7,1-9,5,0 9,6,0-10,6,0-10,6,1-10,7,1

Tab. 8.6 (continued)

Region	ON sequence and OFF sequence
11.13	10,7,1-10,7,0-10,6,0-9,6,0 9,6,0-10,6,0-10,7,0-10,7,1
11.14	10,7,1-10,7,0-9,7,0-9,6,0 9,7,0-10,7,0-10,7,1-10,8,1
11.15	10,8,1-10,8,0-10,7,0-9,7,0 9,7,0-10,7,0-10,8,0-10,8,1
11.16	10,8,1-10,8,0-9,8,0-9,7,0 9,8,0-10,8,0-10,8,1-10,9,1
11.17	10,9,1-10,9,0-10,8,0-9,8,0 9,8,0-10,8,0-10,9,0-10,9,1
11.18	10,9,1-10,9,0-9,9,0-10,9,1 9,9,0-10,9,0-10,9,1-0,10,1
11.19	10,10,1-10,10,0-10,9,0-9,9,0 9,9,0-10,9,0-10,10,0-10,10,1

8.3 Algorithm for the N-level inverter

The first step is to identify the triangle where the reference voltage vector is located. Then the reference voltage vector is synthesized from the vectors that present at the vertices of this triangle and the dwell times of these vectors can be calculated. The triangle can be defined as a three-dimensional array

$$\begin{aligned}\lambda_1 &= \text{floor}[t_{1,2} \times (N - 1)] \\ \lambda_2 &= \text{floor}[t_{2,2} \times (N - 1)] \\ \lambda_0 &= \text{floor}[t_{0,2} \times (N - 1)].\end{aligned}\quad (8.10)$$

The following conclusions are made from the space vector diagram of the eleven-level inverter shown in Fig. 8.5.

There is only one bit is changed between names of adjacent triangles.

The last bit in each row is the same.

If $\lambda_1 + \lambda_2 + \lambda_0 = N - 1$, the reference vector is located on vertices of triangle.

If $\lambda_1 + \lambda_2 + \lambda_0 = N - 2$, the voltage vectors are in the same direction with the voltage vectors of the two-level inverter triangle.

If $\lambda_1 + \lambda_2 + \lambda_0 = N - 3$, the triangle has the opposite direction with the voltage vectors of the two-level inverter triangle.

After identifying the triangle where the reference vector is located, the nearest three voltage vectors are chosen as the compound reference vector. As shown in Fig. 8.6, according to the volt-second balancing principle, the relation of the synthesis of the voltage vector to the reference vector is

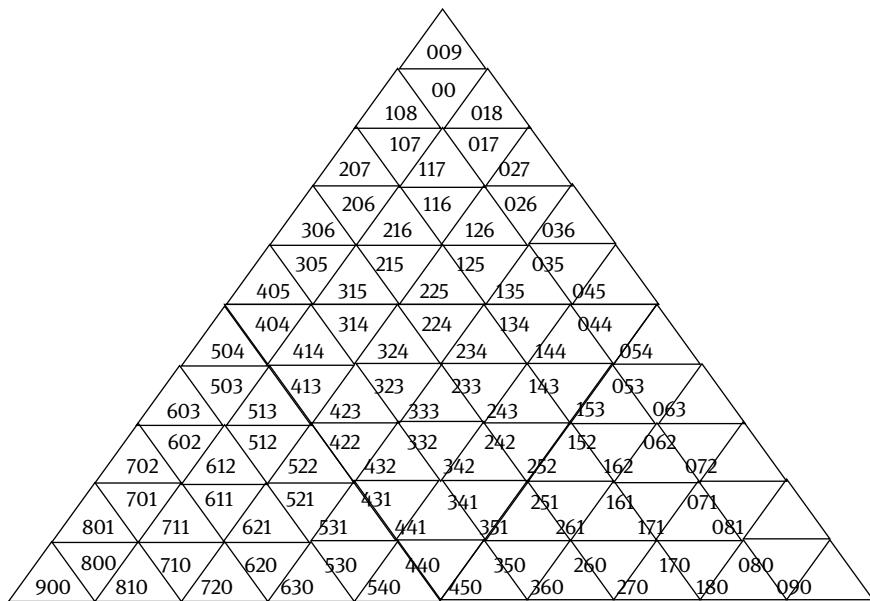


Fig. 8.5: Space vector diagram of the eleven-level inverter in sector I.

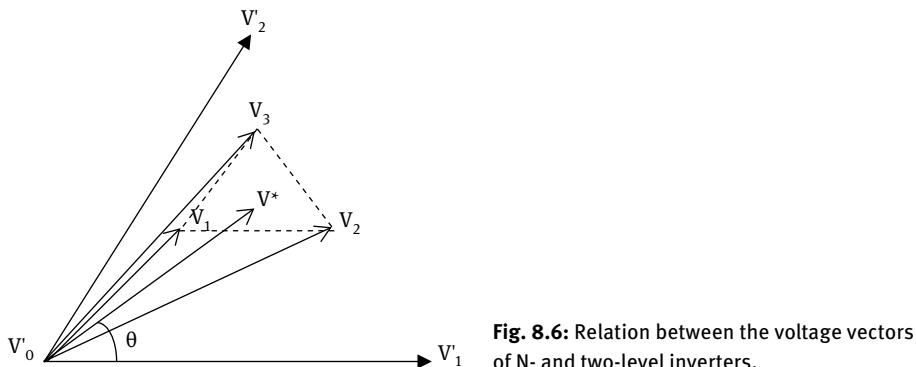


Fig. 8.6: Relation between the voltage vectors of N- and two-level inverters.

$$\begin{aligned} t_1 V_1 + t_{2,N} V_{2,N} + t_{3,N} V_{3,N} &= V^* T_s \\ t_{1,N} + t_{2,N} + t_{3,N} &= T_s. \end{aligned} \quad (8.11)$$

That is,

$$\begin{bmatrix} V_{1,Nx} & V_{2,Nx} & V_{3,Nx} \\ jV_{1,Ny} & jV_{2,Ny} & jV_{3,Ny} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} V_x^* T_s \\ jV_y^* T_s \\ T_s \end{bmatrix}. \quad (8.12)$$

In N-level inverters, there is a mapping relation between the three nearest vectors used to synthesize the vector and the two non-zero vector of the two-level inverter, which is

$$\begin{aligned} V_1 &= a_1 V_{1,2} + b_1 V_{2,2} \\ V_2 &= a_2 V_{1,2} + b_2 V_{2,2} \\ V_3 &= a_3 V_{1,2} + b_3 V_{2,2}. \end{aligned} \quad (8.13)$$

Changing Eq. (8.13) into the matrix and putting it into Eq. (8.12). In complex plane, we can obtain the following matrix.

$$\begin{bmatrix} V_{1,2x} & V_{2,2x} & 0 \\ jV_{1,2y} & jV_{2,2y} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T_s \end{bmatrix}. \quad (8.14)$$

From the two-level inverter to the N-level inverter, the voltage vector transition matrix is defined as

$$R = \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix}. \quad (8.15)$$

The matrix R is reversible.

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} t_{1,2} \\ t_{2,2} \\ T_s \end{bmatrix}. \quad (8.16)$$

$$T_N = \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = R^{-1} \begin{bmatrix} t_{1,2} \\ t_{2,2} \\ T_s \end{bmatrix} = R^{-1} T_2. \quad (8.17)$$

From the solution of these above equations, the dwell time of each vector can be obtained. Thus, there is a simple linear mapping relation between the dwell time of the vectors of the N-level inverter and the two-level inverter. The positive and negative triangles of N-level inverter space vector diagram is as shown in Fig. 8.7

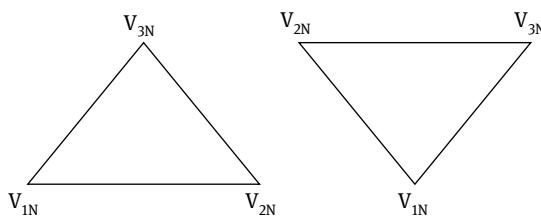


Fig. 8.7: Positive and negative triangles of the N-level inverter space vector diagram.

In a triangle, any voltage vector of the N-level inverter can be given as

$$V = \frac{1}{N} \{\alpha[100] + \beta[110] + \gamma[111]\}$$

Then, the nearest three vectors of positive and negative triangles have the following relationship.

$$\begin{aligned} V_{1,N} &= \frac{1}{N-1} \{\lambda_1[100] + \lambda_2[110] + \gamma[111]\} \\ V_{2,N} &= \frac{1}{N-1} \{(\lambda_1 - 1)[100] + (\lambda_2 + 1)[110] + \gamma[111]\} \\ V_{3,N} &= \frac{1}{N-1} \{\lambda_1[100] + (\lambda_2 + 1)[110] + \gamma[111]\} \end{aligned} \quad (8.18)$$

The direction and length of the voltage in the N-level inverter are represented by coefficients λ_1 and λ_2 . Parameter γ controls the redundancy vector. The matrix R is the voltage vector transform matrix, but the matrix R^{-1} is the time transition matrix from the two-level inverter to the N-level inverter, respectively. These positive triangle transition matrices are given by

$$R_{\text{positive}} = \begin{bmatrix} \frac{\lambda_1}{N-1} & \frac{\lambda_1+1}{N-1} & \frac{\lambda_1}{N-1} \\ \frac{\lambda_2}{N-1} & \frac{\lambda_2}{N-1} & \frac{\lambda_2+1}{N-1} \\ 1 & 1 & 1 \end{bmatrix} \quad (8.19)$$

$$R_{\text{positive}}^{-1} = \begin{bmatrix} -(N-1) & -(N-1) & (\lambda_2 + \lambda_1 + 1) \\ (N-1) & 0 & -\lambda_1 \\ 0 & (N-1) & -\lambda_2 \end{bmatrix} \quad (8.20)$$

The negative triangle transition matrices can be obtained from the following relationships:

$$\begin{aligned} V_{1,N} &= \frac{1}{N-1} \{\lambda_1[100] + \lambda_2[110] + \gamma[111]\} \\ V_{2,N} &= \frac{1}{N-1} \{(\lambda_1 - 1)[100] + (\lambda_2 + 1)[110] + \gamma[111]\} \\ V_{3,N} &= \frac{1}{N-1} \{\lambda_1[100] + (\lambda_2 + 1)[110] + \gamma[111]\} \end{aligned} \quad (8.21)$$

$$R_{\text{positive}} = \begin{bmatrix} \frac{\lambda_1}{N-1} & \frac{\lambda_1+1}{N-1} & \frac{\lambda_1}{N-1} \\ \frac{\lambda_2}{N-1} & \frac{\lambda_2}{N-1} & \frac{\lambda_2+1}{N-1} \\ 1 & 1 & 1 \end{bmatrix} \quad (8.22)$$

$$R_{\text{negative}}^{-1} = \begin{bmatrix} 0 & -(N-1) & (\lambda_2 + 1) \\ -(N-1) & 0 & \lambda_1 \\ (N-1) & (N-1) & -(\lambda_1 + \lambda_2) \end{bmatrix} \quad (8.23)$$

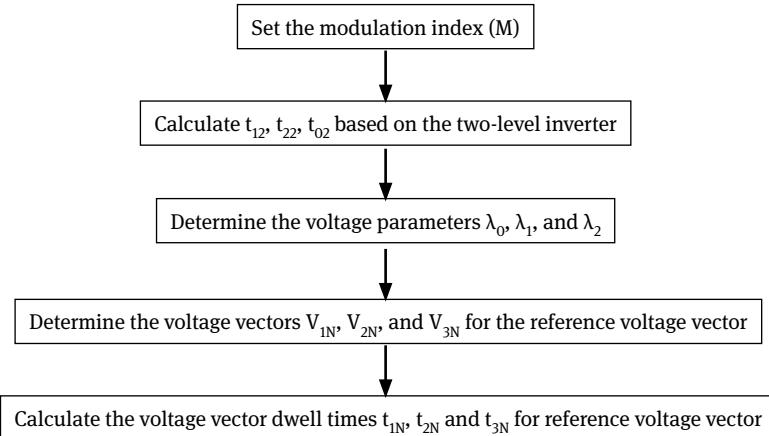


Fig. 8.8: Flowchart of the N-level inverter.

Thus, the analytical SVPWM algorithm for the N-level inverter can be deduced from the two-level inverter as shown in Fig. 8.8.

8.4 Results and discussions

The proposed method is verified by designing a model for the N-level inverter and simulating for the three-, five-, seven-, nine-, and eleven-level inverters. The simulation parameters and specifications of induction motor used in this method are given in Appendix V. Figures 8.9 to 8.14 show the results of the three-level inverter. The phase voltages, line voltages, and output voltage total harmonic distortion (THD) are shown in Figs. 8.9 to 8.11, respectively. The stator currents, rotor speed, and torque of the three-level inverter fed induction motor are shown in Figs. 8.12 to 8.14, respectively. Figures 8.15 to 8.20 show the results of the five-level inverter. The phase voltages, line voltages, and output voltage THD are shown in Figs. 8.15 to 8.17, respectively. The stator currents, rotor speed, and torque of the five-level inverter fed induction motor are shown in Figs. 8.18 to 8.20, respectively. The seven-level inverter results are shown in Figs. 8.21 to 8.26. The phase voltages, line voltages, and output voltage THD are shown in Figs. 8.21 to 8.23, respectively. The stator currents, rotor speed, and torque of the seven-level inverter fed induction motor are shown in Figs. 8.24 to 8.26, respectively. The results of the nine-level inverter are shown in Figs. 8.27 to 8.32 shows the results of the seven-level inverter. The phase voltages, line voltages, and output voltage THD are shown in Figs. 8.27 to 8.29, respectively.

The stator currents, rotor speed, and torque of the nine-level inverter fed induction motor are shown in Figs. 8.30 to 8.32, respectively. The results of the eleven-level inverter are shown in Figs. 8.33 to 8.38. The phase voltages, line voltages, and output voltage THD are shown in Figs. 8.33 to 8.35, respectively. The stator currents, rotor speed, and torque of the eleven-level inverter fed induction motor are shown in Figs. 8.36 to 8.38, respectively.

The line-to-line voltages and harmonic spectra of three-, five-, seven-, nine-, and eleven-level inverters are entirely the same as traditional SVPWM algorithm, and it shows that as the level of inverter increases the line voltage in a nearly standard sine wave. The THD, RMS current, and torque ripples decrease as the level of inverter increases. A simulation analysis using a higher level showed that it merely modifies the level setting number N , indicating that the algorithm is flexible and transplantable.

8.4.1 Three-level inverter

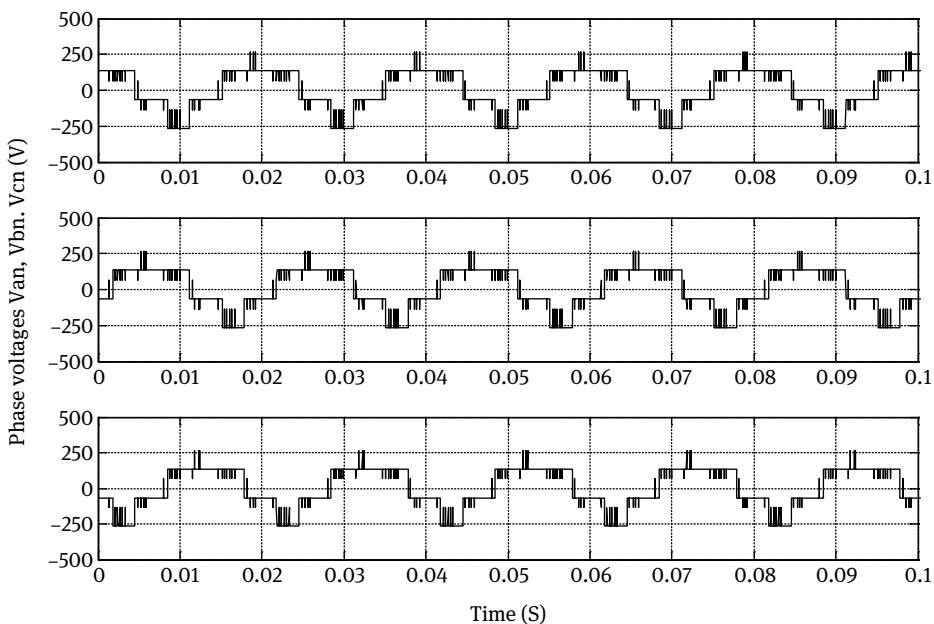


Fig. 8.9: Phase voltages of the three-level inverter.

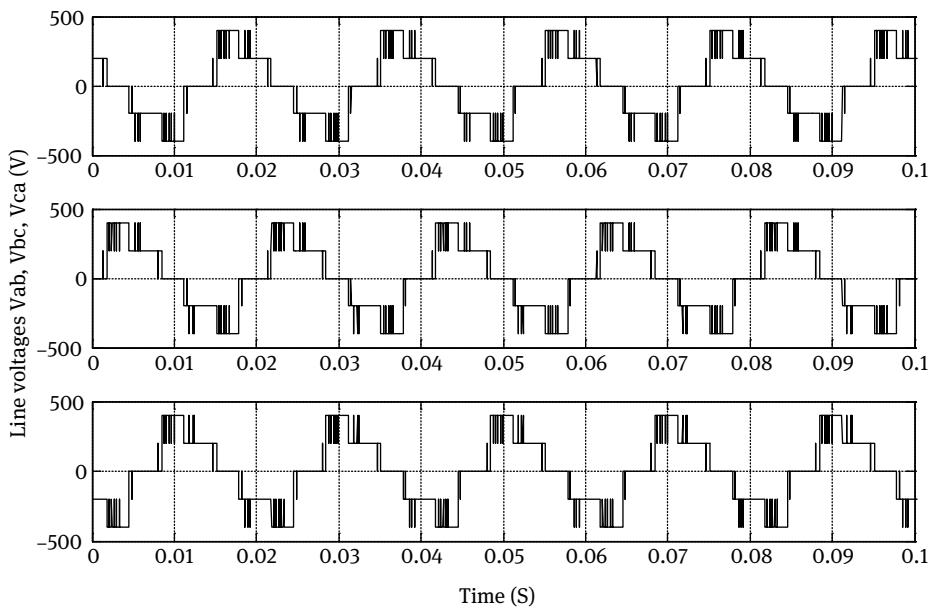


Fig. 8.10: Line-to-line voltages of the three-level inverter.

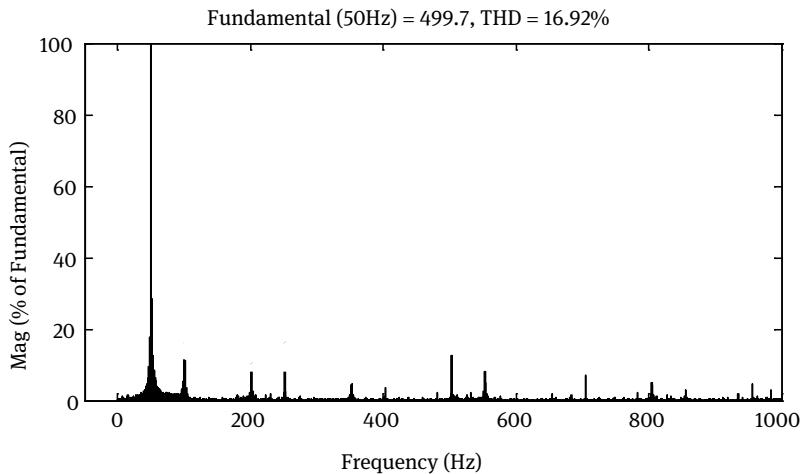


Fig. 8.11: Output line voltage harmonic spectrum of the three-level inverter.

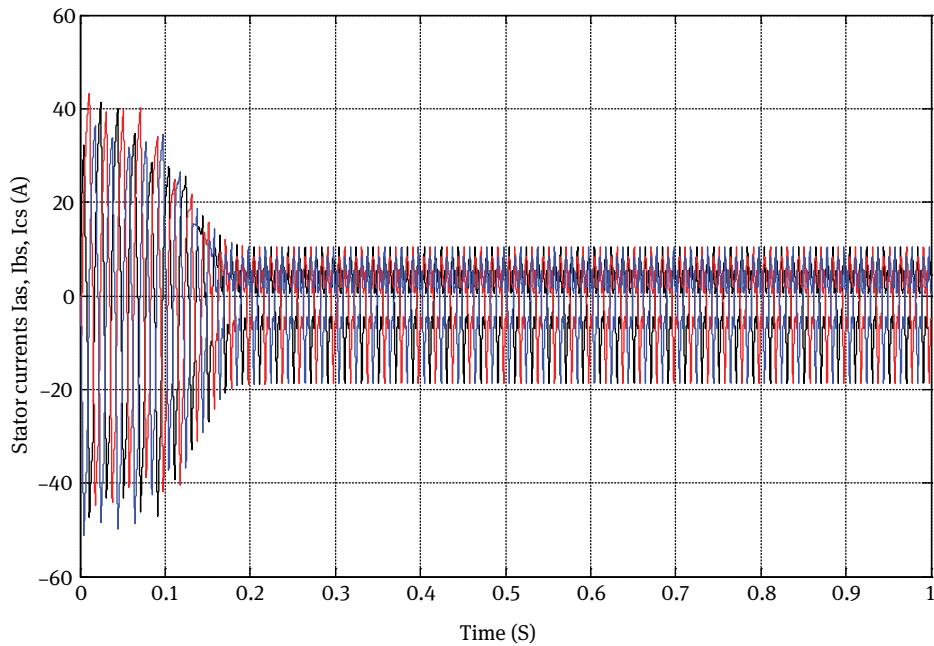


Fig. 8.12: Stator currents of the three-level inverter fed induction motor.

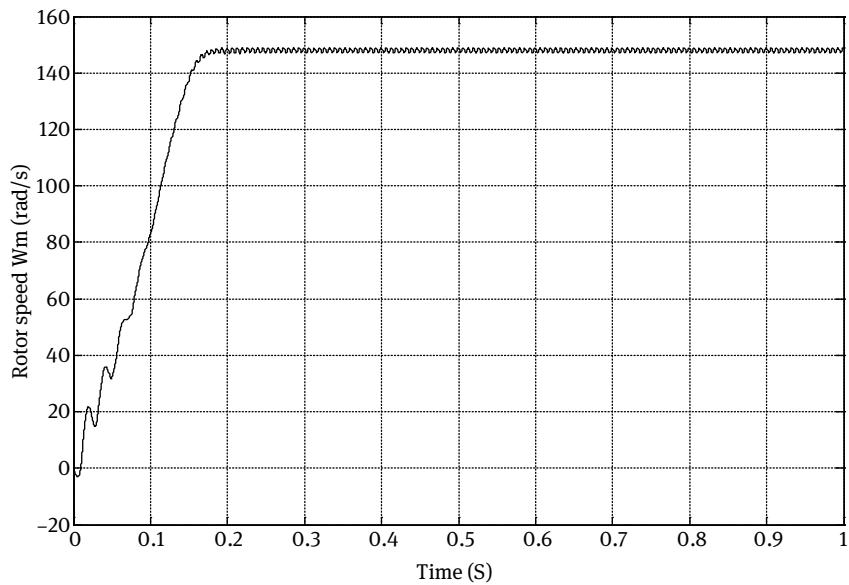


Fig. 8.13: Speed response of the three-level inverter fed induction motor.

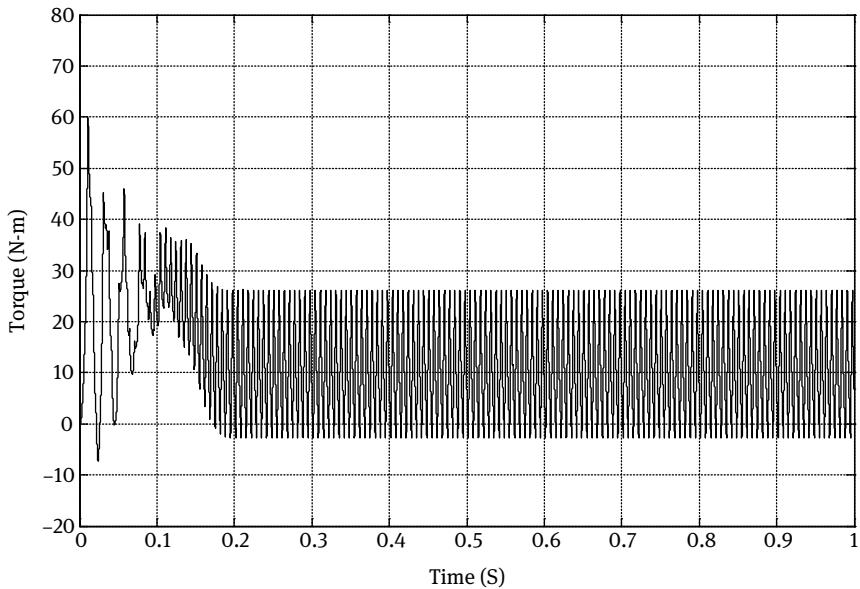


Fig. 8.14: Torque response of the three-level inverter fed induction motor.

8.4.2 Five-level inverter

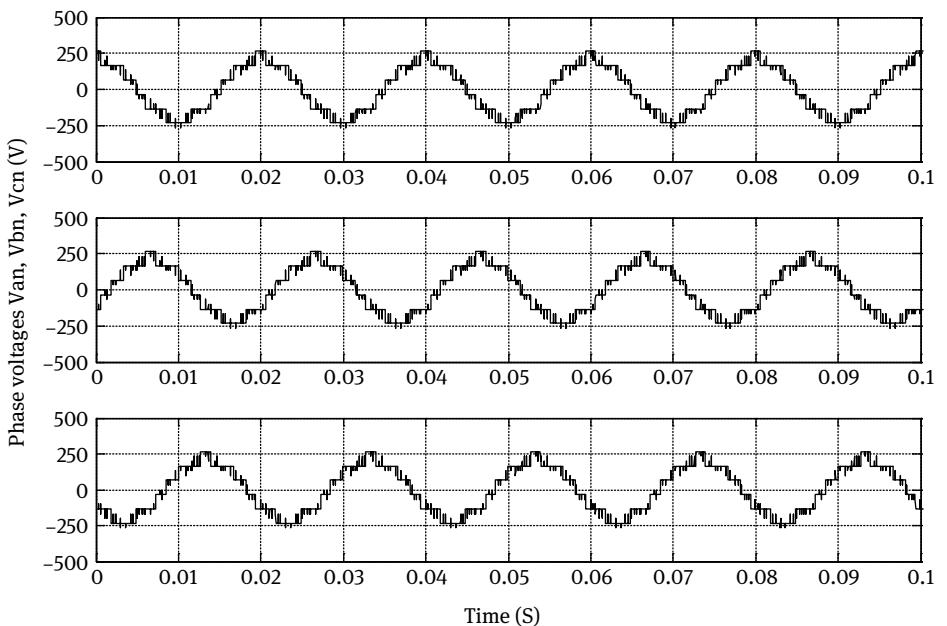


Fig. 8.15: Phase voltages of the five-level inverter.

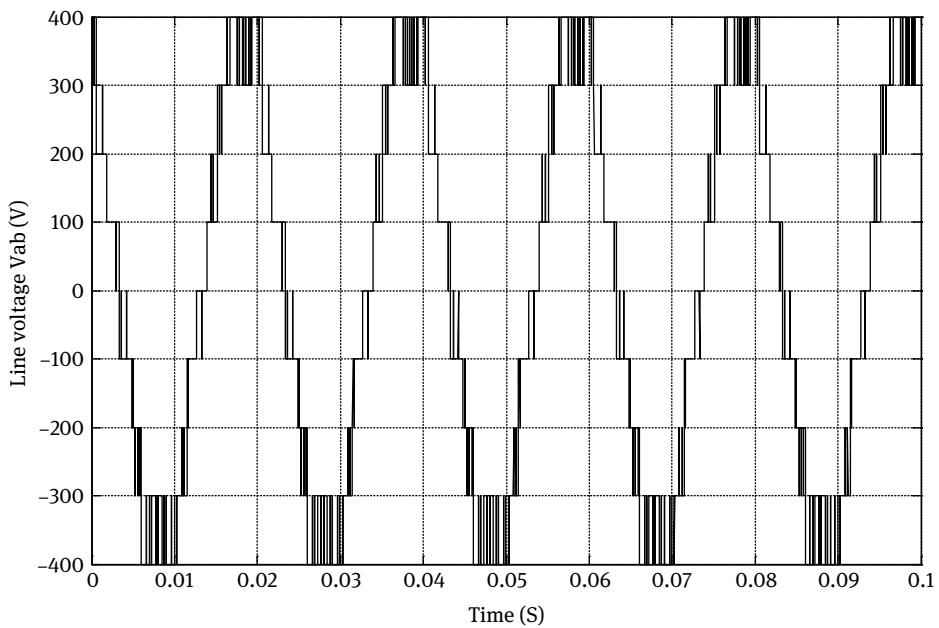


Fig. 8.16: Line-to-line voltage of the five-level inverter.

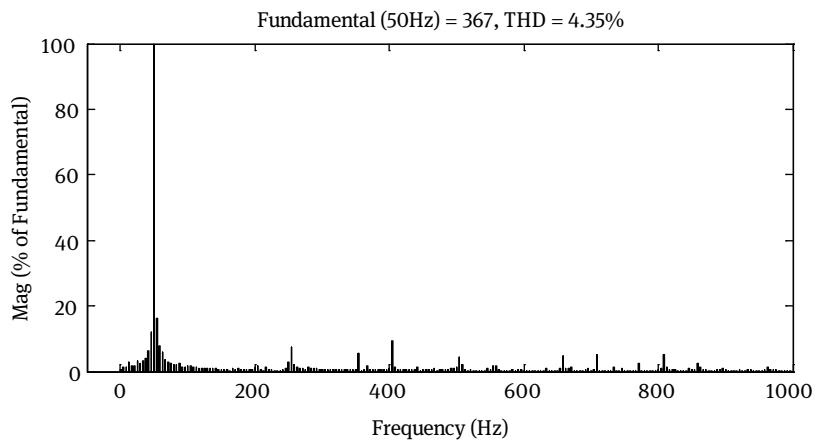


Fig. 8.17: Output line voltage harmonic spectrum of the five-level inverter.

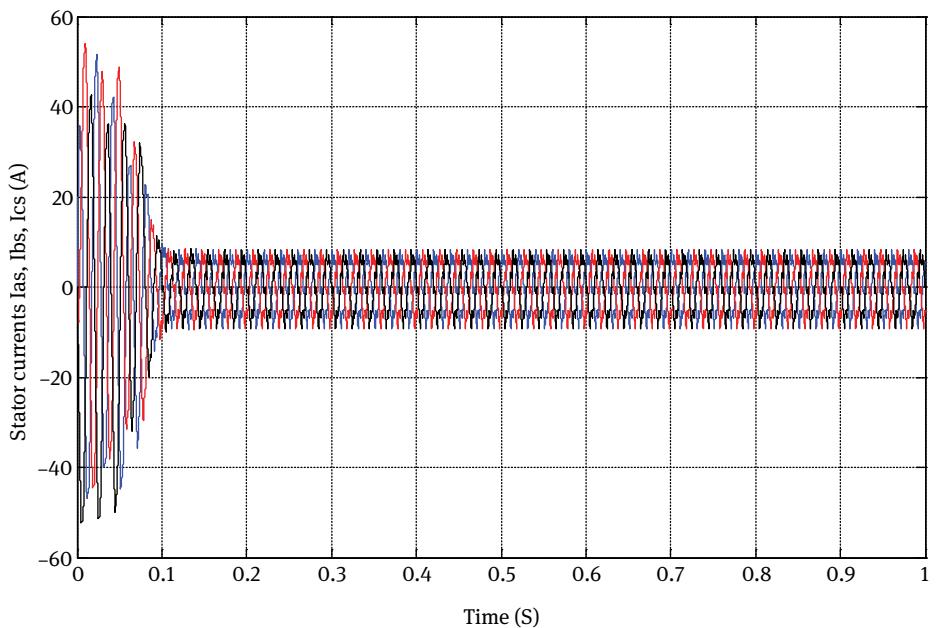


Fig. 8.18: Stator currents of the five-level inverter fed induction motor.

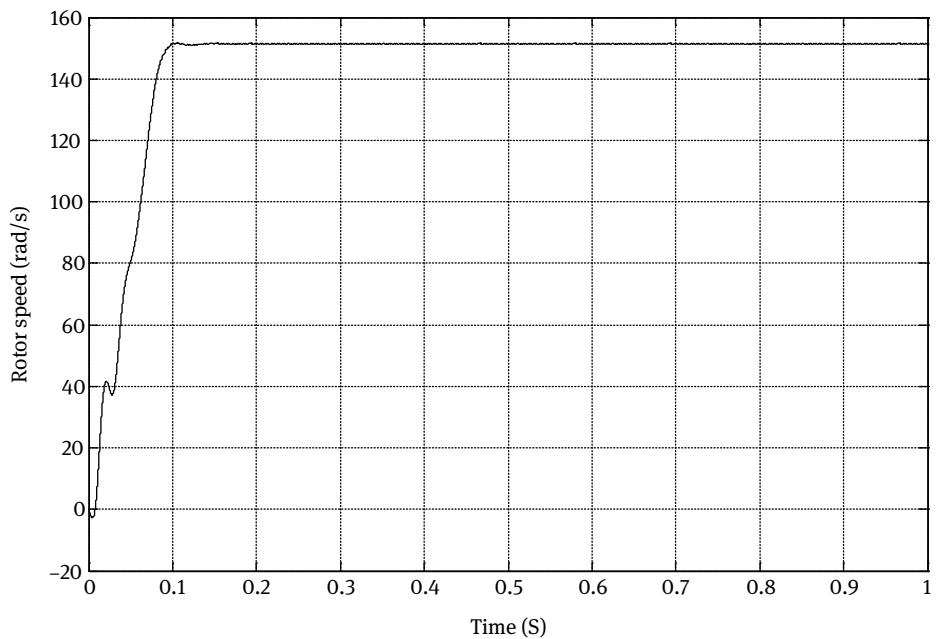


Fig. 8.19: Speed response of the five-level inverter fed induction motor.

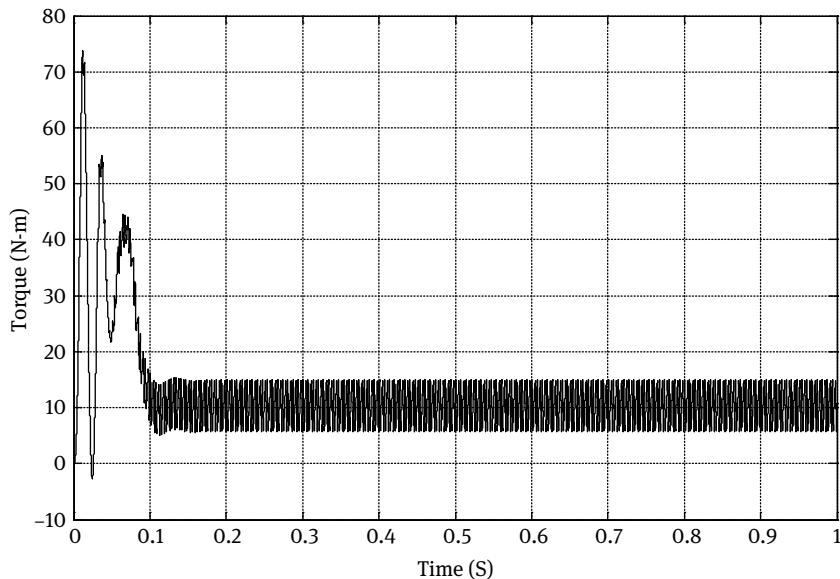


Fig. 8.20: Torque response of the five-level inverter fed induction motor.

8.4.3 Seven-level inverter

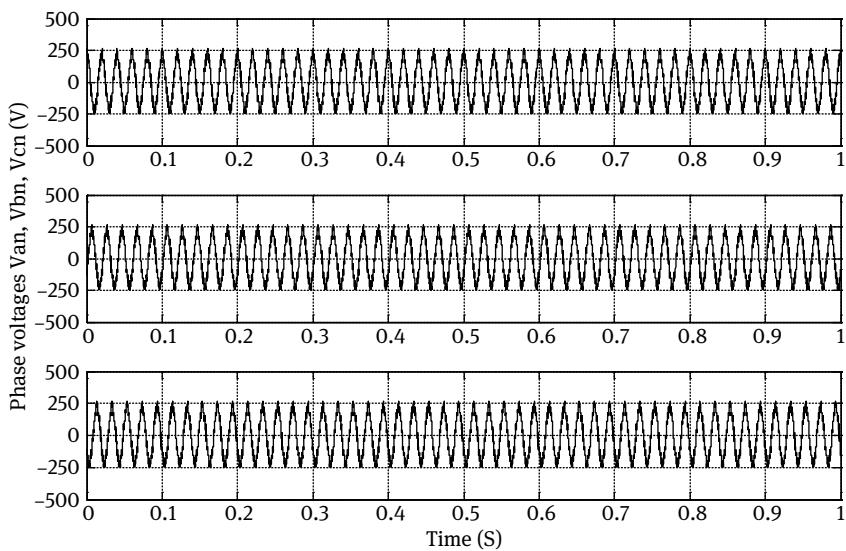


Fig. 8.21: Phase voltages of the seven-level inverter.

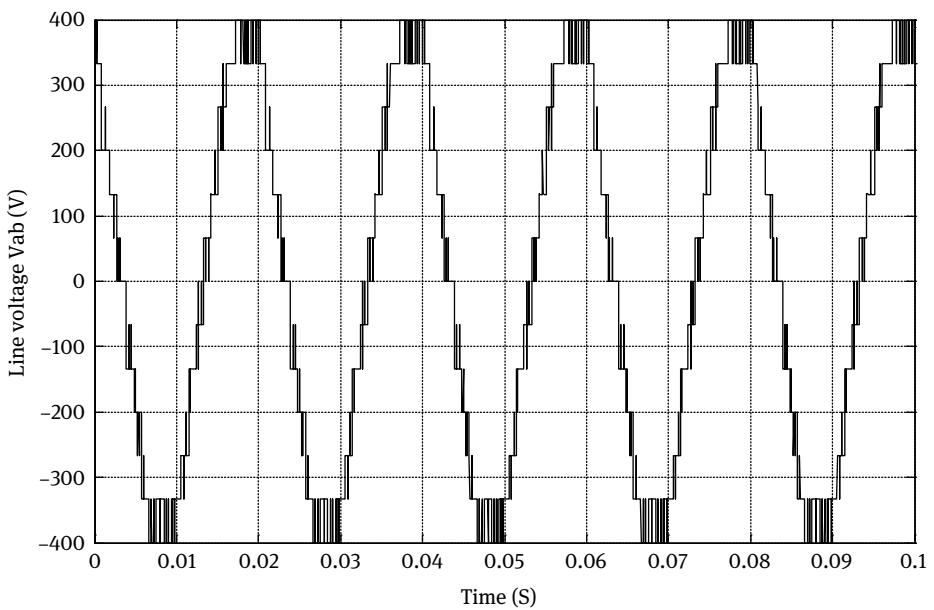


Fig. 8.22: Line-to-line voltage of the seven-level inverter.

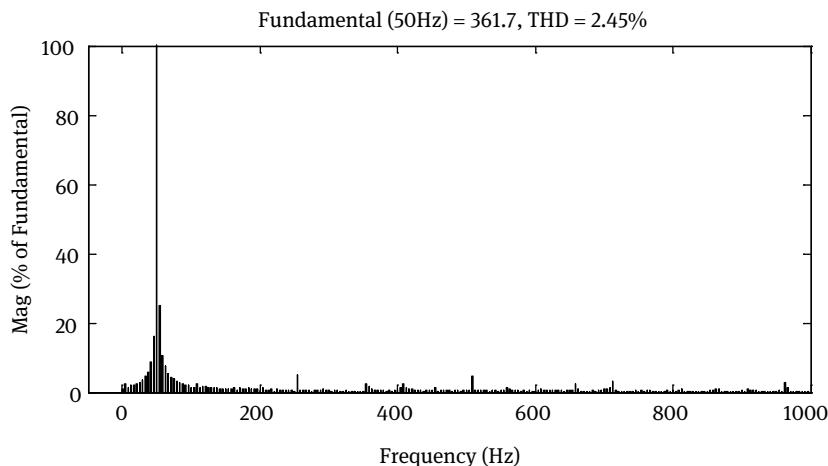


Fig. 8.23: Output line voltage harmonic spectrum of the seven-level inverter.

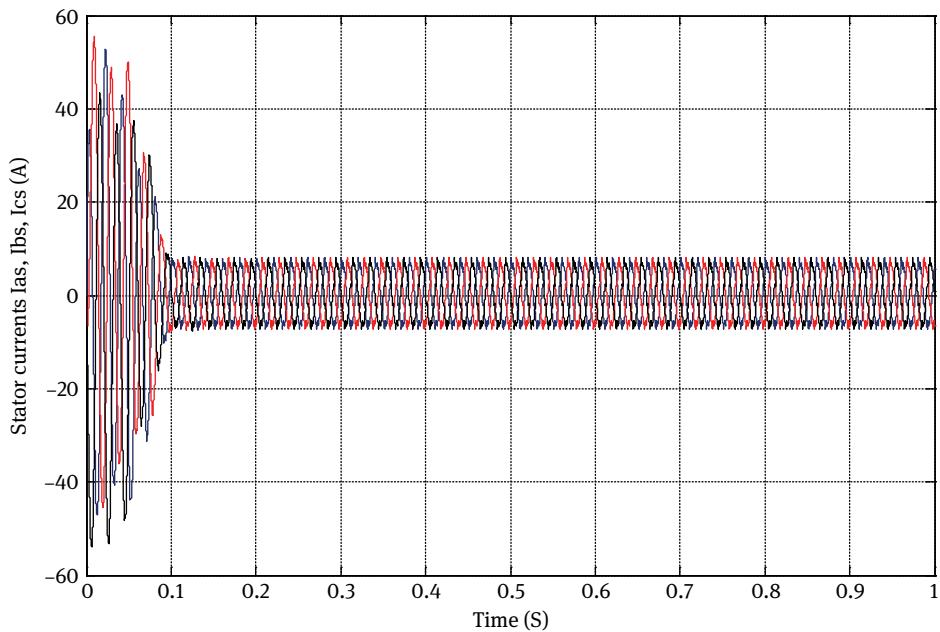


Fig. 8.24: Stator currents of the seven-level inverter fed induction motor.

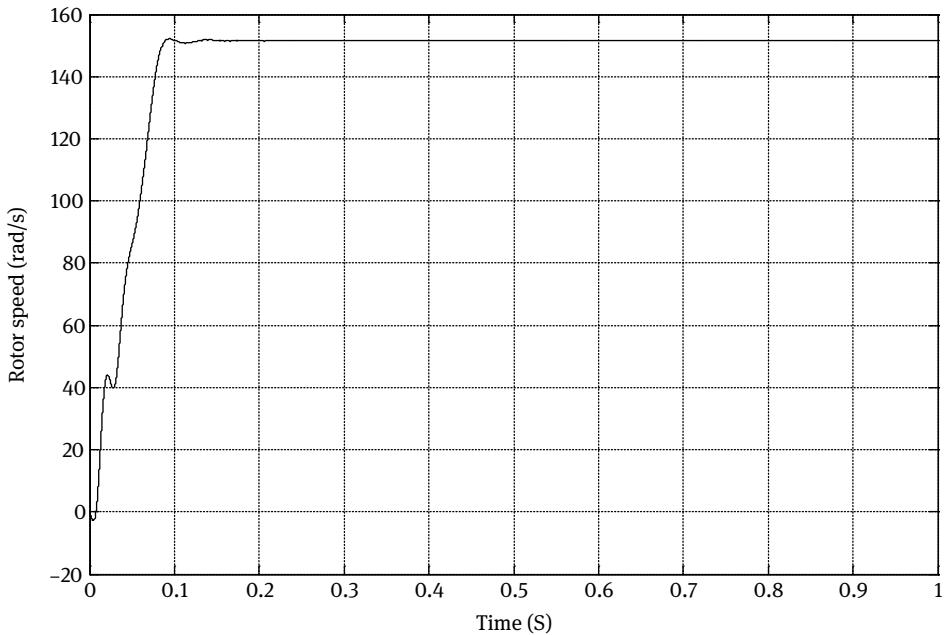


Fig. 8.25: Speed response of the seven-level inverter fed induction motor.

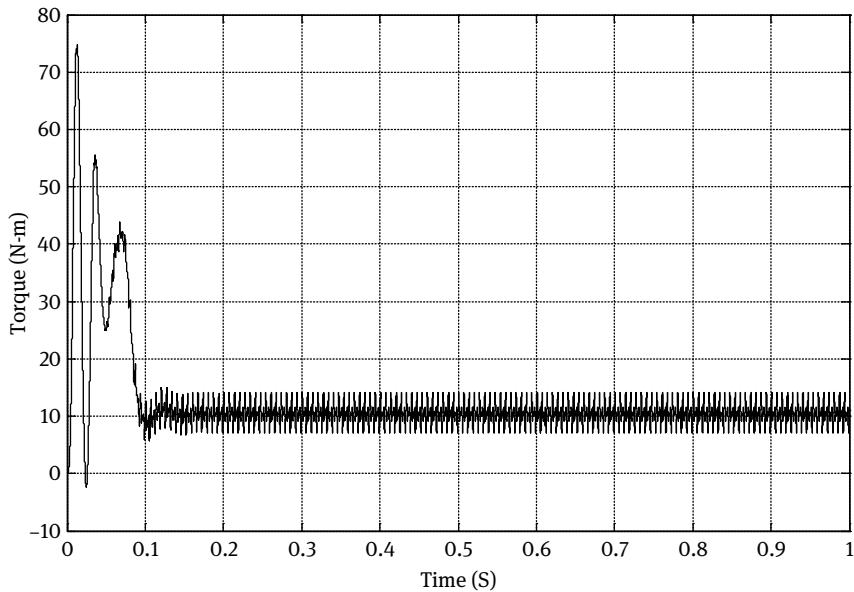


Fig. 8.26: Torque response of the seven-level inverter fed induction motor.

8.4.4 Nine-level inverter

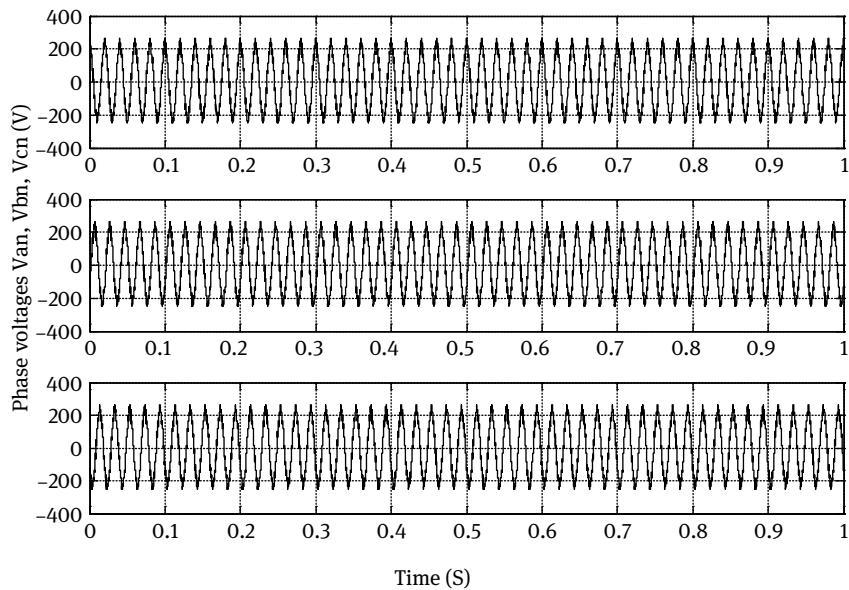


Fig. 8.27: Phase voltages of the nine-level inverter.

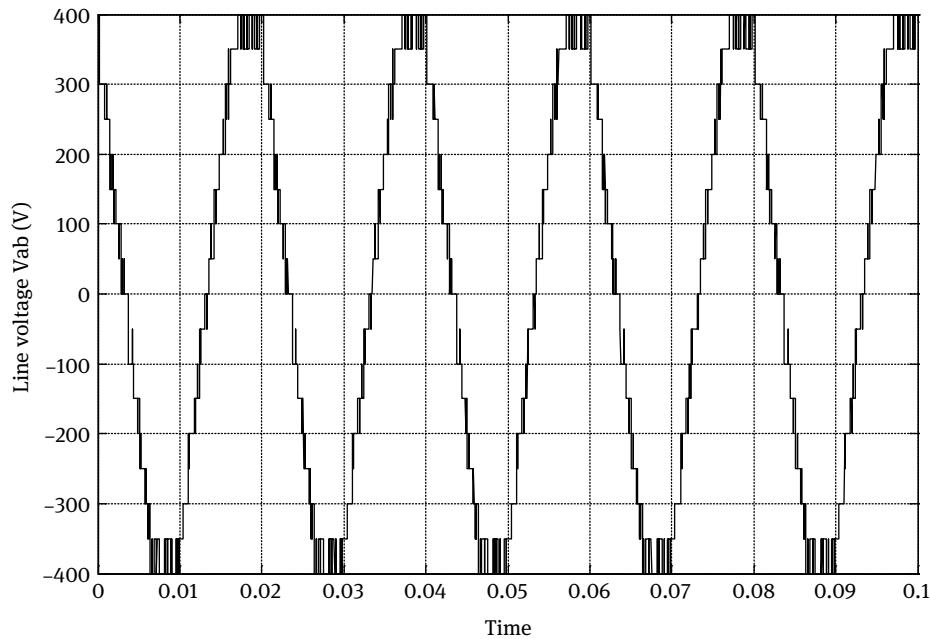


Fig. 8.28: Line-to-line voltage of the nine-level inverter.

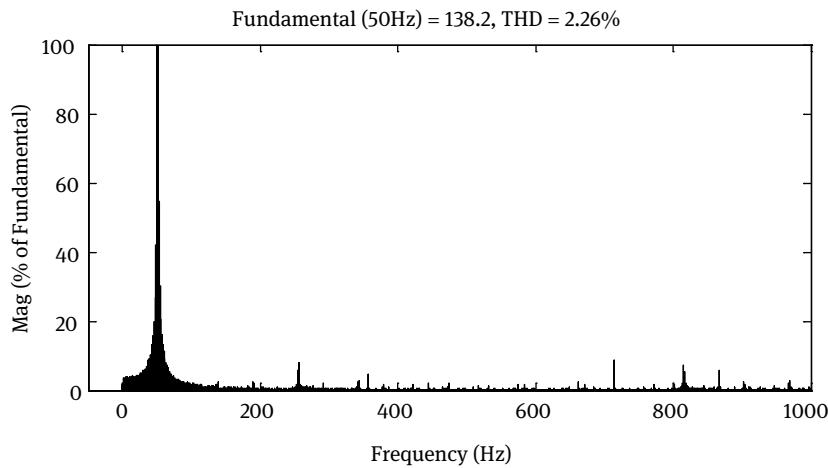


Fig. 8.29: Output line voltage harmonic spectrum of the nine-level inverter.

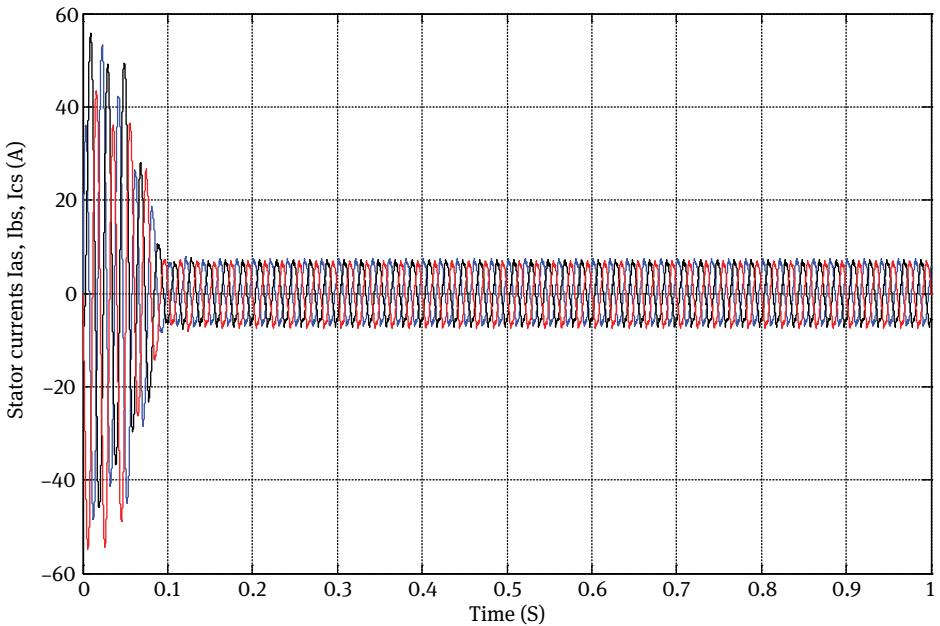


Fig. 8.30: Stator currents of the nine-level inverter fed induction motor.

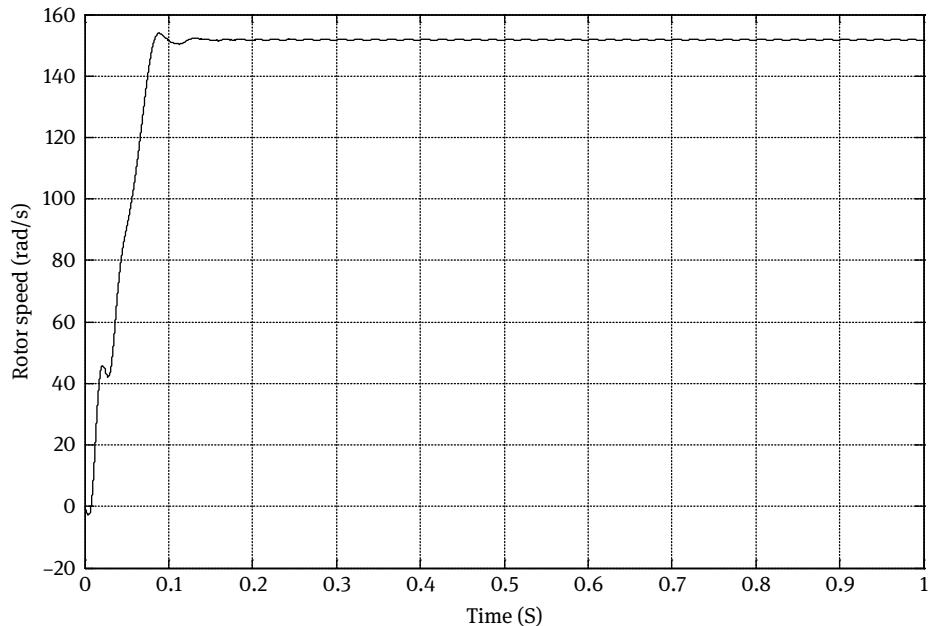


Fig. 8.31: Speed response of the nine-level inverter fed induction motor.

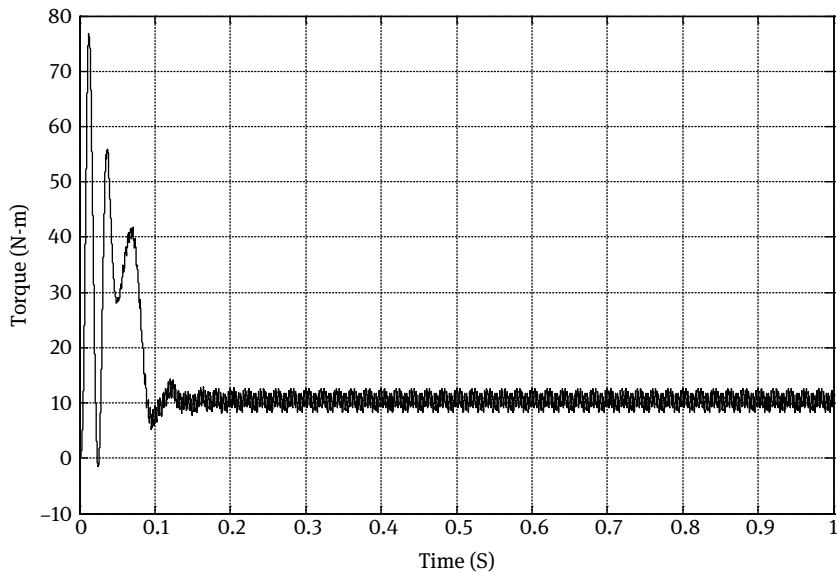


Fig. 8.32: Torque response of the nine-level inverter fed induction motor.

8.4.5 Eleven-level inverter

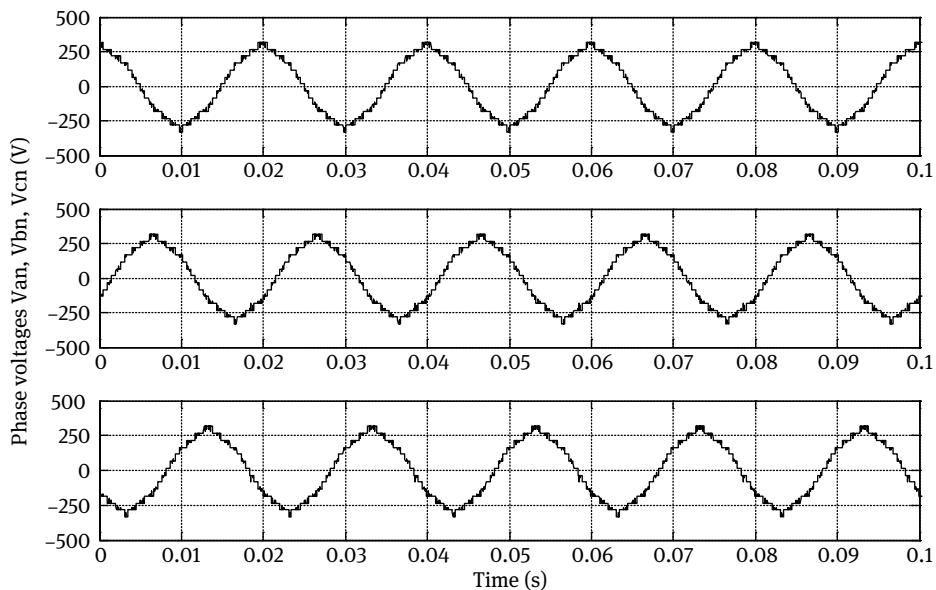


Fig. 8.33: Phase voltages of the eleven-level inverter.

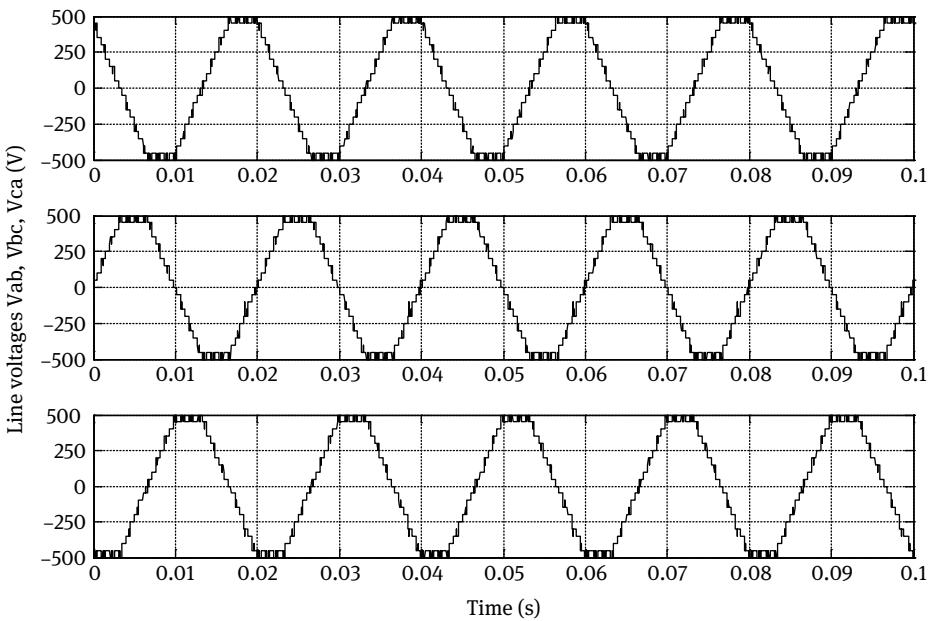


Fig. 8.34: Line-to-line voltages of the eleven-level inverter.

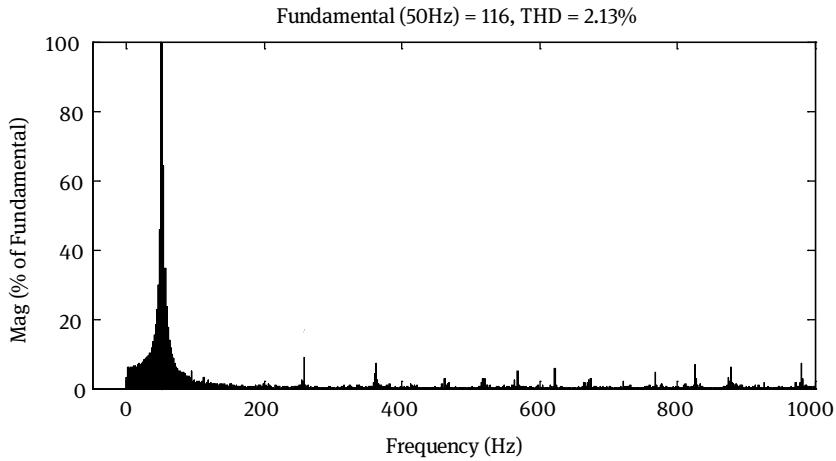


Fig. 8.35: Output line voltage harmonic spectrum of the eleven-level inverter.

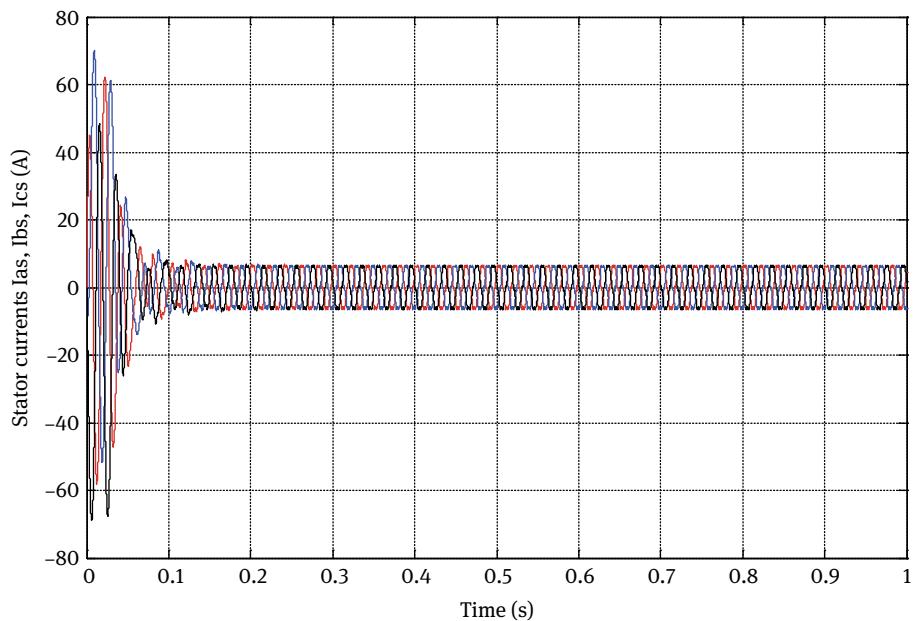


Fig. 8.36: Stator currents of the eleven-level inverter fed induction motor.

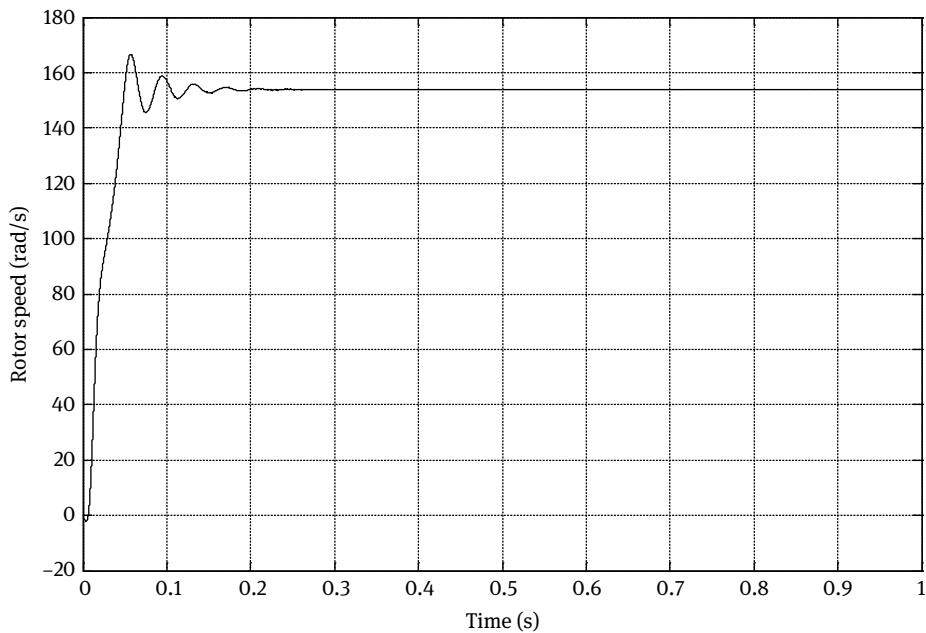


Fig. 8.37: Speed response of the eleven-level inverter fed induction motor.

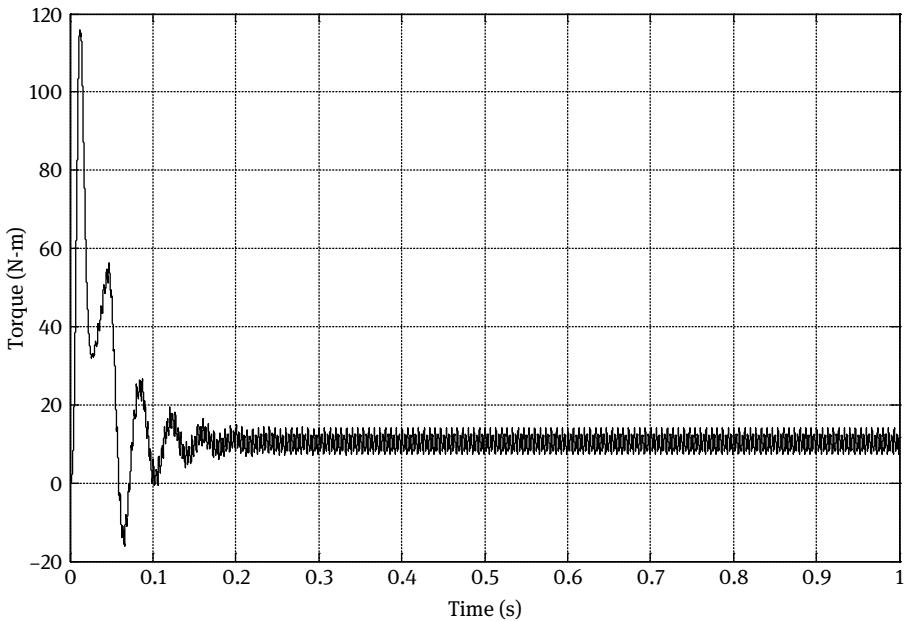


Fig. 8.38: Torque response of the eleven-level inverter fed induction motor.

Tab. 8.7: Performance of multilevel inverters.

S.No.	Level of inverter	THD (%)	Speed (rpm)	Torque ripple (%)
1	Three	16.92	1415	9.2
2	Five	4.35	1440	7.8
3	Seven	2.45	1445	6.5
4	Nine	2.26	1450	4.2
5	Eleven	2.13	1453	3.8

8.5 Conclusions

An analytical SVPWM algorithm for multilevel inverter fed induction motor is based on two-level inverter is proposed and described in detail. An intrinsic relationship between multilevel and two-level inverters is developed, and using linear transformation, the switching time of vectors for the two-level inverter can be transformed for the multilevel inverter. A novel classification of voltage vectors is proposed to determine switching sequence. This method can be extended for the N-level inverter also. The results shows that the output voltage THD for the three-, five-, seven-, nine-, and eleven-level inverters is 16.92%, 4.35%, 2.45%, 2.26%, and 2.13%, respectively as shown in Tab. 8.7. As the level of the inverter increases, the THD and the torque ripples are effectively decreased and the rotor speed is improved.

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Appendices

Appendix I

Simulation parameters are as follows:

SVPWM parameters:

Modulation index $m = 0.8$

dc supply voltage = 300 V

No. of switching intervals $n = 48$

Sampling frequency = 2400 Hz

Sampling time $T_s = 4.166 \text{ e}^{-4}$ seconds

Three-phase induction motor:

3 HP, 220 V, 50 Hz, 4 poles, 1500 rpm

$R_s = 0.55 \Omega$; $R_r = 0.78 \Omega$

$L_s = 93.38 \text{ mH}$; $L_r = 93.36 \text{ mH}$

$L_m = 90.5 \text{ mH}$

$J = 0.019 \text{ kg-m}^2$

$F_r = 0.000051 \text{ N-m/rad/s}$

$T_L = 10.32 \text{ N-m}$

Appendix II

Simulation parameters are as follows:

SVPWM parameters:

Modulation index $m = 0.8$

dc-link voltage = 400 V

No. of switching intervals $n = 72$

Sampling frequency = 3600 Hz

Sampling time $T_s = 2.7778 \text{ e}^{-4}$ seconds

Three-phase induction motor:

3 HP, 400 V, 50 Hz, 4 poles, 1500 rpm

$R_s = 1.405 \Omega$; $R_r = 1.395 \Omega$

$L_s = 5.839 \text{ mH}$; $L_r = 5.839 \text{ mH}$

$L_m = 172.2 \text{ mH}$

$J = 0.0131 \text{ kg-m}^2$

$F_r = 0.002985 \text{ N-m/rad/s}$

$T_L = 10.00 \text{ N-m}$

Appendix III

Simulation parameters are as follows:

SVPWM parameters:

Modulation index $m = 0.8$

dc-link voltage = 400 V

No. of switching intervals $n = 192$

Sampling frequency = 9600 Hz

Sampling time $T_s = 1.0417 \times 10^{-4}$ seconds

Three-phase induction motor:

2 HP, 400 V, 1500 W, 50 Hz, 4 poles, 1430 rpm

$R_s = 1.405 \Omega$; $R_r = 1.395 \Omega$; $L_s = 5.839 \text{ mH}$; $L_r = 5.839 \text{ mH}$; $L_m = 143 \text{ mH}$

$J = 0.0131 \text{ kg-m}^2$; $F_r = 0.002985 \text{ N-m/rad/s}$; $T_L = 10.00 \text{ N-m}$

- The conditions for identifying reference vector location in multilevel inverters and corrections required to duty cycles are given in Tabs. A6.1, A6.2, and A6.3.

Tab. A6.1: Location of the reference vector and corrected duty cycles of the three-level inverter.

Region	Condition for location of the reference vector	Corrected m_1 , m_2 , and m_3 for the switching states
2	$m_1 > 0.5$	$m_1 = m_1 - 0.5$ $m_2 = m_2$ $m_3 = 1 - m_1 - m_2$;
3	$m_1 < 0.5, m_2 < 0.5$ and $m_1 + m_2 > 0.5$	$m_1 = 0.5 - m_1$ $m_2 = 0.5 - m_2$ $m_3 = m_1 + m_2 - 0.5$;
4	$m_2 > 0.5$	$m_1 = m_1$ $m_2 = m_2 - 0.5$ $m_3 = 1 - m_1 - m_2$;

Tab. A6.2: Location of the reference vector and corrected duty cycles of the four-level inverter.

Region	Condition for location of the reference vector	Corrected m_1 , m_2 , and m_3 for the switching states
5	$0.66 < m_1 < 1$ and $m_2 < 0.33$ and $m_1 + m_2 < 1$	$m_1 = m_1 - 0.66$ $m_2 = m_2$ $m_3 = 1 - m_1 - m_2$;
6	$0.33 < m_1 < 0.66$ and $m_2 < 0.33$ and $m_1 + m_2 > 0.66$	$m_1 = 0.66 - m_1$; $v = 0.33 - m_2$ $m_3 = m_1 + m_2 - 0.66$;
7	$0.33 < m_1 < 0.66$ and $0.33 < m_2 < 0.66$ and $m_1 + m_2 < 1$	$m_1 = m_1 - 0.33$ $m_2 = m_2 - 0.33$ $m_3 = 1 - m_1 - m_2$;

Tab. A6.2 (continued)

Region	Condition for location of the reference vector	Corrected m_1 , m_2 , and m_3 for the switching states
8	$m_1 < 0.33$ and $0.33 < m_2 < 0.66$ and $m_1 + m_2 > 0.66$	$m_1 = 0.33 - m_1$ $m_2 = 0.66 - m_2$ $m_3 = m_1 + m_2 - 0.66;$
9	$m_1 < 0.33$ and $0.66 < m_2 < 1$ and $m_1 + m_2 < 1$	$m_1 = m_1$ $m_2 = m_2 - 0.66$ $m_3 = 1 - m_1 - m_2;$

Tab. A6.3: Location of the reference vector and corrected duty cycles of five-level inverter.

Region	Condition for location of the reference vector	Corrected m_1 , m_2 , and m_3 for the switching states
10	$0.75 < m_1 < 1$ and $m_2 < 0.25$ and $m_1 + m_2 < 1$	$m_1 = m_1 - 0.75$; $m_2 = m_2$; $m_3 = 1 - m_1 - m_2$
11	$0.5 < m_1 < 0.75$ and $m_2 < 0.25$ and $m_1 + m_2 > 0.75$	$m_1 = 0.75 - m_1$; $m_2 = 0.25 - m_2$; $m_3 = m_1 + m_2 - 0.75$
12	$0.5 < m_1 < 0.75$ and $0.25 < m_2 < 0.5$ and $m_1 + m_2 < 1$	$m_1 = m_1 - 0.5$; $m_2 = m_2 - 0.25$; $m_3 = 1 - m_1 - m_2$
13	$0.25 < m_1 < 0.5$ and $0.25 < m_2 < 0.5$ and $m_1 + m_2 > 0.75$	$m_1 = 0.5 - m_1$; $m_2 = 0.5 - m_2$; $m_3 = m_1 + m_2 - 0.75$
14	$0.25 < m_1 < 0.5$ and $0.5 < m_2 < 0.75$ and $m_1 + m_2 < 1$	$m_1 = m_1 - 0.25$; $m_2 = m_2 - 0.5$; $m_3 = 1 - m_1 - m_2$
15	$m_1 < 0.25$ and $0.5 < m_2 < 0.75$ and $m_1 + m_2 > 0.75$	$m_1 = 0.25 - m_1$; $m_2 = 0.75 - m_2$; $m_3 = m_1 + m_2 - 0.75$
16	$m_1 < 0.25$ and $0.75 < m_2 < 1$ and $m_1 + m_2 < 1$	$m_1 = m_1$; $m_2 = m_2 - 0.75$; $m_3 = 1 - m_1 - m_2$

2. The look-up tables for multilevel inverters

Tab. A6.4: Switching sequence of the two-level inverter.

Sector	Region	ON sequence					OFF sequence				
1	1	000	100	110	111		111	110	100	000	
2	2	000	010	110	111		111	110	010	000	
3	3	000	010	011	111		111	011	010	000	
4	4	000	001	011	111		111	011	001	000	
5	5	000	001	101	111		111	101	001	000	
6	6	000	100	101	111		111	101	100	000	

Tab. A6.5: Switching sequence of the three-level inverter.

Sector	Region	ON sequence					OFF sequence			
1	1	000	100	110	111		111	110	100	000
	2	100	200	210	211		211	210	200	100
	3	100	110	210	200		200	210	110	100
	4	110	210	220	221		221	220	210	110
2	5	111	110	010	000		000	010	110	111
	6	221	220	120	110		110	120	220	221
	7	221	121	120	110		110	120	121	221
	8	121	120	020	010		010	020	120	121
3	9	111	121	122	222		222	122	121	111
	10	010	020	021	121		121	021	020	010
	11	010	011	021	121		121	021	011	010
	12	011	021	022	122		122	022	021	011
4	13	111	011	001	000		000	001	011	111
	14	122	022	012	011		011	012	022	122
	15	122	112	012	011		011	012	112	122
	16	112	012	002	001		001	002	012	112
5	17	000	001	101	111		111	101	001	000
	18	001	002	102	112		112	102	002	001
	19	001	101	102	112		112	102	101	001
	20	101	102	202	212		212	202	102	101
6	21	111	101	100	000		000	100	101	111
	22	212	202	201	101		101	201	202	212
	23	101	201	211	212		212	211	201	101
	24	100	200	201	211		211	201	200	100

Tab. A6.6: Switching sequence of the four-level inverter.

Sector	Region	ON sequence					OFF sequence			
1	1	000	100	110	111		111	110	100	000
	2	100	200	210	211		211	210	200	100
	3	100	110	210	211		211	210	110	100
	4	110	210	220	221		221	220	210	110
	5	200	300	310	311		311	310	300	200
	6	200	210	310	311		311	310	210	200
	7	210	310	320	321		321	320	310	210
	8	210	220	320	321		321	320	220	210
	9	220	320	330	331		331	330	320	220

Tab. A6.6 (continued)

Sector	Region	ON sequence					OFF sequence			
2	10	222	232	332	333	333	332	232	222	
	11	221	231	331	332	332	331	231	221	
	12	221	121	120	110	110	120	121	221	
	13	121	131	231	232	232	231	131	121	
	14	220	230	330	331	331	330	230	220	
	15	220	230	231	331	331	231	230	220	
	16	120	130	230	231	231	230	130	120	
	17	120	130	131	231	231	131	130	120	
	18	020	030	130	131	131	130	030	020	
3	19	000	010	011	111	111	011	010	000	
	20	010	020	021	121	121	021	020	010	
	21	010	011	021	121	121	021	011	010	
	22	011	021	022	122	122	022	021	011	
	23	020	030	031	131	131	031	030	020	
	24	020	021	031	131	131	031	021	020	
	25	021	031	032	132	132	032	031	021	
	26	021	022	032	132	132	032	022	021	
	27	022	032	033	133	133	033	032	022	
4	28	222	223	233	333	333	233	223	222	
	29	122	022	012	011	011	012	022	122	
	30	122	123	223	233	233	223	123	122	
	31	112	113	123	223	223	123	113	112	
	32	022	023	033	133	133	033	023	022	
	33	022	023	123	133	133	123	023	022	
	34	012	013	023	123	123	023	013	012	
	35	012	013	113	123	123	113	013	012	
	36	002	003	013	113	113	013	003	002	
5	37	000	001	101	111	111	101	001	000	
	38	001	002	102	112	112	102	002	001	
	39	001	101	102	112	112	102	101	001	
	40	101	102	202	212	212	202	102	101	
	41	002	003	103	113	113	103	003	002	
	42	002	102	103	113	113	103	102	002	
	43	102	103	203	213	213	203	103	102	
	44	102	202	203	213	213	203	202	102	
	45	202	203	303	313	313	303	203	202	
6	46	222	322	323	333	333	323	322	222	
	47	212	202	201	101	101	201	202	212	
	48	212	312	322	323	323	322	312	212	
	49	211	311	312	322	322	312	311	211	
	50	202	302	303	313	313	303	302	202	
	51	202	302	312	313	313	312	302	202	
	52	201	301	302	312	312	302	301	201	
	53	201	301	311	312	312	311	301	201	
	54	200	300	301	311	311	301	300	200	

Tab. A6.7: Switching sequence of the five-level inverter.

Sector	Region	ON sequence					OFF sequence			
1	1	222	322	332	333	333	332	322	222	
	2	322	422	432	433	433	432	422	322	
	3	322	332	432	433	433	432	332	322	
	4	332	432	442	443	443	442	432	332	
	5	311	411	421	422	422	421	411	311	
	6	311	321	421	422	422	421	321	311	
	7	321	421	431	432	432	431	421	321	
	8	321	331	431	432	432	431	331	321	
	9	331	431	441	442	442	441	431	331	
	10	300	400	410	411	411	410	400	300	
	11	300	310	410	411	411	410	310	300	
	12	310	410	420	421	421	420	410	310	
	13	310	320	420	421	421	420	320	310	
	14	320	420	430	431	431	430	420	320	
	15	320	330	430	431	431	430	330	320	
	16	330	430	440	441	441	440	430	330	
2	17	333	343	443	444	444	443	343	333	
	18	332	342	442	443	443	442	342	332	
	19	332	342	343	443	443	343	342	332	
	20	232	242	342	343	343	342	242	232	
	21	331	341	441	442	442	441	341	331	
	22	331	341	342	442	442	342	341	331	
	23	231	241	341	342	342	341	241	231	
	24	231	241	242	342	231	242	241	231	
	25	131	141	241	242	131	241	141	131	
	26	330	340	440	441	330	440	340	330	
	27	330	340	341	441	330	341	340	330	
	28	230	240	340	341	230	340	240	230	
	29	230	240	241	341	230	241	240	230	
	30	130	140	240	241	130	240	140	130	
	31	130	140	141	241	130	141	140	130	
	32	030	040	140	141	030	140	040	030	
3	33	000	010	011	111	000	011	010	000	
	34	010	020	021	121	010	021	020	010	
	35	010	011	021	121	010	021	011	010	
	36	011	021	022	122	011	022	021	011	
	37	131	141	142	242	131	142	141	131	
	38	132	142	242	243	132	242	142	132	
	39	132	142	143	243	132	143	142	132	
	40	133	143	243	244	244	243	143	133	
	41	133	143	144	244	244	144	143	133	
	42	030	040	041	141	141	041	040	030	
	43	031	041	141	142	142	141	041	031	
	44	031	041	042	142	142	042	041	031	

Tab. A6.7 (continued)

Sector	Region	ON sequence					OFF sequence		
	45	032	042	142	143	143	142	042	032
	46	032	042	043	143	143	043	042	032
	47	033	043	143	144	144	143	043	033
	48	033	043	044	144	144	044	043	033
4	49	333	334	344	444	444	344	334	333
	50	233	234	244	344	344	244	234	233
	51	223	123	122	112	112	122	123	223
	52	223	224	234	334	334	234	224	223
	53	133	134	144	244	244	144	134	133
	54	123	133	144	244	244	144	133	123
	55	123	124	134	234	234	134	124	123
	56	113	123	124	224	224	124	123	113
	57	113	114	124	224	224	124	114	113
	58	033	034	044	144	144	044	034	033
	59	023	033	034	134	134	034	033	023
	60	023	024	034	134	134	034	024	023
	61	013	023	024	124	124	024	023	013
	62	013	014	024	124	124	024	014	013
	63	003	013	014	114	114	014	013	003
	64	003	004	014	114	114	014	004	003
5	65	000	001	101	111	111	101	001	000
	66	001	002	102	112	112	102	002	001
	67	001	101	102	112	112	102	101	001
	68	101	102	202	212	212	202	102	101
	69	103	113	114	214	214	114	113	103
	70	102	103	113	213	213	113	103	102
	71	102	103	203	213	213	203	103	102
	72	202	203	213	313	313	213	203	202
	73	202	203	303	313	313	303	203	202
	74	003	004	104	114	114	104	004	003
	75	003	103	104	114	114	104	103	003
	76	103	104	204	214	214	204	104	103
	77	103	203	204	214	214	204	203	103
	78	203	204	304	314	314	304	204	203
	79	203	303	304	314	314	304	303	203
	80	303	304	404	414	414	404	304	303
6	81	333	433	434	444	444	434	433	333
	82	323	423	424	434	434	424	423	323
	83	323	423	433	434	434	433	423	323
	84	322	422	423	433	433	423	422	322
	85	302	303	313	413	413	313	303	302
	86	302	312	313	413	413	313	312	302
	87	312	412	413	423	423	413	412	312

Tab. A6.7 (continued)

Sector	Region	ON sequence				OFF sequence			
	88	312	412	422	423	423	422	412	312
	89	311	411	412	312	312	412	411	311
	90	303	403	404	414	414	404	403	303
	91	303	403	413	414	414	413	403	303
	92	302	402	403	413	413	403	402	302
	93	302	402	412	413	413	412	402	302
	94	301	401	402	412	412	402	401	301
	95	301	401	411	412	412	411	401	301
	96	300	400	401	411	411	401	400	300

Appendix IV

The simulation parameters are as follows:

SVPWM parameters:

Modulation index $m = 0.8$

dc-link voltage = 400 V

No. of switching intervals $n = 72$

Sampling frequency = 3600 Hz

Sampling time $T_s = 2.7778 \text{ e}^{-4}$ seconds

Three-phase induction motor:

5.4 HP, 400 V, 50 Hz, 4 poles, 1430 rpm

$R_s = 1.405 \Omega$; $R_r = 1.395 \Omega$

$L_s = 5.839 \text{ mH}$; $L_r = 5.839 \text{ mH}$

$L_m = 172.2 \text{ mH}$

$J = 0.0131 \text{ kg-m}^2$

$F_r = 0.002985 \text{ N-m/rad/s}$

$T_L = 10.00 \text{ N-m}$

Appendix V

The simulation parameters are as follows:

SVPWM parameters:

Modulation index $m = 0.8$

dc-link voltage = 400 V/500 V (eleven-level inverter)

No. of switching intervals $n = 66$

Sampling frequency = 3300 Hz

Sampling time $T_s = 3.0303 \text{ e}^{-4}$ seconds

Three-phase induction motor:

2 HP, 400 V, 1500 W, 50 Hz, 4 poles, 1500 rpm

$R_s = 1.405 \Omega$; $R_r = 1.395 \Omega$

$L_s = 5.839 \text{ mH}$; $L_r = 5.839 \text{ mH}$

$L_m = 172.2 \text{ mH}$

$J = 0.0131 \text{ kg-m}^2$

$F_r = 0.002985 \text{ N-m/rad/s}$

$T_L = 10.00 \text{ N-m}$

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