DAC YF GCN-RL Circuit Designer: Transistor Sizing with GNN & RL

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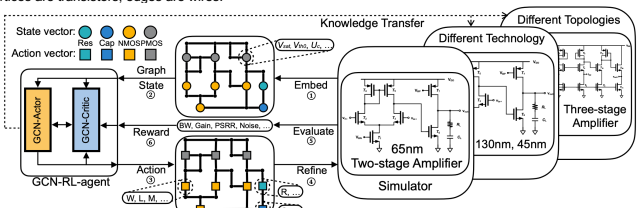
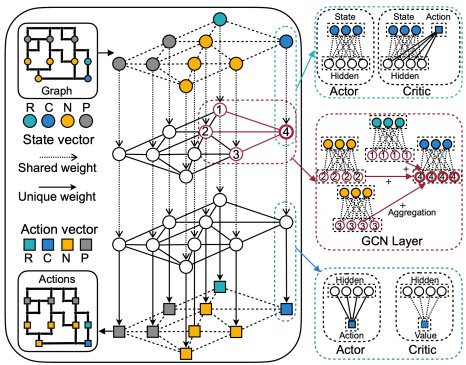
Overview

Although there have been plenty of work on transistor sizing targeting one circuit, limited research has been done on transferring knowledge from one circuit to another to reduce re-design overhead. We leverage Reinforcement Learning (RL) algorithm to conduct knowledge transfer between different technology nodes and schematics. Moreover, inspired by the fact that ***circuit is a graph***, we propose to learn on the schematic graph with Graph Convolutional Neural Networks (GCN). The GCN-RL agent extracts the features on the schematic graph, whose vertices are transistors, edges are wires.



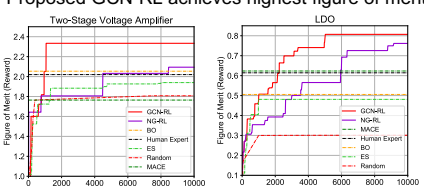
GCN-RL Overview: (1) The circuit schematic is embedded into a graph, where the nodes are the transistors, the edges are wires. Then simulator generates a state vector for each transistor. (2) The GCN extract features from the graph and feed the states (the top graph with circle vertices) to the RL agent. (3) The RL agent processes each vertex and generates an action vector for each vertex, which is passed to the graph (the bottom graph with square vertices). (4) Then the environment de-normalizes and refines the actions. (5) The simulator simulates the circuit, (6) computes a FoM value (the reward) and returns it to the RL agent to update the RL agent.

Proposed GCN-RL Agent

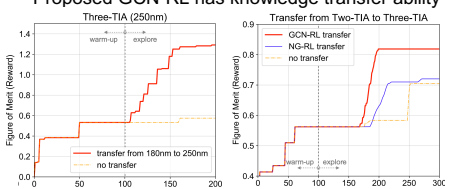


The proposed GCN-RL agent. The actor network generates the parameters for circuits. The critic network estimates whether the generated parameters have good performance.

Proposed GCN-RL achieves highest figure of merits



Proposed GCN-RL has knowledge transfer ability



Conclusions

1. GCN-RL consistently achieves higher Figure of Merits (FoMs) on four different circuits than conventional black box optimization methods (BO, ES, random search);

2. GCN-RL has the transfer ability between technology nodes and schematics.

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