Improving Robustness of Quantum Computing with Machine Learning

A Hybrid Classical-Quantum Computer System Perspective

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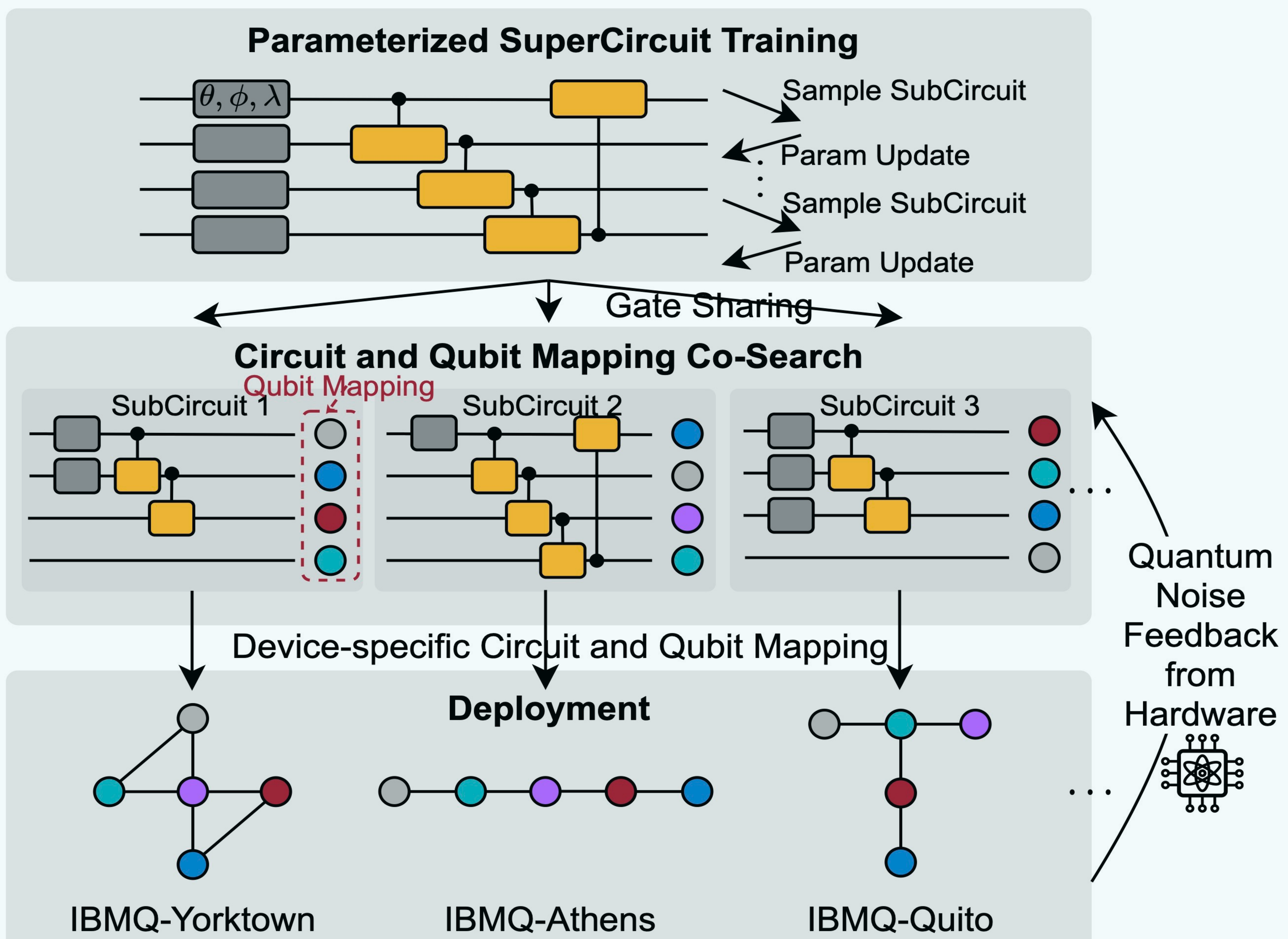
Near-Term: Variational Quantum Algorithms

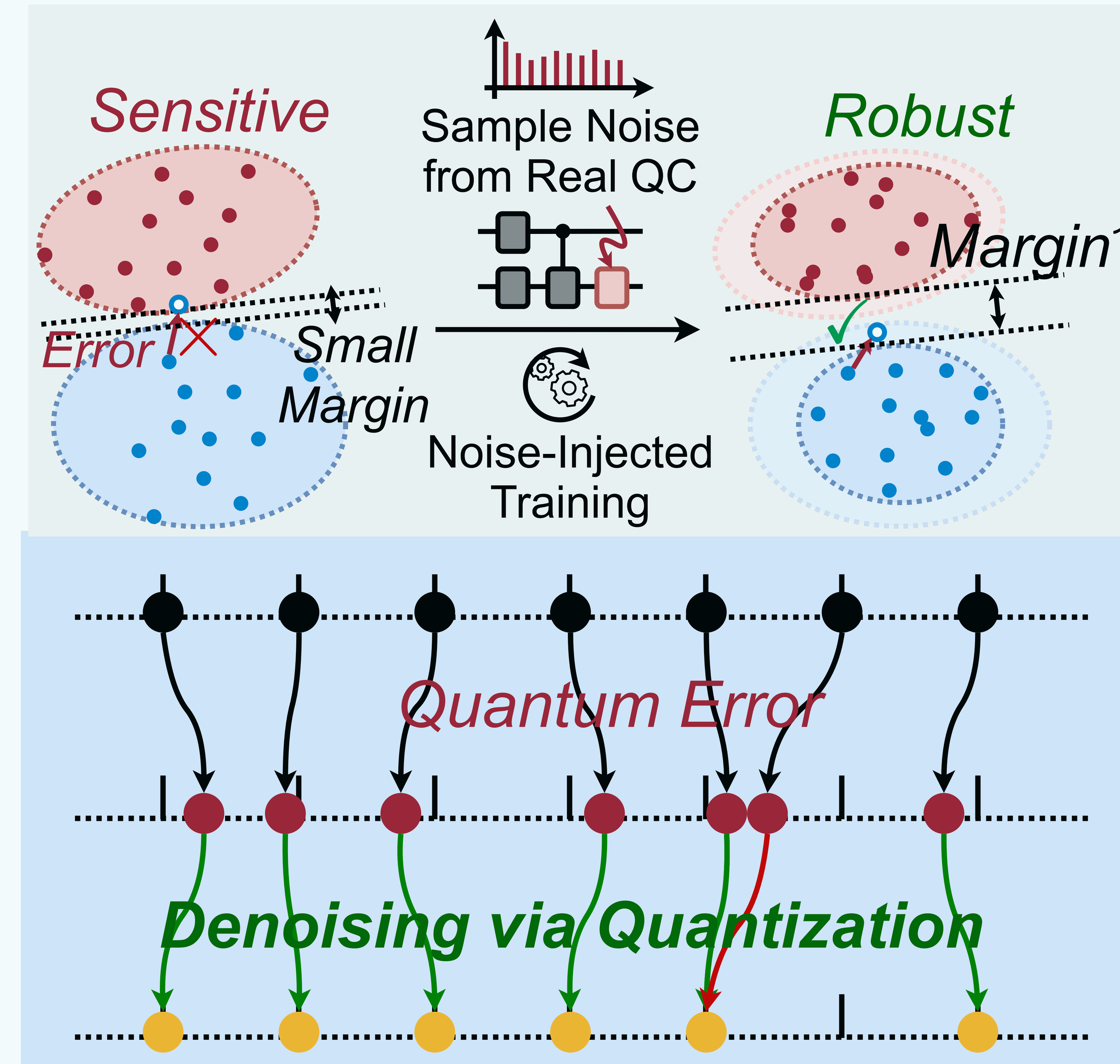
NAS for Robust Quantum Circuit Architecture

- Leverage a SuperCircuit to search for robust circuit with high efficiency
- 95% 2-class, 85% 4-class, and 32% 10-class acc on real quantum machine
- Achieve more accurate VQE eigenvalue than UCCSD baseline



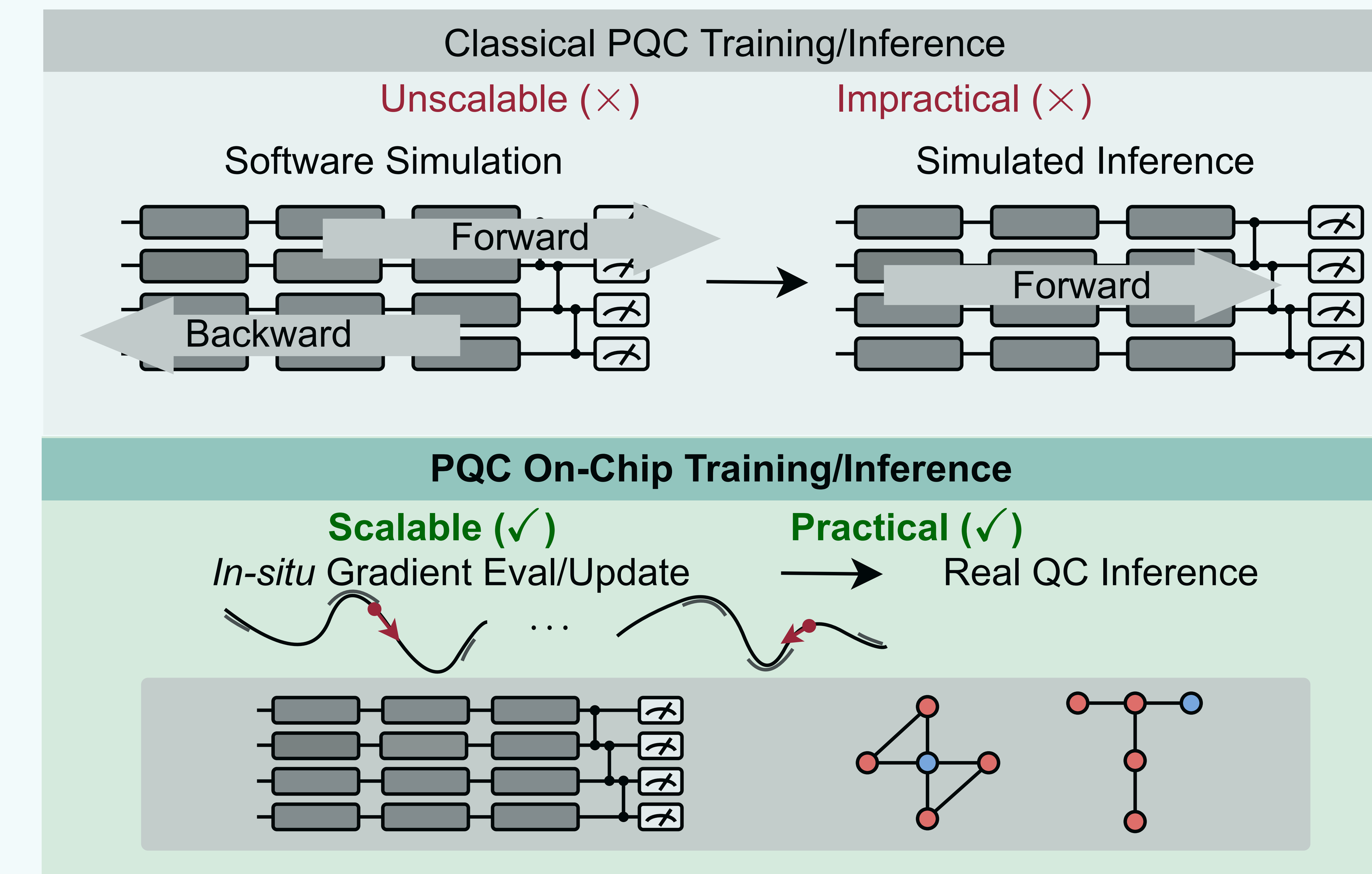
Quantization and Noise-Injection for Robustness

- Insert noise during the training of parameters to improve robustness
- Perform quantization of measurement outcomes for denoising
- Improves accuracy by up to 43%



Quantum On-Chip Training for Better Scalability

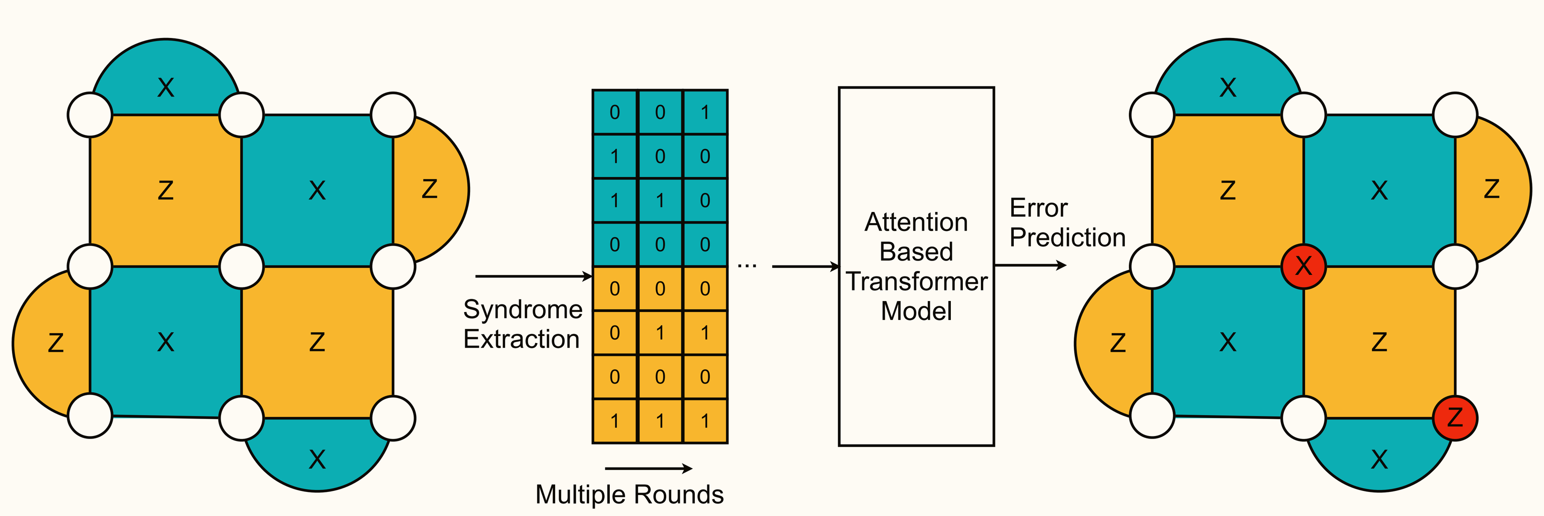
- First experimental demonstration of parameter shift rule on real quantum machines (IBMQ)
- Propose gradient pruning to further remove unreliable gradients and speedup training process
- Over 90% and 60% accuracy for 2-class and 4-class image classification



Long-Term: Quantum Error Correction

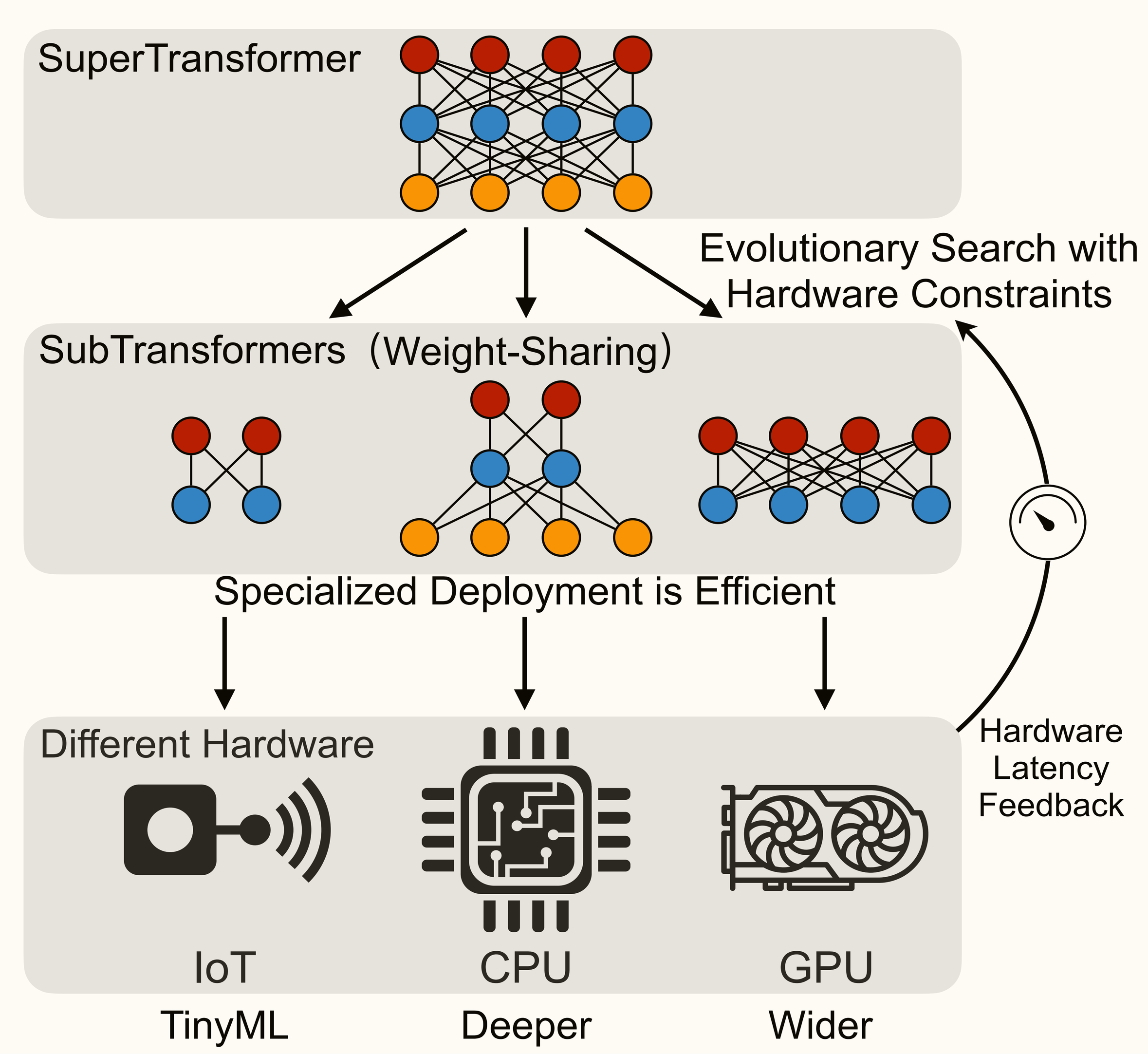
Transformer for Quantum Error Correction Code Decoder

- In the long term, we need quantum error correction code to further surpass quantum error
- QEC reduces logical error rates by introducing redundancy – encoding the quantum information to multiple qubits
- QEC requires a powerful decoder to process the syndromes obtained from syndrome qubit and predict the errors on the data qubit
- We propose a Transformer based decoder to process the Surface Code error syndromes to achieve high accuracy decoding than the traditional non-ML based decoders such as Union-Find



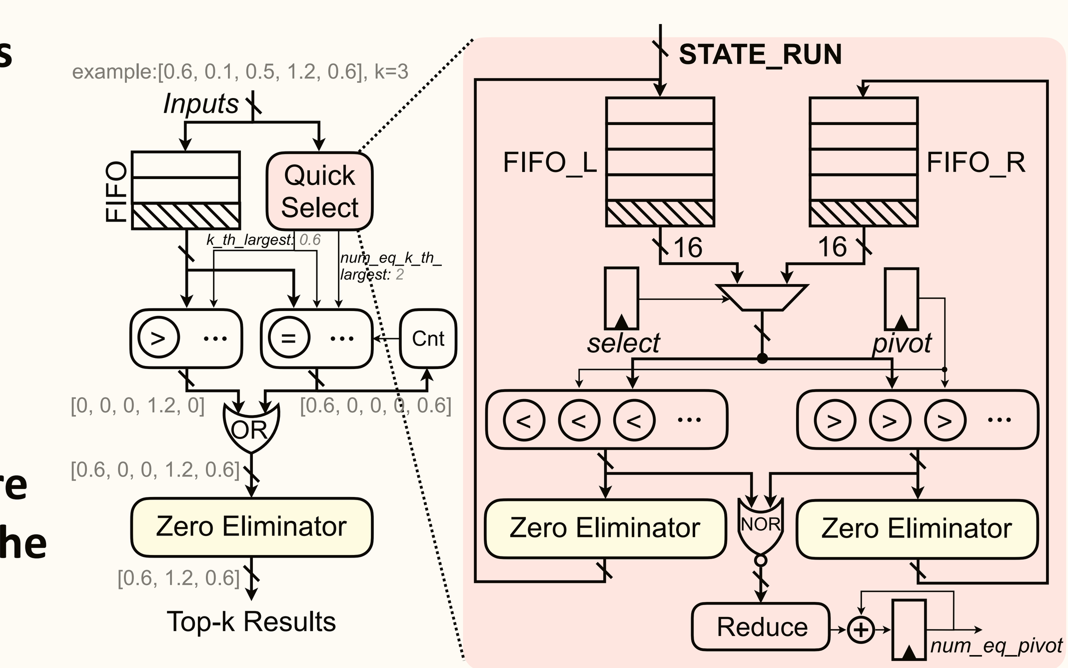
Hardware-Aware Transformer for QEC

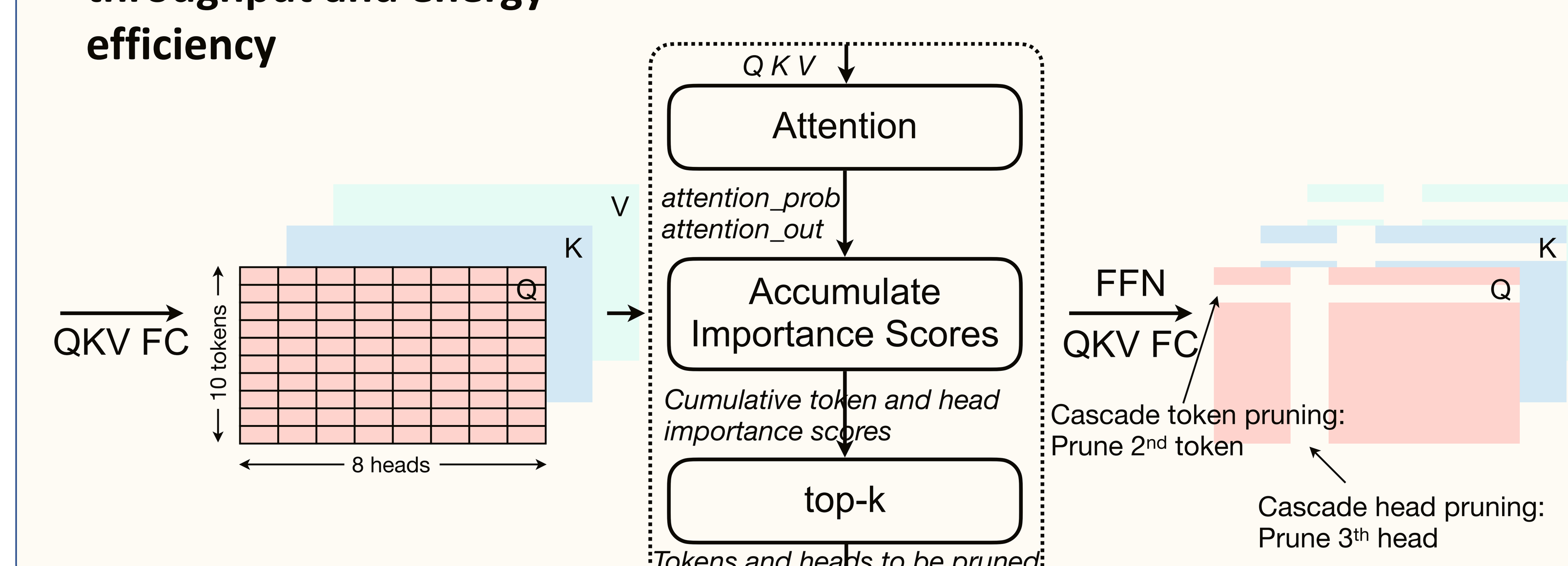
- The Transformer based decoder needs to be very efficiency to process the error syndromes in real-time
- We propose hardware aware transformer to find the most efficient model according to the quantum hardware decoherence time requirements



SpAtten: Syndrome Token Pruning Transformer Hardware Accelerator

- Not all syndrome tokens are created equal
- We propose token pruning to remove unimportant tokens to accelerate the Transformer processing
- We also design hardware accelerator to support the Transformer for higher throughput and energy efficiency





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