GCN-RL Circuit Designer: Transferable Automatic Transistor Sizing with Graph Neural Networks and Reinforcement Learning

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HAN LAB
Hardware, AI and Neural-nets

GCN-RL Circuit Designer: Transferable Automatic Transistor Sizing with Graph Neural Networks and Reinforcement Learning

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Motivation: Analog IC is Labor Intensive for Design

Digital IC

Standard Cell Libraries
Synthesis: Design Compiler, Genius…
Place & Route: IC Compiler…

Highly Automatic

Analog IC

Manual schematic design
Manual transistor sizing
Manual layout design

Less Automatic
Labor Intensive

GCN-RL Circuit Designer: ML for Hardware
Better Performance with Less Human Labor

Motivation:
Transistor sizing is challenging

- Large design space
- Complex trade-offs

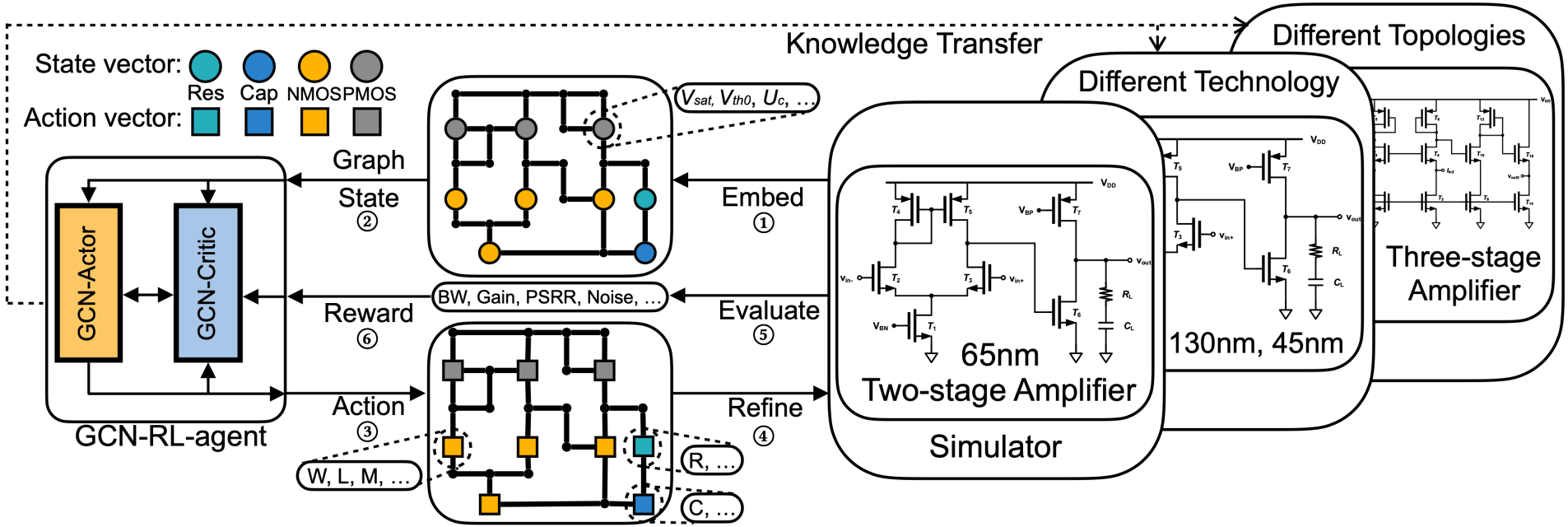
Transfer learning to reduce design porting overhead

- Between technology nodes
- Between different circuit schematics

Leverage Graph Neural Networks

- *Circuit is a graph*
- Involve graph information into optimization loop

Method: GCN-RL Circuit Designer Overview

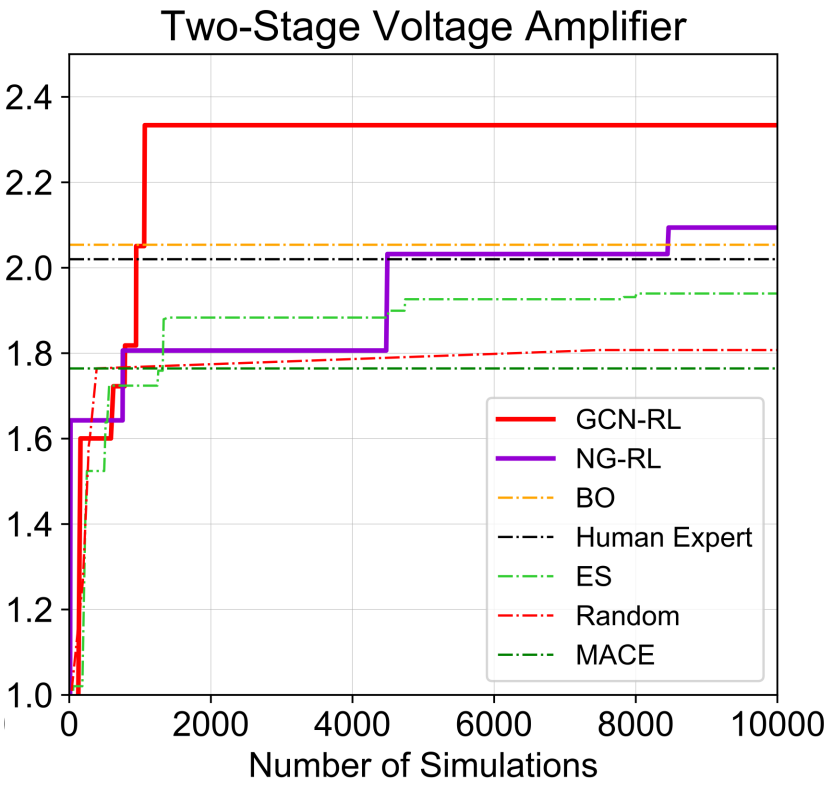


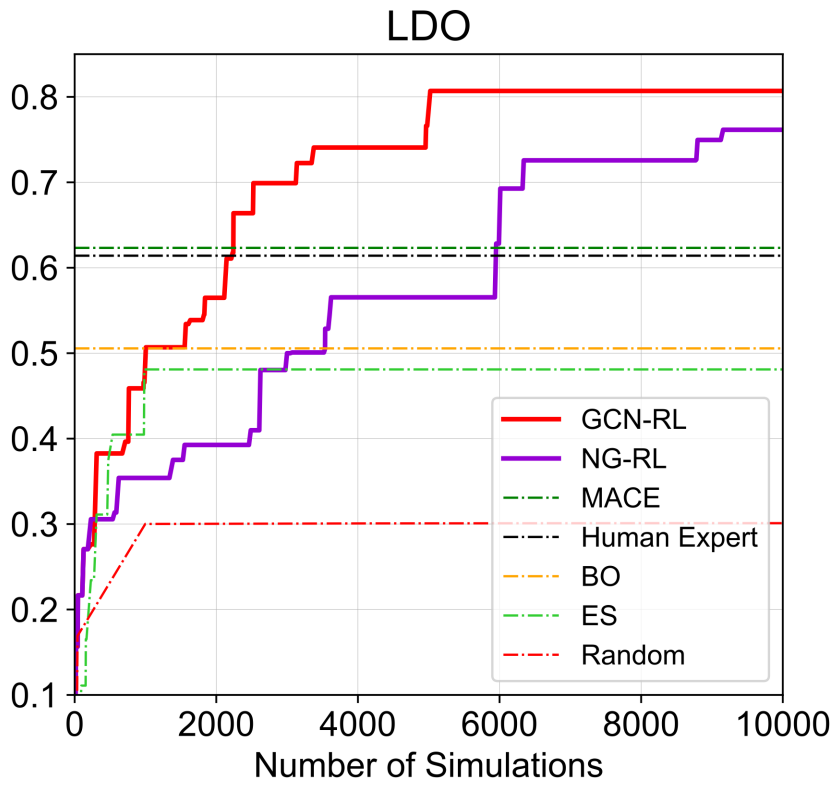
GCN-RL Achieves highest FoM

	2.32	2.02	1.15	0.61
	2.46±0.02	1.74±0.06	0.74±0.03	0.27±0.03
	2.66±0.03	1.91±0.02	1.30±0.03	0.40±0.07
	2.48±0.03	1.85±0.19	1.24±0.14	0.45±0.05
	2.54±0.01	1.70±0.08	1.27±0.04	0.58±0.04
	2.59±0.06	1.98±0.12	1.39±0.01	0.71±0.05
	2.69±0.03	**2.23±0.11**	**1.40±0.01**	**0.79±0.02**

GCN-RL consistently achieved Highest FoMs with small variance

GCN-RL Achieves highest FoM





GCN-RL has highest FoM and fast converging speed

Graph info improves FoM (GCN-RL v.s. NG-RL)

GCN-RL with Transfer Learning is Better Than no Transfer