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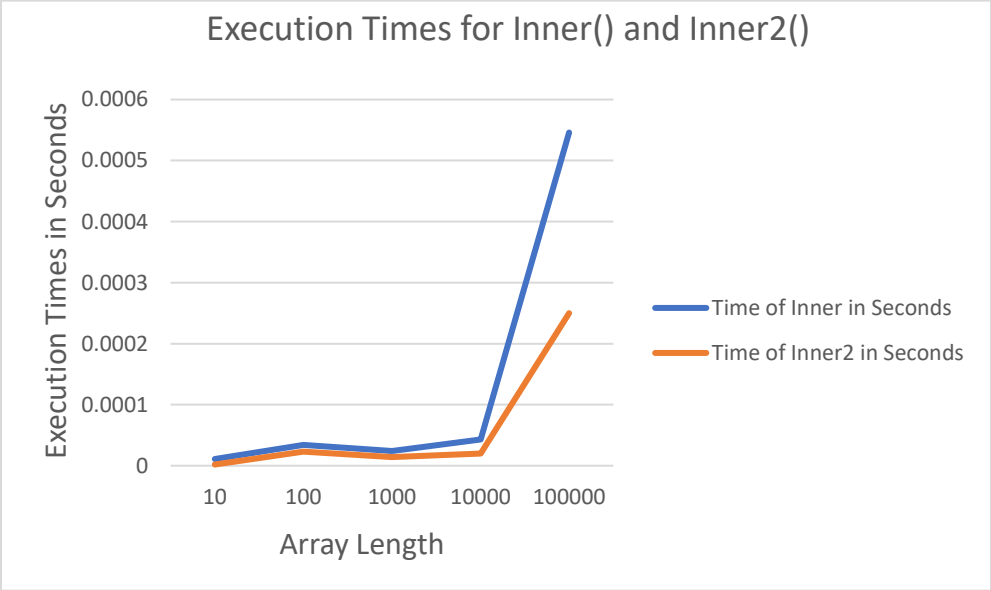
# Assignment 6 Solutions Document

2. a) The instructions “adds $xmm0, %xmm1” and “addq $1, %rdx” cannot be pipelined because the instruction “cmpq %rcx, %rdx” needs to compare the results that were computed from the adds and addq instructions from the two previous steps.

b) Float addition has a latency of 3 cycles, while all integer operations have a latency of 1 cycle. Float addition is represented by the instruction “adds %xmm0, %xmm1”, while integer addition is represented by the instruction “addq $1, %rdx”. This means that the instruction “adds %xmm0, %xmm1” has a latency of 3 cycles, while the instruction “addq $1, %rdx” has a latency of 1 cycle. Therefore, the best-case CPE for the loop as currently written will be a latency of 3 cycles, since the instruction “adds %xmm0, %xmm1” is slower than the instruction “addq $1, %rdx”.

d)




Based on this graph, it can be seen that it takes less time for Inner2 to execute than the first Inner function, meaning that the Inner2 function executes faster than the first inner function. According to the graph, as the array length increases, the time it takes to execute each function based on that certain array length increases.