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Linear Power Supply
Lab Report Submission

by:

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EN2111 Electronic Circuit Design

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Contents

1 Introduction

This experiment focuses on implementing a transistorized voltage regulator with a current-limiting circuit using two diodes. The design aims to maintain a reliable output voltage while protecting circuit components from excessive current flow. For our group a and b value were 4 and 0. So the regulator was designed to operate with an input voltage range of 17 V ± 1.5 V and maintain an output voltage within 6 V ± 2.5 V. A current-limiting mechanism was incorporated to restrict the maximum current to 50 mA, preventing potential damage to the circuit. The experiment involved analyzing the regulator's performance under various load conditions, including short circuits and different resistive loads, to evaluate its voltage stability and current-limiting effectiveness.

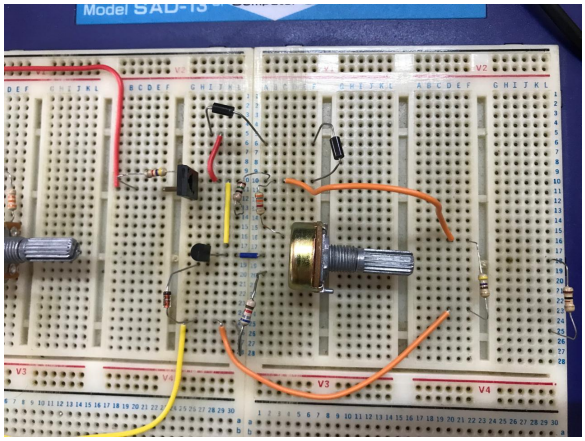

Figure 1: Our Circuit

2 Component Selection

2.1 Choosing the transistor T1

T1 was chosen considering the maximum power dissipation of the circuit. And the maximum power is occurring when input voltage is maximum and output voltage is minimum.

$$\text{Maximum power dissipation} = (V_{i,\max} - V_{o,\min}) \times I_c = (18.5 - 3.5) \times 50 \times 10^{-3}\,\text{W} = 0.75\,\text{W}$$

With this power rating BD139 NPN transistor was chosen as it can handle upto 1.25 W.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		NPN		PNP		
		BD135	BD139	BD136	BD140	
V_{CBO}	Collector-base voltage (I_E = 0)	45	80	-45	-80	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	45	80	-45	-80	V
V_{EBO}	Emitter-base voltage (I_C = 0)	5		-5		V
I_C	Collector current	1.5		-1.5		A
I_{CM}	Collector peak current	3		-3		A
I_B	Base current	0.5		-0.5		A
P_{TOT}	Total dissipation at $T_c \leq 25$ °C	12.5				W
P_{TOT}	Total dissipation at $T_{amb} \leq 25$ °C	1.25				W
T_{stg}	Storage temperature	-65 to 150				°C
T_j	Max. operating junction temperature	150				°C

Figure 2: Transistor Datasheet-Power Dissipation

h_{FE} (1)	DC current gain	NPN	I_C = 5 mA, V_{CE} = 2 V I_C = 150 mA, V_{CE} = 2 V I_C = 0.5 A, V_{CE} = 2 V	25 40 25		250	
		PNP	I_C = -5 mA, V_{CE} = -2 V I_C = -150 mA, V_{CE} = -2 V I_C = -0.5 A, V_{CE} = -2 V	25 40 25		250	

Figure 3: Transistor Datasheet- β

2.2 Choosing R1, R2, R3 and Zener Diode

Following are the equations used to find the above values.

$$(V_z + 0.7) = \frac{R_2 + R_3}{R_1 + R_2 + R_3} V_{0,\min}$$

$$(V_z + 0.7) = \frac{R_3}{R_1 + R_2 + R_3} V_{0,\max}$$

Zener Diode and R_2 were chosen arbitrarily.

R_1, R_3 were chosen according to those values and the above equations.

$$V_z = 2.2V$$

$$R_2 = 10k\,\Omega \text{ potentiometer}$$

$$2.2 + 0.7 = \frac{10k + R_3}{R_1 + 10k + R_3} \times 3.5$$

$$2.2 + 0.7 = \frac{R_3}{R_1 + 10k + R_3} \times 8.5$$

By solving the above equations:

$$R_1 = 3.477\,\text{k}\Omega$$

$$R_3 = 7\,\text{k}\Omega$$

With the practical values in the market, we chose $R_1 = 3.3k\Omega$, $R_3 = 6.8k\Omega$.

2.3 Choosing R

$$I_{R,\min} = I_{\text{knee}} + \frac{I_c}{\beta}$$

$$I_{R,\min} = \frac{V_{i,\min} - V_{o,\max} - 0.7}{R} = \frac{15.5 - 8.5 - 0.7}{R}$$

$$I_{R,\min} = \frac{50\,\text{mA}}{250} + 1\,m\text{A}$$

Using the above equations: $R = 5.25\,\text{k}\Omega$

With the practical values in the market, we chose $R = 5.1\,\text{k}\Omega$ and $R = 1\,\text{k}\Omega$.

2.4 Choosing components for current Limiting Circuit

Two 0.7 V Si diodes (1N4007) were used to implement the current limiting circuit.
Calculations for the resistor value for the current limiting circuit:

$$R = \frac{V}{I} = \frac{0.7}{0.05} = 14\Omega$$

With the resistors available in the market, we chose a $15\,\text{k}\Omega$ resistor to implement this circuit.

3 Results

3.1 Load Regulation Vs Output Voltage

$$\% \text{ Load Regulation} = \frac{V_{\text{no load}} - V_{\text{load}}}{V_{\text{load}}} \times 100$$

The following table shows the experimentally measured output voltages for different load resistances, with the input voltage fixed at 17 V:

Load	$220\,\Omega$	$330\,\Omega$	$470\,\Omega$	$2.2k\,\Omega$	$3.3k\,\Omega$
$4.0V$	$3.92V$	$3.96V$	$3.96V$	$4.01V$	$3.99V$
$4.5V$	$4.35V$	$4.43V$	$4.45V$	$4.49V$	$4.49V$
$5.0V$	$4.81V$	$4.90V$	$4.93V$	$4.98V$	$4.99V$
$5.5V$	$5.24V$	$5.36V$	$5.40V$	$5.48V$	$5.49V$
$6.0V$	$5.69V$	$5.82V$	$5.87V$	$5.98V$	$5.98V$
$6.5V$	$6.11V$	$6.28V$	$6.32V$	$6.46V$	$6.48V$
$7.0V$	$6.50V$	$6.73V$	$6.80V$	$6.94V$	$6.96V$
$7.5V$	$6.89V$	$7.18V$	$7.29V$	$7.44V$	$7.48V$
$8.0V$	$7.31V$	$7.64V$	$7.75V$	$7.93V$	$7.95V$

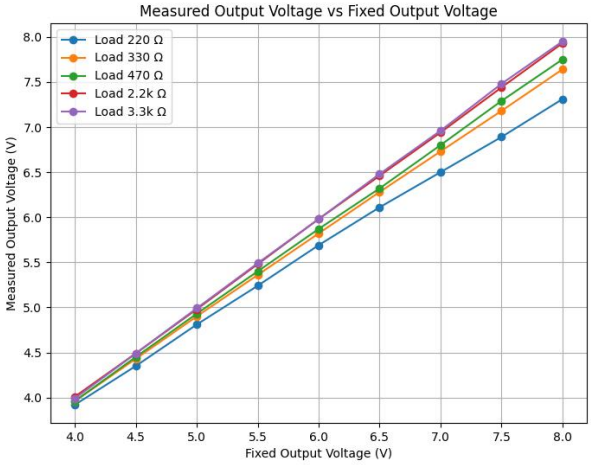

Figure 4: Fixed Output Voltage vs. Measured Output Voltage for Different Resistors

The following table shows the calculated load regulation for each cell.

Load	$220\,\Omega$	$330\,\Omega$	$470\,\Omega$	$2.2k\,\Omega$	$3.3k\,\Omega$
4.0	2.04	1.01	1.01	-0.25	0.25
4.5	3.45	1.58	1.12	0.22	0.22
5.0	3.95	2.04	1.42	0.40	0.20
5.5	4.96	2.61	1.85	0.36	0.18
6.0	5.45	3.09	2.21	0.33	0.33
6.5	6.38	3.50	2.85	0.62	0.31
7.0	7.69	4.01	2.94	0.86	0.57
7.5	8.85	4.46	2.88	0.81	0.27
8.0	9.44	4.71	3.23	0.88	0.63

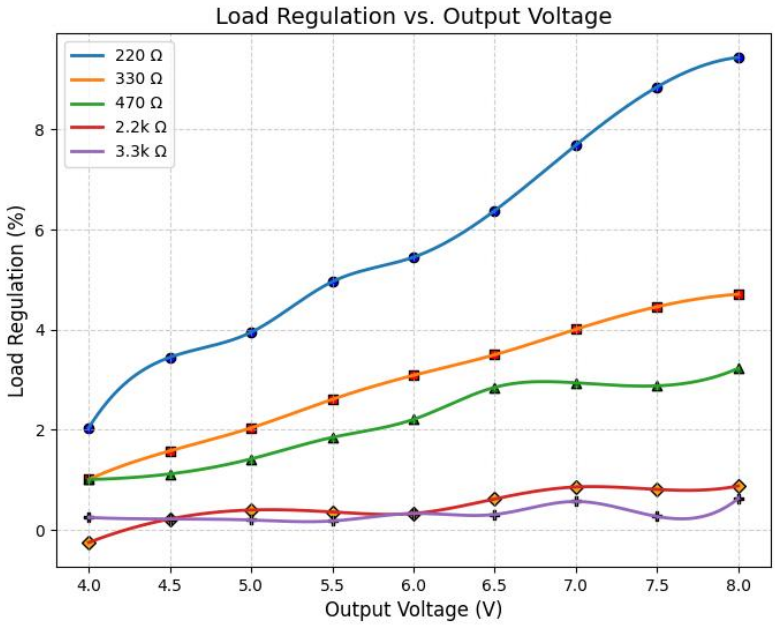

Figure 5: Load Regulation vs. Output Voltage for Different Resistors

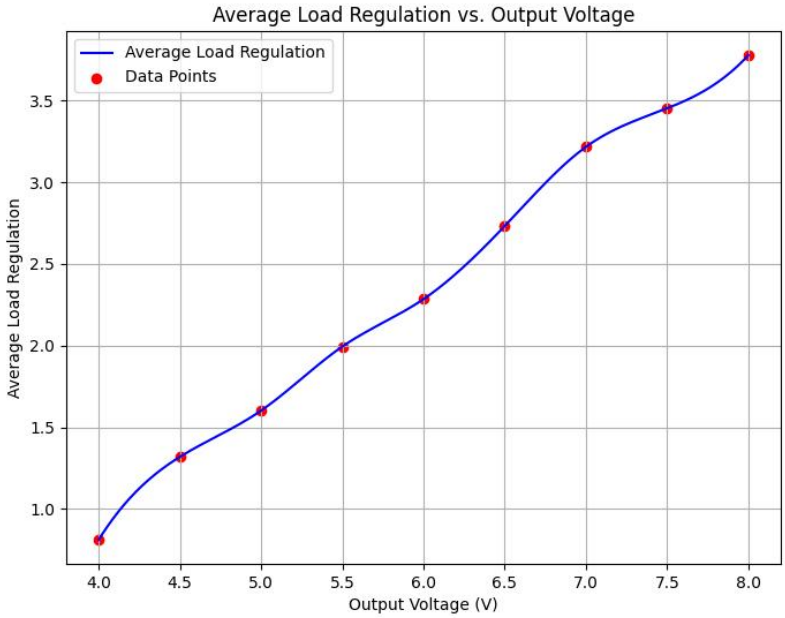

Figure 6: Average Load Regulation vs. Output Voltage

3.2 Line Regulation Vs Output Voltage

$$\%\text{Line Regulation} = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \times 100$$

The following table shows the experimentally measured output voltages for different input voltages.

Input Voltage (V)	$4.0V$	$4.5V$	$5.0V$	$5.5V$	$6.0V$	$6.5V$	$7.0V$	$7.5V$	$8.0V$
$15.5V$	$3.87V$	$4.33V$	$4.81V$	$5.28V$	$5.76V$	$6.25V$	$6.76V$	$7.27V$	$7.78V$
$16.0V$	$3.92V$	$4.39V$	$4.87V$	$5.35V$	$5.84V$	$6.34V$	$6.85V$	$7.35V$	$7.86V$
$16.5V$	$3.96V$	$4.44V$	$4.94V$	$5.43V$	$5.92V$	$6.42V$	$6.93V$	$7.43V$	$7.93V$
$17.0V$	$4.01V$	$4.50V$	$5.00V$	$5.50V$	$6.00V$	$6.50V$	$7.01V$	$7.50V$	$8.00V$
$17.5V$	$4.05V$	$4.55V$	$5.06V$	$5.57V$	$6.07V$	$6.58V$	$7.08V$	$7.57V$	$8.06V$
$18.0V$	$4.09V$	$4.60V$	$5.13V$	$5.64V$	$6.14V$	$6.65V$	$7.15V$	$7.64V$	$8.11V$
$18.5V$	$4.13V$	$4.65V$	$5.19V$	$5.70V$	$6.21V$	$6.73V$	$7.22V$	$7.70V$	$8.17V$

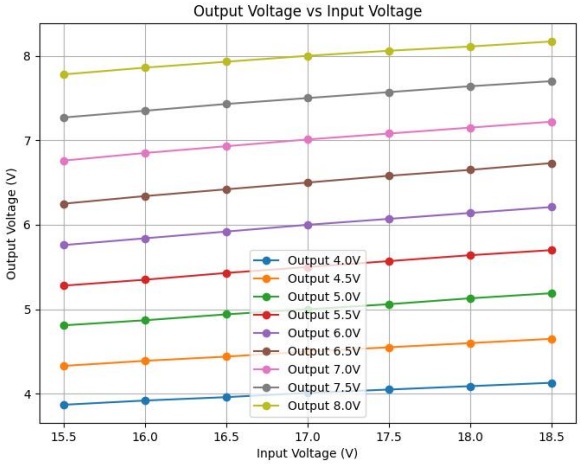

Figure 7: Input Voltage vs. Output Voltage

The following table shows the calculated line regulation for each data cell.

Input Voltage (V)	**Output Voltage (V)**								
	4	4.5	5	5.5	6	6.5	7	7.5	8
15.5	8.67	11.33	12.67	14.67	16.00	16.67	16.00	15.33	14.67
16.0	8.00	11.00	13.00	15.00	16.00	16.00	15.00	15.00	14.00
16.5	8.00	12.00	12.00	14.00	16.00	16.00	14.00	14.00	14.00
17.5	10.00	10.00	12.00	14.00	14.00	16.00	16.00	14.00	12.00
18.0	9.00	10.00	13.00	14.00	14.00	15.00	15.00	14.00	11.00
18.5	8.67	10.00	12.67	13.33	14.00	15.33	14.67	13.33	11.33

Table 1: Input Voltage vs. Output Voltage

Output Voltage (V)	4	4.5	5	5.5	6	6.5	7	7.5	8
Average Line Regulation	8.73	10.87	12.53	14.33	15.20	15.93	15.20	14.47	13.13

Table 2: Average Line Regulation for Different Output Voltages

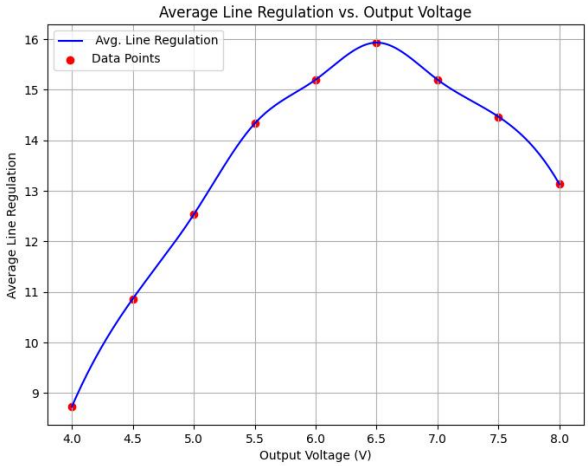

Figure 8: Average Line Regulation for Different Output Voltages

3.3 Output Voltage vs. Load Current

Fixed Output Voltage (V)	Parameter	1	2	3	4	5
6 V	Output Voltage (V)	5.69	5.82	5.87	5.98	5.98
	Load Current (mA)	24.3	17.82	12.42	2.66	1.79
7 V	Output Voltage (V)	6.50	6.73	6.80	6.94	6.96
	Load Current (mA)	29.7	20.58	14.72	3.2	2.13

Table 3: Measured Output Voltage and Load Current

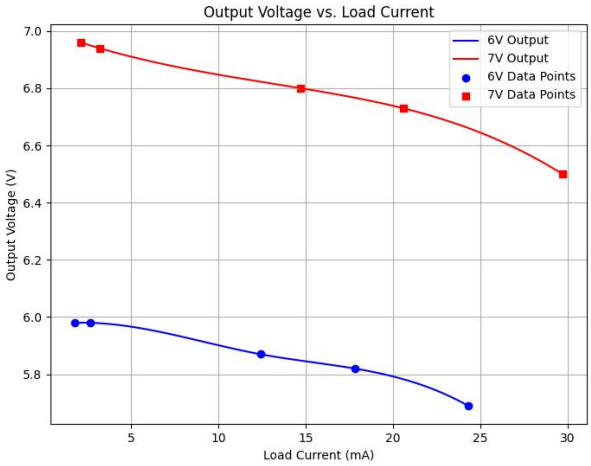

Figure 9: Output Voltage vs. Load Current