## DESCRIPTION

The HY57V561620T is a 268,435,456bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V561620 is organized as 4 banks of 4,194,304x16.

The HY57V561620T is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline ( CAS latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

## FEATURES

? Single 3.3V ±0.3V power supply

? All device pins are compatible with LVTTL interface

? JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch

? All inputs and outputs referenced to positive edge of system clock

? Data mask function by UDQM and LDQM

? Internal four banks operation

? Auto refresh and self refresh

? 8192 refresh cycles / 64ms

? Programmable Burst Length and Burst Type

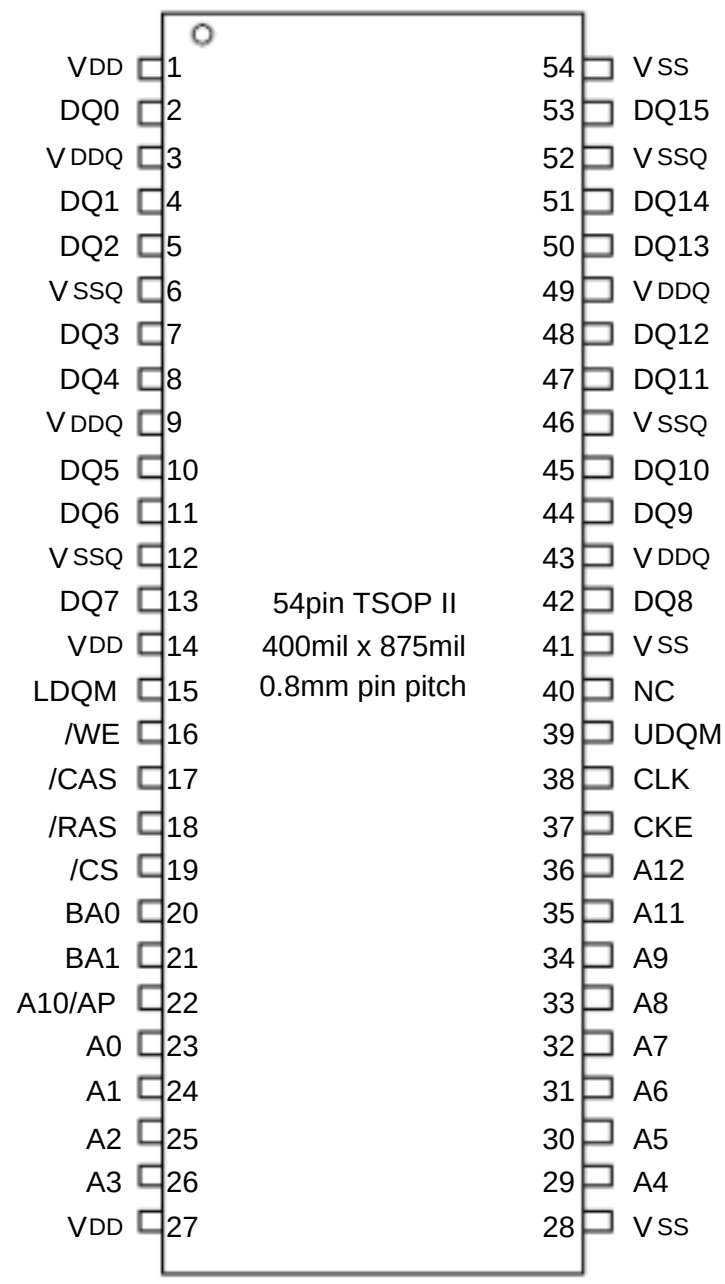
- 1, 2, 4, 8 and Full Page for Sequential Burst
- 1, 2, 4 and 8 for Interleave Burst

? Programmable CAS Latency ; 2, 3 Clocks

## ORDERING INFORMATION

| Part No. | Clock Frequency | Power | Organization | Interface | Package |
|---|---|---|---|---|---|
| HY57V561620T-HP | 133MHz | Normal | 4Banks x 4Mbits x16 | LVTTL | 400mil 54pin TSOP II |
| HY57V561620T-H | 133MHz | | | | |
| HY57V561620T-8 | 125MHz | | | | |
| HY57V561620T-P | 100MHz | | | | |
| HY57V561620T-S | 100MHz | | | | |
| HY57V561620LT-HP | 133MHz | Lower Power | | | |
| HY57V561620LT-H | 133MHz | | | | |
| HY57V561620LT-8 | 125MHz | | | | |
| HY57V561620LT-P | 100MHz | | | | |
| HY57V561620LT-S | 100MHz | | | | |

## PIN CONFIGURATION

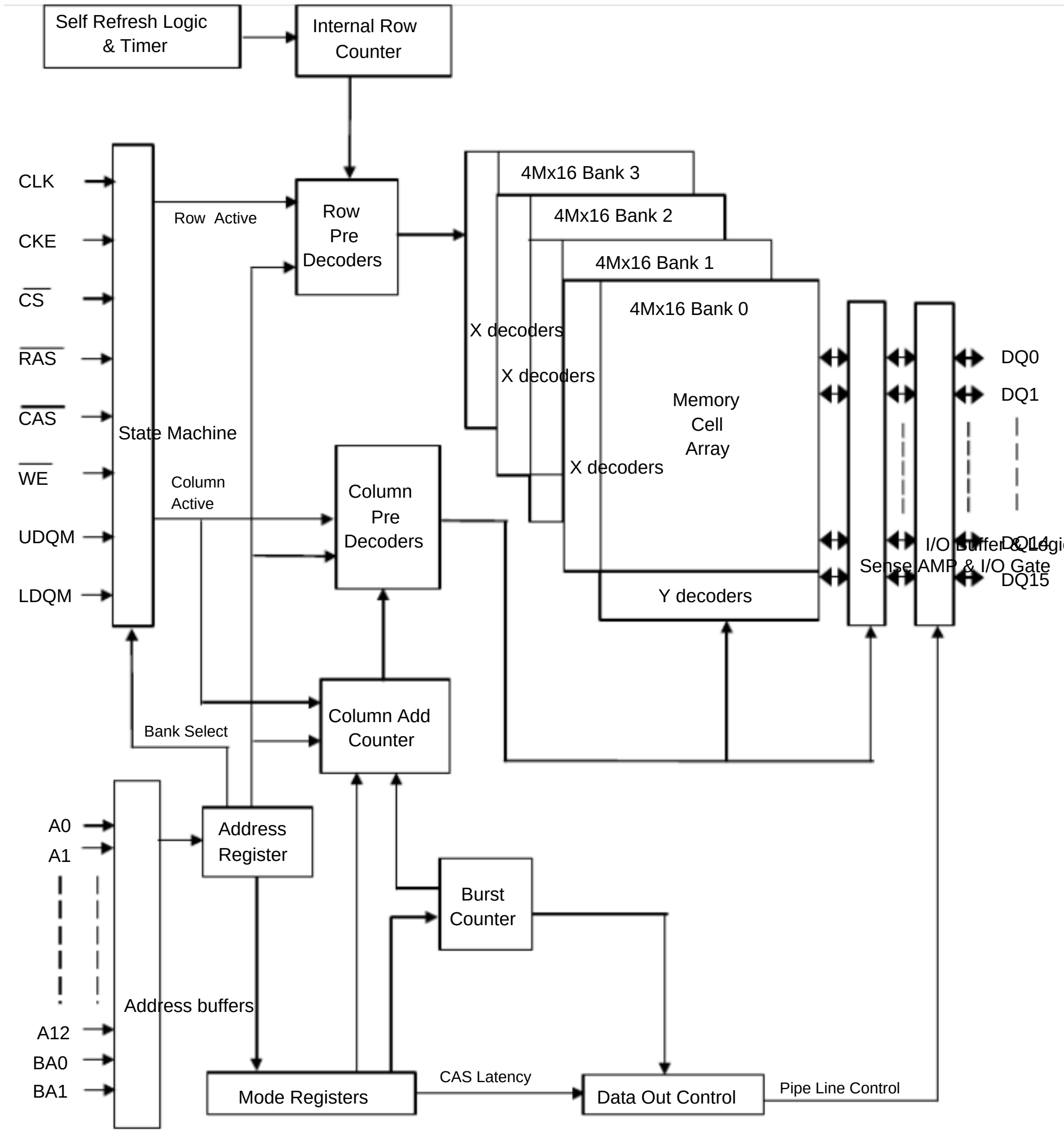



## PIN DESCRIPTION

| PIN | PIN NAME | DESCRIPTION |
|---|---|---|
| CLK | Clock | The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK |
| CKE | Clock Enable | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh |
| $\overline{CS}$ | Chip Select | Enables or disables all inputs except CLK, CKE, UDQM and LDQM |
| BA0, BA1 | Bank Address | Selects bank to be activated during $\overline{RAS}$ activity<br>Selects bank to be read/written during $\overline{CAS}$ activity |
| A0 ~ A12 | Address | Row Address : RA0 ~ RA12, Column Address : CA0 ~ CA8<br>Auto-precharge flag : A10 |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Row Address Strobe, Column Address Strobe, Write Enable | $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation<br>Refer function truth table for details |
| UDQM, LDQM | Data Input/Output Mask | Controls output buffers in read mode and masks input data in write mode |
| DQ0 ~ DQ15 | Data Input/Output | Multiplexed data input / output pin |
| VDD /VSS | Power Supply/Ground | Power supply for internal circuits and input buffers |
| VDDQ /VSSQ | Data Output Power/Ground | Power supply for output buffers |
| NC | No Connection | No connection |

## FUNCTIONAL BLOCK DIAGRAM

4Mbit x 4banks x16  I/O Synchronous DRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Ambient Temperature | TA | 0 ~ 70 | ℃ |
| Storage Temperature | TSTG | -55 ~ 125 | ℃ |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -1.0 ~ 4.6 | V |
| Voltage on VDD relative to VSS | VDD, VDDQ | -1.0 ~ 4.6 | V |
| Short Circuit Output Current | IOS | 50 | mA |
| Power Dissipation | PD | 1 | W |
| Soldering Temperature ?Time | TSOLDER | 260 ?10 | ℃ ?Sec |

Note : Operation at above absolute maximum rating can adversely affect device reliability

## DC OPERATING CONDITION (TA=0 to 70 ℃)

| Parameter | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VDD, VDDQ | 3.0 | 3.3 | 3.6 | V | 1 |
| Input High Voltage | VIH | 2.0 | 3.0 | VDDQ + 0.3 | V | 1,2 |
| Input Low Voltage | VIL | VSSQ-2.0 | 0 | 0.8 | V | 1,3 |

Note :
1. All voltages are referenced to VSS = 0V
2. VIH (max) is acceptable 5.6V AC pulse width with ≤3ns of duration
3. VIL (max) is acceptable -2.0V AC pulse width with ≤3ns of duration

## AC OPERATING CONDITION (TA=0 to 70 ℃, VDD=3.3 ±0.3V, VSS=0V)

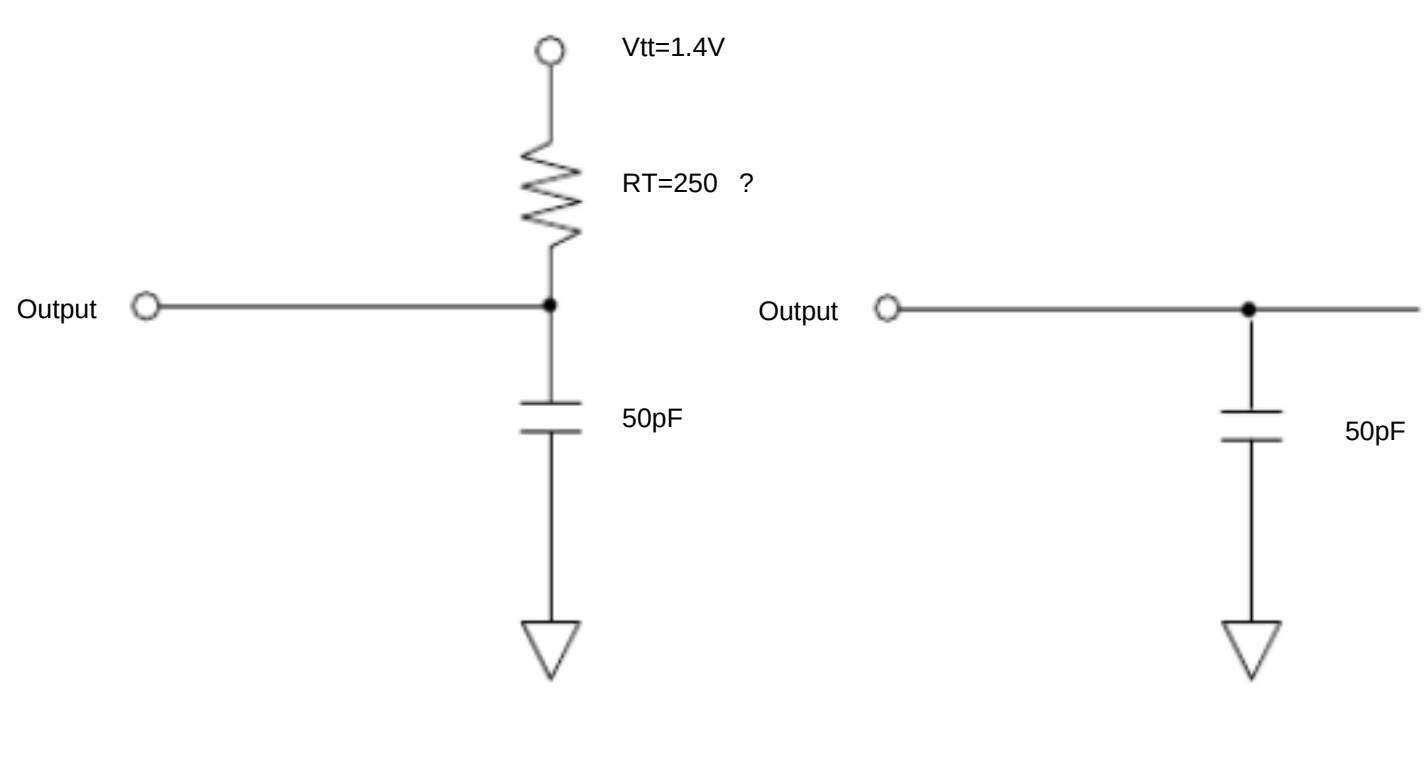
| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| AC Input High / Low Level Voltage | VIH / VIL | 2.4/0.4 | V | |
| Input Timing Measurement Reference Level Voltage | Vtrip | 1.4 | V | |
| Input Rise / Fall Time | tR / tF | 1 | ns | |
| Output Timing Measurement Reference Level | Voutref | 1.4 | V | |
| Output Load Capacitance for Access Time Measurement | CL | 50 | pF | 1 |

Note :
1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)
   For details, refer to AC/DC output circuit

## CAPACITANCE (TA=25 ℃, f=1MHz)

| Parameter | Pin | Symbol | -H | | -8/P/S | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input capacitance | CLK | $C_{I1}$ | 2.5 | 3.5 | 2.5 | 4.0 | pF |
| | A0 ~ A12, BA0, BA1, CKE, CS, RAS, CAS, WE, UDQM, LDQM | $C_{I2}$ | 2.5 | 3.8 | 2.5 | 5.0 | pF |
| Data input / output capacitance | DQ0 ~ DQ15 | $C_{I/O}$ | 4.0 | 6.5 | 4.0 | 6.5 | pF |

## OUTPUT LOAD CIRCUIT




DC Output Load Circuit

AC Output Load Circuit

## DC CHARACTERISTICS I (TA=0 to 70 ℃, $V_{DD}$=3.3 ±0.3V)

| Parameter | Symbol | Min. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | -1 | 1 | uA | 1 |
| Output leakage current | $I_{LO}$ | -1 | 1 | uA | 2 |
| Output high voltage | $V_{OH}$ | 2.4 | - | V | $I_{OH}$ = -4mA |
| Output low voltage | $V_{OL}$ | - | 0.4 | V | $I_{OL}$ =+4mA |

Note :

1. $V_{IN}$ = 0 to 3.6V, All other pins are not under test = 0V
2. $D_{OUT}$ is disabled, $V_{OUT}$ =0 to 3.6V

## DC CHARACTERISTICS II (TA=0 ℃ to 70 ℃, $V_{DD}$=3.3V ±0.3V, $V_{SS}$=0V)

| Parameter | Symbol | Test Condition | Speed | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | -HP | -H | -8 | -P | -S | | |
| Operating Current | IDD1 | Burst Length=1, One bank active<br>tRAS ≥tRAS(min),tRP ≥tRP(min), IO=0mA | 120 | 120 | 110 | 100 | 100 | mA | 1 |
| Precharge Standby Current in power down mode | IDD2P | CKE ≤VIL(max), tCK = min. | 2 | | | | | mA | |
| | IDD2PS | CKE ≤VIL(max), tCK = ∞ | 2 | | | | | | |
| Precharge Standby Current in non power down mode | IDD2N | CKE ≥VIH(min), $\overline{CS}$ ≥VIH(min), tCK = min<br>Input signals are changed one time during 2clks.<br>All other pins ≥VDD-0.2V or ≤0.2V | 20 | | | | | mA | |
| | IDD2NS | CKE ≥VIH(min), tCK = ∞<br>Input signals are stable. | 10 | | | | | | |
| Active Standby Current in power down mode | IDD3P | CKE ≤VIL(max), tCK = min | 3 | | | | | mA | |
| | IDD3PS | CKE ≤VIL(max), tCK = ∞ | 3 | | | | | | |
| Active Standby Current in non power down mode | IDD3N | CKE ≥VIH(min), $\overline{CS}$ ≥VIH(min), tCK = min<br>Input signals are changed one time during 2clks.<br>All other pins ≥VDD-0.2V or ≤0.2V | 25 | | | | | mA | |
| | IDD3NS | CKE ≥VIH(min), tCK = ∞<br>Input signals are stable | 15 | | | | | | |
| Burst Mode Operating Current | IDD4 | tCK ≥tCK(min),<br>tRAS ≥tRAS(min), IO=0mA<br>All banks active | 150 | 150 | 140 | 120 | 120 | mA | 1 |
| Auto Refresh Current | IDD5 | tRRC ≥tRRC(min), All banks active | 260 | 260 | 260 | 250 | 250 | mA | 2 |
| Self Refresh Current | IDD6 | CKE ≤0.2V | 3 | | | | | mA | 3 |
| | | | 1.5 | | | | | mA | 4 |

Note :

1. $I_{DD1}$ and $I_{DD4}$ depend on output loading and cycle rates. Specified values are measured with the output open.
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II
3. HY57V561620T-HP/H/8/P/S
4. HY57V561620LT-HP/H/8/P/S

## AC CHARACTERISTICS I

| Parameter | | Symbol | -HP | | -H | | -8 | | -P | | -S | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| System clock cycle time | $\overline{CAS}$ Latency = 3 | tCK3 | 7.5 | 1000 | 7.5 | 1000 | 8 | 1000 | 10 | 1000 | 10 | 1000 | ns | |
| | $\overline{CAS}$ Latency = 2 | tCK2 | 10 | | 10 | | 10 | | 10 | | 12 | | ns | |
| Clock high pulse width | | tCHW | 2.5 | - | 2.5 | - | 3 | - | 3 | - | 3 | - | ns | 1 |
| Clock low pulse width | | tCLW | 2.5 | - | 2.5 | - | 3 | - | 3 | - | 3 | - | ns | 1 |
| Access time from clock | $\overline{CAS}$ Latency = 3 | tAC3 | - | 5.4 | - | 5.4 | - | 6 | | 6 | | 6 | ns | 2 |
| | $\overline{CAS}$ Latency = 2 | tAC2 | - | 6 | - | 6 | - | 6 | | 6 | | 6 | ns | |
| Data-out hold time | | tOH | 2.7 | - | 2.7 | - | 3 | - | 3 | - | 3 | - | ns | |
| Data-Input setup time | | tDS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Data-Input hold time | | tDH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| Address setup time | | tAS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Address hold time | | tAH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| CKE setup time | | tCKS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| CKE hold time | | tCKH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| Command setup time | | tCS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | 2 | - | ns | 1 |
| Command hold time | | tCH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | 1 | - | ns | 1 |
| CLK to data output in low Z-time | | tOLZ | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | ns | |
| CLK to data output in high Z-time | $\overline{CAS}$ Latency = 3 | tOHZ3 | 2.7 | 5.4 | 2.7 | 5.4 | 3 | 6 | 3 | 6 | 3 | 6 | ns | |
| | $\overline{CAS}$ Latency = 2 | tOHZ2 | 3 | 6 | 3 | 6 | 3 | 6 | 3 | 6 | 3 | 6 | ns | |

Note :

1. Assume tR / tF (input rise and fall time ) is 1ns.
2. Access times to be measured with input signals of 1v/ns slew rate, 0.8v to 2.0v

## AC CHARACTERISTICS II

| Parameter | | Symbol | -HP | | -H | | -8 | | -P | | -S | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $\overline{RAS}$ cycle time | Operation | tRC | 65 | - | 65 | - | 68 | - | 70 | - | 70 | - | ns | |
| | Auto Refresh | tRRC | 65 | - | 65 | - | 68 | - | 70 | - | 70 | - | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay | | tRCD | 20 | - | 20 | - | 20 | - | 20 | - | 20 | - | ns | |
| $\overline{RAS}$ active time | | tRAS | 45 | 100K | 45 | 100K | 48 | 100K | 50 | 100K | 50 | 100K | ns | |
| $\overline{RAS}$ precharge time | | tRP | 20 | - | 20 | - | 20 | - | 20 | - | 20 | - | ns | |
| $\overline{RAS}$ to $\overline{RAS}$ bank active delay | | tRRD | 15 | - | 15 | - | 16 | - | 20 | - | 20 | - | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ delay | | tCCD | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | CLK | |
| Write command to data-in delay | | tWTL | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | CLK | |
| Data-in to precharge command | | tDPL | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| Data-in to active command | | tDAL | 5 | - | 5 | - | 5 | - | 4 | - | 4 | - | CLK | |
| DQM to data-out Hi-Z | | tDQZ | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| DQM to data-in mask | | tDQM | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | CLK | |
| MRS to new command | | tMRD | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| Precharge to data output Hi-Z | $\overline{CAS}$ Latency = 3 | tPROZ3 | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | CLK | |
| | $\overline{CAS}$ Latency = 2 | tPROZ2 | - | - | - | - | - | - | 2 | - | 2 | - | CLK | |
| Power down exit time | | tPDE | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | CLK | |
| Self refresh exit time | | tSRE | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | CLK | 1 |
| Refresh Time | | tREF | - | 64 | - | 64 | - | 64 | - | 64 | - | 64 | ms | |

Note :

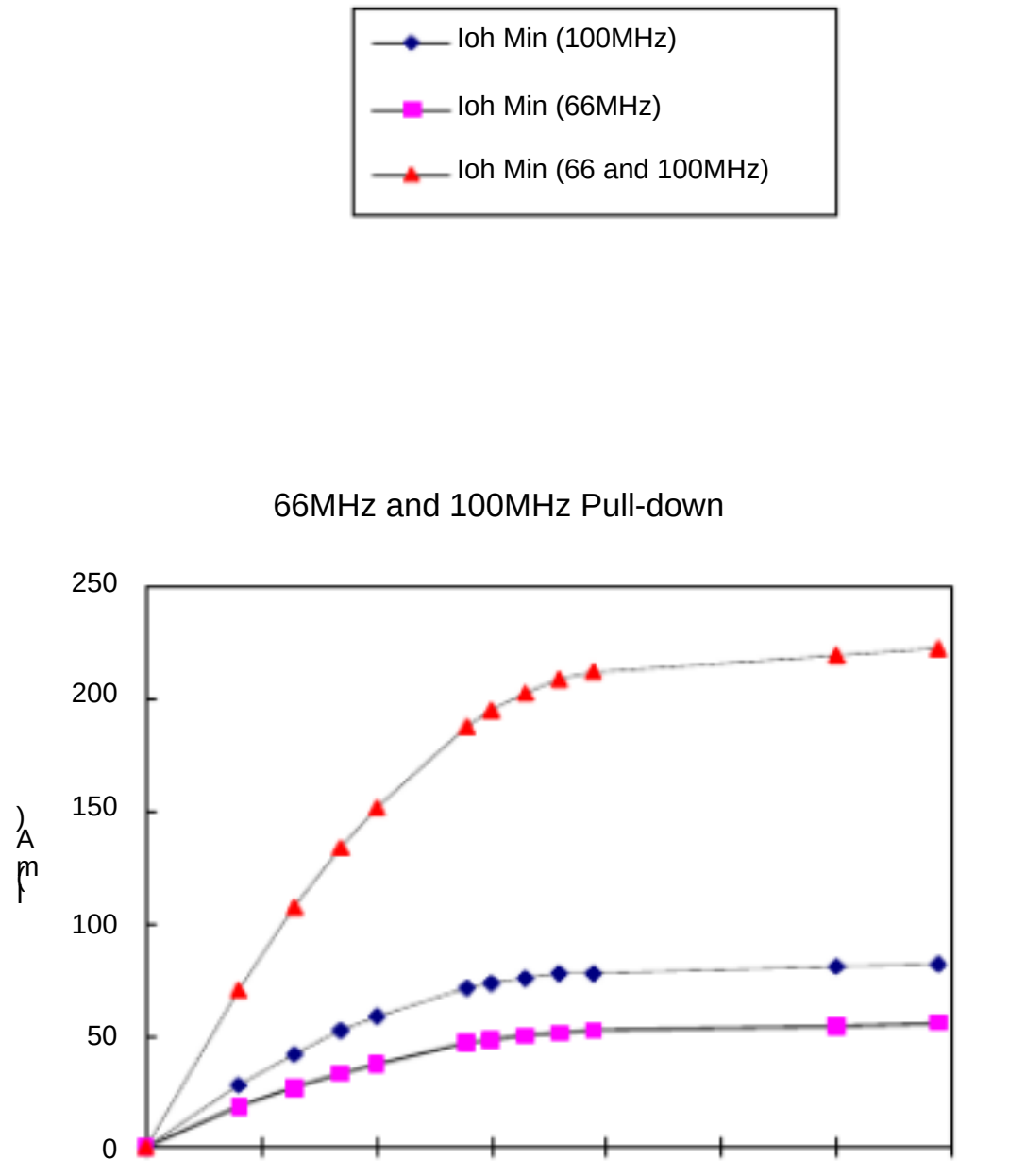
1. A new command can be given tRRC after self refresh exit.

# IBIS SPECIFICATION

## $I_{OH}$ Characteristics (Pull-up)

| Voltage | 100MHz Min | 100MHz Max | 66MHz Min |
|---|---|---|---|
| (V) | I (mA) | I (mA) | I (mA) |
| 3.45 | | -2.4 | |
| 3.3 | | -27.3 | |
| 3.0 | 0.0 | -74.1 | -0.7 |
| 2.6 | -21.1 | -129.2 | -7.5 |
| 2.4 | -34.1 | -153.3 | -13.3 |
| 2.0 | -58.7 | -197.0 | -27.5 |
| 1.8 | -67.3 | -226.2 | -35.5 |
| 1.65 | -73.0 | -248.0 | -41.1 |
| 1.5 | -77.9 | -269.7 | -47.9 |
| 1.4 | -80.8 | -284.3 | -52.4 |
| 1.0 | -88.6 | -344.5 | -72.5 |
| 0.0 | -93.0 | -502.4 | -93.0 |

66MHz and 100MHz Pull-up




## $I_{OL}$ Characteristics (Pull-down)

| Voltage | 100MHz Min | 100MHz Max | 66MHz Min |
|---|---|---|---|
| (V) | I (mA) | I (mA) | I (mA) |
| 0.0 | 0.0 | 0.0 | 0.0 |
| 0.4 | 27.5 | 70.2 | 17.7 |
| 0.65 | 41.8 | 107.5 | 26.9 |
| 0.85 | 51.6 | 133.8 | 33.3 |
| 1.0 | 58.0 | 151.2 | 37.6 |
| 1.4 | 70.7 | 187.7 | 46.6 |
| 1.5 | 72.9 | 194.4 | 48.0 |
| 1.65 | 75.4 | 202.5 | 49.5 |
| 1.8 | 77.0 | 208.6 | 50.7 |
| 1.95 | 77.6 | 212.0 | 51.5 |
| 3.0 | 80.3 | 219.6 | 54.2 |
| 3.45 | 81.4 | 222.6 | 54.9 |

66MHz and 100MHz Pull-down

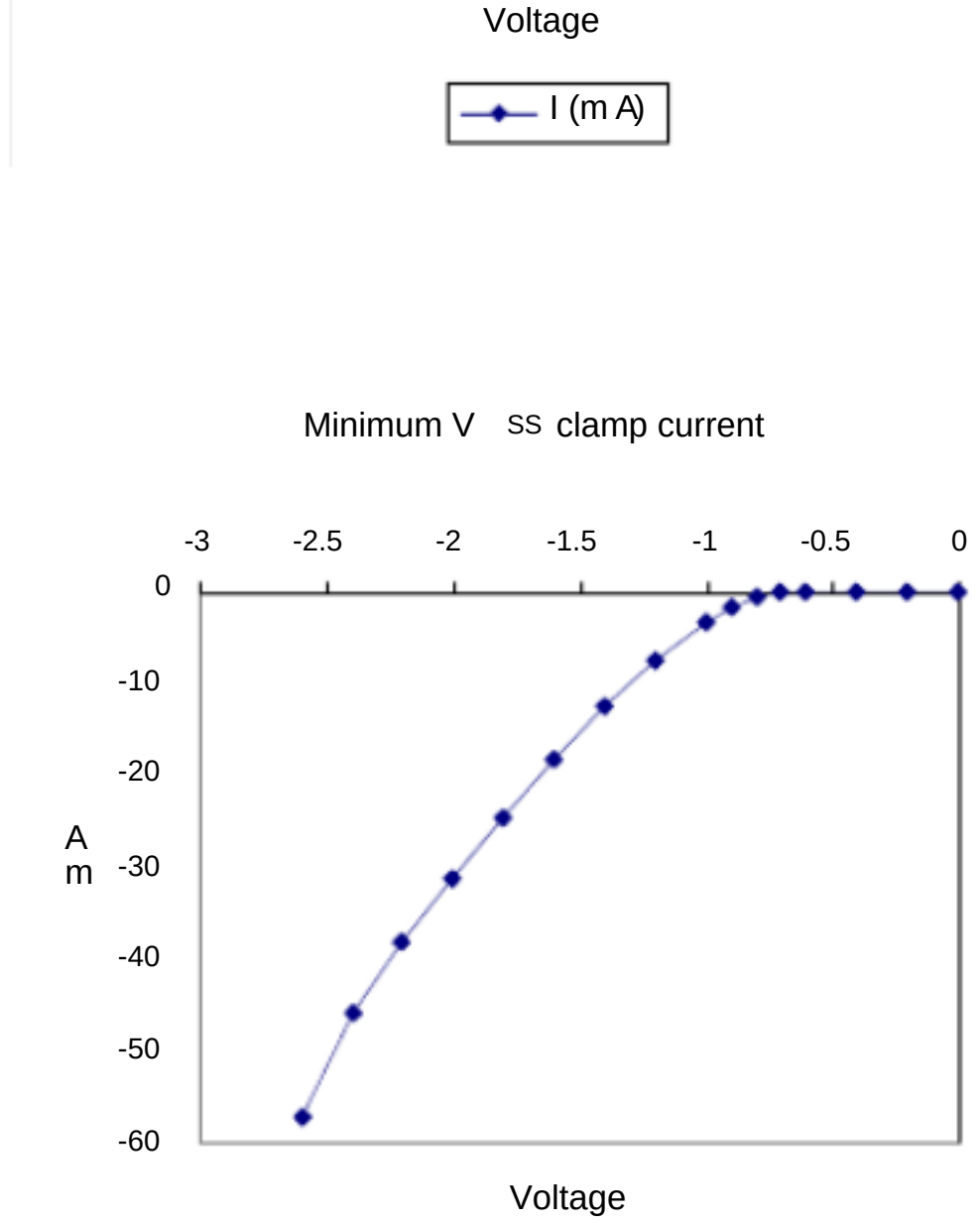



** IBIS spec. is also applied to 133MHz device.

V DD Clamp @ CLK, CKE, CS, DQM & DQ

| V DD (V) | I(mA) |
|---|---|
| 0.0 | 0.0 |
| 0.2 | 0.0 |
| 0.4 | 0.0 |
| 0.6 | 0.0 |
| 0.7 | 0.0 |
| 0.8 | 0.0 |
| 0.9 | 0.0 |
| 1.0 | 0.23 |
| 1.2 | 1.34 |
| 1.4 | 3.02 |
| 1.6 | 5.06 |
| 1.8 | 7.35 |
| 2.0 | 9.83 |
| 2.2 | 12.48 |
| 2.4 | 15.30 |
| 2.6 | 18.31 |

Minimum V DD clamp current
(Referenced to V DD)




V SS Clamp @ CLK, CKE, CS, DQM & DQ

| VSS (V) | I (mA) |
|---|---|
| -2.6 | -57.23 |
| -2.4 | -45.77 |
| -2.2 | -38.26 |
| -2.0 | -31.22 |
| -1.8 | -24.58 |
| -1.6 | -18.37 |
| -1.4 | -12.56 |
| -1.2 | -7.57 |
| -1.0 | -3.37 |
| -0.9 | -1.75 |
| -0.8 | -0.58 |
| -0.7 | -0.05 |
| -0.6 | 0.0 |
| -0.4 | 0.0 |
| -0.2 | 0.0 |
| 0.0 | 0.0 |

Minimum V SS clamp current

# DEVICE OPERATING OPTION TABLE

## HY57V561620(L)T-HP

| | CAS Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 133MHz(7.5ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 5.4ns | 2.7ns |
| 125MHz(8ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| 100MHz(10ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |

## HY57V561620(L)T-H

| | CAS Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 133MHz(7.5ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 5.4ns | 2.7ns |
| 125MHz(8ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| 100MHz(10ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |

## HY57V561620(L)T-8

| | CAS Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 125MHz(8ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| 100MHz(10ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| 83MHz(12ns) | 2CLKs | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 6ns | 3ns |

## HY57V561620(L)T-P

| | CAS Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 100MHz(10ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |
| 83MHz(12ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |
| 66MHz(15ns) | 2CLKs | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 6ns | 3ns |

## HY57V561620(L)T-S

| | CAS Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 100MHz(10.0ns) | 3CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |
| 83MHz(12.0ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |
| 66MHz(15.0ns) | 2CLKs | 2CLKs | 4CLKs | 6CLKs | 2CLKs | 6ns | 3ns |

## COMMAND TRUTH TABLE

| Command | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | | H | X | L | L | L | L | X | OP code | | | 1 |
| No Operation | | H | X | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| Bank Active | | H | X | L | L | H | H | X | RA | | V | |
| Read | | H | X | L | H | L | H | X | CA | L | V | |
| Read with Autoprecharge | | | | | | | | | | H | | |
| Write | | H | X | L | H | L | L | X | CA | L | V | |
| Write with Autoprecharge | | | | | | | | | | H | | |
| Precharge All Banks | | H | X | L | L | H | L | X | X | H | X | |
| Precharge selected Bank | | | | | | | | | | L | V | |
| Burst Stop | | H | X | L | H | H | L | X | X | | | |
| UDQM, LDQM | | H | X | | | | | V | X | | | |
| Auto Refresh | | H | H | L | L | L | H | X | X | | | |
| Self Refresh | Entry | H | L | L | L | L | H | X | X | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Precharge power down | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Clock Suspend | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| | Exit | L | H | X | | | | X | | | | |

Note :
1. OP Code : Operand Code
2. V = Valid, X = Don t care, H = Logic High, L= Logic Low, RA = Row Address, CA = Column Address.

PACKAGE INFORMATION

400mil 54pin Thin Small Outline Package