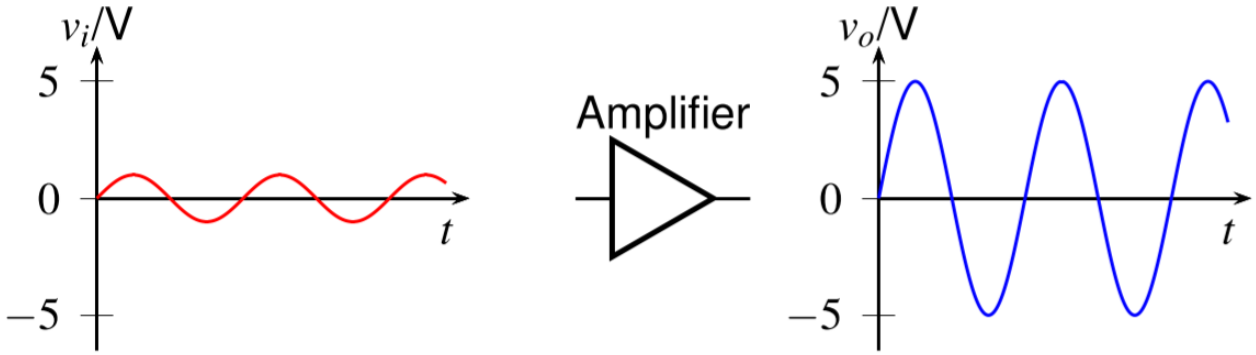
Chapter 1 Introduction

1-1 Signal Amplification

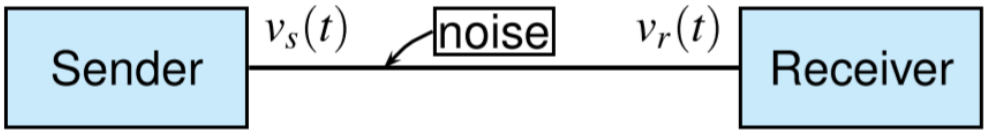


$$v_o(t) = C \cdot v_i(t)$$

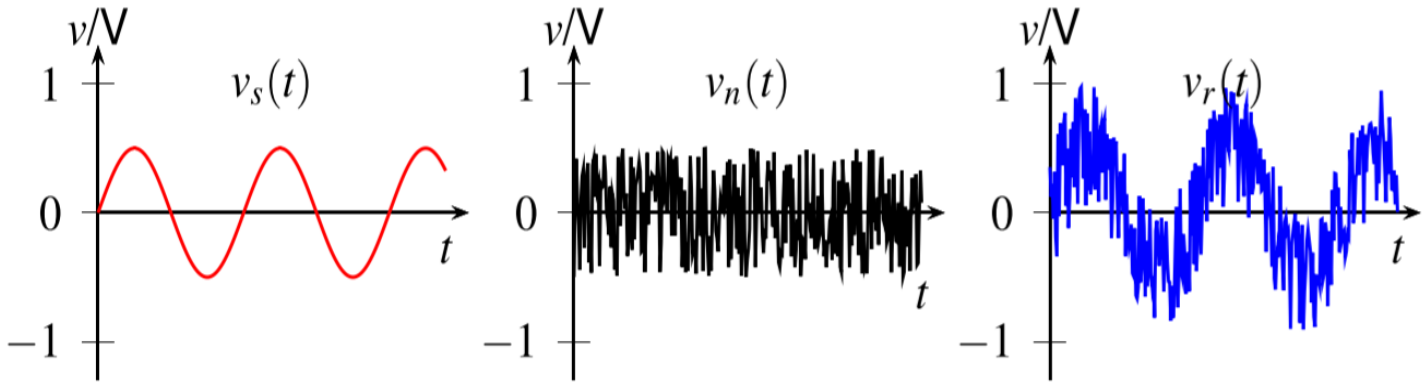
- $v_i(t)$: input signal
- $v_o(t)$: output signal
- A: **amplifier gain**

Case 1: Signal Transmission

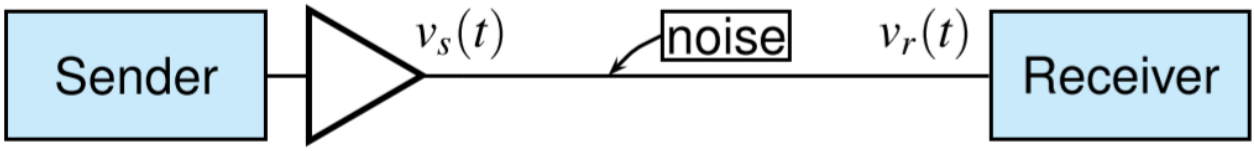
A small signal need to be transmitted from a sender to a receiver through a wired channel



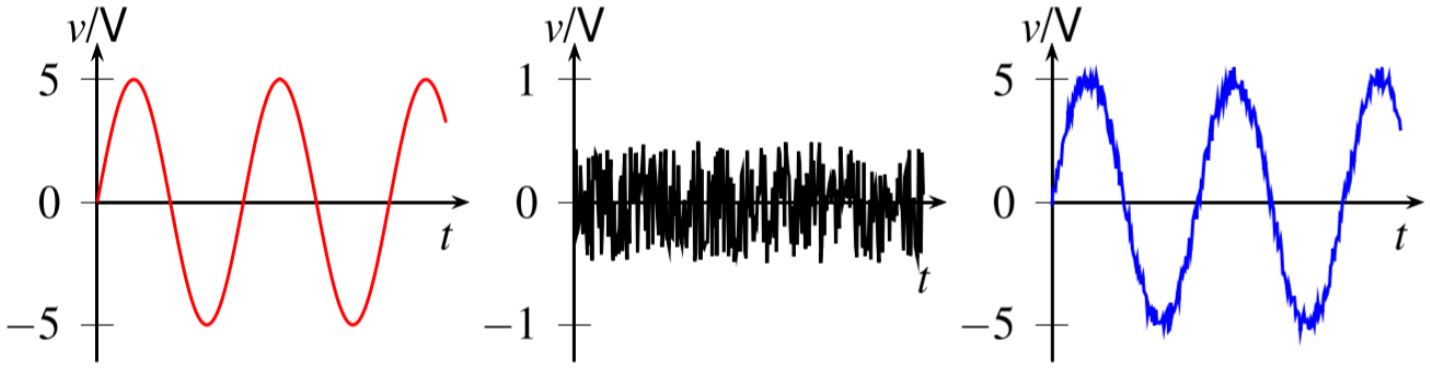
It could be hard to be finished because the transmitting channels are noisy. Let $v_n(t)$ denote the noise voltage, then $v_r(t) = v_s(t) + v_n(t)$



If the signal is amplified before transmission

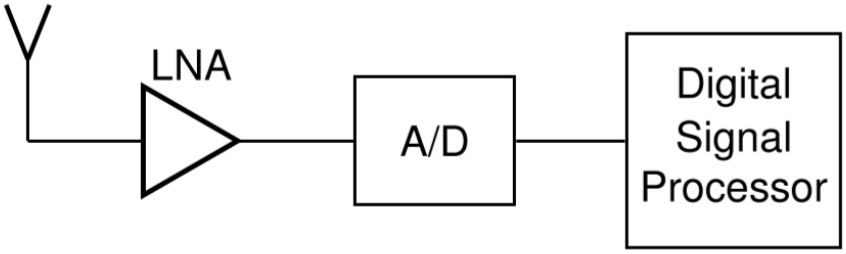


Then it could be easier to identify the receive voltage



Case 2: Digital Mobile Phone

The signal processing subsystem in a digital mobile phone

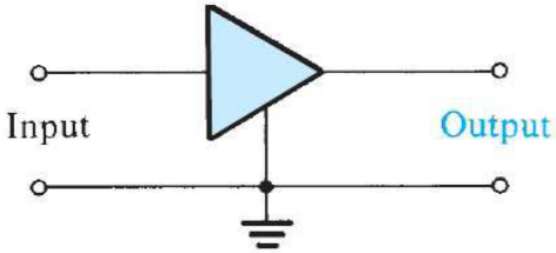


- LNA: low noise amplifier
- A/D: analog to digital converter

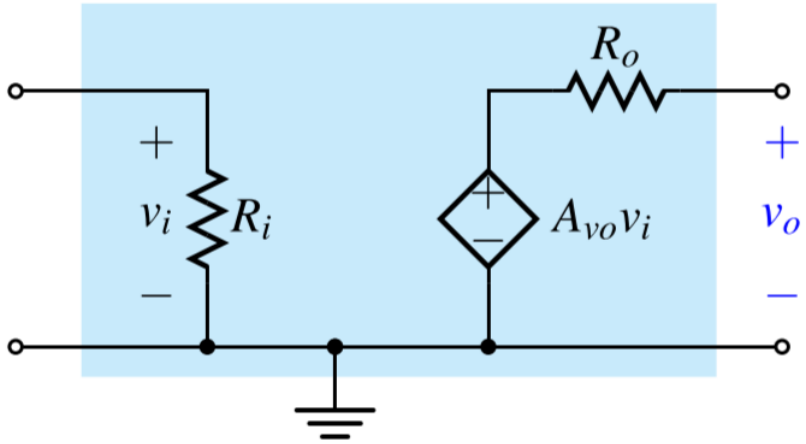
Since the signal received by antenna is too weak, which is usually in μV range, while the A/D converter required the input signal with the range from 0 to 3.3 V.

The processing could be much easier if the signal magnitude is larger.

1-2 Amplifiers



The signal amplifier is a two-port network and only **dependent sources** could be used to realize amplifiers

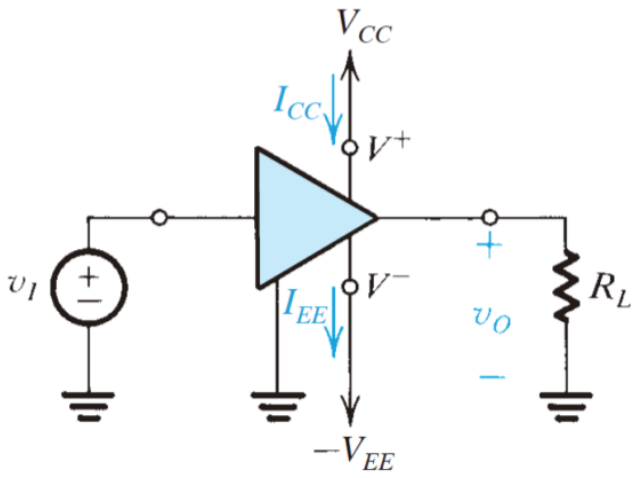


- R_i: input resistance
- R_o: output resistance
- A_{vo}: **open-circuit** voltage gain

Different Amplifiers

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		$A_{vo} = \frac{v_o}{v_i}$	$R_i = \infty, R_o = 0$
Current Amplifier		$A_{is} = \frac{i_o}{i_i}$	$R_i = 0, R_o = \infty$
Transconductance Amplifier		$G_m = \frac{i_o}{v_i}$	$R_i = \infty, R_o = \infty$
Transresistance Amplifier		$R_m = \frac{v_o}{i_i}$	$R_i = 0, R_o = 0$

Amplifier Power Efficiency



The DC power delivered to the amplifier is

$$P_{dc} = V_{CC} I_{CC} + V_{EE} I_{EE}$$

The power-balance equation over the circuit is

$$P_{dc} + P_I = P_L + P_{\text{dissipated}}$$

The amplifier power efficiency is

$$\eta = \frac{P_L}{P_{dc}} \times 100\%$$

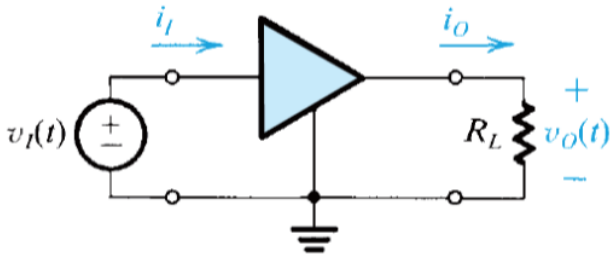
Characters of Amplifiers

There are several important parameter of amplifiers:

- A: Gain
- R_i: Input Resistance
- R_o: Output Resistance

Amplifier Gain

A voltage amplifier fed with a signal $v_i(t)$ and connected to a load resistance R_L



- Voltage Gain: $A_v = \frac{v_o}{v_i}$
- Current Gain: $A_i = \frac{i_o}{i_i}$
- Power Gain: $A_p = \frac{v_o i_o}{v_i i_i}$

And there is relationship between power gain, voltage gain and current gain is

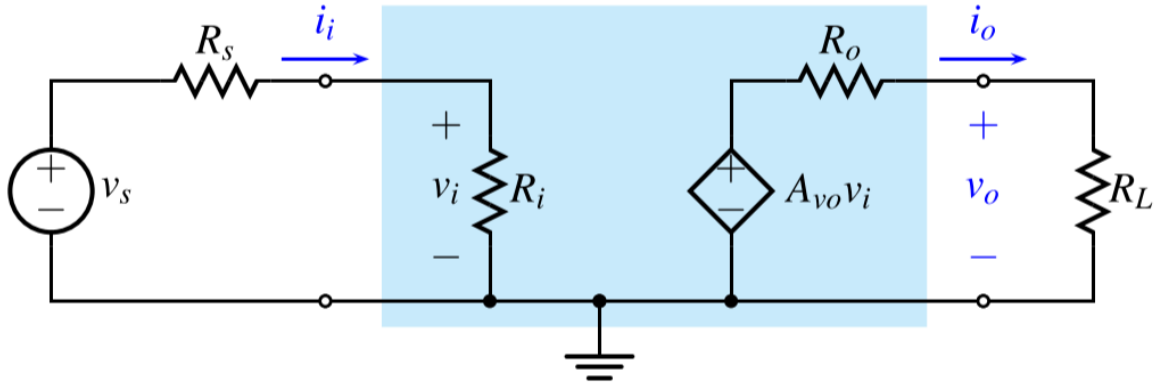
$$A_p = A_o A_i$$

And electronics engineers prefer to express amplifier gain with **logarithmic measure**

- Voltage Gain in decibels: $20 \log ||A_v|| \ dB$
- Current Gain in decibels: $20 \log ||A_i|| \ dB$
- Power Gain in decibels: $10 \log ||A_p|| \ dB$

Input and Output Resistance

The input resistance R_i is **an equivalent resistance** that accounts for the fact that the amplifier draws an input current from the signal source



$$v_i = v_s \frac{R_i}{R_i + R_s}$$

A **voltage amplifier** with ***larger input resistance*** draw less current from the signal source, and its v_i is closer to v_s

$$v_o = A_{vo} v_i \frac{R_L}{R_L + R_o}$$

A **voltage amplifier** with ***smaller output resistance*** has stronger ability to drive a heavy load

Determine Input and Output Resistance

- Determine R_i: by applying an **input voltage** v_i and calculating the **input current** i_i

$$R_i = \frac{v_i}{i_i}$$

- Determine R_o: by finding ratio of the **open-circuit output voltage** to the **short-circuit output current**

Overall Gain

- Voltage Gain

$$A_v = \frac{v_o}{v_i} = A_{vo} \cdot \frac{R_L}{R_L + R_o}$$

- Overall Gain

$$\frac{v_o}{v_s} = A_{vo} \cdot \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$$

Characterizing Amplifiers

A perfect **voltage amplifier** should have

- large input resistance
- small output resistance
- a gain that is controllable ina wide range

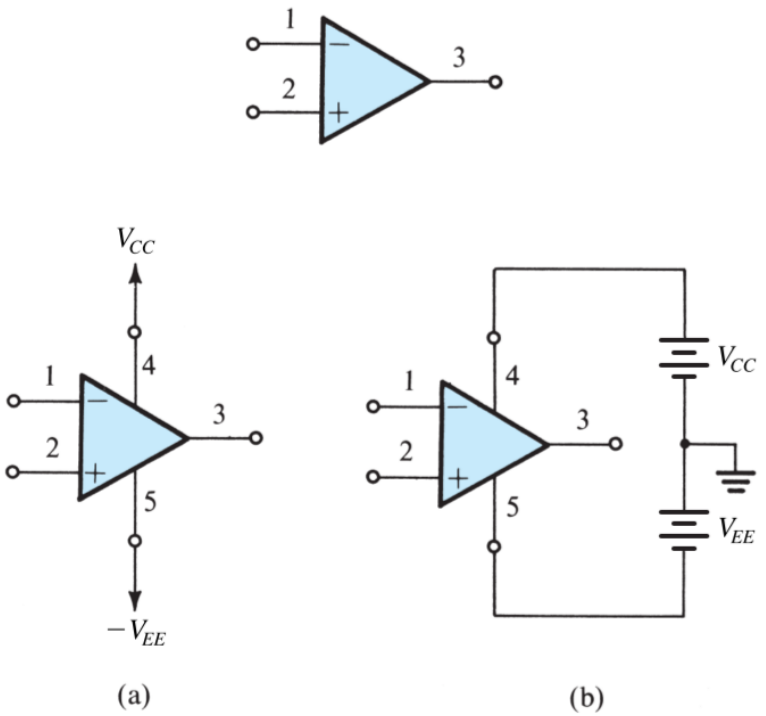
Chapter 2 Op Amp

2-1 Ideal Op Amp

Models of Ideal Op Amp

From a signal point of view the op amp has three terminals: two inputs and one output terminal

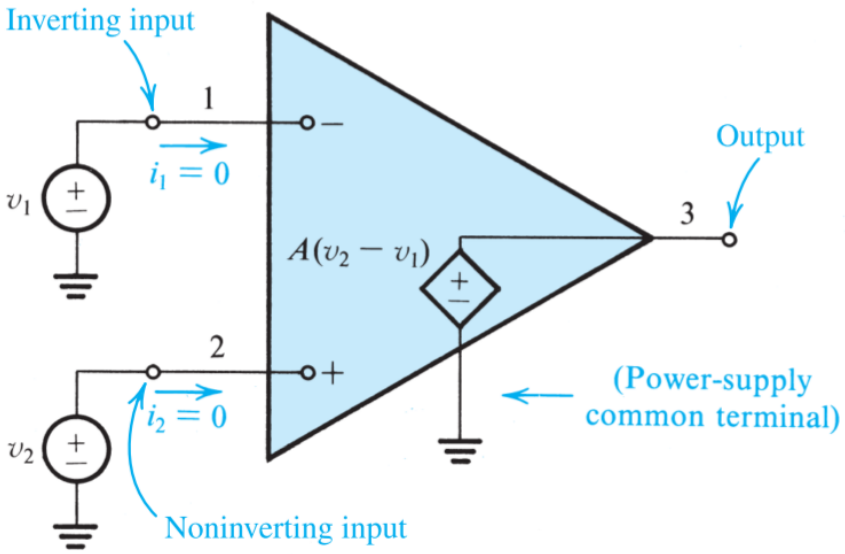
Pin	Terminal
1	Negative Input
2	Positive Input
3	Output



Most IC op amp have 5 terminals: two inputs, one output and two DC power terminals

Pin	Terminal
1	Negative Input
2	Positive Input
3	Output
4	Positive Power
5	Negative Power

Function and Characteristics of the Ideal Op Amp



- Infinite input impedance
- Zero output impedance
- Zero common-mode gain
- Infinite open-loop gain A
- Infinite bandwidth

Differential and Common-Mode Signals

The differential input signal v_{Id} is simply the difference between the two input signals v_1 and v_2

$$v_{Id} = v_2 - v_1$$

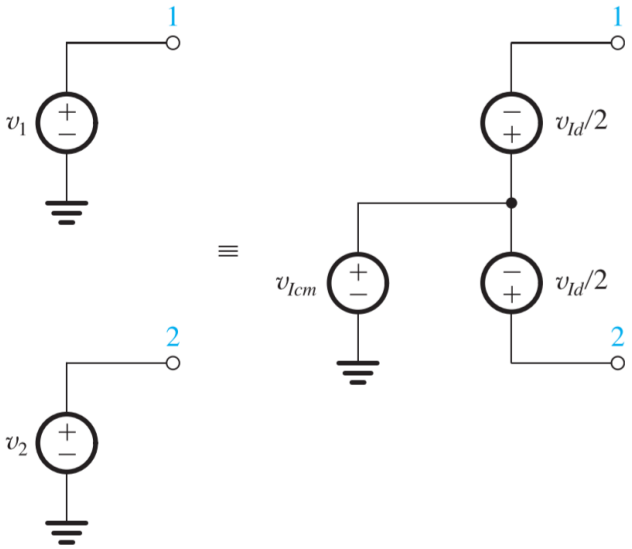
The common-mode input signal v_{Icm} is the average of the two input signals v_1 and v_2

$$v_{Icm} = \frac{1}{2}(v_1 + v_2)$$

Made the equation express v_1 and v_2 as

$$\begin{cases} v_1 = v_{Icm} - v_{Id}/2 \\ v_2 = v_{Icm} + v_{Id}/2 \end{cases}$$

which could turn the input terminals into another presentation

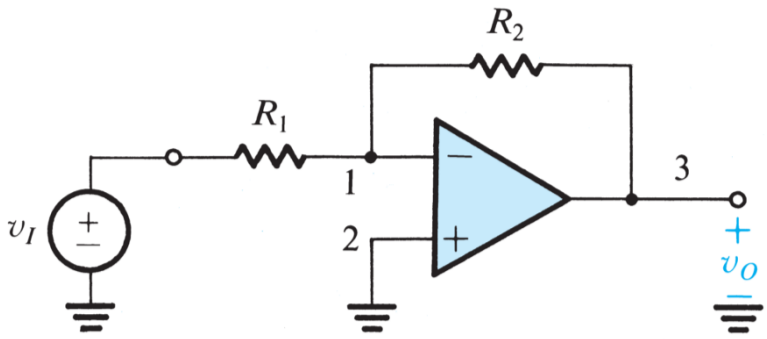


Analysis Method

There are tree rules to analyze the op amp circuit

- **virtual short**: $v_+ = v_-$
- **virtual open**: $i_+ = 0, i_- = 0$
- **zero output resistance**: $R_O = 0$

2-2 Inverting Amplifier



The **closed-loop gain** G could be determined as

$$G = \frac{v_O}{v_I}$$

Since $v_- = v_+ = 0$

$$i_1 = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1} \quad i_2 = \frac{0 - v_O}{R_2} = -\frac{v_O}{R_2}$$

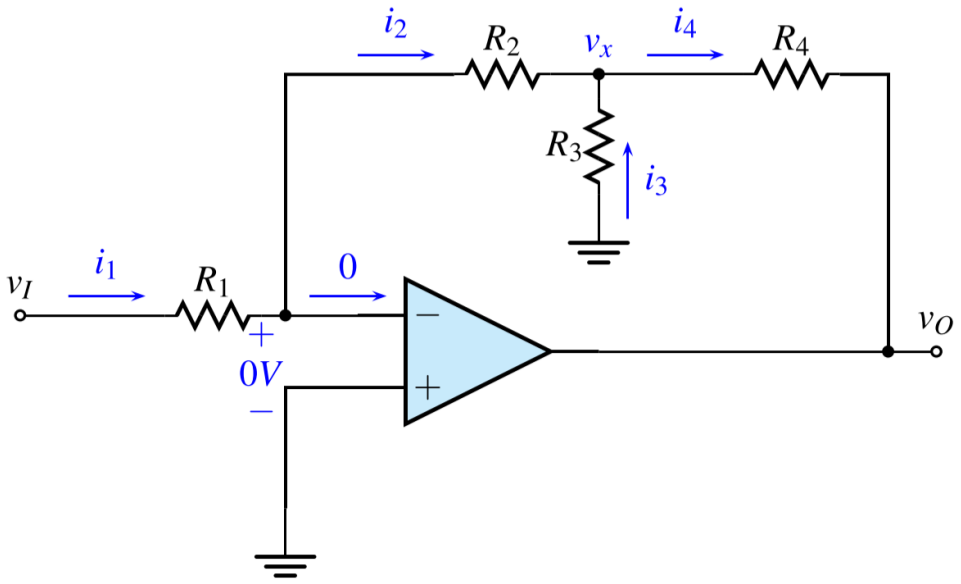
And we have $i_1 = i_2$

$$\frac{v_I}{R_1} = -\frac{v_O}{R_2}$$

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

- gain: R_2/R_1
- input resistance: R_1
- output resistance: $R_O = 0$

T-shape Feedback Network



Since $v_- = v_+ = 0$

$$i_1 = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

And we have $i_1 = i_2$

$$v_x = -i_2 R_2 = -i_1 R_2 = -\frac{R_2}{R_1} v_I$$

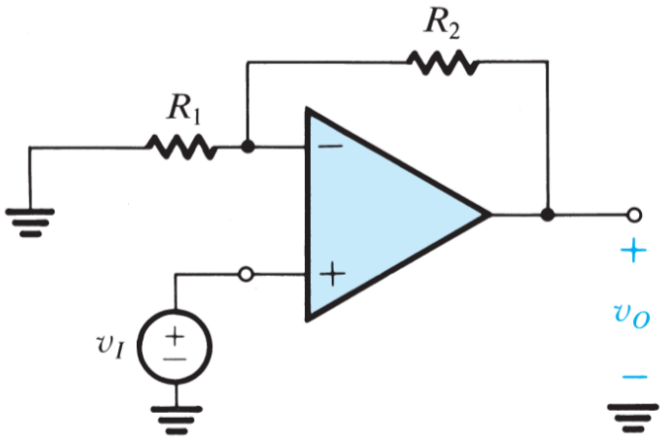
Therefore i_3 could be determined as

$$i_3 = \frac{v_x}{R_3} = -\frac{R_2}{R_1} \cdot \frac{v_I}{R_3}$$

The output voltage could be calculated

$$
\begin{aligned}
v_o &= v_x + i_4 R_4 \\
&= -\frac{R_2}{R_1} v_I - (i_2 + i_3) R_4 \\
&= -\frac{R_2}{R_1} v_I - (i_1 + i_3) R_4 \\
&= -\frac{R_2}{R_1} v_I - (\frac{1}{R_1} + \frac{R_2}{R_1} \cdot \frac{1}{R_3}) v_I R_4 \\
&= -(\frac{R_2}{R_1} + \frac{R_4}{R_1} + \frac{R_2}{R_1}\frac{R_4}{R_3}) v_I
\end{aligned}
$$

2-3 Noninverting Amplifier



The **closed-loop gain** G could be determined as

$$
G = \frac{v_O}{v_I}
$$

Since $v_- = v_+ = v_1$

$$
i_1 = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1} \quad i_2 = \frac{v_O - v_I}{R_2}
$$

And we have $i_1 = i_2$

$$\frac{v_I}{R_1} = \frac{v_O - v_I}{R_2}$$

$$(R_1 + R_2)v_I = R_1 v_O$$

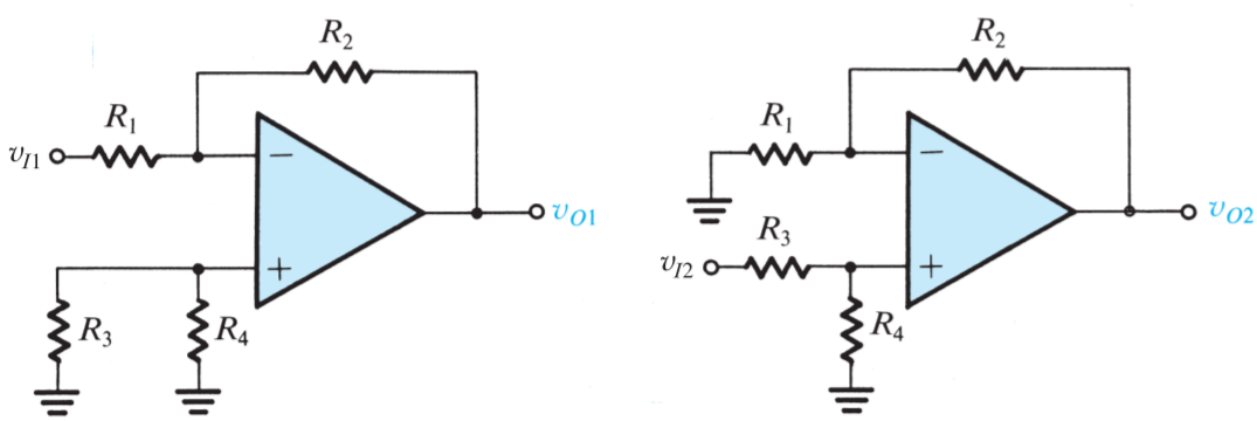
$$\frac{v_O}{v_I} = (1 + \frac{R_2}{R_1})$$

- gain: $1 + \frac{R_2}{R_1}$
- input resistance: $R_I = \infty$
- output resistance: $R_O = 0$

2-4 Difference Amplifier

A difference amplifier is one that responds to the difference between the two signals applied at its input and ideally rejects signals that are common to the two inputs.

Take the following two amplifiers into consideration



$$v_{O1} = -\frac{R_2}{R_1}v_{I1} \qquad v_{O2} = (1 + \frac{R_2}{R_1})\frac{R_4}{R_3 + R_4}v_{I2}$$

To produce no response to the common part, which means $v_{I1} = v_{I2}$

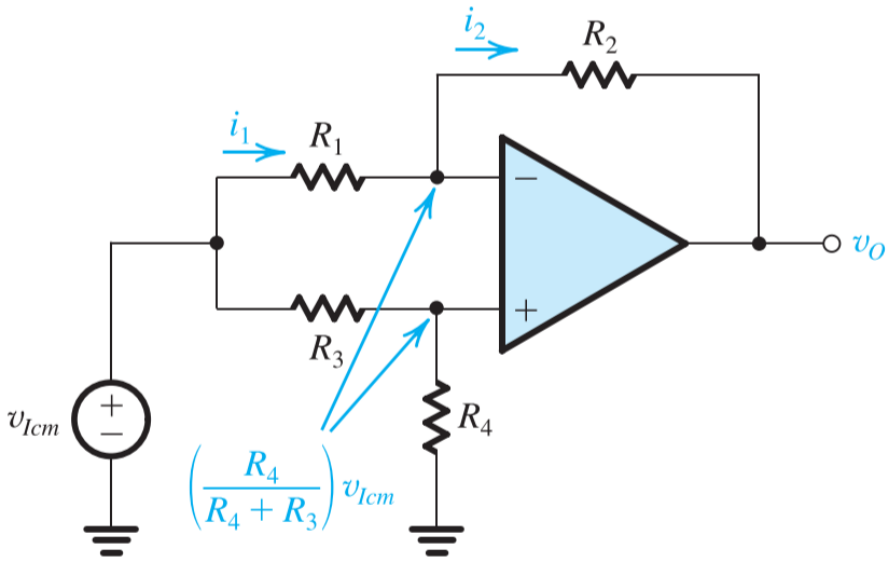
$$v_{O1} + v_{O2} = 0$$

$$\frac{R_2}{R_1} v_{I1} = (1 + \frac{R_2}{R_1}) \frac{R_4}{R_3 + R_4} v_{I2}$$

$$\frac{R_2}{R_1} \cdot \frac{R_1}{R_1 + R_2} = \frac{R_4}{R_3 + R_4}$$

$$\frac{R_4}{R_2} = \frac{R_3}{R_1}$$

Now the common difference amplifier could be analyzed in the same way



The voltage on the input terminals could be determined as

$$\frac{R_4}{R_3 + R_4} v_{Icm}$$

The current on R_1 is

$$i_1 = \frac{R_3}{R_1} \frac{1}{R_3 + R_4} v_{Icm}$$

And we know $i_1 = i_2$

$$v_O = \frac{R_4}{R_3 + R_4} v_{Icm} - \frac{R_3}{R_1} \frac{R_2}{R_3 + R_4} v_{Icm}$$

$$= \frac{v_{Icm}}{R_3 + R_4} (R_4 - \frac{R_3}{R_1} R_2)$$

$$\frac{v_O}{v_{Icm}} = \frac{R_4}{R_3 + R_4} (1 - \frac{R_2}{R_1} \frac{R_3}{R_4}) = 0$$

Since we've chosen the resistor ratio, the gain for the common-mode is 0

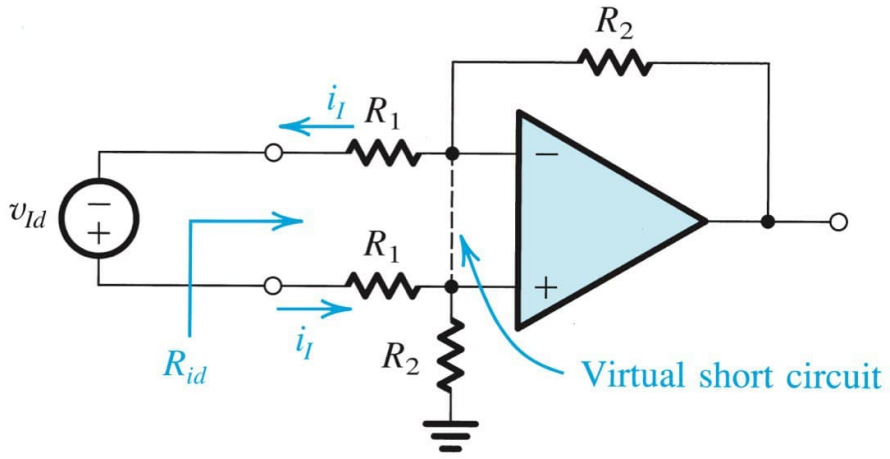
But any mismatch in the resistance ratio could cause A_{cm} nonzero, hence, high input resistance is required for a difference amplifier, which is called **differential input resistance** R_{id}

We assume that

$$R_3 = R_1 \qquad R_4 = R_2$$

And the definition of the **differential input resistance** is

$$R_{Id} = \frac{v_{Id}}{i_I}$$



Since the two terminals shares the same voltage, the loop seems to be a short circuit.

$$v_{Id} = i_I R_1 + 0 + i_I R_1$$

Thus

$$R_{Id} = 2R_1$$

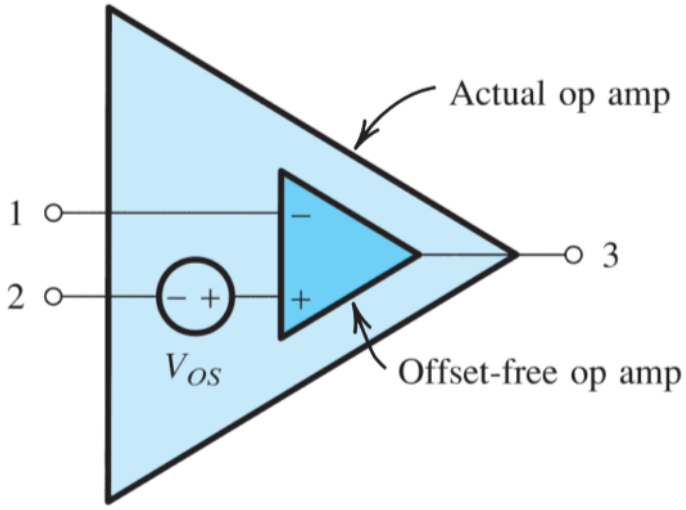
2-5 DC Imperfections

Offset Voltage

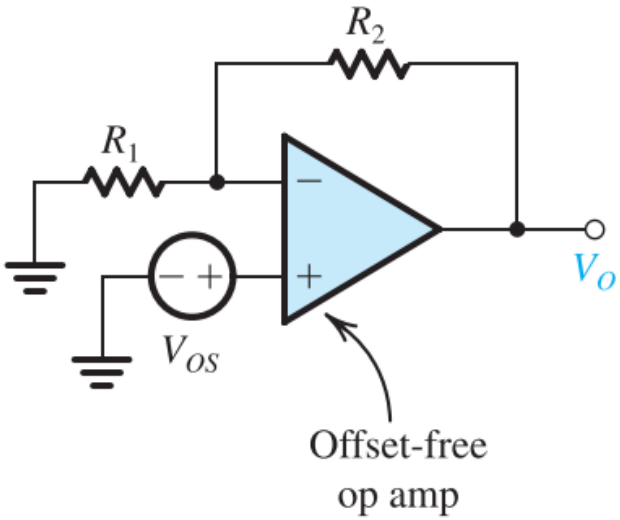
If the two input terminals of the op amp are tied together and connected to ground, it will be found that despite the fact thar $v_{Id} = 0$, a finite dc voltage exists at the output.

The op-amp output can be brought back to its ideal value of $0\ V$ by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp.

It follows that the **input offset voltage** V_{OS} must be of equal magnitude and of opposite polarity of the voltage



Based on the principle of superposition, we can find the both the inverting and the noninverting amplifier configurations result in the same circuit

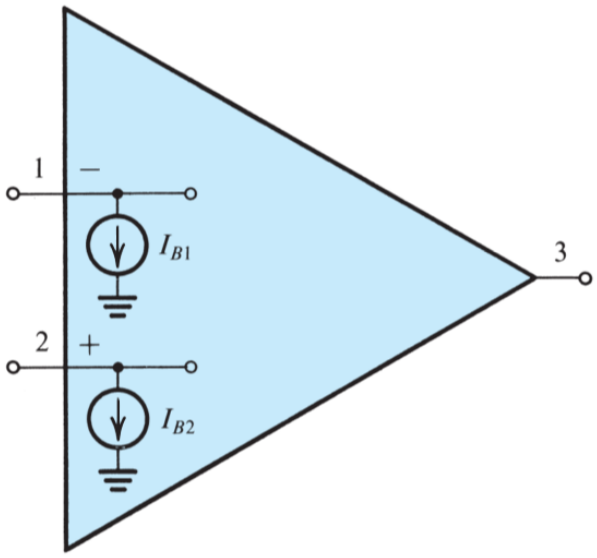


The output voltage due to V_{OS} is found to be

$$V_O = V_{OS}\left[1 + \frac{R_2}{R_1}\right]$$

Input Bias and Offset Currents

In order for the op amp to operate, its two input terminals have to be supplied with dc currents, termed the **input bias currents**, which are independent og the fact that a real op amp has finite input resistance



The average value I_B is called the **input bias current**

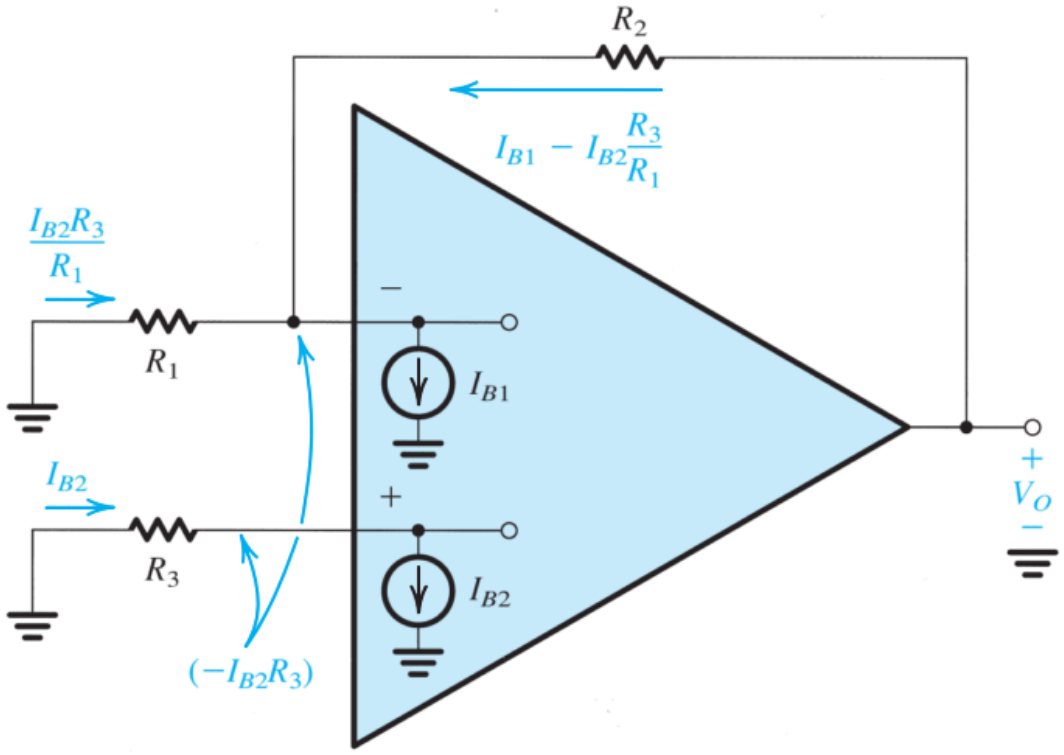
$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and the difference is called the **input offset current** and is given by

$$I_{OS} = |I_{B1} - I_{B2}|$$

> Typical values for general-purpose op amps are $I_B = 100\ nA$ and $I_{OS} = 10\ nA$

Now we can analyses the closed loop amplifier, taking into account the input bias currents



$$V_O = -I_{B2}R_3 + R_2(I_{B1} - \frac{R_3}{R_1}I_{B2})$$

Consider the case $I_{B1} = I_{B2} = I_B$, which results in

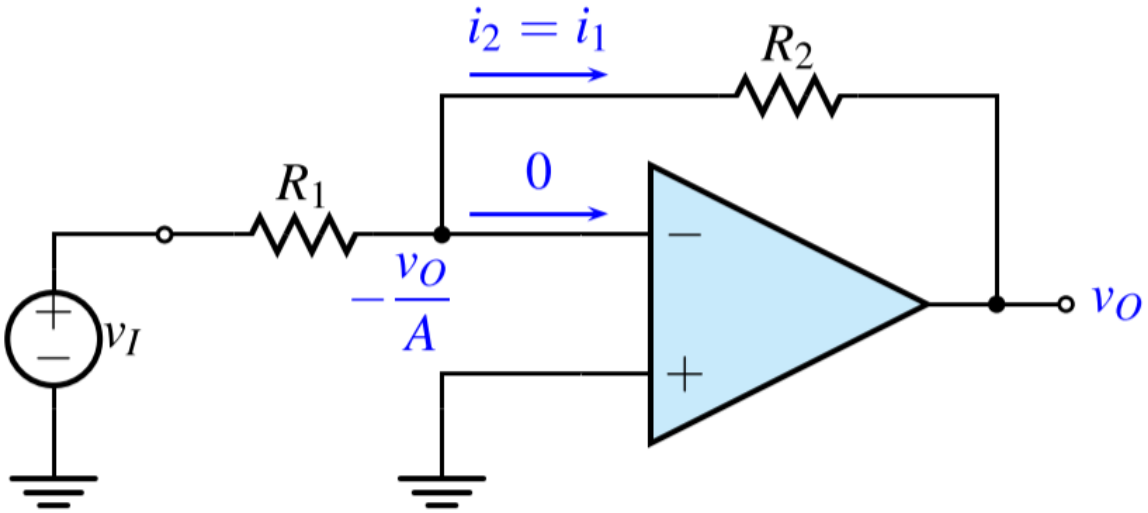
$$V_O = I_B[R_2 - R_3(1 + R_2/R_1)]$$

Thus output voltage could be zero when selecting R_3 equal to

$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1R_2}{R_1 + R_2}$$

But in an **ac-coupled** amplifier the dc resistance seen by the inverting terminal is R_2, then R_3 is chosen equal to R_2

Effect of Finite Open-loop Gain



Since the op-amp open-loop gain A is finite

$$v_+ - v_- = \frac{v_O}{A} \Rightarrow v_- = -\frac{v_O}{A}$$

thus

$$i_1 = \frac{v_I - (-v_O/A)}{R_1} = \frac{v_I + v_O/A}{R_1}$$

Then the output voltage v_O becomes

$$v_O = -\frac{v_O}{A} - i_1 R_2 = -\frac{v_O}{A} - \left(\frac{v_I + v_O/A}{R_1}\right) R_2$$

where the the closed-loop gain is found as

$$G = \frac{v_O}{v_I} = -\frac{R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

Similarly, we could get the closed-loop gain for the noninverting amplifier

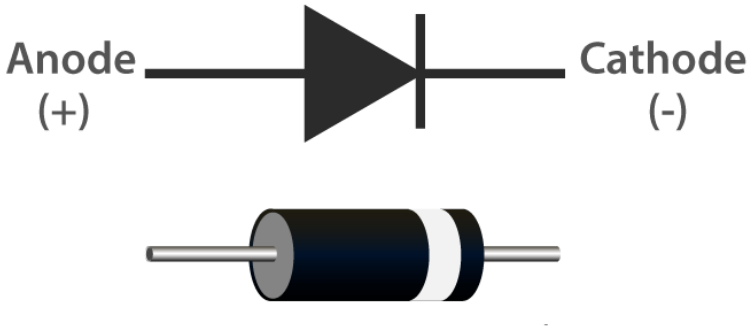
$$G = \frac{v_O}{v_I} = \frac{1 + (R_2/R_1)}{1 + (1 + R_2/R_1)/A}$$

Chapter 3 Diode

3-1 Ideal Diode

The **ideal diode** may be considered to be the most fundamental nonlinear circuit element, which has two nodes:

- **anode**: the positive terminal
- **cathode**: the negative terminal

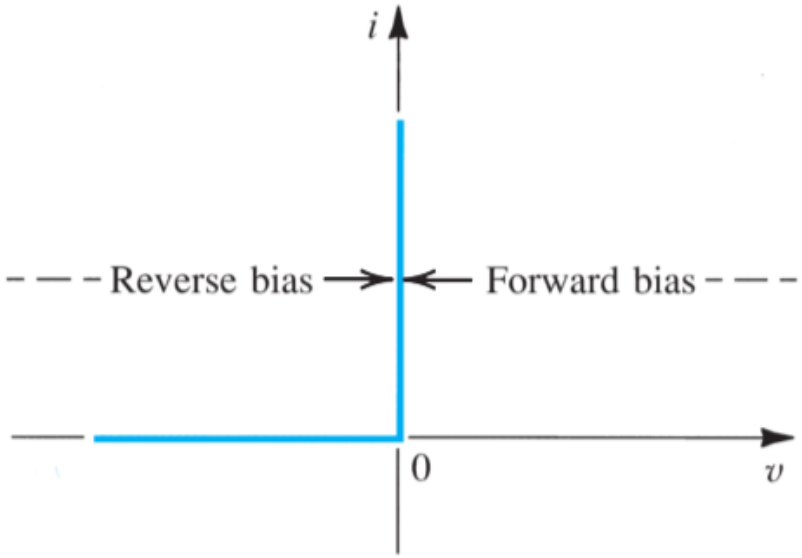


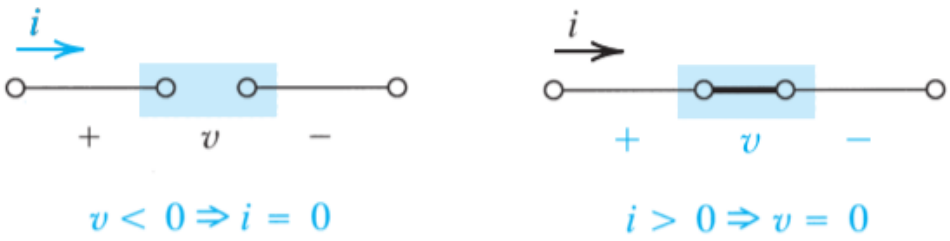
If a negative voltage is applied

- no current flows
- reverse biased
- **cut off**

If a positive current is applied

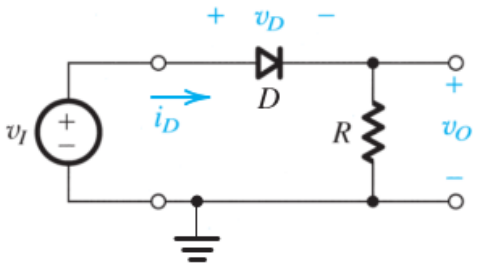
- zero voltage drop
- forward biased
- **turn on**



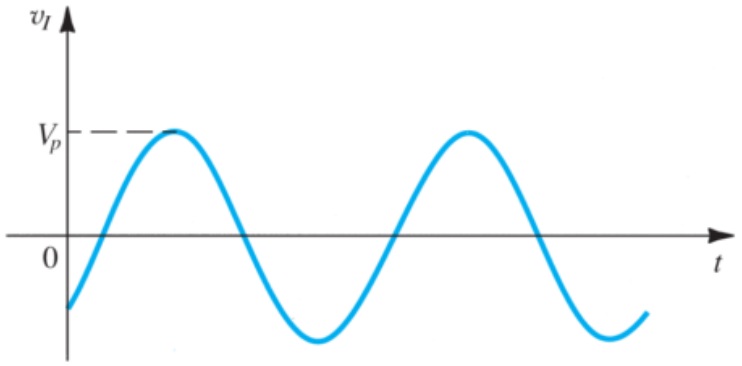


$v < 0 \Rightarrow i = 0$ $\quad$ $i > 0 \Rightarrow v = 0$

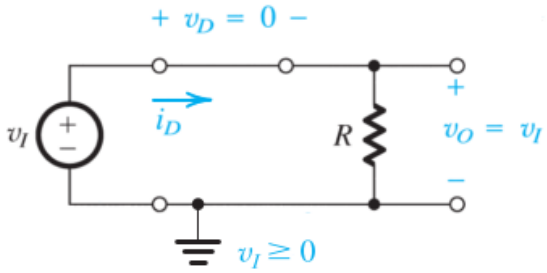
A simple Application: The Rectifier



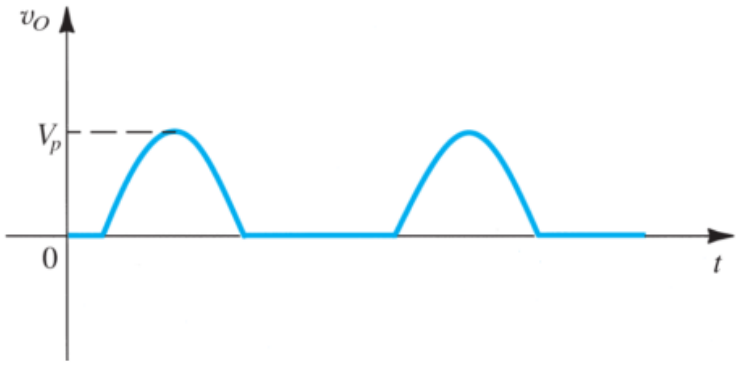
(a)



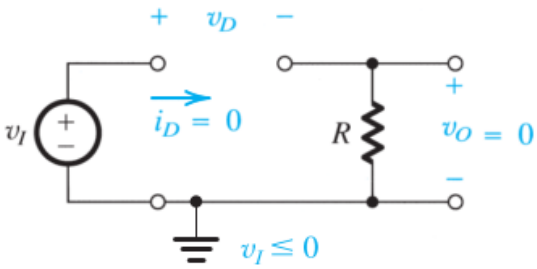
(b)



(c)

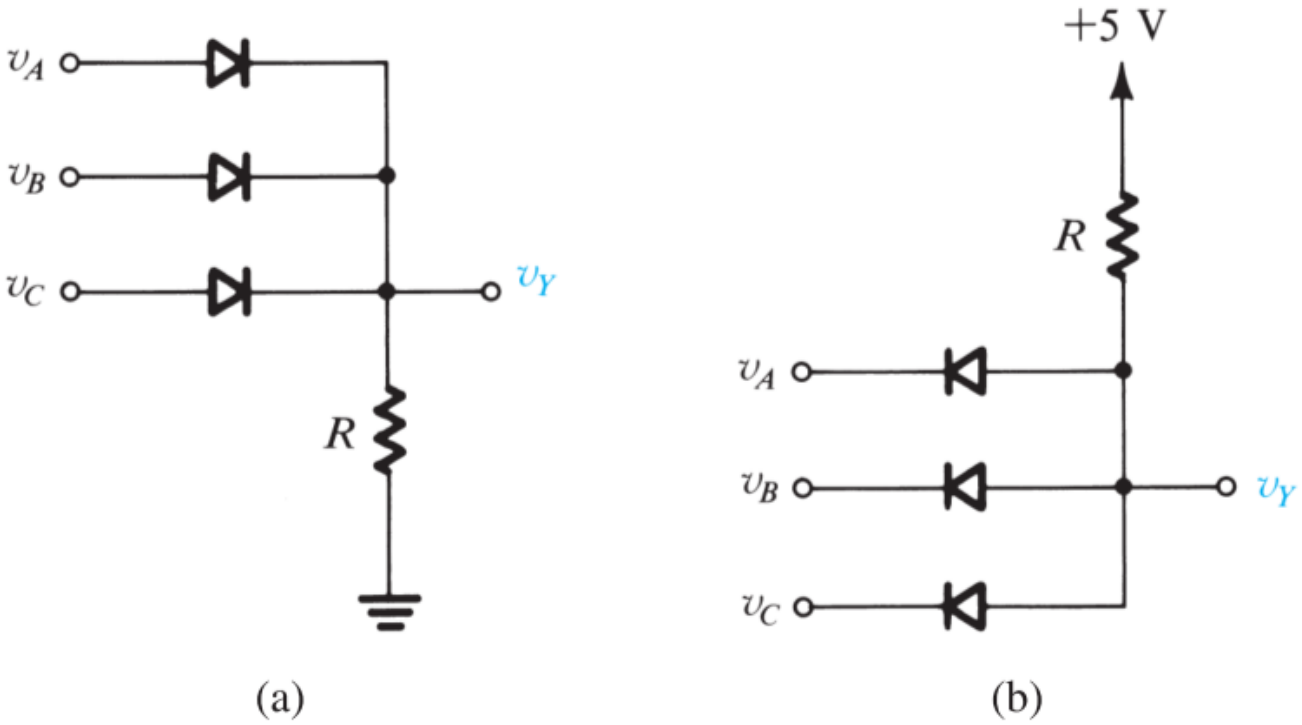


(e)



(d)

Another Application: Diode Logic Gates



For the figure (a), the circuit implements with the **logic OR function**

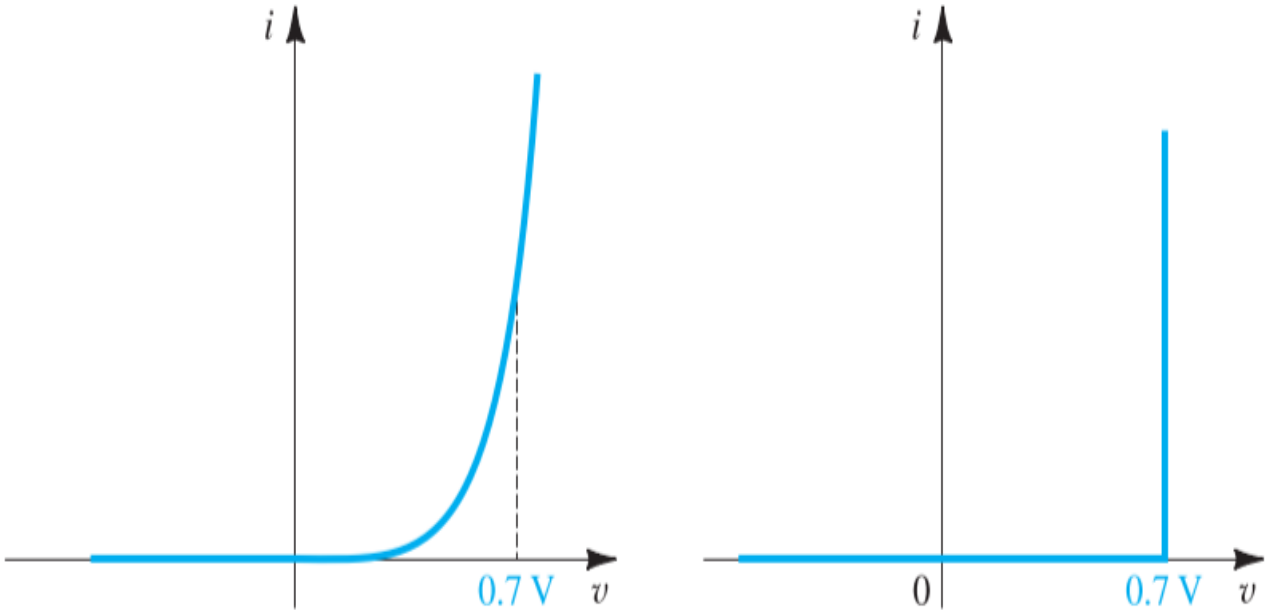
$$Y = A + B + C$$

For the figure (b), the circuit implements with the **logic AND function**

$$Y = A \cdot B \cdot C$$

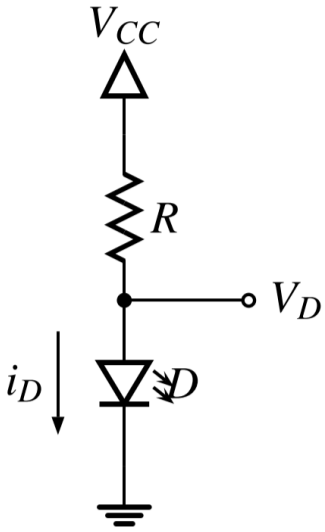
The Constant-Voltage-Drop Model

The simplest and most widely used diode model is the constant-voltage-drop model. This model is based on the observation that a forward-conducting diode has a voltage drop that varies in a relatively narrow range from 0.6 to 0.8 volt. The model assumes **this voltage to be constant at a value of 0.7 volt**



3-2 Special Diode Types

LED

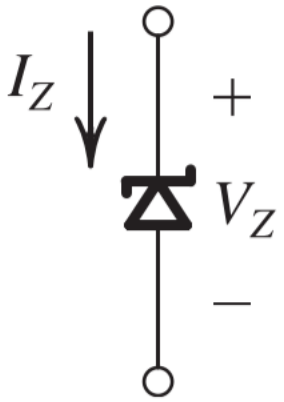


The light-emitting diode converts a forward current into light and the current on the diode could be determined by

$$i_D = \frac{V_{CC} - V_D}{R}$$

> typical current ratings ranges from around 1 mA to 20 mA depending on the size of a LED

Zener Diodes

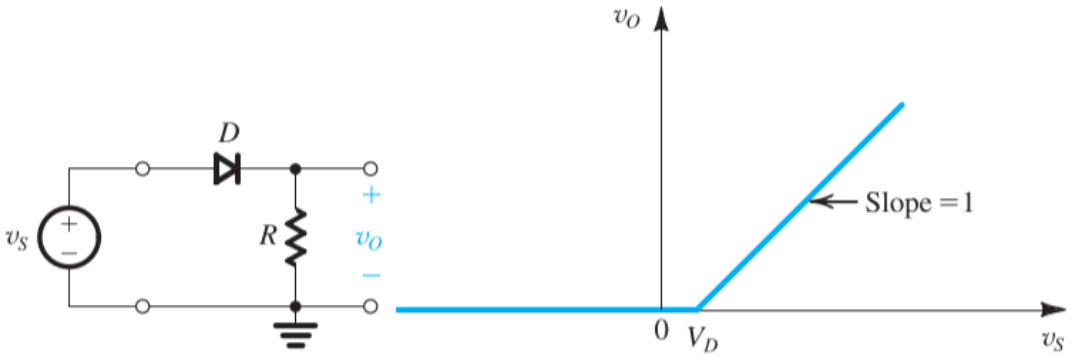


A Zener diode is a special type of diode designed to reliably allow current to flow "backwards" when a certain set reverse voltage, where it is be equivalently expressed as

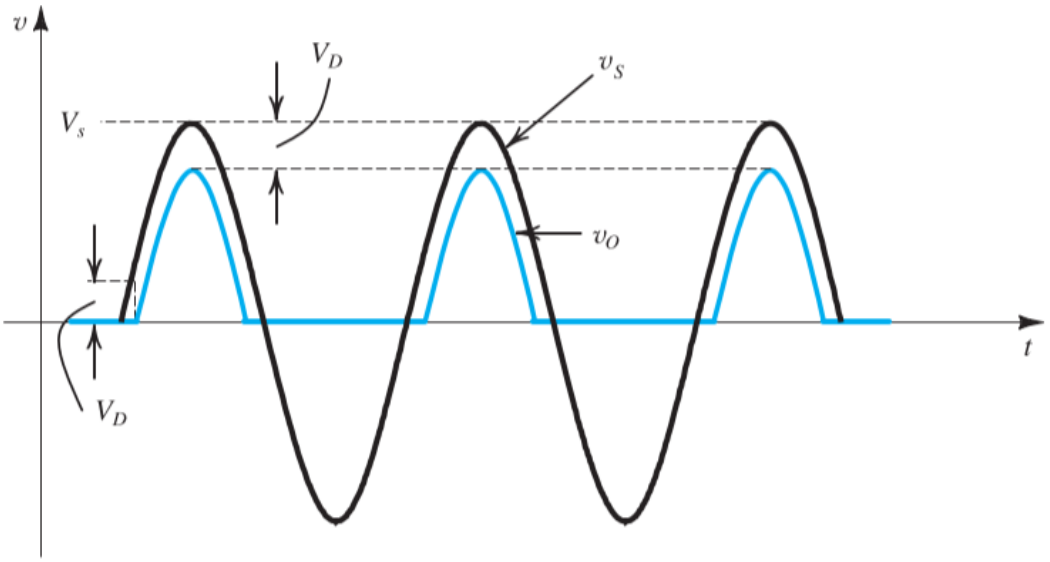
$$V_Z = V_{Z0} + r_Z I_Z$$

3-3 Rectifier and Limiting Circuits

The Half-Wave Rectifier



(a) (b)

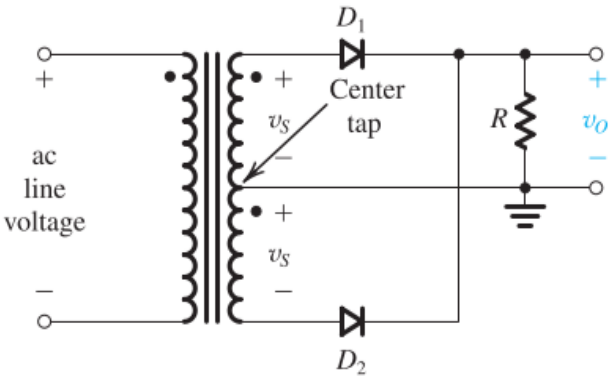


(c)

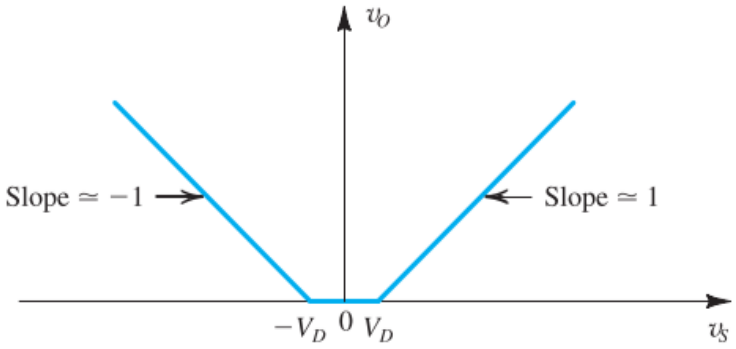
$$PIV = V_S$$

> **peak inverse voltage (PIV)**: the voltage that the diode must be able to withstand without breakdown

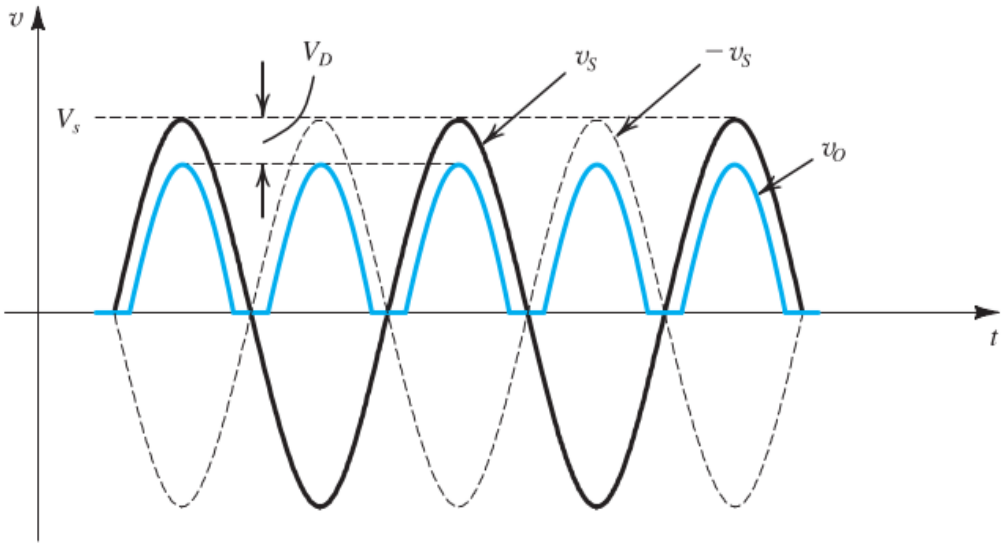
The Full-Wave Rectifier



(a)



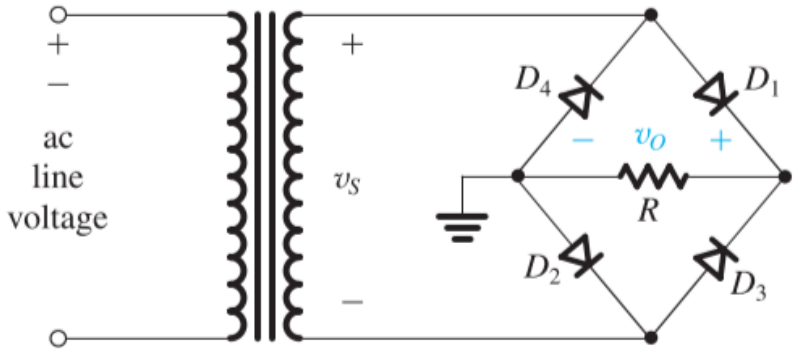
(b)



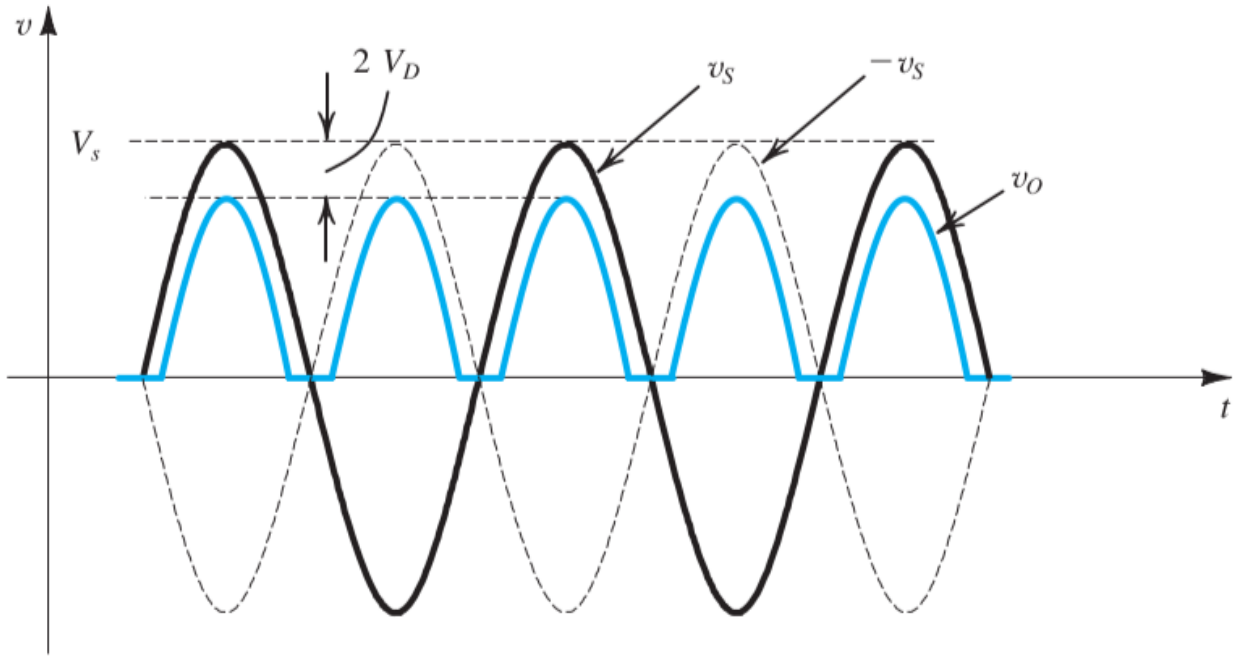
(c)

$$PIV = 2V_S - V_D$$

The Bridge Rectifier



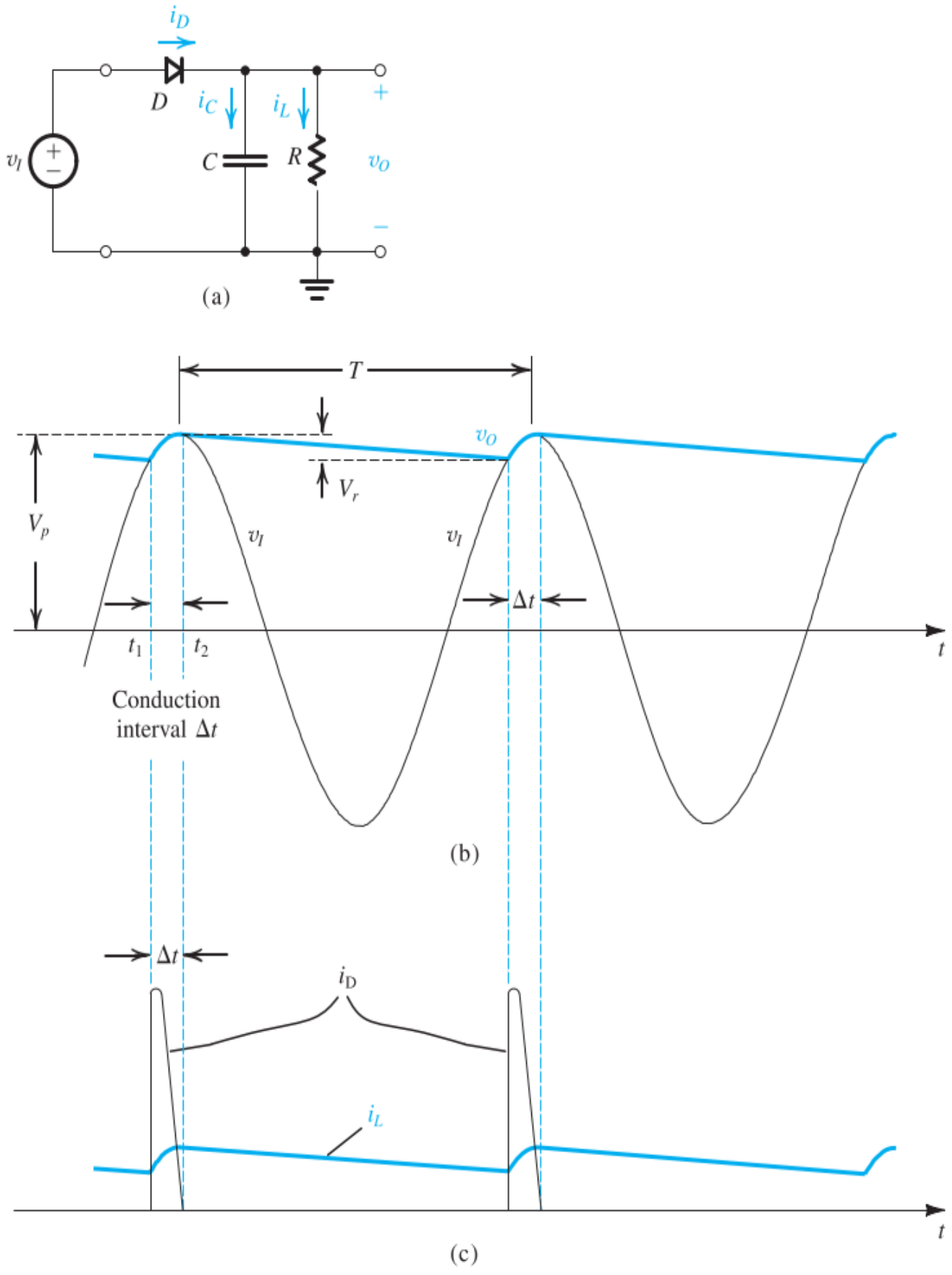
(a)



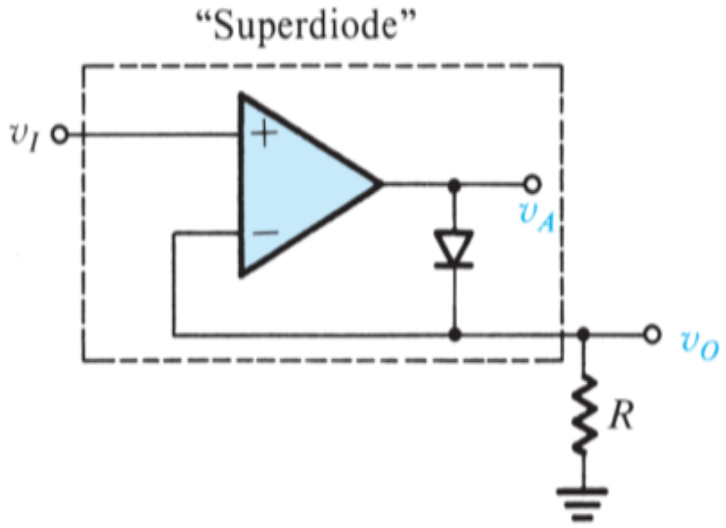
(b)

$$PIV = V_S - 2V_D + V_D = V_S - V_D$$

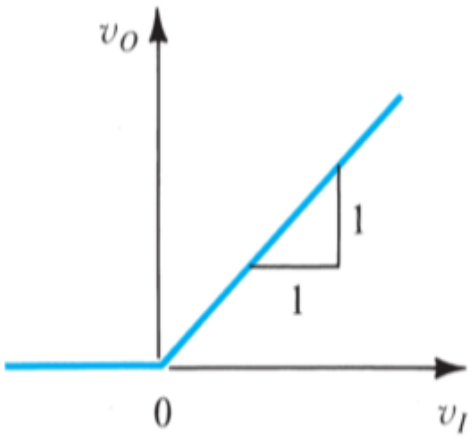
The Peak Rectifier



Precision Half-Wave Rectifier

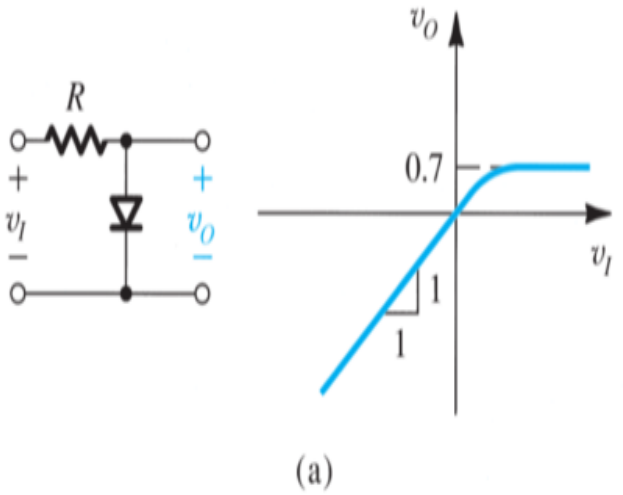


(a)

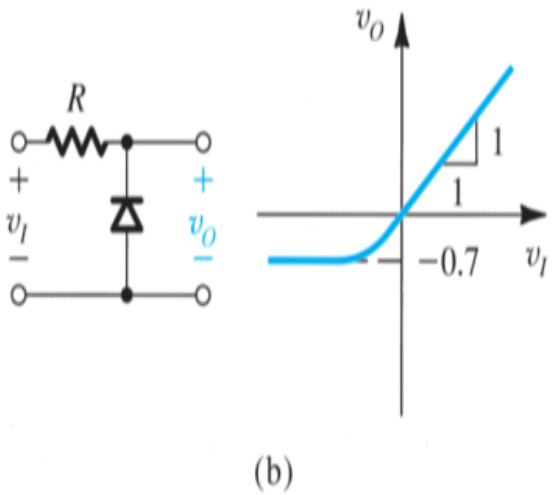


(b)

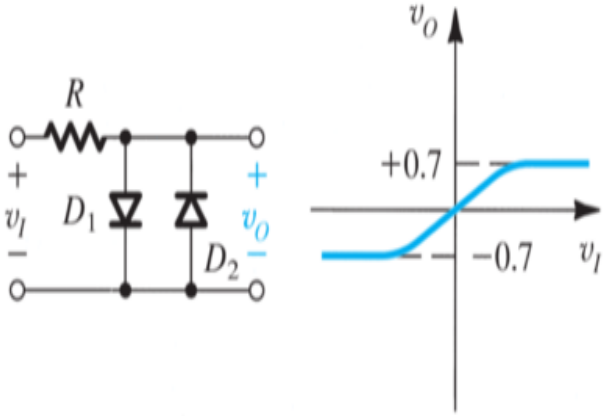
Limiter Circuits



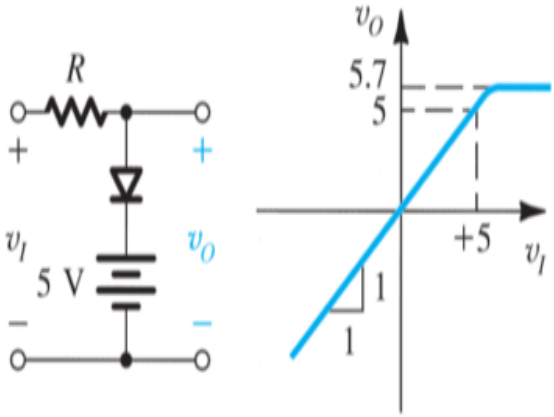
(a)



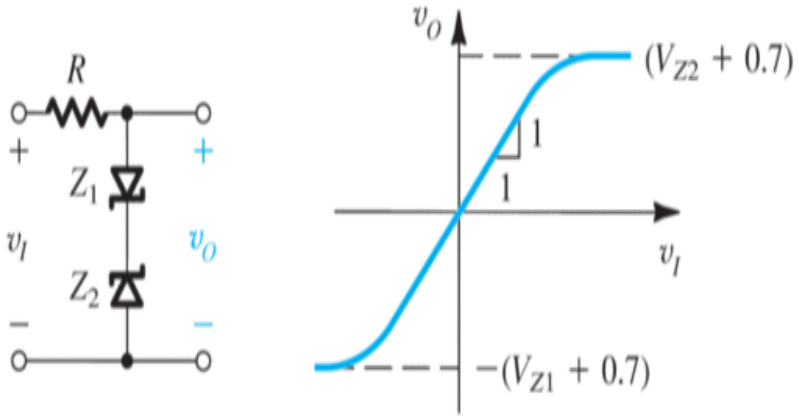
(b)



(c)

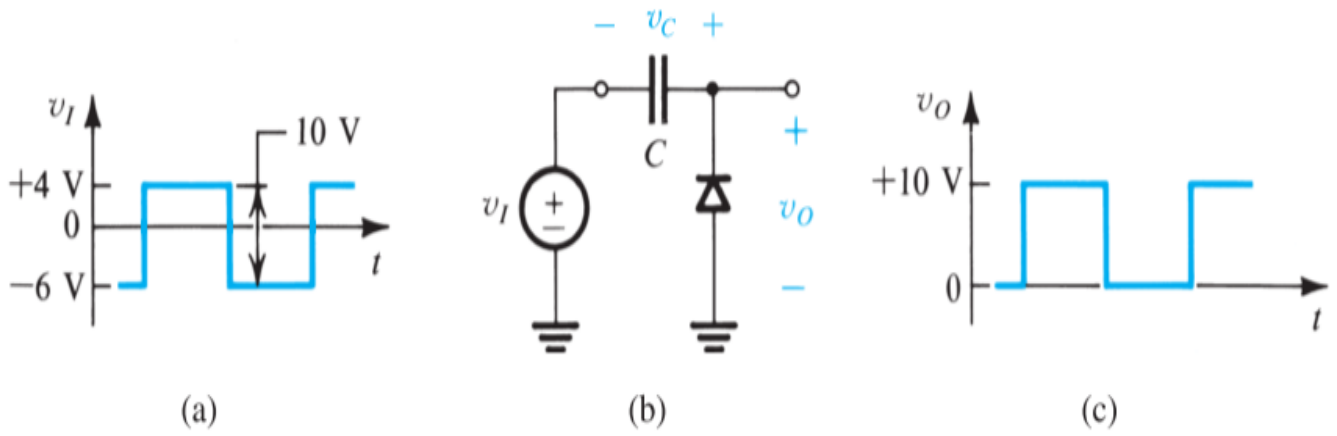


(d)



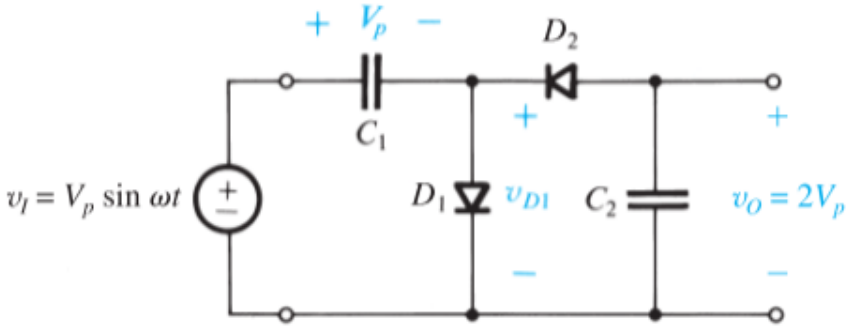
(e)

Clamped Capacitor

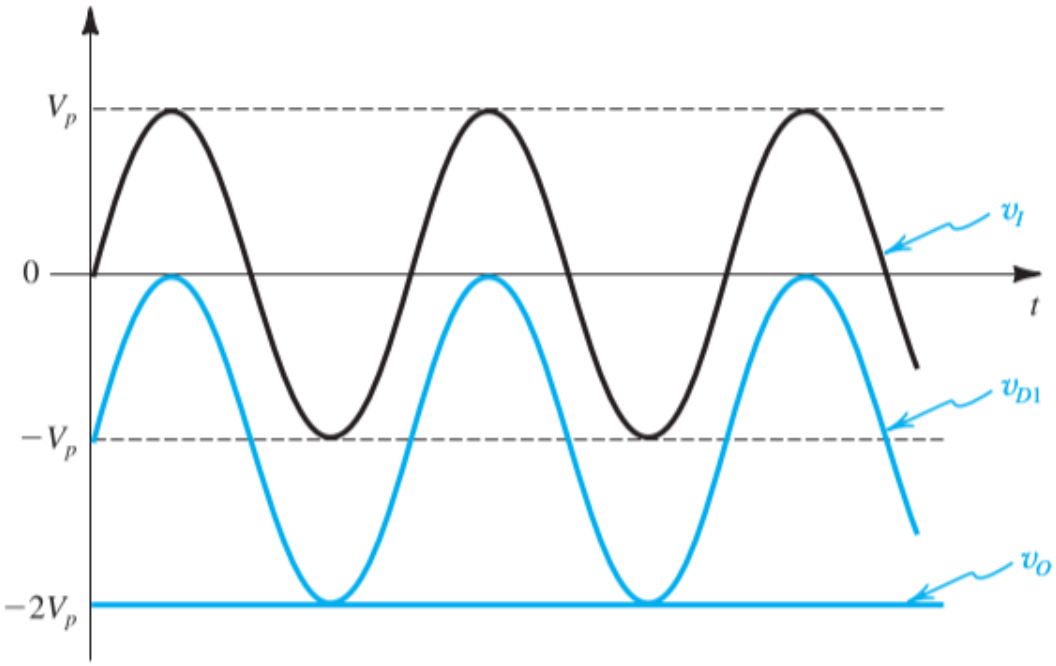


(a) (b) (c)

Voltage Doubler



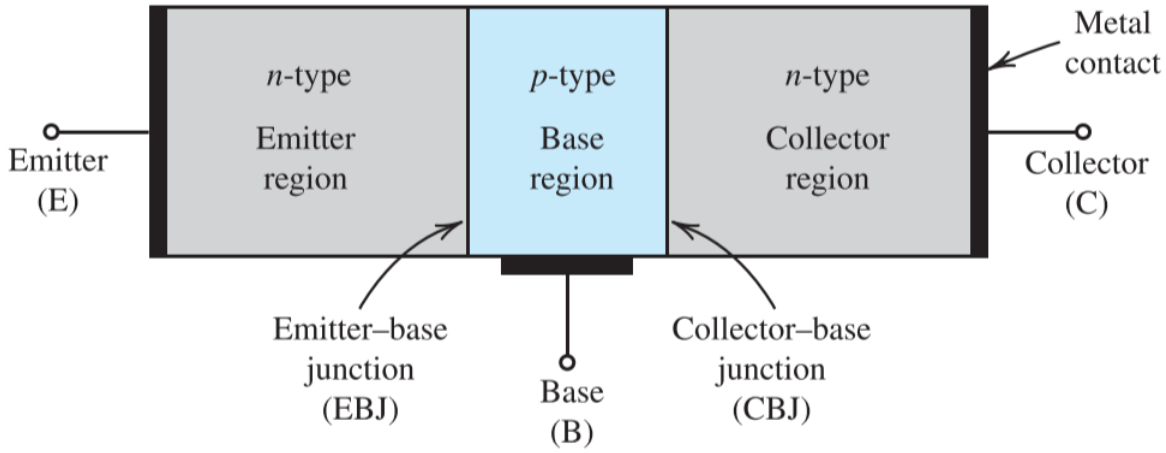
(a)



(b)

4-1 Device Structure and Physical Operation

The BJT consists of three semiconductor regions: the **emitter(E)** region, the **base(B)** region and the **collector(C)** region

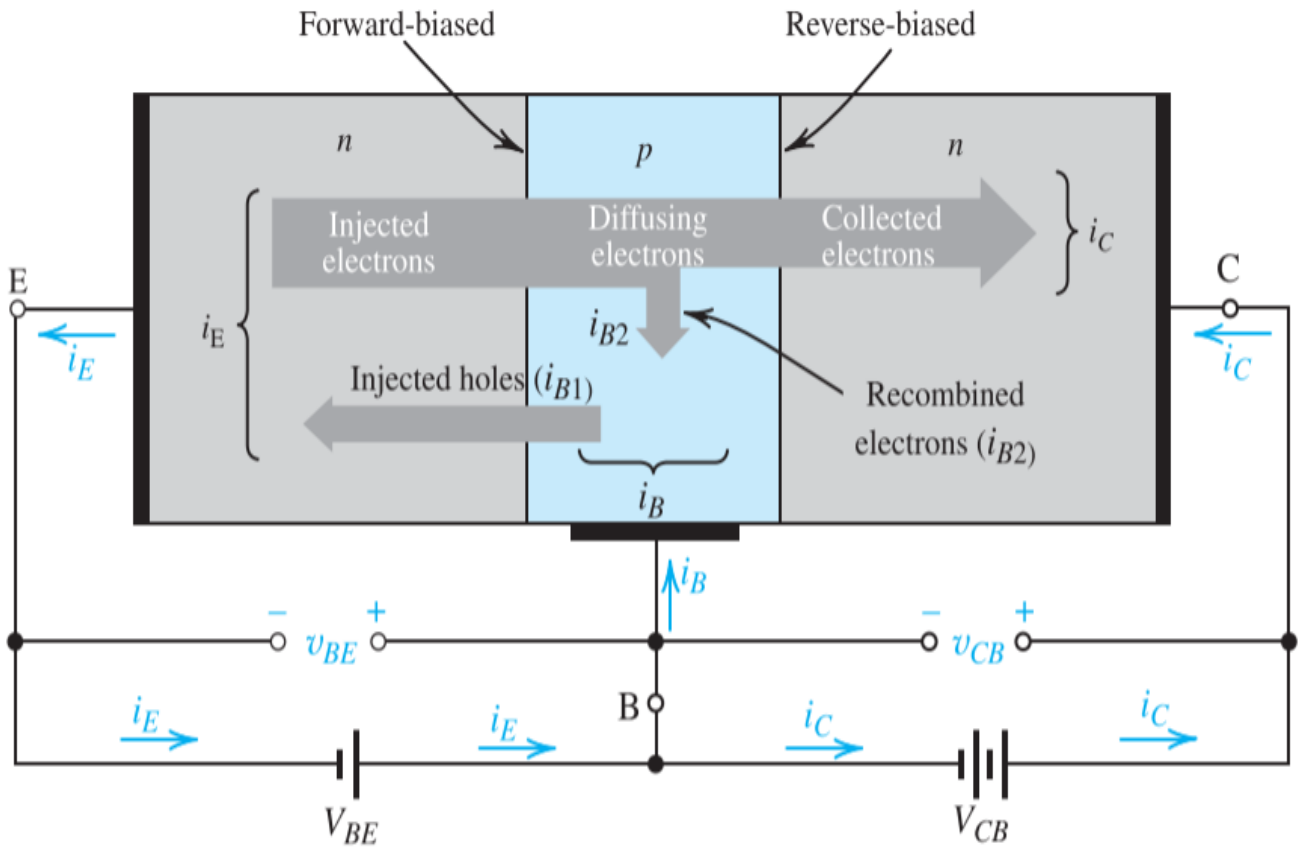


The transistor consists of two pn junctions, the **emitter-base junction** and **collector-base junction**. According to the different bias condition of each junction, there're three different working modes of transistors

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

The npn Transistor

Operation in Active Mode



The current on the collector could be defined as

$$i_C = I_S e^{v_{BE}/V_T}$$

- I_S: saturation current
- V_T: the thermal voltage ($25\ mV$ at room temperature)

The base current consists of two basic parts: the injected holes to the emitter and the recombined electrons from the majority current

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

- β: transistor parameter (mostly in range 50 to 200)

The emitter current is the sum of the base current and the emitter current

$$i_E = i_C + i_B = \frac{\beta + 1}{\beta} i_C = \frac{\beta + 1}{\beta} I_S e^{v_{BE}/V_T}$$

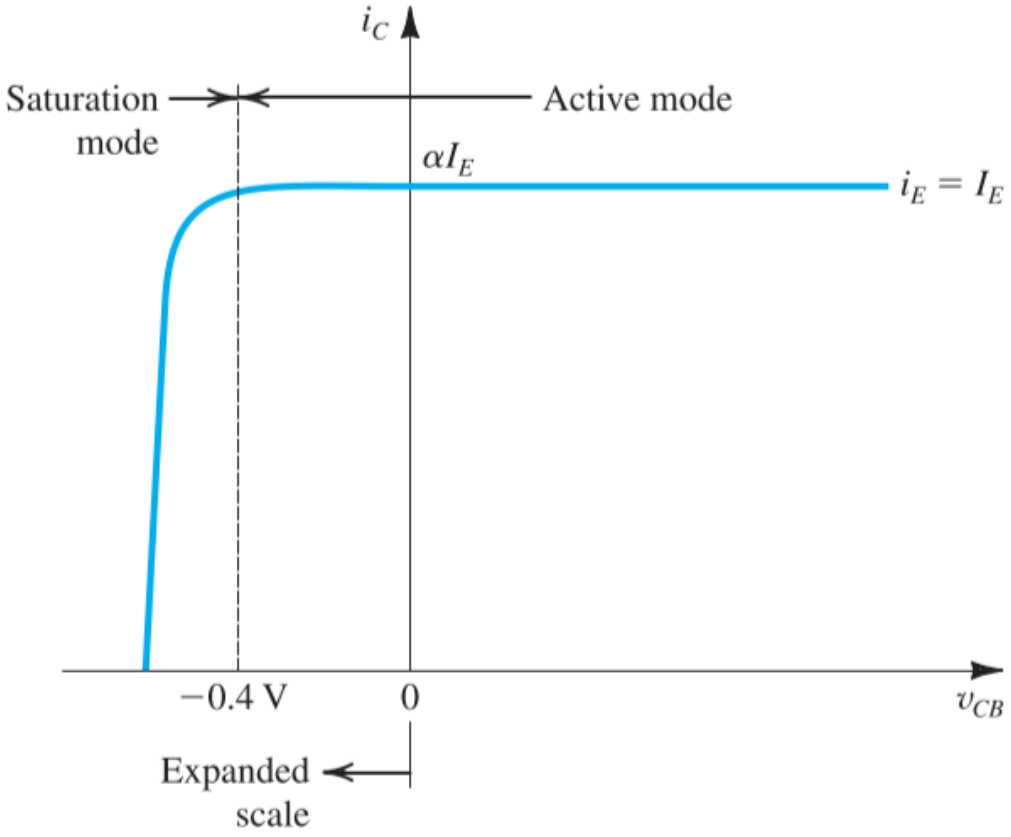
If we define

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

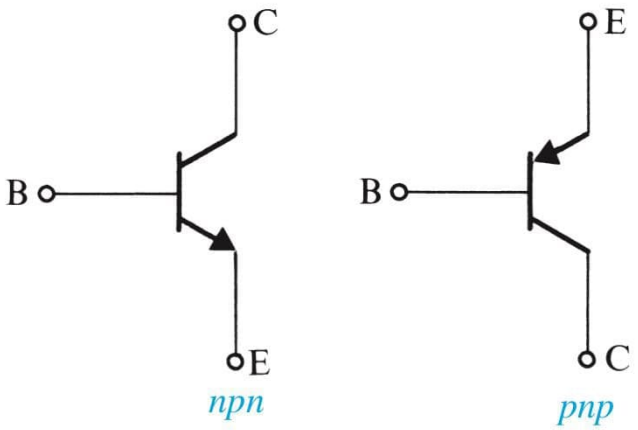
Then the current of the collector could be expressed as

$$i_C = \alpha i_E$$

- α: common-base current gain

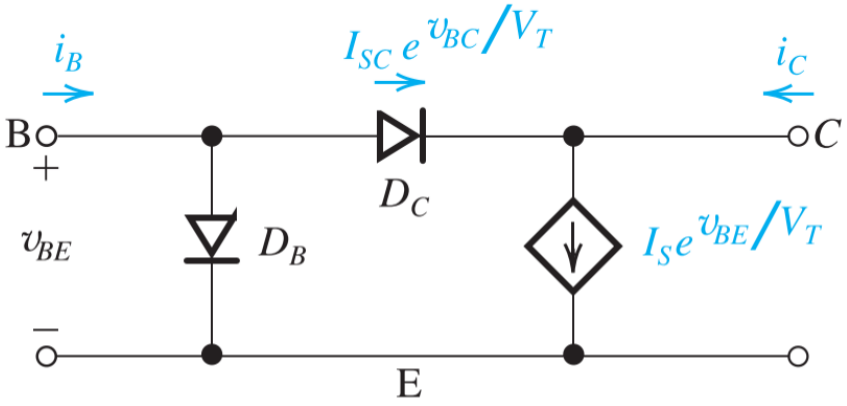


Large-signal Model



The models above could be applied for any positive value of v_{BE}, and thus these models are referred to as **large-signal models**

Operation in Saturation Mode



$$i_B = (I_s/\beta)e^{v_{BE}/V_T} + I_{sc}e^{v_{BC}/V_T}$$

$$i_C = I_s e^{v_{BE}/V_T} - I_{sc}e^{v_{BC}/V_T}$$

And the transistor parameter is defined as the ratio of the current on base to the collector

$$\beta_{\text{forced}} = \left.\frac{i_B}{i_C}\right|_{\text{saturation}} \leq \beta$$

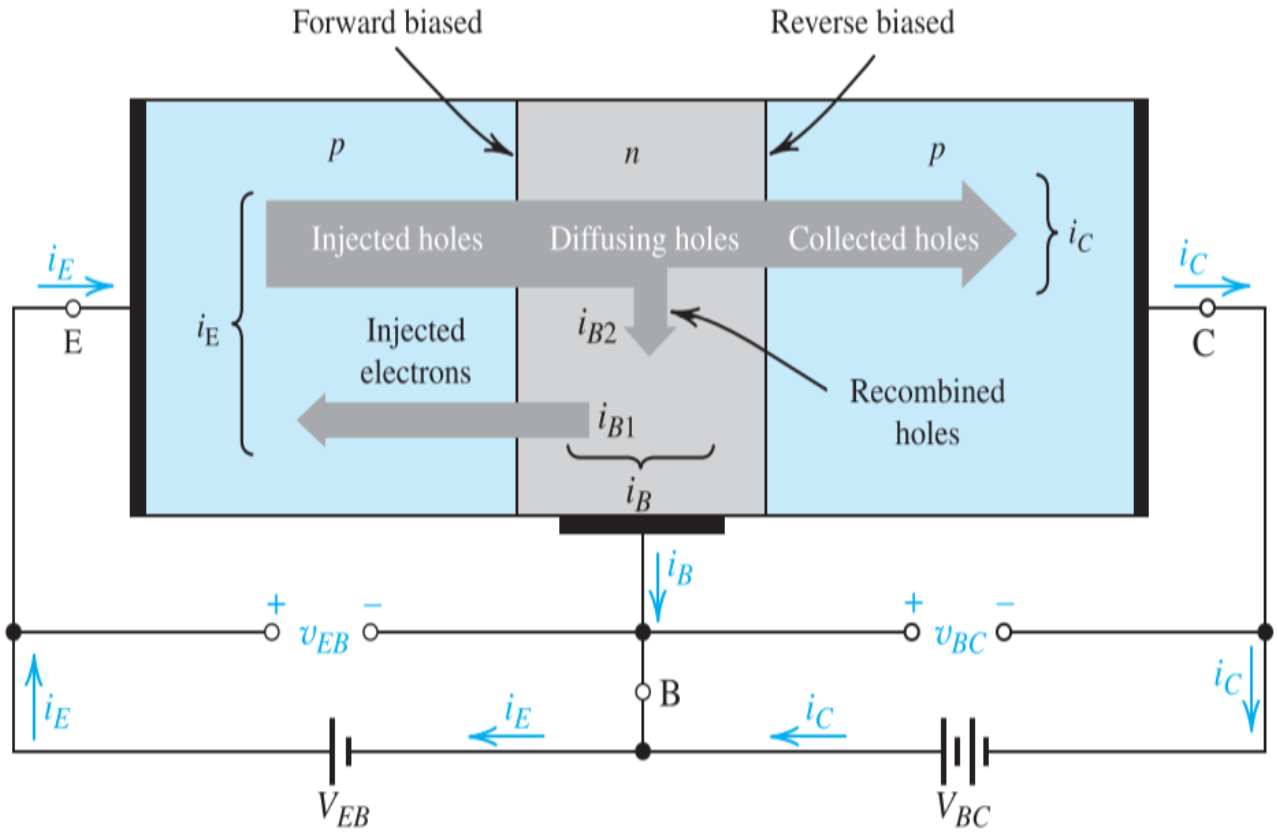
And we also have the saturation voltage

$$V_{CEsat} = V_{BE} - V_{BC}$$

And the saturation voltage at the edge of saturation is $V_{CEsat} = 0.3\ V$, while a transistor deep in saturation has $V_{CEsat} = 0.2\ V$

The pnp Transistor

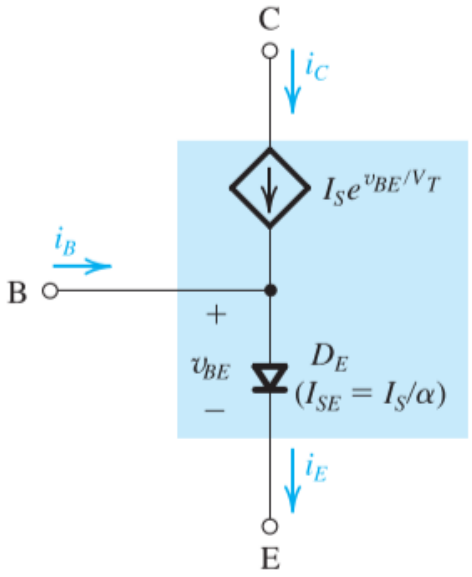
Operation in Active Mode



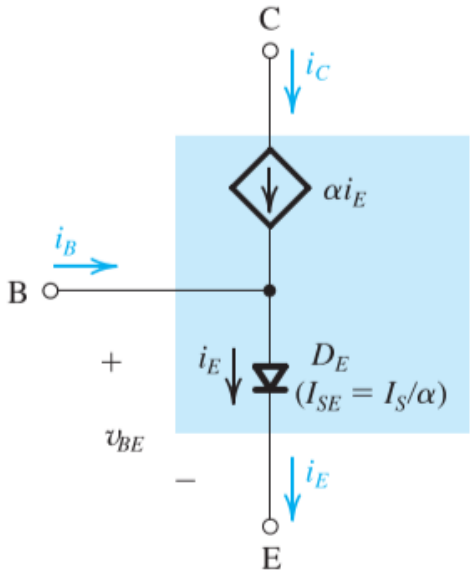
It can be easily seen that the current-voltage relationship of the *pnp* transistor will be identical to that of the *npn* transistor except that v_{BE} has to be replaced by v_{EB}

And the *pnp* transistor can operate in the saturation mode in a manner analogous to that described for the *npn* device

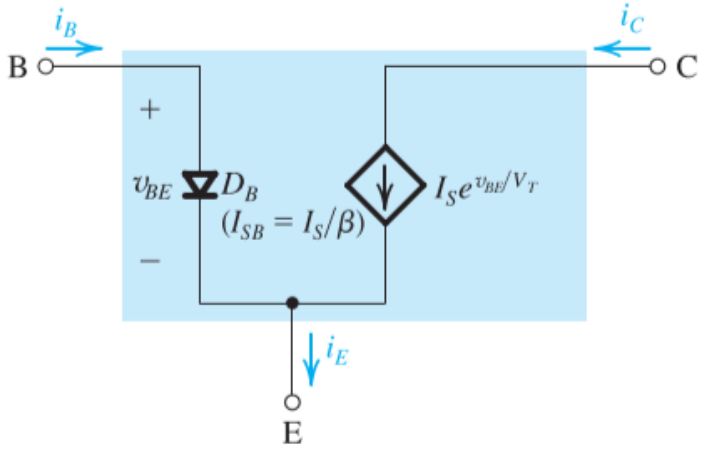
Large-signal Model



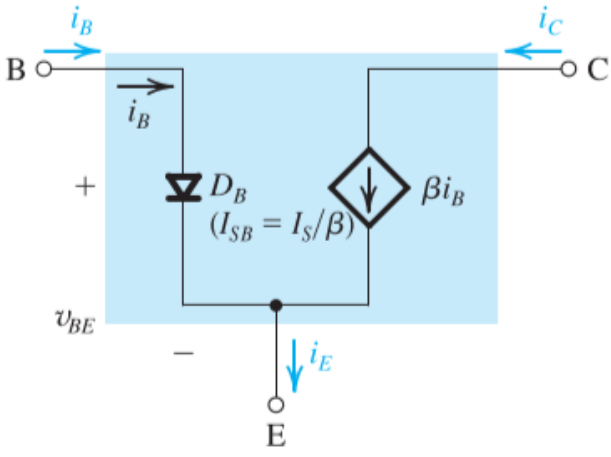
(a)



(b)

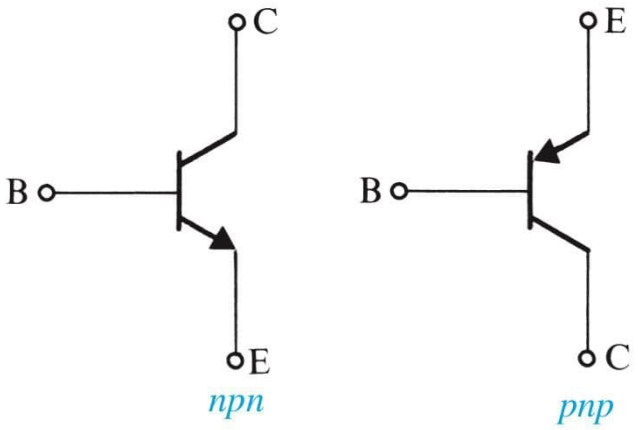


(c)

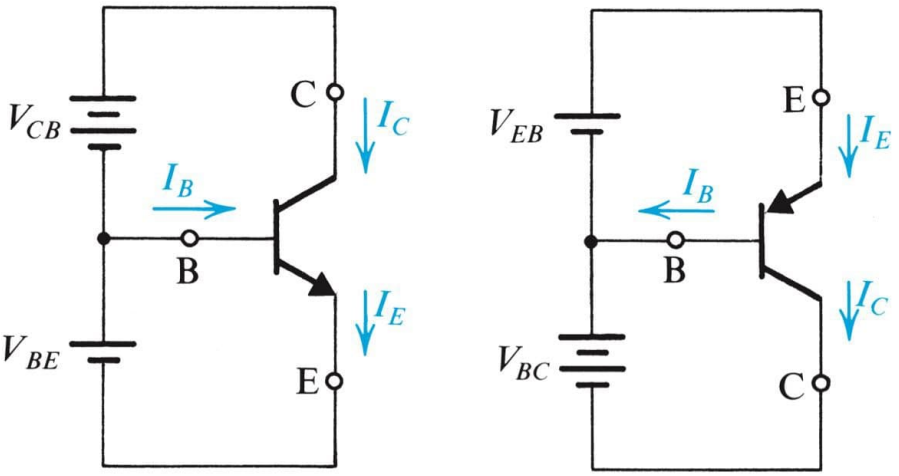


(d)

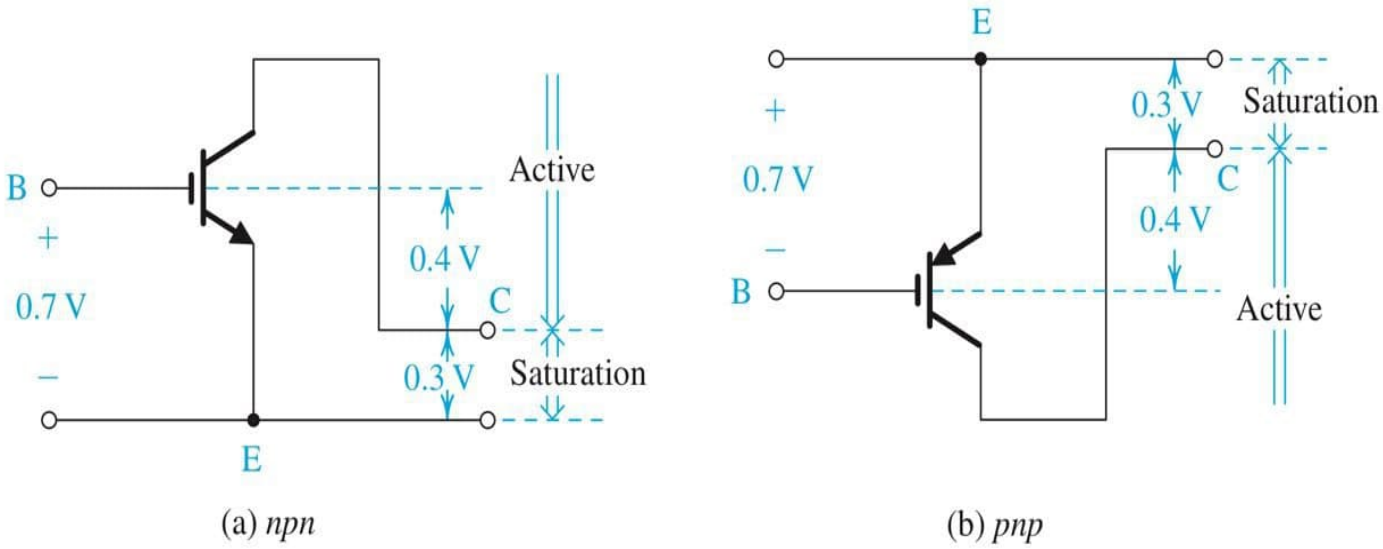
4-2 Current-Voltage Characteristics



The polarity of the device *npn* or *pnp* is indicated by the direction of the **arrowhead on the emitter**, which points in the direction of normal current flow in the emitter, also the forward direction of the base-emitter junction.



According to the concepts mentioned in the first part, we could find the voltage characteristics of the both kinds of transistors



$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

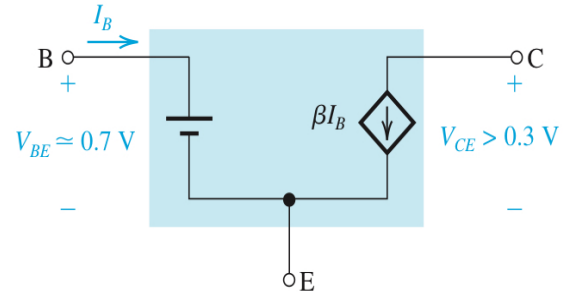
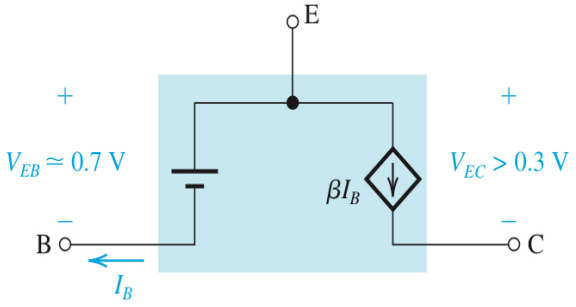
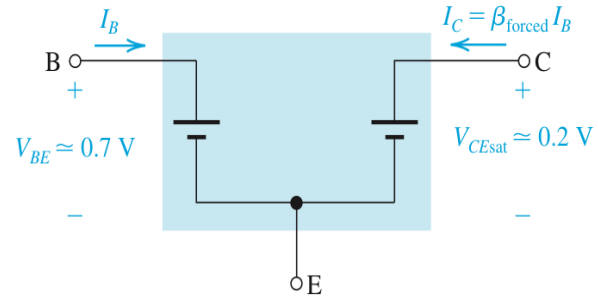
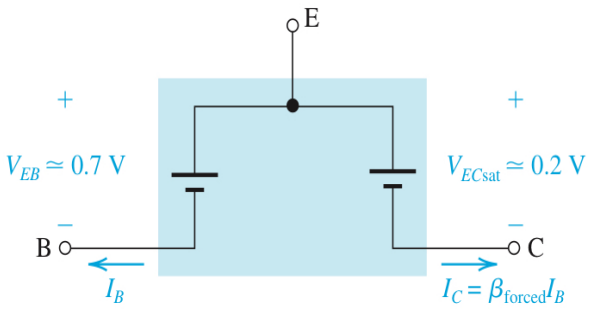
> $V_T = \frac{kT}{q} \approx 25\ mV$
> for *pnp* transistor, replace v_{BE} with v_{EB}

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\alpha = \frac{\beta}{\beta+1}$$

4-3 BJT Circuits at DC

Table 6.3 Simplified Models for the Operation of the BJT in DC Circuits

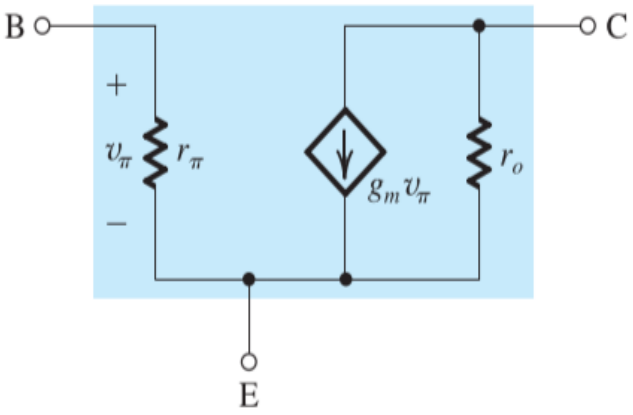
	npn	*pnp*
Active EBJ: Forward Biased CBJ: Reverse Biased		
Saturation EBJ: Forward Biased CBJ: Forward Biased		

4-4 Small Signal Analysis

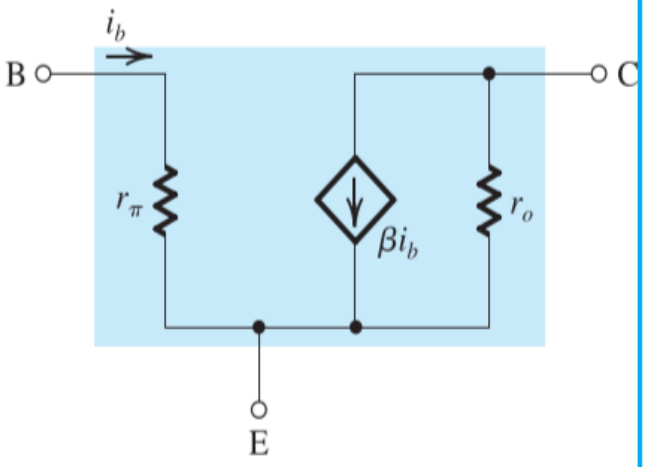
Table 7.3 Small-Signal Models of the BJT

Hybrid-π Model

■ $(g_m v_\pi)$ Version

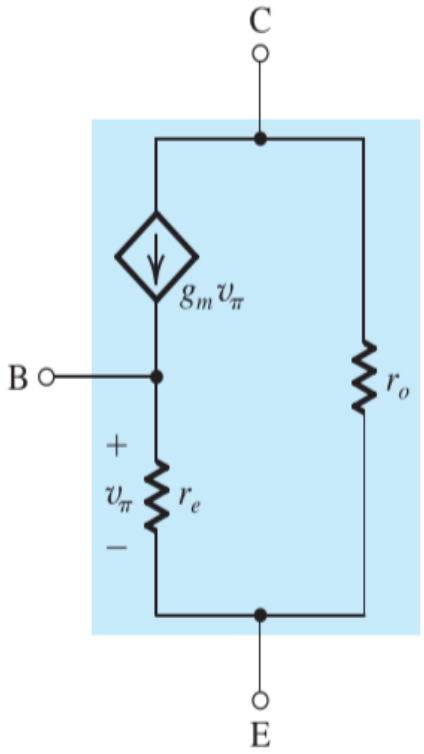


■ (βi_b) Version

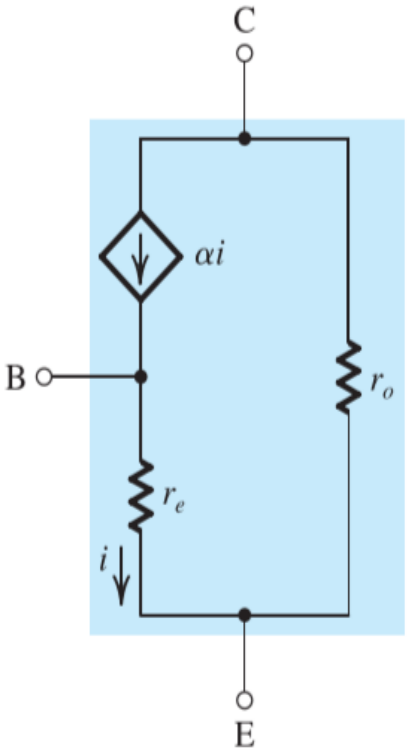


T Model

■ $(g_m v_\pi)$ Version



■ (αi) Version



Model Parameters in Terms of DC Bias Currents

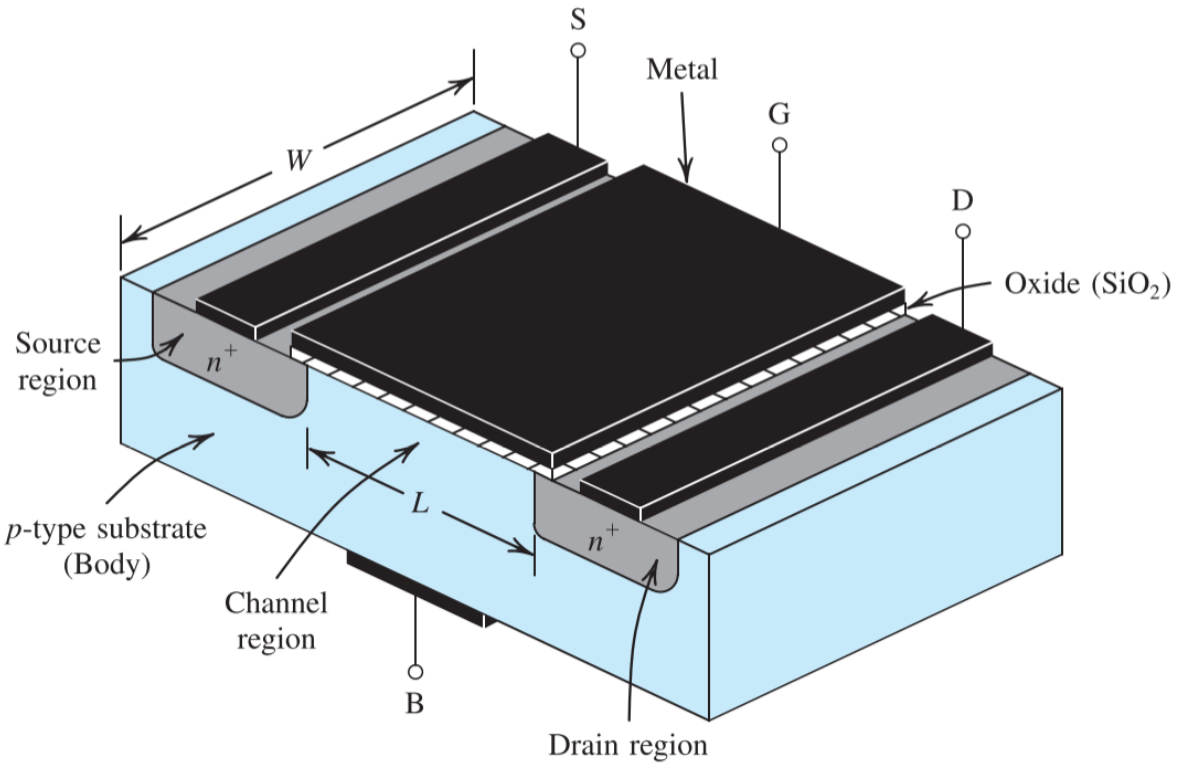
$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha \frac{V_T}{I_C} \qquad r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} \qquad r_o = \frac{|V_A|}{I_C}$$

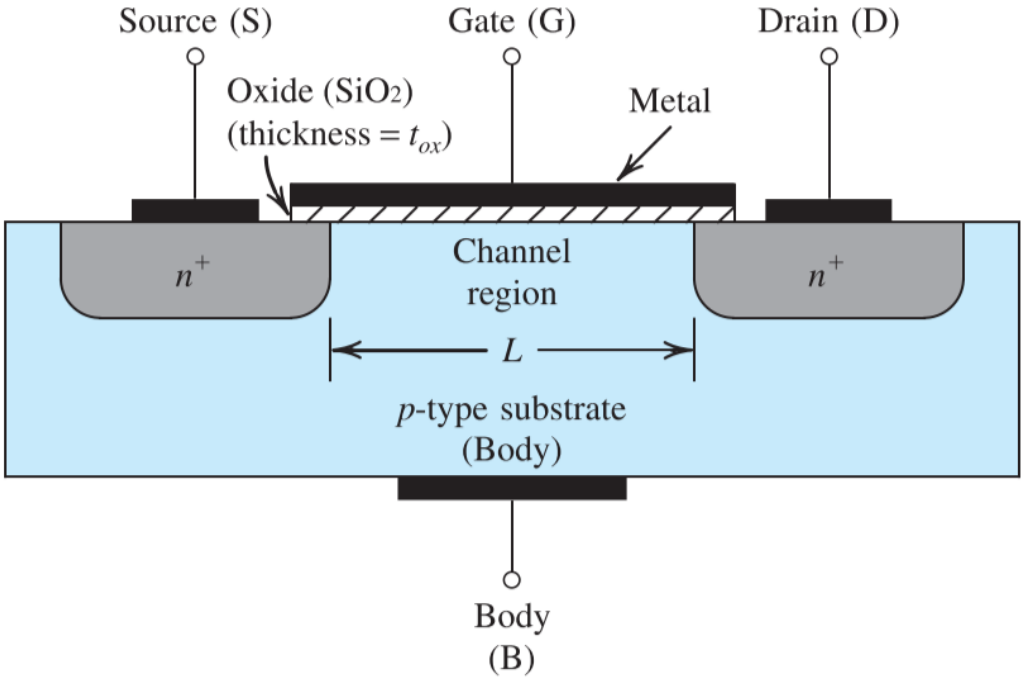
v_T	i_E i_C	i_B i_C	i_C
In Terms of g_m			
$r_e = \frac{\alpha}{g_m}$	$r_\pi = \frac{\beta}{g_m}$		
In Terms of r_e			
$g_m = \frac{\alpha}{r_e}$	$r_\pi = (\beta + 1) r_e$	$g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$	
Relationships between α and β			
$\beta = \frac{\alpha}{1 - \alpha}$	$\alpha = \frac{\beta}{\beta + 1}$	$\beta + 1 = \frac{1}{1 - \alpha}$	

Chapter 5 MOS Field-Effect Transistors

5-1 Device Structure and Physical Operation

Device Structure



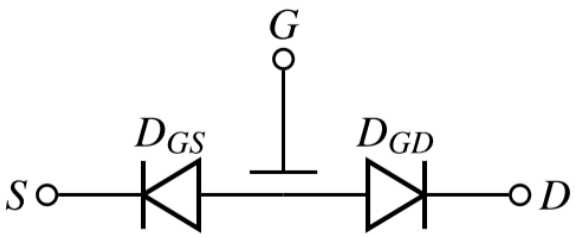


The figures above show the physical structure of the n-channel enhancement-type MOSFET

- two heavily doped n-type regions: **source** and **drain** regions
- thin layer of silicon dioxide of thickness t_{ox}: covering area between source and drain regions
- metal is deposited on the top of oxide: form the **gate electrode** of the device
- metal is also deposited on source, drain and **body** regions

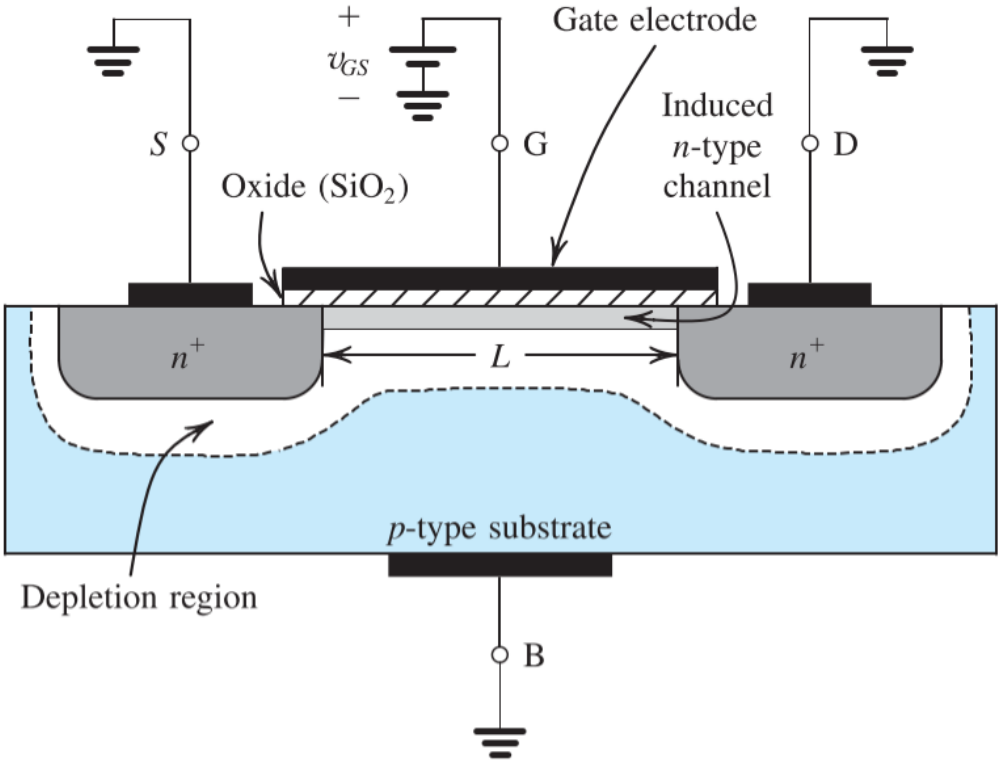
Physical Operations

Zero Gate Voltage



With zero voltage applied to the two back-to-back diodes exist in series between drain and source, which prevent the current conduction from source to drain as the voltage v_{DS} is applied

Creating a Channel for Current Flow



Apply a positive voltage v_{GS} between the **gate** to **source**

- free holes are **repelled** from the region of the substrate under the gate
- the positive voltage **attracted** electron from source and drain region to the channel region, which created an n-type channel
- the induced n region forms a **channel** for current flow

Since the flow have been established

- the gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric
- the electric field thus develops in the vertical direction
- the field control the amount of charge in the channel also the conductivity

> **threshold voltage** V_t: to accumulate enough electrons to the channel, v_{GS} must exceed threshold voltage
> **override voltage** V_{OV}: the excess of v_{GS} over V_t is termed as **effective voltage** $V_{OV} = v_{GS} - V_t$

The magnitude of the electron charge in the channel

$$\|Q\| = C_{ox}(WL)v_{OV}$$

- C_{ox}: **oxide capacitance**

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

- ϵ_{ox}: the permittivity of the silicon dioxide

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.45 \times 10^{-11}\ F/m$$

- t_{ox}: oxide thickness

Applying a Small Voltage

Now apply a **small positive voltage** v_{DS} between drain and source

The current on the drain region is

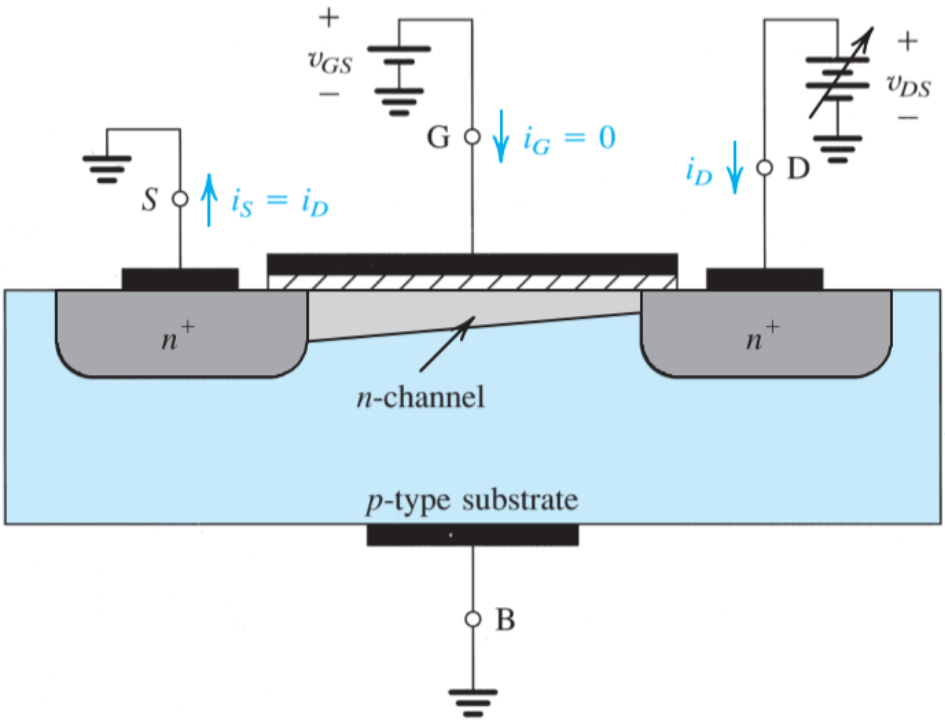
$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)v_{OV}\right]v_{DS}$$

- μ_n: the mobility of the electrons
- W/L: aspect ratio

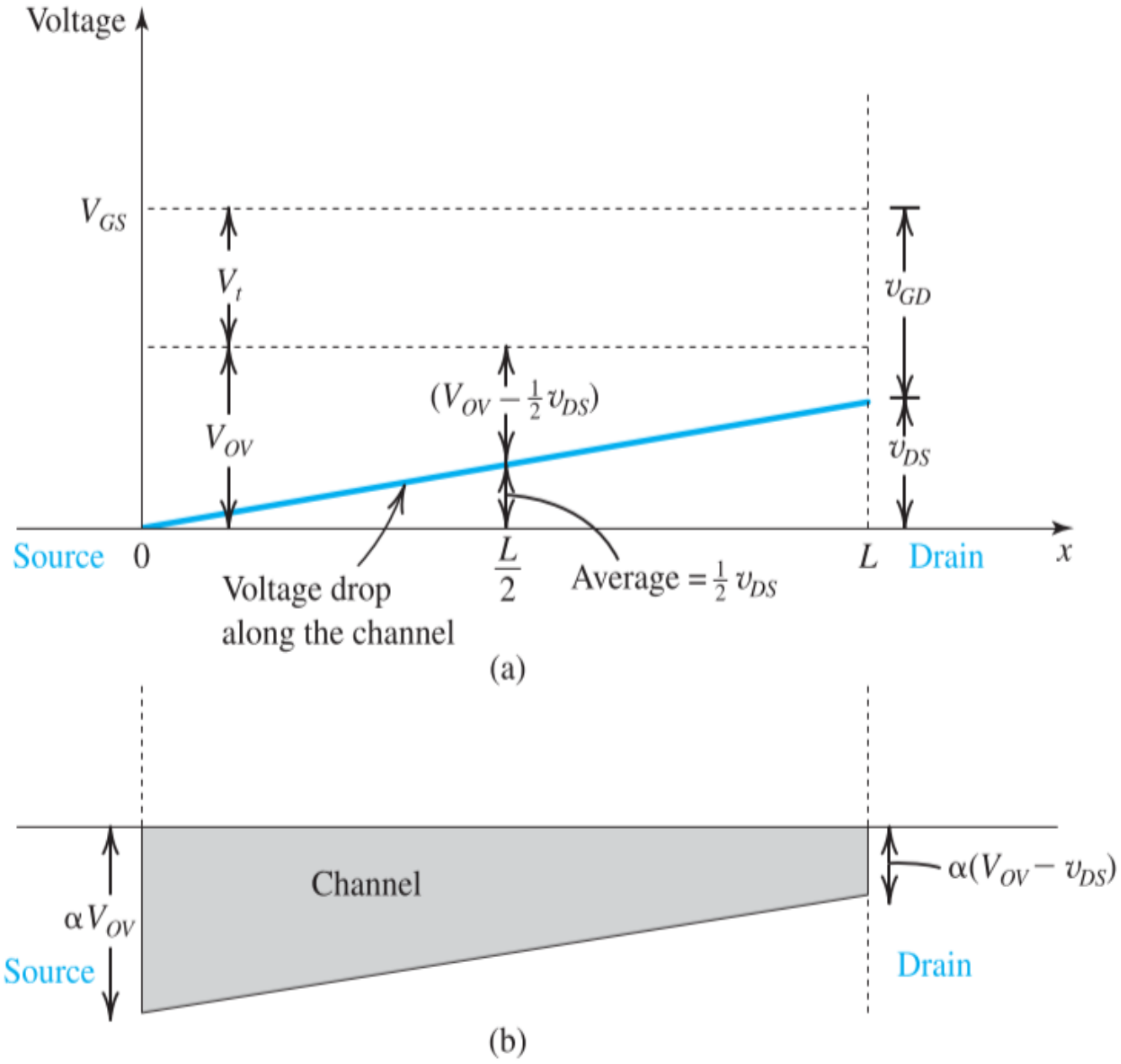
Since the other factor are determined in manufacturing, we could denote the factor as

- $k_n = \mu_n C'_{ox}$: the factor termed process transconductance parameter
- $k_n = k'_n(W/L)$: MOSFET transconductance parameter

Increase Voltage on Drain



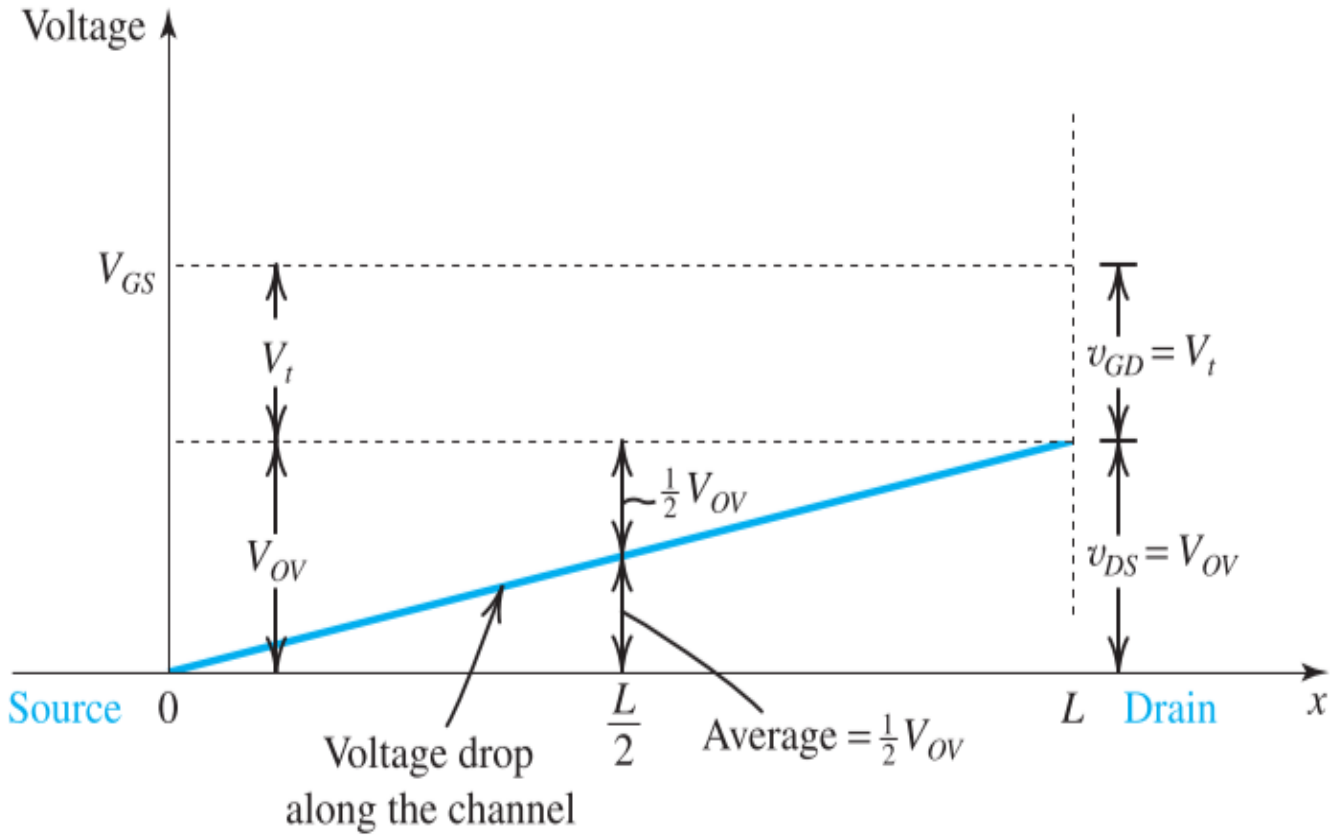
As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. The relationship between i_D and v_{DS} could be derived according to the figure.



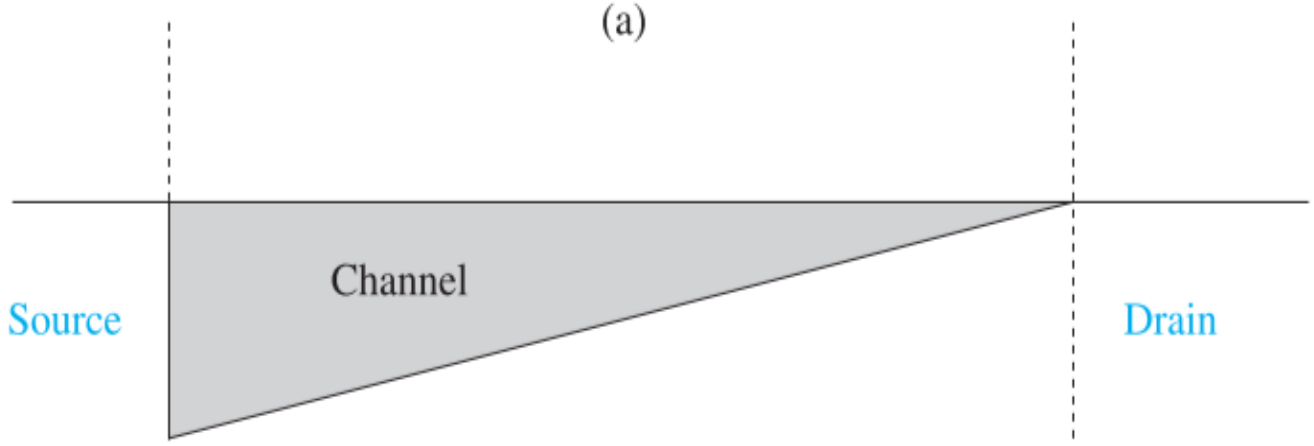
$$
\begin{aligned}
i_D &= k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS} \\
&= k_n'\left(\frac{W}{L}\right)\left(V_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right) \\
&= k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]
\end{aligned}
$$

Current Saturation

Increasing v_{DS} over V_{OV}, the current through the channel remains constant at the value reaches for $v_{DS} = V_{OV}$. The drain current thus saturates.



(a)



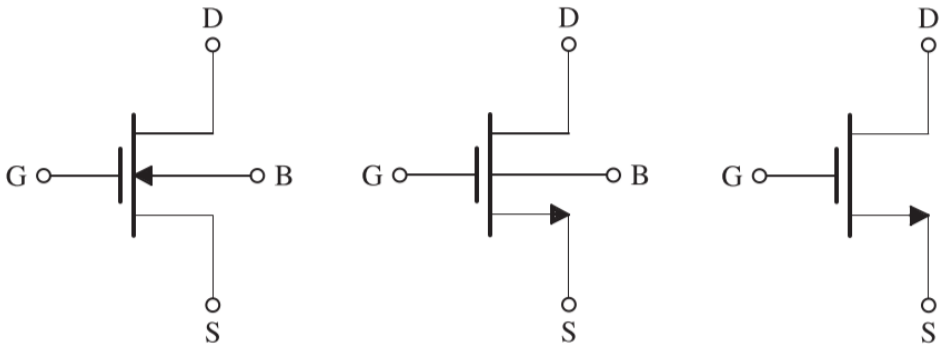
(b)

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

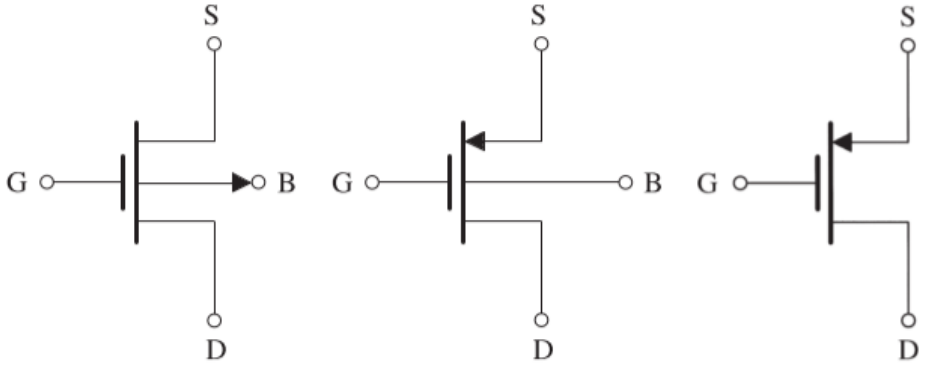
$$= \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

5-2 Current-Voltage Characteristic

Circuit Symbol



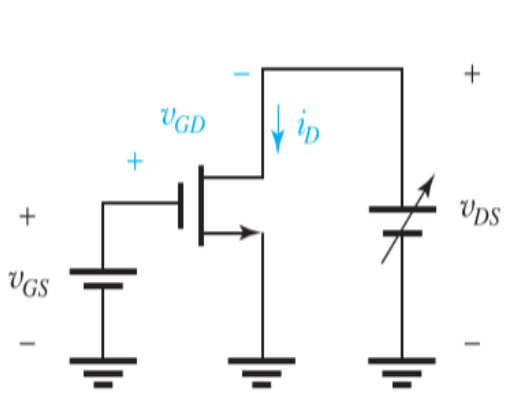
The figure above show the circuit symbol for the n-channel MOSFET

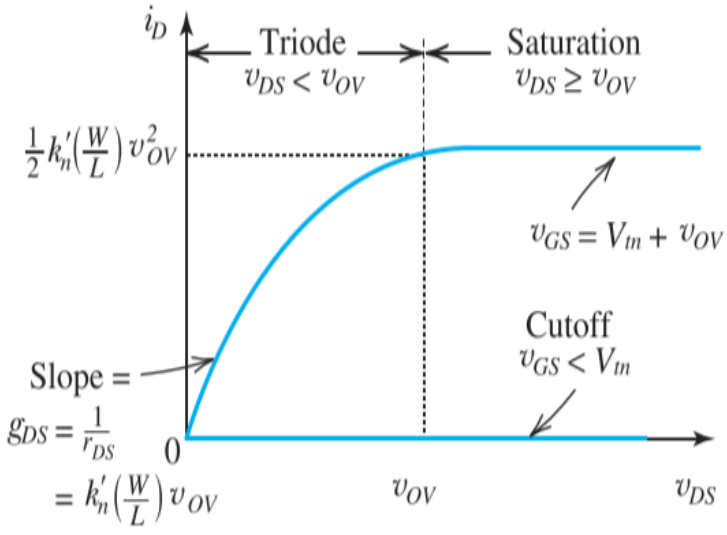


The figure above show the circuit symbol for the p-channel MOSFET

Current-Voltage Relationship on Drain

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

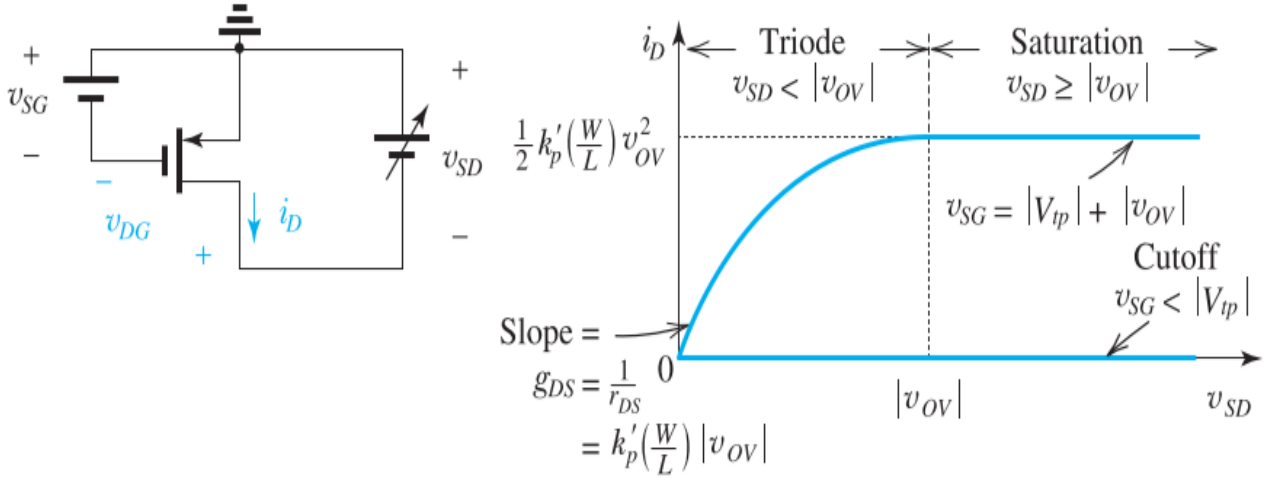
Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor



- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

5-3 Small Signal Analysis

Table 7.2 Small-Signal Models of the MOSFET

Small-Signal Parameters

NMOS transistors

- **Transconductance:**

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

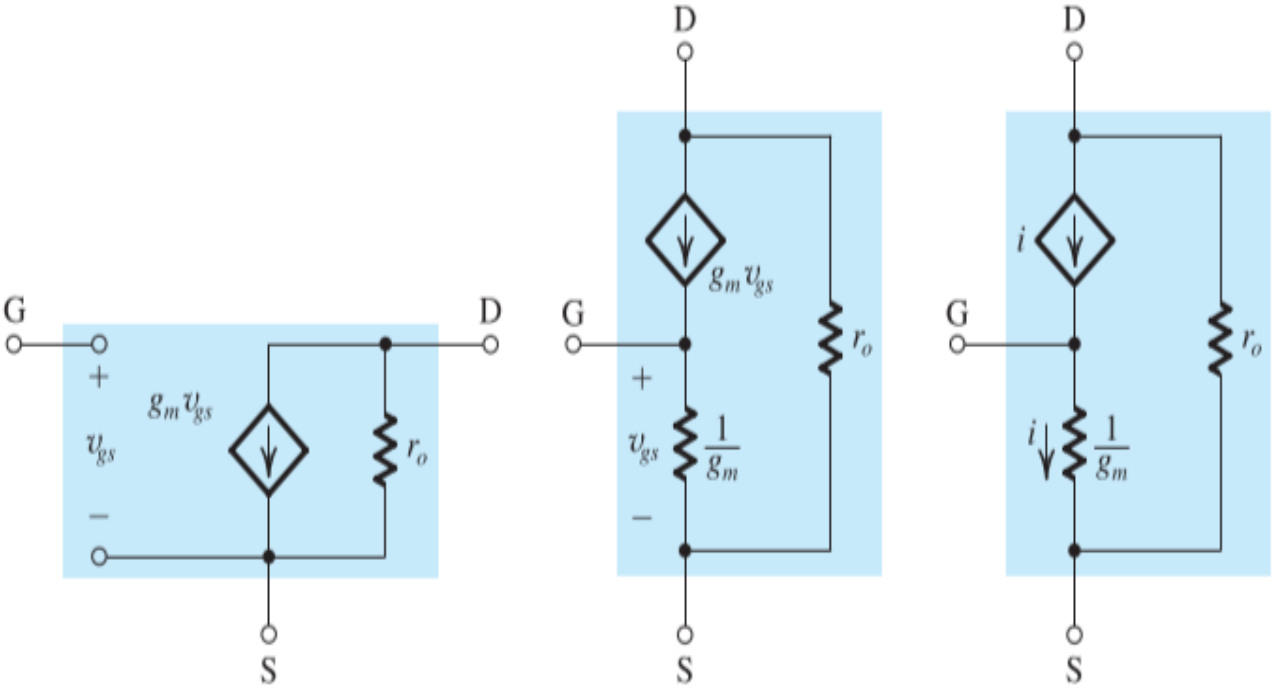
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS *except* using $|V_{OV}|$, $|V_A|$, $|\lambda|$ and replacing μ_n with μ_p.

Small-Signal, Equivalent-Circuit Models



Hybrid-π model T models