

**Project: I**

**Hardware Design Methodologies for ASICs  
and FPGA**

by:  
Hanuman Sagar Bathula

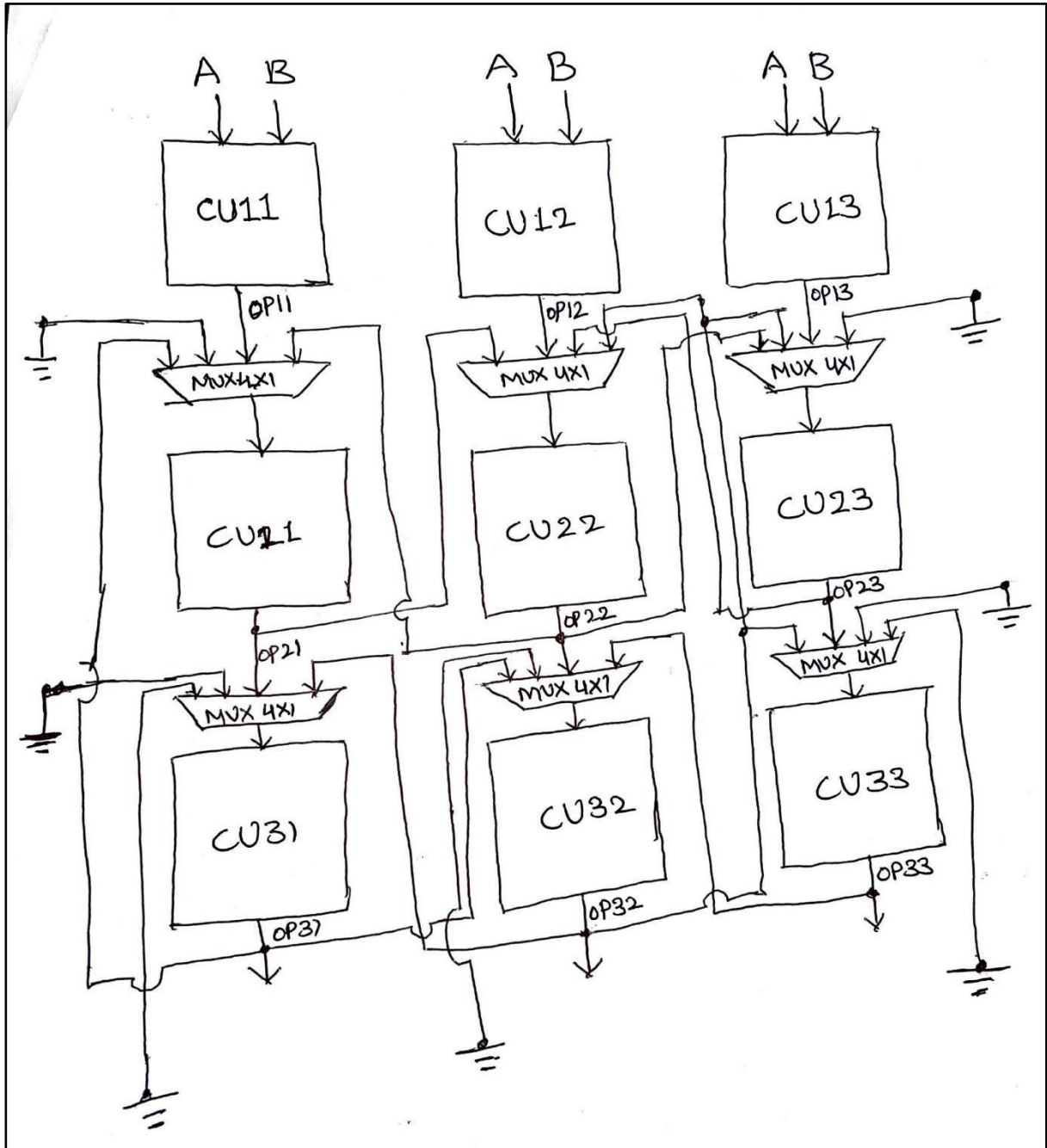
Under The Guidance of Instructor:  
Dr. Gayatri Mehta

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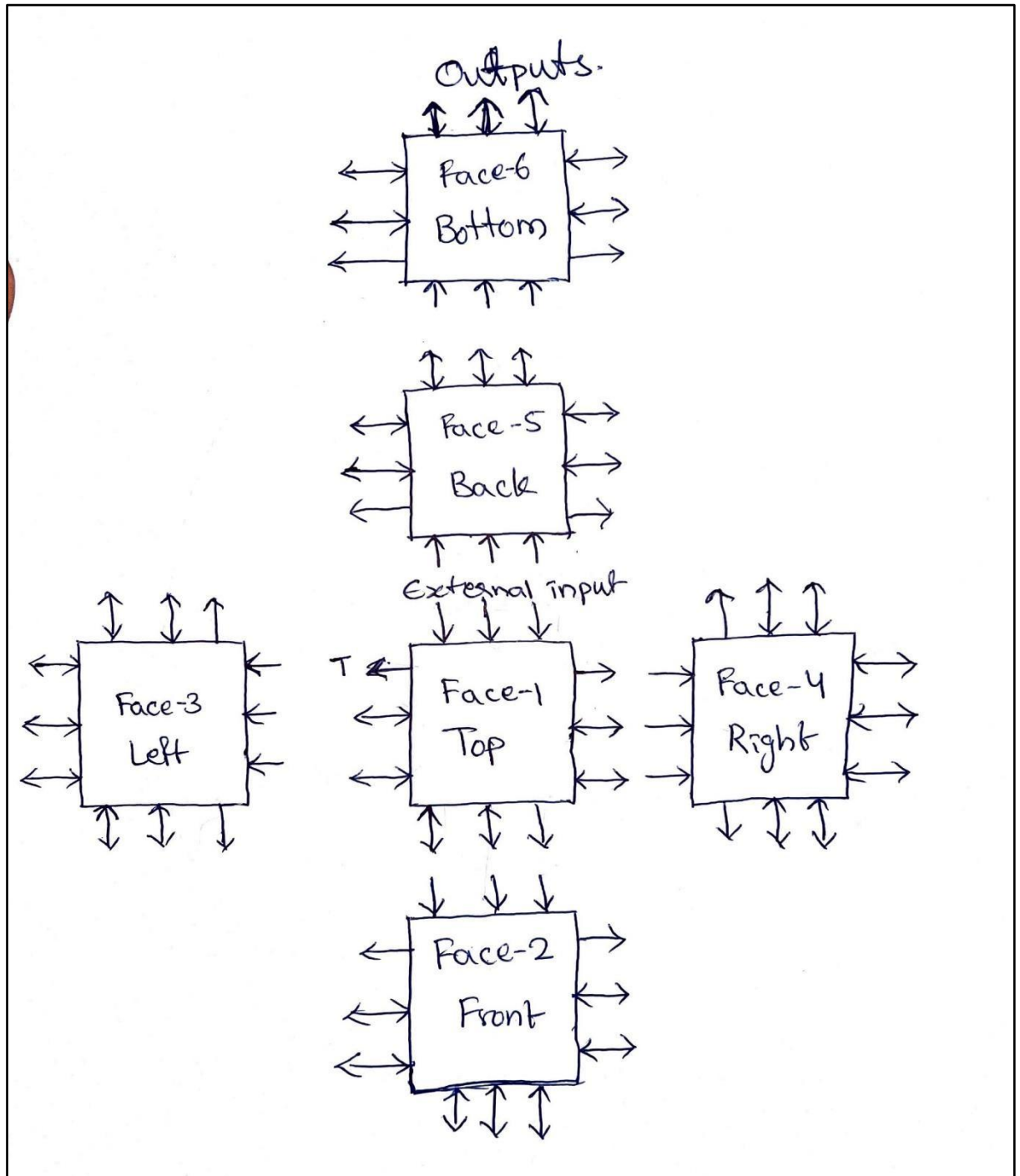
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## Block Diagrams:

Block Diagram for the Face Module:



The inputs grounded for the multiplexers in the above figure are connected to the ALUs on the adjacent sides.



Block Diagram

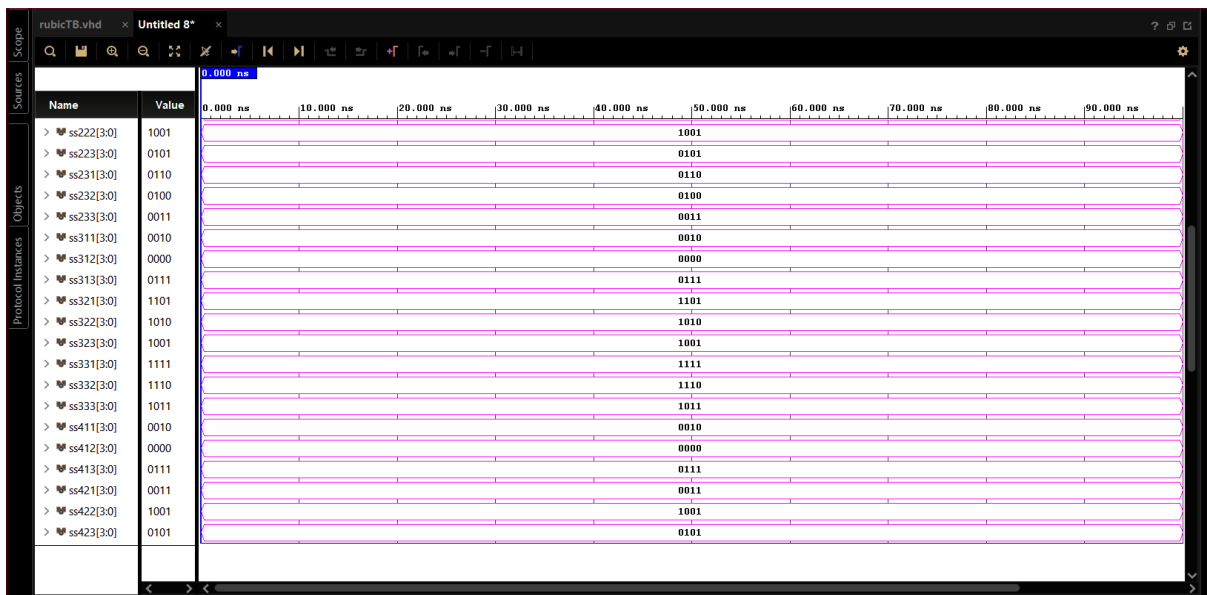
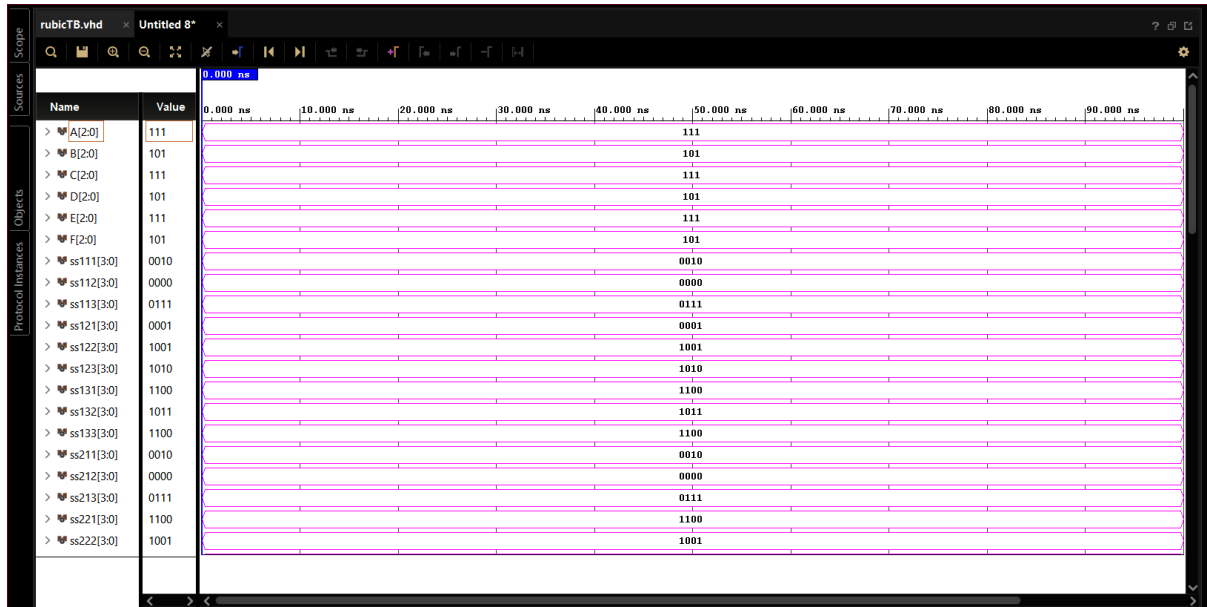
Outputs of CU s from all the edges of face 1 are given to the corresponding CUs of the adjacent face, as shown in the figure above.

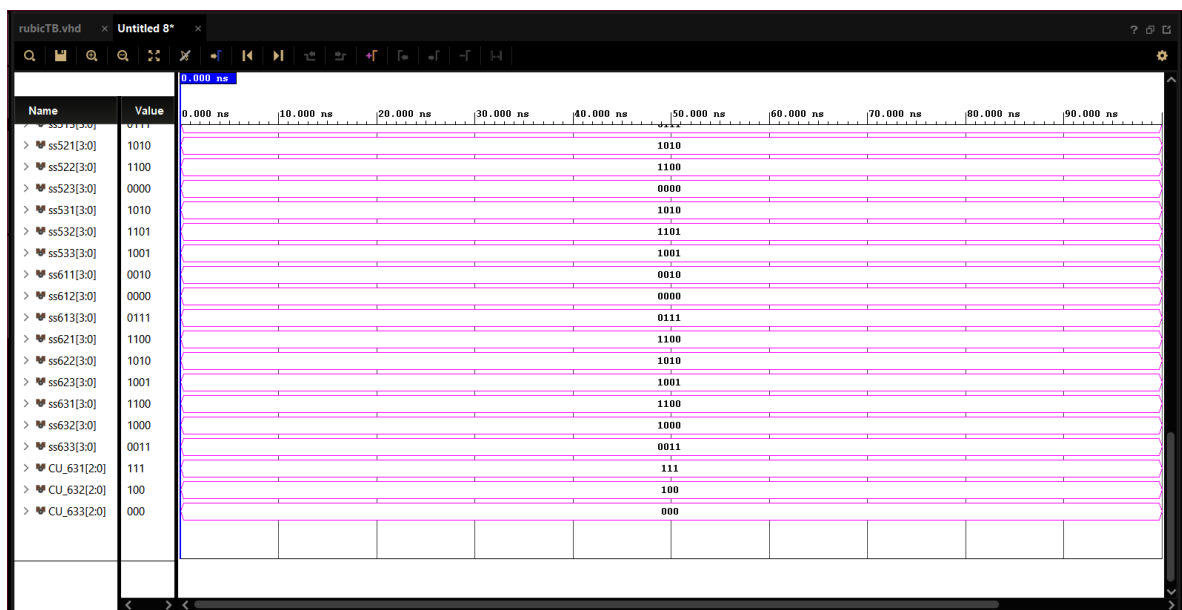
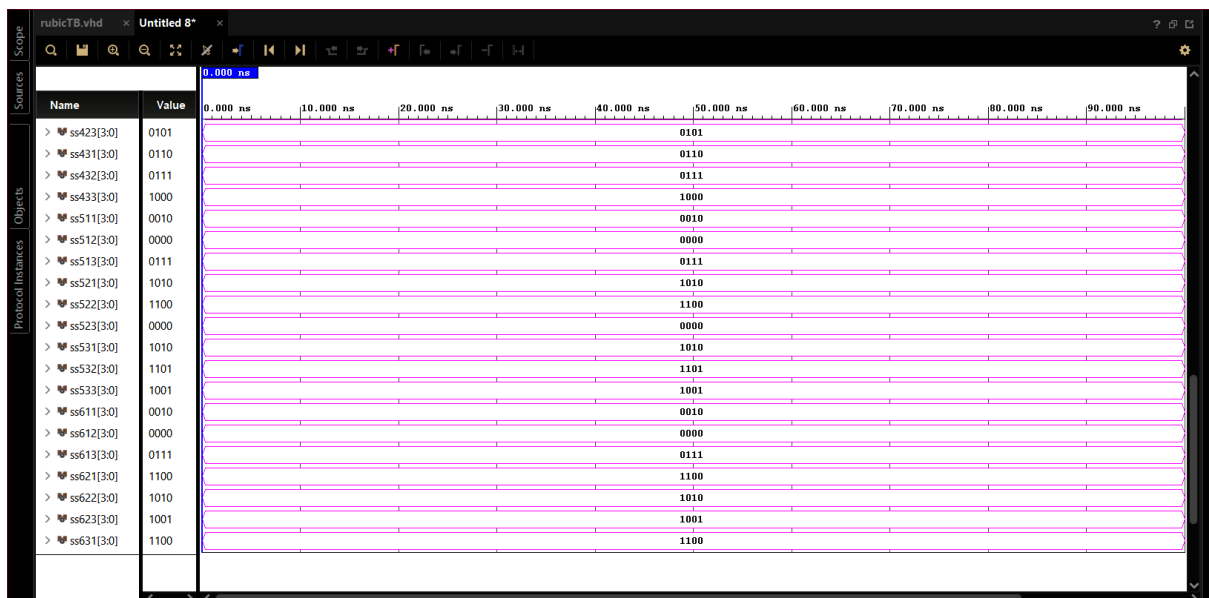
## **Design Explanations:**

- We built face by repeating a CU nine times and the Cube by repeating that face six times.
- Our design is bi- directional, implemented using 4:1 multiplexers
- Designed in such a way that it is possible to select the inputs from any adjacent CU, for second and third rows of CU's
- If there is an overflow for a CU, then three LSB bits are taken as output.
- For shift operations, of the two inputs the first input which is 'A' in our case is shifted with input 'B' times.
- The two inputs of a CU can be passed with the use of two separate select lines. i.e., given as if they are separate operations.

# Results:

## Waveform for Test Case-1:

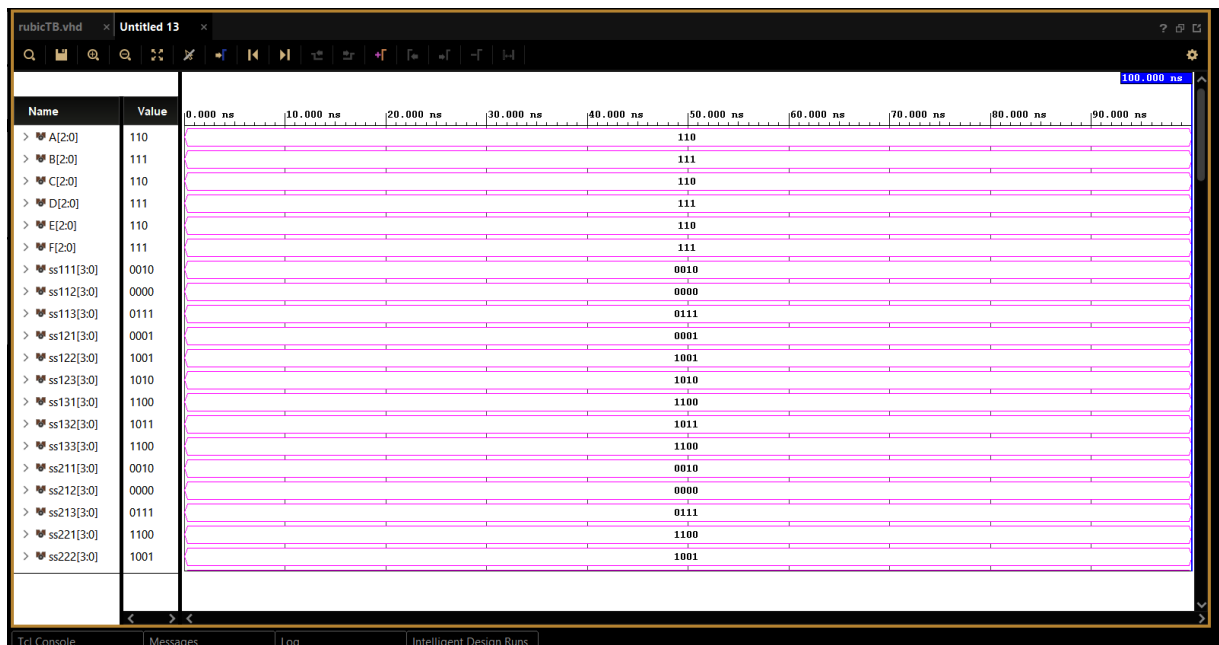




**Table for Test Case 2:**

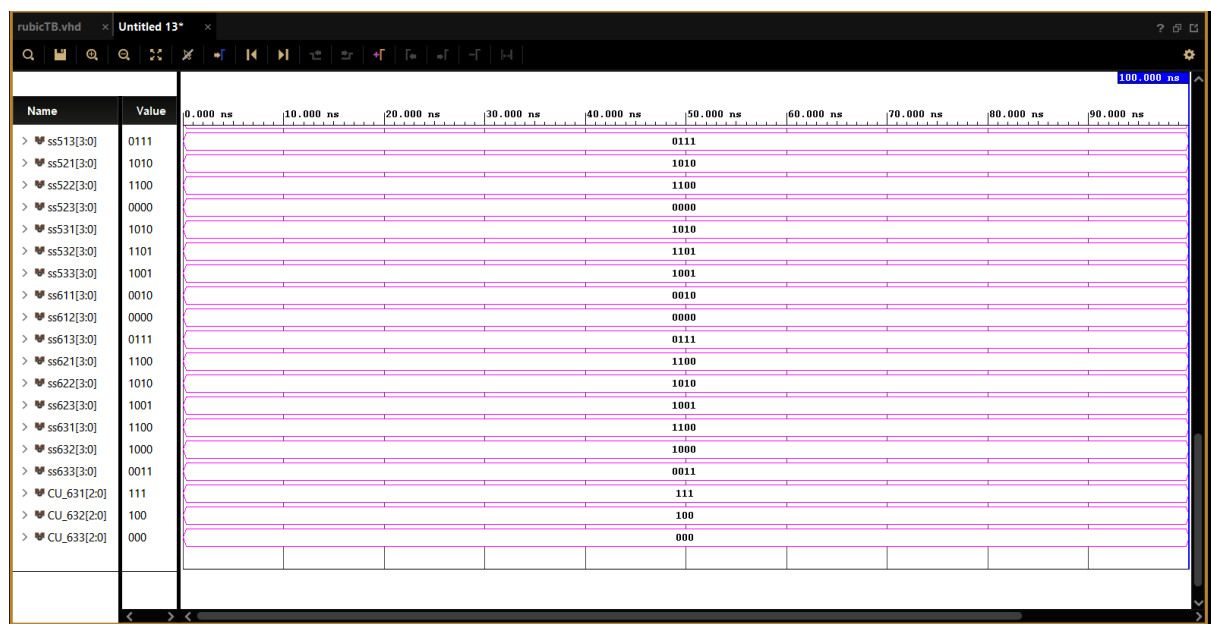
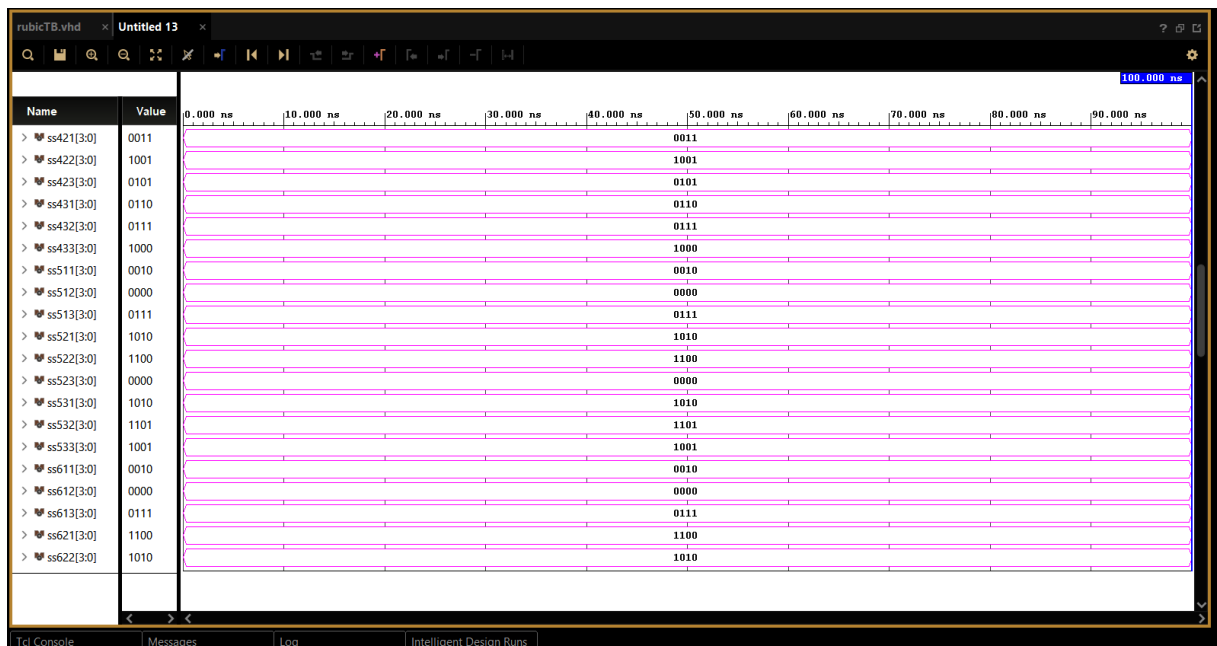
S.No	Both Inputs		Origin of Inputs	CU Operation	Final Output
	A	B			
1	111	101	External Inputs	MUL	011
2	010	010	CU111	RSL	011
3	000	000	CU513	ADD	110
4	111	111	CU523	NAND	001
5	000	000	CU533	RSL	010
6	111	111	CU613	NAND	101
7	001	001	CU623	LSL	000

**Waveform for Test Case-2:**



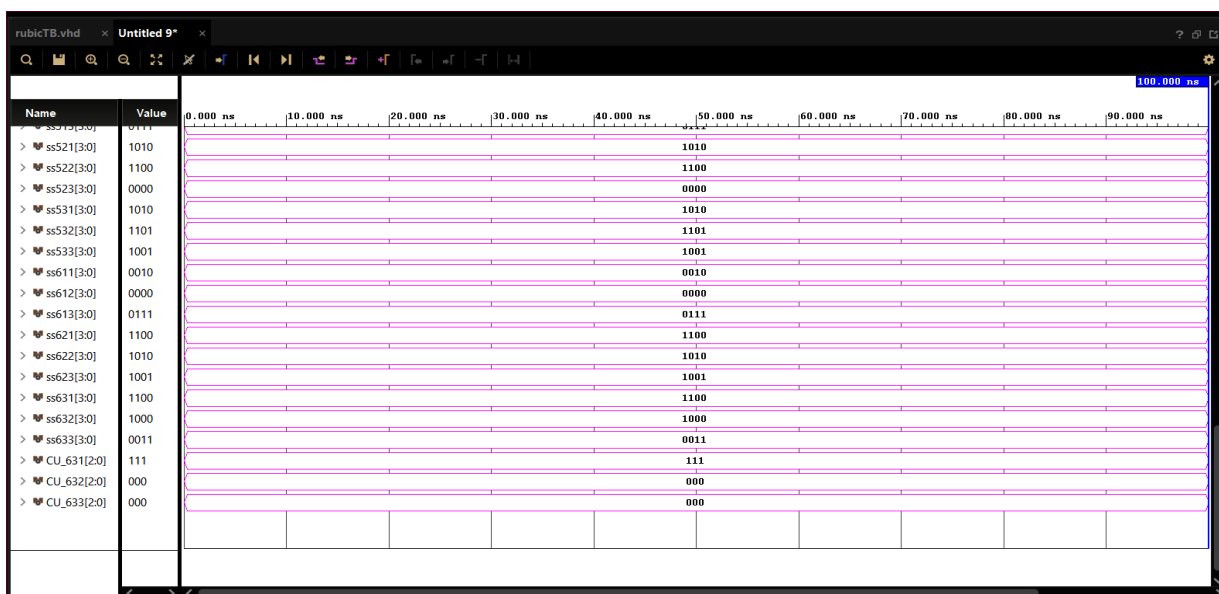
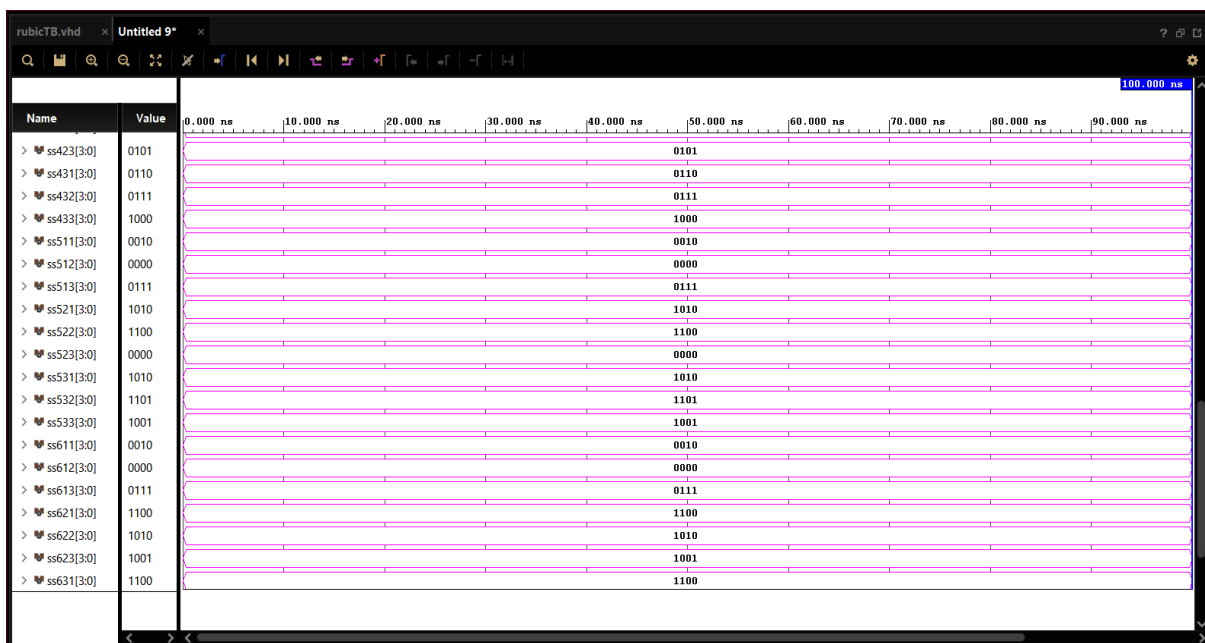






## Waveform for Test Case-3:

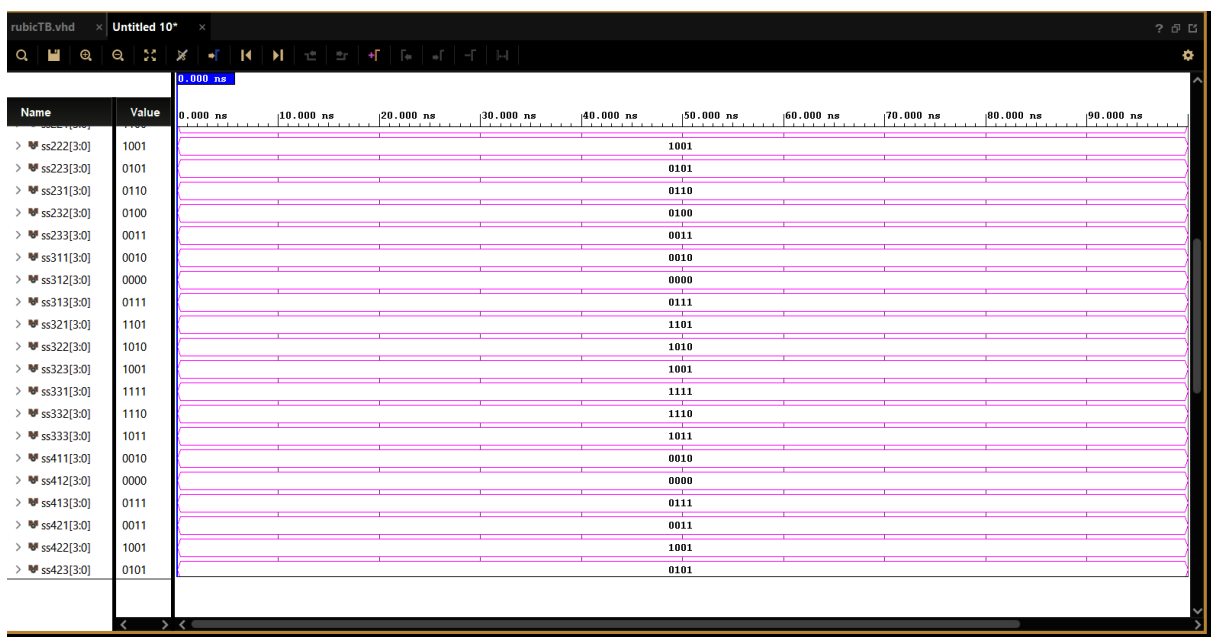
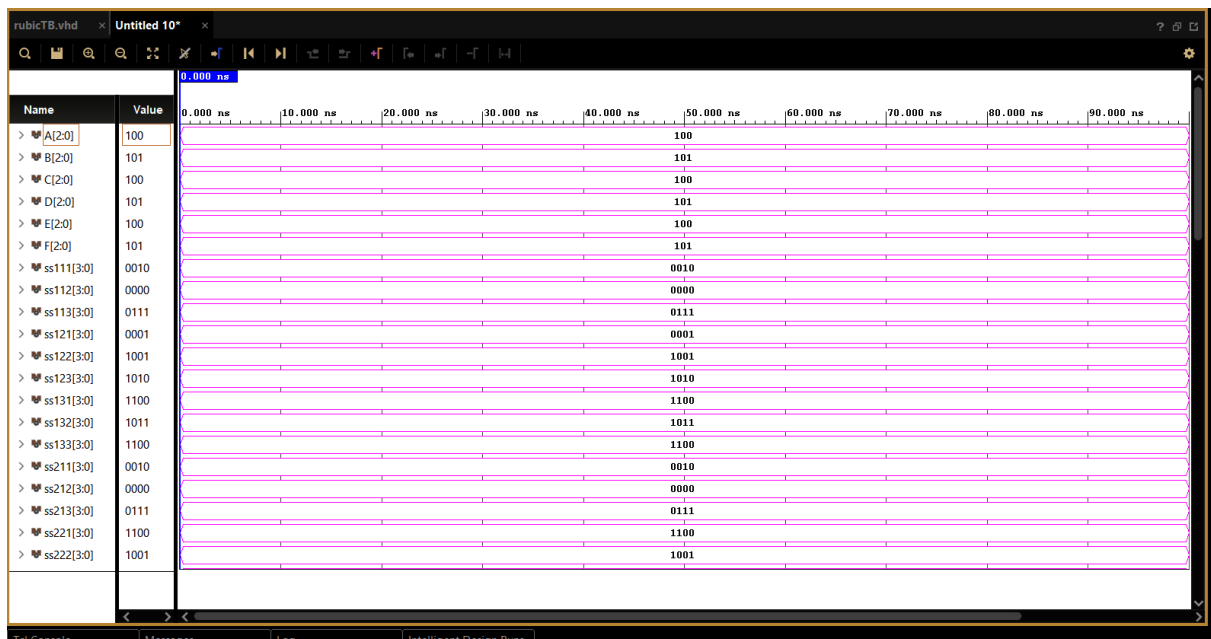


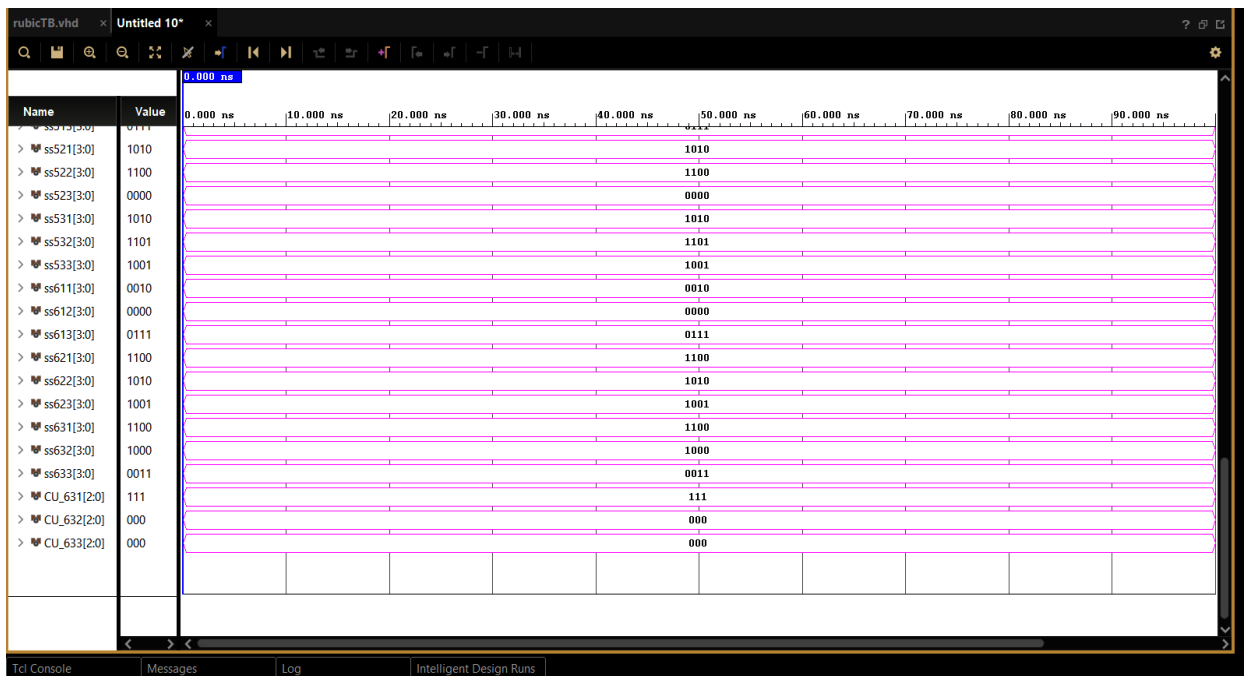
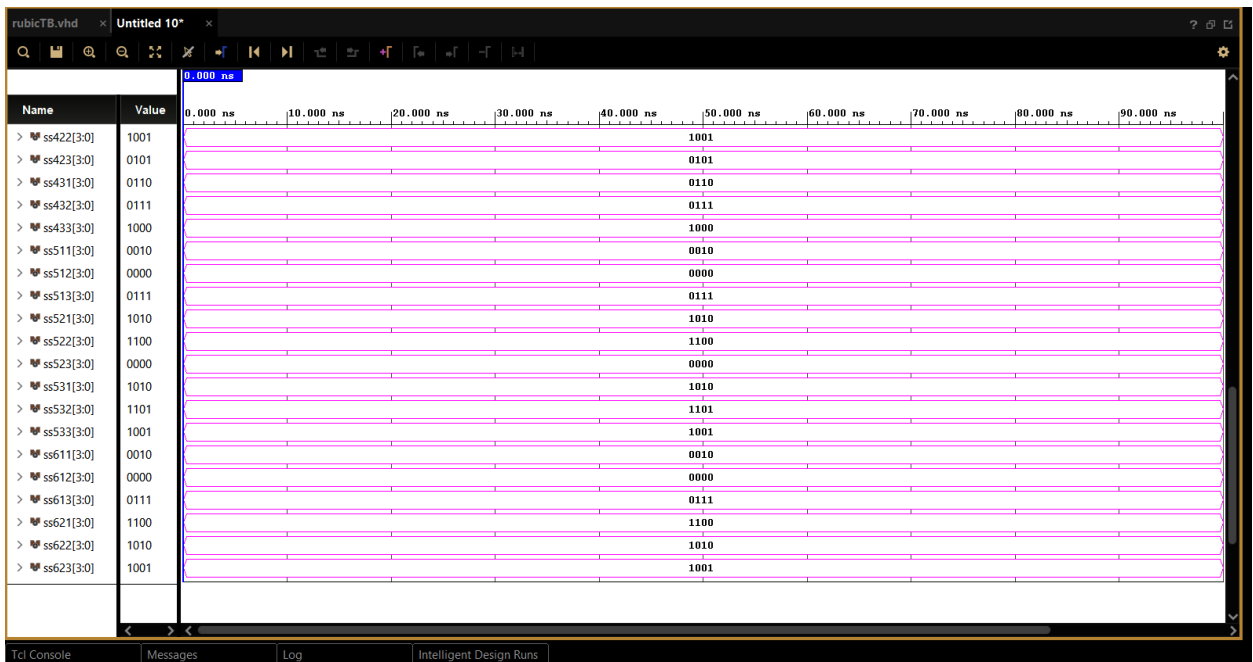


**Table for Test Case 4:**

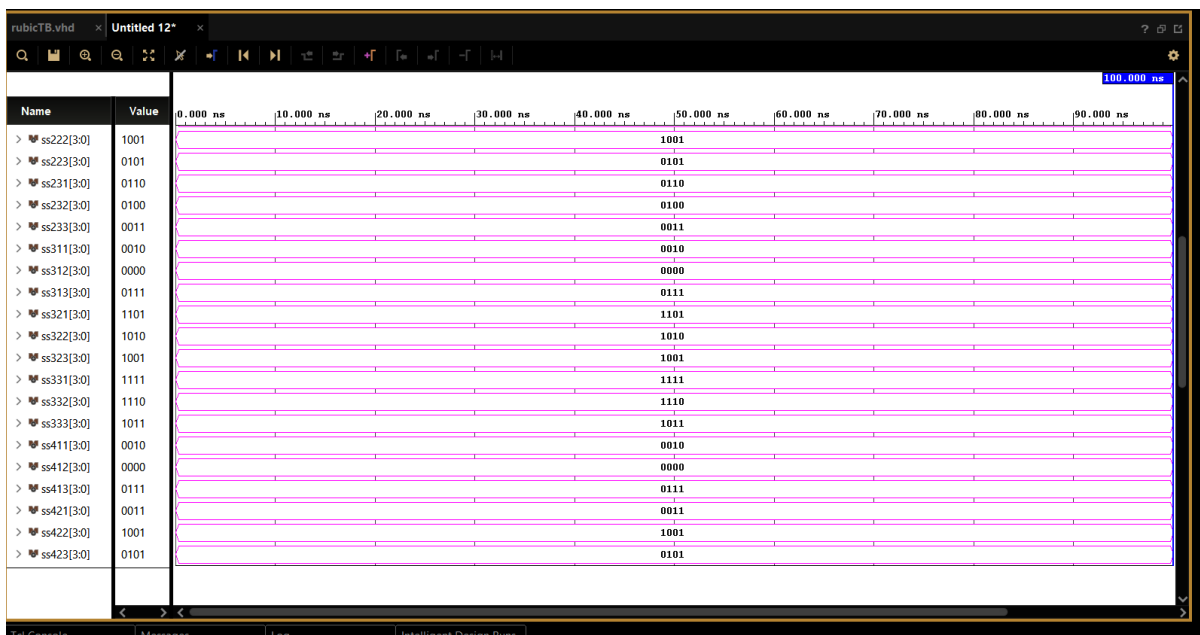
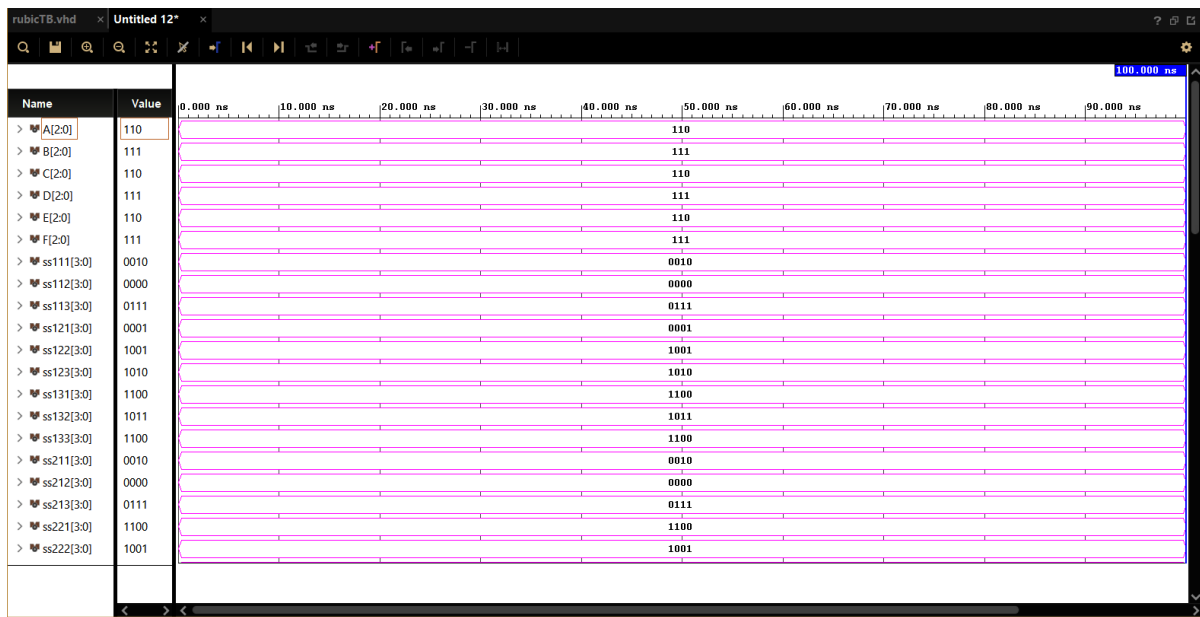
S.No	Both Inputs		Origin of Inputs	CU Operation	Final Output
	A	B			
1	110	111	External Inputs	MUL	010
2	010	010	CU111	SUB	000
3	000	000	CU121	XNOR	111
4	111	111	CU131	XOR	000
5	000	000	CU132	XNOR	111
6	111	111	CU133	MUL	001
7	001	001	CU411	LSL	010
8	010	010	CU421	NAND	101
9	101	101	CU422	SLA	111
10	111	111	CU423	NOR	000
11	000	000	CU521	XNOR	111
12	111	111	CU522	ADD	110
13	110	110	CU523	NAND	001
14	001	001	CU533	RSL	010
15	010	010	CU613	NAND	101
16	101	101	CU623	LSL	000

## Waveform for Test Case-4:

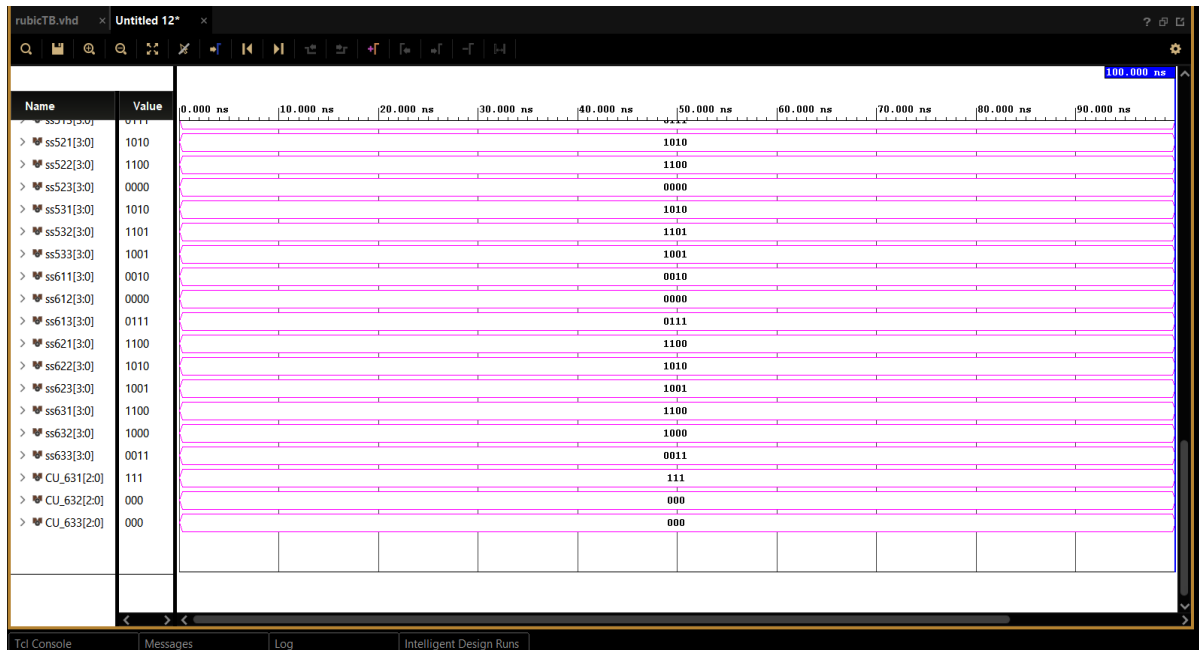
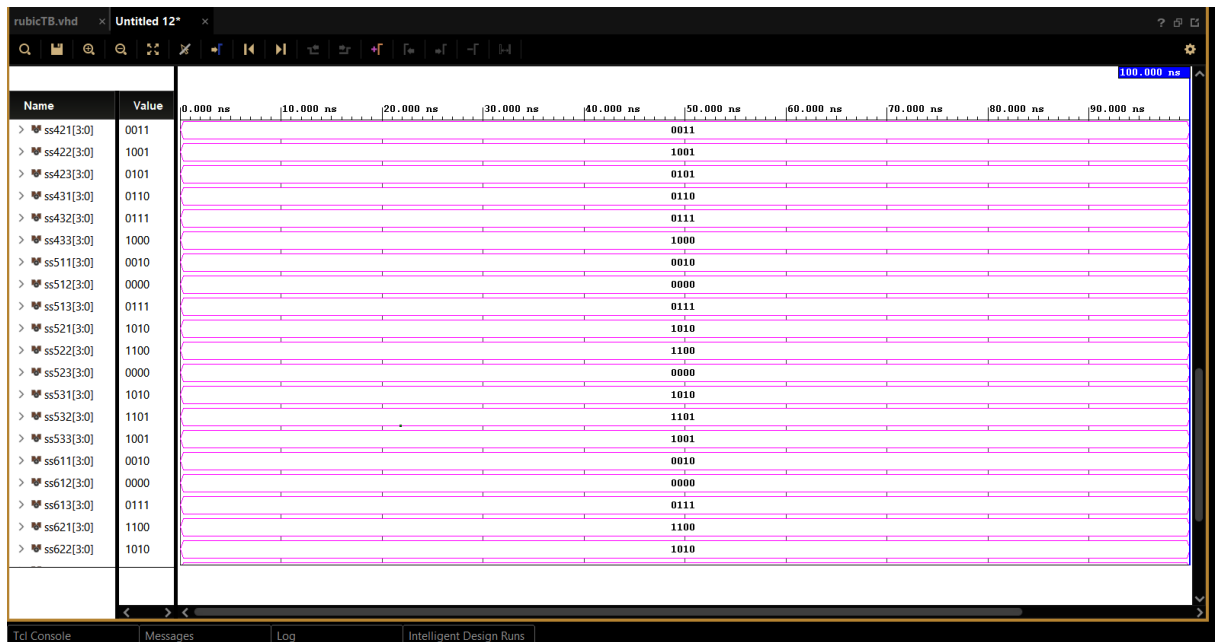




# Waveform for Test Case-5:







## Operation Labelling Table:

Where CU111 is Face 1 and Row 1 and Column 1 CU

Labelling operation for each CU	
CU111	MUL
CU112	ADD
CU112	RSL
CU121	SUB
CU122	NAND
CU123	XNOR
CU131	XNOR
CU132	XOR
CU133	XNOR
CU211	MUL
CU212	ADD
CU213	RSL
CU221	XNOR
CU222	NAND
CU223	SLA
CU231	SRA
CU232	LSR
CU233	LSL

CU311	MUL
CU312	ADD
CU313	RSL
CU321	PA
CU322	NOR
CU323	NAND
CU331	NO-OP
CU332	PB
CU333	XOR
CU411	MUL
CU412	ADD
CU413	RSL
CU421	LSL
CU422	NAND
CU423	SLA
CU431	SLR
CU432	RSL
CU433	RSR
CU511	MUL
CU512	ADD
CU513	RSL
CU521	NOR
CU522	XNOR

CU523	ADD
CU531	NOR
CU532	PA
CU533	NAND
CU611	MUL
CU612	ADD
CU613	RSL
CU621	XNOR
CU622	NOR
CU623	NAND
CU631	XNOR
CU632	RSR
CU633	LSL

### CU Operations by Selection line:

S.No:	Selection input	Operation
0	0000	Addition
1	0001	Subtraction
2	0010	Multiplication
3	0011	Logical Shift Left
4	0100	Logical Shift Right
5	0101	Arithmetic Shift Left
6	0110	Arithmetic Shift Right
7	0111	Rotate Shift Left
8	1000	Rotate Shift Right
9	1001	NAND
10	1010	NOR
11	1011	XOR
12	1100	XNOR
13	1101	PASS Data A
14	1110	PASS Data B
15	1111	No operation
16	Default	All Zeroes

## Abbreviations

Short Name	Full Form
CU	Computational Unit
ADD	Addition
MUL	Multiplication
SUB	Subtraction
LSL	Logical Shift Left
LSR	Logical Shift Right
RSL	Rotate Shift Left
RSR	Rotate Shift Right
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
NOT	NOT Gate
AND	AND Gate
NAND	NAND Gate
OR	OR Gate
NOR	NOR Gate
XOR	XOR Gate
XNOR	XNOR Gate
PA	Pass A
PB	Pass B
NO-OP	No-Operation