Project: I

Hardware Design Methodologies for ASICs and FPGA

by:

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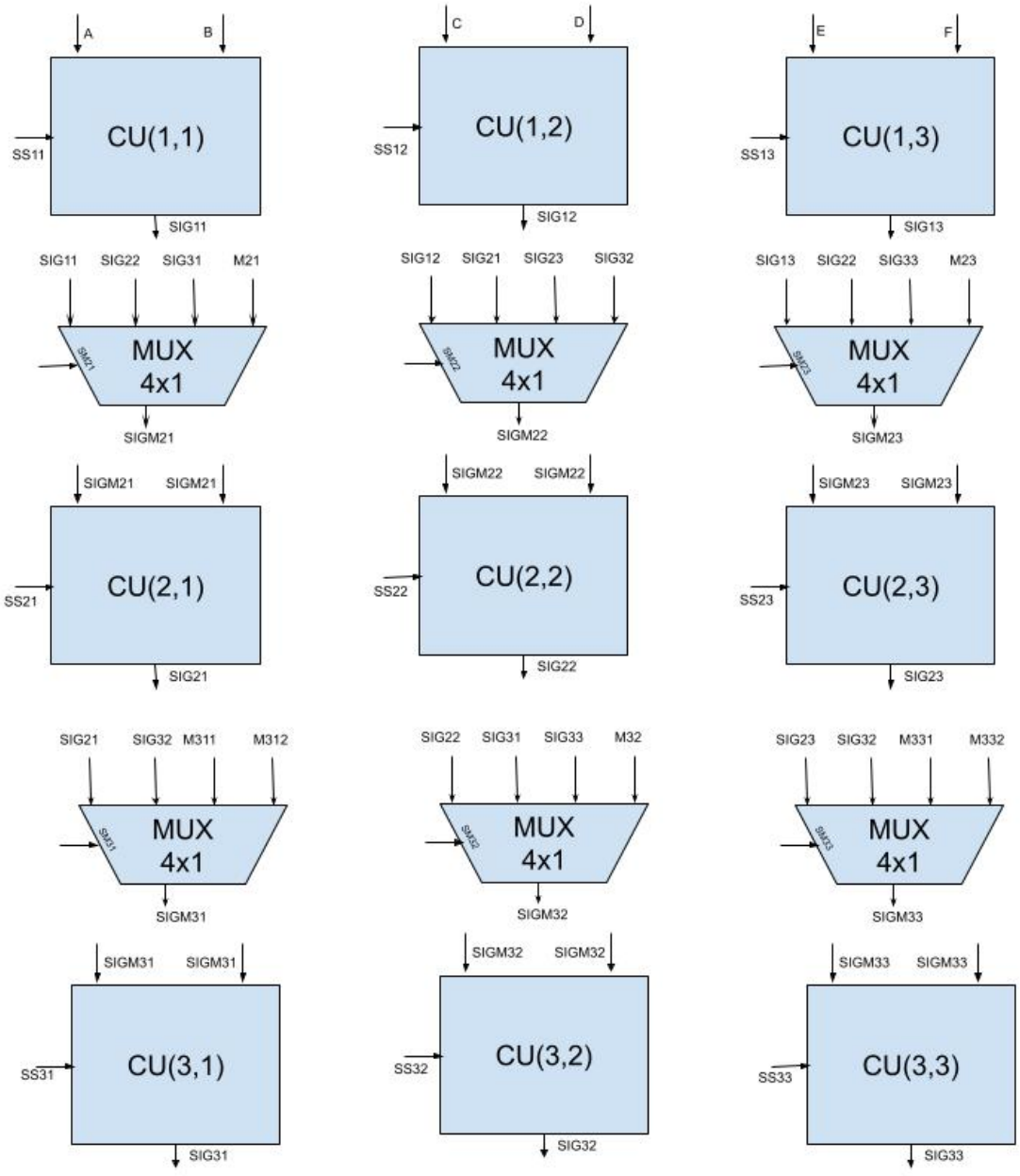
Block Diagrams:

Block Diagram for the Face Module:

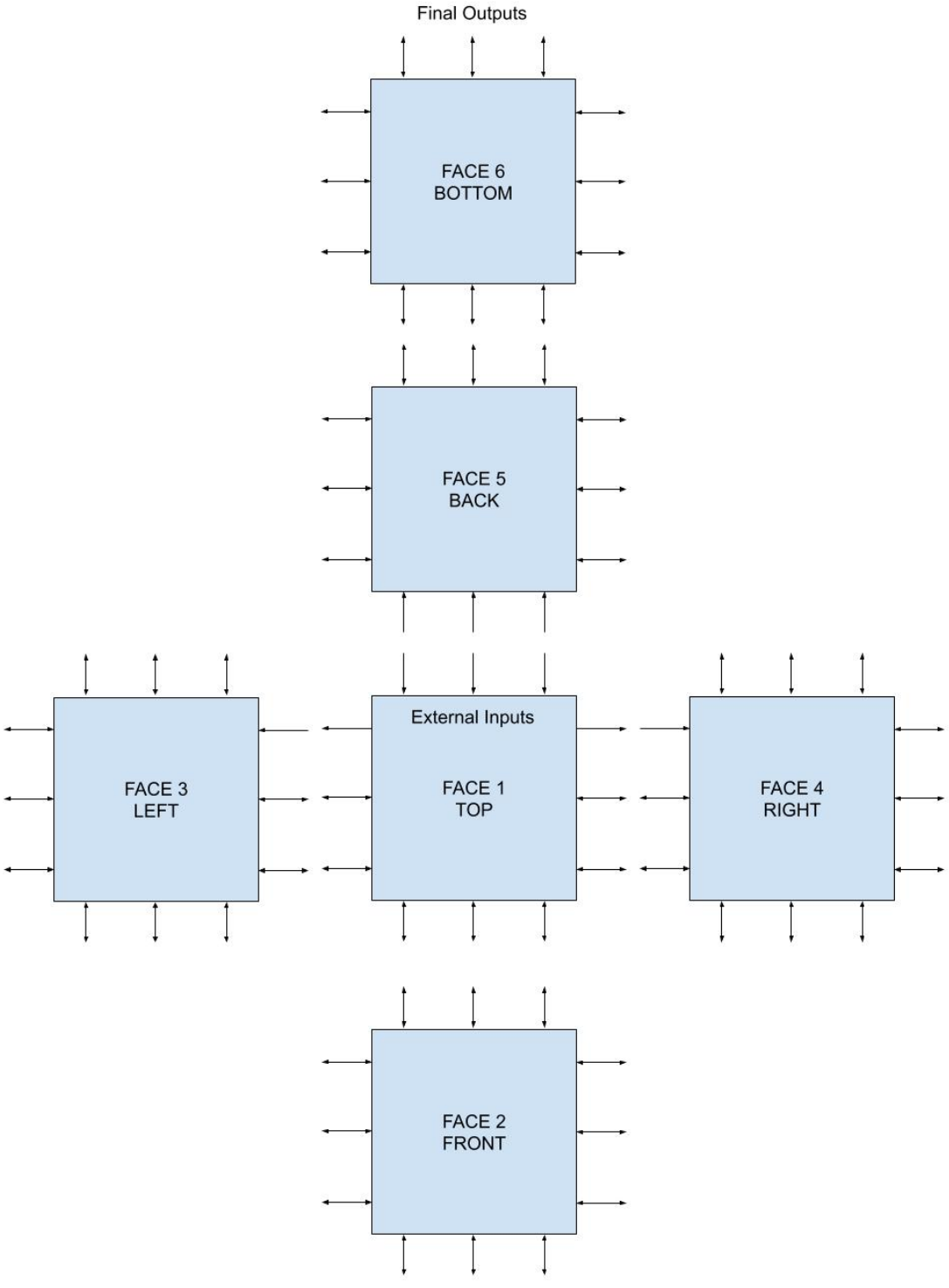


Face Module

Face Final Outputs has been assigned as below
CU_11<=SIG11; CU_12<=SIG12; CU_13<=SIG13; CU_21<=SIG21; CU_22<=SIG22; CU_23<=SIG23; CU_31<=SIG31; CU_32<=SIG32; CU_33<=SIG33.

M21, M23, M311, M312, M32, M331, M332 inputs for the multiplexers in the above figure are connected to the ALUs on the adjacent sides.

Overall Architecture



Rubik's Cube Architecture

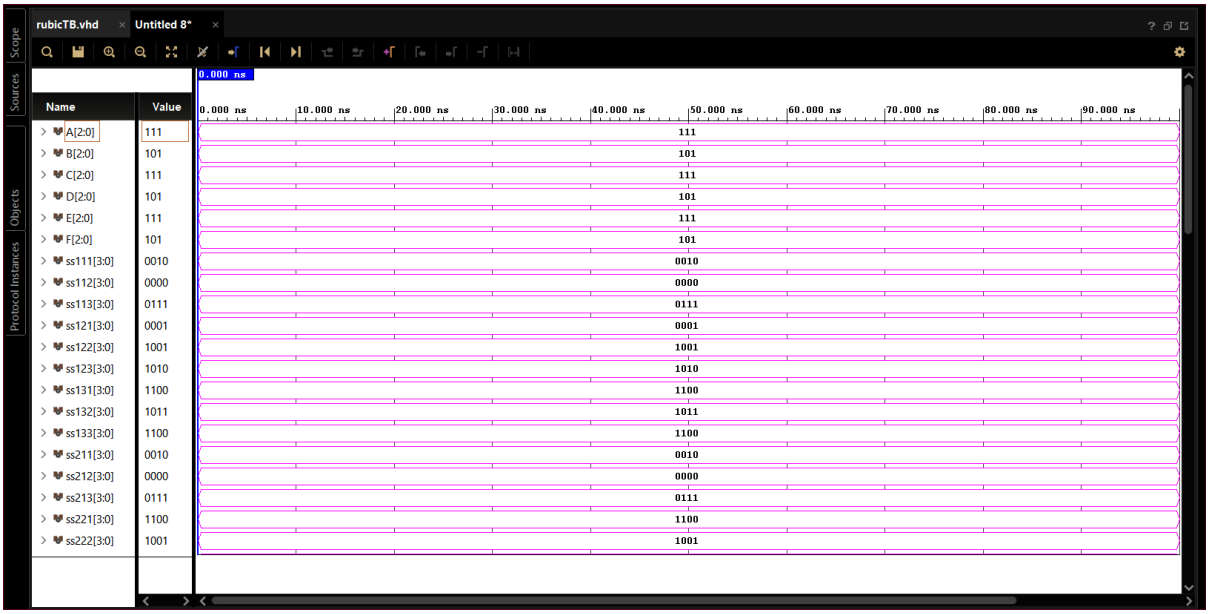
Outputs of CUs from all the edges of face 1 are given to the corresponding CUs of the adjacent face, as shown in the above figure.

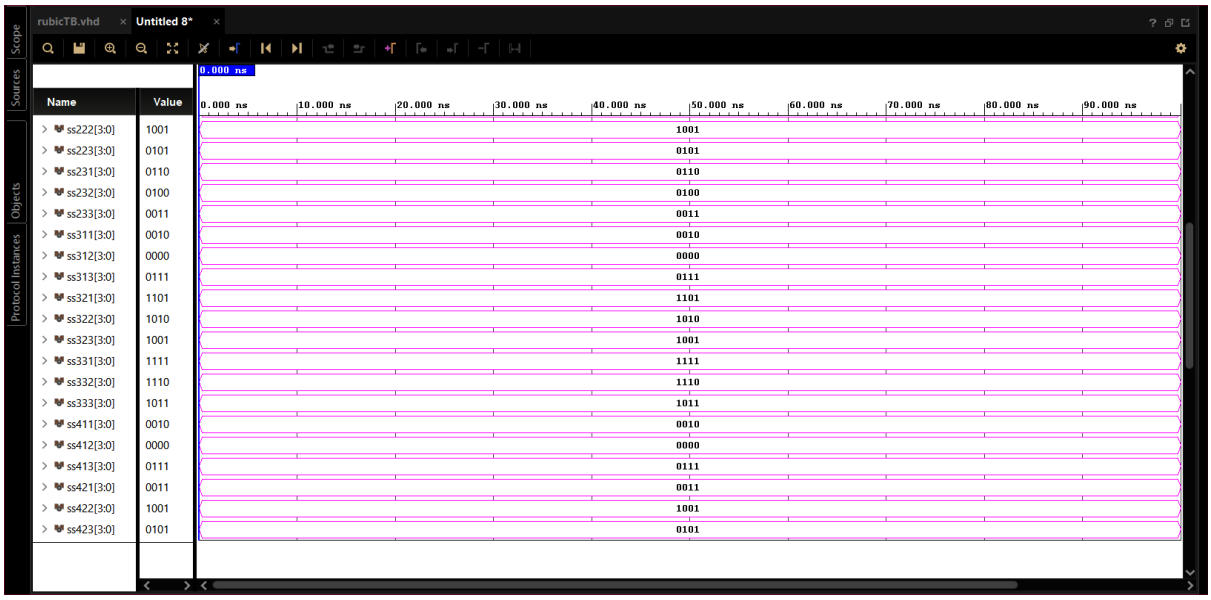
Design Explanations:

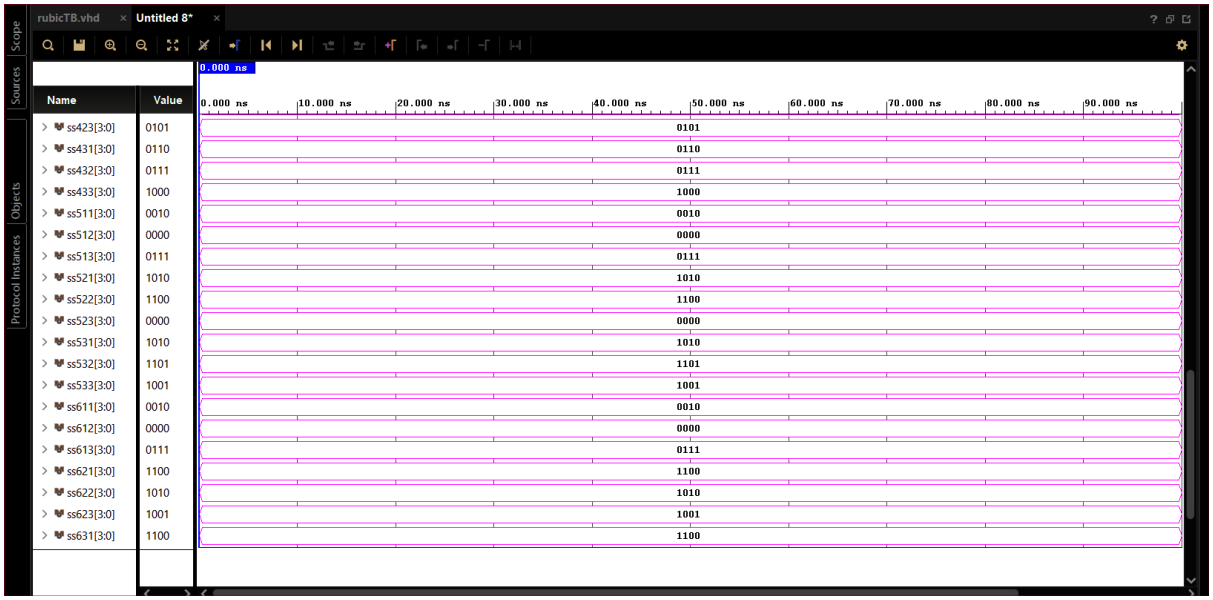
- We built face by repeating a CU nine times and the Cube by repeating that face six times.
- Our design is bi- directional, implemented using 4:1 multiplexers
- Designed in such a way that it is possible to select the inputs from any adjacent CU, for second and third rows of CU's
- If there is an overflow for a CU, then three LSB bits are taken as output.
- For shift operations, of the two inputs the first input which is 'A' in our case is shifted with input 'B' times.
- The two inputs of a CU can be passed with the use of two separate select lines. i.e., given as if they are separate operations.

Results:

Waveform for Test Case-1:



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Objects
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30.000 ns
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50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
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ss431[3:0] 0110
ss432[3:0] 0111
ss433[3:0] 1000
ss511[3:0] 0010
ss512[3:0] 0000
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
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ss533[3:0] 1001
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ss612[3:0] 0000
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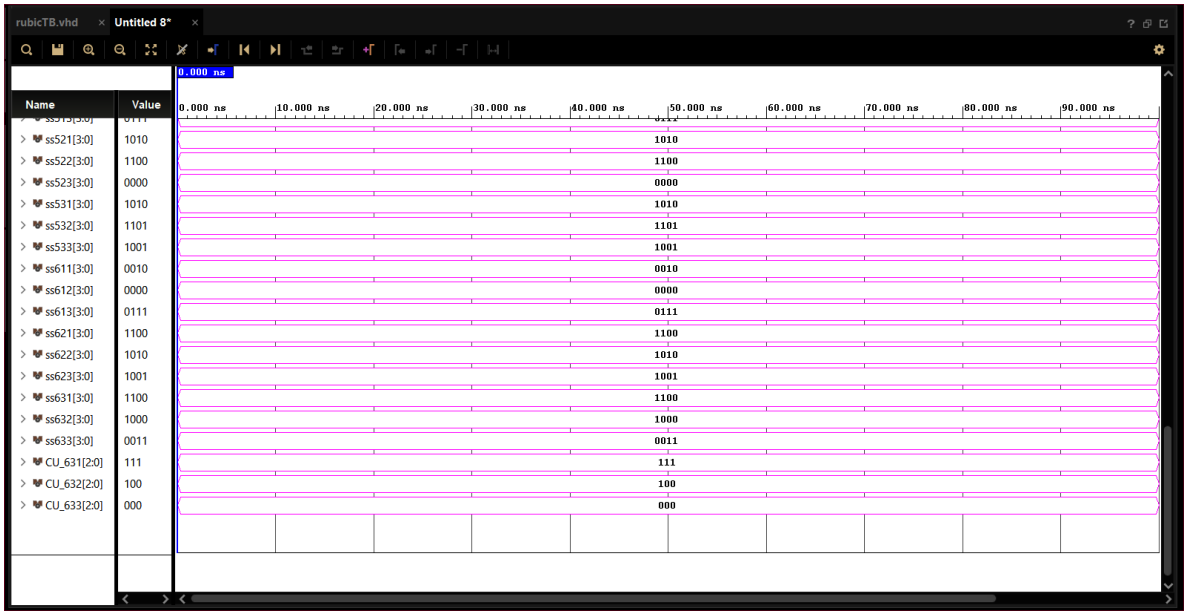
ss631[3:0] 1100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40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
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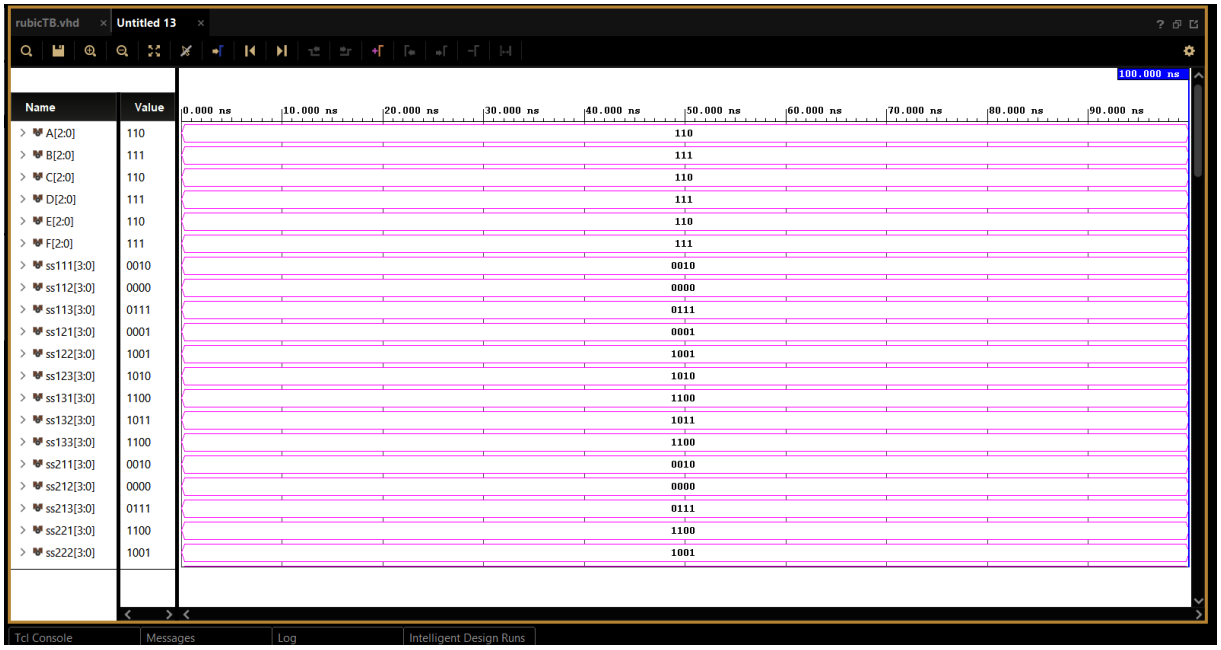
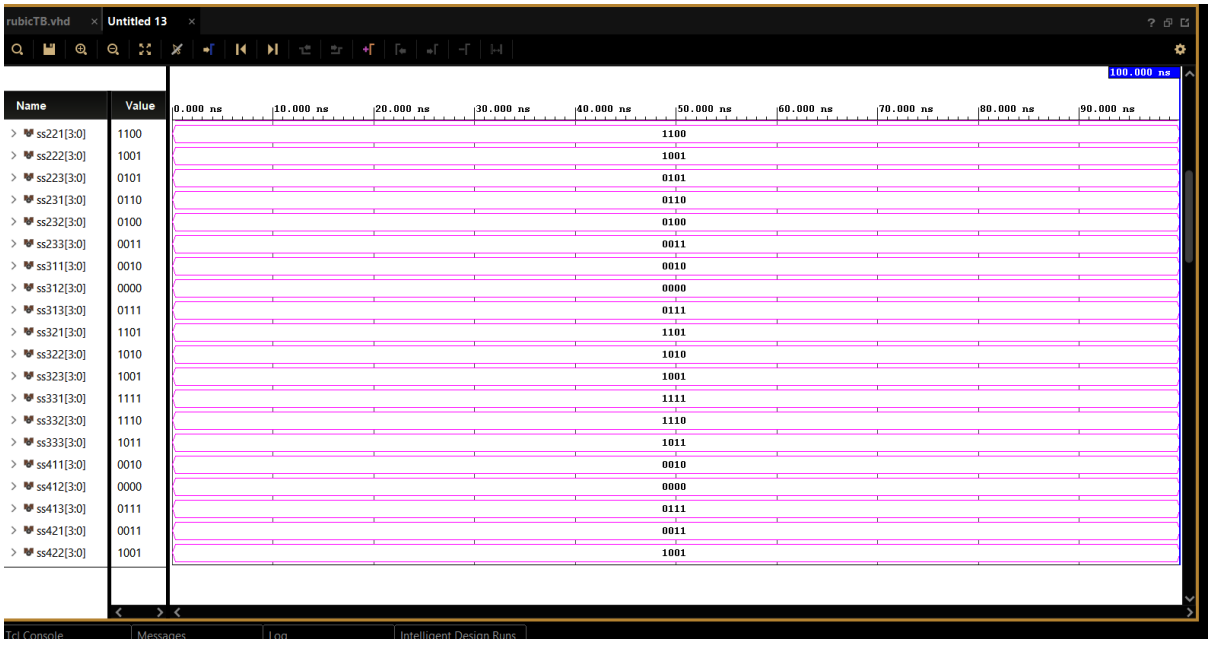
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100
ss632[3:0] 1000
ss633[3:0] 0011
CU_631[2:0] 111
CU_632[2:0] 100
CU_633[2:0] 000

Table for Test Case 2:

S.No	Both Inputs		**Origin of Inputs**	**CU Operation**	**Final Output**
	A	B			
1	111	101	External Inputs	MUL	011
2	010	010	CU111	RSL	011
3	000	000	CU513	ADD	110
4	111	111	CU523	NAND	001
5	000	000	CU533	RSL	010
6	111	111	CU613	NAND	101
7	001	001	CU623	LSL	000

Waveform for Test Case-2:

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30.000 ns
40.000 ns
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ss223[3:0] 0101
ss231[3:0] 0110
ss232[3:0] 0100
ss233[3:0] 0011
ss311[3:0] 0010
ss312[3:0] 0000
ss313[3:0] 0111
ss321[3:0] 1101
ss322[3:0] 1010
ss323[3:0] 1001
ss331[3:0] 1111
ss332[3:0] 1110
ss333[3:0] 1011
ss411[3:0] 0010
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ss413[3:0] 0111
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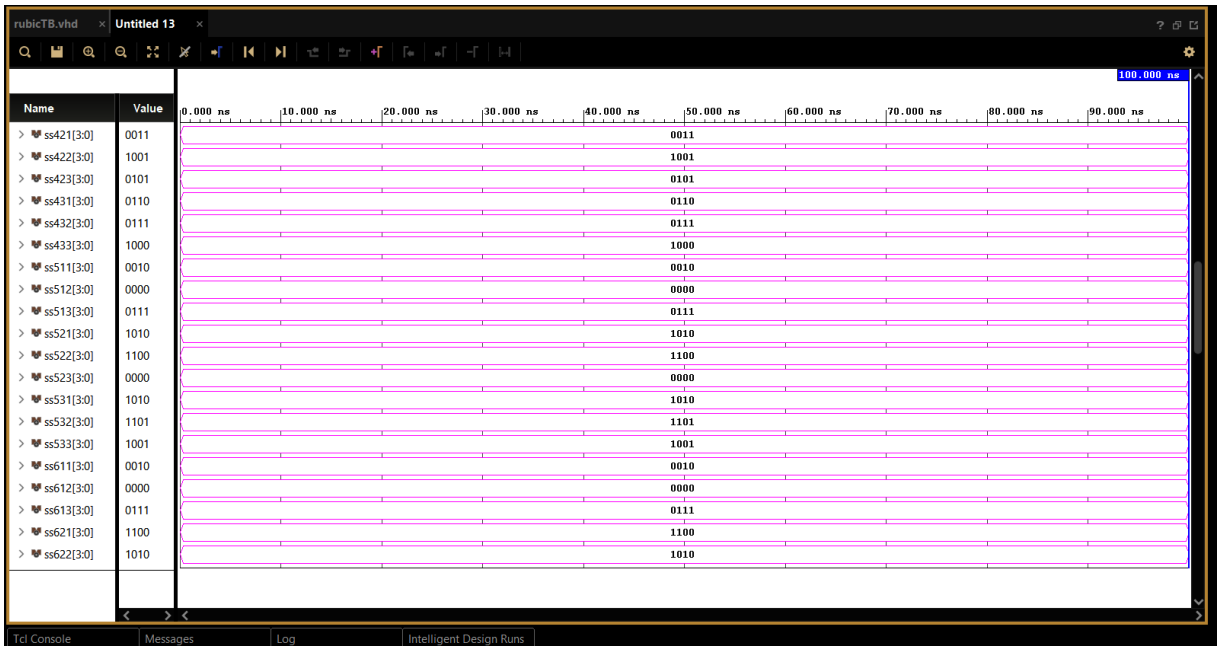
ss422[3:0] 1001
Tcl Console
Messages
Log
Intelligent Design Runs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30.000 ns
40.000 ns
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90.000 ns
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ss422[3:0] 1001
ss423[3:0] 0101
ss431[3:0] 0110
ss432[3:0] 0111
ss433[3:0] 1000
ss511[3:0] 0010
ss512[3:0] 0000
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
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ss531[3:0] 1010
ss532[3:0] 1101
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ss611[3:0] 0010
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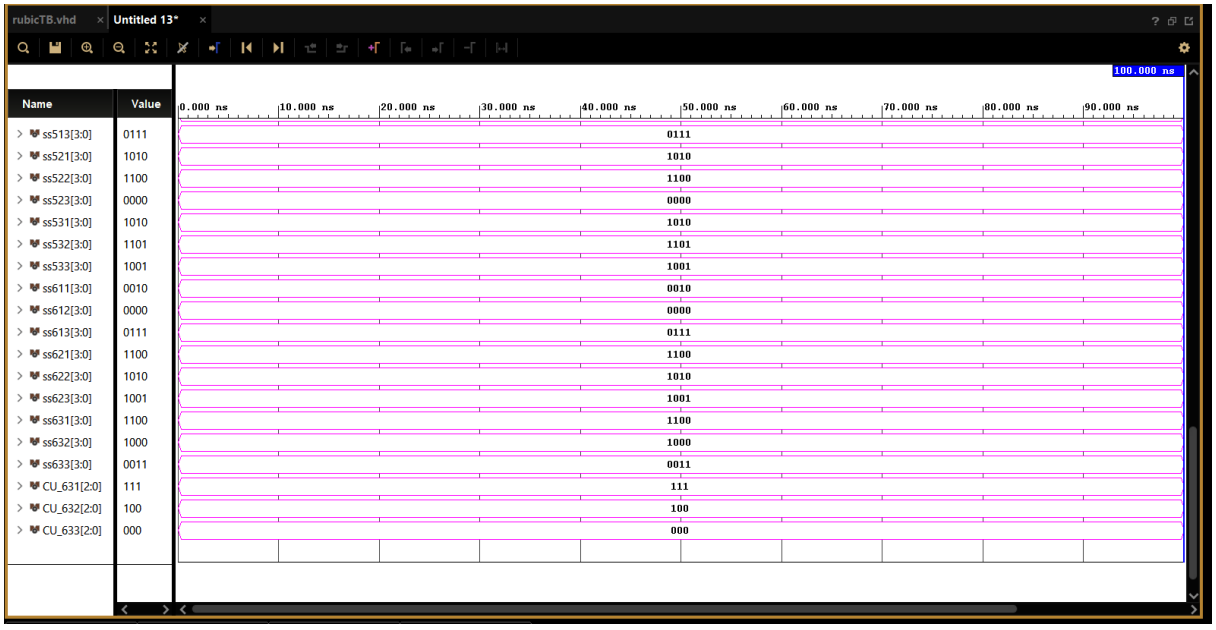
ss622[3:0] 1010
Tcl Console
Messages
Log
Intelligent Design Runs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20.000 ns
30.000 ns
40.000 ns
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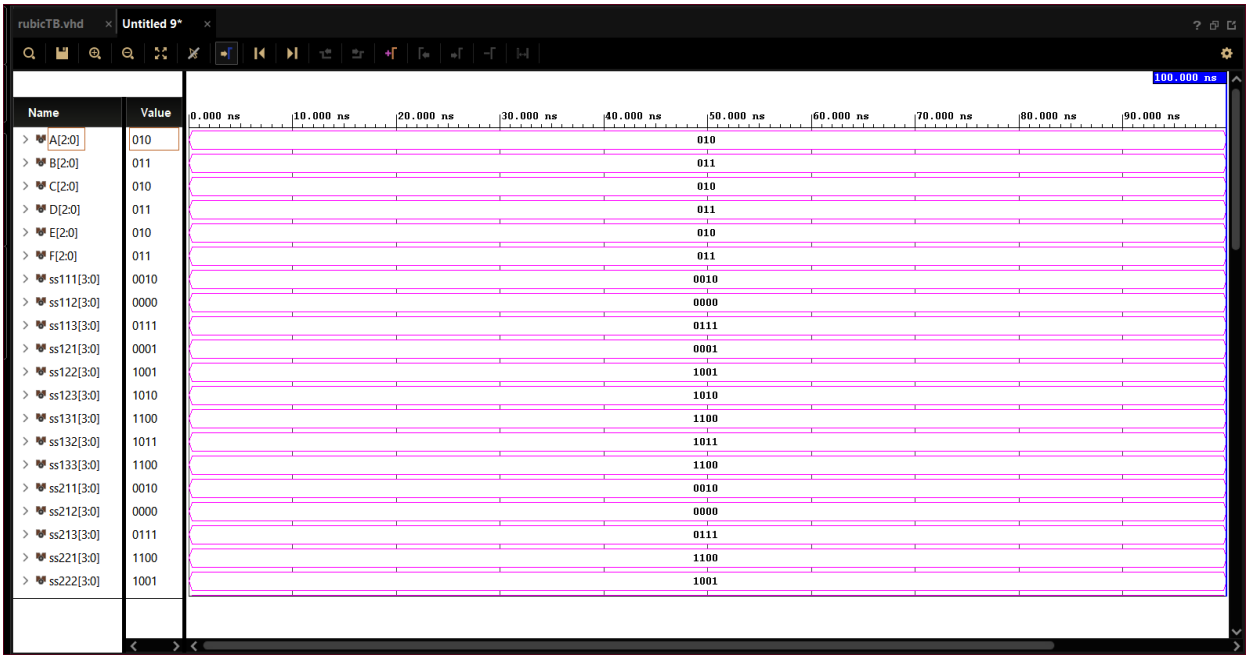
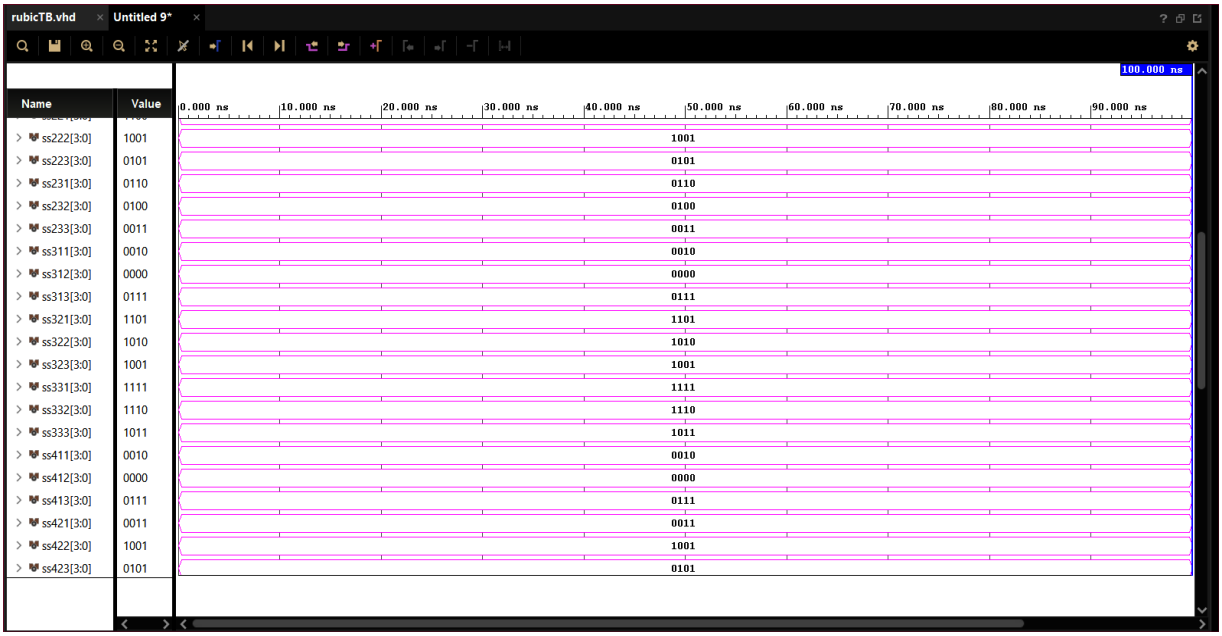
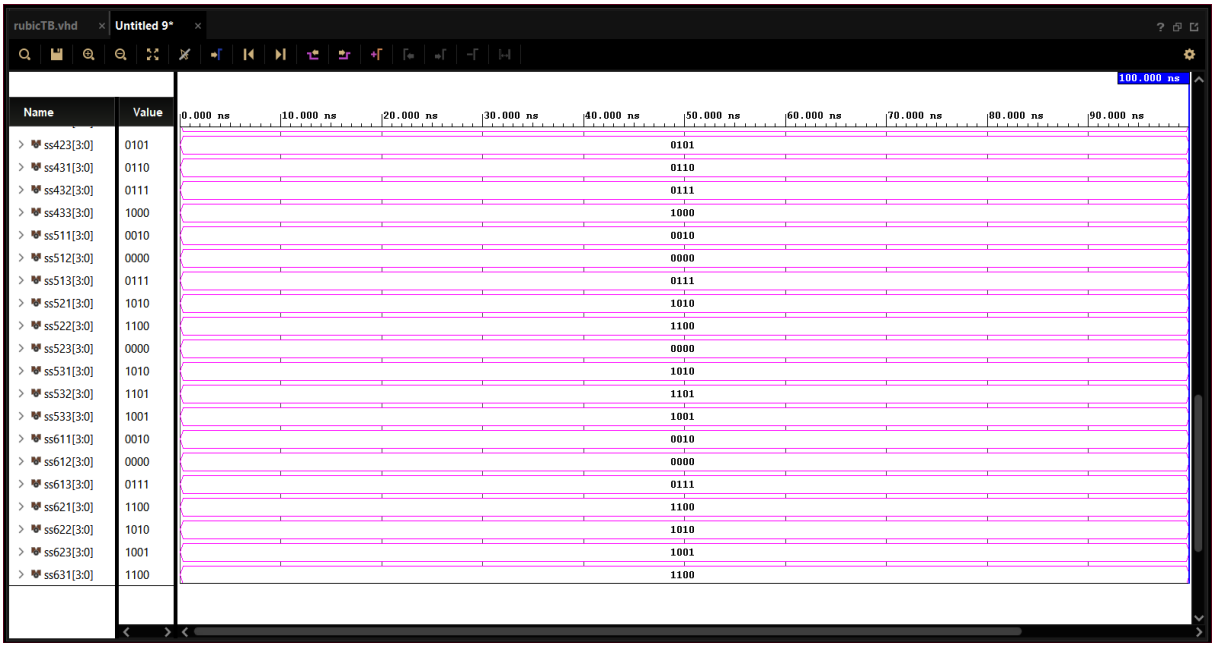
60.000 ns
70.000 ns
80.000 ns
90.000 ns
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100
ss632[3:0] 1000
ss633[3:0] 0011
CU_631[2:0] 111
CU_632[2:0] 100
CU_633[2:0] 000

Waveform for Test Case-3:



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Value
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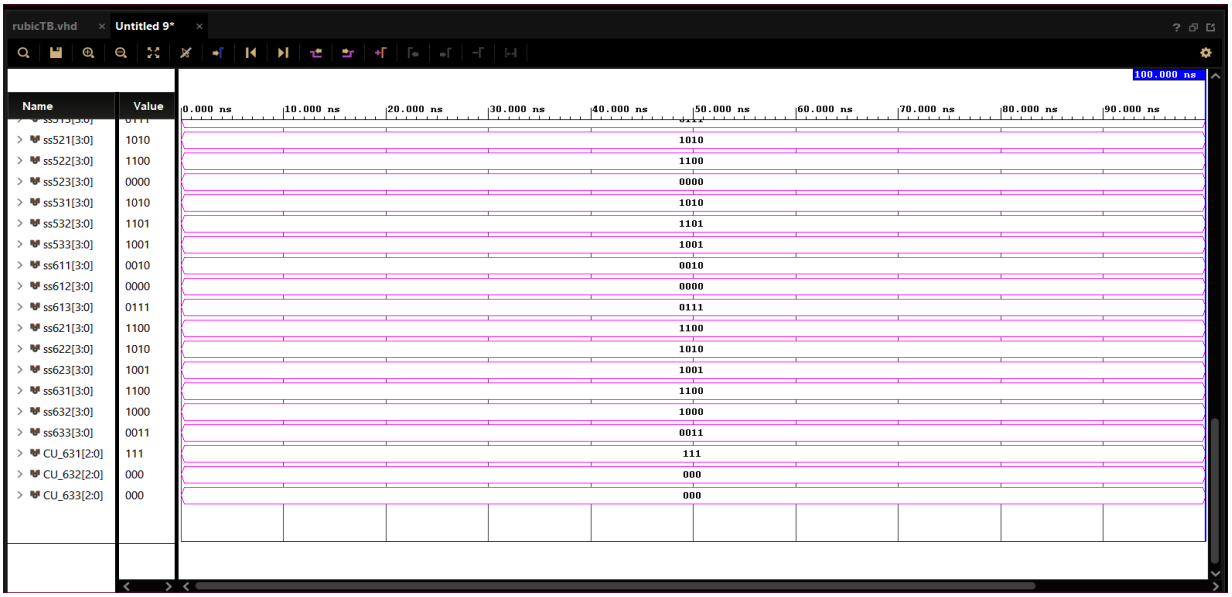
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
ss423[3:0] 0101
ss431[3:0] 0110
ss432[3:0] 0111
ss433[3:0] 1000
ss511[3:0] 0010
ss512[3:0] 0000
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100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Name
Value
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
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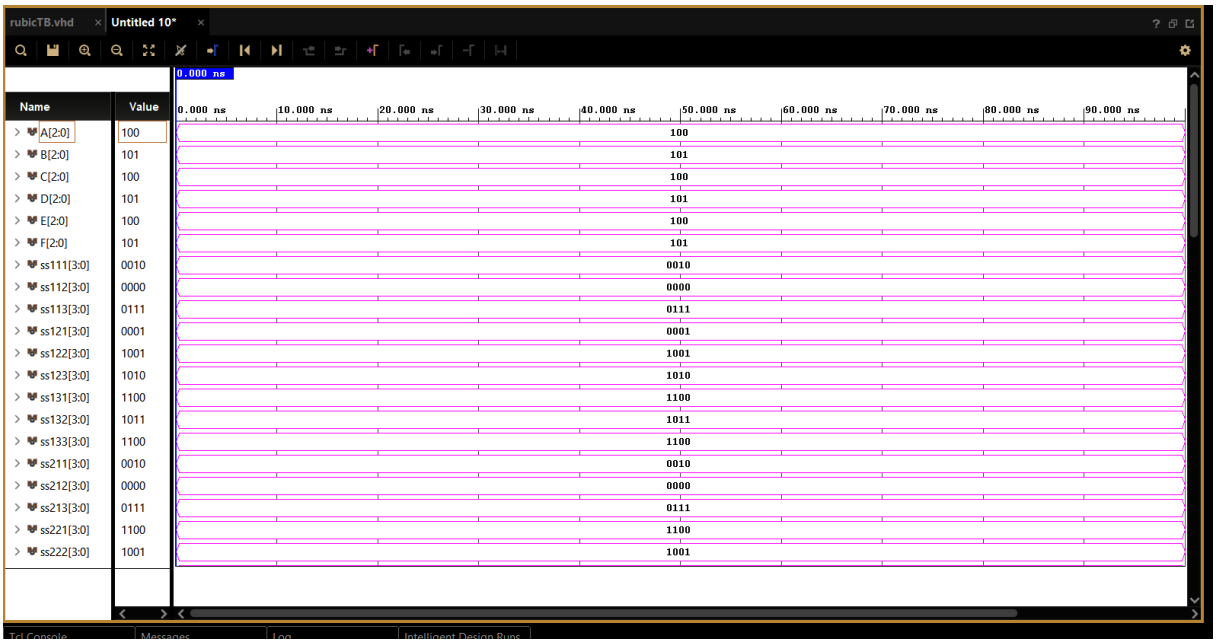
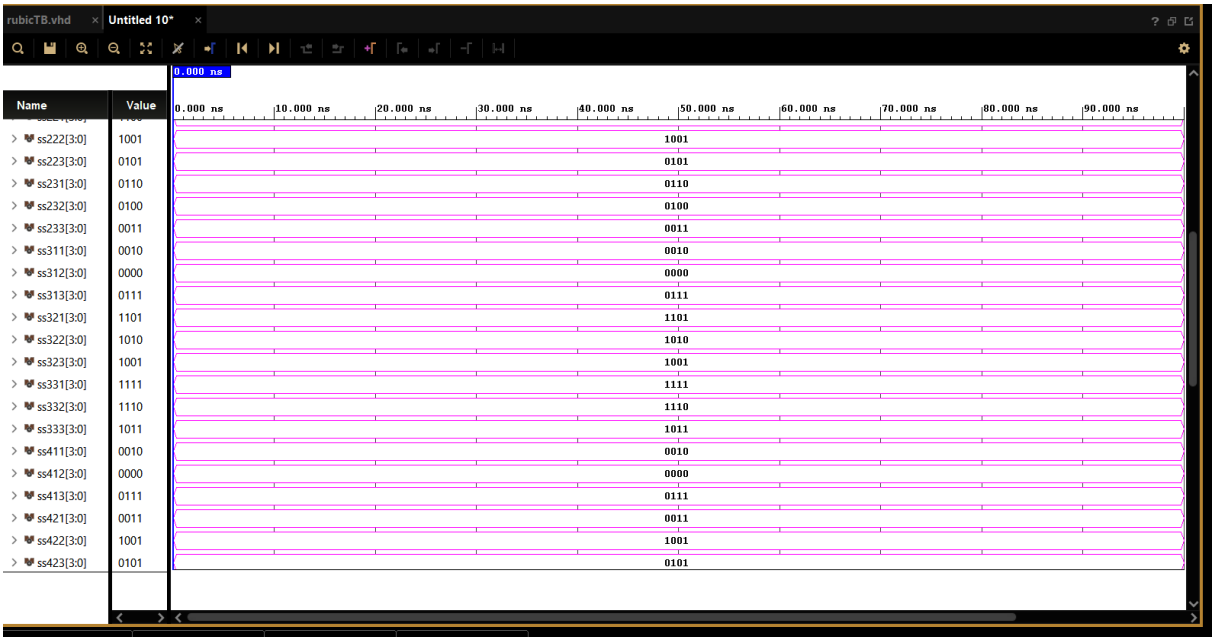
70.000 ns
80.000 ns
90.000 ns
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100
ss632[3:0] 1000
ss633[3:0] 0011
CU_631[2:0] 111
CU_632[2:0] 000
CU_633[2:0] 000

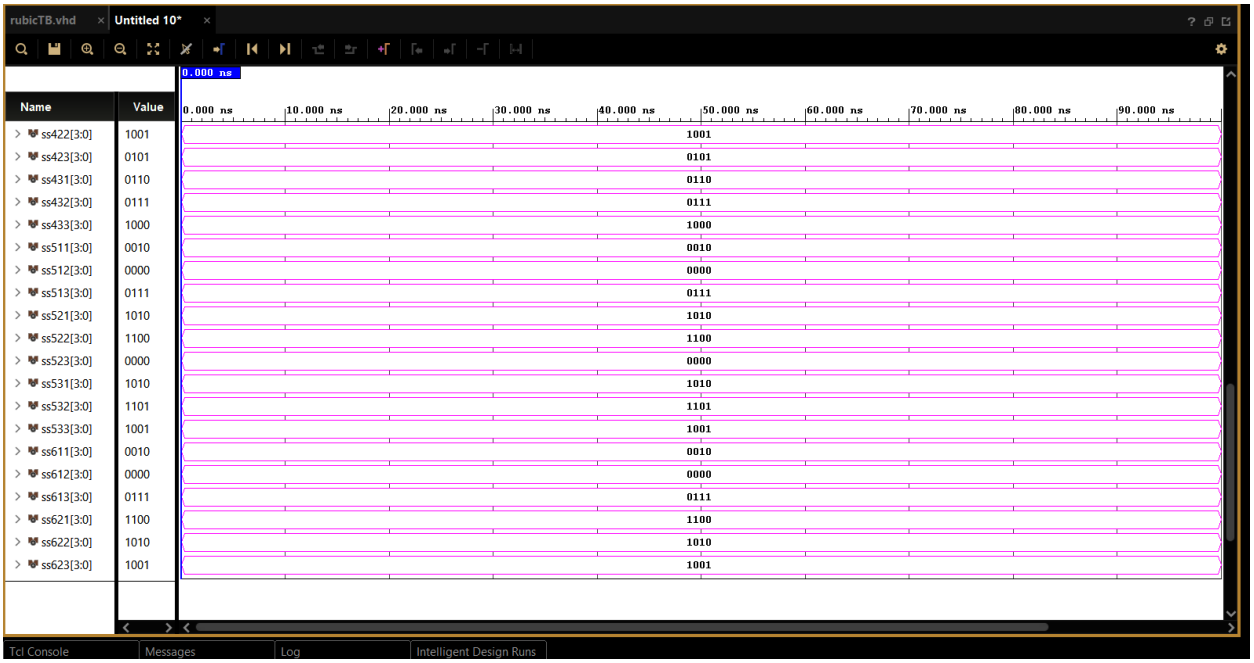
Table for Test Case 4:

S.No	Both Inputs		Origin of Inputs	CU Operation	Final Output
	A	B			
1	110	111	External Inputs	MUL	010
2	010	010	CU111	SUB	000
3	000	000	CU121	XNOR	111
4	111	111	CU131	XOR	000
5	000	000	CU132	XNOR	111
6	111	111	CU133	MUL	001
7	001	001	CU411	LSL	010
8	010	010	CU421	NAND	101
9	101	101	CU422	SLA	111
10	111	111	CU423	NOR	000
11	000	000	CU521	XNOR	111
12	111	111	CU522	ADD	110
13	110	110	CU523	NAND	001
14	001	001	CU533	RSL	010
15	010	010	CU613	NAND	101
16	101	101	CU623	LSL	000

Waveform for Test Case-4:



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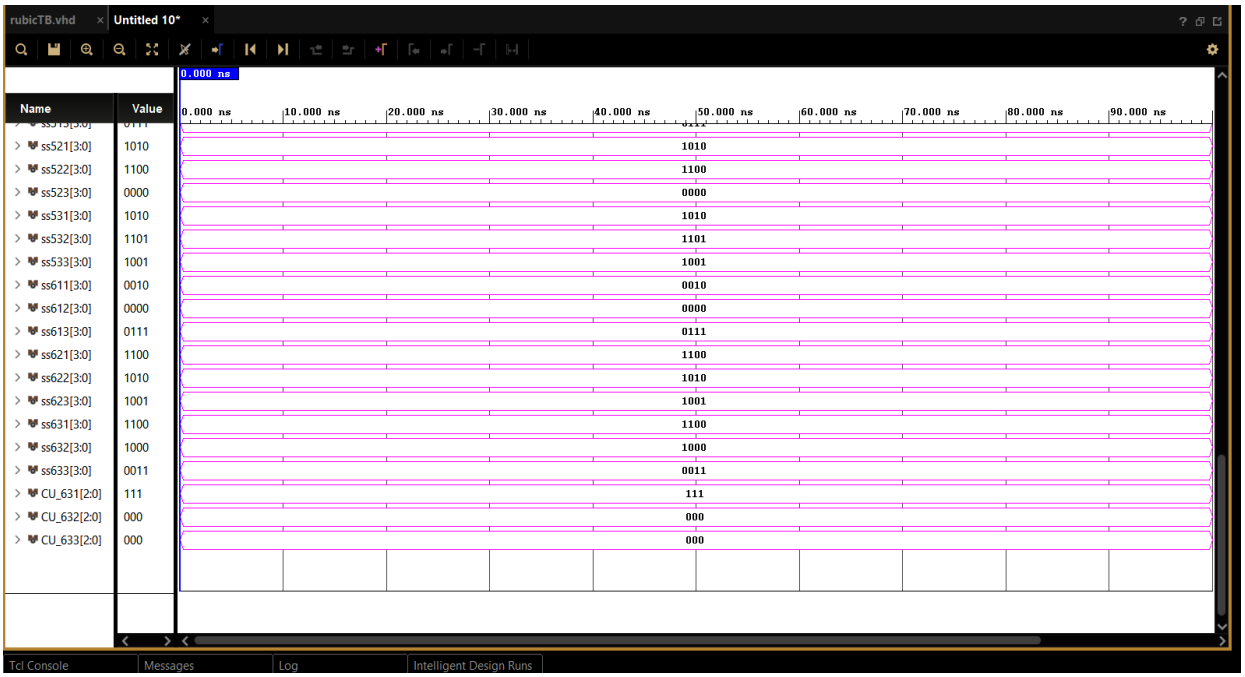
ss512[3:0] 0000
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
Tcl Console
Messages
Log
Intelligent Design Runs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ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100
ss632[3:0] 1000
ss633[3:0] 0011
CU_631[2:0] 111
CU_632[2:0] 000
CU_633[2:0] 000
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
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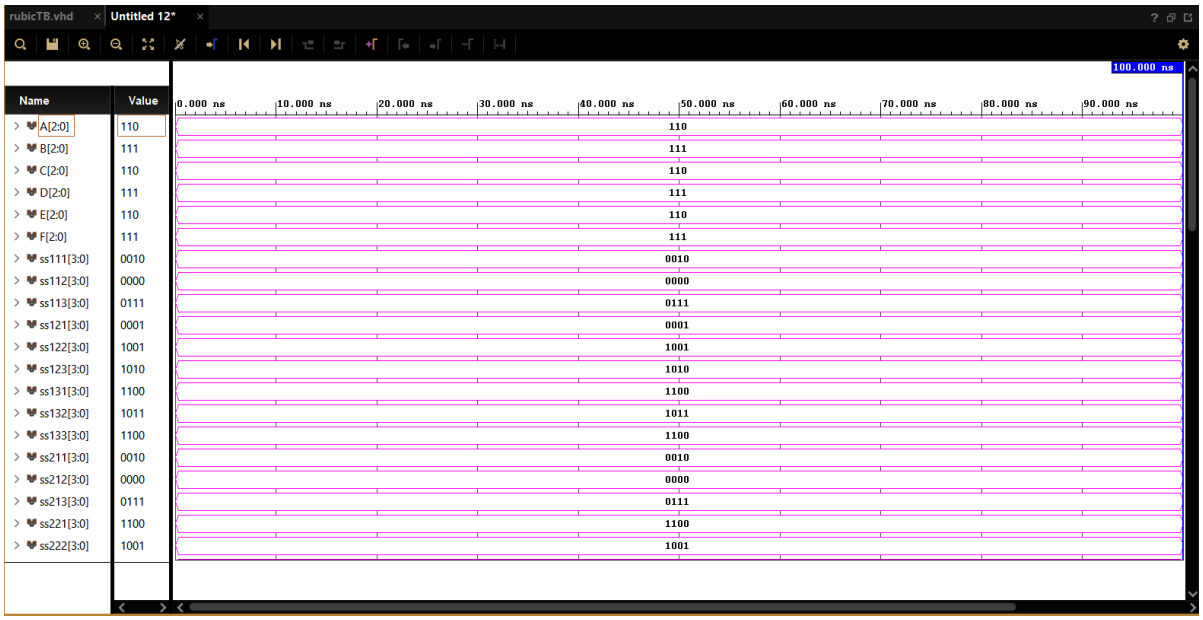
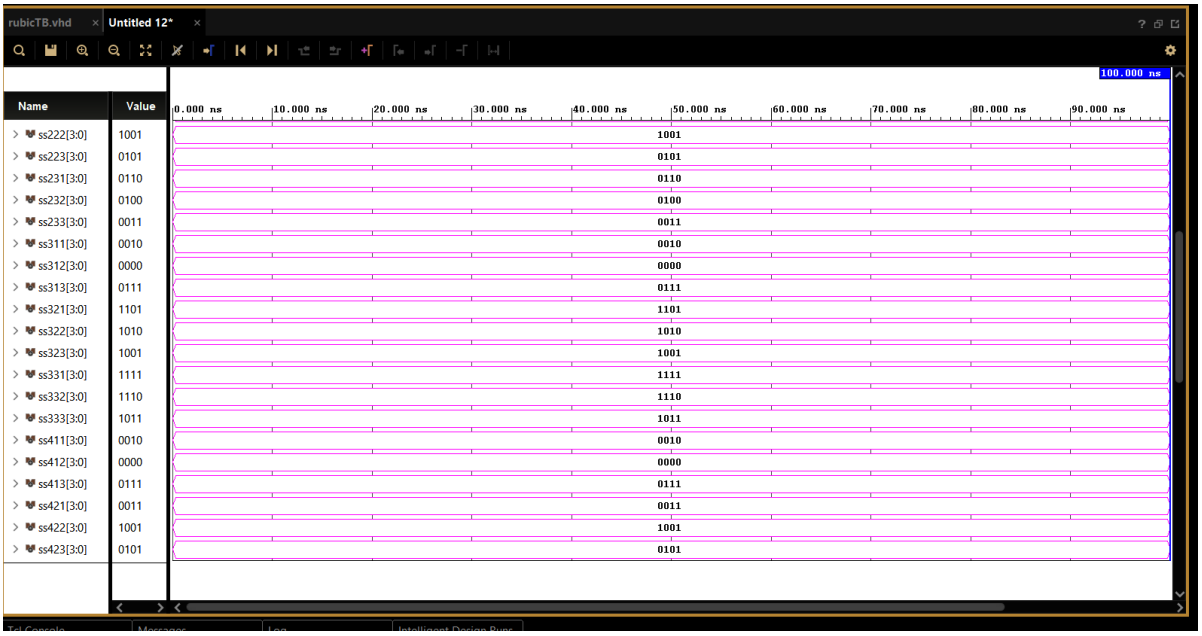
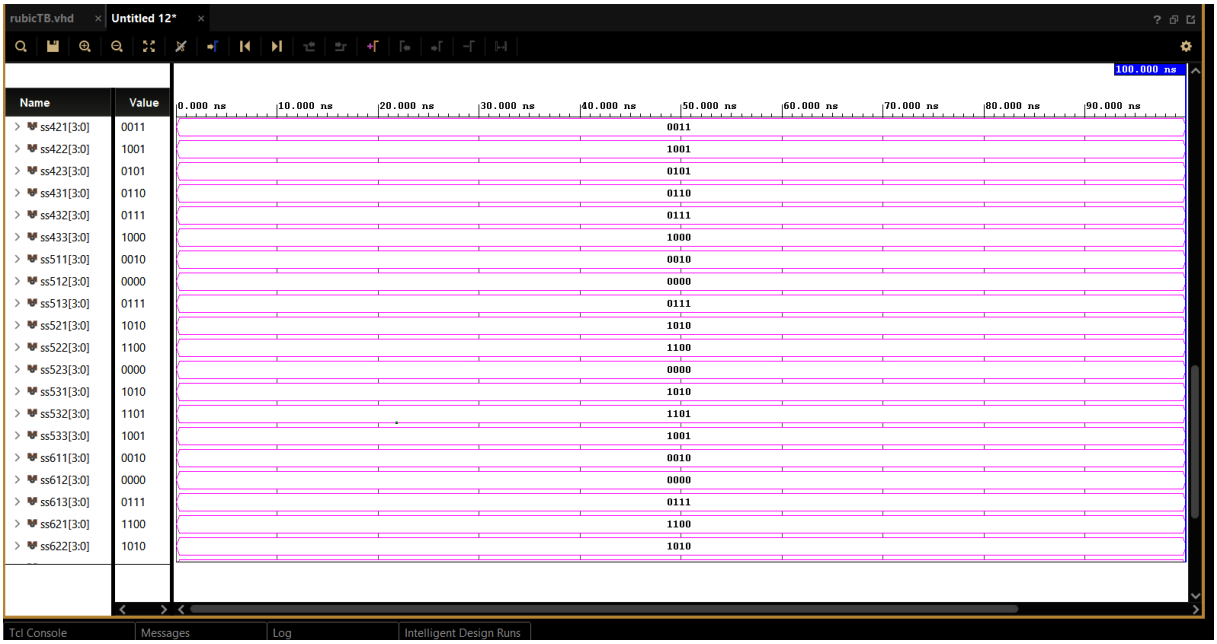
80.000 ns
90.000 ns
Tcl Console
Messages
Log
Intelligent Design Runs

Waveform for Test Case-5:



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40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
90.000 ns
ss421[3:0] 0011
ss422[3:0] 1001
ss423[3:0] 0101
ss431[3:0] 0110
ss432[3:0] 0111
ss433[3:0] 1000
ss511[3:0] 0010
ss512[3:0] 0000
ss513[3:0] 0111
ss521[3:0] 1010
ss522[3:0] 1100
ss523[3:0] 0000
ss531[3:0] 1010
ss532[3:0] 1101
ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
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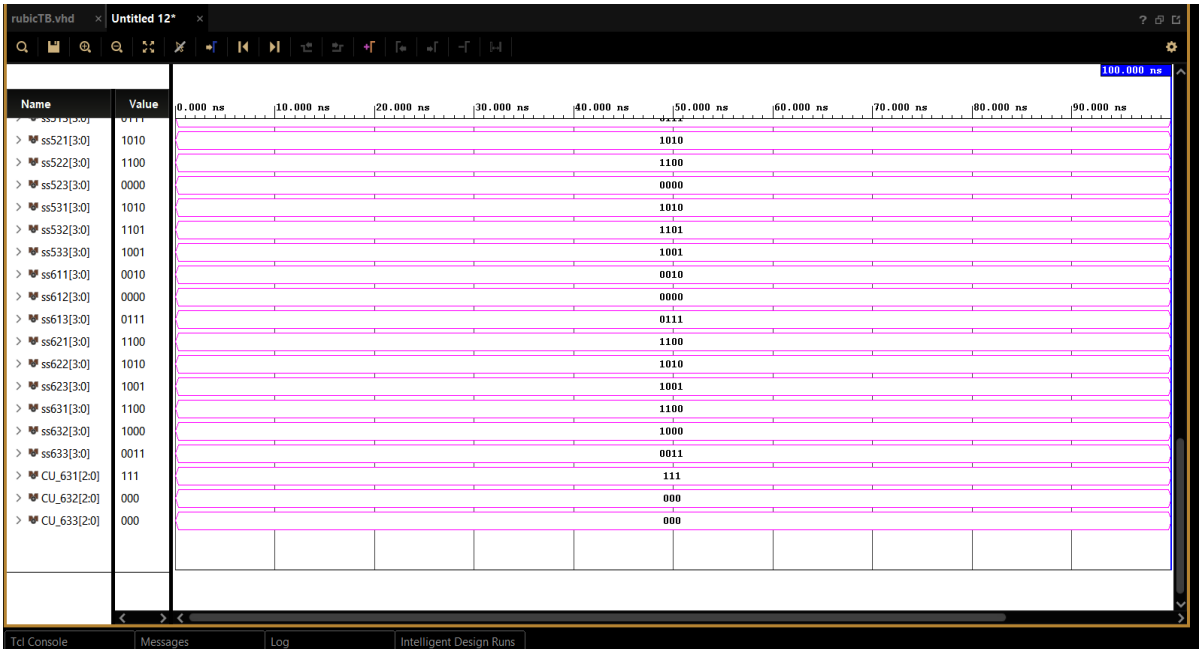
Tcl Console
Messages
Log
Intelligent Design Runs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80.000 ns
90.000 ns
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ss523[3:0] 0000
ss531[3:0] 1010
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ss533[3:0] 1001
ss611[3:0] 0010
ss612[3:0] 0000
ss613[3:0] 0111
ss621[3:0] 1100
ss622[3:0] 1010
ss623[3:0] 1001
ss631[3:0] 1100
ss632[3:0] 1000
ss633[3:0] 0011
CU_631[2:0] 111
CU_632[2:0] 000
CU_633[2:0] 000
Tcl Console
Messages
Log
Intelligent Design Runs

Operation Labelling Table:

Where CU111 is Face 1 and Row 1 and Column 1 CU

Labelling operation for each CU	
CU111	MUL
CU112	ADD
CU112	RSL
CU121	SUB
CU122	NAND
CU123	XNOR
CU131	XNOR
CU132	XOR
CU133	XNOR
CU211	MUL
CU212	ADD
CU213	RSL
CU221	XNOR
CU222	NAND
CU223	SLA
CU231	SRA
CU232	LSR

CU233	LSL
CU311	MUL
CU312	ADD
CU313	RSL
CU321	PA
CU322	NOR
CU323	NAND
CU331	NO-OP
CU332	PB
CU333	XOR
CU411	MUL
CU412	ADD
CU413	RSL
CU421	LSL
CU422	NAND
CU423	SLA
CU431	SLR
CU432	RSL
CU433	RSR
CU511	MUL
CU512	ADD
CU513	RSL
CU521	NOR

CU522	XNOR
CU523	ADD
CU531	NOR
CU532	PA
CU533	NAND
CU611	MUL
CU612	ADD
CU613	RSL
CU621	XNOR
CU622	NOR
CU623	NAND
CU631	XNOR
CU632	RSR
CU633	LSL

CU Operations by Selection line:

S.No:	Selection input	Operation
0	0000	Addition
1	0001	Subtraction
2	0010	Multiplication
3	0011	Logical Shift Left
4	0100	Logical Shift Right
5	0101	Arithmetic Shift Left
6	0110	Arithmetic Shift Right
7	0111	Rotate Shift Left
8	1000	Rotate Shift Right
9	1001	NAND
10	1010	NOR
11	1011	XOR
12	1100	XNOR
13	1101	PASS Data A
14	1110	PASS Data B
15	1111	No operation
16	Default	All Zeroes

Abbreviations

Short Name	Full Form
CU	Computational Unit
ADD	Addition
MUL	Multiplication
SUB	Subtraction
LSL	Logical Shift Left
LSR	Logical Shift Right
RSL	Rotate Shift Left
RSR	Rotate Shift Right
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
NOT	NOT Gate
AND	AND Gate
NAND	NAND Gate
OR	OR Gate
NOR	NOR Gate
XOR	XOR Gate
XNOR	XNOR Gate
PA	Pass A
PB	Pass B
NO-OP	No-Operation