Design of combinational Circuits using Quantum-dot Cellular Automata Technology

Mini Project Work (22EC5PWPJ1) report submitted to

Visvesvaraya Technological University, Belagavi in partial fulfilment of the requirements for the degree of

Bachelor of Engineering in Electronics and Communication Engineering

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Certificate

Certified that the mini project work entitled " Design of combinational Circuits usingQuantum-dot Cellular Automata Technology" is a bonafide record of workdone carried out by

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in partial fulfilment of the requirements for the degree of Bachelor pf Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belagavi, dur- ing the year 2022 – 23. It is certified that all corrections/suggestions indicated during the internal assessments have been incorporated.

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Semester End Examination

Name of the Examiner Signature with Date

1.

2

DECLARATION

We, hereby declare that the mini project work entitled ' Design of combinational Circuits using Quantum-dot Cellular Automata Technology' has been carried out by us under the guidance of **R.C RADHA**, Professor, Department of Electronics and Communication Engineering, B. M. S. College of Engineering, Bengaluru, in partial fulfilment of the requirements for the degree of Bachelor of Engineering in Mechanical Engineering of Visvesvaraya Technological University, Belagavi.

We further declare that we have not submitted this report either in part or in full to any other university for the award of any degree/diploma.

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We would like to thank our Head of the Department, **Dr. Siddappaji**, Professor & Head, Department of Electronics and Communication, B. M. S. College of Engineering, Bengaluru, and our Principal, **Dr. S. Muralidhara**, Principal, B. M. S. College of Engineering, Bengaluru.

We would like to thank **Our Parents**, whose love and guidance are important to us in whatever I pursue. They are the ultimate role models who provide unending inspiration to us. Finally we would like to thank the one and all who have directly or indirectly helped us in completing this project work successfully.

ABSTRACT:

There has been a constant evolution from first computer starting from electro-mechanical switches and relays to vacuum tubes triodes, to transistors and the current era Metal-Oxide Field-Effect Transistor(MOSFETs). Each evolution has had a significant improvement in computational and power parameters compared to its previous generation technology. According to Moore"s law number of transistors in a chip doubles after every 18 months, but seeing the current trend and the $MOS" technology limitations it will reach a saturation. There is a need to research and develop other avenues of semiconductor industry.

There have been many proposals and researches on $beyond CMOS" technology, among which Spin Wave Devices, Nano-Magnetic Logic and Quantum Dot Cellular Automata (QCA) are the most feasible solutions. QCA is found to be most feasible, efficient and advantageous in terms of parallelism, implementation, accuracy, computation and area on chip. In this report QCA as a technology and its implementation in semiconductor industry is discussed. In this report construction and design of basic gates, wires and clocking cycles using QCA has been comprehensively discussed.

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CHAPTER 1

INTRODUCTION

1.1 What is a Quantum Dot?

Quantum dots are tiny semiconductor particles that can be as small as a few nanometers in diameter. They are often referred to as artificial atoms due to their unique electronic properties, which are somewhat similar to those of individual atoms.

Quantum dots are very small, typically ranging from 2 to 10 nanometers in diameter. Because of their small size, they exhibit quantum mechanical properties that are not observed in larger materials.

Quantum dots exhibit Quantum Confinement where Quantum dots confine the motion of electrons and holes (electron vacancies) within their structure. This confinement leads to discrete energy levels, similar to those observed in atoms. This property makes Quantum dots a fascinating nano material with multiple desirable tunable properties.

1.2 What is Quantum Dot Cellular Automata?

Quantum-dot Cellular Automata (QCA) is a novel computing paradigm that operates at the nanoscale level, utilizing the spatial distribution of electron charge configuration in quantum dots to represent binary information.

Cellular Automata (CA) is an attractive emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers. A QCA is a square nanostructure of electron wells confining free electrons. Each cell has four quantum dots which can hold a single electron per dot. The physical representation of a Quantum Dot Cellular Automata.

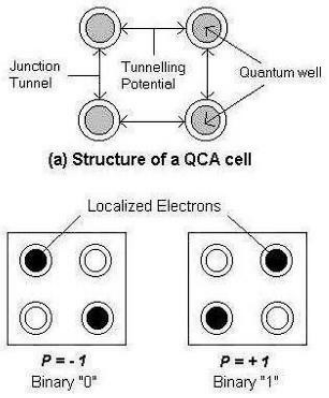

Figure 1.1: QCA CELL

1.3 Fundamentals Of Quantum Dot cellular Automata:

1.3.1 THE 90 DEGREE QCA CELL:

The QCA cell has the four quantum dots at four corners of the square, the two electrons always take place at the diagonally opposite dots (to minimize Columbic Repulsion).

This cell is mostly used in the design processes. It affects the next identical cell in a way that the next cell also imbibes the same polarization as the previous cell and not the inverted one.

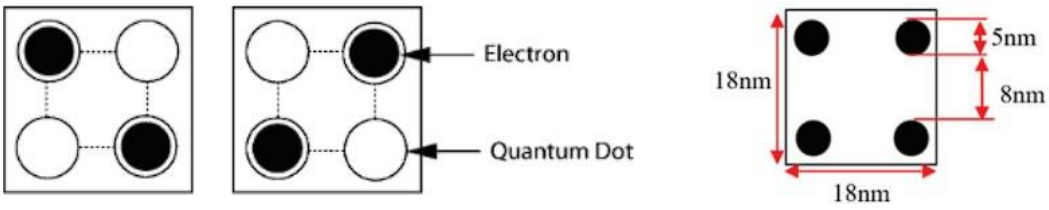

Figure 1.2 : 90 Degree QCA Cell

1.3.2 THE 45 DEGREE QCA CELL:

The 45o QCA is also known as rotated QCA cell. The cell identical in operation to the 90o cell but the location of metal islands within the cells differentiates the two.

This also ensures the presence of electrons at the least interaction locations.

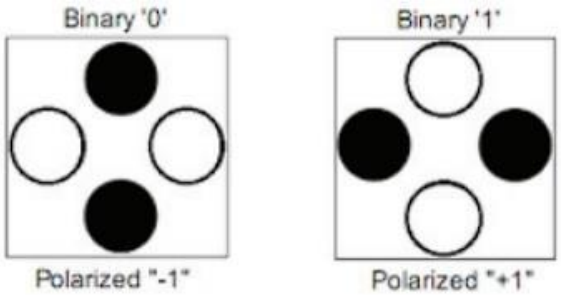

Figure 1.3 : 45 Degree QCA Cell

1.3.3 QCA WIRE:

QCA cells when placed in a tandem, one after another, form the QCA wire.

The first cell of a wire is known as driver cell and the last cell is known as Ripper cell.

The wire is properly clocked for proper propagation of data and for synchronization of input and output to different circuit parts.

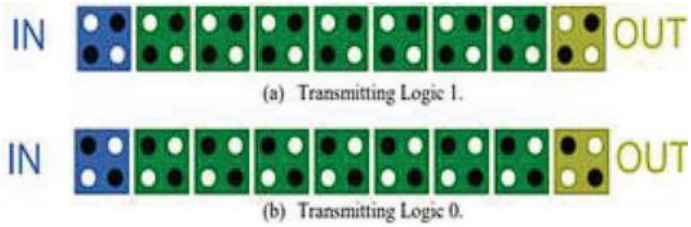

Figure 1.4: Wire for 90 degree Cell

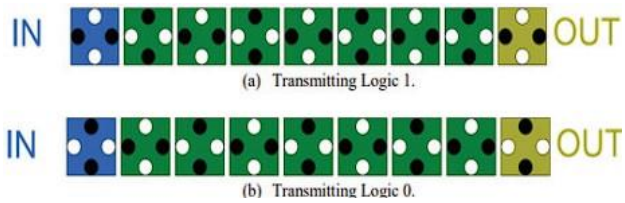

Figure 1.5: Wire for 45 degree Cell

1.3.4 QCA CLOCK:

During the switch phase of clock, the energy barriers start raising and the cell attains a definite polarization based on the driving input and the polarization of neighbouring cells. The electrons get confined in the 3-d space of the quantum dot.

In the hold phase, of QCA clock, the potential barriers retain the higher value, the energy walls are greater and proscribes electrons from tunnelling. The cells have a definite polarization obtained during the switch phase and will retain that, however the adjacent cells (those which are not in the hold phase) are influenced.

In Release phase the potential barriers start lowering, electrons get free from the confinement and the cells lose their polarization. In this state the cells don't affect neighbouring cells computational state.

Relax phase follows the release phase of same clock cycle and is followed by the switch phase of next clock cycle. This is the inversion phase of hold in the sense that the potential barriers are completely lowered and electrons are free of confinement. This accounts for the meta-state of cell; at this phase the cells don't influence other cells.

Each clock zone amounts for delay of 0.25 of the clock cycle.

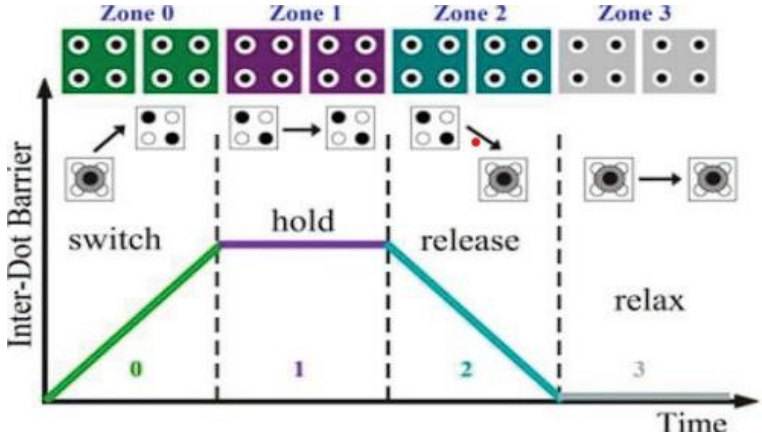

Figure 1.6: QCA Clock Phases

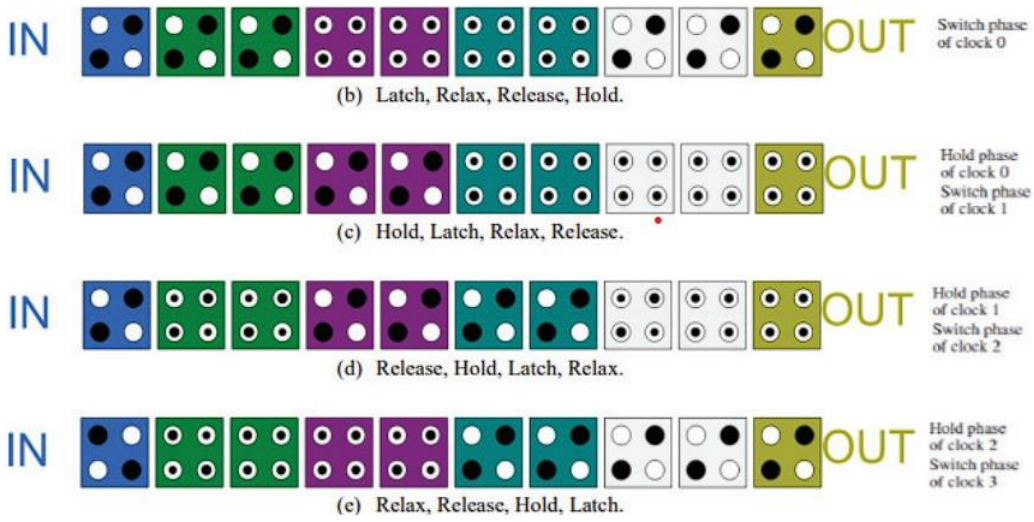

Figure 1.7: Clock Phase Description

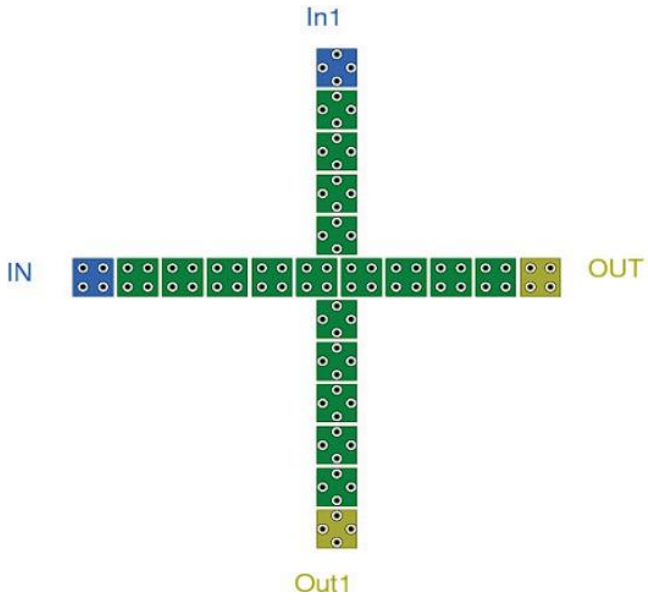

Figure 1.8: Wire Crossover OR Wire intersection

Chapter 2

LITERATURE SURVEY

Using the quantum states of the electrons in quantum dots, QCA functions according to the laws of quantum mechanics. Quantum dots (qubits) are used in QCA to represent binary information as bits. Four quantum dots stacked in a square pattern make up a QCA cell. These dots' charge distributions show binary states (0 or 1). The QCA cells' internal charge transport is controlled by Coulombic interactions and quantum tunneling. QCA cells are able to process information and carry out logical operations because of their unique charge configuration. This study serves as the foundation for our project and suggests QCA as an alternative to MOS technology.[1]

CMOS technology is founded on the application of complementary field-effect MOSFETs, which are made up of layers of semiconductor, oxide, and metal. The paper demonstrates the equivalent and geometric scaling of planar and fin MOSFETs, as well as their potential and constraints. The fundamentals of CMOS technology are provided for a range of devices and development phases. The technological limit of planar CMOS technology during the last ten years is demonstrated, as well as the economic and technical bounds of Moore's Law. This analytical overview stresses the need for an alternative semi-conductor Technology.[2]

In order to overcome CMOS limitations, spintronic logic uses magnetization for ultra-low voltage but has inefficient charge-to-spin conversion. With the new multiferroic oxide, the magneto-electric spin-orbit (MESO) technology promises 10–100× reduced switching energy than 2018 CMOS. The effective substitute, quantum dot cellular automata (QCA), presents itself with lower power consumption, quicker switching, and less leakage. QCA offers an attractive way to overcome traditional technological constraints in computing paradigm advancement, such as spintronics.[3]

Spintronic devices face challenges such as high energy dissipation, demanding solutions like enhanced Voltage-Controlled Magnetic Anisotropy(VCMA) coefficients. Quantum Dot Cellular Automata (QCA) technology can potentially address these challenges by offering energy-efficient computation and compact structures. QCA's ability to perform low-power, high-speed operations makes it a candidate for resolving the energy consumption issues associated with spintronics. [4]

The study proposes Chemically Assembled Electronic Nanotechnology (CAEN), a type of electronic nanotechnology that builds nanometer-scale electronic circuits by harnessing quantum-mechanical processes through self-alignment, as an alternate remedy. Nanoscale technologies employ quantum mechanics to compute, it comprise single-electron transistors, nanowire transistors, quantum dots, and more. We have incorporated QCA into our project through the physical and architectural use of Nana-scale technologies mentioned in the above paper. [5]

As devices get smaller, CMOS technology must contend with issues like power consumption, structural variances, leakage currents, and electron tunnelling. prospective remedies include carbon nanotubes (CNTs), whose strength from sp2 bonding reduces tunnelling and whose excellent thermal conductivity and stability point to their prospective application as interconnects in the future, which will lessen secondary effects. With its low power consumption and negligible electron scattering, QCA—which relies on electron tunnelling between quantum dots—offers faster charge movement than CMOS or CNFETs, improved signal propagation, and decreased heat dissipation. QCA as a possible remedy to overcome the limits of CMOS and CNTs in next electrical systems. [6]

The reference book covers a number of cutting-edge computer technologies, including optical, DNA, and quantum-dot cellular automata. It features tutorials on a CAD tool that will be very helpful to novices, along with examples that explain things. We have designed a multi-bit comparator by referring the above book.[7]

Chapter 3

Motivation, Problem definition and Methodology

3.1 MOTIVATION:

The continual pursuit of smaller, faster, and more energy-efficient electronic devices faces significant hurdles with the inherent limitations of traditional Complementary Metal-Oxide-Semiconductor (CMOS) technology at the nano-scale level. These limitations include challenges related to quantum mechanical behaviour, unexpected results at low currents, and design complexity, restricting further size reduction of transistors beyond 10 nm. The need for a transformative technology that overcomes these limitations and aligns with the demands of contemporary computing and communication applications is evident.

3.2 PROBLEM DEFINATION:

3.2.1 AIM

To implement multiple gates and combinational circuits in QCA Technology and to display the simulation results.

3.2.2 OBJECTIVE:

Circuit implementation of :

1. NOT GATE
2. MAJORITY GATE
3. AND GATE
4. NAND GATE
5. OR GATE
6. NOR GATE
7. XOR GATE
8. FULL ADDER

9. MULTIPLEXER

10. COMPARATOR

3.3 Methodology

Circuit implementation in QCA designer:

- Utilize QCA Designer software to design and simulate various logic gates and combinational circuits using Quantum-dot Cellular Automata (QCA) technology.
- Follow the QCA Designer's user interface to create the layout of each circuit, taking into account the unique properties and constraints of QCA technology.
- Validate the functionality of each circuit through simulation and analyze the results to ensure correctness.

Chapter 4

DESIGN AND IMPLEMENTATION

4.1 NOT GATE: The output is the complement of the input provided to the gate.

4.1.1 QCA Circuit:

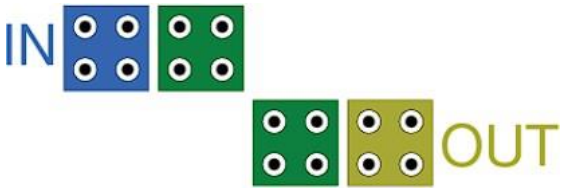

Fig. 4.1.1 QCA Not Gate

A	Z
0	1
1	0

Fig. 4.1.2 Truth Table

4.1.2 QCA Designer Simulation:

NOT Gate be made by QCA cells by inverting the position of electrons in QCA cell , so that input logic '0' will result as output '1' and input logic '1' will result as output '0' as shown below.

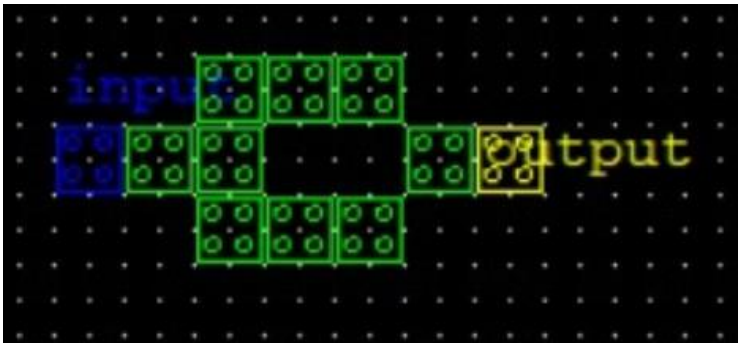

Fig. 4.1.3. QCA Not gate in QCA Designer

Fig. 4.1.4 QCA Not gate Output in QCA Designer

44.2 MAJORITY GATE:

The gate has three inputs and the output is same as the input that is present in majority.

4.2.1 QCA Circuit:

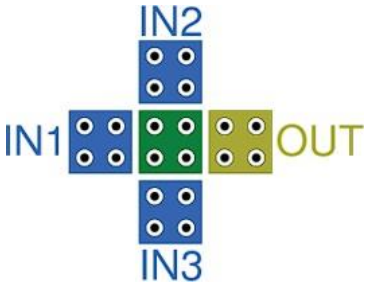

Fig. 4.2.1 QCA Majority Gate

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 4.2.2 Majority Gate Truth Table

4.2.2 QCA Designer Simulation: The majority gate serves as a fundamental component for constructing various logic gates within QCA circuits. In essence, it determines the output based on the most frequently occurring digit in the input. For instance, when the input is "001", the majority gate yields an output of "0", indicating the prevalent digit in the input. Likewise, for input "111", the majority gate produces an output of "1", reflecting the dominant digit within the input sequence.

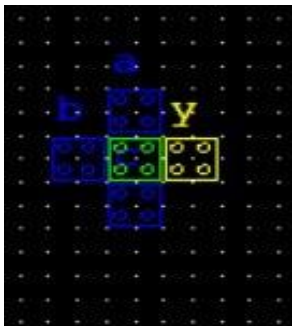

Fig. 4.2.3 QCA Majority Gate in QCA Designer

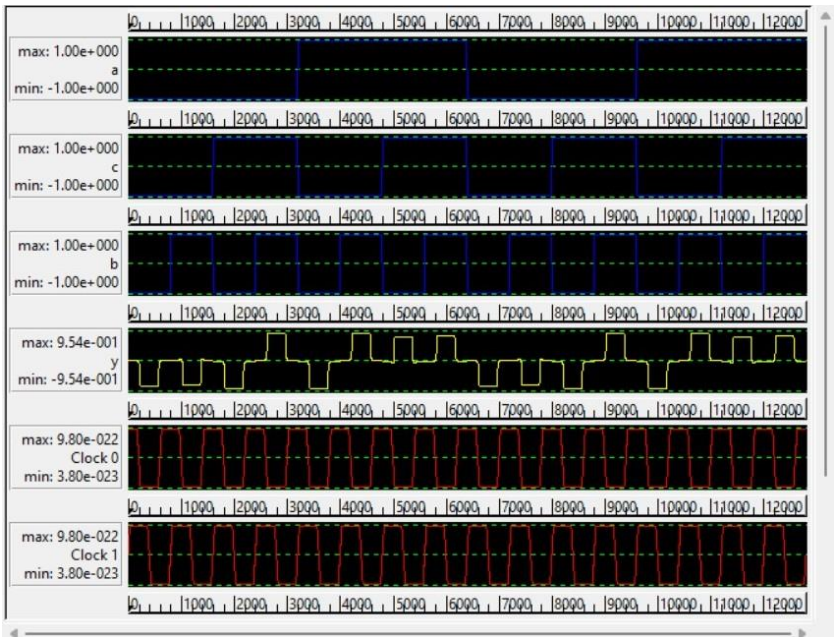

Fig. 4.2.4 QCA Majority Gate Simulation Results

4.3 AND GATE:

Using the above mentioned basic building blocks, i.e., Wires, Inverter and Majority gate, we will now design logic gates in the next section of this paper**.** AND gate performs the AND operation (O=A.B). The output is high (1) only when all the inputs are high.

4.3.1 QCA Circuit:

By fixing one of the inputs of three-input MV gate to logic '0', we can have a Two-input AND function realization as shown in Fig. 4.3.1. . When all input cells are in the high state, the output cells align to produce a high output; otherwise, the output remains low.

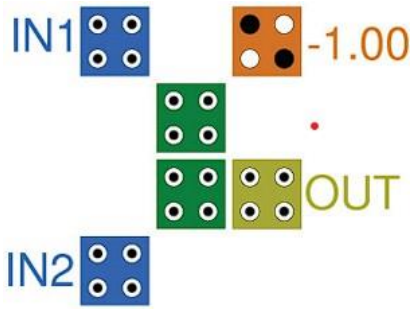

Fig. 4.3.1 QCA And Gate

Truth Table		
B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 4.3.2 Truth Table

4.3.2 QCA Designer simulation:

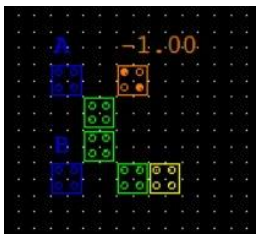

Fig. 4.3.3 QCA And Gate in QCA Designer

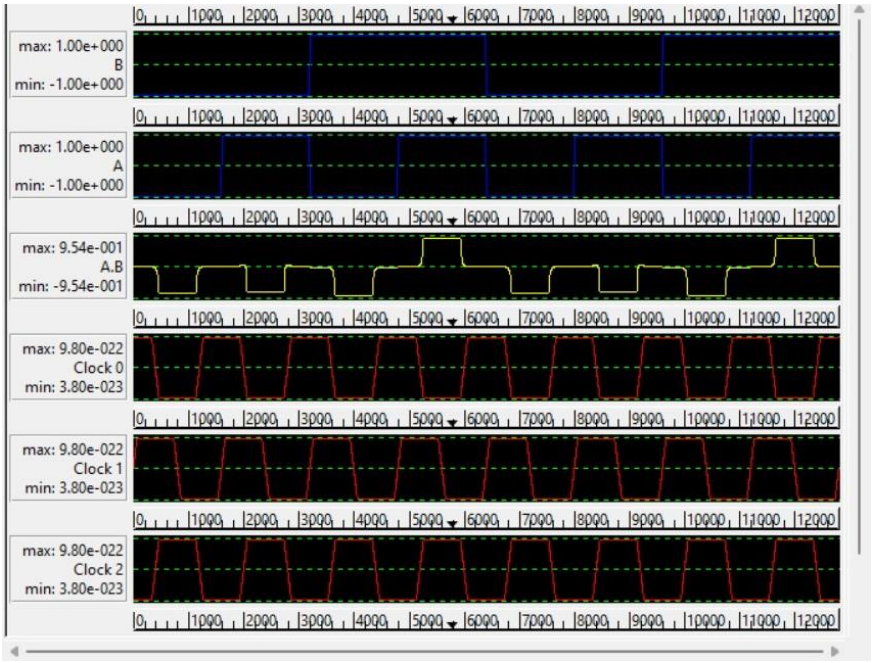

Fig. 4.3.4 QCA And Gate Simulation Results

4.4 NAND GATE:

NAND gate is the inverted AND gate and the outputs are compliments of the respective AND gate outputs. It has one constant input at polarization -1

4.4.1 QCA Circuit: By inserting inverter to the output of AND gate, NAND gate can be designed as shown in Fig. 4.4.1

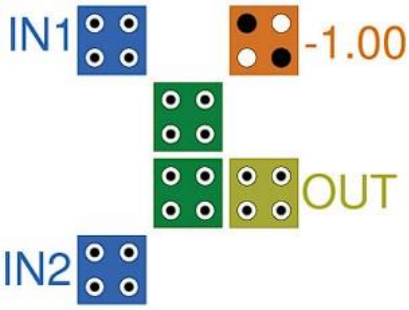

Fig. 4.4.1 QCA Nand Gate

Truth Table		
B	A	Q
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 4.4.2 Truth Table

4.4.2 QCA Designer simulation:

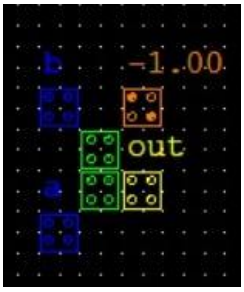

Fig. 4.4.3 QCA Nand Gate in QCA Designer

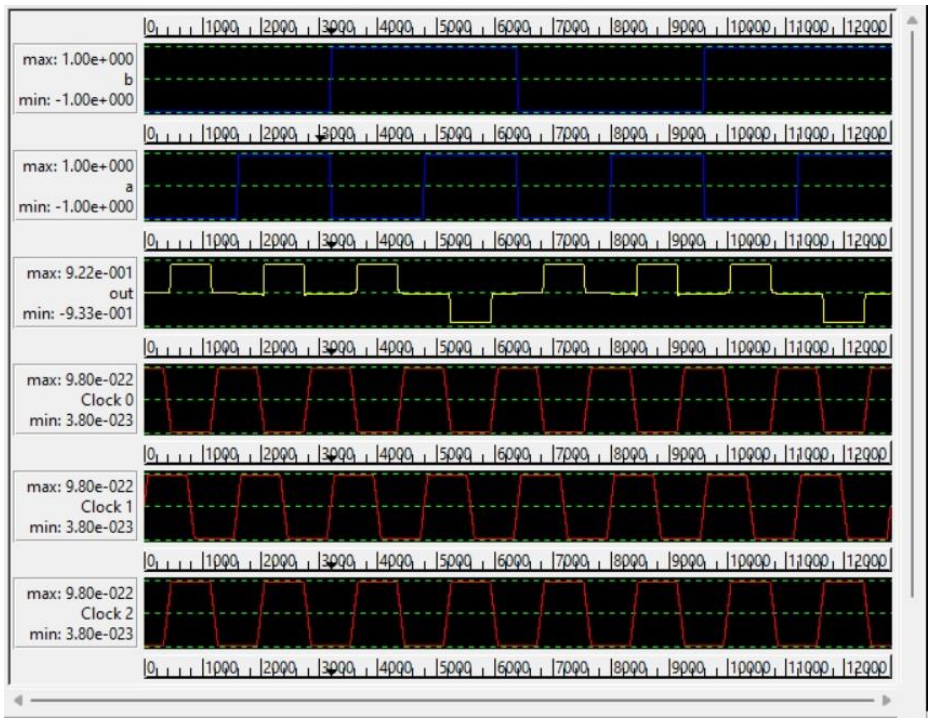

Fig. 4.4.4 QCA Nand Gate Simulation Results

4.5 OR GATE:

OR gate logic gives a high (1) output when any of the inputs is high (1), else low (0). It performs the OR operation on the inputs (O= A+B), it uses only 6 cells and has one ancilla input of polarization 1.

4.5.1 QCA Circuit: Looking into the design of Two-Input OR gate, we see that when a Three input MV gate has one of its inputs fixed to logic '1', the output function obtained is OR function. This is as shown in Fig. 4.5.1 below.

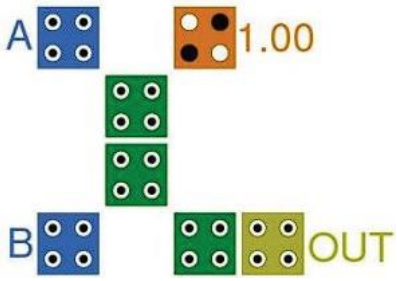

Fig. 4.5.1 QCA OR Gate

Truth Table		
B	A	Q
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 4.5.2 Truth Table

4.5.2 QCA Designer simulation:

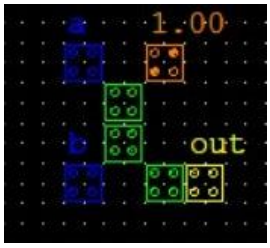

Fig. 4.5.3 QCA OR Gate in QCA Designer

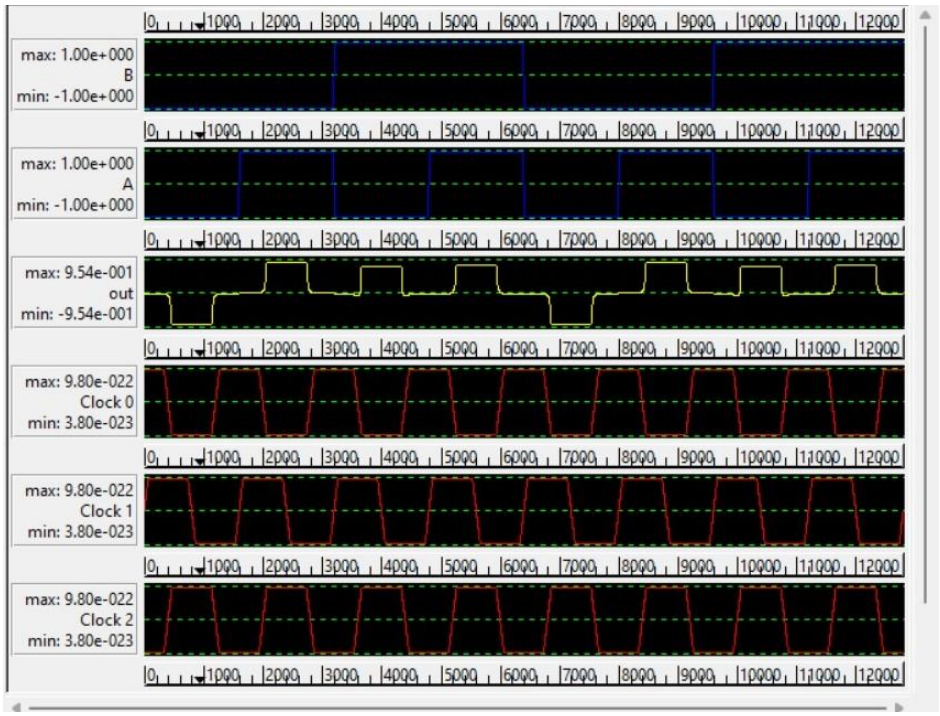

Fig. 4.4.4 QCA OR Gate Simulation Results

4.6 NOR GATE:

NOR gate is the complement gate of OR gate, it gives output high (1) only when either none of the inputs is high (1) or all the inputs are high.

4.6.1 QCA Circuit: NOR gate can be designed by inserting inverter to the output of OR gate, NOR gate can be created as shown in Fig. 4.6.1

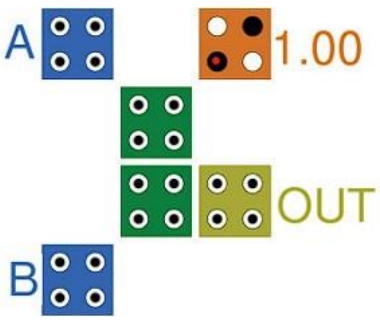

Fig. 4.6.1 QCA NOR Gate

Truth Table		
B	A	Q
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 4.6.2 Truth Table

4.6.2 QCA Designer simulation:

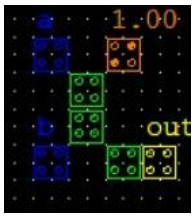

Fig. 4.6.3 QCA NOR Gate in QCA Designer

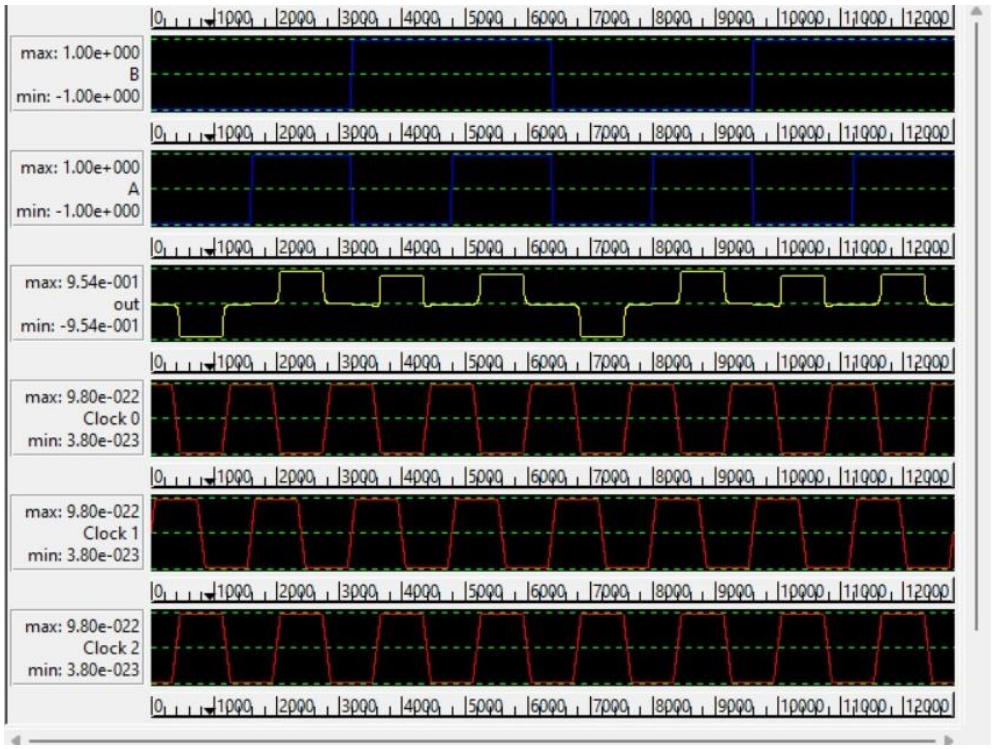

Fig. 4.6.4 QCA NOR Gate Simulation Results

4.7 XOR GATE:

The gate performs XOR operation and gives a high (1) output only when the inputs are different and not same.

4.7.1 QCA Circuit: It produces a high output if the number of high inputs is odd, making it useful for arithmetic and cryptographic applications.

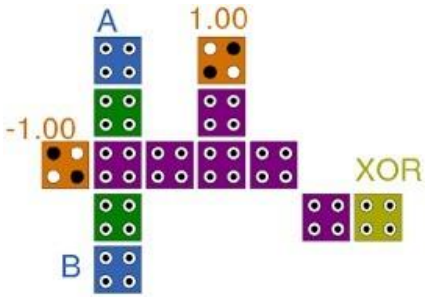

Fig. 4.7.1 QCA XOR Gate

Truth Table		
B	A	Q
0	0	0
0	1	1
1	0	1
1	1	0

Fig.4.7.2 Truth Table

4.7.2 QCA Designer simulation:

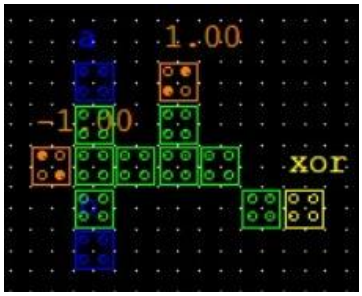

Fig. 4.7.3 QCA XOR Gate in QCA Designer

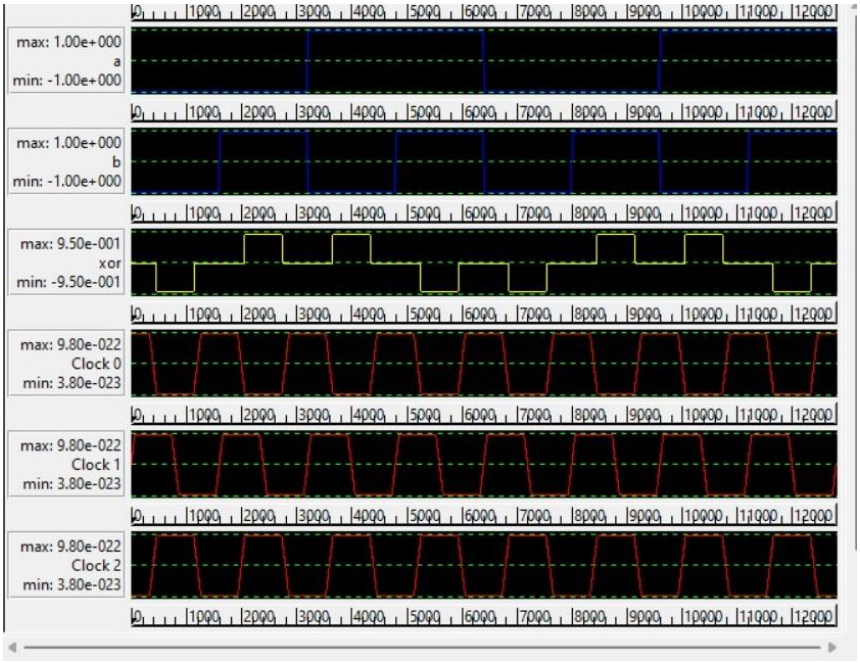

Fig. 4.7.4 QCA XOR Gate Simulation Results

4.8 FULL ADDER:

The full adder is a combinational logic circuit that takes in three inputs: a, b, and a carry-in input (cin). It produces two outputs: the sum (sum), which is the result of adding a, b, and the carry-in, and the carry-out (carry), which indicates if there's a carry-over from the addition operation.

4.8.1 QCA Circuit:

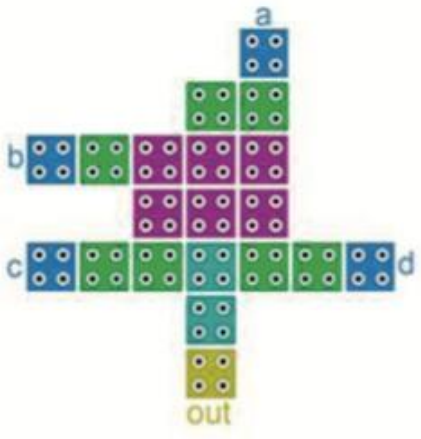

Fig. 4.8.1 QCA Full Adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig.4.8.2 Truth Table

4.8.2 QCA Designer simulation:

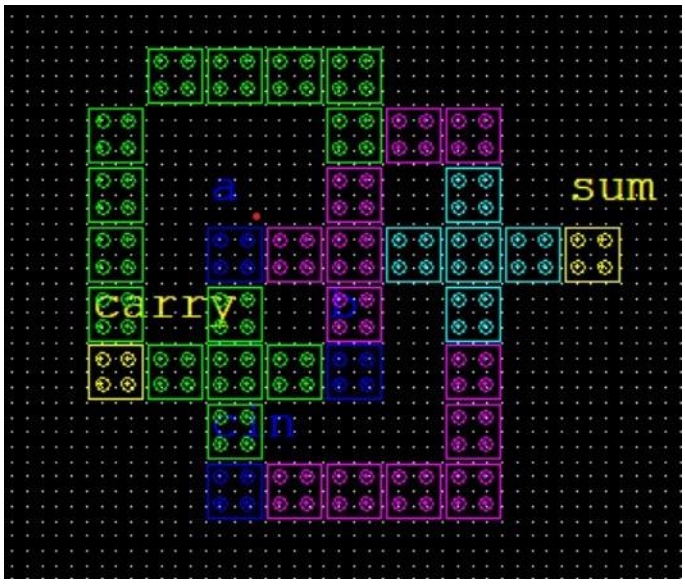

Fig. 4.8.3 QCA XOR Gate in QCA Designer

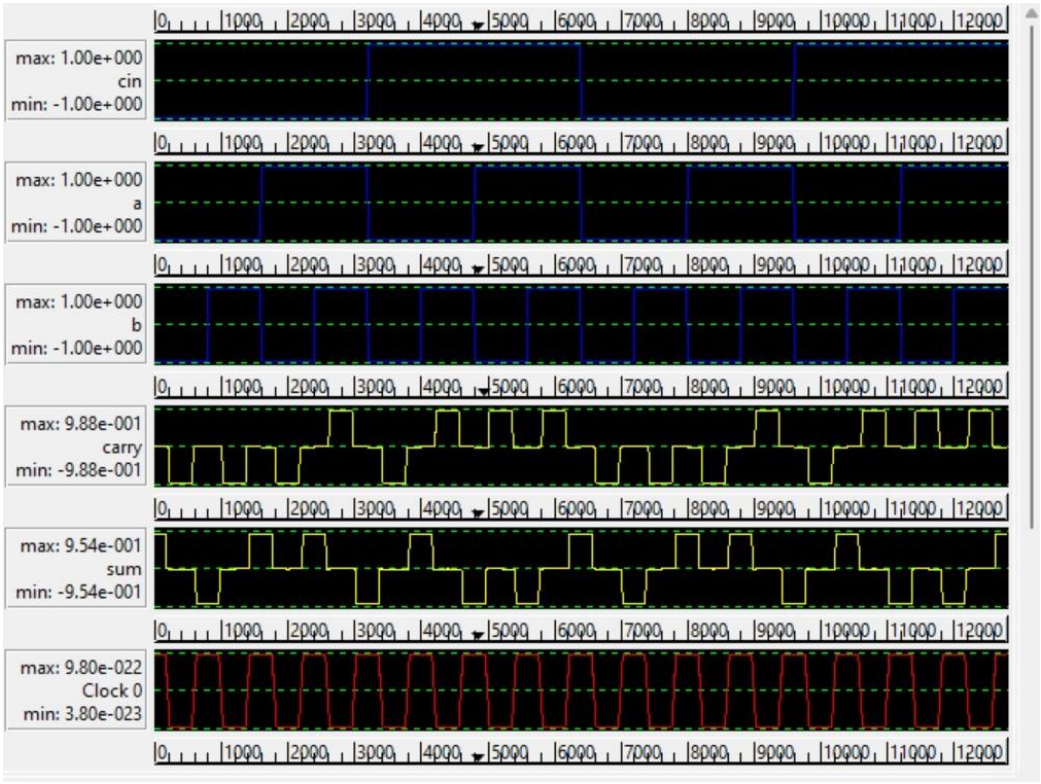

Fig. 4.7.4 QCA XOR Gate Simulation Results

4.9 2X1 MULTIPLEXER:

In a 2×1 multiplexer implemented in Quantum-dot Cellular Automata (QCA) technology, there are two input lines, denoted as A and B, one selection line labeled S, and a single output line, denoted as OUTPUT. Depending on the state of the selection line S, one of the two input lines will be connected to the output line OUTPUT. This behavior is determined by the configuration of cells in the QCA layout corresponding to the states of the selection line.

4.9.1 QCA Circuit: The following figure shows the implementation of 2X1 Mix using 3 majority gates and one inverter.[9]

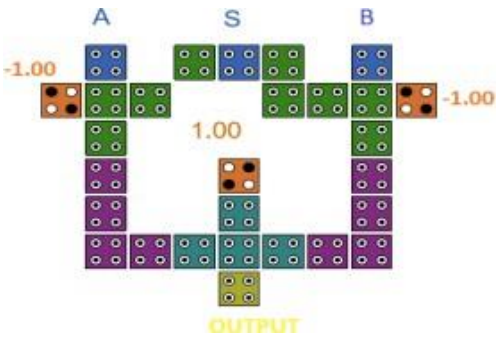

Fig.4.8.1 QCA 2X1 MUX

Select	Inputs		Output
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

Fig. 4.8.2 Truth Table

4.9.2 QCA Designer simulation:

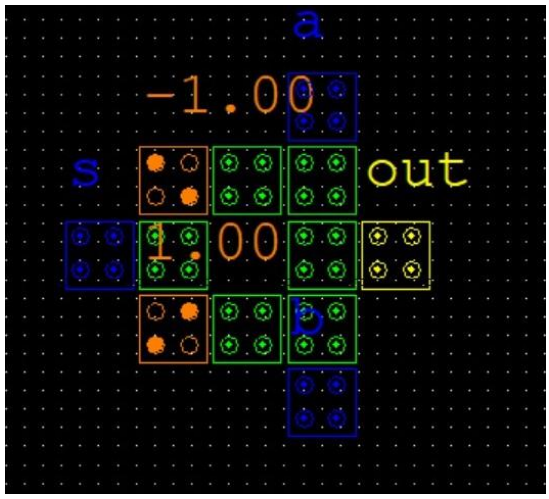

Fig. 4.9.3 QCA 2X1 Mux in QCA Designer

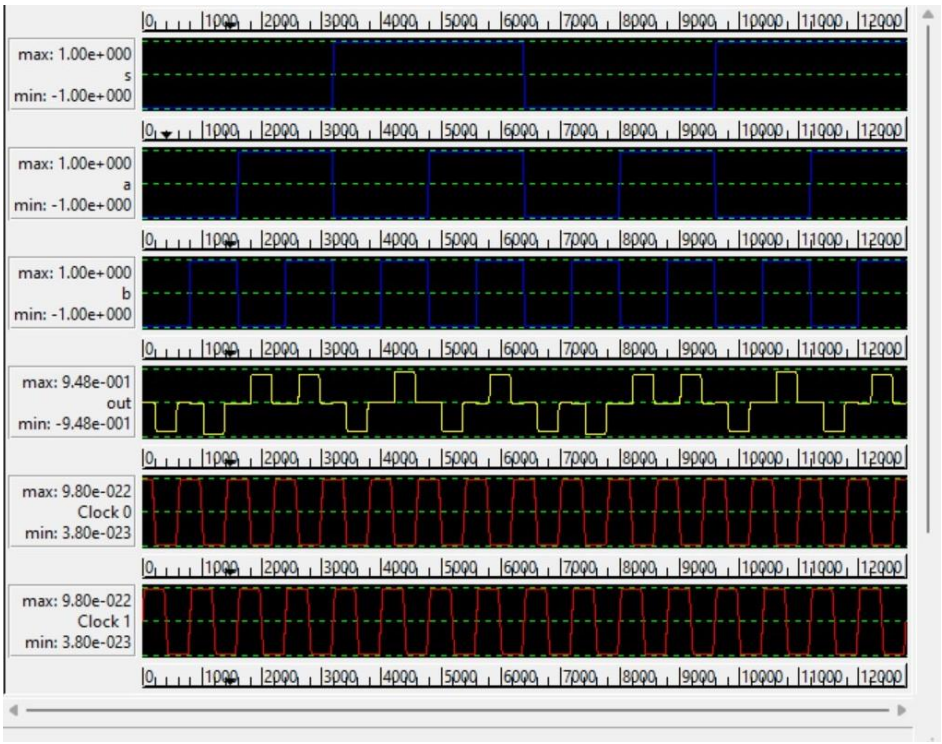

Fig. 4.9.4 QCA 2X1 Mux Simulation Results

4.10 1-bit Comparator:

A comparator is a combinational circuit designed to analyze two binary numbers, determining their relationship: whether one number is equal to, less than, or greater than the other. The circuit has two inputs, designated for A and B respectively, and three output terminals: one for indicating when A is greater than B, one for when A equals B, and one for when A is less than B.

4.10.1 QCA Circuit: 1- bit comparator is designed using two majority(3 input) gate and one xor gate. Input for the first Majority gate will be A, B and -1. Input for the second majority gate will be the same as first. And input for the xor will be A and B.[8]

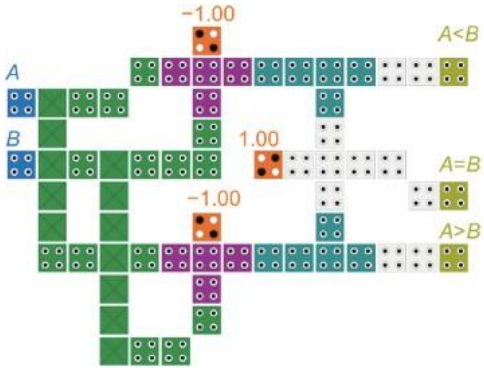

Fig.4.10.2 1-bit Comparator

A	B	A=B	A<B	A>B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

Fig.4.10.2 Truth Table

4.10.2 QCA Designer simulation:

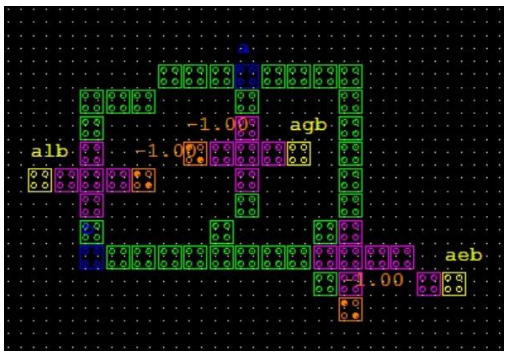

Fig. 4.9.3 QCA 1-bit Comparator in QCA Designer

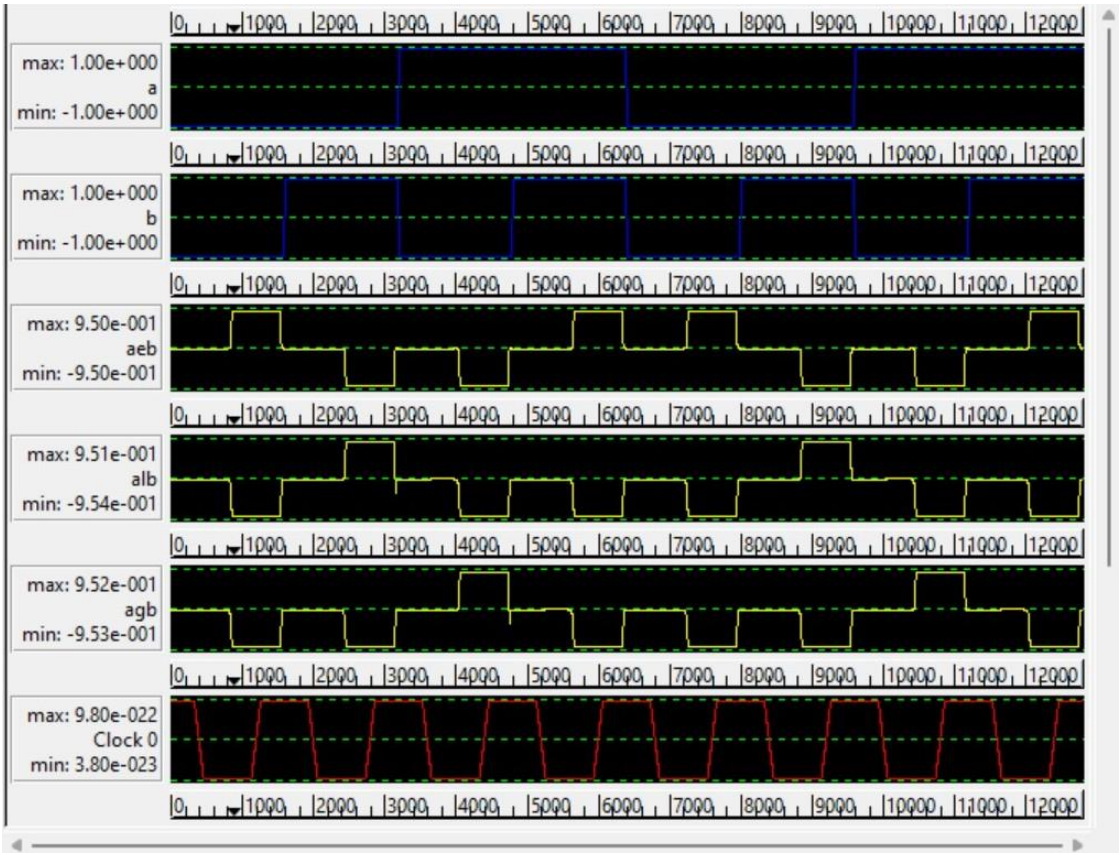

Fig. 4.9.4 QCA 1-bit Comparator Simulation Results

Chapter 5

CONCLUSION

Design of combinational circuit has been carried out in QCA Designer. The design and implementation of QCA circuit is based on the polarity of the cellular automata. The clock phases, which includes the switch phase, the hold phase, release phase and relax phase each have a distinct function which must be included in the design for smooth and functional operation of the circuit.

A simple comparative analysis was done manually and in cadence software to show that QCA has better timing parameters and size parameters than MOSFET circuit. There are multiple design problems encountered throughout the process. Mainly the way to use the clock phases to trigger the different parts of the circuit.

There is no way to utilise the circuit whose functionality has already been already realised we cannot use the concepts of and gate or OR gate in the subsequent circuit. This proves as a challenge as independent analysis of the circuit and the polarity propagation has to be considered

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[9] Design and analysis of (2x1) and (4x1) Multiplexer circuit in Quantum Dot Cellular Automata

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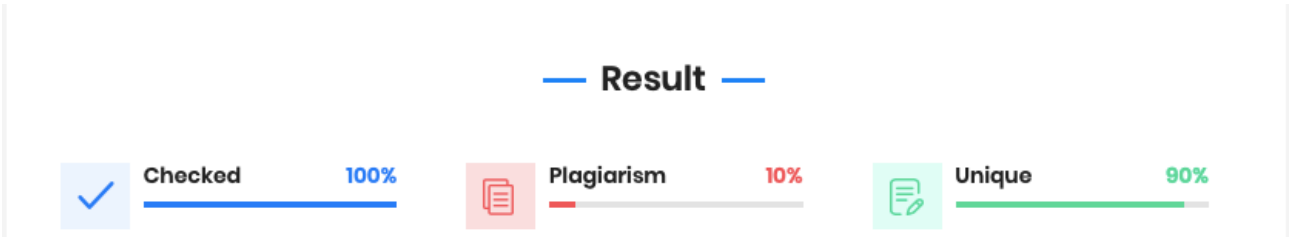

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There has been a constant evolution from first computer starting from electro-mechanical switches and relays to vacuum tubes triodes, to transistors and the current era Metal Oxide Field-Effect Transistor(MOSFETs). Each evolution has had a significant improvement in computational and power parameters compared to its previous generation technology. According to Moore's law number of transistors in a chip doubles after every 18 months, but seeing the current trend and the "MOS" technology limitations it will reach a saturation.
There is a need to research and develop other avenues of semiconductor industry. QCA is found to be most feasible, efficient and advantageous in terms of parallelism, implementation, accuracy, computation and area on chip. In this paper QCA as a technology and its implementation in semiconductor industry is discussed. In this paper construction and design of basic gates, wires and clocking cycles using QCA has been comprehensively discussed.
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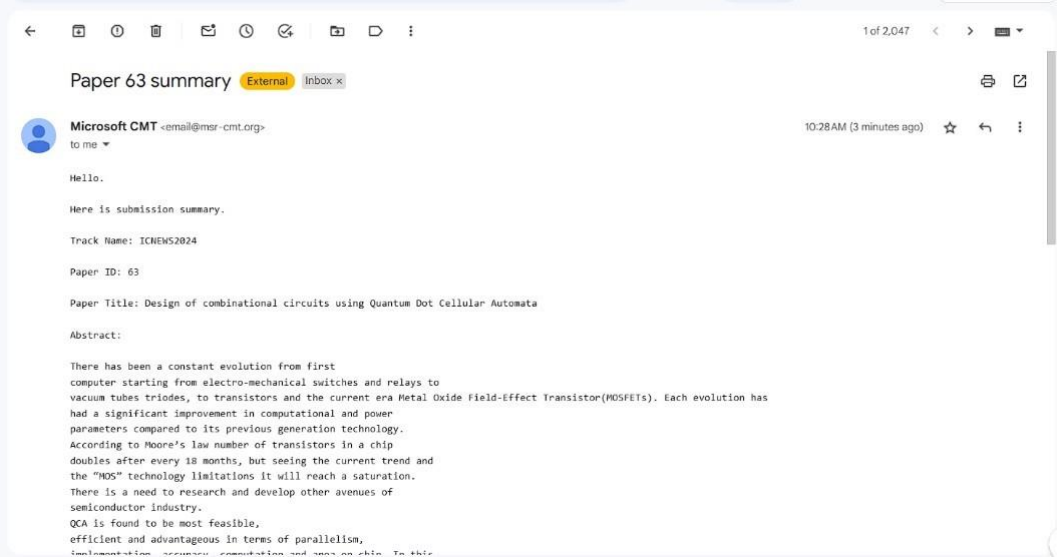

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