“Design of combinational Circuits using Quantum-dot Cellular Automata Technology”

Lochan G

Electronics and Communication Engineering
B.M.S college of Engineering
Banglore, India
lochan.ec21@bmsce.ac.in

Dhanush D

Electronics and Communication Engineering
Electronics and Communication Engineering
Banglore, India
dhanush.ec21@bmsce.ac.in

Eshwar Bevoor

Electronics and Communication Engineering
Electronics and Communication Engineering
Banglore, India
eshwar.ec21@bmsce.ac.in

Hanumesh V Burli

Electronics and Communication Engineering
Electronics and Communication Engineering
Banglore, India
hanumesh.ec21@bmsce.ac.in

Abstract— There has been a constant evolution from first computer starting from electro-mechanical switches and relays to vacuum tubes triodes, to transistors and the current era Metal-Oxide Field-Effect Transistor(MOSFETs). Each evolution has had a significant improvement in computational and power parameters compared to its previous generation technology. According to Moore’s law number of transistors in a chip doubles after every 18 months, but seeing the current trend and the “MOS” technology limitations it will reach a saturation. There is a need to research and develop other avenues of semiconductor industry.

There have been many proposals and researches on “beyond CMOS” technology, among which Spin Wave Devices, Nano-Magnetic Logic and Quantum Dot Cellular Automata (QCA) are the most feasible solutions. QCA is found to be most feasible, efficient and advantageous in terms of parallelism, implementation, accuracy, computation and area on chip. In this paper QCA as a technology and its implementation in semiconductor industry is discussed. In this paper construction and design of basic gates, wires and clocking cycles using QCA has been comprehensively discussed.

Keywords—MOSFETs, Moore’s law, CMOS, Nano-Magnetic Logic, Spin Wave Devices, QCA, clocking cycles.

I. INTRODUCTION

Quantum dots are tiny semiconductor particles that can be as small as a few nanometers in diameter. They are often referred to as artificial atoms due to their unique electronic properties, which are somewhat similar to those of individual atoms. Quantum dots are very small, typically ranging from 2 to 10 nanometers in diameter. Because of their small size, they exhibit quantum mechanical properties that are not observed in larger materials. Quantum dots exhibit Quantum Confinement where Quantum dots confine the motion of electrons and holes (electron vacancies) within their structure. This confinement leads to discrete energy levels, similar to those observed in atoms. This property makes Quantum dots a fascinating nano material with multiple desirable tunable properties.

Cellular Automata (CA) is an attractive emerging technology that takes advantage of quantum effects, which become increasingly apparent at the scale of a few nanometers. A QCA is a square nanostructure of electron wells confining free electrons. Each cell has four quantum dots which can hold a single electron per dot. The physical representation of a Quantum Dot Cellular Automata.

II. QCA BASICS

A. THE 90 DEGREE QCA CELL:

The QCA cell has the four quantum dots at four corners of the square, the two electrons always take place at the diagonally opposite dots (to minimize Columbic Repulsion). This cell is mostly used in the design processes. It affects the next identical cell in a way that the next cell also imbibes the same polarization as the previous cell and not the inverted one. Maintaining the Integrity of the Specifications

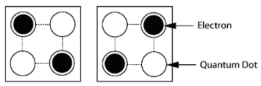


Fig. 1. 90 DEGREE QCA CELL

B. THE 45 DEGREE QCA CELL:

The 45degree QCA is also known as rotated QCA cell. The cell identical in operation to the 90degree cell but the location of metal islands within the cells differentiates the two. This also ensures the presence of electrons at the least interaction locations.

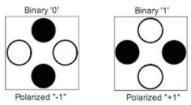


Fig. 2. 45 DEGREE QCA CELL

C. QCA WIRE:

QCA cells when placed in a tandem, one after another, form the QCA wire. The first cell of a wire is known as driver cell and the last cell is known as Ripper cell. The wire is properly clocked for proper propagation of data and for synchronization of input and output to different circuit parts.

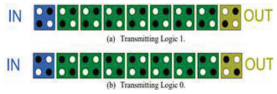


Fig. 3. Wire for 90 degree Cell

D. QCA CLOCK:

During the switch phase of clock, the energy barriers start raising and the cell attains a definite polarization based on the driving input and the polarization of neighbouring cells. The electrons get confined in the 3-d space of the quantum dot. In the hold phase, of QCA clock, the potential barriers retain the higher value, the energy walls are greater and proscribes electrons from tunnelling. The cells have a definite polarization obtained during the switch phase and will retain that, however the adjacent cells (those which are not in the hold phase) are influenced. In Release phase the potential barriers start lowering, electrons get free from the confinement and the cells lose their polarization. In this state the cells don't affect neighbouring cells computational state. Relax phase follows the release phase of same clock cycle and is followed by the switch phase of next clock cycle. This is the inversion phase of hold in the sense that the potential barriers are completely lowered and electrons are free of confinement. This accounts for the meta-state of cell; at this phase the cells don't influence other cells.

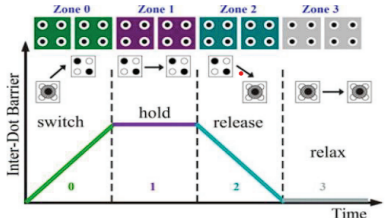


Fig. 4. QCA Clock Phases

III. GATE DESIGN IN QCA AND SIMULATION RESULTS

A. NOT GATE

The inverter or NOT gate can be implemented using QCA by placing two QCA cells at 45 degrees with respect to each other such that they interact inversely. Using QCA Designer tool the following simulations were done:

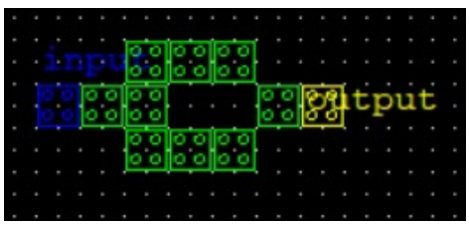
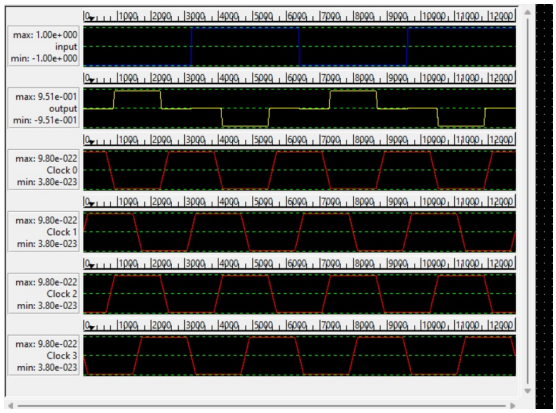


Fig. 5. NOT Gate



.

Fig. 6 QCA NOT Gate Simulation Results

B. MAJORITY GATE

Majority gate is designed by arranging five QCA cells in cross patterns, shown in Figure 2. Depending on majority of inputs the majority gate produces the output. This majority gate forms the basic building block to implement various logic gates in QCA circuits. For example if the input provided to majority gate is "001", then output is "0" which indicates the maximum digit repetition in the input. Similarly for input "111", output of majority gate is "1" and so on. In general, the majority gate takes inputs in odd number to produce an output.

Fig. 7. MAJORITY Gate

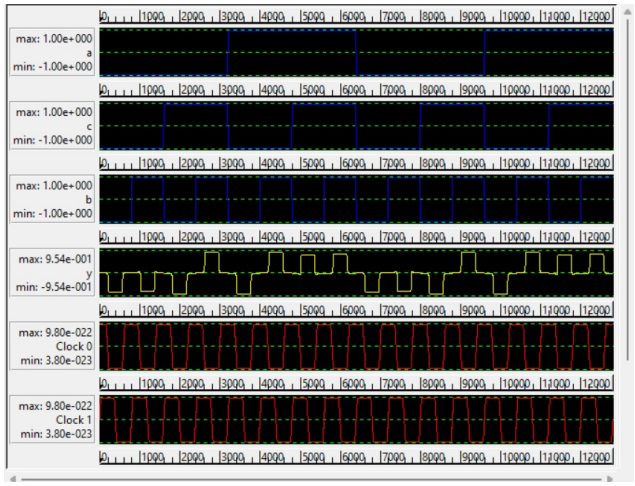


Fig. 8 QCA MAJORITY GATE Simulation Results

C. 2X1 MULTIPLEXER:

In a 2×1 multiplexer implemented in Quantum-dot Cellular Automata (QCA) technology, there are two input lines, denoted as A and B, one selection line labeled S, and a single output line, denoted as OUTPUT. Depending on the state of the selection line S, one of the two input lines will be connected to the output line OUTPUT. This behavior is determined by the configuration of cells in the QCA layout corresponding to the states of the selection line.

The following figure shows the implementation of 2X1 Mix using 3 majority gates and one inverter.[9]

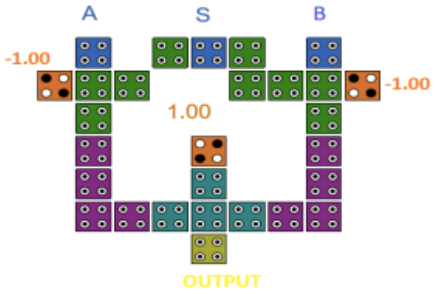


Fig. 9. QCA 2X1 MUX

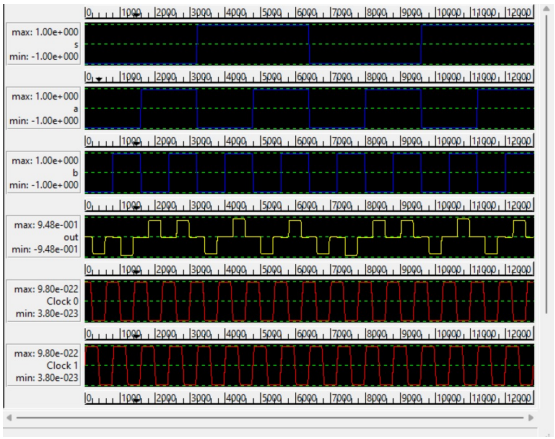


Fig.10 QCA 2X1 Mux Simulation Results

D. 1-BIT COMPARATOR:

A comparator is a combinational circuit designed to analyze two binary numbers, determining their relationship: whether one number is equal to, less than, or greater than the other. The circuit has two inputs, designated for A and B respectively, and three output terminals: one for indicating when A is greater than B, one for when A equals B, and one for when A is less than B.

1- bit comparator is designed using two majority(3 input) gate and one xor gate. Input for the first Majority gate will be A, B and -1. Input for the second majority gate will be the same as first. And input for the xor will be A and B. [8]

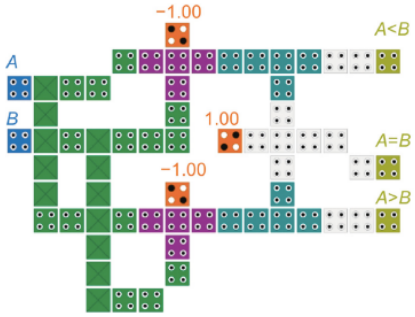


Fig. 11. QCA 1-bit comparator

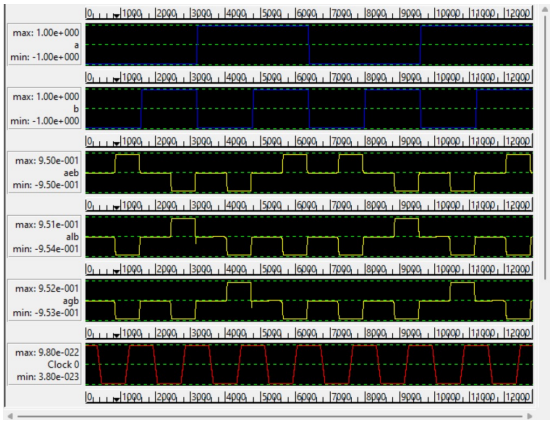


Fig.12 QCA 1-bit comparator

E. XOR GATE:

The XOR gate is a base unit for designing arithmetic circuits. Fig. 5 illustrates the structure of 2 input XOR Gate. The design has only eight QCA cells, a latency of two clock phases and only 0.0066μm^2 of area. XOR gate can be created by using logic implementation shown in

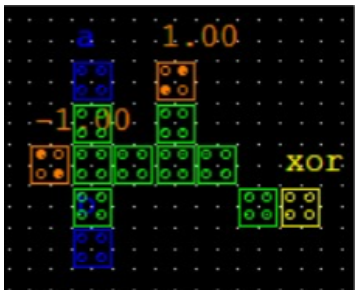


Fig. 13. XOR Gate

It produces a high output if the number of high inputs is odd, making it useful for arithmetic and cryptographic applications.

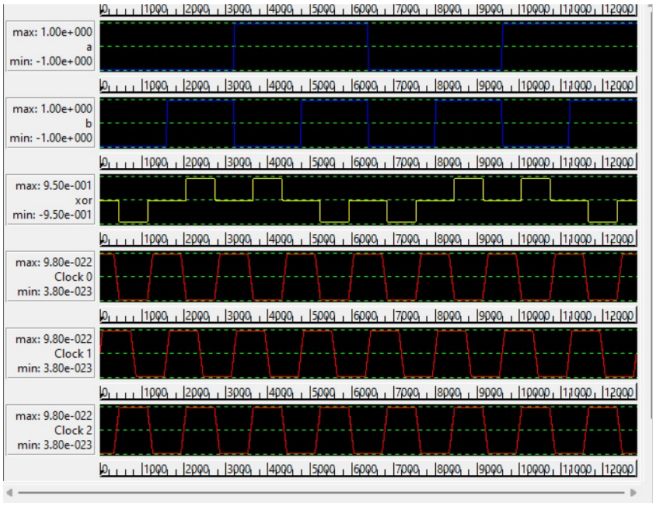


Fig. 14 QCA XOR Gate Simulation Results

F. AND GATE:

Using the above mentioned basic building blocks, i.e., Wires, Inverter and Majority gate, we will now design logic gates in the next section of this paper**.** AND gate performs the AND operation (O=A.B). The output is high (1) only when all the inputs are high.

By fixing one of the inputs of three-input MV gate to logic '0', we can have a Two-input AND function realization as shown in Fig.15 When all input cells are in the high state, the output cells align to produce a high output; otherwise, the output remains low.

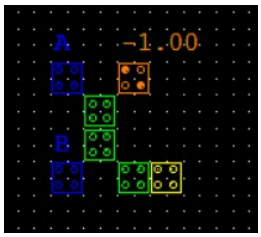


Fig. 15 QCA And Gate in QCA Designer

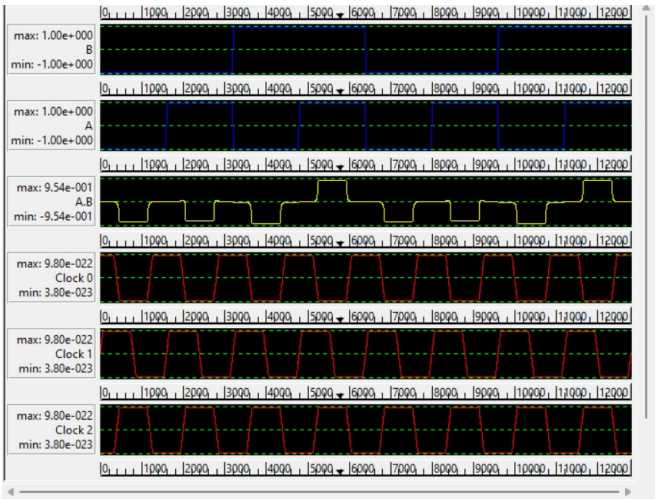


Fig. 16 QCA And Gate Simulation Results

G. OR GATE:

OR gate logic gives a high (1) output when any of the inputs is high (1), else low (0). It performs the OR operation on the inputs (O= A+B), it uses only 6 cells and has one ancilla input of polarization 1.

Looking into the design of Two-Input OR gate, we see that when a Three input MV gate has one of its inputs fixed to logic '1', the output function obtained is OR function. This is as shown in Fig. 17 below.

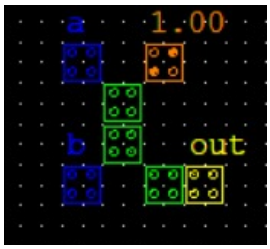


Fig. 17 QCA OR Gate in QCA Designer

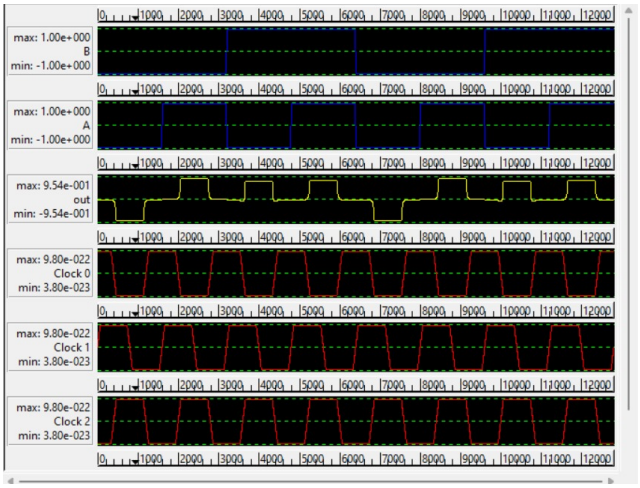


Fig. 18 QCA OR Gate Simulation Results

H. NOR GATE:

NOR gate is the complement gate of OR gate, it gives output high (1) only when either none of the inputs is high (1) or all the inputs are high.

NOR gate can be designed by inserting inverter to the output of OR gate, NOR gate can be created as shown in Fig. 19

Fig. 19 QCA NOR Gate in QCA Designer

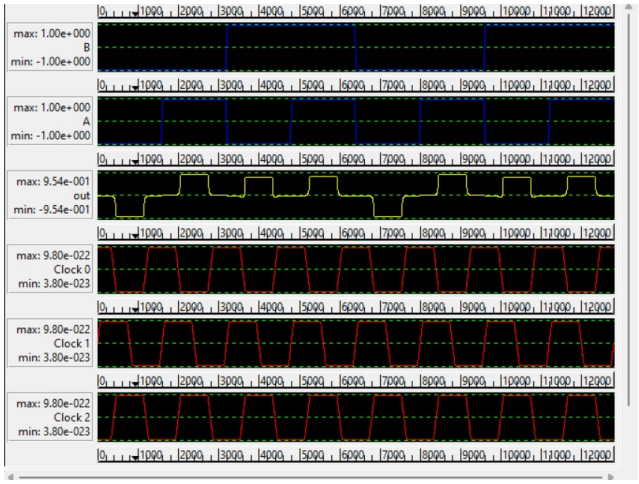


Fig. 4.6.4 QCA NOR Gate Simulation Results

IV. CONCLUSION:

Design of combinational circuit has been carried out in QCA Designer. The design and implementation of QCA circuit is based on the polarity of the cellular automata. The clock phases, which includes the switch phase, the hold phase, release phase and relax phase each have a distinct function which must be included in the design for smooth and functional operation of the circuit.

A simple comparative analysis was done manually and in cadence software to show that QCA has better timing parameters and size parameters than MOSFET circuit. There are multiple design problems encountered throughout the process. Mainly the way to use the clock phases to trigger the different parts of the circuit.

ACKNOWLEDGMENT *(Heading 5)*

This work would not have been possible without the support and the facilities of the Department of Mechanical Engineering, B. M. S. College of Engineering, Bengaluru as well as the comments and suggestions from the committee members of project work evaluation.

We are especially indebted to our guide and mentor **R.C Radha**, Professor, Department of Electronics and Communication Engineering, B. M. S. College of Engineering, Bengaluru, who has been supportive and instrumental in completing the academic goals in time.

We would like to express our sincere gratitude to the mini project coordinator, **Mrs Monika Sharma**, Assistant Professor, Department of Electronics and Communication Engineering, BMSCE, for the help rendered in learning the art of publishing.

We would like to thank our Head of the Department, **Dr. Siddappaji**, Professor & Head, Department of Electronics and Communication, B. M. S. College of Engineering, Bengaluru, and our Principal, **Dr. S. Muralidhara**, Principal, B. M. S. College of Engineering, Bengaluru.

.

REFERENCES

[1] Snider, G.L., Orlov, A.O., Kummamuru, R.K. et al. Quantum-dot Cellular Automata. MRS Online Proceedings Library 696, 76 (2001). https://doi.org/10.1557/PROC-696-N7.6

[2] Bespalov, V.A., Dyuzhev, N.A. & Kireev, V.Y. Possibilities and Limitations of CMOS Technology for the Production of Various Microelectronic Systems and Devices. Nanotechnol Russia 17, 24–38 (2022). https://doi.org/10.1134/S2635167622010037

[3] H. Liu et al., "Synchronous Circuit Design With Beyond-CMOS Magnetoelectric Spin–Orbit Devices Toward 100-mV Logic," in IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 5, no. 1, pp. 1-9, June 2019, doi: 10.1109/JXCDC.2019.2897598.

[4] Barla, P., Joshi, V.K. & Bhat, S. Spintronic devices: a promising alternative to CMOS devices. *J Comput Electron* **20**, 805–837 (2021). https://doi.org/10.1007/s10825-020-01648-6

[5] S. Copen Goldstein and M. Budiu, "NanoFabrics: spatial computing using molecular electronics," Proceedings 28th Annual International Symposium on Computer Architecture, Gothenburg, Sweden, 2001, pp. 178-189, doi: 10.1109/ISCA.2001.937446.

[6] Bajaj, Karishma & Gambhir, Shilpa & Singh, Shashank. (2016). CMOS Technology Vs Carbon Nano Scale FET's.

[7] Quantum-Dot Cellular Automata Based Digital Logic Circuits: A Design Perspective. Authors: Trailokya Nath Sasamal , Ashutosh Kumar Singh , Anand Mohan

[8] Ali Hussien Majeed, Mohd Shamian Zainal, Esam Alkaldy, Danial Md. Nor, Single-bit comparator in quantum-dot cellular automata (QCA) technology using novel QCA-XNOR gates, Journal of Electronic Science and Technology, Volume 19, Issue 3, 2021, 100078, ISSN 1674-862X, https://doi.org/10.1016/j.jnlest.2020.100078.

[9] Design and analysis of (2x1) and (4x1) Multiplexer circuit in Quantum Dot Cellular Automata, https://ijiet.com/wp-content/uploads/2019/08/16.pdf

[10] Hanckel, B., Petticrew, M., Thomas, J. *et al.* The use of Qualitative Comparative Analysis (QCA) to address causality in complex systems: a systematic review of research on public health interventions. *BMC Public Health* **21**, 877 (2021). https://doi.org/10.1186/s12889-021-10926-2

[11]Smita C. Chetti, Omkar Yatgal, QCA: A survey and design of logic circuits, Global Transitions Proceedings,

Volume 3, Issue 1, 2022, Pages 142-148, ISSN 2666-285X, https://doi.org/10.1016/j.gltp.2022.04.012

[12] Majeed, Ali & Zainal, Shamian & Alkaldy, Esam. (2019). Quantum-dot Cellular Automata: Review Paper. 11. 143-158.

[13] M. Naji Asfestani and S. Rasouli Heikalabad, "A novel multiplexer-based structure for random access memory cell in quantum-dot cellular automata," Physica B: Condensed Matter, vol. 521, pp. 162-167, 2017.

[14] F. Ahmad, "An optimal design of QCA based 2 n :1/1:2 n multiplexer/demultiplexer and its efficient digital logic realization," Microprocessors and Microsystems, vol. 56, pp. 64-75, 2018.

[15] A. Sadoghifar and S. R. Heikalabad, "A Content-Addressable Memory structure using quantum cells in nanotechnology with energy dissipation analysis," Physica B: Condensed Matter, vol. 537, pp. 202-206, 2018.

[16] I. Amlani, A. Orlov, R. Kummamuru, G. Bernstein, C. Lent, and G. Snider, “Experimental demonstration of a leadless quantum-dot cellular automata cell,” Applied Physics Letters, vol. 77, no. 5, pp. 738– 740, 2000.

[17] A. Orlov, I. Amlani, G. Bernstein, C. Lent, and G. Snider, “Realization of a functional cell for quantum-dot cellular automata,” Science, vol. 277, no. 5328, pp. 928–930, 1997.

[18] Karthigai Lakshmi .S, and Athisha .G, “Efficient Design of Logical Structures and Functions Using Nanotechnology Based Quantum Dot Cellular Automata Design,” International Journal of Computer Applications, 2010.

[19] G. H. Bernstein, "Quantum-dot cellular automata by electric and magnetic field coupling," in Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003., 2003, pp. 223-229.

[20] M. Choi, M. Choi, Z. Patitz, and N. Park, "Efficient and Robust Delay-Insensitive QCA (Quantum-Dot Cellular Automata) Design," in 2006 21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,

[21] D. P. Kelly and J. C. Lusth, "Logic devices for partitioned quantum-dot cells," in Proceedings of the 2001 1st IEEE Conference on Nanotechnology. IEEE-NANO 2001 (Cat. No.01EX516), 2001, pp. 374-379.

[22] K. Walus, R. A. Budiman, and G. A. Jullien, "Split current quantum-dot cellular automata-modeling and simulation," IEEE Transactions on Nanotechnology, vol. 3, pp. 249-255, 2004.