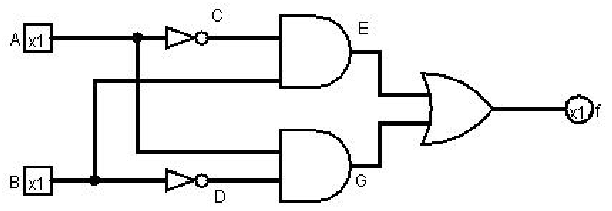
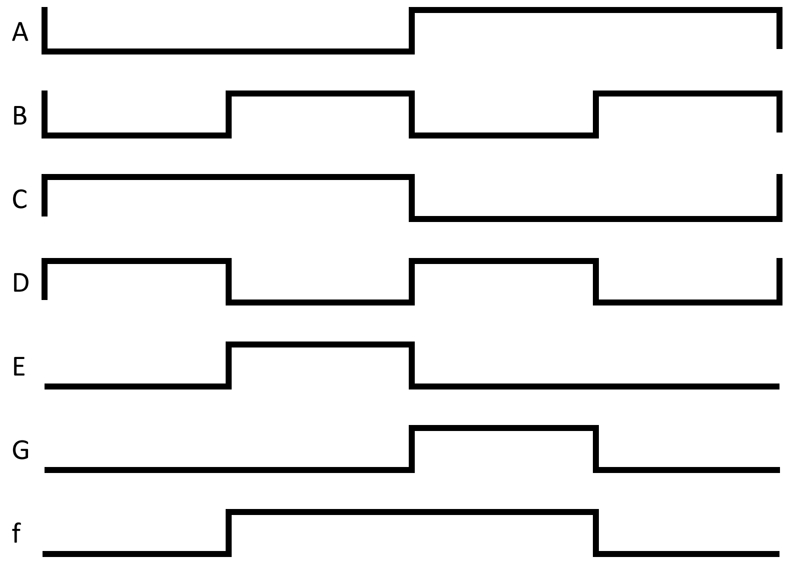
1. Timing
    a. Worst case path
        i. Route through a circuit that takes the longest in terms of gates
        ii. In the example below, worst case path is 3 gates
        iii. Either A -> NOT -> AND -> OR or B -> NOT -> AND -> OR
        iv. Worst case path determines clock speed
            1. Need to wait for all gates to finish to get output before we start new clock cycle
        v. Can also assign times to each type of gate to determine time output is generated
    b. Timing diagram
        i. Visual representation of truth tables at different parts of a digital logic circuit
        ii. Initial values of inputs iterate over all possible combinations (like a truth table)
        iii. Truth values at later points are shown based on each of those combinations
    c. Example
        i. Implementation of XOR using only AND, OR, NOT
        ii. $A \oplus B = A * \sim B + \sim A * B$
        iii. Assume that we have the following gate delays: NOT = 3 ns, AND = 5 ns, OR = 4 ns. What is the clock time of the circuit?





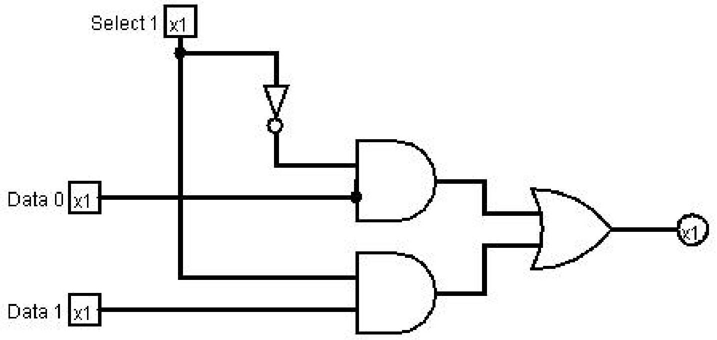
2. Combinational circuit building blocks
    a. Talked about gates so far
    b. We now move on to other important pieces of digital design
3. Multiplexors
    a. Also known as MUXes
    b. MUXes select one output from multiple inputs
        i. Used to control signal and data routing
    c. For *n* data inputs, a MUX has $s = \lceil \log_2 n \rceil$ select bits that control which input we select.
    d. Implementation
        i. *n* AND gates
            1. Each one has one data input

2. Also has *s* select inputs
3. The select inputs are all true for only one AND gate at a time

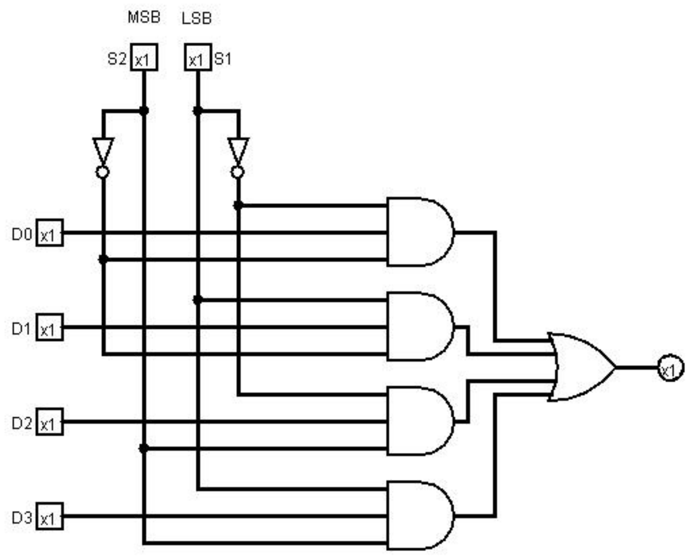
ii. One OR gate
1. *n* inputs from the AND gates
2. Only one of the AND gates will have a non-zero output (unless that gate's output is all zeroes)

e. Can use MUXes to implement functions
i. Hook up constant 0s or 1s to each input
ii. MUX takes in input bits and outputs corresponding constant for that input

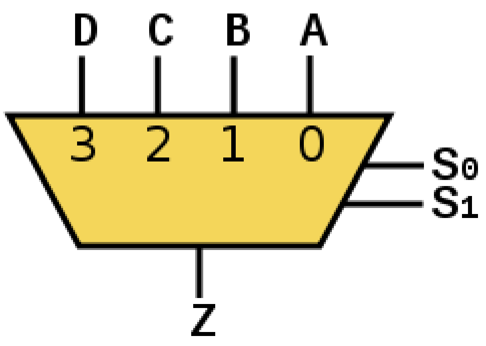
f. Example
i. 2 to 1 MUX



ii. 4 to 1 MUX



Depiction in a circuit diagram


D
C
B
A
3
2
1
0
S0
S1
Z