564 Digital Signal Processing

Computing Assignment

Module 3

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Introduction

In this module, we first have the signal after sub-sampling from the previous part of receiver. Then, due to the channel we have does not introduce other additive noise, so the equalizer does not need to be implement. Hence, the signal after sub-sampling will go directly to the matched filter, which should be design as.

$$h_{mf}[n] = \begin{cases} h_{rc}[31-n] & ; \quad n = 0, 1, 2, \cdots, 31 \\ 0 & ; \quad \text{Otherwise.} \end{cases}$$

After we have the impulse response of h_mf, we will let it pass through the FIR filter we designed earlier with the sub-sampling signal in I-channel and Q-channel. Next, before another sub-sampling, we need to estimate the delay of the signal which cause by the system. The algorithm we implement is shown as,

$$c_{fd}[m] = \sum_{n=0}^{P-1} f_1[n] d_1[n-m]$$

with the delay m as 31. After the delay estimation we can sub-sampling the signal in both channel by factor of 4 again. Last, we need to detect the symbol when its positive the output would be 1, otherwise it would be -1. This is the process of this module, and we can get the original signal input to this system by this receiver. My goal is to make sure that the demodulation output signal from the receiver would be the same as the input signal from the transistor.

Project Results

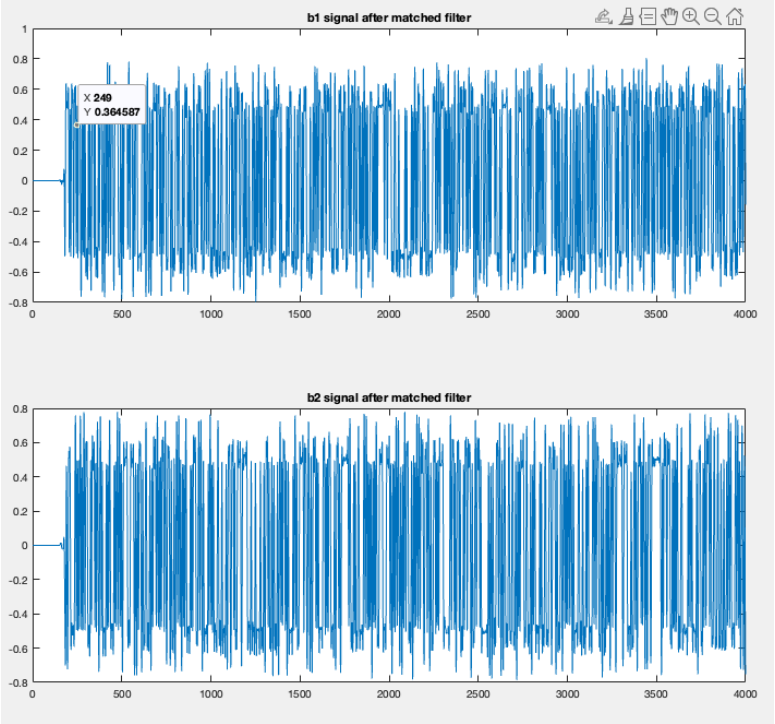

Figure 1.

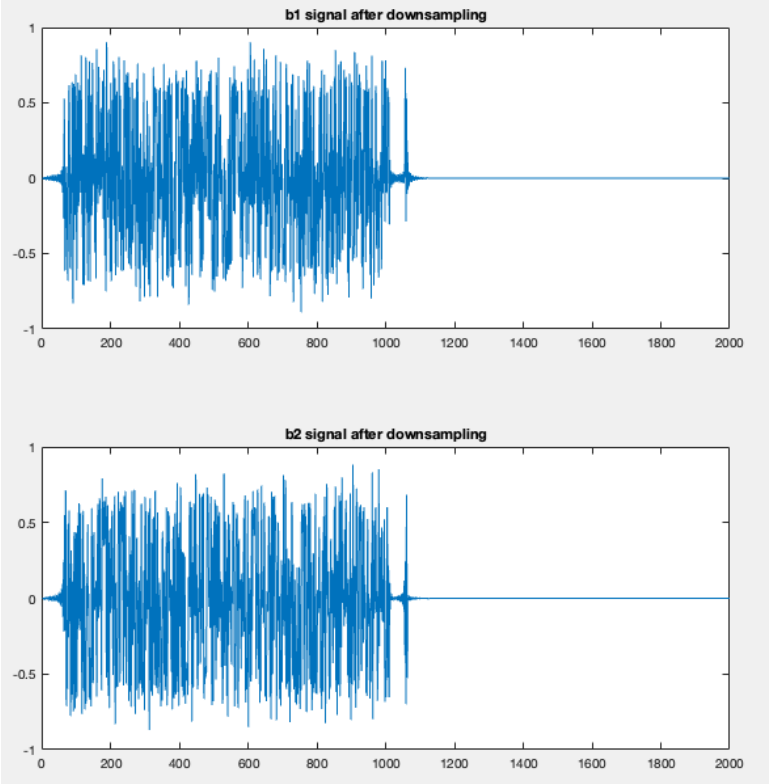

Figure 2.

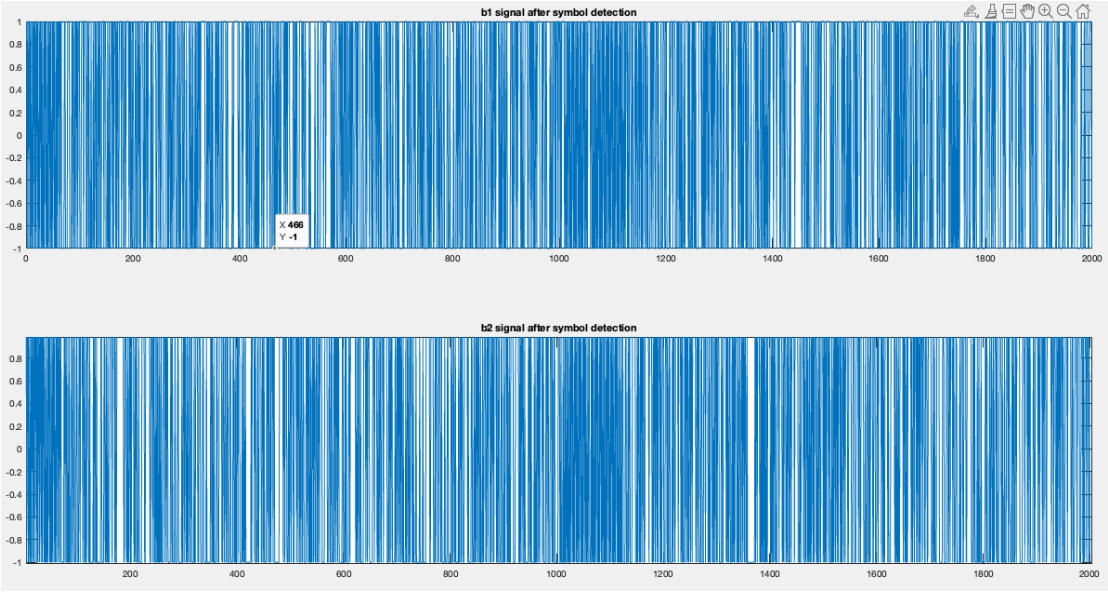

Figure 3.

The figure 1 shows the signal after the matched filter which is implemented by the impulse response and the FIR filter we design earlier. Next, in the figure 2, we can see that this signal results came out by the correlation function with the delay m in it. After that it pass through a down sampling process with factor of 4. Last, the figure 3 shows the results after the symbol detection for the positive and negative value would leads to 1 and -1 respectively. Furthermore, this is also the output result of the receiver we design for this project. I believe it works properly which it gave us the binary output which is same as the original input we generate for the transistor.

Conclusion

By working on this project, it gave me the chance to understand the process of a QPSK modulation and demodulation in the transistor and receiver. Moreover, I understand and learned how to design different kinds of filter such as bandpass filter, lowpass filter, matched filter for this implementation. In my point of view, the outcome results from the receiver looks reasonable for me, since by the symbol detection, it generates the binary data properly. However, to make my implementation more professional, I believe their need more accurate parameter for it, since the signal would mix with more noise in reality. Hence, we should count those noise component in to make the whole measurement more professional.