



Welcome to The Hardware Lab!

Fall 2019

Lab 6: Peripheral Components: VGA, Mouse, and Dual FPGA

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Agenda

- Lab 6 Outline
- Lab 6 Basic Questions
- Lab 6 Advanced Questions



Lab 6 Outline

- Basic questions (2%)
 - Individual assignment
 - Due on **11/28/2018**. Demonstration on your FPGA board (**In class**)
 - Only demonstration is necessary. Nothing to submit.
- Advanced questions (5%)
 - Group assignment
 - ILMS submission due on **12/12/2018. 23:59:59**.
 - Demonstration on your FPGA board (**In class**)
 - Assignment submission (**Submit to ILMS**)
 - Source codes and testbenches
 - Lab report in PDF

Lab 6 Rules

- You can use **ANY** modeling techniques
- If not specifically mentioned, we assume the following SPEC
 - **CLK** is **positive edge triggered**
 - Synchronously reset the Flip-Flops when **RESET == 1'b0**

Lab 6 Submission Requirements

- Source codes and testbenches
 - Please follow the templates **EXACTLY**
 - We will test your codes by TAs' testbenches
- Lab 6 report
 - Please submit your report in a single **PDF** file
 - Please **draw** the **block diagrams** and **state transition diagrams** of your designs
 - Please **explain** your designs in detail
 - Please **list** the contributions of each team member clearly
 - **Please explain how you test your design**
 - What you have **learned** from Lab 6

Agenda

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- **Lab 6 Basic Questions**
- Lab 6 Advanced Questions



Basic Questions

- Individual assignment
- FPGA demonstration (due on 11/28/2018. In class.)
 - VGA sample code
 - Mouse sample code
- Demonstrate your work by FPGA

Basic FPGA Demonstration 1

- **VGA sample codes**

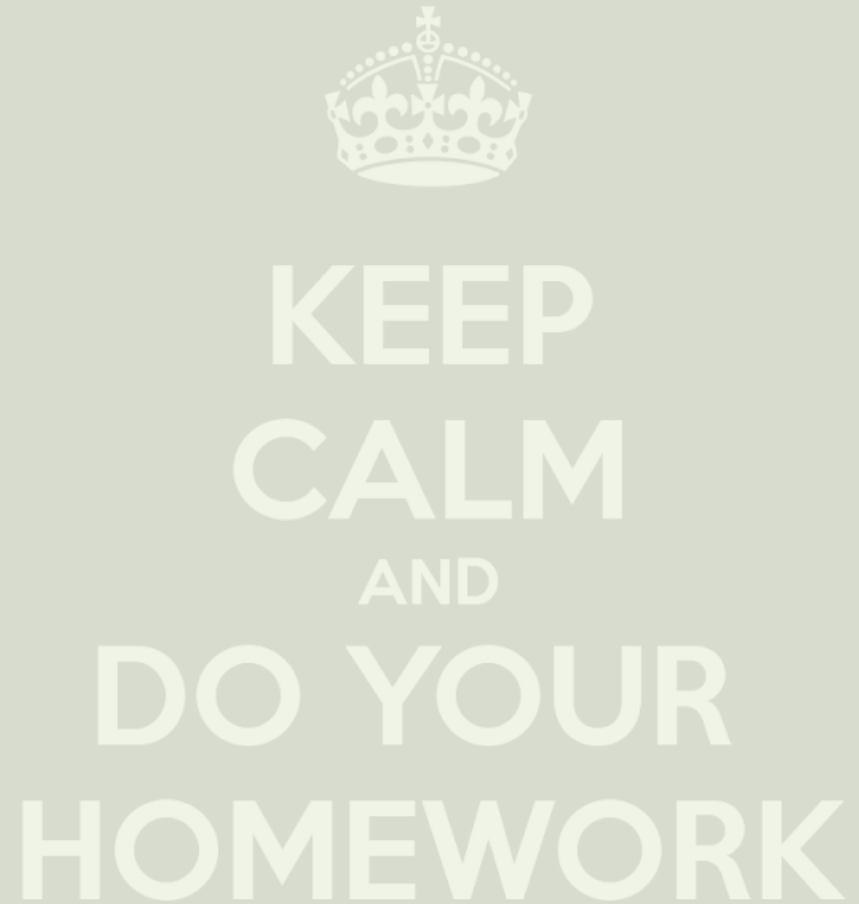
- Please implement the keyboard sample codes 1 & 2 released on ILMS

- **Mouse sample codes**

- Please implement the mouse sample code released on ILMS

Agenda

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- **Lab 6 Advanced Questions**








Advanced Questions

- Group assignment
- FPGA demonstration (due on 12/12/2018. In class.)
 - Mixing keyboard and VGA together
 - Dual FPGA communication

Mixing Keyboard and VGA

- Use the keyboard to control your VGA display
- Control the image displayed on the screen according to the following commands
- If you press P right after Reset, the image starts scrolling up

	Image scrolling up	P	Pause scrolling / Start scrolling
	Image scrolling down	V	Flip vertically
	Image scrolling left	H	Flip horizontally
	Image scrolling right	Mid-Button 	Reset 1. Stop scrolling (Pause) 2. Image sets back to origin (No flip)

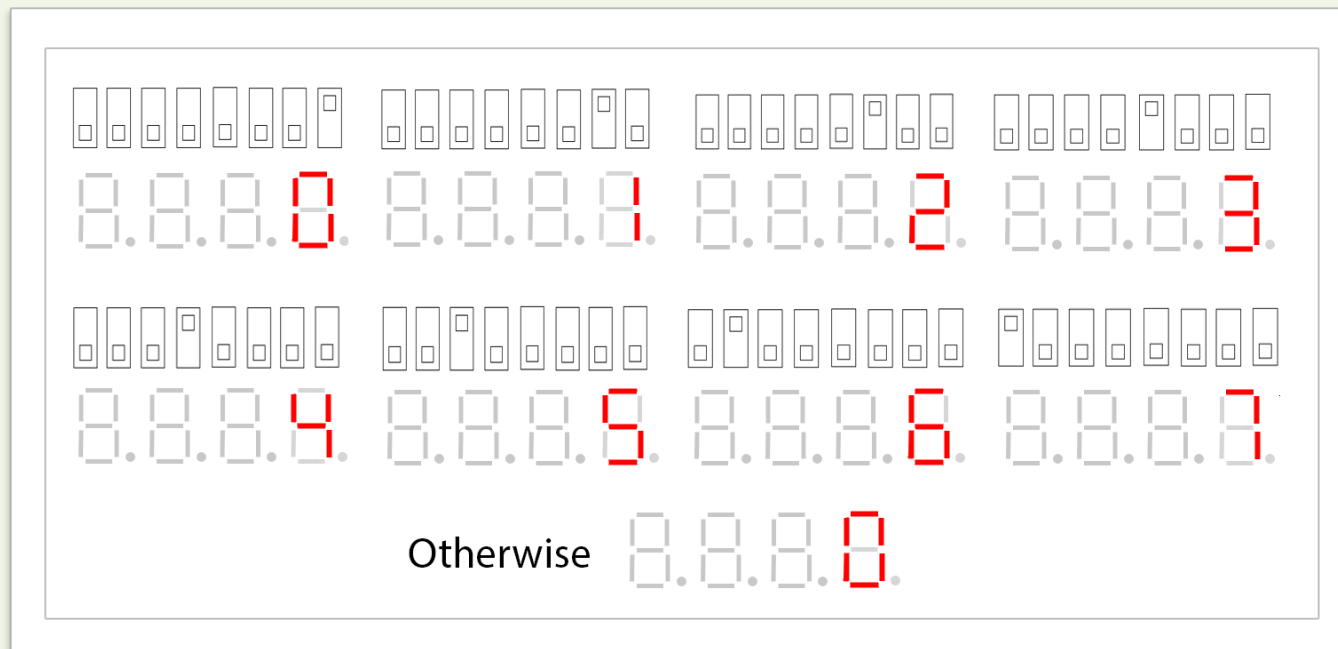
Dual FPGA Communication Requirements

- Please design a simple FPGA-to-FPGA communication protocol
- The protocol is required to fulfill the following requirements:
 - Use the Handshaking protocol described below to send a number from a **Master** FPGA to a **Slave** FPGA
 - [**Master** -> **Slave**] Request
 - [**Slave** -> **Master**] ACK
 - [**Master** -> **Slave**] Send data (number)
 - Your design should be demonstrable in an observable speed so that TAs can know whether your design is correct or not
 - Your design should be stable and should avoid signal loss

Dual FPGA Communication

Data Representation

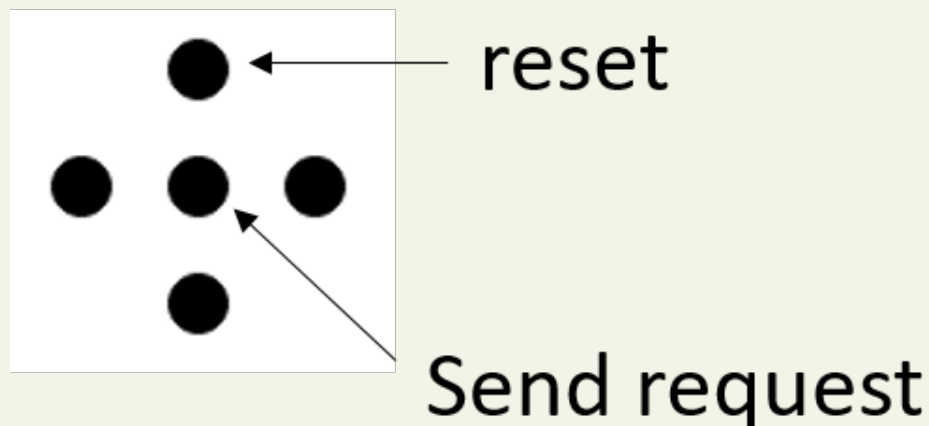
- For the **Master** FPGA, please use switches to represent numbers in one-hot form
- For the **Slave** FPGA, please display the numbers on your 7-segment displays
- Please illuminate LED[0] for at least 1 second when FPGA receive a request or an ACK
- Below are input and the corresponding 7-segment display



Dual FPGA Communication

Button Control

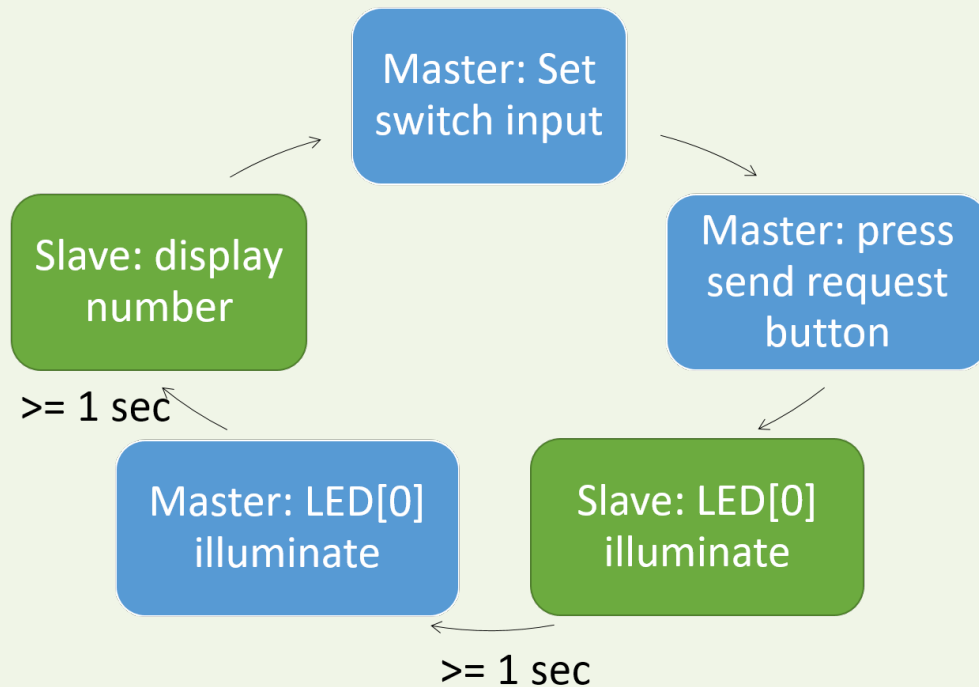
- The UP button is for reset, and the MIDDLE button is for sending request
- The communication starts only after the send request button on **Master** FPGA is pressed
- When the **Master** FPGA resets, it stop communicate with the **Slave** FPGA until the next send request button is pressed
- When the **Slave** FPGA resets, the 7-segment display 0 until next request
- The reset action of the two FPGA is independent of each other



Dual FPGA Communication

Communication Process

- The whole communicate process is designed as below:



- The display on the Slave FPGA should be hold until the data of next request is received



Thank you for your attention!

*Schloß Neuschwanstein, Germany
This picture is taken by Chun-Yi Lee himself, who is also a fan of photography