Artificial Intelligence and Machine Learning

Midterm Report

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Contents

Chapter 1

Electronic Components

1.1 Resistor

Under normal circumstances, in order to prevent the LED from being damaged due to an excessively high voltage applied to the LED, a control resistor is used to limit the flow of current to make the circuit operate smoothly.

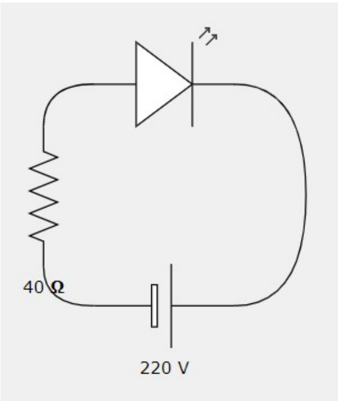


Figure 1.1

1.1.1 Variable resistor(Potentiometer)

Different from general resistors, it has three terminals. When in use, by changing the resistance value between the sliding end and the two fixed ends, different voltage division ratios are formed, so as to change the potential of the sliding point.

1.2 Operational Amplifier

Basically, an operational amplifier has two inputs (inverting and non-inverting) and one output.And the operational amplifier will generate two different outputs according to whether the voltage passed in by Vp is greater than Vn like (2.7).

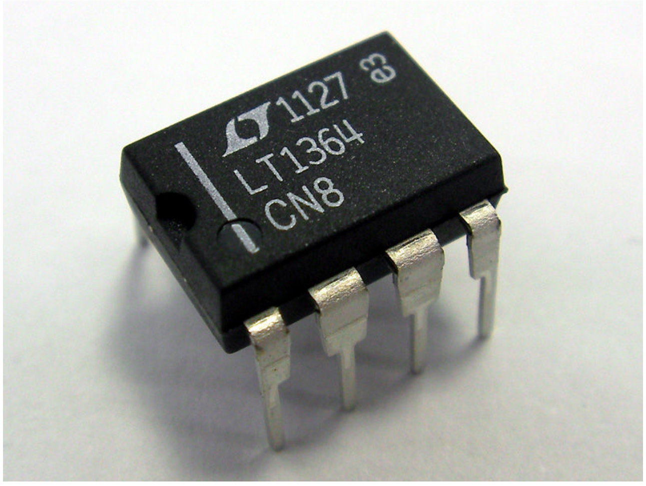


Figure 1.2

1.3 Power supply

In order to supply the electronic power, we at least use two 9V batteries in this project because we need both positive (+) and negative (-) voltages like Figure 1.3.

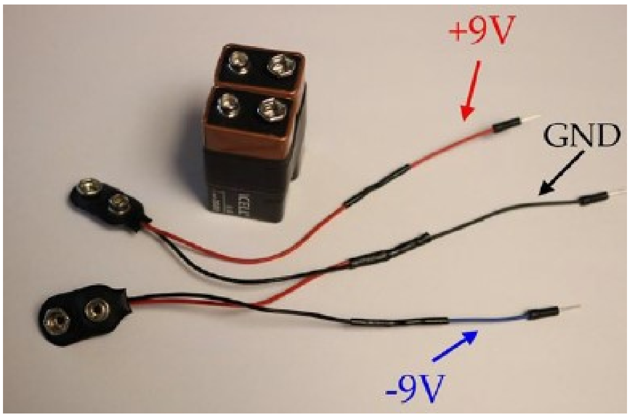


Figure 1.3

Need to pay attention when implementing

- how the battery clips are wired
- Ensuring the supply voltages are stable even under varying load conditions, you can use a +5V regulator and a -5V regulator.

1.3.1 Voltage regulator

The purpose of a voltage regulator is to provide a stable voltage that does not change under different load conditions, and when wiring up these regulators, remember their ”pin out.” which the function of each pin is different, as shown in Figure 1.4.

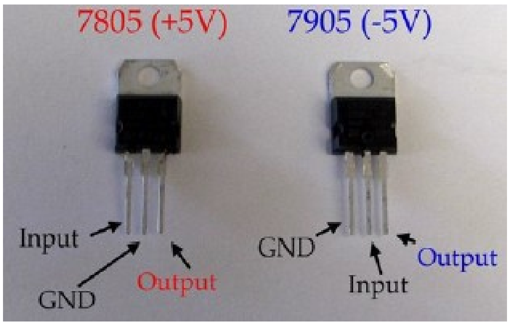


Figure 1.4

1.4 LED

LEDs are often used to identify whether current is looping in a circuit, with shorter legs of cathode and longer legs of anode. In circuit diagrams, LEDs are sometimes represented as diodes.

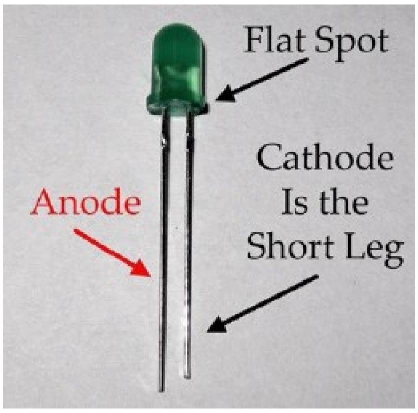


Figure 1.5

1.5 SPDT switch

In order to have two dissimilar outputs to the network, a SPDT could switch two different paths of circuits by using a switch which as shown Figure 1.6, and can be done manually or included through the electromagnetic coil.

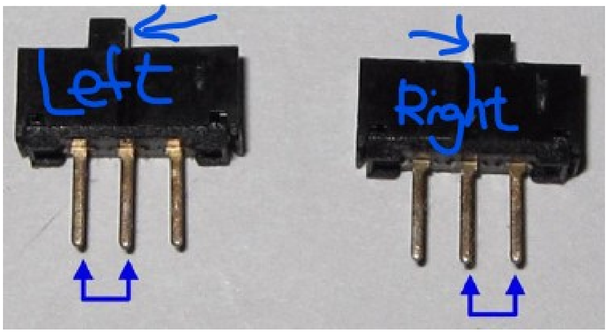


Figure 1.6

Chapter 2

Basic Circuit

2.1 Voltages Summing

The Figure 2.1 is the summation circuit. By KCL(Kirchhoff's Current Law), the sum of current entering the output node must always be 0.

$$I_1 + I_2 = 0 \tag{2.1}$$

We can use Ohm's law to replace $I_1,\ I_2$, then become

$$\frac{V_{\text{out}} - V_1}{R_1} + \frac{V_{\text{out}} - V_2}{R_2} = 0 \tag{2.2}$$

So we can get the voltage of output node V_{out} is

$$V_{\text{out}} = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2} \tag{2.3}$$

For the case in the textbook, the resistor R_1 is equal to the resistor R_2. So, we can get the output voltage was the average of the input voltages.

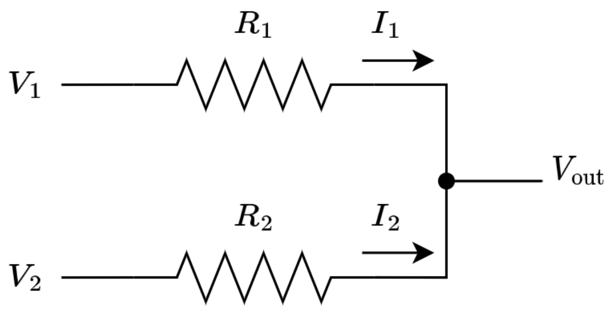


Figure 2.1: Summation circuit

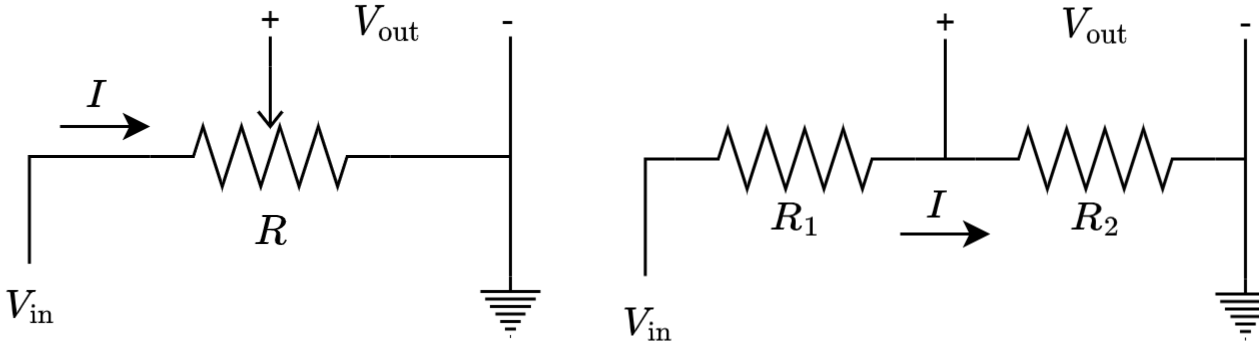
2.2 Voltage Dividing

The Figure 2.2 is the circuit of dividing voltage by Potentiometer. Because the R_1 and R_2 are in the same loop. The current passed through both resistors was equal. From the Ohm's law and resistor series rule, we can get the current I.

$$I = \frac{V_{\text{in}}}{R} = \frac{V_{\text{in}}}{R_1 + R_2} \tag{2.4}$$

Then we can get the output voltage V_{out}.

$$V_{\text{out}} = IR_2 = \frac{R_2}{R_1 + R_2} V_{\text{in}} \tag{2.5}$$



(a) Potentiometer

(b) Equivalent

Figure 2.2: Divide circuit

2.3 Voltage Comparing

Figure 2.3 is the open loop operational amplifier(Op-Amp). And the relation between output voltage and input voltages is

$$V_{\text{out}} = A_{\text{OL}} \left(V_{\text{p}} - V_{\text{n}} \right) \tag{2.6}$$

the A_{OL} is the open loop gain of op-amp. In general, the gain value is huge but the power supply can't provide that high voltage. We can rewrite the (2.6) become

$$V_{\text{out}} = \begin{cases} +V, & \text{if } V_{\text{p}} > V_{\text{n}} \\ -V, & \text{if } V_{\text{p}} < V_{\text{n}} \\ 0, & \text{if } V_{\text{p}} = V_{\text{n}} \end{cases} \tag{2.7}$$

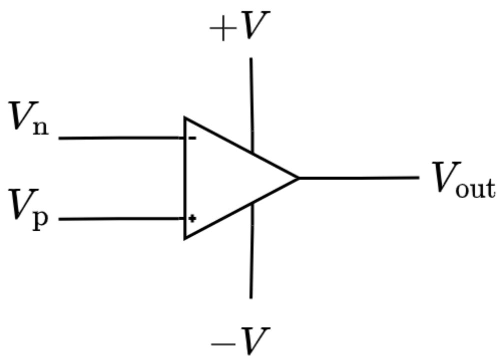


Figure 2.3: Operational amplifier

Chapter 3

Build Up Neural Network

3.1 Introduction

The target of the neural network is to function like an XOR gate. So we define the neural network like Figure 3.1. For the input layer, it will input True(+5V) or False(-5V). After the input layer, the signal will fully connect to the hidden layer. Each hidden node will sum up two signals after weighting. Then go through the activation function and output to the output layer. There has only one node in the output layer. Same as the hidden layer, the node in the output layer will sum up two signals after weighting and pass through the activation function. After the activation function will output the result(True or False) of the neural network.

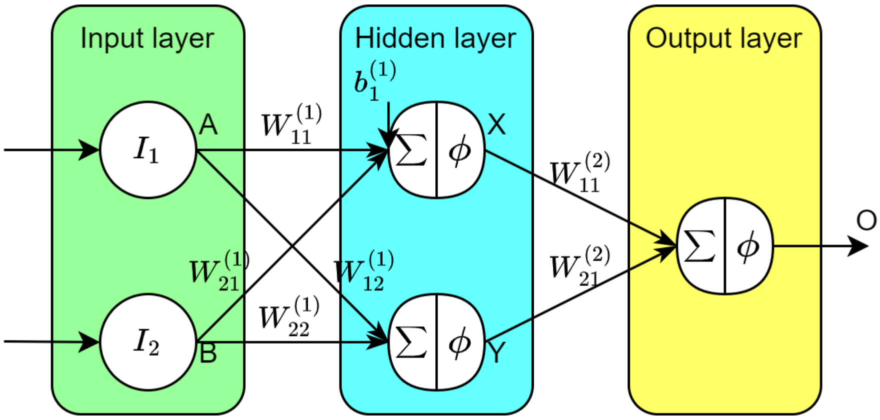


Figure 3.1: Neural network architecture

The weighting method is using a potentiometer to divide the voltage in Ch.2.2. So the weight value will between 0 and 1. And the summation method is summed up by circuit summing. From the result of Ch.2.1, the circuit summation actually is finding the average over all the input. And the activation function is using Op-Amp comparator in Ch.2.3. For Figure 3.2, the comparator will compare the input and the reference voltage. If the voltage is bigger then the reference voltage, then will output the positive supply. Otherwise, will output the negative supply.

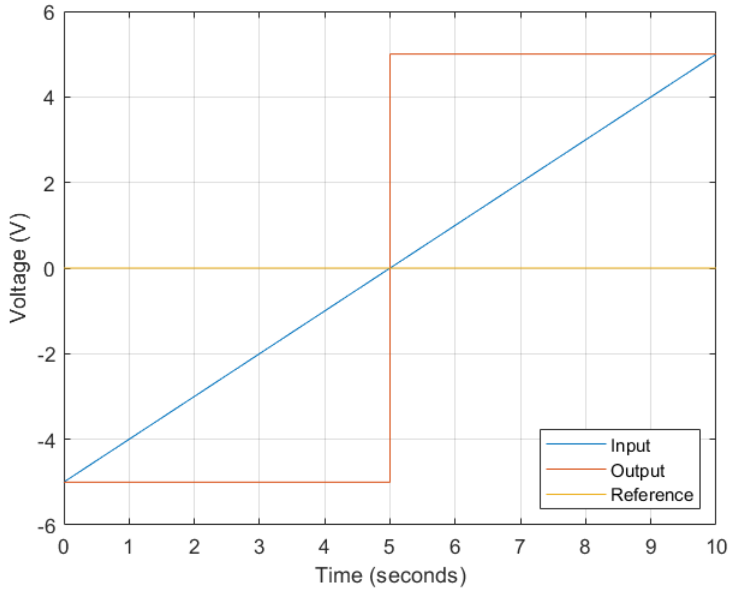


Figure 3.2: Op-Amp comparator activation function

For the beginning to build up the neural network, we need to build up the power system. The power system is like Figure 3.3. There have two different voltage for the electronic components. One is $+5V$ comes from 7805 regulator for positive power supply. Another is $-5V$ comes from 7905 regulator for negative power supply. This two power will use at create the signals and amplifier's power.

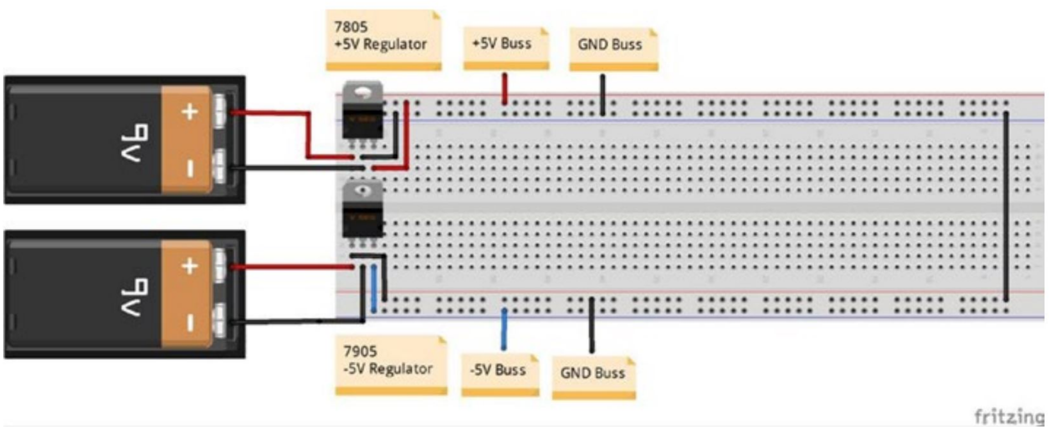


Figure 3.3: Protoboard power system

3.2 Input layer

The input layer node is present by Figure 3.4. The True and False signal is controlled by the SPDT switch. If the switch connects to the positive power supply, the input layer will output a True signal. Otherwise, if the switch connects to the negative power supply, the input layer will output a False signal. And we can see that there has a branch after the SPDT switch. We will connect a LED to display the state of input signal. If the LED is on, the output is True. Otherwise, the output will be False.

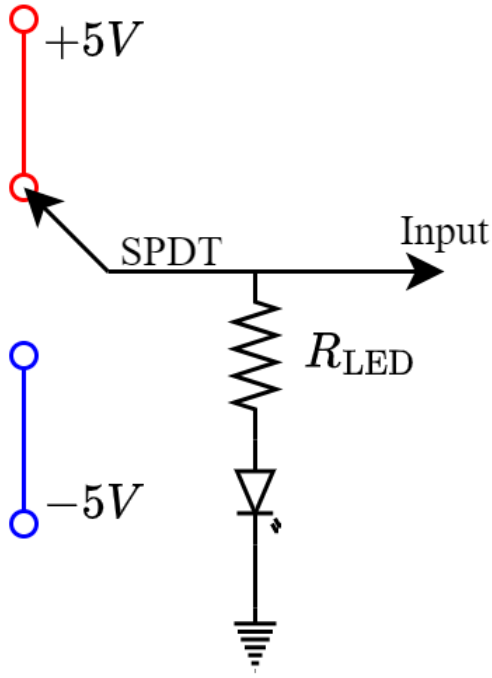


Figure 3.4: Input node circuit

After adding the input layer on the protoboard will be like Figure 3.5.

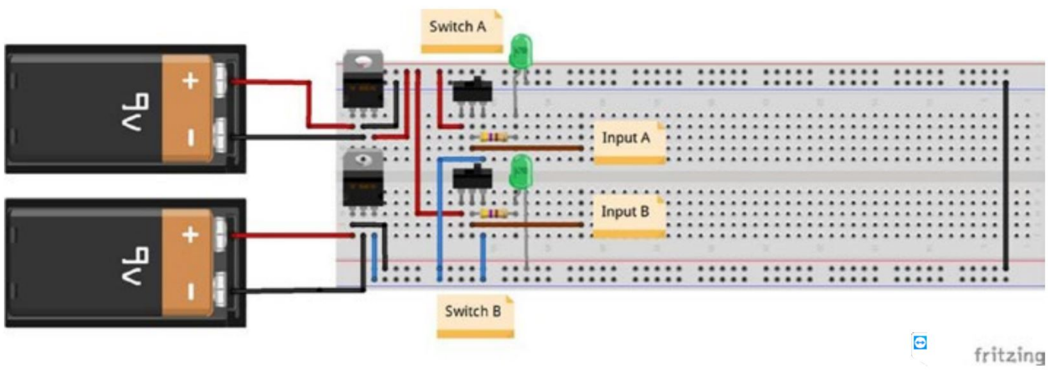


Figure 3.5: Input layer on the protoboard

3.3 Hidden layer

The hidden layer node is present by Figure 3.6 and Figure 3.7. For the first node in hidden layer will connect to two signal from input layer and a bias signal. And the second node will connect to two signals from input layer. First, those signals will pass through a potentiometer to divide voltage. Next, connect two signals to two 100KΩ resistor and connect it together to get the average signals. Last after sum up, we will connect to the comparator as activation function then output.

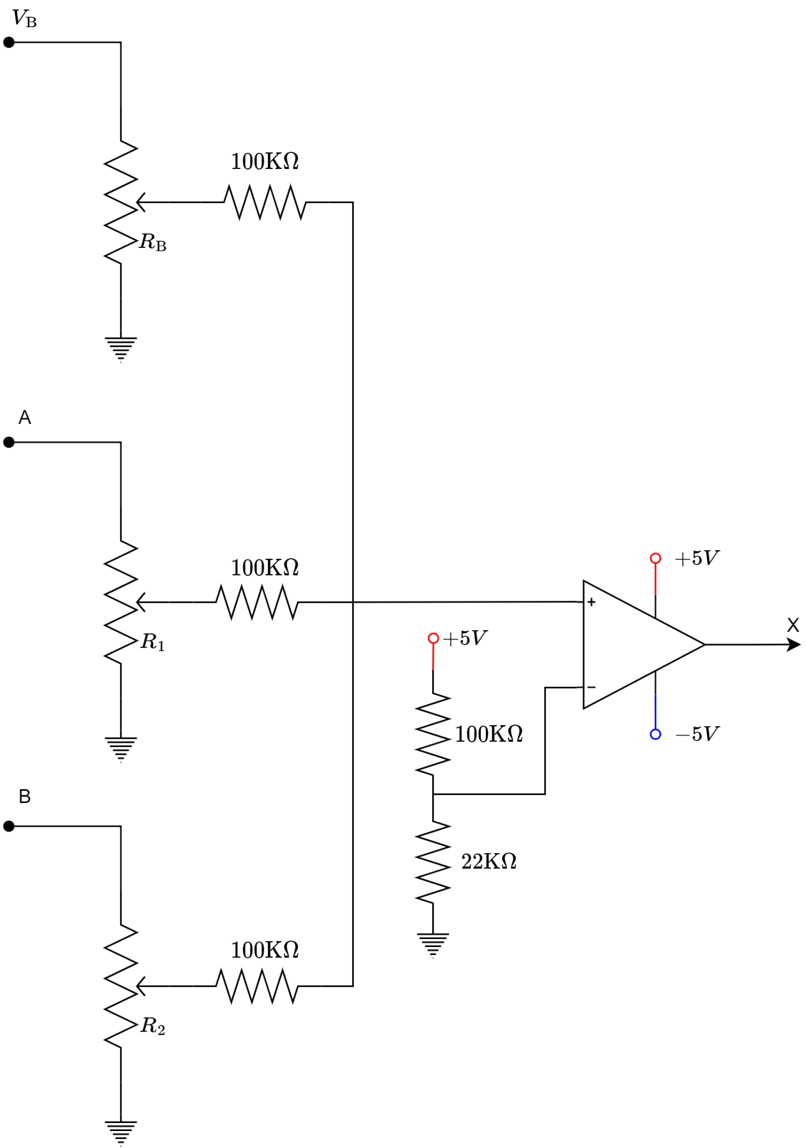


Figure 3.6: First hidden node circuit

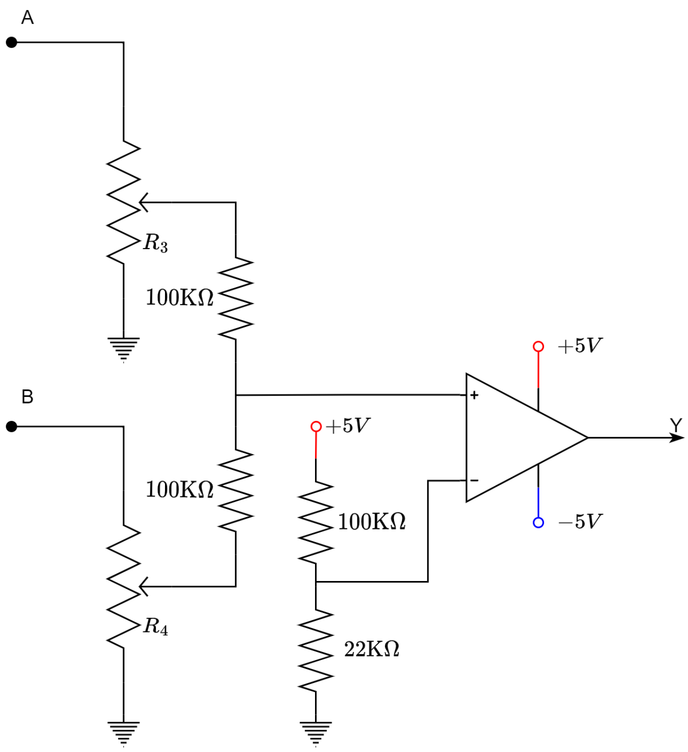


Figure 3.7: Second hidden node circuit

After adding the hidden layer on the protoboard will be like Figure 3.8.

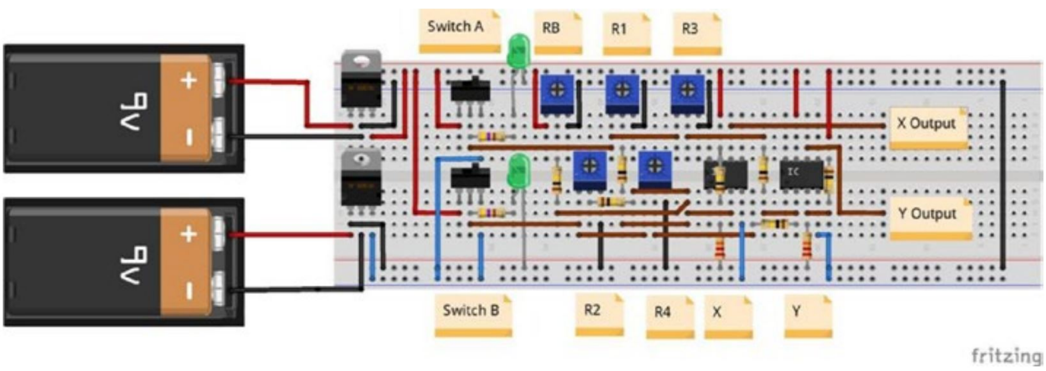


Figure 3.8: Hidden layer on the protoboard

3.4 Output layer

The output layer is present by Figure 3.9. For the output layer is similar to the hidden node. The different is the input signal X and Y is from the output of hidden layer. And the output will connect to a LED system to display the result.

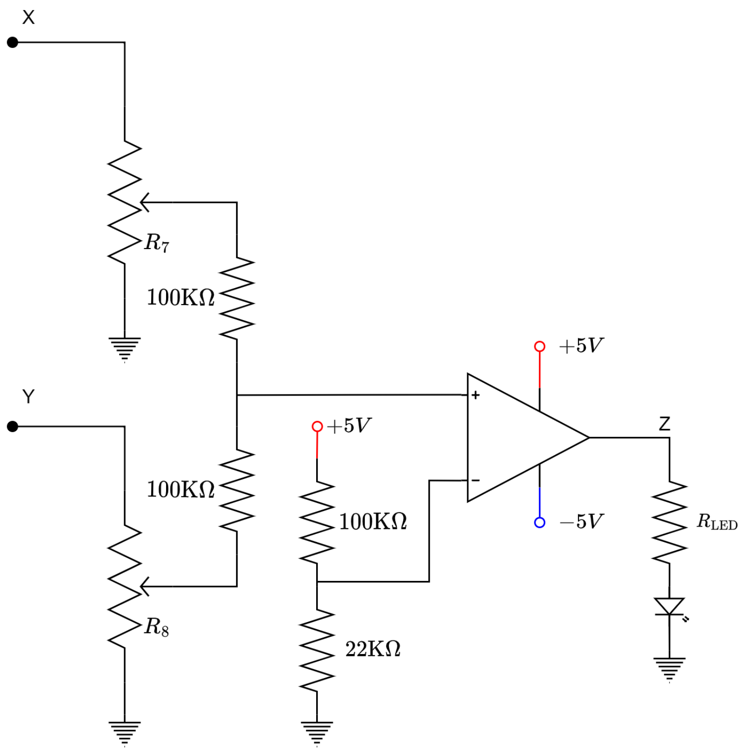


Figure 3.9: Output layer circuit

After adding the output layer on the protoboard will be like Figure 3.10.

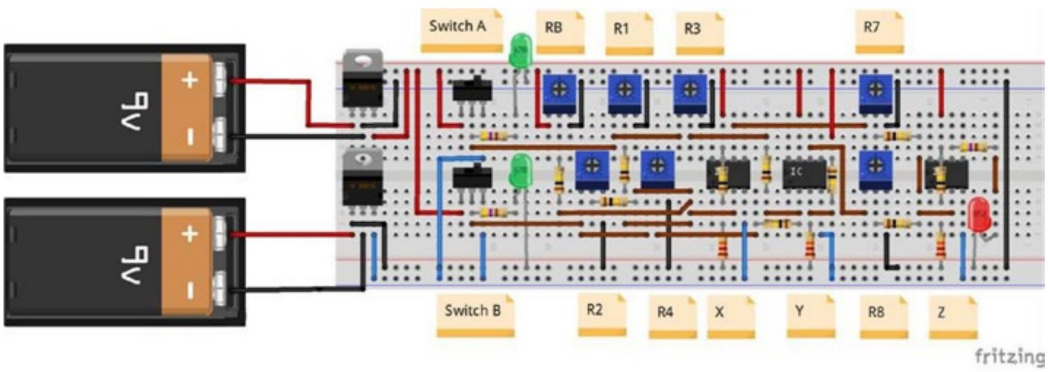


Figure 3.10: Output layer on the protoboard

3.5 Summary

From Figure 3.1 we can know that the neural network model is

$$\begin{bmatrix} X \\ Y \end{bmatrix} = \phi\left(\begin{bmatrix} W_{11}^{(1)} & W_{12}^{(1)} \\ W_{21}^{(1)} & W_{22}^{(1)} \end{bmatrix}\begin{bmatrix} A \\ B \end{bmatrix} + \begin{bmatrix} b_1^{(1)} \\ 0 \end{bmatrix}\right) = \phi\left(v^{(1)}\right) \tag{3.1}$$

$$Z = \phi\left(\begin{bmatrix} W_{11}^{(2)} & W_{12}^{(2)} \end{bmatrix}\begin{bmatrix} X \\ Y \end{bmatrix}\right) = \phi\left(v^{(2)}\right) \tag{3.2}$$

A and B are the input signal, X and Y are the output signal of hidden layer. The weight and the bias of hidden layer is

$$W^{(1)} = \begin{bmatrix} \frac{R_1}{3\times 100} & \frac{R_2}{3\times 100} \\ \frac{R_3}{2\times 100} & \frac{R_4}{2\times 100} \end{bmatrix} \tag{3.3}$$

$$b^{(1)} = \begin{bmatrix} \frac{R_b}{3\times 100} \\ 0 \end{bmatrix} \tag{3.4}$$

the term of $\frac{1}{2}$ or $\frac{1}{3}$ is taking average of each node, and the term of $\frac{1}{100}$ is from voltage divide. The weight of output layer is

$$W^{(2)} = \frac{1}{2\times 100} \begin{bmatrix} R_7 & R_8 \end{bmatrix} \tag{3.5}$$

For the value of resistors, $R_\mathrm{n} \in [0, 100]$. And the activation function is

$$\phi(x) = \begin{cases} +5, & \text{if } x > \frac{5\times 22}{122} \\ -5, & \text{if } x < \frac{5\times 22}{122} \\ 0, & \text{if } x = \frac{5\times 22}{122} \end{cases} \tag{3.6}$$

Chapter 4

Training Neural Network

4.1 Weight Tuning

After following the instructions in the textbook to set up the neural network system using electronic components, we tested it using the principles of an XOR gate. We used switches to control the input signals, and LEDs to check the status at the input and output layers. The initial state of neural network is shown in Table 4.1.

Table 4.1: Initial truth table

A	B	Z	XOR
F	F	T	F
T	F	F	T
F	T	T	T
T	T	F	F

We found there are two sets are violates the definition of XOR. Therefore, in order to know exactly the cause of the failure, we use a meter to measure the voltage value received by each variable resistor and Op-Amp in sequence. In the following, when the result is wrong then we will tune some potentiometer a little bit until all the result is correct. And the main idea is that we know the absolute value of voltage will between 0 volts and 5 volts. When the result is too big, then we can tune down those points when the voltage is close to 5V, and vice versa.

From Table 4.2, we can see the output state is incorrect. For the purpose of changing Z to a negative value, we can know that the main factor that can affect Z is V7 and V8 by Figure 3.9. However, the absolute value of voltage will be less than 5V. Then we can obtain the voltage V8 is close to the high boundary that the voltage at Z becomes positive, and it also close to the boundary. So that, we tune down the resistor R8 to low down the V8 until the output LED turn-off.

Table 4.2: The first tuning loop when A=F, B=F

A is False, B is False, correct Z is False												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
3.59	0.96	-2.46	4.63	-4.92	-0.51	1.83	-1.35	-0.51	5.02	-4.68	-4.75	-4.78
			⇓					⇓				
Adjust to												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94	0.53		3.90	-4.92	-0.7			-1.77				

Note: ⇓ means decrease the voltage, ⇑ means increase the voltage. The red word means the output state has changed, and the blue word means the voltage change caused by the potentiometer change.

In the next state, the output of the neural network is false when the first input signal is true and the second input signal is false. The output does not match the principle of an XOR gate, so we need to adjust the weight through measuring the voltage value.

According to Table 4.3, increasing the voltage of V9 would change the output to a positive value. Figure 3.9 shows that the voltages of V7 and V8 can affect the value of V9 and ultimately the output state. However, Table 4.3 indicates that the voltage of V8 is already high and the voltage of V7 is negative. In order to change the output to a positive value, we need to increase the voltage of V7. The main factors that can affect V7 are X and Y. If we can make the voltage of X positive, it would also cause the voltage of V7 to become positive. To do this, we can increase the voltages of V1 or Vb in order to increase the summation voltage of V5. In this case, we will try tuning up the voltage of V1 until the output LED receives a true signal.

Table 4.3: The first loop when A=T, B=F

A is True, B is False, correct Z is True												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94	0.62	-2.62	4.01	-4.92	0.30	1.50	1.18	-1.51	5.02	0.15	5.05	-4.73
							⇑					
Adjust to												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
3.55	3.59	3.2		5.03	0.94		2.55					

In the next state, the first input signal is false and the second input signal is true, then the output of the neural network is false. We can compare with the initial state in Table 4.1, after adjusting the weight twice, the result of this state becomes incorrect. Therefore, we need to regulate some weight in this situation.

According to Table 4.4, similar to the previous situation, we need to make the voltage of V7 and X positive in order to get a positive output signal. This can be achieved by decreasing the voltage of V1 and increasing the voltages of V2 and VB. However, during the first adjustment, we already lowered the voltage of V2, so it would not make sense to increase it again. As a result, we only adjust V1 and VB. Basis of the result in Table 4.4, the voltage at X didn't change and it's difficult to make the voltage V1 and

VB more extreme. If we adjust the voltages too much, it could easily affect other situations, so we will stop at here.

Table 4.4: The first loop when A=F, B=T

A is False, B is True, correct Z is True												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94	0.60	-2.67	3.90	-4.91	-0.05	1.28	-2.49	1.12	5.02	-0.27	-4.94	4.26
						⇑	⇓					
Adjust to												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94				-4.91	0.58	2.40	-1.51					

According to Table 4.5, the output Z matches to the principle for XOR gate. So, we don't need to make any changes in this case.

Table 4.5: The first loop when A=T, B=T

A is True, B is True, correct Z is True												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94	-0.92	2.02	-3.92	5.03	2.05	2.76	1.91	1.45	-4.92	4.52	4.96	4.40
Adjust to												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4

According to Table 4.6, we can see that the only incorrect result occurs when the first input is true and the second input is false. Therefore, we only need to focus on correcting this situation.

Table 4.6: After first loop

A	B	Z	XOR
F	F	F	F
T	F	F	T
F	T	T	T
T	T	F	F

Based on Table 4.7 and the first tuning loop, in order to make the voltage of Z become positive, we need to adjust V1, V2, and VB to let X and V7 become positive. However, we can see that the negative voltage of V1 is already low and there is almost no room for adjustment. Additionally, we cannot increase the voltage V2. So, we try to modify the voltage VB to solve the problem.

Table 4.7: The second loop when A=T, B=F

A is True, B is False, correct Z is True												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
-4.94	0.60	-2.67	3.90	-4.91	0.58	2.40	-1.51	1.12	5.02	-0.27	-4.94	4.26
						⇑						
Adjust to												
Z	V9	V7	V8	X	V5	VB	V1	V2	Y	V6	V3	V4
3.58	3.46	2.91		5.03	1.02	3.65						

After the second loop, we check the data of neural network, as shown in Table 4.8. In evident that the results are matches the principles of the XOR gate.

Table 4.8: After first loop

A	B	Z	XOR
F	F	F	F
T	F	T	T
F	T	T	T
T	T	F	F