Chapter 59
Stepper Motor Controller (SMC)

59.1 Chip-specific Stepper Motor Controller (SMC) information

The chip has one Stepper Motor Controller (SMC) module capable of driving up to 6 stepper motors for instrument cluster gauges.

Each stepper motor is driven by 4 outputs to drive 2 coils.

Control of this module will be typically, but not exclusively, by the CortexM0+ IO Processor subsystem.

59.2 Introduction

The Stepper Motor Controller (SMC) block is a PWM motor controller suitable for driving small stepper and air core motors used in instrumentation applications. The module can also be used for other motor control or PWM applications that match the frequency, resolution and output drive capabilities of the module. The SMC has 12 PWM channels associated with two pins each (24 pins in total).

59.2.1 Features

The SMC includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- Left, right, or center aligned PWM
- Short-circuit detection in each PWM channel with programmable time-out

59.2.2 Modes of Operation

59.2.2.1 Functional Modes

59.2.2.1.1 Dither Function

Dither function can be selected or deselected by setting or clearing the MCCTL0[DITH] bit. This bit influences all PWM channels. For details, please refer to MCCTL0[DITH].

59.2.2.2 PWM Channel Configuration Modes

The 12 PWM channels can operate in three functional modes. Those modes are, with some restrictions, selectable for each channel independently.

59.2.2.2.1 Dual Full H-Bridge Mode

This mode is suitable to drive a stepper motor or a 360° air gauge instrument. In this mode two adjacent PWM channels are combined, and two PWM channels drive four pins.

59.2.2.2.2 Full H-Bridge Mode

This mode is suitable to drive any load requiring a PWM signal in a H-bridge configuration using two pins.

59.2.2.2.3 Half H-Bridge Mode

This mode is suitable to drive a 90° instrument driven by one pin.

59.2.2.3 PWM Alignment Modes

Each PWM channel can operate independently in three different alignment modes. For details, please refer to PWM Alignment Modes.

59.2.2.4 Low-Power Modes

The behavior of the SMC in low-power modes is programmable. For details, please refer to SMC Halt Mode and SMC Stop Mode.

59.2.3 Block Diagram

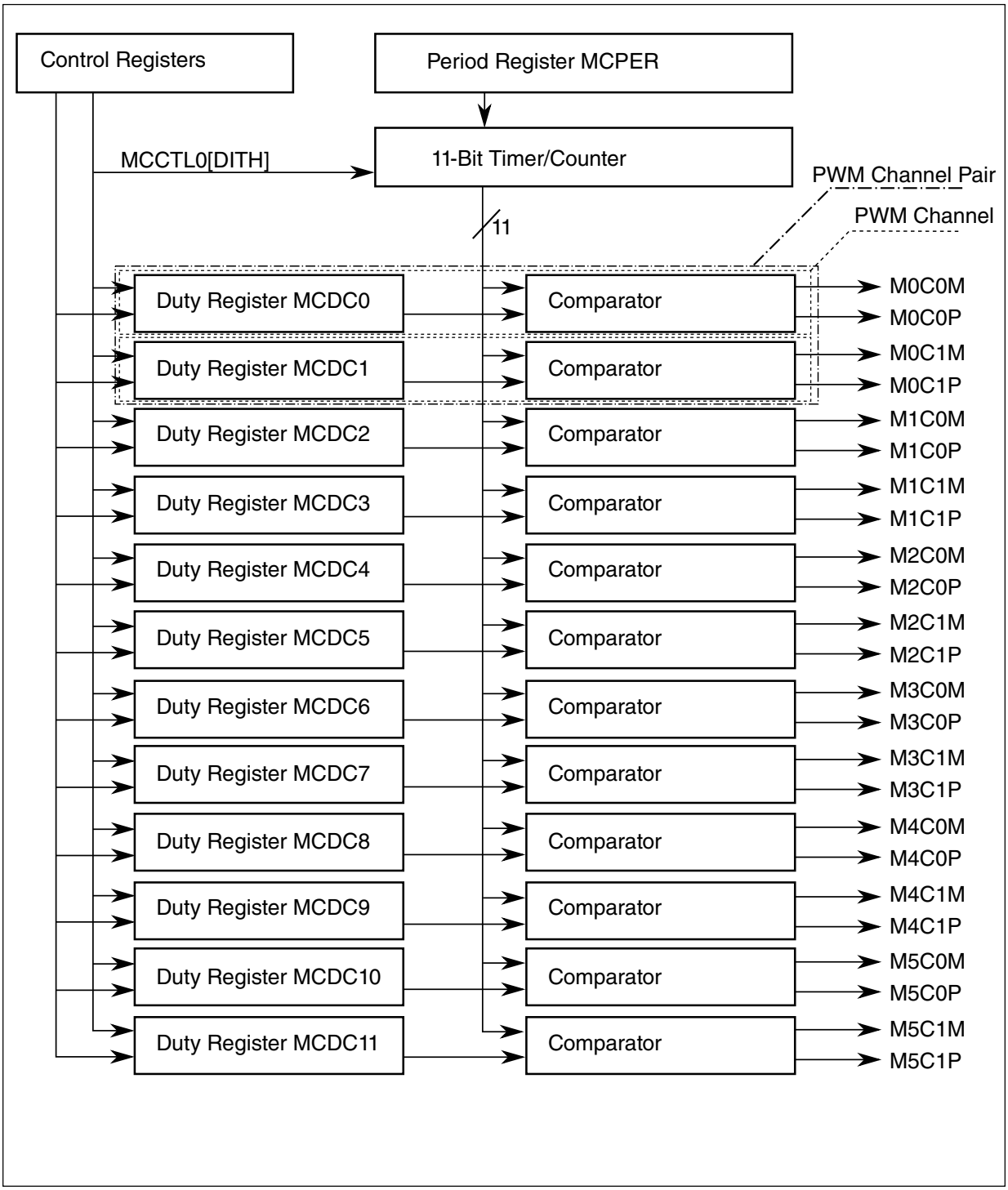

Figure 59-1. SMC Block Diagram

59.3 External Signal Description

The SMC is associated with 24 pins. Table 59-1 lists the relationship between the PWM channels, signal pins, PWM channel pairs (motor numbers), coils and nodes they are supposed to drive if all channels are set to dual full H-bridge configuration.

Table 59-1. PWM Channel and Pin Assignment

Pin Name	PWM Channel	PWM Channel Pair[1]	Coil	Node
M0C0M	0	0	0	Minus
M0C0P				Plus
M0C1M	1		1	Minus
M0C1P				Plus
M1C0M	2	1	0	Minus
M1C0P				Plus
M1C1M	3		1	Minus
M1C1P				Plus
M2C0M	4	2	0	Minus
M2C0P				Plus
M2C1M	5		1	Minus
M2C1P				Plus
M3C0M	6	3	0	Minus
M3C0P				Plus
M3C1M	7		1	Minus
M3C1P				Plus
M4C0M	8	4	0	Minus
M4C0P				Plus
M4C1M	9		1	Minus
M4C1P				Plus
M5C0M	10	5	0	Minus
M5C0P				Plus
M5C1M	11		1	Minus
M5C1P				Plus

1. A PWM Channel Pair always consists of PWM channel x and PWM channel x+1 (x = 2·n). The term “PWM Channel Pair” is equivalent to the term “Motor”. For example, Channel Pair 0 is equivalent to Motor 0.

59.3.1 M0C0M/M0C0P/M0C1M/M0C1P — PWM Output Pins for Motor 0

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state (for details refer to Modes of Operation).

59.3.2 M1C0M/M1C0P/M1C1M/M1C1P — PWM Output Pins for Motor 1

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state (for details refer to Modes of Operation).

59.3.3 M2C0M/M2C0P/M2C1M/M2C1P — PWM Output Pins for Motor 2

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state (for details refer to Modes of Operation).

59.3.4 M3C0M/M3C0P/M3C1M/M3C1P — PWM Output Pins for Motor 3

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state (for details refer to Modes of Operation).

59.3.5 M4C0M/M4C0P/M4C1M/M4C1P — PWM Output Pins for Motor 4

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state (for details refer to Modes of Operation).

59.3.6 M5C0M/M5C0P/M5C1M/M5C1P — PWM Output Pins for Motor 5

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state (for details refer to Modes of Operation).

59.4 Memory Map and Register Definition

This section provides the memory map and a detailed description of all registers of the 10-bit 12-channel SMC module.

Access type can be

- RW: Read and Write
- Data access type is 8,16 or 32 bit. It is recommended to access the various register using the access types shown in the following table for consistent write operations.

SMC memory map

Address offset (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
0	Motor Controller Period Register (SMC_MCPER)	16	R/W	0000h	59.4.1/2188
2	Motor Controller Control Register 1 (SMC_MCCTL1)	8	R/W	00h	59.4.2/2189
3	Motor Controller Control Register 0 (SMC_MCCTL0)	8	R/W	00h	59.4.3/2190
10	Motor Controller Channel Control Register (SMC_MCCC3)	8	R/W	00h	59.4.4/2191
11	Motor Controller Channel Control Register (SMC_MCCC2)	8	R/W	00h	59.4.4/2191
12	Motor Controller Channel Control Register (SMC_MCCC1)	8	R/W	00h	59.4.4/2191
13	Motor Controller Channel Control Register (SMC_MCCC0)	8	R/W	00h	59.4.4/2191

Table continues on the next page...

SMC memory map (continued)

Address offset (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
14	Motor Controller Channel Control Register (SMC_MCCC7)	8	R/W	00h	59.4.4/2191
15	Motor Controller Channel Control Register (SMC_MCCC6)	8	R/W	00h	59.4.4/2191
16	Motor Controller Channel Control Register (SMC_MCCC5)	8	R/W	00h	59.4.4/2191
17	Motor Controller Channel Control Register (SMC_MCCC4)	8	R/W	00h	59.4.4/2191
18	Motor Controller Channel Control Register (SMC_MCCC11)	8	R/W	00h	59.4.4/2191
19	Motor Controller Channel Control Register (SMC_MCCC10)	8	R/W	00h	59.4.4/2191
1A	Motor Controller Channel Control Register (SMC_MCCC9)	8	R/W	00h	59.4.4/2191
1B	Motor Controller Channel Control Register (SMC_MCCC8)	8	R/W	00h	59.4.4/2191
20	Motor Controller Duty Cycle Register (SMC_MCDC1)	16	R/W	0000h	59.4.5/2192
22	Motor Controller Duty Cycle Register (SMC_MCDC0)	16	R/W	0000h	59.4.5/2192
24	Motor Controller Duty Cycle Register (SMC_MCDC3)	16	R/W	0000h	59.4.5/2192
26	Motor Controller Duty Cycle Register (SMC_MCDC2)	16	R/W	0000h	59.4.5/2192
28	Motor Controller Duty Cycle Register (SMC_MCDC5)	16	R/W	0000h	59.4.5/2192
2A	Motor Controller Duty Cycle Register (SMC_MCDC4)	16	R/W	0000h	59.4.5/2192
2C	Motor Controller Duty Cycle Register (SMC_MCDC7)	16	R/W	0000h	59.4.5/2192
2E	Motor Controller Duty Cycle Register (SMC_MCDC6)	16	R/W	0000h	59.4.5/2192
30	Motor Controller Duty Cycle Register (SMC_MCDC9)	16	R/W	0000h	59.4.5/2192
32	Motor Controller Duty Cycle Register (SMC_MCDC8)	16	R/W	0000h	59.4.5/2192
34	Motor Controller Duty Cycle Register (SMC_MCDC11)	16	R/W	0000h	59.4.5/2192
36	Motor Controller Duty Cycle Register (SMC_MCDC10)	16	R/W	0000h	59.4.5/2192
43	Short-circuit Detector Time-out Register (SMC_MCSDTO)	8	R/W	00h	59.4.6/2193
45	Short-circuit Detector Enable Register (SMC_MCSDE2)	8	R/W	00h	59.4.7/2193
46	Short-circuit Detector Enable Register (SMC_MCSDE1)	8	R/W	00h	59.4.7/2193
47	Short-circuit Detector Enable Register (SMC_MCSDE0)	8	R/W	00h	59.4.7/2193
49	Short-circuit Detector Interrupt Enable Register (SMC_MCSDIEN2)	8	R/W	00h	59.4.8/2194
4A	Short-circuit Detector Interrupt Enable Register (SMC_MCSDIEN1)	8	R/W	00h	59.4.8/2194
4B	Short-circuit Detector Interrupt Enable Register (SMC_MCSDIEN0)	8	R/W	00h	59.4.8/2194
4D	Short-circuit Detector Interrupt Register (SMC_MCSDI2)	8	R/W	00h	59.4.9/2194
4E	Short-circuit Detector Interrupt Register (SMC_MCSDI1)	8	R/W	00h	59.4.9/2194
4F	Short-circuit Detector Interrupt Register (SMC_MCSDI0)	8	R/W	00h	59.4.9/2194

59.4.1 Motor Controller Period Register (SMC_MCPER)

Setting PER to 0 will shut off all PWM channels as if MCCCx[MCAM] is set to 0 in all channel control registers after the next period timer counter overflow. In this case, the motor controller releases all pins.

NOTE

Programming PER to 1 and setting the MCCTL0[DITH] bit will be managed as if PER is programmed to 0. All PWM channels will be shut off after the next period timer counter overflow.

Address: 0h base + 0h offset = 0h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0					PER										
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SMC_MCPER field descriptions

Field	Description
15–11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PER	PWM Period - PER defines the number of motor controller timer counter clocks a PWM period lasts. The motor controller timer counter is clocked with the frequency f_{TC} . If dither mode is enabled (MCCTL0[DITH] = 1, refer to MCCTL0[DITH], PER[0] is ignored and reads as a 0. In this case PER = 2 * MCDCx[DUTY[10:1]].

59.4.2 Motor Controller Control Register 1 (SMC_MCCTL1)

This register controls the behavior of the analog section of the SMC as well as the interrupt enables.

Address: 0h base + 2h offset = 2h

Bit	7	6	5	4	3	2	1	0
Read	RECIRC	0						MCTOIE
Write								
Reset	0	0	0	0	0	0	0	0

SMC_MCCTL1 field descriptions

Field	Description
7 RECIRC	**Recirculation in (Dual) Full H-Bridge Mode** (refer to MCCTL1[RECIRC]) - RECIRC only affects the outputs in (dual) full H-bridge modes. In half H-bridge mode, the PWM output is always active low. RECIRC = 1 will also invert the effect of the MCDCx[SIGN] bits (refer to MCDCx[SIGN] in (dual) full H-bridge modes. RECIRC must be changed only while no PWM channel is operating in (dual) full H-bridge mode; otherwise, erroneous output pattern may occur.

Table continues on the next page...

SMC_MCCTL1 field descriptions (continued)

Field	Description
	0 Recirculation on the high side transistors. Active state for PWM output is logic low, the static channel will output logic high. 1 Recirculation on the low side transistors. Active state for PWM output is logic high, the static channel will output logic low.
6–1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 MCTOIE	**Motor Controller Timer Counter Overflow Interrupt Enable** 0 Interrupt disabled. 1 Interrupt enabled. An interrupt will be generated when the motor controller timer counter overflow interrupt flag (MCCTL0[MCTOIF]) is set.

59.4.3 Motor Controller Control Register 0 (SMC_MCCTL0)

This register controls the operating mode of the SMC module.

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Address: 0h base + 3h offset = 3h

Bit	7	6	5	4	3	2	1	0
Read	0	MCPRE		MCHME	0	DITH	0	MCTOIF
Write								w1c
Reset	0	0	0	0	0	0	0	0

SMC_MCCTL0 field descriptions

Field	Description
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6–5 MCPRE	**Motor Controller Prescaler Select** - MCPRE determines the prescaler value that sets the motor controller timer counter clock frequency (f_{TC}). The clock source for the prescaler is the peripheral bus clock (f_{BUS}) as shown in . Writes to MCPRE will not affect the timer counter clock frequency fTC until the start of the next PWM period. 00 $f_{TC} = f_{Bus}$ 01 $f_{TC} = f_{Bus}/2$ 10 $f_{TC} = f_{Bus}/4$ 11 $f_{TC} = f_{Bus}/8$
4 MCHME	**Motor Controller Halt Mode Enable (refer to SMC Halt Mode)** 0 Disable SMC halt mode. 1 Enable SMC halt mode.
3 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.

Table continues on the next page...

SMC_MCCTL0 field descriptions (continued)

Field	Description
2 DITH	**Motor Control/Driver Dither Feature Enable** (refer to MCCTL0[DITH] 0 Dither feature is disabled. 1 Dither feature is enabled.
1 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
0 MCTOIF	**Motor Controller Timer Counter Overflow Interrupt Flag** - This bit is set when a motor controller timer counter overflow occurs. The bit is cleared by writing a 1 to the bit. 0 A motor controller timer counter overflow has not occurred since the last reset or since the bit was cleared. 1 A motor controller timer counter overflow has occurred.

59.4.4 Motor Controller Channel Control Register (SMC_MCCC*n*)

Each PWM channel has one associated control register to control output delay, PWM alignment, and output mode. The number of each register refers directly the PWM channel it controls. The relation between channels, pin names and register names is shown in Table 59-2.

NOTE

The SMC will release the pins after the next PWM timer counter overflow without accommodating any channel delay if a single channel has been disabled or if the period register has been cleared or all channels have been disabled. Program one or more inactive PWM frames (duty cycle = 0) before writing a configuration that disables a single channel or the entire SMC.

Address: 0h base + 10h offset + (1d × i), where i=0d to 11d

Bit	7	6	5	4	3	2	1	0
Read	MCOM		MCAM		0		CD	
Write								
Reset	0	0	0	0	0	0	0	0

SMC_MCCC*n* field descriptions

Field	Description
7–6 MCOM	**Output Mode** - MCOM controls the PWM channel's output mode. 00 Half H-bridge mode, PWM on pin MnCxM, pin MnCxP is released 01 Half H-bridge mode, PWM on pin MnCxP, pin MnCxM is released 10 Full H-bridge mode 11 Dual full H-bridge mode

Table continues on the next page...

SMC_MCCC*n* field descriptions (continued)

Field	Description
5–4 MCAM	**PWM Channel Alignment Mode** - MCAM controls the PWM channel's PWM alignment mode and operation. MCAM and MCOM are double buffered. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER[PER] is set to 0) or if a timer counter overflow occurs. Reads of the register return the most recent written value, which are not necessarily the currently active values. 00 Channel disabled 01 Left aligned 10 Right aligned 11 Center aligned
3–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
CD	**PWM Channel Delay** - Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks. The delay will be n/f_{TC} . 00 Zero PWM clocks channel delay 01 One PWM clock channel delay 10 Two PWM clocks channel delay 11 Three PWM clocks channel delay

59.4.5 Motor Controller Duty Cycle Register (SMC_MCDC*n*)

Each duty cycle register sets the sign and duty functionality for the respective PWM channel. The number of each register refers directly to the PWM channel it controls. The relation between channels, pin names and register names is shown in Table 59-2.

To prevent the output from inconsistent signals, the duty cycle registers are double buffered. The SMC module will use working registers to generate the output signals. The working registers are copied from the bus accessible registers at the following conditions:

- MCPER[PER] is set to 0 (all channels are disabled in this case)
- MCCCx[MCAM] of the respective channel is set to 0 (channel is disabled)
- A PWM timer counter overflow occurs while in half H-bridge or full H-bridge mode
- A PWM channel pair is configured to work in Dual Full H-Bridge mode and a PWM timer counter overflow occurs after the odd[1] duty cycle register of the channel pair has been written.

In this way, the output of the PWM will always be either the old PWM waveform or the new PWM waveform, not some variation in between.

1. Odd duty cycle register: MCDCx+1, x = 2xn

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active sign, duty cycle, and dither functionality due to the double buffering scheme.

Address: 0h base + 20h offset + (2d × i), where i=0d to 11d

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	SIGN					DUTY										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SMC_MCDC*n* field descriptions

Field	Description
15–11 SIGN	Sign Bit - The SIGN[4] bit is used to define which output will drive the PWM signal in (dual) full-H-bridge modes. The SIGN[4] bit has no effect in half-bridge modes. See MCDCx[SIGN] and Table 59-3 for detailed information about the impact of MCCTL1[RECIRC] and SIGN[4] bit on the PWM output. Sign Bit Extension - The SIGN[3:0] bits replicate the SIGN[4] bit towards the DUTY field to make the whole register a signed representation for the duty cycle length.
DUTY	Duty Cycle Length - DUTY defines the number of motor controller timer counter clocks the corresponding output is driven low (MCCTL1[RECIRC] = 0) or is driven high (MCCTL1[RECIRC] = 1). Setting all bits to 0 will give a static high output in case of MCCTL1[RECIRC] = 0; otherwise, a static low output. Values greater than or equal to the contents of the period register will generate a static low output in case of MCCTL1[RECIRC] = 0, or a static high output if MCCTL1[RECIRC] = 1.

59.4.6 Short-circuit Detector Time-out Register (SMC_MCSDTO)

Address: 0h base + 43h offset = 43h

Bit	7	6	5	4	3	2	1	0
Read Write	TOUT							
Reset	0	0	0	0	0	0	0	0

SMC_MCSDTO field descriptions

Field	Description
TOUT	**Time-out** — The value TOUT is an unsigned 8-bit number. This value is used as load value for the short-circuit detection counters. This value is applied to all 24 short-circuit detection blocks. Due to synchronization and sampling, TOUT must always be larger than 2 (see also Short-circuit Detection).

59.4.7 Short-circuit Detector Enable Register (SMC_MCSDE*n*)

Address: 0h base + 45h offset + (1d × i), where i=0d to 2d

Bit	7	6	5	4	3	2	1	0
Read Write	SDEN							
Reset	0	0	0	0	0	0	0	0

SMC_MCSDE*n* field descriptions

Field	Description
SDEN	Short-Circuit Detector Enable - Each short-circuit detector can be enabled or disabled according to the mapping described in Table 59-6. The short-circuit detector of a given pin is enabled if the related enable bit is set to 1.

59.4.8 Short-circuit Detector Interrupt Enable Register (SMC_MCSDIEN*n*)

Address: 0h base + 49h offset + (1d × i), where i=0d to 2d

Bit	7	6	5	4	3	2	1	0
Read Write	SDIE							
Reset	0	0	0	0	0	0	0	0

SMC_MCSDIEN*n* field descriptions

Field	Description
SDIE	**Short-Circuit Detector Interrupt Enable** - The interrupt of each short-circuit detector can individually be enabled or disabled according to the mapping described in Table 59-6. The short-circuit detector interrupt of a given pin is enabled if the related interrupt enable bit is set to 1.

59.4.9 Short-circuit Detector Interrupt Register (SMC_MCSDI*n*)

Address: 0h base + 4Dh offset + (1d × i), where i=0d to 2d

Bit	7	6	5	4	3	2	1	0
Read Write	SDIF							
Reset	0	0	0	0	0	0	0	0

SMC_MCSDI*n* field descriptions

Field	Description
SDIF	Short-circuit Detector Interrupt Flag - In case of a detected short-circuit, the corresponding bit according to the mapping in Table 59-6 is set in the short-circuit detector interrupt register. If this specific interrupt is also enabled in the interrupt enable register MCSDIEN0, than this event will rise an external interrupt.

59.5 Functional Description

59.5.1 Modes of Operation

59.5.1.1 PWM Output Modes

The SMC is configured between three output modes.

- Dual full H-bridge mode can be used to control either a stepper motor or a 360° air core instrument. In this case two PWM channels are combined.
- In full H-bridge mode, each PWM channel is updated independently.
- In half H-bridge mode, one pin of the PWM channel can generate a PWM signal to control a 90° air core instrument (or other load requiring a PWM signal) and the other pin is unused.

The mode of operation for PWM channel x is determined by the output mode bits MCCCx[MCOM]. After a reset occurs, each PWM channel will be disabled, the corresponding pins are released.

Each PWM channel consists of two pins. One output pin will generate a PWM signal. The other will operate as logic high or low output depending on the state of the recirculation bit MCCTL1[RECIRC] (refer to MCCTL1[RECIRC]), while in (dual) full H-bridge mode, or will be released, while in half H-bridge mode. The state of the sign bit MCDCx[SIGN[4]] in the duty cycle register determines the pin where the PWM signal is driven in full H-bridge mode. While in half H-bridge mode, the state of the released pin is determined by other modules associated with this pin.

Associated with each PWM channel pair n are two PWM channels, x and x + 1, where x = 2 * n and n (0,1,2... 5) is the PWM channel pair number. Duty cycle register x controls the sign of the PWM signal (which pin drives the PWM signal) and the duty cycle of the PWM signal for SMC channel x. The pins associated with PWM channel x are MnC0P and MnC0M. Similarly, duty cycle register x + 1 controls the sign of the PWM signal and the duty cycle of the PWM signal for channel x + 1. The pins associated with PWM channel x + 1 are MnC1P and MnC1M. This is summarized in Table 59-2.

Table 59-2. Corresponding Registers and Pin Names for each PWM Channel Pair

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
n	MCCCx	MCDCx	PWM Channel x, x = 2·n	MnC0M
				MnC0P
	MCCCx+1	MCDCx+1	PWM Channel x+1, x = 2·n	MnC1M
				MnC1P
0	MCCC0	MCDC0	PWM Channel 0	M0C0M

Table continues on the next page...

Table 59-2. Corresponding Registers and Pin Names for each PWM Channel Pair (continued)

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
				M0C0P
	MCCC1	MCDC1	PWM Channel 1	M0C1M
				M0C1P
1	MCCC2	MCDC2	PWM Channel 2	M1C0M
				M1C0P
	MCCC3	MCDC3	PWM Channel 3	M1C1M
				M1C1P
2	MCCC4	MCDC4	PWM Channel 4	M2C0M
				M2C0P
	MCCC5	MCDC5	PWM Channel 5	M2C1M
				M2C1P
3	MCCC6	MCDC6	PWM Channel 6	M3C0M
				M3C0P
	MCCC7	MCDC7	PWM Channel 7	M3C1M
				M3C1P
4	MCCC8	MCDC8	PWM Channel 8	M4C0M
				M4C0P
	MCCC9	MCDC9	PWM Channel 9	M4C1M
				M4C1P
5	MCCC10	MCDC10	PWM Channel 10	M5C0M
				M5C0P
	MCCC11	MCDC11	PWM Channel 11	M5C1M
				M5C1P

59.5.1.2 Relationship Between PWM Mode and PWM Channel Enable

The pair of SMC channels cannot be placed into dual full H-bridge mode unless both SMC channels have been enabled (MCCCx[MCAM] not equal to 0) and dual full H-bridge mode is selected for both PWM channels (MCCCx[MCOM] = 0x3). If only one channel is set to dual full H-bridge mode, this channel will operate in full H-bridge mode, the other as programmed.

59.5.1.3 Relationship Between Sign, Duty, Dither, RECIRC, Period, and PWM Mode Functions

59.5.1.3.1 PWM Alignment Modes

Each PWM channel can be programmed individually to three different alignment modes. The alignment mode is determined by the MCCCx[MCAM] bits in the corresponding channel control register.

Left aligned (MCCCx[MCAM] = 0x1): The output will start active (low if MCCTL1[RECIRC] = 0 or high if MCCTL1[RECIRC] = 1) and will turn inactive (high if MCCTL1[RECIRC] = 0 or low if MCCTL1[RECIRC] = 1) after the number of counts specified by the corresponding duty cycle register.

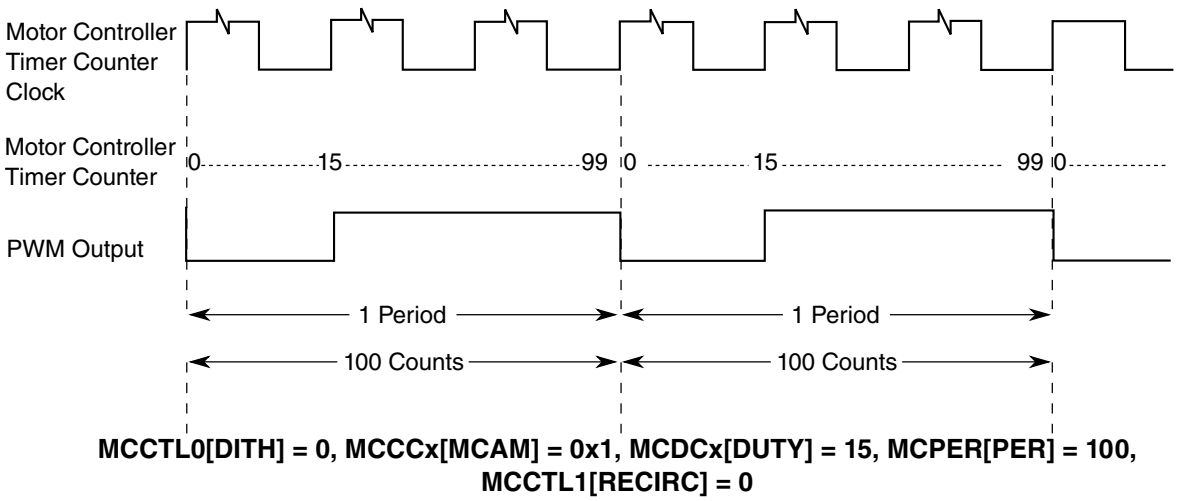
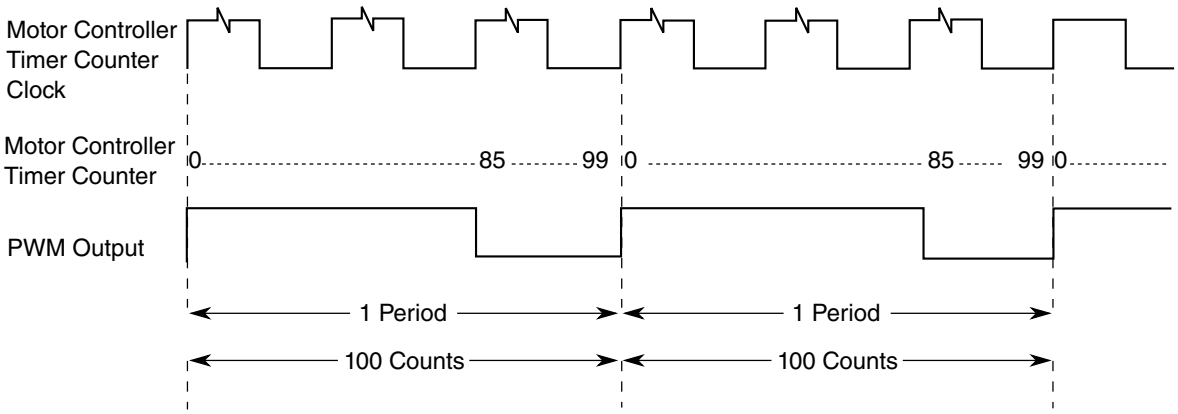


Figure 59-2. Left Aligned

Right aligned (MCCCx[MCAM] = 0x2): The output will start inactive (high if MCCTL1[RECIRC] = 0 and low if

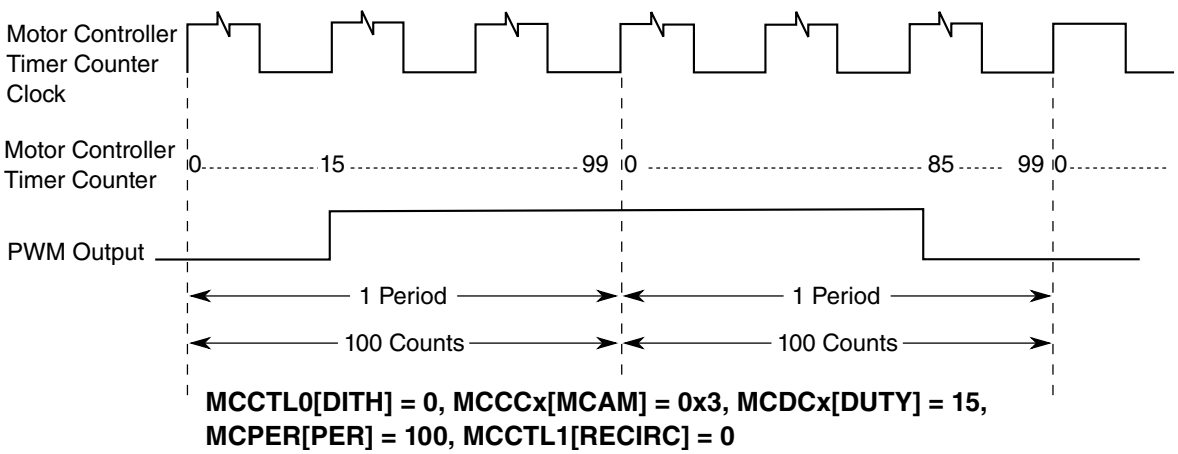
MCCTL1[RECIRC] = 1) and will turn active after the number of counts specified by the difference of the contents of period register and the corresponding duty cycle register.



MCCTL0[DITH] = 0, MCCCx[MCAM] = 0x2, MCDCx[DUTY] = 15, MCPER[PER] = 100, MCCTL1[RECIRC] = 0

Figure 59-3. Right Aligned

Center aligned (MCCCx[MCAM] = 0x3): Even periods will be output left aligned, odd periods will be output right aligned. PWM operation starts with the even period after the channel has been enabled. PWM operation in center aligned mode might start with the odd period if the channel has not been disabled before changing the alignment mode to center aligned.



MCCTL0[DITH] = 0, MCCCx[MCAM] = 0x3, MCDCx[DUTY] = 15, MCPER[PER] = 100, MCCTL1[RECIRC] = 0

Figure 59-4. Center Aligned

59.5.1.3.2 Sign Bit (MCDCx[SIGN])

Assuming MCCTL1[RECIRC] = 0 (the active state of the PWM signal is low), when the MCDCx[SIGN[4]] bit for the corresponding channel is cleared, MnC0P (if the PWM channel number is even, n = 0, 1, 2...5, see Table 59-2) or MnC1P (if the PWM channel number is odd, n = 0, 1, 2...5 see Table 59-2), outputs a logic high while in (dual) full H-bridge mode. In half H-bridge mode the state of the MCDCx[SIGN[4]] bit has no effect. The PWM output signal is generated on MnC0M (if the PWM channel number is even, n = 0, 1, 2...5, see Table 59-2) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2...5).

Assuming MCCTL1[RECIRC] = 0 (the active state of the PWM signal is low), when the MCDCx[SIGN[4]] bit for the corresponding channel is set, MnC0M (if the PWM channel number is even, n = 0, 1, 2...5, see Table 59-2) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2...5, see Table 59-2), outputs a logic high while in (dual) full H-bridge mode. In half H-bridge mode the state of the MCDCx[SIGN[4]] bit has no effect. The PWM output signal is generated on MnC0P (if the PWM channel number is even, n = 0, 1, 2...5, see Table 59-2) or MnC1P (if the PWM channel number is odd, n = 0, 1, 2...5) .

Setting MCCTL1[RECIRC] = 1 will also invert the effect of the MCDCx[SIGN[4]] bit such that while MCDCx[SIGN[4]] = 0, MnC0P or MnC1P will generate the PWM signal and MnC0M or MnC1M will be a static low output. While MCDCx[SIGN[4]] = 1, MnC0M or MnC1M will generate the PWM signal and MnC0P or MnC1P will be a static low output. In this case the active state of the PWM signal will be high.

See the following table for detailed information about the impact of MCDCx[SIGN[4]] and MCCTL1[RECIRC] bit on the PWM output.

Table 59-3. Impact of MCCTL1[RECIRC] and MCDCx[SIGN[4]] Bit on the PWM Output

Output Mode	MCCTL1[RECIRC]	MCDCx[SIGN[4]]	MnCyM	MnCyP
(Dual) Full H-Bridge	0	0	$\overline{\text{PWM}}$[1]	1
(Dual) Full H-Bridge	0	1	1	$\overline{\text{PWM}}$
(Dual) Full H-Bridge	1	0	0	PWM[2]
(Dual) Full H-Bridge	1	1	PWM	0
Half H-Bridge: PWM on MnCyM	Don't care	Don't care	$\overline{\text{PWM}}$	—[3]
Half H-Bridge: PWM on MnCyP	Don't care	Don't care	—	$\overline{\text{PWM}}$

1. $\overline{\text{PWM}}$: The PWM signal is low active. e.g., the waveform starts with 0 in left aligned mode. Output M generates the PWM signal. Output P is static high.
2. PWM: The PWM signal is high active. e.g., the waveform starts with 1 in left aligned mode. output P generates the PWM signal. Output M is static low.
3. The state of the output transistors is not controlled by the SMC.

59.5.1.3.3 Recirculation Bit (MCCTL1[RECIRC])

The MCCTL1[RECIRC] bit controls the flow of the recirculation current of the load. Setting MCCTL1[RECIRC] = 0 will cause recirculation current to flow through the high side transistors, and MCCTL1[RECIRC] = 1 will cause the recirculation current to flow through the low side transistors. The MCCTL1[RECIRC] bit is only active in (dual) full H-bridge modes.

Effectively, MCCTL1[RECIRC] = 0 will cause a static high output on the output terminal not driven by the PWM, MCCTL1[RECIRC] = 1 will cause a static low output on the output terminals not driven by the PWM. To achieve the same current direction,

the MCDCx[SIGN[4]] bit behavior is inverted if MCCTL1[RECIRC] = 1. Figure 59-5, Figure 59-6, Figure 59-7, and Figure 59-8 illustrate the effect of the MCCTL1[RECIRC] bit in (dual) full H-bridge modes.

MCCTL1[RECIRC] bit must be changed only while no PWM channel is operated in (dual) full H-bridge mode.

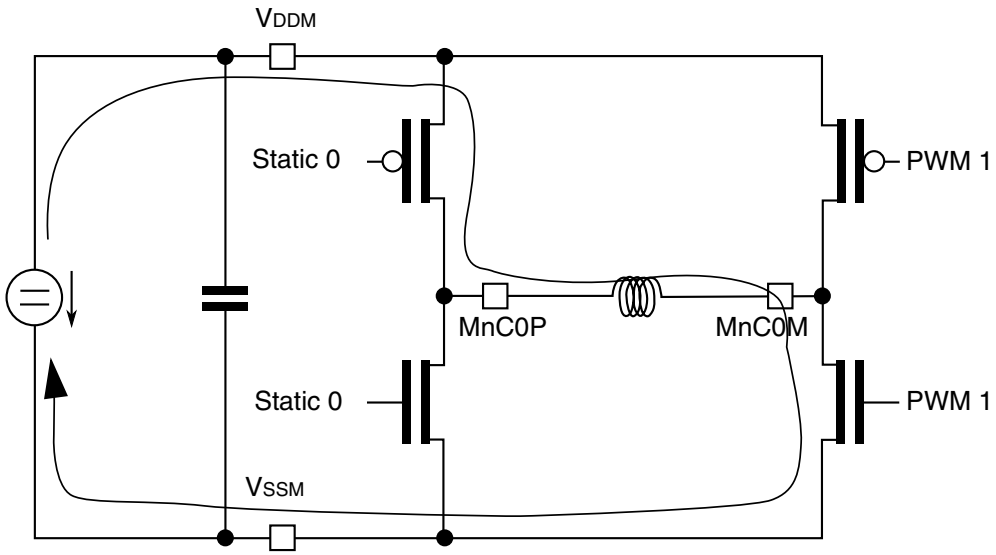


Figure 59-5. PWM Active Phase, MCCTL1[RECIRC] = 0, MCDCx[SIGN[4]] = 0

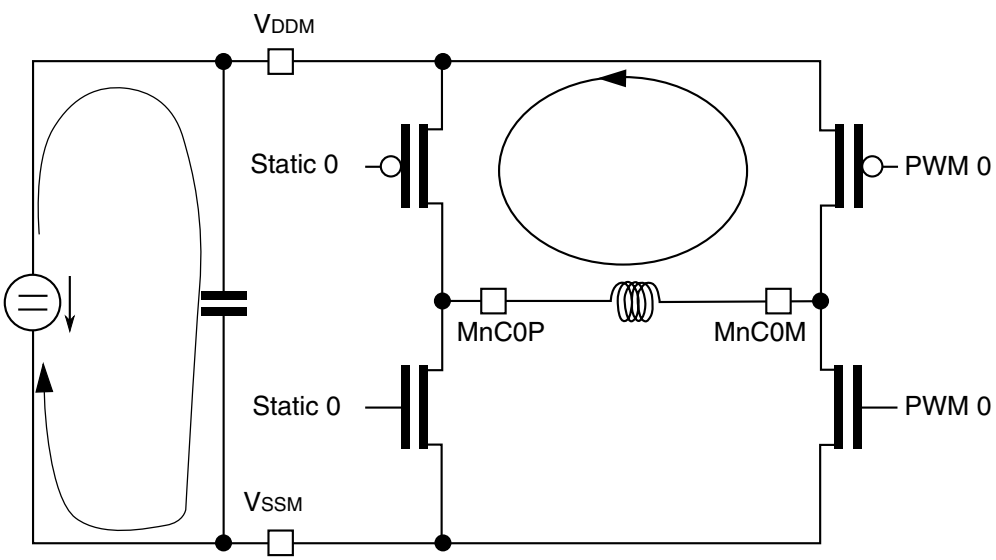


Figure 59-6. PWM Passive Phase, MCCTL1[RECIRC] = 0, MCDCx[SIGN[4]] = 0

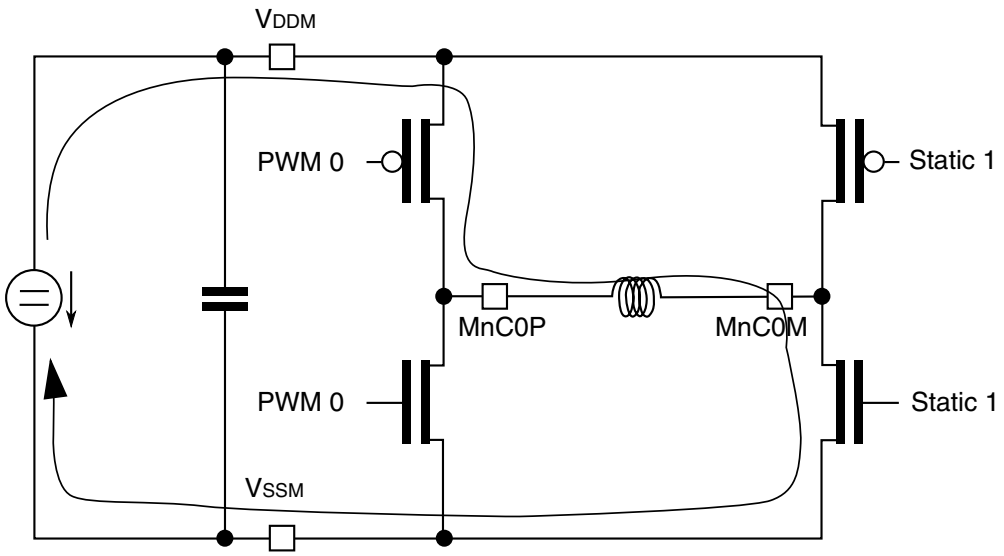


Figure 59-7. PWM Active Phase, MCCTL1[RECIRC] = 1, MCDCx[SIGN[4]] = 0

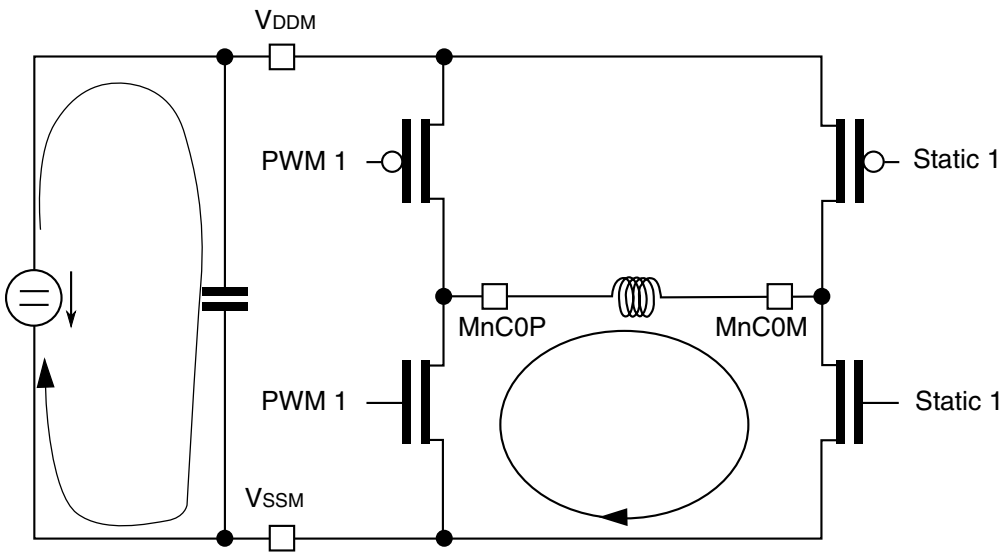


Figure 59-8. PWM Passive Phase, MCCTL1[RECIRC] = 1, MCDCx[SIGN[4]] = 0

59.5.1.3.4 Relationship Between MCCTL1[RECIRC] Bit, MCDCx[SIGN[4]] Bit, MCCCx[MCOM] Bits, PWM State, and Output Transistors

Please refer to Figure 59-9 for the output transistor assignment.

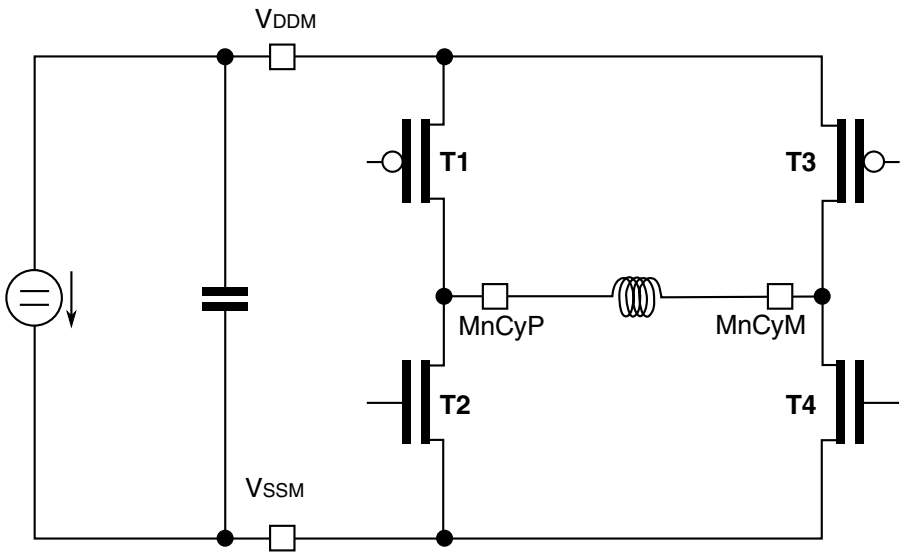


Figure 59-9. Output Transistor Assignment

Table 59-5 illustrates the state of the output transistors in different states of the SMC module. '—' means that the state of the output transistor is not controlled by the SMC.

Table 59-4. State of Output Transistors in Various Modes

Mode	MCCCx[MCOM]	PWM Duty	MCCTL1[RECIRC]	MCDCx[SIGN[4]]	T1	T2	T3	T4
Off	Don't care	—	Don't care	Don't care	—	—	—	—
Half H-Bridge	0x0	Active	Don't care	Don't care	—	—	OFF	ON
Half H-Bridge	0x0	Passive	Don't care	Don't care	—	—	ON	OFF
Half H-Bridge	0x1	Active	Don't care	Don't care	OFF	ON	—	—
Half H-Bridge	0x1	Passive	Don't care	Don't care	ON	OFF	—	—
(Dual) Full	0x2 or 0x3	Active	0	0	ON	OFF	OFF	ON
(Dual) Full	0x2 or 0x3	Passive	0	0	ON	OFF	ON	OFF
(Dual) Full	0x2 or 0x3	Active	0	1	OFF	ON	ON	OFF
(Dual) Full	0x2 or 0x3	Passive	0	1	ON	OFF	ON	OFF
(Dual) Full	0x2 or 0x3	Active	1	0	ON	OFF	OFF	ON
(Dual) Full	0x2 or 0x3	Passive	1	0	OFF	ON	OFF	ON
(Dual) Full	0x2 or 0x3	Active	1	1	OFF	ON	ON	OFF
(Dual) Full	0x2 or 0x3	Passive	1	1	OFF	ON	OFF	ON

59.5.1.3.5 Dither Bit (MCCTL0[DITH])

The purpose of the dither mode is to increase the minimum length of output pulses without decreasing the PWM resolution, in order to limit the pulse distortion introduced by the slew rate control of the outputs. If dither mode is selected the output pattern will repeat after two timer counter overflows. For the same output frequency, the shortest

output pulse will have twice the length while dither feature is selected. To achieve the same output frame frequency, the prescaler of the SMC module has to be set to twice the division rate if dither mode is selected; e.g., with the same prescaler division rate the repeat rate of the output pattern is the same as well as the shortest output pulse with or without dither mode selected.

The MCCTL0[DITH] bit enables or disables the dither function.

MCCTL0[DITH] = 0: dither function is disabled.

When MCCTL0[DITH] is cleared and assuming left aligned operation and MCCTL1[RECIRC] = 0, the PWM output will start at a logic low level at the beginning of the PWM period (motor controller timer counter = 0x000). The PWM output remains low until the motor controller timer counter matches the 11-bit PWM duty cycle value MCDCx[DUTY]. When a match (output compare between motor controller timer counter and MCDCx[DUTY]) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the contents of MCPER[PER] – 1). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level. This completes one PWM period. The PWM period repeats every MCPER[PER] counts of the motor controller timer counter. If MCDCx[DUTY] >= MCPER[PER], the output will be static low. If MCDCx[DUTY] = 0, the output will be continuously at a logic high level. The relationship between the motor controller timer counter clock, motor controller timer counter value, and PWM output while MCCTL0[DITH] = 0 is shown in the following figure:.

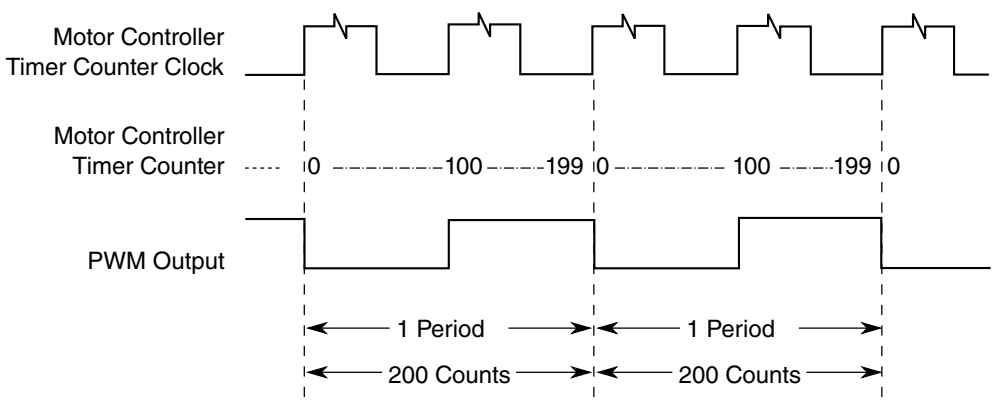


Figure 59-10. PWM Output: MCCTL0[DITH] = 0, MCCCx[MCAM] = 0x1, MCDCx[DUTY] = 100, MCPER[PER] = 200, MCCTL1[RECIRC] = 0

MCCTL0[DITH] = 1: dither function is enabled

Please note if MCCTL0[DITH] = 1, the bit MCPER[PER[0]] will be internally forced to 0 and read always as 0.

When MCCTL0[DITH] is set and assuming left aligned operation and MCCTL1[RECIRC] = 0, the PWM output will start at a logic low level at the beginning of the PWM period (when the motor controller timer counter = 0). The PWM output remains low until the motor controller timer counter matches the 10-bit PWM duty cycle value MCDCx[DUTY]. When a match (output compare between motor controller timer counter and MCDCx[DUTY]) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the value defined by MCPER[PER[10:1]] – 1). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level. This completes the first half of the PWM period. During the second half of the PWM period, the PWM output will remain at a logic low level until either the motor controller timer counter matches the 10-bit PWM duty cycle value MCDCx[DUTY] if MCDCx[DUTY[0]]= 0, or the motor controller timer counter matches the 10-bit PWM duty cycle value + 1 (the value of MCDCx[DUTY[10:1]] is incremented by 1 and is compared with the motor controller timer counter value) if MCDCx[DUTY[0]] = 1 for the corresponding channel. When a match occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the value defined by MCPER[PER[10:1]] – 1). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level.

This process will repeat every number of counts of the motor controller timer counter defined by the period register contents (MCPER[PER]). If the output is neither set to 0% nor to 100% there will be four edges on the PWM output per PWM period in this case. Therefore, the PWM output compare function will alternate between MCDCx[DUTY] and MCDCx[DUTY] + 1 every half PWM period if MCDCx[DUTY[0]] for the corresponding channel is set to 1. The relationship between the motor controller timer counter clock (fTC), motor controller timer counter value, and left aligned PWM output if MCCTL0[DITH] = 1 is shown in Figure 59-12 and Figure 59-13. Figure 59-14 and Figure 59-15 show right aligned and center aligned PWM operation respectively, with dither feature enabled and MCDCx[DUTY[0]] = 1. Please note: In the following examples, the MCPER[PER] value, which is, if MCCTL0[DITH] = 1, always an even number.

Note

The MCCTL0[DITH] bit must be changed only if the SMC is disabled (all channels disabled or period register cleared) to avoid erroneous waveforms.

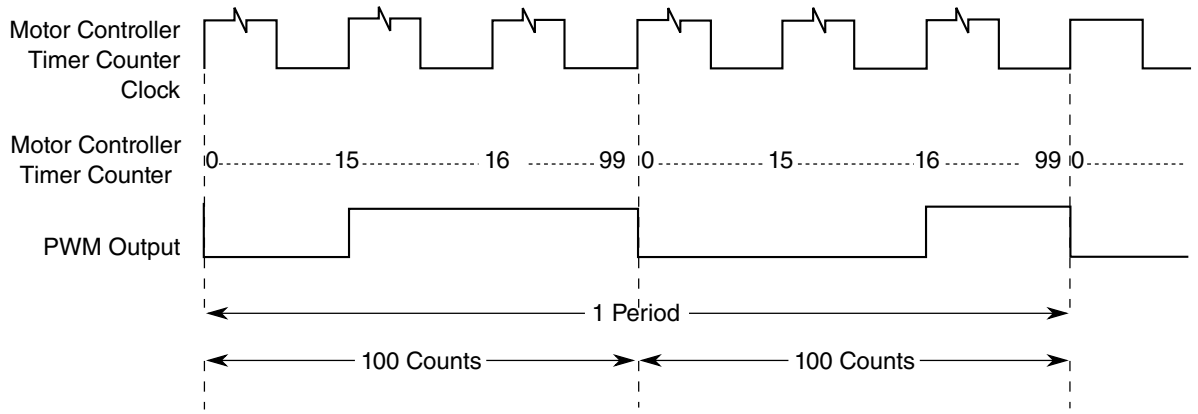


Figure 59-11. PWM Output: MCCTL0[DITH] = 1, MCCCx[MCAM] = 0x1, MCDCx[DUTY] = 31, MCPER[PER] = 200, MCCTL1[RECIRC] = 0

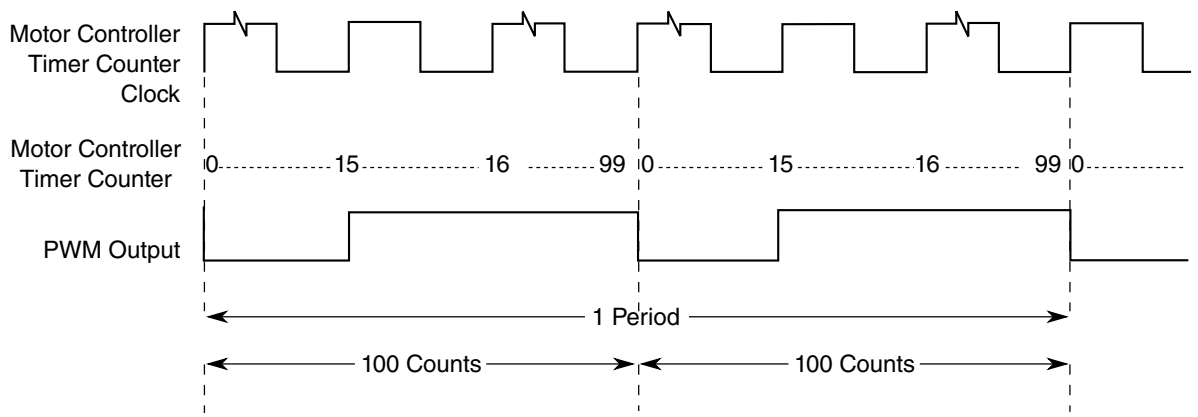


Figure 59-12. PWM Output: MCCTL0[DITH] = 1, MCCCx[MCAM] = 0x1, MCDCx[DUTY] = 30, MCPER[PER] = 200, MCCTL1[RECIRC] = 0

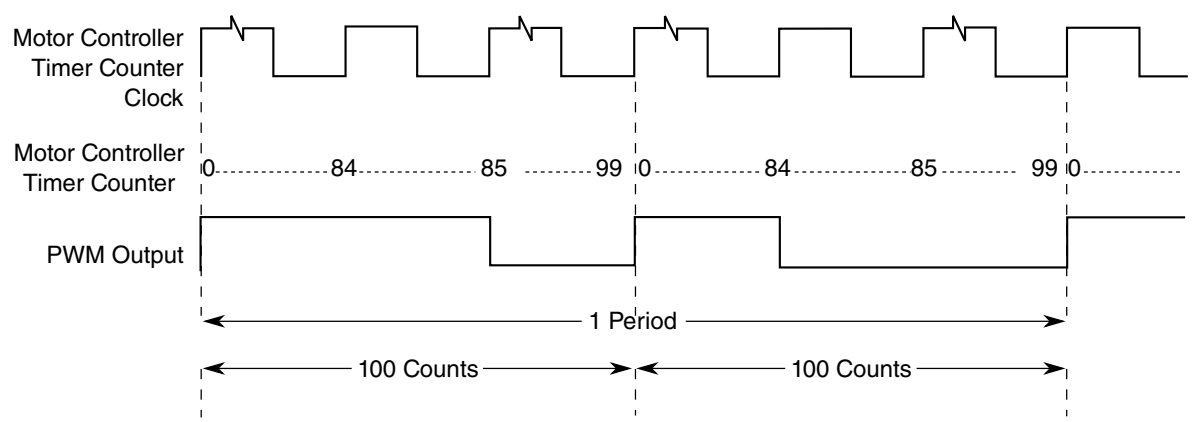


Figure 59-13. PWM Output: MCCTL0[DITH] = 1, MCCCx[MCAM] = 0x2, MCDCx[DUTY] = 31, MCPER[PER] = 200, MCCTL1[RECIRC] = 0

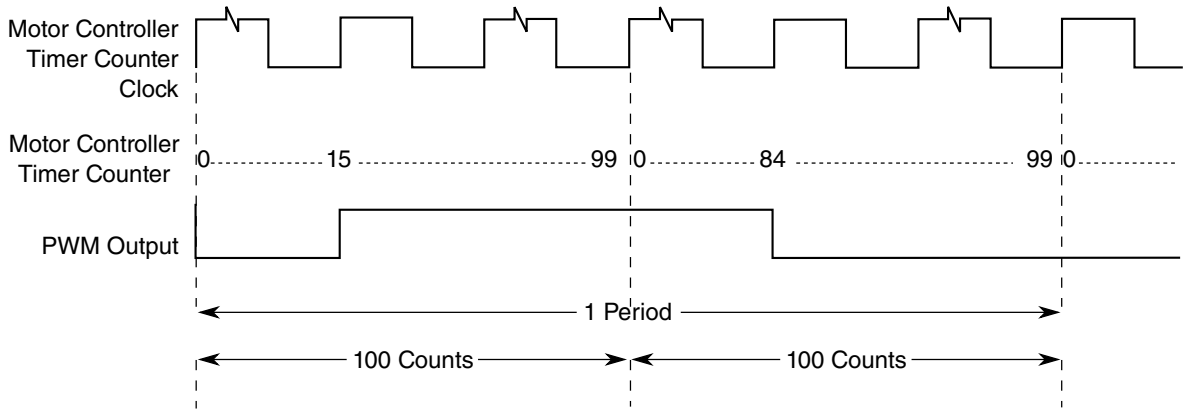


Figure 59-14. PWM Output: MCCTL0[DITH] = 1, MCCCx[MCAM] = 0x3, MCDCx[DUTY] = 31, MCPER[PER] = 200, MCCTL1[RECIRC] = 0

59.5.2 PWM Duty Cycle

The PWM duty cycle for the SMC channel x can be determined by dividing the decimal representation of the bits MCDCx[DUTY] by the decimal representation of the bits MCPER[PER] and multiplying the result by 100% as shown in Equation 20 on page 2206.

$$\text{EffectivePWMChannel}X\ \%\ \text{DutyCycle} = \frac{\text{DUTY}}{\text{MCPER}}.100\ \%$$

Equation 20

Note

x = PWM Channel Number = 0, 1, 2, 3 … 11. This equation is only valid if MCDCx[DUTY] <= MCPER[PER] and MCPER[PER] is not equal to 0.

Whenever MCDCx[DUTY] >= MCPER[PER], a constant low level (MCCTL1[RECIRC] = 0) or high level (MCCTL1[RECIRC] = 1) will be output.

59.5.3 Motor Controller Counter Clock Source

The following figure shows how the PWM motor controller timer counter clock source is selected.

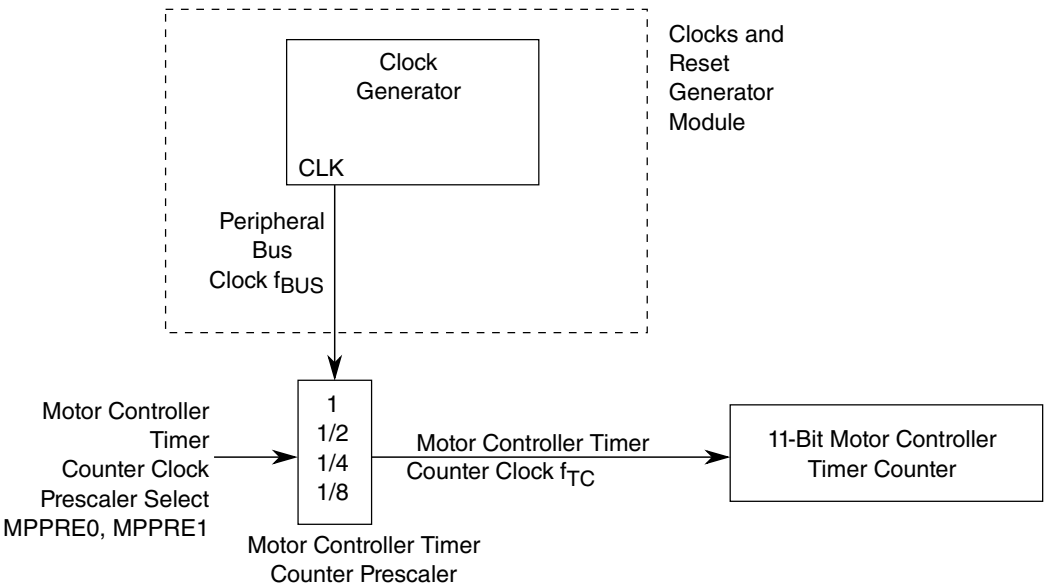


Figure 59-15. Motor Controller Counter Clock Selection

The peripheral bus clock is the source for the motor controller counter prescaler. The motor controller counter clock rate, f_{TC}, is set by selecting the appropriate prescaler value. The prescaler is selected with the MCCTL0[MCPRE] bits. The SMC channel frequency of operation can be calculated using Equation 21 on page 2207

$$\mathrm{MotorChannelFrequency(Hz)} = \frac{f_{TC}}{\mathrm{MCPER} \cdot M}$$

Equation 21

if MCCTL0[DITH] = 0.

The SMC channel frequency of operation can be calculated using Equation 22 on page 2207

$$\mathrm{MotorChannelFrequency(Hz)} = \frac{f_{TC}}{\mathrm{MCPER} \cdot M/2}$$

Equation 22

if MCCTL0[DITH] = 1.

Note

Both equations are only valid if MCPER[PER] is not equal to 0. M = 1 for left or right aligned mode, M = 2 for center aligned mode.

Table 59-5 shows examples of the SMC channel frequencies that can be generated based on different peripheral bus clock frequencies and the prescaler value.

Table 59-5. SMC Channel Frequencies (Hz), MCPER[PER] = 256, MCCTL0[DITH] = 0, MCCCx[MCAM] = 0x2, 0x1

Prescaler	Peripheral Bus Clock Frequency				
	16 MHz	10 MHz	8 MHz	5 MHz	4 MHz
1	62500	39063	31250	19531	15625
1/2	31250	19531	15625	9766	7813
1/4	15625	9766	7813	4883	3906
1/8	7813	4883	3906	2441	1953

Note

Due to the selectable slew rate control of the outputs, clipping may occur on short output pulses.

59.5.4 Output Switching Delay

In order to prevent large peak current draw from the motor power supply, selectable delays can be used to stagger the high logic level to low logic level transitions on the SMC outputs. The timing delay, td, is determined by the MCCCx[CD] bits in the corresponding channel control register and is selectable between 0, 1, 2, or 3 motor controller timer counter clock cycles.

Note

A PWM channel gets disabled at the next timer counter overflow without notice of the switching delay.

59.5.5 SMC Halt Mode

The system can send a signal to the SMC block to request the SMC halt mode. Whether the SMC block reacts on the signal and goes into SMC halt mode depends on the setting of the MCCTL0[MCHME] bit. MCCTL0[MCHME] = 1: The system request for SMC halt mode is taken into account.

All module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the MCCTL1[RECIRC] bit during SMC halt mode{vc_6}. The SMC module registers stay the same as they were prior to entering SMC halt mode{vc_6}. Therefore, after exiting from SMC halt mode, the associated port pins will resume to the same functionality they had prior to entering SMC halt mode .

- MCCTL0[MCHME] = 0: The external request for SMC halt mode is ignored. The PWM clocks continue to run and the associated port pins maintain the functionality they had before the SMC halt mode request.

59.5.6 SMC Stop Mode

If the SMC module is requested to enter the stop mode, all module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the MCCTL1[RECIRC] bit. The SMC module registers stay the same as they were prior to entering SMC stop mode.Therefore, after exiting from SMC stop mode, the associated port pins will resume to the same functionality they had prior to entering SMC stop mode.

59.5.7 Short-circuit Detection

Each PWM pin is equipped with a short-circuit detection function. Hence, 24 instances (4 for each PWM module) of the short-circuit detector exist.

Table 59-6. Cross-reference PWM Signal to Short-circuit Detector Register Bits

Short-Circuit Detector Index *sd*	PWM Channel	Pin Name	Related SD Enable Bit	Related SD Int Enable Bit	Related SD Int Bit
23	10	M5C0M	MCSDE2[SDEN[7]]	MCSDIEN2[SDIE[7]]	MCSDI2[SDIF[7]]
22	8	M4C0M	MCSDE2[SDEN[6]]	MCSDIEN2[SDIE[6]]	MCSDI2[SDIF[6]]
21	6	M3C0M	MCSDE2[SDEN[5]]	MCSDIEN2[SDIE[5]]	MCSDI2[SDIF[5]]
20	4	M2C0M	MCSDE2[SDEN[4]]	MCSDIEN2[SDIE[4]]	MCSDI2[SDIF[4]]
19	2	M1C0M	MCSDE2[SDEN[3]]	MCSDIEN2[SDIE[3]]	MCSDI2[SDIF[3]]
18	0	M0C0M	MCSDE2[SDEN[2]]	MCSDIEN2[SDIE[2]]	MCSDI2[SDIF[2]]
17	11	M5C1M	MCSDE2[SDEN[1]]	MCSDIEN2[SDIE[1]]	MCSDI2[SDIF[1]]
16	9	M4C1M	MCSDE2[SDEN[0]]	MCSDIEN2[SDIE[0]]	MCSDI2[SDIF[0]]
15	7	M3C1M	MCSDE1[SDEN[7]]	MCSDIEN1[SDIE[7]]	MCSDI1[SDIF[7]]
14	5	M2C1M	MCSDE1[SDEN[6]]	MCSDIEN1[SDIE[6]]	MCSDI1[SDIF[6]]
13	3	M1C1M	MCSDE1[SDEN[5]]	MCSDIEN1[SDIE[5]]	MCSDI1[SDIF[5]]
12	1	M0C1M	MCSDE1[SDEN[4]]	MCSDIEN1[SDIE[4]]	MCSDI1[SDIF[4]]
11	10	M5C0P	MCSDE1[SDEN[3]]	MCSDIEN1[SDIE[3]]	MCSDI1[SDIF[3]]
10	8	M4C0P	MCSDE1[SDEN[2]]	MCSDIEN1[SDIE[2]]	MCSDI1[SDIF[2]]
9	6	M3C0P	MCSDE1[SDEN[1]]	MCSDIEN1[SDIE[1]]	MCSDI1[SDIF[1]]
8	4	M2C0P	MCSDE1[SDEN[0]]	MCSDIEN1[SDIE[0]]	MCSDI1[SDIF[0]]
7	2	M1C0P	MCSDE0[SDEN[7]]	MCSDIEN0[SDIE[7]]	MCSDI0[SDIF[7]]

Table continues on the next page...

Table 59-6. Cross-reference PWM Signal to Short-circuit Detector Register Bits (continued)

Short-Circuit Detector Index *sd*	PWM Channel	Pin Name	Related SD Enable Bit	Related SD Int Enable Bit	Related SD Int Bit
6	0	M0C0P	MCSDE0[SDEN[6]]	MCSDIEN0[SDIE[6]]	MCSDI0[SDIF[6]]
5	11	M5C1P	MCSDE0[SDEN[5]]	MCSDIEN0[SDIE[5]]	MCSDI0[SDIF[5]]
4	9	M4C1P	MCSDE0[SDEN[4]]	MCSDIEN0[SDIE[4]]	MCSDI0[SDIF[4]]
3	7	M3C1P	MCSDE0[SDEN[3]]	MCSDIEN0[SDIE[3]]	MCSDI0[SDIF[3]]
2	5	M2C1P	MCSDE0[SDEN[2]]	MCSDIEN0[SDIE[2]]	MCSDI0[SDIF[2]]
1	3	M1C1P	MCSDE0[SDEN[1]]	MCSDIEN0[SDIE[1]]	MCSDI0[SDIF[1]]
0	1	M0C1P	MCSDE0[SDEN[0]]	MCSDIEN0[SDIE[0]]	MCSDI0[SDIF[0]]

Each single short-circuit detector is a timer, measuring the time during which the signals PWM and FB are not equal (see Figure 59-17). If this time is greater than or equal to the time represented by MCSDTO[TOUT], then a short-circuit is assumed.

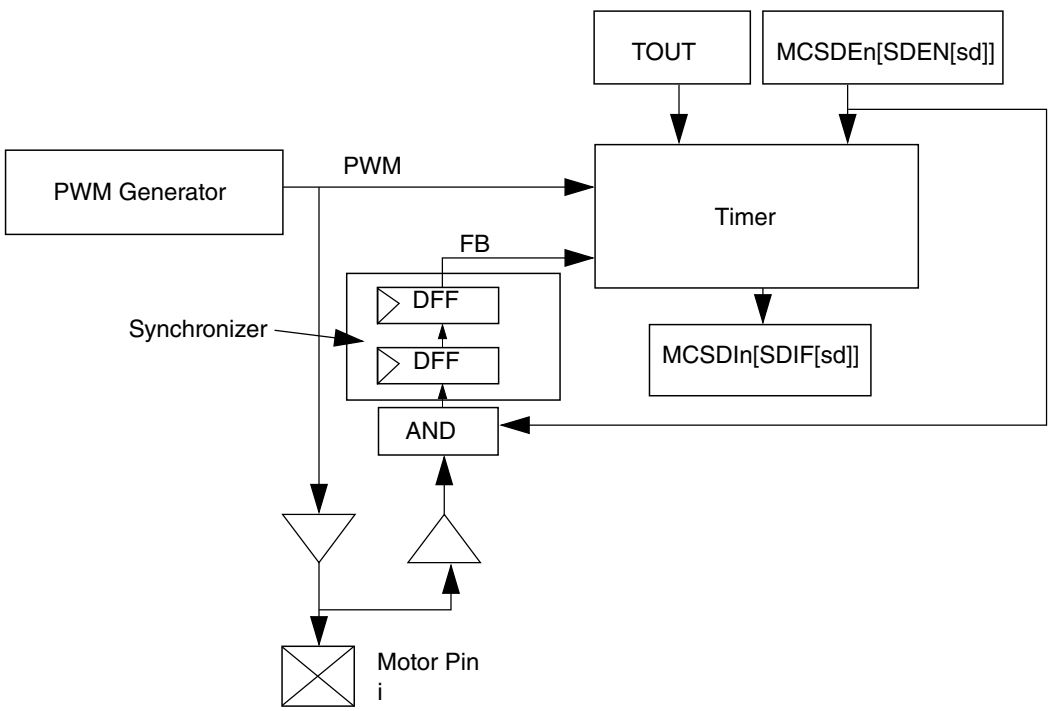
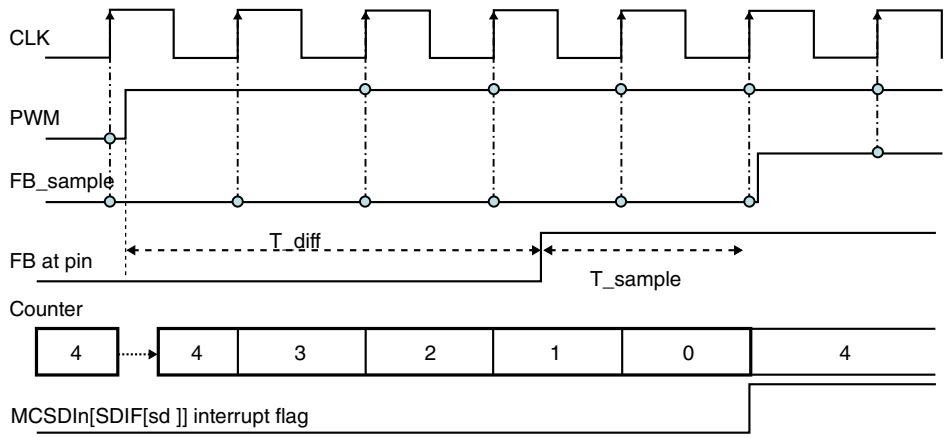


Figure 59-16. Short-circuit Detector Overview



T_sample	:Sample and synchronization delay
T_diff	:Delay between FB at pin and the internal PWM signal
PWM	:Signal from motor controller
FB at pin	:This is the signal directly after the input driver of the pad s ignal
FB_Sample	:Pad signal after sampling and synchronization

Figure 59-17. Example for MCSDTO[TOUT] = 4

- Hence, if PWM != FB, the timer starts counting if the short-circuit detector is enabled at least one clock cycle before (see MCSDE0, MCSDE1 or MCSDE2")
- If PWM == FB, the timer stops and is reset to the time-out value MCSDTO[TOUT] in order to be ready for the next transaction
- IF PWM != FB and the timer state is larger or equal MCSDTO[TOUT], than
  - One of the interrupt flags MCSDI0[SDIF], MCSDE1[SDIF] or MCSDI2[SDIF] is set in order to flag a short-circuit.
  - The interrupt flag is cleared by writing one, by reset or by disabling the short-circuit detector
  - The timer is stopped and reloaded with the time-out value MCSDTO[TOUT] in order to be ready for the next transaction
- If a short-circuit detector is disabled (MCSDEn[SDEN[*sd*]] == 0), the related short-circuit detector counter is halted and preloaded with the register value of MCSDTO[TOUT]. The related bit in MCSDIn[SDIF[*sd*]] of this specific short-circuit detector is set to 0. This means that, if all short-circuit detectors are disabled, all bits of MCSDIn stay at 0. No interrupt from the detector can be generated independently of the interrupt mask in MCSDIENn.
- In case of low power-modes, the state of the short-circuit detector is frozen. After exit of the low power mode, the short-circuit detector will resume operation from the previous state. If the short-circuit detector should restart with defined state (counter

value = MCSDTO[TOUT], than the related detector shall be disabled and enabled again. This will reload the counter with the MCSDTO[TOUT] value and restart the short-circuit detector.

The maximum time span which the timer can cover depends on the clock frequency F of the main clock. The maximum delay D covered by the counter is D = MCSDTO[TOUT]* F. Due to sampling and synchronization of the feedback signal, the value of MCSDTO[TOUT] must always be larger than 2.

The two synchronizer stages imply also, that a a short-circuit with a duration of less than or equal to 2 clock cycles cannot be detected.

Two special cases shall be highlighted:

- Static short-circuit to ground and PWM signal = 1 see Figure 59-18. In this case, the enable of the short-circuit detector starts the sampling process and the interrupt bit is set MCSDTO[TOUT]+1 cycles after enabling the short-circuit detector
- Static short-circuit to VDD and PWM signal = 0 see Figure 59-19 : In this case. the enable of the short-circuit detector starts the sampling process and the interrupt bit is set MCSDTO[TOUT]+3 cycles after enabling the short-circuit detector due to the synchronizer which has been cleared during disable of the short-circuit detector

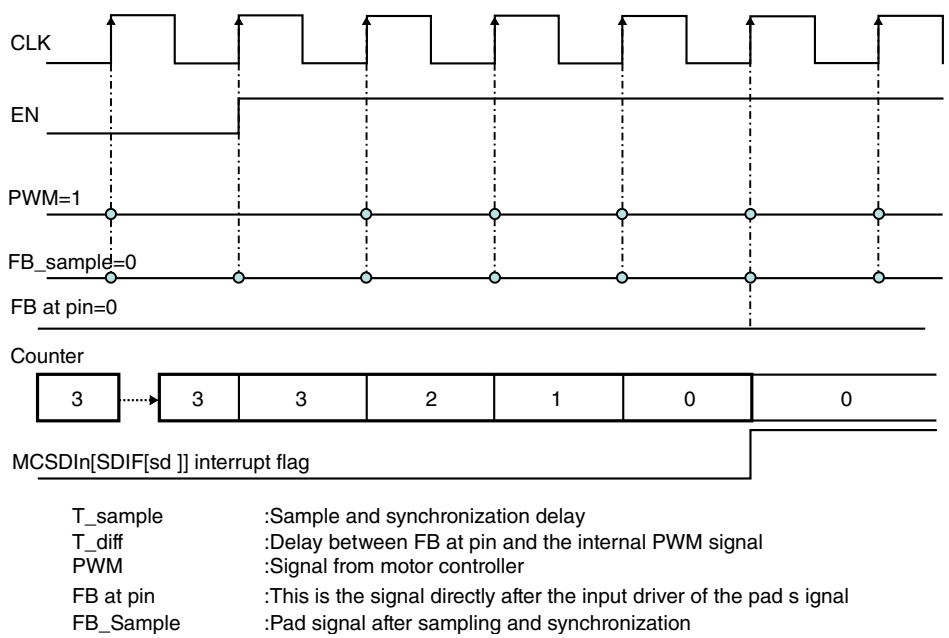
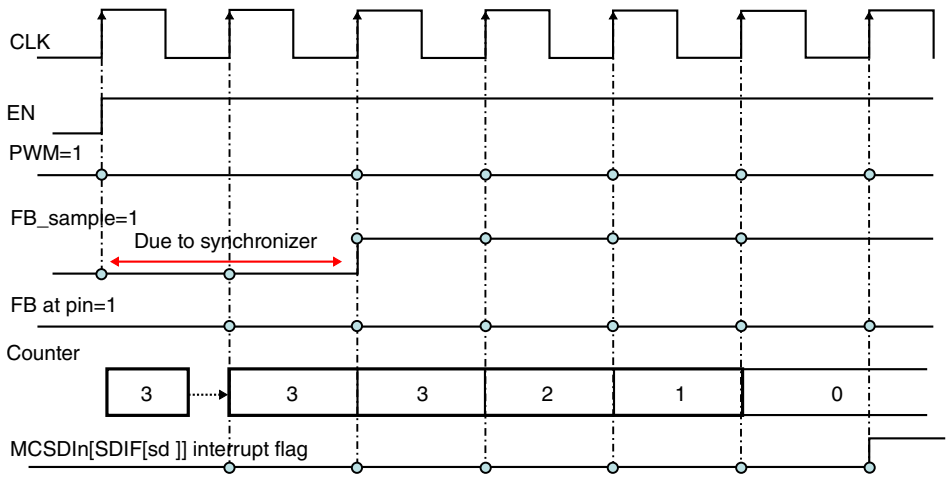


Figure 59-18. Static Short-circuit, PWM signal always at 1 and FB always at 0, MCSDTO[TOUT]=3



T_sample	:Sample and synchronization delay
T_diff	:Delay between FB at pin and the internal PWM signal
PWM	:Signal from motor controller
FB at pin	:This is the signal directly after the input driver of the pad s ignal
FB_Sample	:Pad signal after sampling and synchronization

Figure 59-19. Static Short-circuit, PWM signal always at 0 and FB always at 1, MCSDTO[TOUT]=3

Note

The short-circuit detection block does not disable a port in case of a short-circuit. It is task of the microcontroller to manage the event of a short-circuit.

59.6 Reset

The SMC is reset by system reset. All associated ports are released, all registers of the SMC module will switch to their reset state as defined in Memory Map and Register Definition.

59.7 Interrupts

The SMC has one interrupt output which is the bitwise OR function of 25 individual interrupt request sources:

- One time counter overflow interrupt: An interrupt will be requested when the MCCTL1[MCTOIE] bit in is set and the running PWM frame is finished. The interrupt is cleared by either setting the MCCTL1[MCTOIE] bit to 0 or to write a one to the MCCTL0[MCTOIF] bit
- 24 Interrupts for the short-circuit detection, one for each PWM pin: Whenever a short-circuit is detected on one PWM pin and the short-circuit detector enable bit MCSDEn[SDEN[*sd*]] is set, than the related interrupt flag MCSDIn[SDIF[*sd*]] is set according to the mapping shown inTable 59-6. The interrupt flag in MCSDIn[SDIF[*sd*]] will also rise an external interrupt if the interrupt enable bit MCSDIENn[SDIE[*sd*]] is set. To clear the interrupt flag, either write a one into the related bit position MCSDIn[SDIF[*sd*]] or disable the related short-circuit detector by writing zero to MCSDEn[SDEN[*sd*]]. If the short-circuit detector is enabled and a static short-circuit exists, then the MCSDIn[SDIF[*sd*]] flag will be asserted directly after clearing it, because the short-circuit detector is still enabled and will detect the short-circuit again. To avoid this behavior, disable the short-circuit detector channel after detection of the short-circuit.

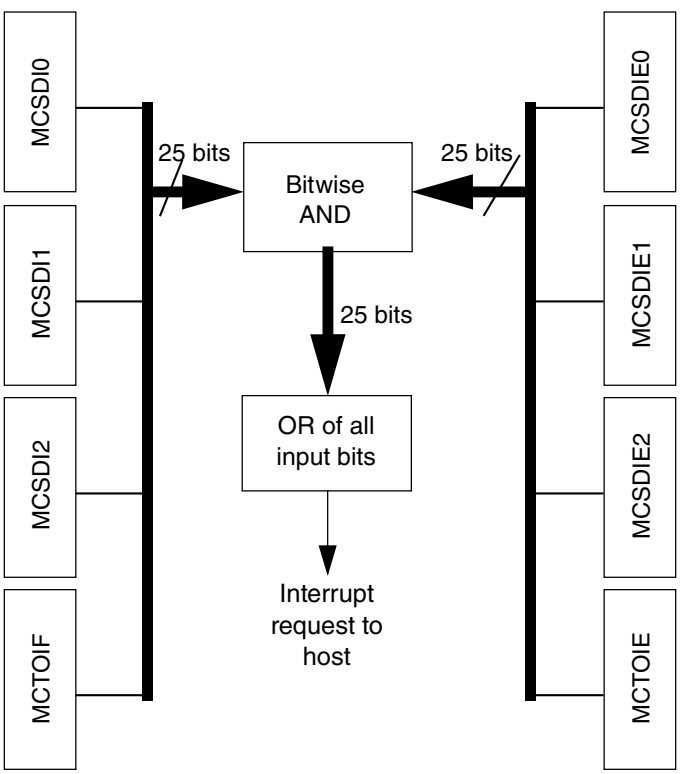


Figure 59-20. SMC Interrupt Generation