ECE483 Project: Low Dropout Regulator

Due Date: May 7, 2018 10am CST

Low dropout regulators (LDOs) are commonly used to generate supply voltages to sensitive analog circuits from a single voltage typically provided by a switching type DC-DC converter. Using voltage, V_{IN}, generated by the DC-DC converter, you are to design an LDO depicted in Fig. 1 that generates a *clean* output voltage, V_{OUT} and meets the specifications given in Table 1.

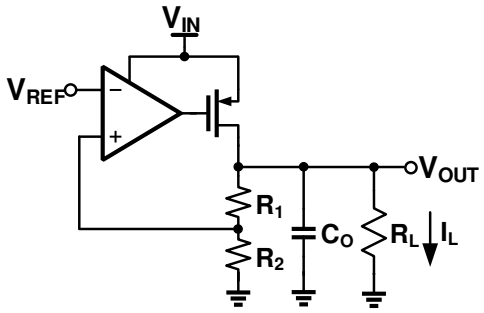

Figure 1: LDO schematic.

Table 1: LDO specifications

Technology	ECE483 0.18μm CMOS
Input voltage (V_{IN})	$1.8V \pm 10\%$
Output voltage (V_{OUT})	$1.0V - 1.3V$
Output voltage error	$\leq \pm 3\%$
Load current (I_L)	$1mA - 25mA$
Output capacitance (C_O)	$\leq 500pF$
DC load regulation	$\leq 20\mu V/mA$
DC line regulation	$\leq 2mV/V$
DC PSR	$\leq -40dB$
PSR at 1MHz	$\leq -20dB$
Transient response (1mA to 20mA step)	Undershoot $\leq 5\%$
Quiescent current	Minimum

Report Guidelines

The report should describe all the design choices you made with justification, present relevant simulation results and should **not exceed 5 pages**. The report should **strictly adhere** to the following outline:

(1) Overall design approach with emphasis on system level trade-offs and the design choices made to arrive at your amplifier architecture should be presented in the first page. You should explain your design decisions and compare the tradeoffs with alternative choices.

(2) Clearly drawn complete amplifier schematic (do not cut-and-paste Cadence schematic) along with tabulated device sizes, bias currents, g_ms, and Δs of all the devices should be shown in second page. Indicate transistors operating in triode region separately.

(3) The simulated performance summary of the LDO should also be provided in page 2 (see example performance summary table shown in next page).

(4) Clearly annotated simulated results as specified below should be presented in pages 3-5.

(page 3) (i) Loop-gain AC response (magnitude and phase) with clearly marked DC gain, loop-gain bandwidth, phase- and gain-margins for minimum and maximum load currents at $V_{OUT} = 1.3V$ and $V_{IN} = 1.8V$. (ii) Loop gain phase margin versus load current at $V_{OUT} = 1.3V$ and $V_{IN} = 1.8V$. (iii) DC loop gain versus load current at $V_{OUT} = 1.3V$ and $V_{IN} = 1.8V$. (iv) DC loop gain versus output voltage for $V_{IN} = 1.8V, 1.7V,$ and $1.6V$ at $I_L = 25mA$ and $I_L = 1mA$. (iv) Output voltage error, V_E, ($V_E[\%] = \frac{V_{OUT} - \beta V_{REF}}{V_{OUT}} \times 100$) versus output voltage for $V_{IN} = 1.8V, 1.7V,$ and $1.6V$ at $I_L = 25mA$ and $I_L = 1mA$. (v) Quiescent current verus load current at $V_{OUT} = 1.3V$ and $V_{IN} = 1.8V$.

(page 4) (i) Load regulation versus output voltage at $V_{IN} = 1.8V$. (ii) Load regulation versus input voltage at $V_{OUT} = 1.3V$. (iii) Line regulation versus load current at $V_{OUT} = 1.3V$. (iv) Line regulation versus output voltage at $I_L = 25mA$.

(page 5) (i) Load transient response at $V_{OUT} = 1.3V$ and $V_{IN} = 1.8V$. Please make sure to also shown zoomed-in plots to clearly indicate the claimed under-shoot and 1% settling time (ii) Power supply rejection (PSR) plots at minimum and maximum load currents for $V_{IN}/V_{OUT} = 1.8V/1.3V$ and $V_{IN}/V_{OUT} = 1.65V/1.4V$.

(6) Use LaTeX or MS WORD to type-set your report and name the report as lastname1_lastname2.pdf.

Table 2: Performance summary

Design parameter/variable	Simulated performance	Specification
Input voltage (V_{IN})		$1.6V - 2V$
Output voltage (V_{OUT})		$1.0V - 1.3V$
Total capacitance		$\leq 500pF$
Output voltage error		$\leq \pm 3\%$
Load current		$1mA - 25mA$
DC load regulation		$\leq 100\mu V/mA$
DC line regulation		$\leq 2mV/V$
Quiescent current ($I_L = 1mA/25mA$)		Minimum
Current efficiency ($I_L = 1mA/25mA$)		–
PSR: $V_{IN}/V_{OUT} = 1.8V/1.3V, I_L = 25mA$ (@1kHz/1MHz)		-40dB/-20dB
PSR: $V_{IN}/V_{OUT} = 1.65V/1.4VI_L = 25mA$ (@1kHz/1MHz)		-40dB/-20dB
Worst-case PSR		–
DC loop gain: $V_{IN}/V_{OUT} = 1.8V/1.3V$ ($I_L = 1mA/25mA$)		–
DC loop gain: $V_{IN}/V_{OUT} = 1.6V/1.4V$ ($I_L = 1mA/25mA$)		–
Worst-case DC loop gain		–
Loop-gain unity gain frequency ($I_L = 1mA/25mA$)		–
Loop-gain phase margin($I_L = 1mA/25mA$)		–
Loop-gain gain margin ($I_L = 1mA/25mA$)		–
Transient response (1mA to 25mA step)		Undershoot $\leq 5\%$
Transient response (25mA to 1mA step)		Overshoot $\leq 5\%$
Output noise ($I_L = 1mA/I_L = 25mA$)		–