EVK02004 User Manual

Document Information

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Revision History

Revision	Date	Change description
0.1		Initial version
1.0		Updated the connector types, added information about 'Main' tab in GUI and how to use it to setup Tx and Rx using scripts
1.1		Updated external SPI section with information about removing 0 Ohm resistors. Updated BF control section with commands for setting the FTDI pins as inputs
1.2		Based on API release version 1.38. Use of a single .msi installer instead of 3. New GUI layout. Updated typical EVK connections section

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Terminology

Term	Description
EVK	Evaluation Kit
MCX	Micro Coaxial Connector
SMP	Sub miniature push-on
SMA	Sub miniature version A
PA	Power amplifier
LO	Local Oscillator
AGC	Automatic Gain Control
GUI	Graphical User Interface
RFM	RF Module
HW	Hardware
SW	Software
BBK	Beambook
BB	Baseband

1 General

This document describes how to install and use the Sivers Semiconductors beamsteering 5G TRB02801 evaluation kit: EVK02004.

Note: Two evaluation kits are needed to evaluate a radio link. Please read the installation instructions before connecting the EVK to a computer.

2 List of items included in EVK package

- RF Module and motherboard attached to a mechanical support tower
- 5V, 8A power supply adaptor (AC input 100-250V)
- USB-A to micro-B USB cable
- Python SW package, USB driver, and GUI software for controlling the EVK (provided via SFTP)
- User manual (provided via SFTP)

3 Usage

This equipment may only be used with right permissions so that it does not interfere with licensed frequencies.

4 Introduction

4.1 Features

- Coverage of 24.25-29.5 GHz
- Support for dual polarised Tx and Rx data streams
- Zero IF or Low IF baseband signals
- Includes BFM02801 RF Module, Motherboard and Graphical User Interface (GUI)
- Beamsteering with integrated TX and RX patch array antennas
- TX and RX beambooks for beam settings
- Integrated synthesizer with support for up to 256 QAM modulation
- TX and RX LO frequency control
- Support for RX AGC
- Additional SPI, AGC, TX/RX switch connectors for control of the RFM from external controller.
- SMP baseband connectors, for easy connection to external equipment
- Python SW package

4.2 Benefits

- A solution for quick validation and proof of concept
- Plug and Play with a minimum of configuration needed
- Easy control through the USB interface and GUI
- User guideline included in the delivery
- Configuration support included

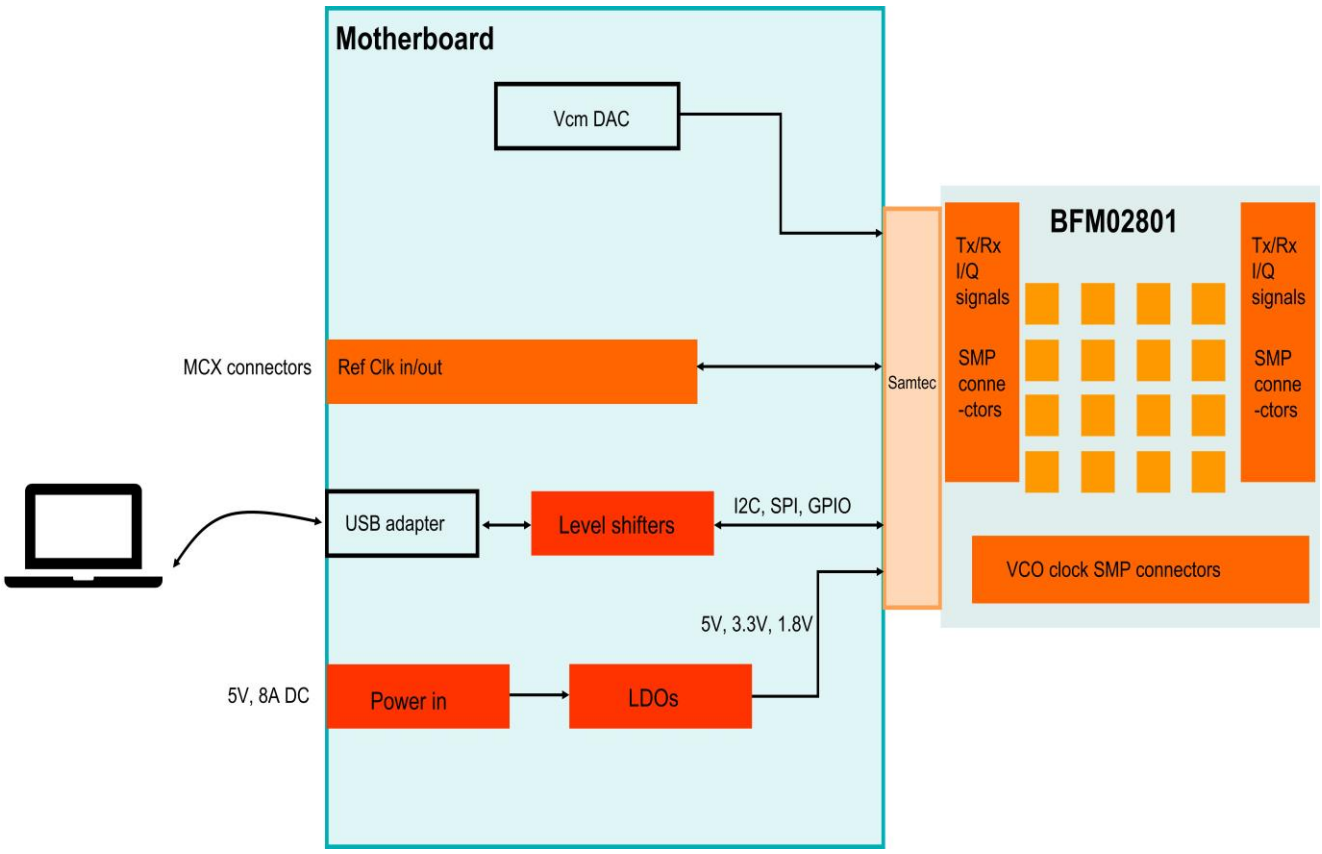
4.3 Overview

The evaluation Kit, EVK02004, is a plug and play platform, including all necessary HW and SW to quickly begin evaluating the latest Sivers Semiconductors 5G beam steering transceiver RFIC, the TRB 02801. The EVK is designed for ease of use and target system integrators and RF engineers validating the RF portion of a 5G link.

The EVK includes everything needed for seamless operation and will enable the user to quickly validate TRB02801's beam steering capabilities together with other system-defining RF parameters, which is critical when developing a new product with tough requirements on time-to-market.

The EVK includes support SW, RFM with integrated TX and RX antenna arrays, Motherboard, USB cable, and power adapter. The BFM02801's output power, gain, beam, DC offset and LO frequency can be controlled via a GUI and a USB interface on a test computer.

Figure 1: Block diagram of the EVK02004



4.4 Connector mappings

All the relevant connectors on the BF Module are marked with their names in Figure 2. The connectors are listed in Table 1.

Figure 2: Photo of the EVK showing the interface connectors

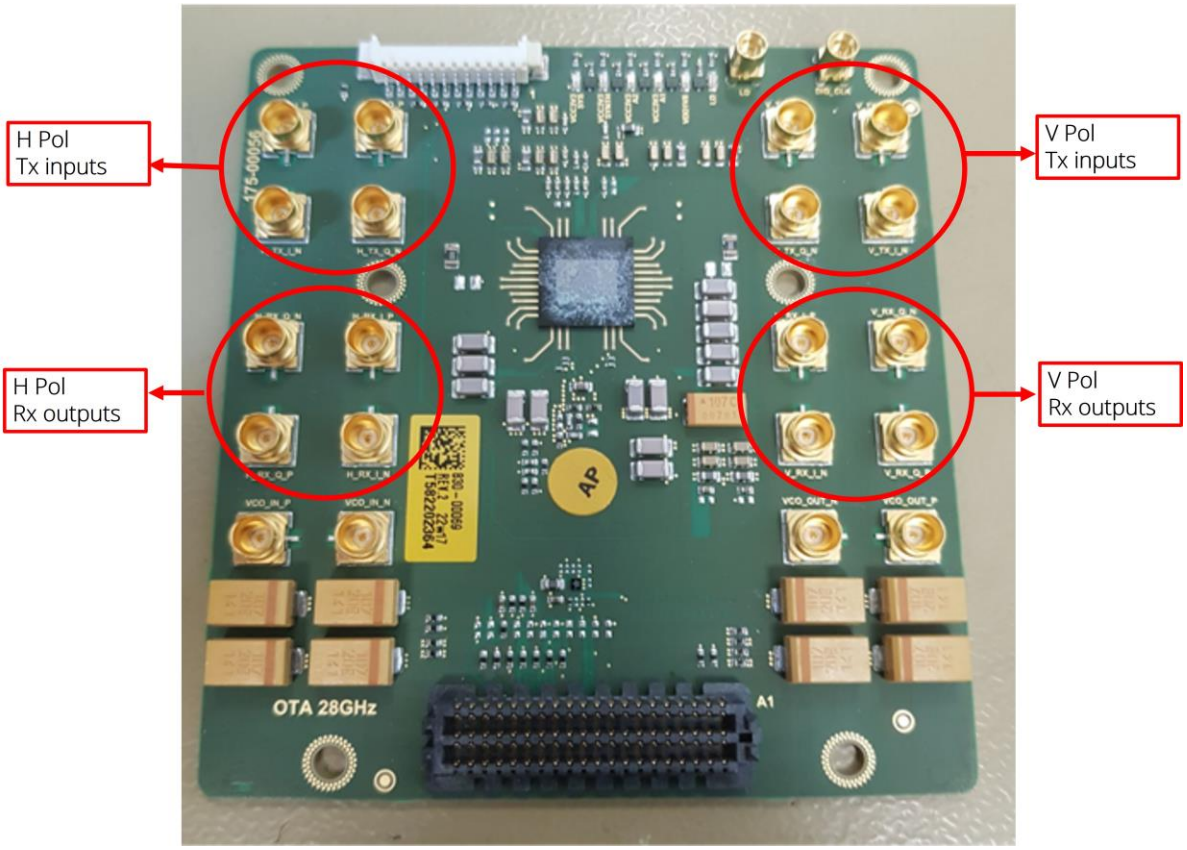


Table 1: BF Module Connectors

Signal name	Input/output	Type of connector	Description
H_TX_I_N	Input	SMP-m	TX baseband I – H Pol
H_TX_I_P	Input	SMP-m	TX baseband I + H Pol
H_TX_Q_N	Input	SMP-m	TX baseband Q - H Pol
H_TX_Q_P	Input	SMP-m	TX baseband Q + H Pol
H_RX_I_N	Output	SMP-m	RX baseband I - H Pol
H_RX_I_P	Output	SMP-m	RX baseband I + H Pol
H_RX_Q_N	Output	SMP-m	RX baseband Q - H Pol
H_RX_Q_P	Output	SMP-m	RX baseband Q + H Pol
V_TX_I_N	Input	SMP-m	TX baseband I – V Pol
V_TX_I_P	Input	SMP-m	TX baseband I + V Pol
V_TX_Q_N	Input	SMP-m	TX baseband Q - V Pol
V_TX_Q_P	Input	SMP-m	TX baseband Q + V Pol
V_RX_I_N	Output	SMP-m	RX baseband I - V Pol

Signal name	Input/output	Type of connector	Description
V_RX_I_P	Output	SMP-m	RX baseband I + V Pol
V_RX_Q_N	Output	SMP-m	RX baseband Q - V Pol
V_RX_Q_P	Output	SMP-m	RX baseband Q + V Pol
VCO_OUT_P	Output	SMP-m	VCO out +
VCO_OUT_N	Output	SMP-m	VCO out -
VCO_IN_P	Input	SMP-m	VCO in +
VCO_IN_N	Input	SMP-m	VCO in -

All the relevant connectors on the motherboard are marked with their names in Figure 3. The connectors are listed in Table 2.

Figure 3: EVK Clock ports

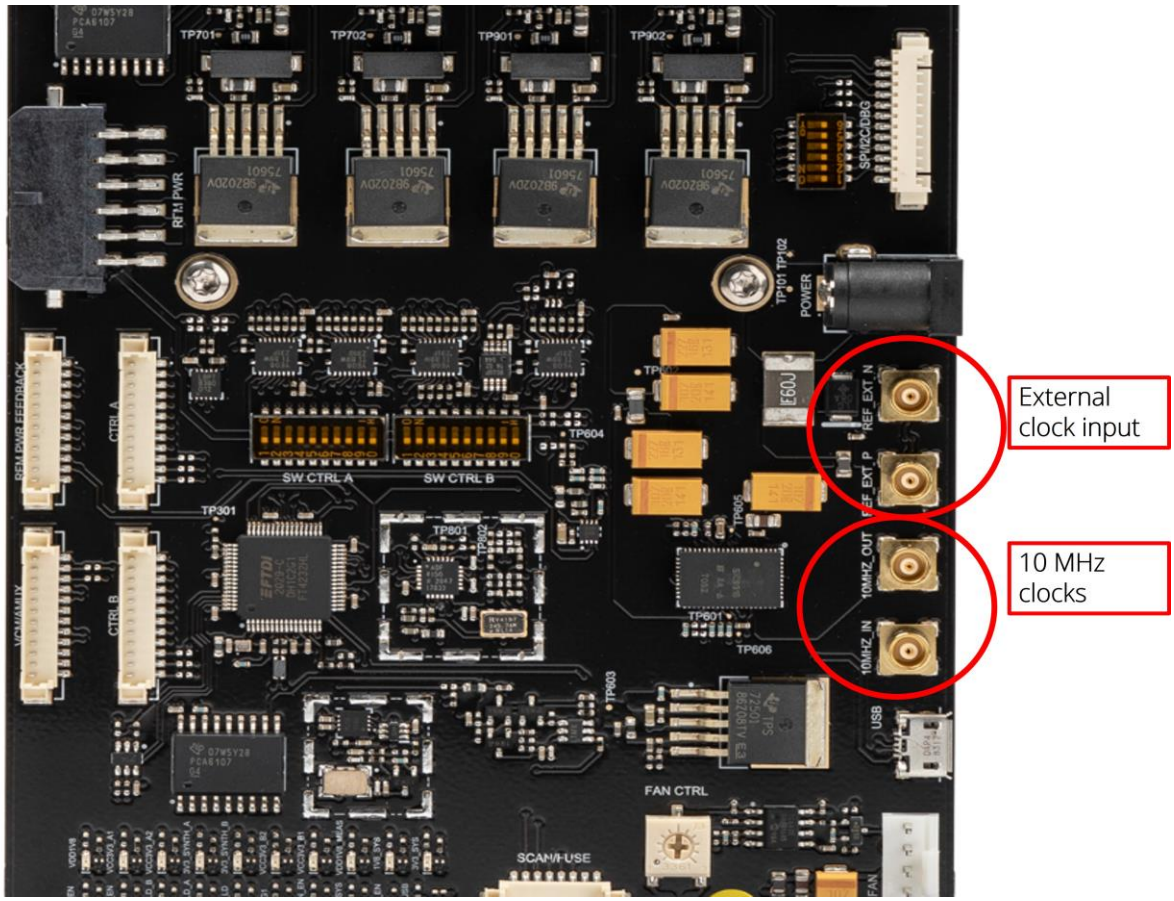


Table 2: EVK connectors

Signal name	Input/output	Type of connector	Description
10MHZ_IN	Input	MCX-f	Single ended 10 MHz clock
10MHZ_OUT	Output	MCX-f	Single ended 10 MHz clock

Signal name	Input/output	Type of connector	Description
REF_EXT_P	Input/Output	MCX-f	245.76 MHz Reference clock +
REF_EXT_N	Input/Output	MCX-f	245.76 MHz Reference clock -

5 Getting started

5.1 System requirements

- A computer with USB interface and Windows10 or later, 64-bit.
- On Windows platform Python 3.8 (64-bit) or Python 3.9 (64-bit) should be installed.

5.2 Installation instructions for Windows

1. Download software package from sftp. Instructions for downloading will be provided.
2. A .msi package needs to be installed. The package, 'install_Sivers_Rapinoe_API.msi', creates a folder in the C drive ('C:\Sivers Semiconductors) and copies all the main APIs to control the RFIC and scripts to install additional python packages.
3. After the installer is finished a text file pops up and lists the things that have been done in the previous step. You can find this file, 'readme.txt', at 'C:\Sivers Semiconductors\Rapinoe\API_install'
4. To complete the installation of this package an additional step is required. The simplest way is to double click 'install.cmd' present at 'API_install' folder at the location given above. It will install all the relevant python packages for the APIs. The packages are installed for all the python versions (3.8 and 3.9) found on the PC. Instead, if a particular python version is preferred, go to the corresponding folder (PY38 or PY39) and run the .cmd file in that folder.
5. At this point it is possible to run the EVK SW environment either from a command line in a terminal window or from the GUI. In either case, first open a terminal window from 'C:\Sivers Semiconductors\Rapinoe\API'.
6. Type the following in the command window to start the EVK SW environment to work from the command line:

   ```
   > python -i evk.py
   ```

   A list of available EVK devices connected to the PC is shown. See below.

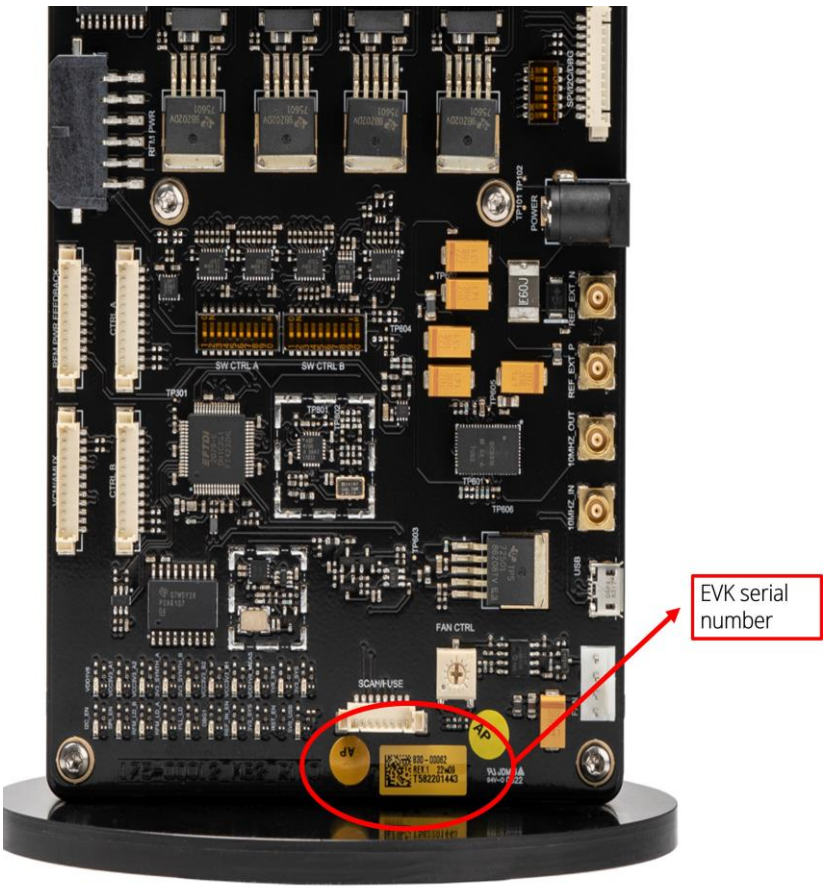
   ```
   > C:\Sivers Semiconductors\Rapinoe\API>python -i evk.py
    Trying to import module MB
     MB 0.1.11 import successful.
    Available motherboards:
     T582201436
   ```

   Type one of the listed seral numbers (in this example case: T582201436) and press enter or if there is just one EVK connected press enter.

```
Enter EVK serial number from above list [T582201436]:
Connecting to motherboard MB2 with serial number T582201436 ...
  MB_DLL    : 0.1.11
  API       : 0.1.38
Expecting 1 device. Trying to connect to it ...
  Device with id 0x12522112 detected.
>>>
```

The EVK environment is now ready to be used. The EVK serial numbers can be found on the motherboard as shown in Figure 4.

Figure 4: EVK serial number

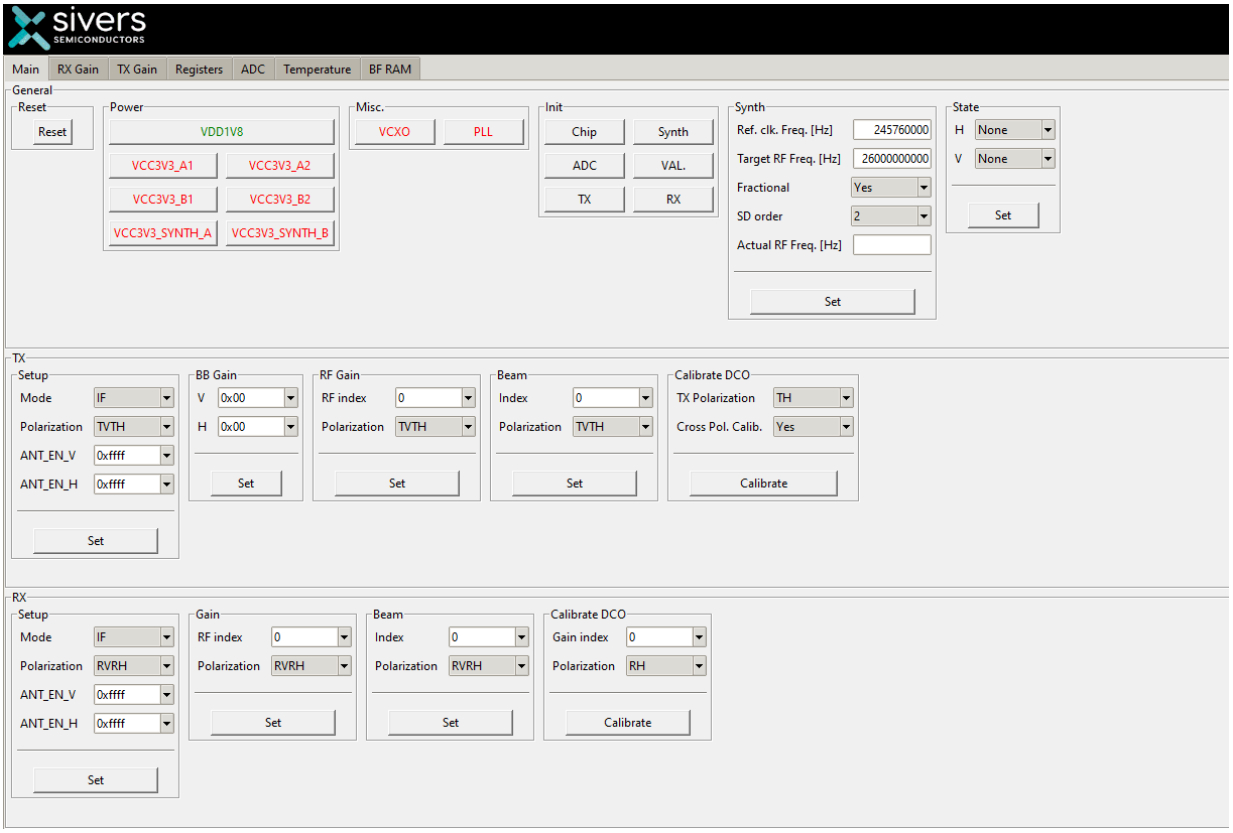


7. Type the following in the command window to start the EVK SW environment for working from the GUI:

```
> python -i evk.py -g
```

The procedure is same as with “python -i evk.py”. A list of available EVK devices connected to the PC is shown. Type one of the listed seral numbers (in this example case: T582201436) and press enter or if there is just one EVK connected, press enter. After connecting to the EVK a GUI will open as shown in Figure 5 .

Figure 5: EVK GUI



6 Using the GUI

6.1 GUI layout overview

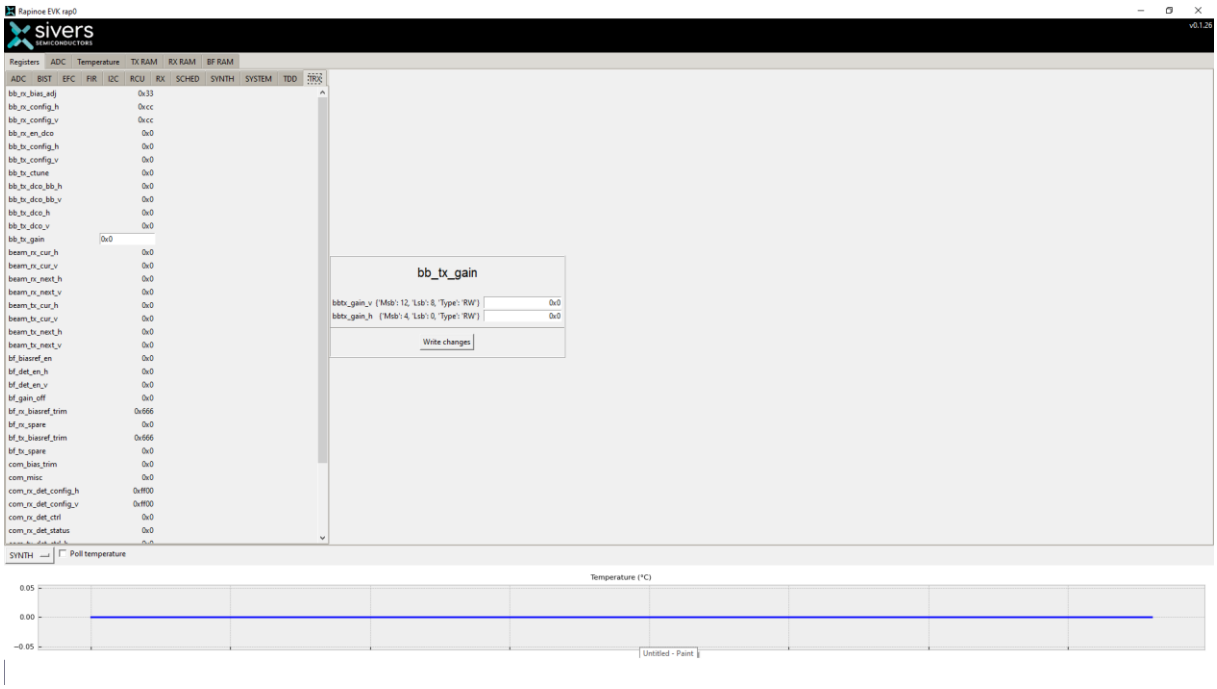
The GUI can be used to program the registers of the RFIC, read various analog values using ADC, read the temperature at different locations in the RFIC, and program the phase shifter and VGA values for up to 256 beams. The GUI has 7 top level tabs as shown in Figure 5. More details about them are given below.

6.1.1 Registers

The 'Registers' tab gives access to all the registers of the RFIC. It is subdivided into 12 tabs as seen in Figure 6. By clicking on any register name more information can be obtained about the fields of the register, bit-length of individual fields and whether the register is read/write or read only. The register values can be modified by writing directly into the box next to the register name (in hex or decimal) and pressing 'Enter' or by writing into individual fields and clicking on 'Write Changes'.

More information about the register contents is given in the register mapwhich can be found at 'C:\Sivers Semiconductors\Rapinoe\API\doc'. The different sheets in the register map file corresponds to the subdivisions in the Registers tab.

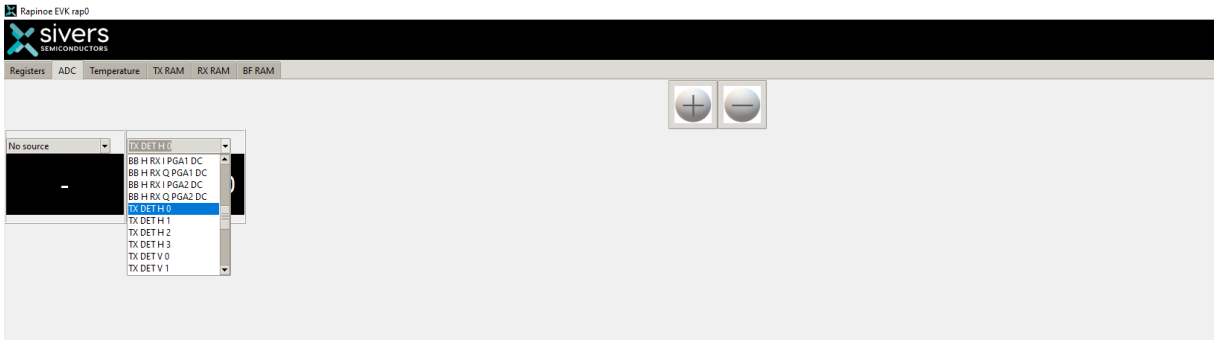
Figure 6: GUI Registers Tab



6.1.2 ADC

The 'ADC' tab gives the option to monitor multiple sources by clicking on the '+' button. The drop-down menu in each window gives the list of sources that can be accessed as shown in Figure 7.

Figure 7: GUI ADC Tab



6.1.3 Temperature

In this tab, the temperature values at different locations in the RFIC can be monitored as shown in Figure 8. Up to 8 sources are available as seen in the top row. The GUI always has one temperature window at the bottom irrespective of the active tab. By default, it is reading synthesiser's temperature. This can be changed using the drop-down menu in the window.

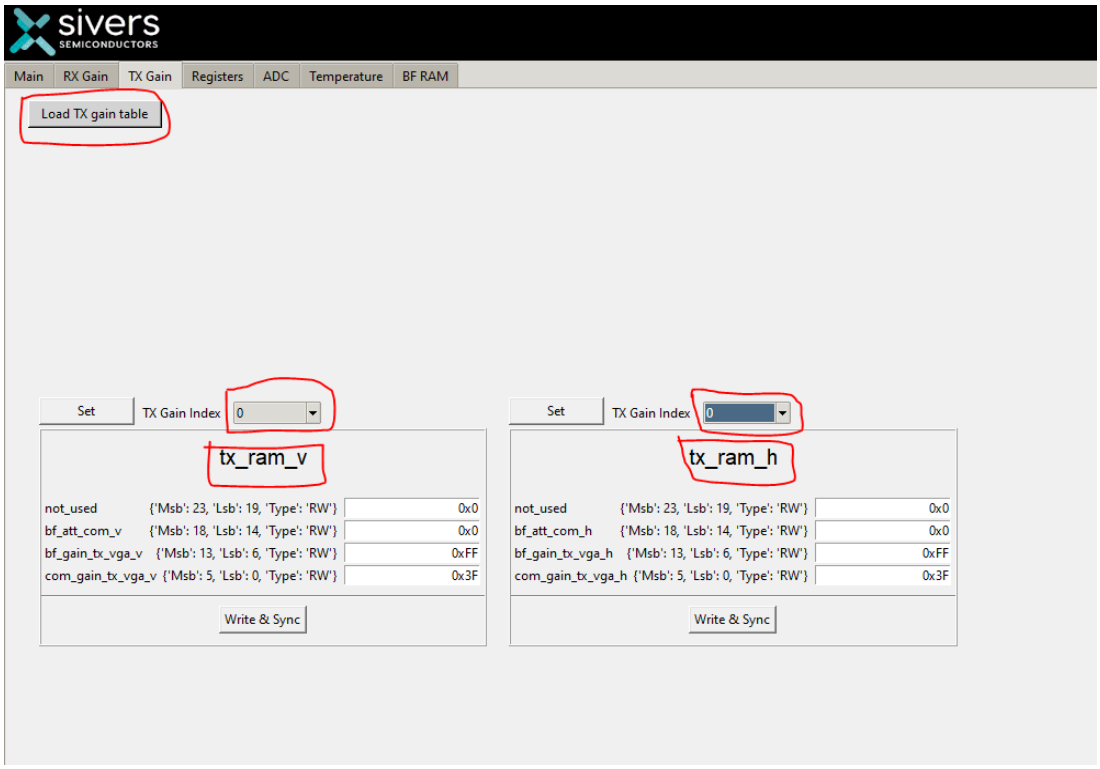
Figure 8: GUI Temperature tab

6.1.4 Tx Gain

The 'TX gain' tab gives the option to work with 64 (index 0 to 63) profiles per polarisation, which are stored in the Tx RAM on the RFIC. As shown in Figure 9 a single index is shown for both vertical and horizontal polarisations along with the different gain fields (Table 3). A different index can be chosen by the drop-down menu and clicking on 'Set'. changes can be made to the gain values by typing in new values and clicking on 'Write & Sync'

(this button turns red when changes are made and turns green after being clicked on). A new gain table can be loaded also.

Figure 9: GUI TX gain tab



More information about the tx_ram register can be found in the register map and TRB02801 user manual.

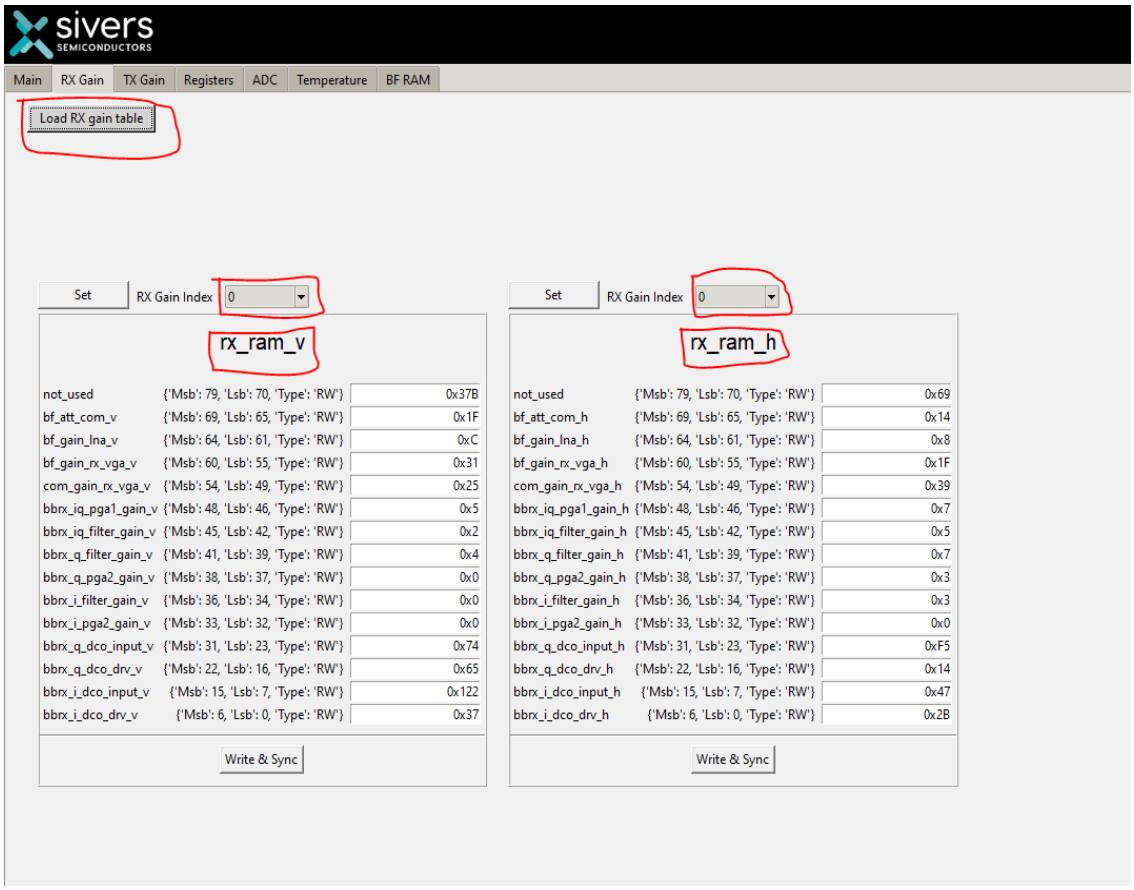
Table 3: tx_ram register fields

Register	Field name	Bit length	Comments
tx_ram_h/v	com_gain_tx_vga	6	TX Common VGA gain for H/V-pol. 0x3F: Max
	bf_gain_tx_vga	8	TX BF VGA gain for H/V-pol. 0xFF: Max
	bf_att_com	5	TX BF Attenuation for H/V-pol. 0x00: 0 dB 0x01: 0.5 dB … 0x1F: 15.5 dB
	not_used	1	Supply voltage select to get correct 1.6 V internal common mode voltage for H or V-pol: 0: 2.7 V 1: 3.3 V

6.1.5 Rx Gain

The 'RX gain' tab gives the option to work with 64 (index 0 to 63) profiles per polarisation, which are stored in the Rx RAM on the RFIC. As shown in Figure 10. A single index is shown for both vertical and horizontal polarisations along with the different gain fields (Table 4). A different index can be chosen by the drop-down menu and clicking on 'Set'. changes can be made to the gain values by typing in new values and clicking on 'Write & Sync' (this button turns red when changes are made and turns green after being clicked on). A new gain table can be loaded also. The DC offset fields are automatically written into after the DC offset calibration routine is done.

Figure 10: GUI RX Gain tab



More information about the rx_ram register can be found in the register map and TRB02801 user manual.

Table 4: rx_ram register fields

Register	Field name	Bit length	Comments
rx_ram_h/v	bbrx_i_dco_drv	7	DCO compensation at BB output driver stage I (H/V-pol)
	bbrx_i_dco_input	9	DCO compensation at BB input stage I (H/V-pol)
	bbrx_q_dco_drv	7	DCO compensation at BB output driver stage I (H/V-pol)
	bbrx_q_dco_input	9	DCO compensation at BB input stage I (H/V-pol)

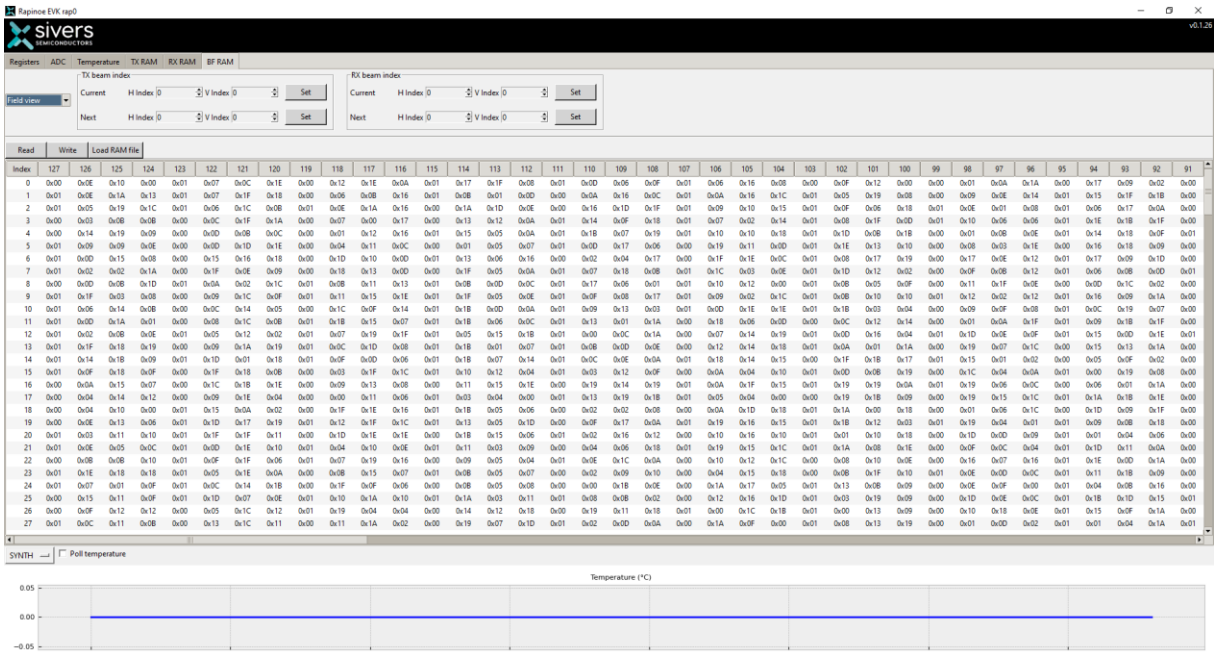
	bbrx_i_pga2_gain	2	**BB mode**: Output gain stage for I (H/V-pol) 00: Max ... 11: Max - 6 dB
	bbrx_i_filter_gain	3	BB Bi-quad 2nd stage gain for I (H/V-pol) 000: Max ... 111: Max - 5 dB
	bbrx_q_pga2_gain	2	**IF mode**: Input gain stage for I and Q (H/V-pol) 00, 01: Max 10, 11: Max - 8 dB **BB mode**: Output gain stage for Q (H/V-pol) 00: Max ... 11: Max - 6 dB
	bbrx_q_filter_gain	3	BB Bi-quad 2nd stage gain for Q (V-pol) 000: Max ... 111: Max - 5 dB
	bbrx_iq_filter_gain	4	**IF mode**: Output gain stage for I and Q (H/V-pol) 0x0: Max ... 0xF: Max - 10 dB **BB mode**: Bi-quad 1st gain stage for I and Q (H/V-pol) 0x0: Max ... 0xF: Max - 5 dB
	bbrx_iq_pga1_gain	3	BB Input stage gain for I and Q (V-pol) 000: Max ... 111: Max - 15 dB
	com_gain_rx_vga	6	RX Common VGA gain for H/V-pol 0x3F: Max
	bf_gain_rx_vga	6	RX BF VGA gain for H/V-pol 0x3F: Max

			0x3E: Max - 0.25 dB ... 0x00: Max - 15 dB
	bf_gain_lna	4	RX BF LNA gain for H/V-pol. Note that not all 4-bit values are allowed 4'b0011: Min gain (No signal) 4'b1001: Max - 6 dB 4'b0110: Max - 6 dB 4'b1100: Max gain
	bf_att_com	5	RX BF Attenuation for H/V-pol. 0x00: 0 dB 0x01: 0.5 dB ... 0x1F: 15.5 dB
	not_used		

6.1.6 BF RAM

The 'BF RAM' tab gives the option to work with 256 (index 0 to 255) beams for the 128 fields of the ram register as shown in Figure 11.

Figure 11: GUI BF RAM tab



The default view is the 'Field view' which shows the 128 fields (column numbers 0 to 128). There are 32 paths in the RFIC (16 paths per polarisation). Each path has 4 fields listed in Table 5. Each beam index has 32*4 = 128

fields. Column numbers 0 to 63 correspond to the 16 paths for horizontal polarisation and column numbers 64 to 127 correspond to the 16 paths for vertical polarisation. When the cursor hovers over a particular value in the columns, the corresponding field name is also shown in a pop-up box along with the number of bits assigned for that field. There are options to view the ram's register value as a whole by choosing 'compact view' from the drop-down menu or the value can also be viewed as a list of bytes using 'byte view'

Table 5: ram register fields per path

Column number	Field name
0	bf_vpa_i
1	bf_vpa_q
2	bf_vpa_att
3	bf_enable

The beam index can point to a Tx beam or an Rx beam. The required indices for Tx and Rx can be selected using the 'TX beam index' and 'RX beam index' blocks. The beams for vertical and horizontal polarisation can be set separately. The 'Set' button turns yellow when you make changes to indicate that the changes have not yet been set. After clicking on 'Set' the colour goes away. All the values in the table can be loaded via a .xml file using the 'Load RAM file' button

The whole BF RAM can be read into the table in the GUI by clicking on 'Read' button.

The BF RAM can be written into by modifying the required fields (by double clicking on required field) and clicking on 'Write' button. When changes are made the corresponding rows and the 'Write' button turns yellow. After clicking on 'Write' the colour goes away.

There are two options to set the beam indices: 'Current' and 'Next'. When the 'Current' option is used the horizontally and vertically polarised beams are set sequentially. That is, they are not synchronised. If both the beams need to be set at the same time, 'Next' option needs to be used. First, the required indices should be 'Set' using the 'Next' option. Then, the same indices should be 'Set' in the 'Current' fields.

7 Setting up the EVK

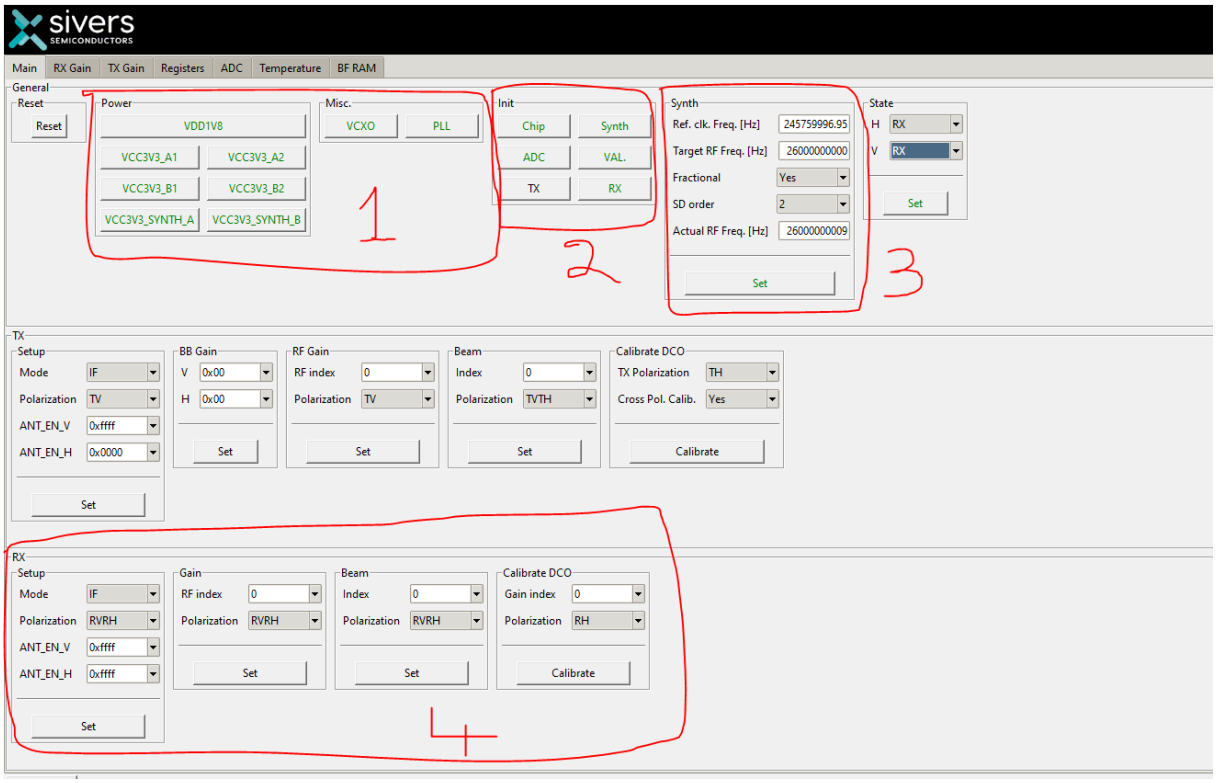
There are many ways to setup the EVK in Rx or Tx mode. They are described below.

7.1 Start the EVK as a RX unit

The EVK can be set in the RX mode by using the GUI or using a test script or writing commands directly in the python prompt.

1. Using the GUI: In the 'Main' tab (see Figure 12) switch on all the power domains (step 1). Different LEDs on the EVK's motherboard will switch on to indicate that the power domains are active. Click in order 'Chip, Synth, ADC, VAL., RX' (step 2). The button text will turn green indicating that the step has been executed. Then set the frequency (step 3). In the 'Rx' section of the 'Main' tab choose and setup the right polarisation (step 4). The gain and beam index should also be set. Note that this is the gain index. The corresponding gain values can be changed in the Rx Gain tab (Section 6.1.5). Even if the gain index and the beam index which are shown in the 'RX' section are the desired ones a 'Set' action should still be performed. Then set the 'State'. Then do 'Calibrate' for the required polarisation. DCO calibration minimises the DC offset appearing at the Rx baseband outputs.. Note that whenever a change is made the 'Set' text in the button turns red. After you click 'Set' the text turns green indicating that the set action has been executed.

Figure 12: GUI Main tab RX



2. Test script method: The scripts are in API/tests folder. Running 'python -i evk.py -t rx_setup' will start the EVK in RX mode. Note that the GUI can also be opened after running the script also (by using the command 'host.open_gui(rap0)' in the command prompt. The GUI will not reflect all the settings done by the script (the settings will remain unaffected when the GUI pops up). Additional changes can be then done via the GUI.

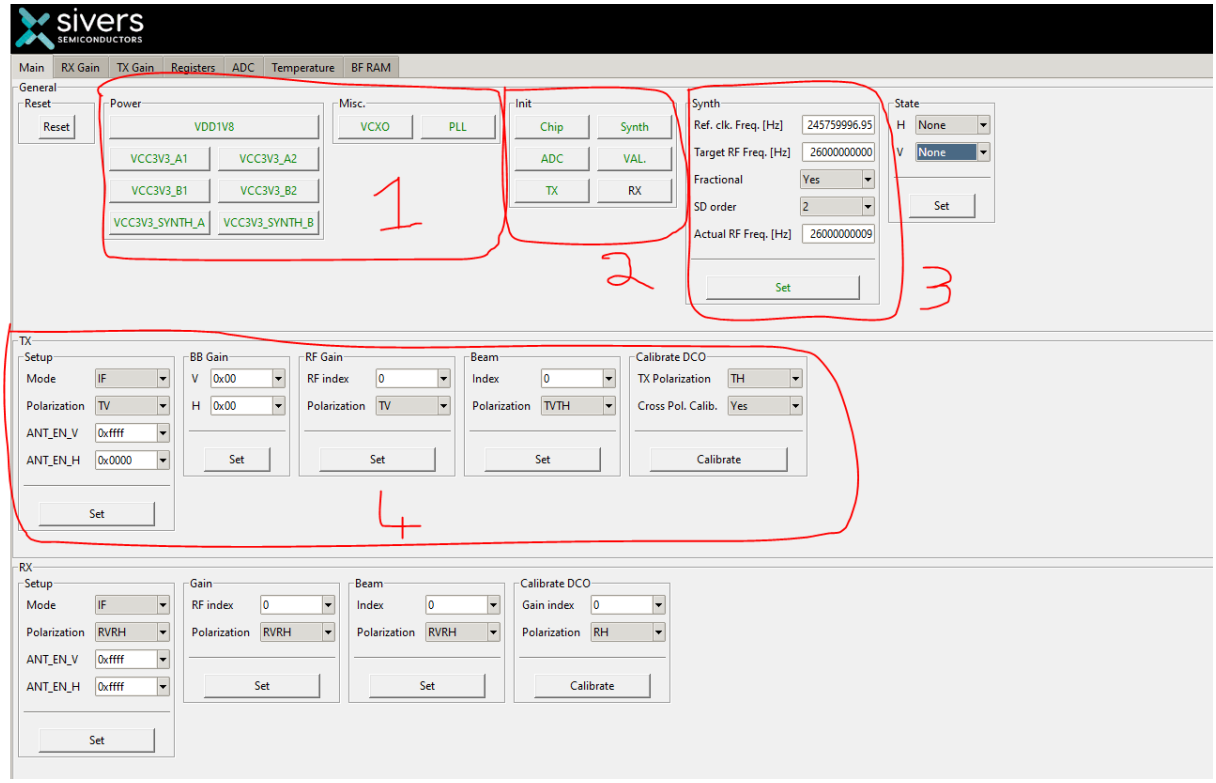
3. The commands in the rx_setup.py script can also be copy pasted onto the python prompt if the prompt was invoked without a test script (using only 'python -i evk.py).

7.2 Start the EVK as a TX unit

The EVK can be set in the TX mode by using the GUI or using a test script or writing commands directly in the python prompt.

1. Using the GUI: In the 'Main' tab (see Figure 13) switch on all the power domains (step 1). Different LEDs on the EVK's motherboard will switch on to indicate that the power domains are active. Click in order 'Chip, Synth, ADC, VAL., TX'(step 2). The button text will turn green indicating that the step has been executed. Then set the frequency (step 3). In the 'Tx' section of the 'Main' tab choose and setup the right polarisation (step 4). The BB gain, RF gain, and beam index should also be set. Note that this is the gain index. The corresponding gain values can be changed in the Tx Gain tab (Section 6.1.4) Even if the BB gain values, RF gain index, and the beam index which are shown in the 'TX' section are the desired ones a 'Set' action should still be performed. Then set the 'State'. Then do 'Calibrate'. DCO calibration minimises the LO leakage. Note that whenever a change is made the 'Set' text in the button turns red. After you click 'Set' the text turns green indicating that the set action has been executed.

Figure 13: GUI Main Tab TX

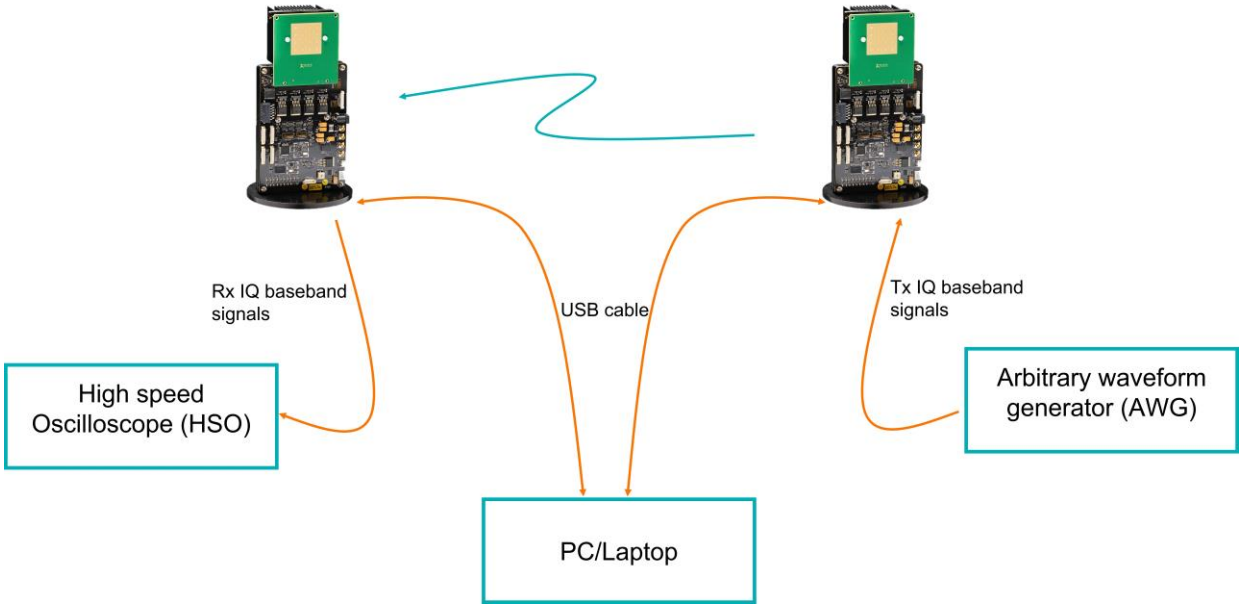


2. Test script method: The scripts are in API/tests folder. Running 'python -i evk.py -t tx_setup' will start the EVK in TX mode. Note that the GUI can also be opened after running the script also (by using the command 'host.open_gui(rap0)' in the command prompt. The GUI will not reflect all the settings done by the script (the settings will remain unaffected when the GUI pops up). Additional changes can be then done via the GUI.
3. The commands in the tx_setup.py script can also be copy pasted onto the python prompt if the prompt was invoked without a test script (using only 'python -i evk.py)

8 Recommended connection to RF instruments

A complete RF link can be set up using 2 EVK02004s, a control computer, an AWG as I/Q signal generator and a HSO/VSA as I/Q signal analyzer (see Figure 14 below). The computer can control the two EVKs from command line or GUI by using their serial numbers.

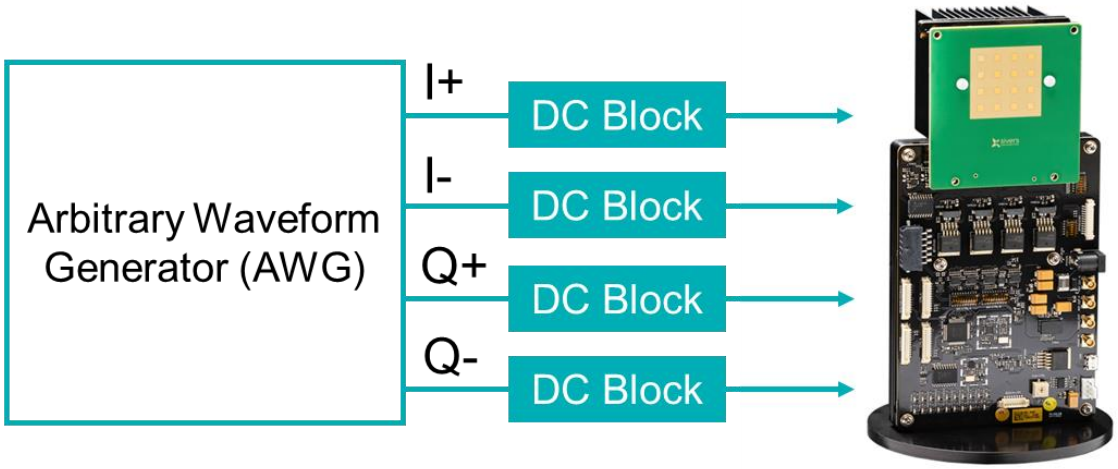
Figure 14: EVK02004 RF Link set-up



For best performance in an RF instrumentation set-up the following recommendation apply:

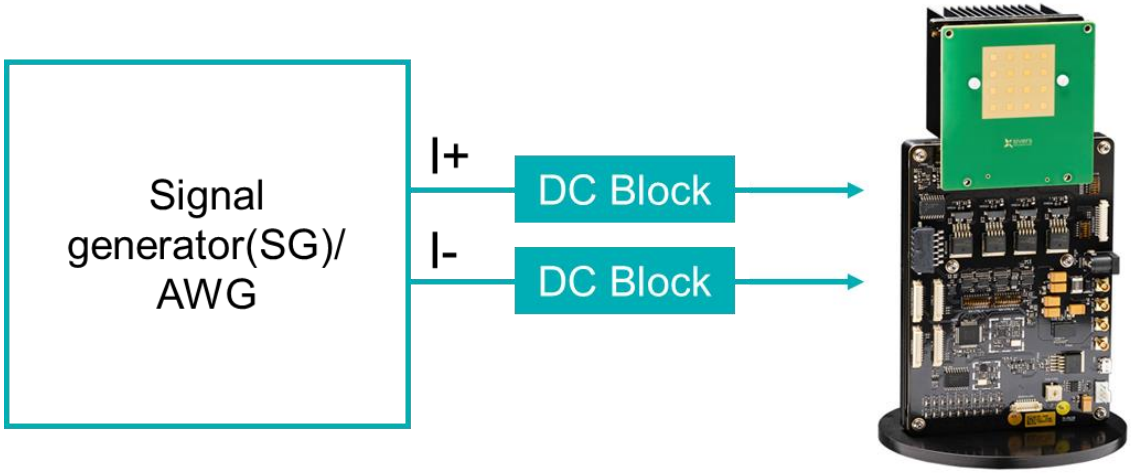
- Connections to TX I/Q ports should be AC-coupled (see Figure 15 and Figure 16). The DC block is to prevent unintentional loading of the ports. Input power for optimum performance is in the range of -15 to -18 dBm.

Figure 15: Connection to Tx ports of the EVK BB mode



For dual pol a second set of I and Q signals i.e., 4 more connections are needed.

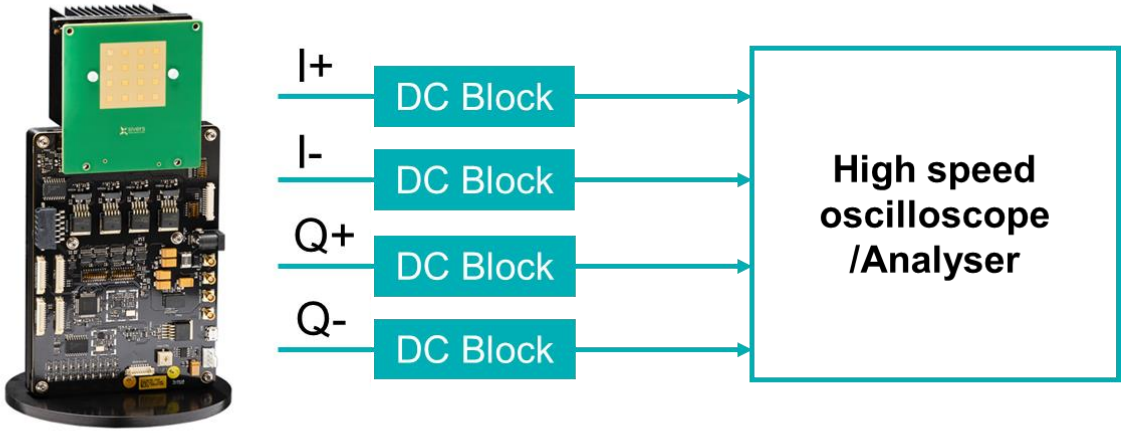
Figure 16: Connection to Tx ports of the EVK IF mode



Either the I+/I- pair or Q+/Q- pair can be used for the Low-IF signal. Using I+/I- pair is recommended. The input signal's frequency range is between 3.5 – 5 GHz. For dual pol a second set of I signals i.e., 2 more connections are needed.

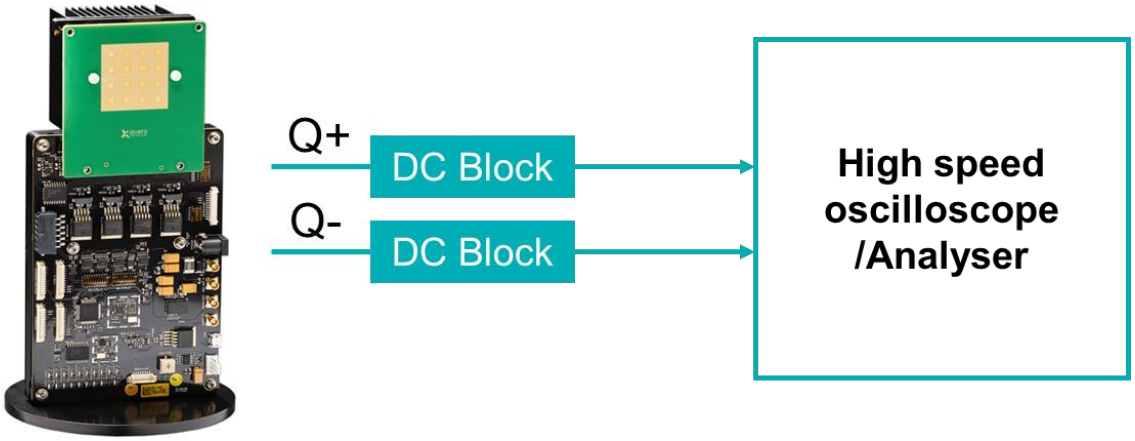
- Connections to RX I/Q ports should be AC-coupled (see Figure 17 and Figure 18). Note that a common mode voltage of 600 mV is generated by the MB2 itself for the I+/I- and Q+/Q- differential lines. TRB02801 design is based on 100Ω differential and a high common mode load impedance and should normally be DC coupled to the modem side, however when you connect it to an oscilloscope you need DC blockers. This is because the scope has dual 50Ω to ground ports.

Figure 17: Connection to Rx ports of the EVK BB mode



For dual pol a second set of I and Q signals i.e., 4 more connections are needed.

Figure 18: Connection to Rx ports of the EVK IF mode

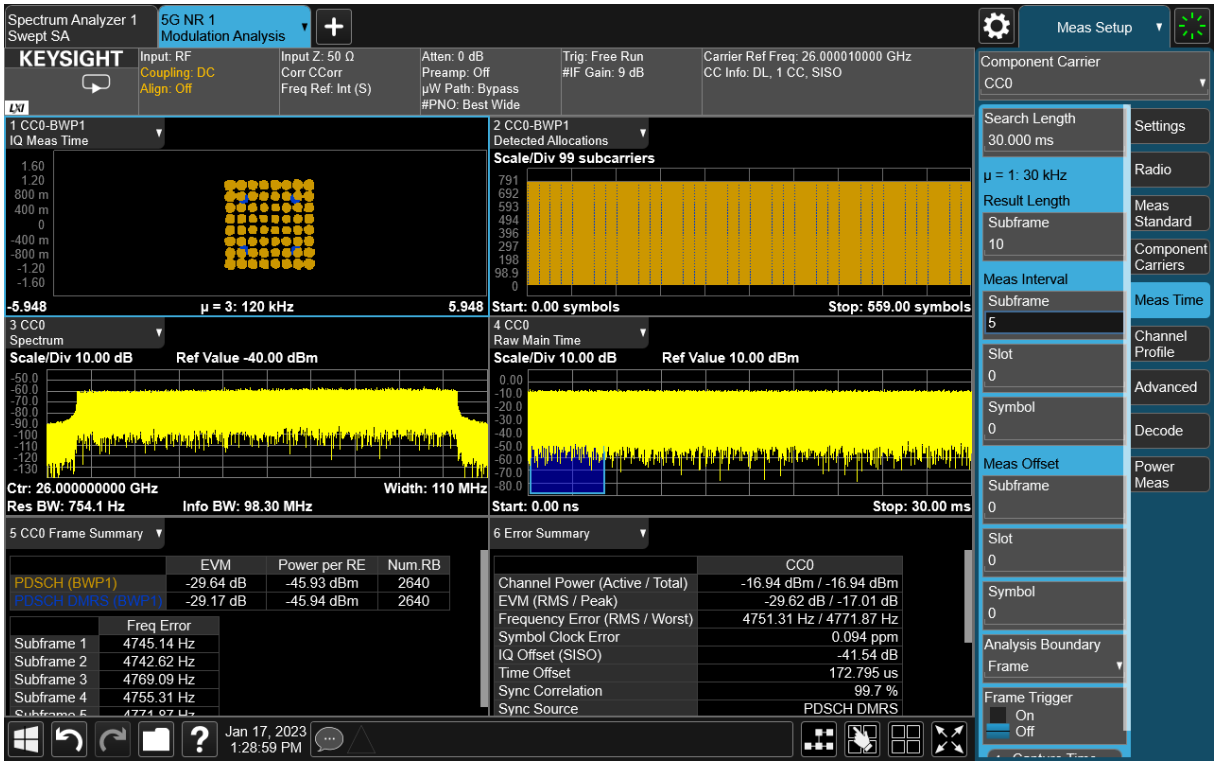


For low IF mode only the Q+/Q- lines are active. For dual pol a second set of Q signals i.e., 2 more connections are needed.

9 Typical Performance Characteristics

For the RF Link set-up described above, a typical performance would look like below Figure 19. In a lab setup the distance between EVKs is around 1m or less. The default EIRP (max gain values in Tx EVK) is quite high, and it will saturate the Rx EVK. It is important to reduce the BF and Common gain in the TX EVK. Also, the LNA, BF, and common gain in Rx EVK must be set appropriately to achieve good performance. The 'Tx Gain' and 'Rx gain' tabs can be used to do this in the GUI. The Tx and Rx scripts also contain the commands to change the gain (commented in the files).

Figure 19 EVK02004 RF Link Performance



10 Appendix

10.1 Using EVK with external control signals

10.1.1 PLL reference clock configurations

The default PLL ref clock configuration for EVK is an internal 245.76MHz, (differential) LVDS-levels ref clock to the RF module. An External single-ended or differential clock can also be used.

10.1.1.1 External single ended clock

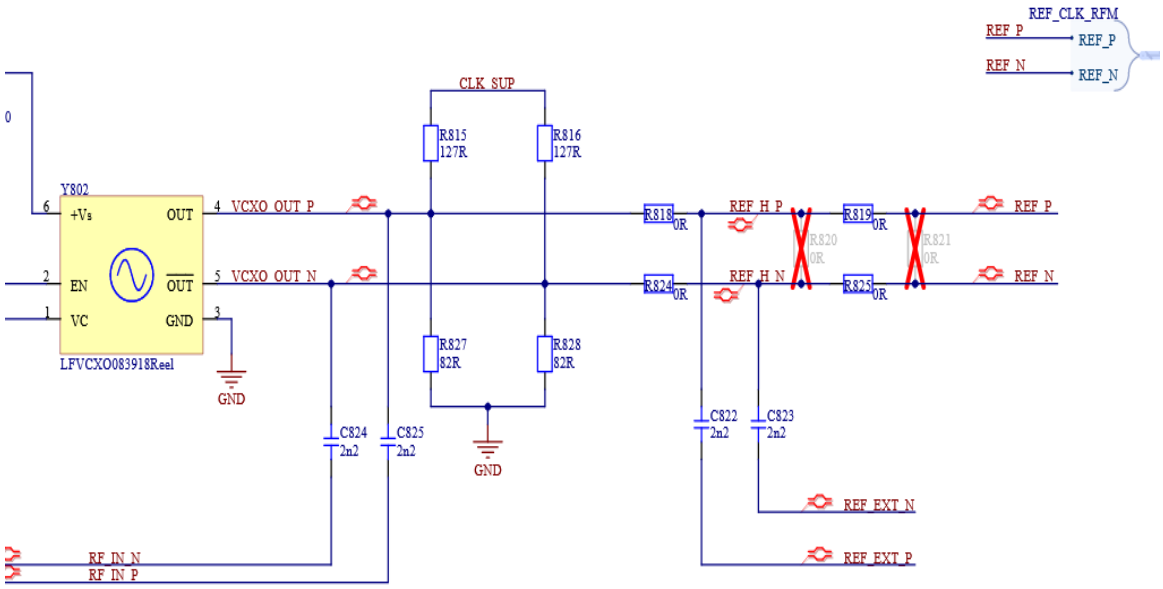
An external 10 MHz single ended clock can be used to derive the 245.76 MHz clock. No modifications are needed on the mother board. There is a detector circuit on the board and if a 10 MHz signal is present it will automatically be chosen.

10.1.1.2 External (differential) PLL ref clock configuration

Modifications on MB2:

- By default, the connection is AC-coupled. REF_EXT_P/N, can be used both as reference clock input and as reference clock output. When used as inputs, R818 and R824 should be removed

Figure 20: Layout view of the external PLL ref clock.



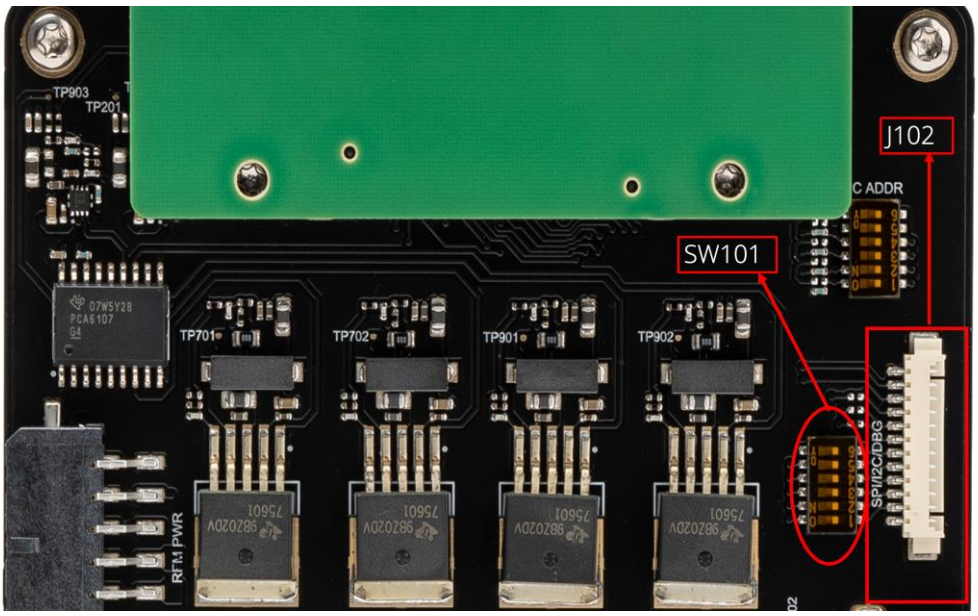
10.2 External SPI control

This chapter describes how to control the EVK with the external SPI signals.

10.2.1 HW setup

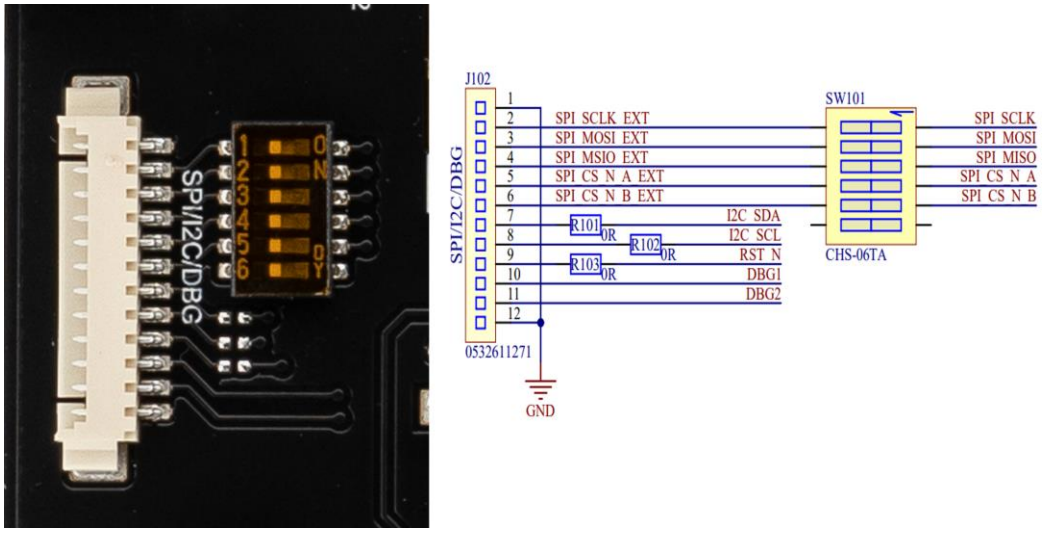
The external SPI host is connected via J102 on the EVK's motherboard, MB2, shown in Figure 21.

Figure 21: "J102" used for external SPI connections, along with the SPI input selector switch "SW101"



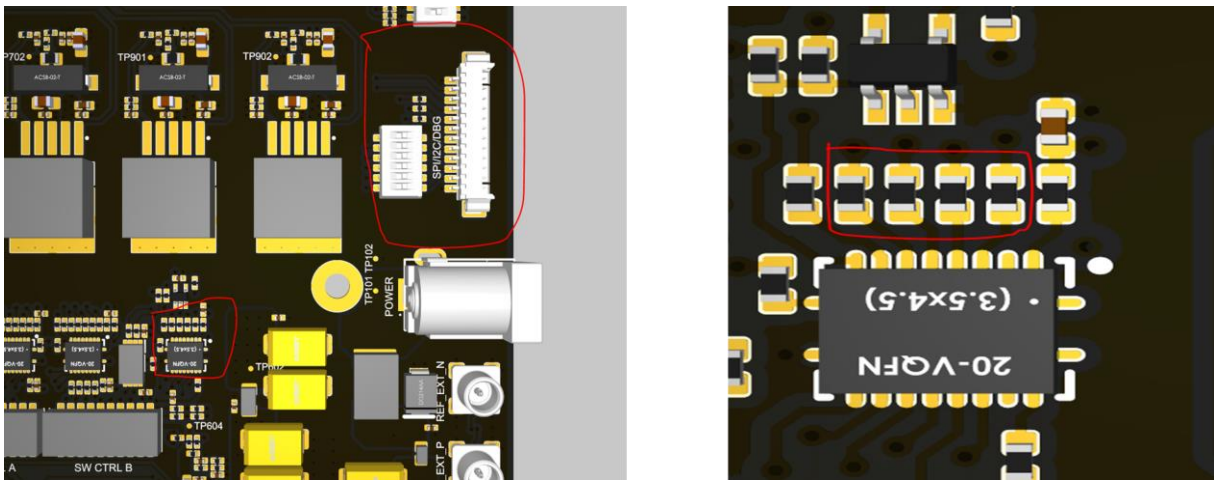
Connect the external SPI signals according to Figure 22. The corresponding inputs on "SW101" should be switched to the "ON" position.

Figure 22: Pin description of "J102" for external SPI connections



In addition, four 0 ohm resistors should also be removed as there is a conflict with the level shifter. The resistors are R506, R507, R508, and R509. Refer to Figure 23 for the positions of the 4 resistors.

Figure 23: Position of 0 Ohm resistors for external SPI control



1.8 V signals should be used. Refer to the datasheet for more information about SPI timing diagram and interface characteristics which includes DC characteristics like IO Voltage, drive current etc and AC characteristics like clock frequency, hold time, setup time etc.

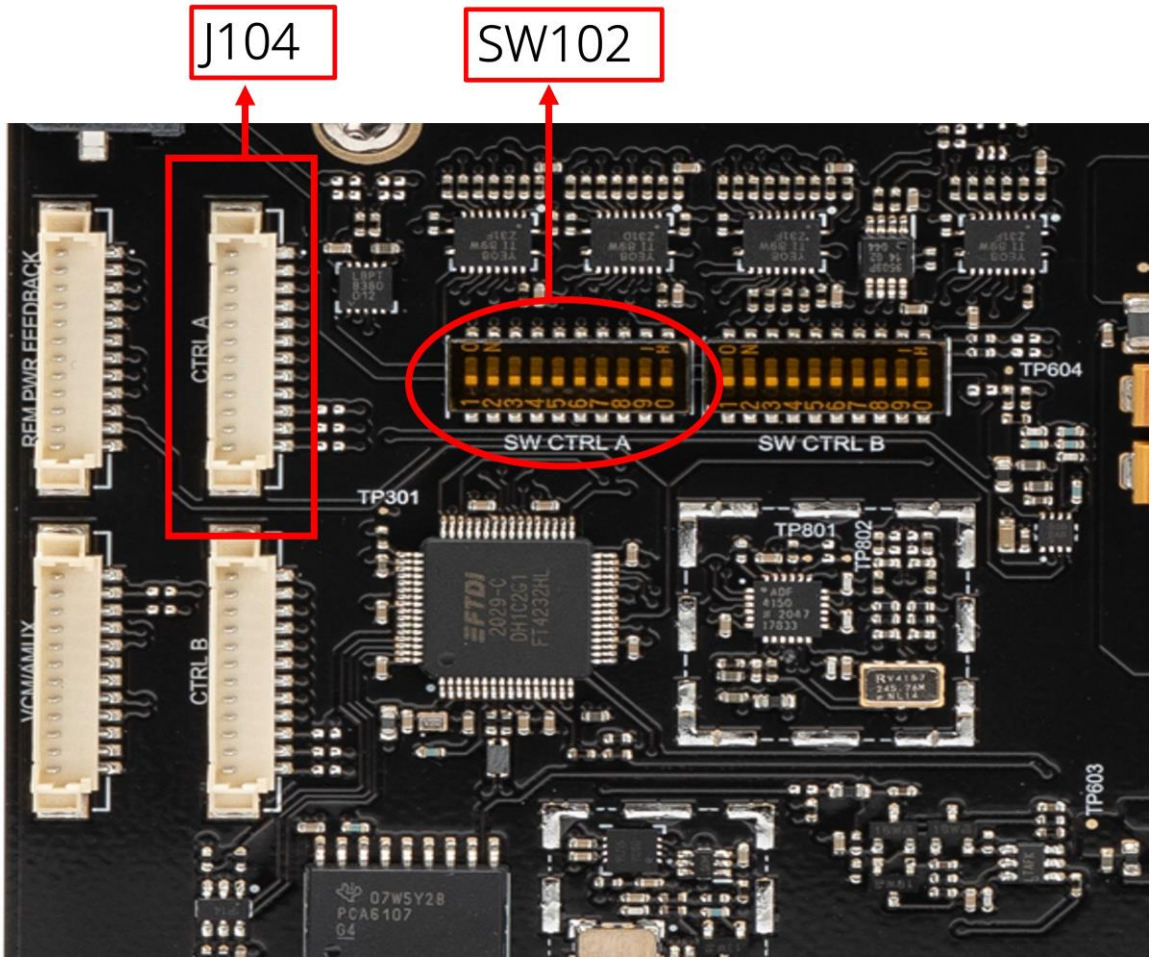
10.3 External Beamforming (BF) control

This can be achieved using the CTRL interface to the RFIC. The control interface is made up of 8 pins as described in Table 6. The connection is done via J104 on MB2 as shown in Figure 24.

Table 6: CTRL interface pin list

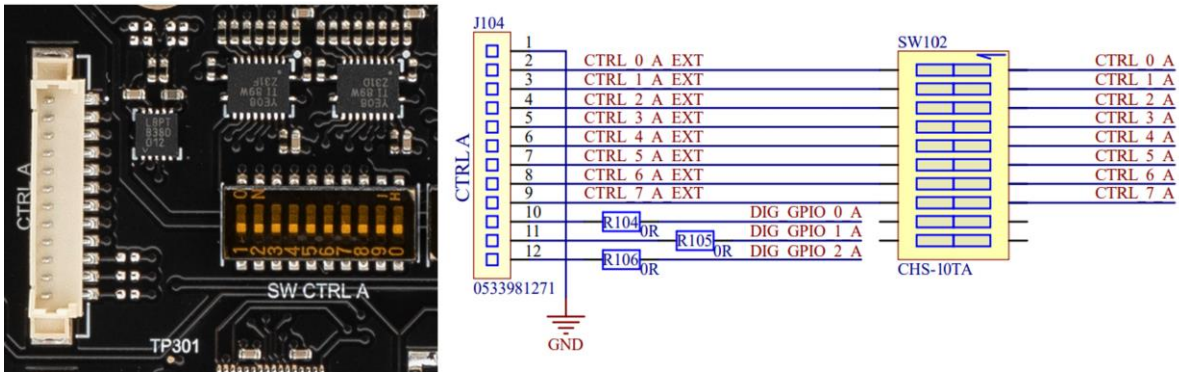
Pin name	Input/output	Type	Size	Description
CTRL_7	Input	Single ended	1	CTRL Strobe
CTRL_6:0	Input	Single ended	7	CTRL Command and data

Figure 24: "J104" used for external CTRL connections, along with the CTRL input selector switch "SW102"



Connect the external CTRL signals according to Figure 25. The corresponding inputs on "SW102" should be switched to the "ON" position.

Figure 25: Pin description of "J104" for external SPI connections



1.8 V signals should be used. Refer to the datasheet for more information about CTRL timing diagram and interface characteristics which includes DC characteristics like IO Voltage, drive current etc and AC characteristics like hold time, setup time etc.

10.3.1 Running with external BF

- The FTDI pins which drive the BF control signals need to be set as inputs when doing external BF control. Use the command sequence below to set the CTRL and DIG_GPIO pins as inputs.

  host.gpio.grp_set(1,0,255,0b11100000)
  host.gpio.grp_dir_set(1,0,0b11100000)
  host.gpio.grp_set(2,0)
  host.gpio.grp_dir_set(2,0)
  host.gpio.grp_set(3,0)
  host.gpio.grp_dir_set(3,0)

10.4 External Tx and Rx gain control

This is also achieved using the CTRL interface to the RFIC. Refer to Section 10.3 (external BF control) for more details.

11 Contact

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