NANYANG TECHNOLOGICAL UNIVERSITY

QUIZ

EE3002 – Microprocessors

27 October 2014 **Time Allowed: 30 minutes**

INSTRUCTIONS:

1. This booklet consists of 5 pages, including this cover page.
2. There are 20 multiple choice questions. All questions carry equal marks.
3. Answer all 20 questions. Shade the most suitable answers from 1 – 20 in the computerized answer sheet provided.
4. Write and shade your matriculation number on the **computerized answer sheet.**
5. The course code is EE3002/IM2002. Instead of writing course title, **write your name**. Leave the seat number empty.
6. Write your name and matriculation number on this cover page and **hand in this booklet together with the computerized answer sheet at the end of the test.**

Name: _____

Matriculation Number:

1. The ARM7TDMI processor has how many modes and states.
    a. 1 modes and 7 states
    b. 2 modes and 6 states
    c. 7 modes and 2 states
    d. 6 modes and 2 states
    e. None of the above

2. The 32-bit number 0xFFFFFFFF in IEEE 754 format represents
    a. NaN
    b. Infinity
    c. -2^{129}
    d. −Infinity
    e. None of the above

3. Represent the decimal number, −1, using 32-bit precision 2's complement form.
    a. 0x80000001
    b. 0xFFFFFFFE
    c. 0xEFFFFFFF
    d. 0xFFFFFFFF
    e. None of the above

4. What are the stages in ARM7TDMI pipeline architecture?
    a. ARM7TDMI doesn't use pipeline architecture.
    b. FETCH and EXECUTE
    c. FETCH, DECODE, EXECUTE, MEMORY, WRITE
    d. DECODE and EXECUTE
    e. FETCH, DECODE, EXECUTE

5. Add the two (32-bit precision) hexadecimal numbers, 0x80000000 and 0x80000000, and determine the values of the NZCV flags.
    a. N = 0, Z = 0, C = 0, V = 0
    b. N = 0, Z = 1, C = 1, V = 0
    c. N = 1, Z = 1, C = 1, V = 1
    d. N = 1, Z = 1, C = 1, V = 0
    e. None of the above

6. Convert the binary number, 11.11, into a decimal number, the answer is :
    a. Cannot be converted
    b. 3.3
    c. 3.75
    d. 11.75
    e. 3.11

7. In an ARM assembly language program, how many bytes will be allocated by the following statement: "Array DCW −1, −2, −3, −4, −5"
    a. 5 bytes
    b. 10 bytes
    c. 20 bytes
    d. 40 bytes
    e. None of the above

8. Which of the following is incorrect?
    a. r0 is also known as a0
    b. r13 is also known as sp
    c. r14 is also known as lr
    d. r15 is also known as pc
    e. None of the above is incorrect.

9. Which of the following instructions uses post-indexed addressing modes:
    a. STR r6, [r4, r0, ASR #4]
    b. LDR r3, [r12], #6
    c. LDR r4, [r3, r2, ROR #6]!
    d. STR r5, [r4, r0]!
    e. None of the above

10. Represent the decimal value 5.5 using 16-bit precision Q8 format.
    a. 0x0580
    b. 0x0550
    c. 0x0055
    d. 0x0058
    e. None of the above

11. What operation do the two following lines of code perform?

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ADD r0, r1, r1, LSL #5
RSB  r0, r0, r1, LSL #1
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    a. r0 = −(r1*30)
    b. r0 = −(r1*17)
    c. r0 = −(r1*16)
    d. r0 = −(r1*15)
    e. none of the above

12. Which of the following statement about the barrel shifter in ARM7TDMI is incorrect?
    a. The barrel shifter only works on the second operand of the ARM instructions.
    b. The barrel shifter only works on the first operand of the ARM instructions.
    c. The barrel shifter can be used to perform certain multiplications.
    d. The barrel shifter can be used to perform certain divisions.
    e. The operation of the barrel shifter is extremely fast.

13. Which of the following are all assembler rules and directives?
    a. ENTRY, END, MEND, MACRO
    b. DCD, DCDU, DCW, AREA
    c. ALIGN, SPACE, RN, LTORG
    d. EQU, AREA, DCWU, DCB
    e. All the above are correct

14. Consider the assembly statement "BEQ loop". Which of the following statements is correct?
    a. The program will branch to the label loop when the C flag is set.
    b. The program will branch to the label loop when the Z flag is clear.
    c. The program will branch to the label loop when the C flag is clear.
    d. The program will branch to the label loop when the Z flag is set.
    e. None of the above.

15. Which of the following instructions is used to store a value to a table? Assume that the values in the table are 32-bit numbers.
    A. LDR r1, =table_base
    B. STR r1, [r0, r2, LSL #2]
    C. LDR r1, [r0, r2, LSL #1]
    D. LDR r1, [r0, r2], #4
    E. STM r9, {r4-r6}

16. Which of the following best describe a jump table?
    A. It stores the addresses of subroutines.
    B. It must be sorted.
    C. It is a binary table.
    D. The value in the table must be in ascending order
    E. It stores several subroutines.

17. What is wrong with the instruction STMDB sp, {r3, r1, r14, r9}?
    A. The registers in the register list are not in proper order.
    B. The option "!" is missing.
    C. The base register should not be in the register list.
    D. Register r14 must be the last register in the register list.
    E. Nothing is wrong with the instruction.

18. The STMDA sp!, <reg-list> and LDMIB sp!, <reg-list> instructions are used to access the stack of a program. What type of stack is used here?
    A. Full Descending (FD)
    B. Full Ascending (FA)
    C. Empty Descending (ED)
    D. Empty Ascending (EA)
    E. None of the above

19. When BL <target> instruction is executed, the following action takes place. Assume that the address of this instruction is 0x00000020 and the <target> address is 0x00000044. The processor is operating in ARM state.
    A. Register pc is loaded with the value of 0x00000044.
    B. Register lr is loaded with the value of 0x00000020.
    C. Registers pc and lr are loaded with 0x00000044 and 0x00000024 respectively.
    D. Registers pc and lr are loaded with 0x00000044 and 0x00000020 respectively.
    E. Registers pc and lr are loaded with 0x00000048 and 0x00000024 respectively.

20. Which of the following instructions cannot be used for a subroutine to return to the calling program?
    A. MOV pc, lr
    B. STMIA sp!, {r0-r3, lr}
    C. LDMIB sp!, {r0-r3, pc}
    D. BX lr
    E. MOV r15, r14