NANYANG TECHNOLOGICAL UNIVERSITY

QUIZ

EE3002 – Microprocessors

27 March 2014 **Time Allowed: 30 minutes**

INSTRUCTIONS:

1. This booklet consists of 5 pages, including this cover page.
2. There are 20 multiple choice questions. All questions carry equal marks.
3. Answer all 20 questions. Shade the most suitable answers from 1 – 20 in the computerized answer sheet provided.
4. Write and shade your matriculation number on the **computerized answer sheet.**
5. The course code is EE3002/IM2002. Instead of writing course title, **write your name**. Leave the seat number empty.
6. Write your name and matriculation number on this cover page and **hand in this booklet together with the computerized answer sheet at the end of the test.**

Name: _____

Matriculation Number:

1. The ARM7TDMI processor has how many modes.
    a. 1
    b. 2
    c. 7
    d. None of the above

2. The 32-bit number 0x7F800000 in IEEE 754 format represents
    a. NaN
    b. Infinity
    c. $1.5*2^{128}$
    d. None of the above

3. Convert the unsigned hexadecimal 0x80000000 into a negative number represented using 2's complement form. Assume the number is stored using 32-bit precision.
    a. 0x80000000
    b. 0x00000000
    c. 0xEFFFFFFF
    d. None of the above

4. What are the stages in ARM7TDMI pipeline architecture?
    a. ARM7TDMI doesn't use pipeline architecture.
    b. FETCH and EXECUTE
    c. FETCH, DECODE and EXECUTE
    d. DECODE and EXECUTE

5. Add the two (32-bit precision) hexadecimal numbers, 0x12345678 and 0x7FFF1111, and determine the values of the C (Carry) flag and V (Overflow) flag.
    a. C = 0, V = 0
    b. C = 0, V = 1
    c. C = 1, V = 0
    d. C = 1, V = 1

6. Convert the binary number, 101.101, into a decimal number, the answer is :
    a. Cannot be converted
    b. 5.101
    c. 5.5
    d. 5.625

7. In an ARM assembly language program, how many bytes will be allocated by the following statement: "Array DCD 1, 2, 3, 4, 5"
    a. 5 bytes
    b. 10 bytes
    c. 20 bytes
    d. None of the above

8. The Link Register (lr) is also known as register ?
    a. r0
    b. r13
    c. r14
    d. r15

9. Which of the following instructions use pre-indexed addressing modes:
    a. STR r6, [r4], r0, ASR #4
    b. LDR r3, [r12], #6
    c. LDR r4, [r3, r2, ROR #6]!
    d. None of the above

10. Which of the following statements is incorrect?
    a. There are 4 flags in the Current Program Status Register and they are N, Z, C, V.
    b. The Current Program Status Register contains the Mode bits.
    c. The Current Program Status Register contains the interrupt disable bits
    d. There are 5 flags in the Current Program Status Register and they are N, Z, B, C, V

11. What operation do the two following lines of code perform?

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ADD r0, r1, r1, LSL #4
RSB  r0, r0, r1, LSL #1
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    a. r0 = −(r1*17)
    b. r0 = −(r1*16)
    c. r0 = −(r1*15)
    d. none of the above

12. Which of the following statement about the barrel shifter in ARM7TDMI is incorrect?
    a. The barrel shifter only works on the second operand of the ARM instructions.
    b. The barrel shifter only works on the first operand of the ARM instructions.
    c. The barrel shifter can be used to perform certain multiplications.
    d. The barrel shifter can be used to perform certain divisions.

13. Which of the following statements about assembler directives is CORRECT?
    a. Assembler directives are instructions for the assembler.
    b. Assembler directives are translated into ARM Instructions.
    c. Assembler directives are executed by the ARM7TDMI processor.
    d. The DCW directive allocates one or more words of memory.

14. Consider the assembly statement "BNE loop". Which of the following statements is correct?
    a. The program will branch to the label loop when the C flag is set.
    b. The program will branch to the label loop when the Z flag is clear.
    c. The program will branch to the label loop when the C flag is clear.
    d. The program will branch to the label loop when the Z flag is set.

15. Which of the following instructions is used to move the register content to an element of a table?
    a. LDR r1, =table_base
    b. STR r1, [r0, r2, LSL #2]
    c. LDR r1, [r0, r2, LSL #1]
    d. LDR r1, [r0, r2], #4

16. Which of the following best describe a jump table?
    a. It must be sorted.
    b. It stores the addresses of subroutines.
    c. It is a literal pool.
    d. The table must be stored at the end of the program.

17. What is wrong with the instruction STMDB sp, {r3, r1, r13, r9}?
    a. The registers in the register list are not in proper order.
    b. The option "!" is missing.
    c. The base register should not be in the register list.
    d. Nothing is wrong with the instruction.

18. The STMIA sp!, <reg-list> and LDMDB sp!, <reg-list> instructions are used to access the stack of a program. What type of stack is used here?
    a. Full Descending (FD)
    b. Full Ascending (FA)
    c. Empty Descending (ED)
    d. Empty Ascending (EA)

19. When BL <target> instruction is executed, the following action takes place. Assume that the address of this instruction is 0x00000010 and the <target> address is 0x00000034. The processor is operating in ARM state.
    a. Register lr is loaded with the value of 0x00000034.
    b. Register pc is loaded with the value of 0x00000010.
    c. Registers pc and lr are loaded with 0x00000034 and 0x00000014 respectively.
    d. Registers pc and lr are loaded with 0x00000038 and 0x00000010 respectively.

20. Which of the following instructions can be used for a subroutine to return to the calling program?
    a. MOV lr, pc
    b. STMIA sp!, {r0-r3, lr}
    c. STMIA sp!, {r0-r3, pc}
    d. BX lr