1. The ARM7TDMI processor has how many states.
    a. 1
    b. 2
    c. 7
    d. None of the above

2. The 32-bit number 0x7FC00000 in IEEE 754 format represents
    a. NaN
    b. Infinity
    c. $1.5*2^{128}$
    d. None of the above

3. Convert the hexadecimal 0x1F00DAAA into its 2's complement form. Assume the number is stored using 32-bit precision.
    a. 0x9F00DAAA
    b. 0xE0FF2555
    c. 0xE0FF2556
    d. None of the above

4. How many stages are there in ARM7TDMI pipeline architecture?
    a. ARM7TDMI doesn't use pipeline architecture.
    b. 5
    c. 3
    d. 2

5. Add the two (32-bit precision) hexadecimal numbers, 0x12345678 and 0xFFFF1111, and determine the values of the C (Carry) flag and V (Overflow) flag.
    a. C = 0, V = 0
    b. C = 0, V = 1
    c. C = 1, V = 0
    d. C = 1, V = 1

6. Convert the decimal number, 10.75, to a binary fraction, the answer is :
    a. Cannot be converted
    b. 1010.11
    c. 1010
    d. 10.11

7. In an ARM assembly language program, how many bytes will be allocated by the following statement: "Array DCW 1, 2, 3, 4, 5"
    a. 5 bytes
    b. 10 bytes
    c. 20 bytes
    d. None of the above

8. The Program Counter (PC) is also known as register ?
    a. r0
    b. r13
    c. r14
    d. r15

9. Which of the following instructions use post-indexed addressing modes:
    a. STR r6, [r4, #4]
    b. LDR r3, [r12], #6
    c. LDRB r4, [r3, r2]!
    d. None of the above

10. Which of the following statements is true?
    a. There are 4 flags in the Current Program Status Register and they are N, Z, C, V
    b. There are 3 flags in the Current Program Status Register and they are Z, C, V
    c. There are 4 flags in the Current Program Status Register and they are Z, B, C, V
    d. There are 5 flags in the Current Program Status Register and they are N, Z, B, C, V

11. What operation do the two following lines of code perform?

```
ADD r0, r1, r1, LSL #1
SUB  r0, r0, r1, LSL #4
```

    a. r0 = r1*3
    b. r0 = r1*16
    c. r0 = −(r1*16)
    d. r0 = r1*(−13)

12. Which of the following statement about the barrel shifter in ARM7TDMI is correct?
    a. The barrel shifter only works on the second operand of the ARM instructions.
    b. The barrel shifter only works on the first operand of the ARM instructions.
    c. The barrel shifter works on both operands of the ARM instructions.
    d. There isn't any barrel shifter in the ARM7TDMI.

13. Which of the following statements about assembler directives is INCORRECT?
    a. Assembler directives are instructions for the assembler.
    b. Assembler directives are not translated into ARM Instructions.
    c. Assembler directives are executed by the ARM7TDMI processor.
    d. AREA, RN, EQU, ENTRY are frequently used assembler directives.

14. Consider the assembly statement "BEQ loop". Which of the following statements is correct?
    a. The program will branch to the label loop when the C flag is set.
    b. The program will branch to the label loop when the N flag is set.
    c. The program will branch to the label loop when the V flag is set
    d. The program will branch to the label loop when the Z flag is set

15. Which of the following instructions is used to load an element of a table to a register? Assume that the elements in the table are 32-bit numbers.
    a. LDR r1, =table_base
    b. STR r1, [r0, r2, LSL #2]
    c. LDR r1, [r0, r2, LSL #1]
    d. LDR r1, [r0, r2], #4

16. Which of the following best describe a jump table?
    a. It stores the addresses of subroutines.
    b. It must be sorted.
    c. It is a binary table.
    d. The value in the table must be in ascending order

17. What is wrong with the instruction STMDB sp, {r3, r1, r14, r9}?
    a. The registers in the register list are not in proper order.
    b. The option "!" is missing.
    c. The base register should not be in the register list.
    d. Nothing is wrong with the instruction.

18. The STMDA sp!, <reg-list> and LDMIB sp!, <reg-list> instructions are used to access the stack of a program. What type of stack is used here?
    a. Full Descending (FD)
    b. Full Ascending (FA)
    c. Empty Descending (ED)
    d. Empty Ascending (EA)

19. When BL <target> instruction is executed, the following action takes place. Assume that the address of this instruction is 0x00000010 and the <target> address is 0x00000034. The processor is operating in ARM state.
    a. Register pc is loaded with the address of target (=0x00000034).
    b. Register lr is loaded with the value of 0x00000010.
    c. Registers pc and lr are loaded with 0x00000034 and 0x00000014 respectively.
    d. Registers pc and lr are loaded with 0x00000038 and 0x00000010 respectively.

20. Which of the following instructions cannot be used for a subroutine to return to the calling program?
    a. MOV pc, lr
    b. STMIA sp!, {r0-r3, lr}
    c. STMIA sp!, {r0-r3, pc}
    d. BX lr