EEE3002 Microprocessors Tutorial 2 (2014 Sem 1)

1) Convert the following decimal numbers into IEEE 754 single-precision format and write your answers in hexadecimal form.
   a) 0.1743129
   b) −31.5
   c) 8E−39

2) Add the following 8-bit binary number pairs using 8-bit addition (result stored in eight bits only) and comment on whether there is an overflow if they were both unsigned numbers or they were both signed numbers.
   a) 0011 1111 and 1101 0011
   b) 0111 1111 and 0111 0011
   c) 1000 1111 and 1101 0011

3) How many modes does the ARM7TDMI processor have? Name the modes also. How many states does it have?

4) What are the standard use of register r13, r14 and r15?

5) If the ARM processor encounters an undefined instruction, from what address will it begin fetching instructions after it changes to Undefined mode? What about a reset?

6) How many stages does the ARM7TDMI pipeline have? Name them.

7) Explain the current program state if the CPSR had the value 0x700000D3

EE3002 Microprocessors Tutorial 2 Solutions

1) This question can be solved using the following steps if it is a NORMAL number
   - Step 1, determine the sign bit (0: positive numbers and 1: negative numbers)
   - Step 2, determine the exponent and stored it as an 8-bit number in excess 127 format.
   - Step 3, determine the mantissa, should be between 1 and 2, then subtract 1 to store the remainder in binary fraction format.
   - Step 4, put everything together.

   a) 0.1743129

Step 1: Compute Sign Bit

0.1743129 is positive, hence sign bit, S, is 0

Step 2: Compute Exponent

floor($\log_2$ 0.1743129) = floor (−2.52) = −3

Exponent = –3
Since exponent in IEEE 754 is excess 127 form or 127 – 3 = 124
124 = 0111 1100B

Step 3: Compute Mantissa

$0.1743129 \times 2^3 = 1.3945032$ (between 1 and 2)

Convert 0.3945032 (subtract 1) into 23 bit binary fraction

round(0.3945032×2^{23}) = 3309333

Convert 3309333 into hexadecimal first

3309333 = 0x327F15 = 01100100111111100010101B (23 bits binary fraction)

Step 4
Putting everything together

S	E	E	E	E	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0	0	1	1	1	1	1	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	0	0	0	1	0	1	0	1
3				E				3				2				7				F				1				5			

b) −31.5

Step 1: Compute Sign Bit

−31.5 is negative, hence sign bit, S, is 1

Step 2: Compute Exponent

floor($\log_2$ (31.5)) = floor (4.977) = 4

Exponent = 4

Since exponent in IEEE 754 is excess 127 form or 127 + 4 = 131

131 = 10000011B

Step 3: Compute Mantissa

31.5 $\times 2^{-4}$ = 1.96875 (between 1 and 2)

Convert 0.96875 (after subtract 1) into 23 bit binary fraction

round(0.96875×2^{23}) = 8126464

Convert 8126464 into hexadecimal first

8126464 = 0x7C0000 = 111 1100 0000 0000 0000 0000B (23 bits binary fraction)

Step 4

Putting everything together

S	E	E	E	E	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
1	1	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C				1				F				C				0				0				0				0			

c) 8E−39

The number is smaller than the smallest magnitude that can be represented by a normal IEEE 754 number, hence it must be a subnormal number.

Step 1: Compute Sign Bit

Positive, hence sign bit, S, is 0

Step 2: Compute Exponent

IEEE 754 Exponent = 0 for subnormal numbers

Step 3: Compute Mantissa

8E-39/2^{-126} = 0.680564734 (less than 1)

Convert 0.680564734 into 23 bit binary fraction

round($0.680564734 \times 2^{23}$) = 5708991

Convert 5708991 into hexadecimal first

5708991 = 0x571CBF = 101 0111 0001 1100 1011 1111B (23 bits binary fraction)

Step 4

Putting everything together

S	E	E	E	E	E	E	E	E	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0	0	0	1	1	1	0	0	1	0	1	1	1	1	1	1
0				0				5				7				1				C				B				F			

2)

		Binary	Unsigned	Signed
a)		0011 1111B	63	63
	+	1101 0011B	+ 211	− 45
		0001 0010B, C =1	18(wrong)	18 (correct)

Unsigned numbers : Overflow
Signed numbers : No Overflow

The Carry flag, C, can be used to indicate Unsigned Overflow.

		Binary	Unsigned	Signed
b)		0111 1111B	127	127
	+	0111 0011B	+ 115	+ 115
		1111 0010B, C = 0	242(correct)	− 14 (wrong)

Unsigned numbers : No Overflow
Signed numbers : Overflow
The Carry flag, C, cannot be used to indicate signed Overflow. A separate flag,V, is used to indicate sign overflow. V will be set to 1 in this case.

		Binary	Unsigned	Signed
c)		1000 1111B	143	− 113
	+	1101 0011B	+ 211	− 45
		0110 0010B, C =1	98(wrong)	98 (wrong)

Both Unsigned and Signed Overflow. C = V = 1. The overflow flag, V, will be set if there is a carry out of Bit 7 but not from Bit 6 (Part c) or if there is a carry out of Bit 6 but not from Bit 7 (Part b). The same principle can be extended to higher word length, a 32-bit addition, the sign bit will be Bit 31 instead of Bit 7, and the largest signed magnitude bit will be Bit 30 instead of Bit 6.

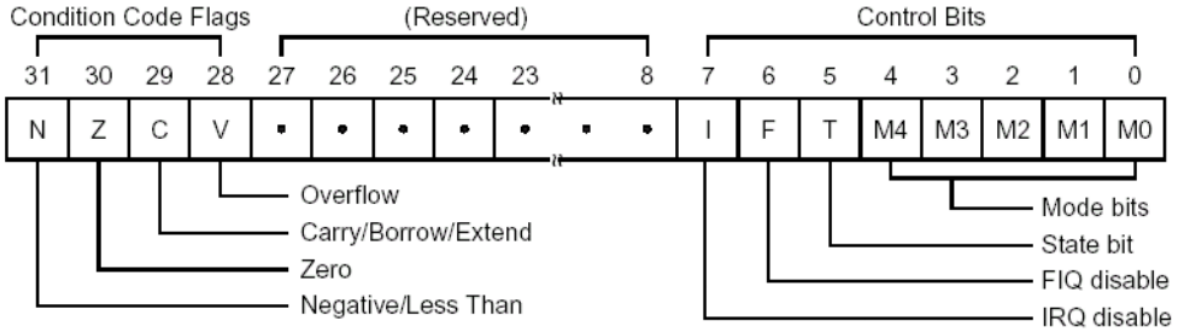
3) ARM7TDMI has 7 processor modes, namely Supervisor, FIQ, IRQ, Abort, Undef, System and User.
ARM7TDMI has two states: ARM state (32-bit instruction) and THUMB state (16-bit instruction).

4) R13 : Stack Pointer which holds the address of the stack in memory
R14 : Link Register which is used as subroutine return address link register.
R15: Program Counter which contains the address of the instruction being fetched (not executed).

5) For Undef exception, the address of the instruction is 0x00000004
For Reset exception, the address of the instruction is 0x00000000

6) The ARM7TDMI has a 3-stage pipelined architecture, the 3 stages are FETCH, DECODE and EXECUTE

7) CPSR is the Current Program Status Register which is of the form shown below:



0x700000D3 = 0111 0000 0000 0000 0000 0000 1101 0011B

Hence flags N = 0, Z = 1, C = 1, V =1 are all set.
I and F is set to 1 means interrupts (IRQ) and fast interrupts (FIQ) are disabled
T = 0, means it is in ARM state
Mode bits = 10011, means the mode is in Supervisor Mode.