

### GENERAL DESCRIPTION

The SGM61163 is an efficient, 6A, synchronous, Buck converter with integrated power MOSFETs and a wide 4.5V to 18V input range. This current mode control device is optimized for high density applications with minimal number of external components. High switching frequency, up to 2MHz, can be chosen to reduce the solution size by smaller inductor and capacitors. This device can be used as a standalone or tracking power supply. The SS/TR pin can be used to control the output voltage startup ramp or as an input for tracking.

Power supply sequencing for two or more power supplies is possible by using the enable input (EN) and the open-drain power good output (PG) signals.

The high-side (HS) MOSFET current is cycle-by-cycle limited for overload protection. The low-side (LS) MOSFET sourcing current is also limited to prevent current runaway. The low-side switch also has a sinking current limit that turns it off if an excessive reverse current flows through it.

Thermal shutdown protection is activated to prevent damage to the device when the junction temperature is above the shutdown threshold.

The SGM61163 is available in a Green TQFN-3.5x3.5-14L package and can operate over the wide ambient temperature range of -40°C to +125°C.

### TYPICAL APPLICATION

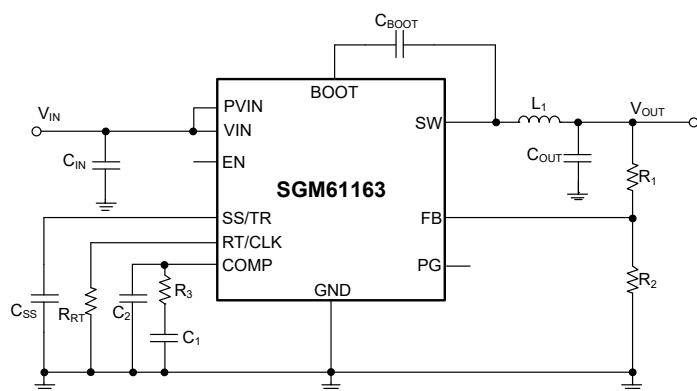


Figure 1. Typical Application Circuit

### FEATURES

- Low Integrated  $R_{DS(on)}$  Switches: 27mΩ/18mΩ
- Split Rails for Supply (VIN) and Power (PVIN)
  - 1.8V to 18V Range for PVIN
  - 4.5V to 18V Range for VIN
- 200kHz to 2MHz Switching Frequency
- External Clock Synchronization
- Voltage Tracking Capability
- 0.6V Internal Reference Voltage
- ±1% Reference Voltage Accuracy
- 3.4µA (TYP) Shutdown Current
- Hiccup Mode Current Limit
- Monotonic Startup with Pre-biased Outputs
- Adjustable Soft-Start Time
- Power Sequencing Capability
- Power Good Output Monitor for Under-Voltage and Over-Voltage Protections
- Adjustable Input Under-Voltage Lockout (UVLO)
- -40°C to +125°C Operating Temperature Range
- Available in a Green TQFN-3.5x3.5-14L Package

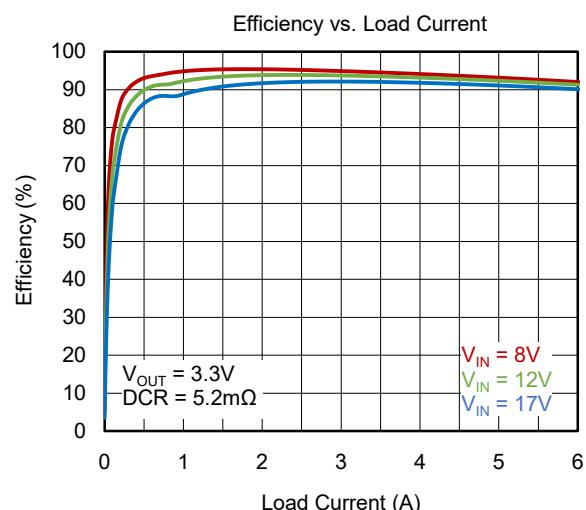
### APPLICATIONS

Industrial and Commercial Power Systems

Distributed Power Systems

Server and Storage

Communications Equipment

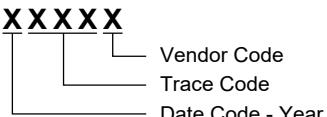


**PACKAGE/ORDERING INFORMATION**

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61163	TQFN-3.5x3.5-14L	-40°C to +125°C	SGM61163XTRI14G/TR	SGM 61163RI XXXXX	Tape and Reel, 6000

**MARKING INFORMATION**

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

VIN Voltage.....	-0.3V to 22V
PVIN Voltage .....	-0.3V to 22V
EN, PG, RT/CLK Voltage.....	-0.3V to 6V
BOOT Voltage .....	-0.3V to 29V
BOOT Voltage 3ns Transient.....	-0.5V to 32V
FB, COMP, SS/TR Voltage.....	-0.3V to 3V
BOOT-SW.....	0V to 7V
SW .....	-1V to 22V
SW 10ns Transient .....	-3V to 22V
SW 3ns Transient .....	-6.5V to 26V
Package Thermal Resistance	
TQFN-3.5x3.5-14L, $\theta_{JA}$ .....	42°C/W
Junction Temperature.....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility	
HBM.....	2000V
CDM .....	1000V

**RECOMMENDED OPERATING CONDITIONS**

Input Voltage Range .....	4.5V to 18V
Power Stage Input Voltage Range.....	1.8V to 18V
Operating Junction Temperature Range.....	-40°C to +150°C

**OVERSTRESS CAUTION**

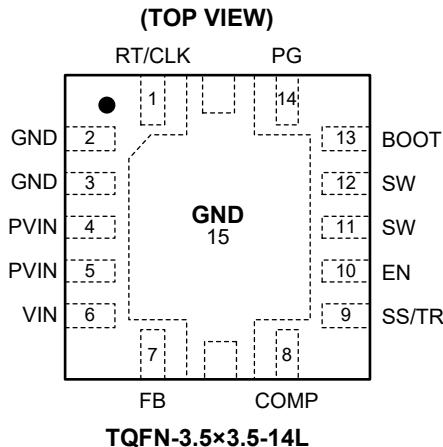
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

**ESD SENSITIVITY CAUTION**

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

**PIN CONFIGURATION****PIN DESCRIPTION**

PIN	NAME	I/O	DESCRIPTION
1	RT/CLK	I	An input pin for RT programming resistor or external CLK input (auto select) for setting the switching frequency. In RT mode, an external timing resistor connected between this pin and GND adjusts the switching frequency. In CLK mode, an external clock sets the switching frequency.
2, 3	GND	G	Ground Pin.
4, 5	PVIN	P	Power Input for the Power Stage Switches. PVIN voltage can be lower or higher than VIN voltage.
6	VIN	P	Power Input for the Control Circuitry.
7	FB	I	Inverting Input of the transconductance error amplifier with $gm = 1450\mu\text{A/V}$ gain.
8	COMP	O	Transconductance Error Amplifier Output. Connect the frequency compensation circuit between this pin and GND.
9	SS/TR	I/O	Soft-start and Tracking Input. Connect a capacitor between the SS and GND pins to set the rise time of the internal voltage reference. A voltage applied on this pin (TR) overrides the internal reference and the output will follow that voltage. This feature is used for tracking and sequencing functions.
10	EN	I	Enable Input Pin with Internal Pull-up. Float this pin to enable the device or pull it down to disable it. The EN input can be used to adjust the input UVLO by a resistor divider from VIN or PVIN.
11, 12	SW	O	Switching Node Output of the Converter.
13	BOOT	I	Bootstrap Input to Supply the High-side Gate Driver. A bootstrap capacitor ( $0.1\mu\text{F}$ ) is required between the BOOT and SW pins. The voltage on this capacitor supplies the gate driver of the high-side MOSFET.
14	PG	O	Power Good Open-drain Output Pin. PG is released to go high by the external pull-up resistor if the output is in regulation. It is pulled low during soft-start, when EN is low or during fault events such as thermal shutdown, dropout and over-voltage.
Exposed Pad	GND	G	Package Thermal Pad and Analog Ground. This pad must be soldered to the ground plane for proper operation and heat relief. Connect it to a PCB ground on the top layer that is only connected to the GND pins and use it as reference for RT, COMP, SS/TR, UVLO setting and VIN bypass.

NOTE: I = input, O = output, I/O = input or output, G = ground, P = power.

**ELECTRICAL CHARACTERISTICS**(T<sub>J</sub> = -40°C to +125°C, V<sub>IN</sub> = 4.5V to 18V, V<sub>PVIN</sub> = 1.8V to 18V, typical values are at V<sub>IN</sub> = 12V and T<sub>J</sub> = +25°C, unless otherwise noted.)

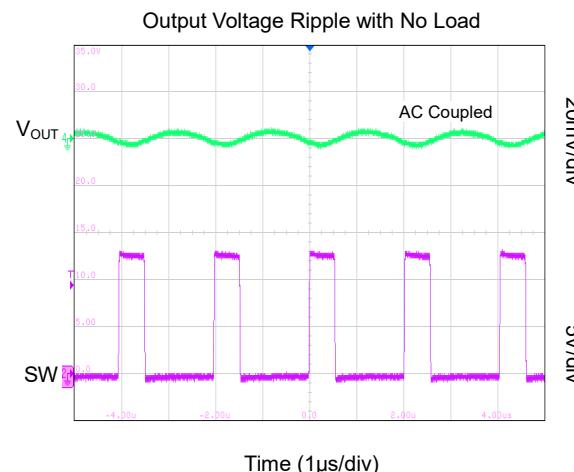
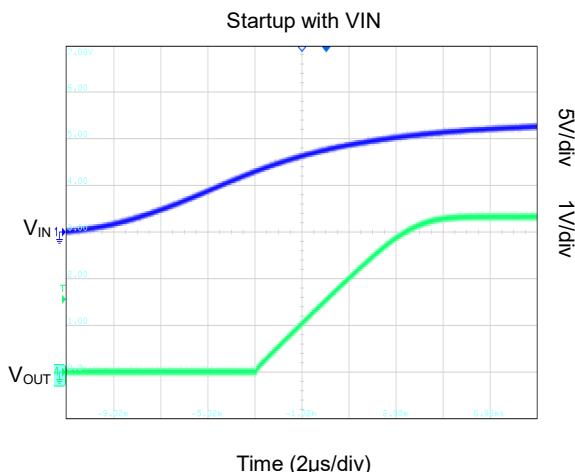
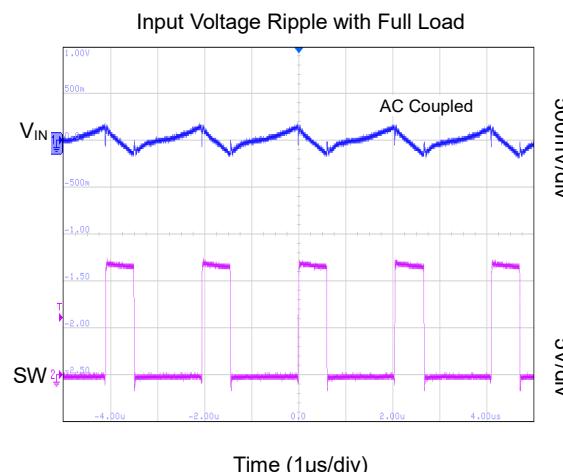
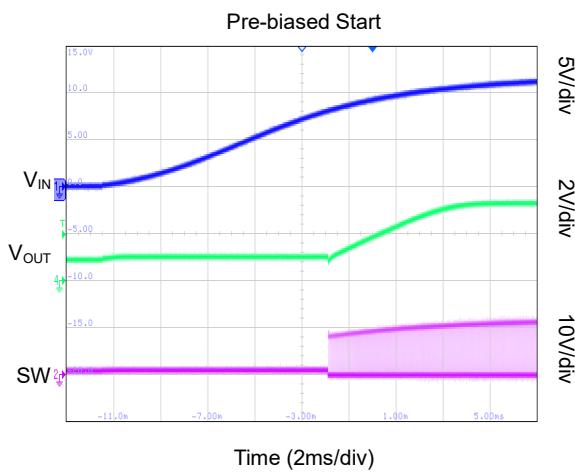
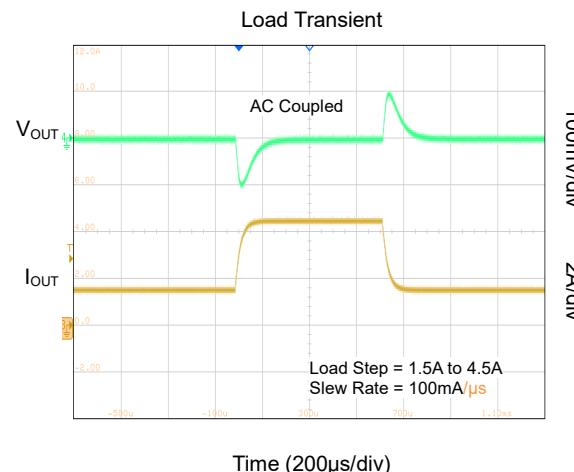
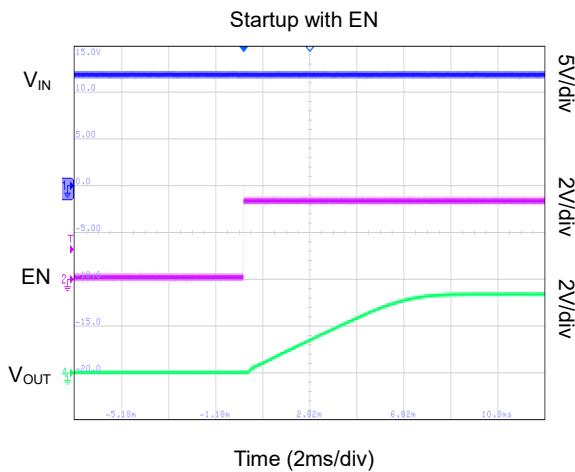
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Voltage (VIN and PVIN Pins)</b>						
PVIN Operating Input Voltage	V <sub>PVIN</sub>		1.8		18	V
PVIN OVP	V <sub>PVIN_OVP</sub>	PVIN rising		24		V
PVIN OVP Hysteresis	V <sub>PVIN_OVP_H</sub>	PVIN falling		0.3		V
VIN Operating Input Voltage	V <sub>IN</sub>		4.5		18	V
VIN Internal UVLO Threshold	V <sub>IN_UVLO</sub>	V <sub>IN</sub> rising		4	4.5	V
VIN Internal UVLO Hysteresis	V <sub>IN_UVLOHYS</sub>			180		mV
VIN Shutdown Supply Current	I <sub>SD</sub>	EN = 0V, V <sub>IN</sub> = 12V		3.4	6.4	µA
VIN Non-Switching Operating Supply Current		V <sub>FB</sub> = 610mV, V <sub>IN</sub> = 12V		1.1	1.5	mA
<b>Enable and UVLO (EN Pin)</b>						
Enable Rising Threshold	V <sub>ENRISING</sub>	Rising		1.20	1.35	V
Enable Falling Threshold	V <sub>ENFALLING</sub>	Falling	1	1.15		V
Input Current	I <sub>P</sub>	EN = 1.1V		1.1		µA
Hysteresis Current	I <sub>H</sub>	EN = 1.3V		3.3		µA
<b>Reference Voltage</b>						
Reference Voltage	V <sub>REF</sub>	Measured at FB, T <sub>J</sub> = +25°C	0.594	0.6	0.606	V
		Measured at FB	0.591		0.609	
<b>Power MOSFETs</b>						
High-side Switch Resistance	R <sub>DSON_H</sub>	BOOT-SW = 3.3V		29	50	mΩ
High-side Switch Resistance <sup>(1)</sup>		BOOT-SW = 5V		27	45	
Low-side Switch Resistance <sup>(1)</sup>	R <sub>DSON_L</sub>	V <sub>IN</sub> = 12V		18	30	mΩ
<b>Error Amplifier</b>						
Error Amplifier Transconductance (gm)	g <sub>meA</sub>	-2µA < I <sub>COMP</sub> < 2µA, V <sub>COMP</sub> = 1V		1450		µA/V
Error Amplifier DC Gain	A <sub>DC</sub>	V <sub>FB</sub> = 0.6V		10000		V/V
Error Amplifier Source/Sink		V <sub>COMP</sub> = 1V, 100mV input overdrive		±120		µA
Start Switching Threshold				0.79		V
COMP to I <sub>SWITCH</sub> gm				16		A/V
<b>Current Limit</b>						
High-side Switch Current Limit Threshold		T <sub>J</sub> = +25°C	9.00	11.5	14.00	A
Low-side Switch Sourcing Current Limit		T <sub>J</sub> = +25°C	7.50	10	12.50	A
Low-side Switch Sinking Current Limit		T <sub>J</sub> = +25°C	2.2	3.2	4.2	A
Hiccup Wait Time				512		Cycles
Hiccup Time before Restart				16384		Cycles
<b>Thermal Shutdown</b>						
Thermal Shutdown	T <sub>SD</sub>			175		°C
Thermal Shutdown Hysteresis	T <sub>SD_HYS</sub>			15		°C

NOTE: 1. Measured at pins.

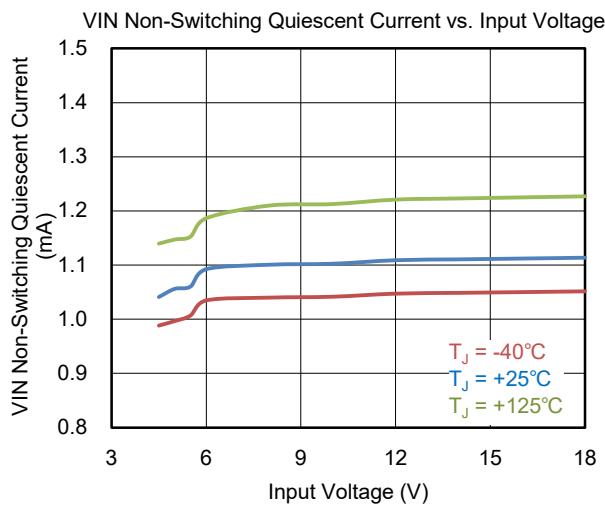
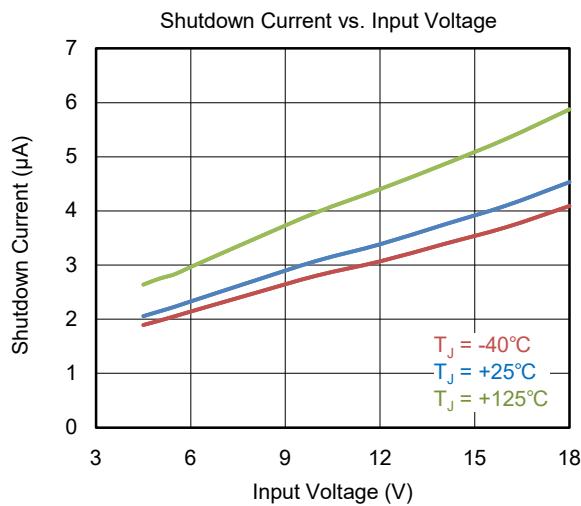
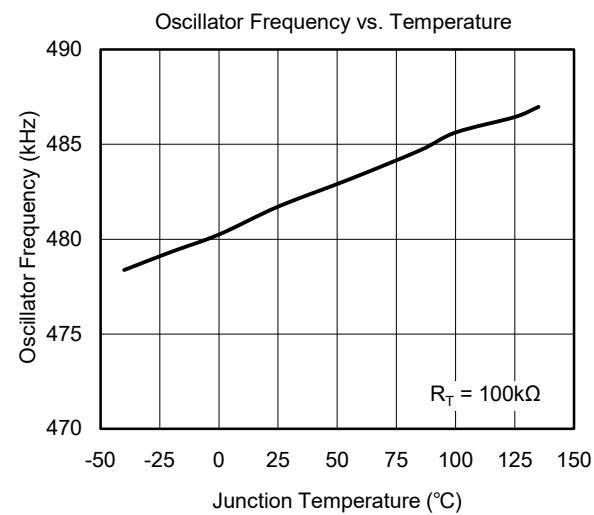
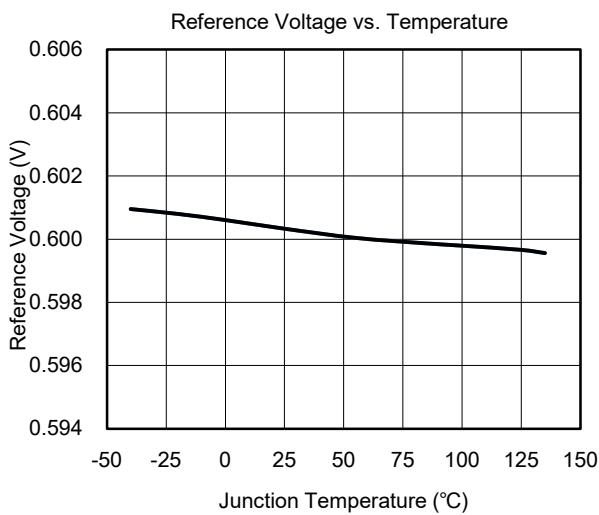
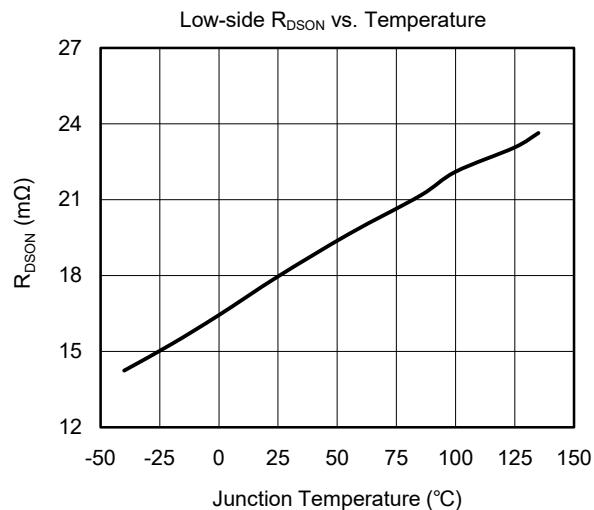
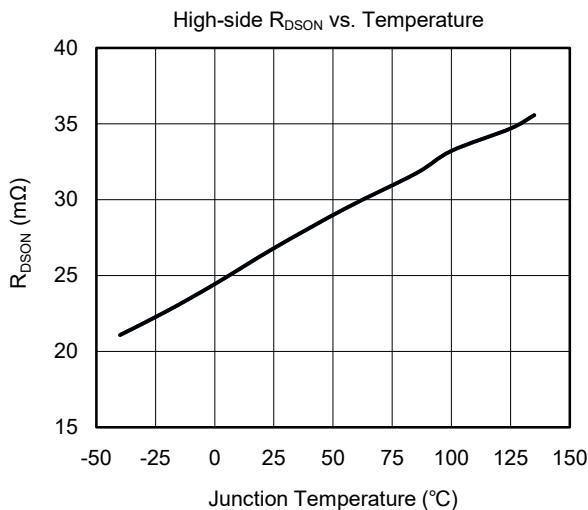
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Timing Resistor and External Clock (RT/CLK Pin)</b>						
Minimum Switching Frequency	f <sub>SW</sub>	R <sub>RT</sub> = 240kΩ (1%)	170	210	250	kHz
Switching Frequency		R <sub>RT</sub> = 100kΩ (1%)	400	480	560	
Maximum Switching Frequency		R <sub>RT</sub> = 21.5kΩ (1%)	1750	2000	2250	
Minimum Pulse Width				20		ns
RT/CLK High Threshold					2	V
RT/CLK Low Threshold			0.8			V
RT/CLK Falling Edge to SW Rising Edge Delay		Measured at 500kHz with RT resistor in series		35		ns
Switching Frequency Range (RT Mode Set Point and PLL Mode)			200		2000	kHz
<b>SW (SW Pin)</b>						
Minimum On-Time	t <sub>ON</sub>	Measured at 90% to 90% of V <sub>IN</sub> , +25°C, I <sub>SW</sub> = 2A		105		ns
Minimum Off-Time	t <sub>OFF</sub>	BOOT-SW ≥ 3V		0		ns
<b>BOOT (BOOT Pin)</b>						
BOOT-SW UVLO				2.5	3	V
<b>Soft-Start and Tracking (SS/TR Pin)</b>						
SS Charge Current	I <sub>SS</sub>			2		µA
SS/TR to FB Matching	V <sub>SSOFFSET</sub>	V <sub>SS/TR</sub> = 0.4V		35	75	mV
<b>Power Good (PG Pin)</b>						
FB Threshold		V <sub>FB</sub> falling (fault)		92% × V <sub>REF</sub>		V
		V <sub>FB</sub> rising (good)		94% × V <sub>REF</sub>		
		V <sub>FB</sub> rising (fault)		108% × V <sub>REF</sub>		
		V <sub>FB</sub> falling (good)		106% × V <sub>REF</sub>		
Output High Leakage		V <sub>FB</sub> = V <sub>REF</sub> , V <sub>PG</sub> = 5.5V		10	400	nA
Output Low		I <sub>PG</sub> = 2mA			0.3	V
Minimum VIN for Valid Output		V <sub>PG</sub> < 0.5V at 100µA		1.8	2.3	V
Minimum SS/TR Voltage for PG					1.5	V

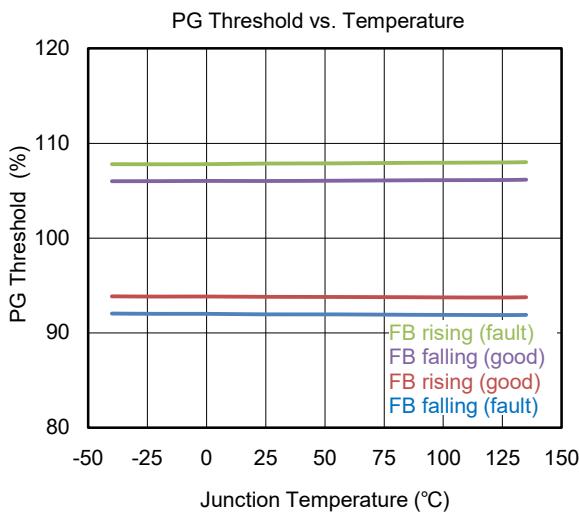
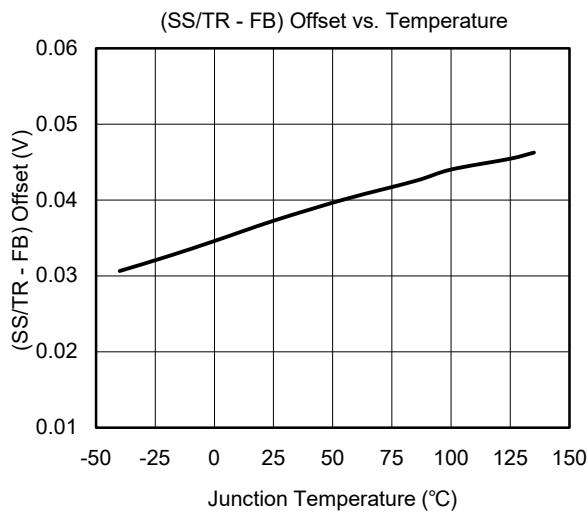
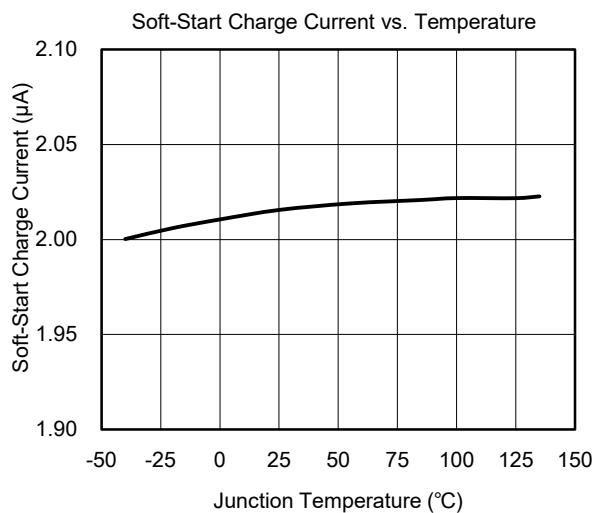
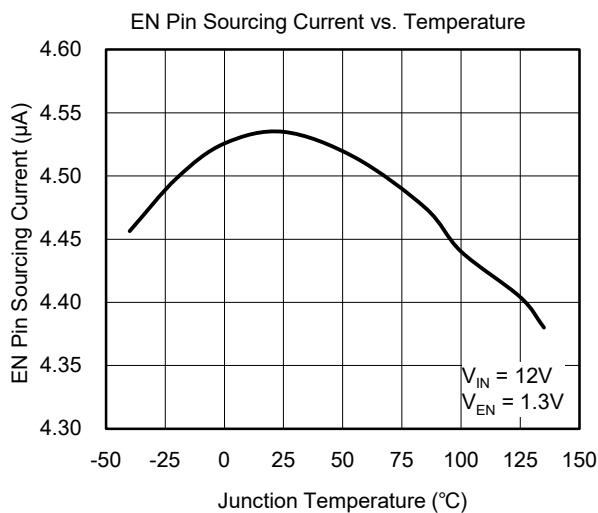
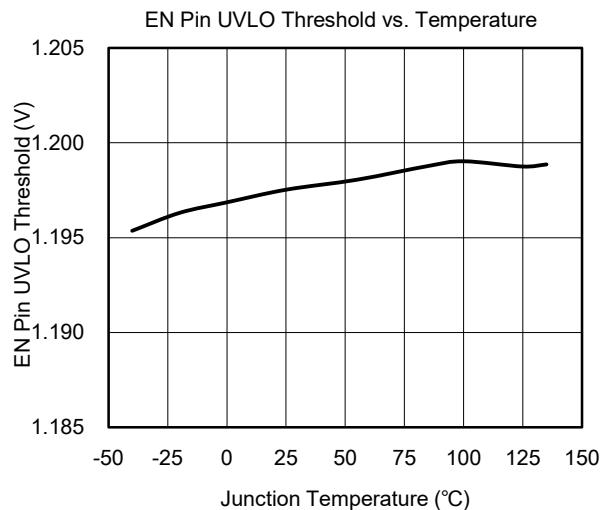
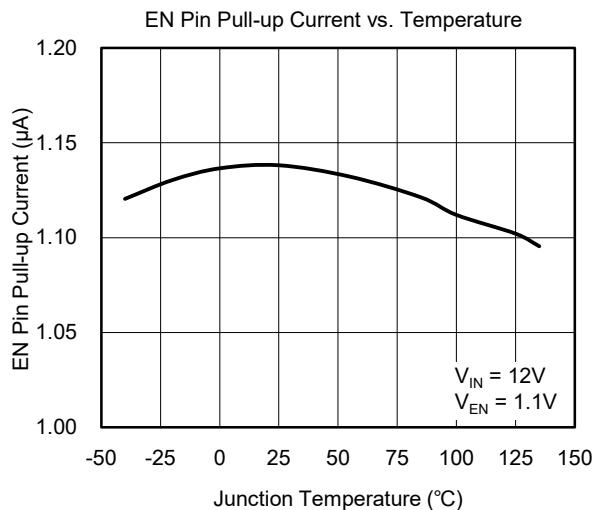
## TYPICAL PERFORMANCE CHARACTERISTICS

 $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 3.3\text{V}$ , unless otherwise noted.

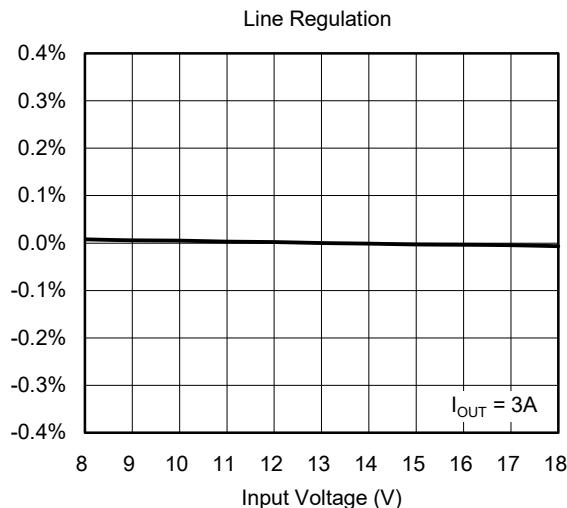
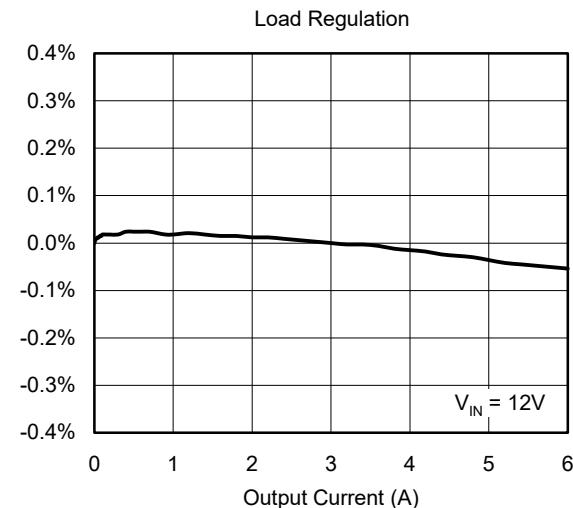
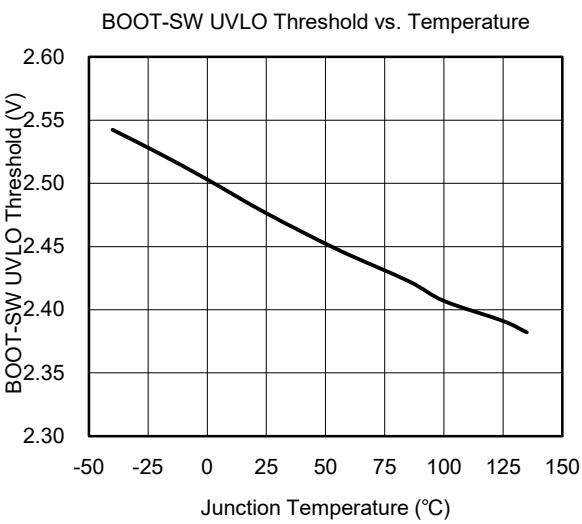
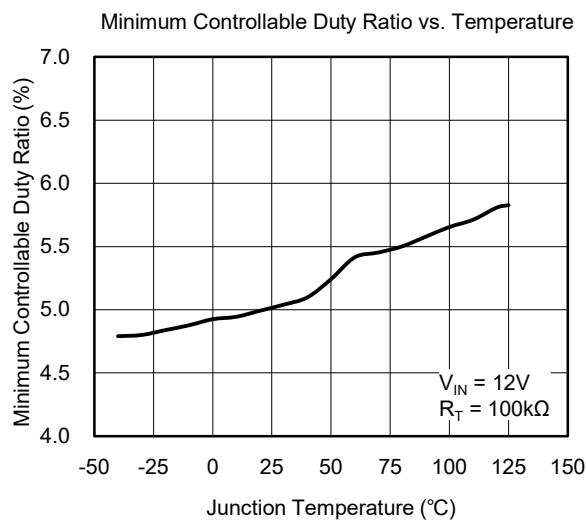
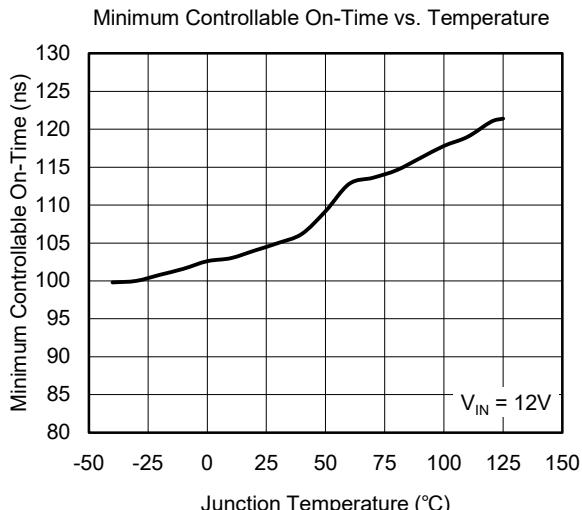
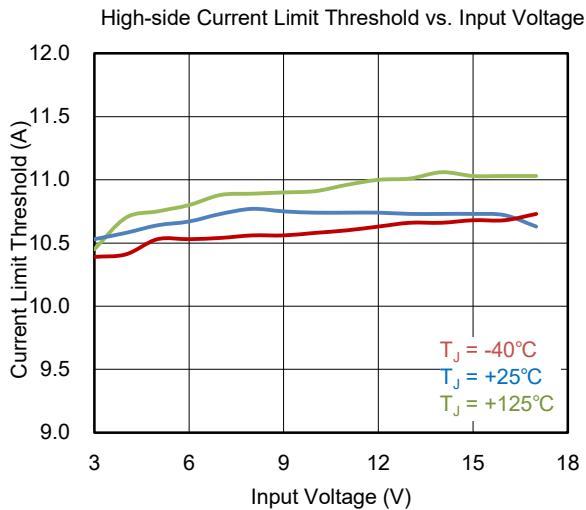
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## FUNCTIONAL BLOCK DIAGRAM

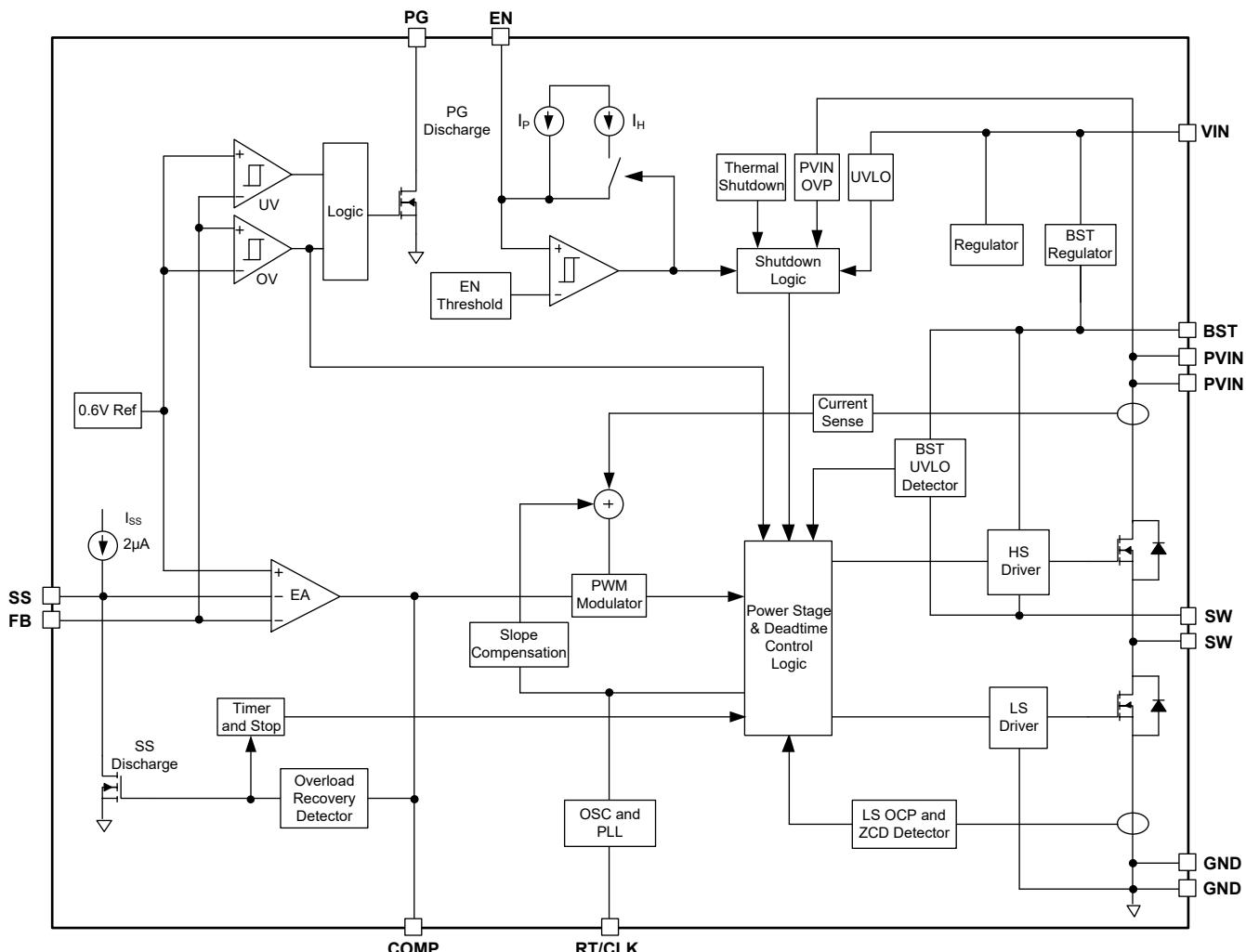


Figure 2. Block Diagram

## DETAILED DESCRIPTION

### Overview

The SGM61163 is a 4.5V to 18V, 6A, synchronous Buck converter with integrated high-side and low-side MOSFETs. The minimum achievable output voltage of this converter is 0.6V, which is equal to the device internal reference voltage ( $V_{REF}$ ).

As a constant frequency, peak current mode control device, SGM61163 can provide fast transient response with a simple compensation circuit. The fixed switching frequency is adjustable from 200kHz to 2000kHz to allow optimization of the efficiency and size of the converter. For adjusting the internal switching frequency, an external resistor  $R_{RT}$  is connected between the RT/CLK pin and GND. The device also accepts an external clock source on this pin to synchronize the oscillator using the internal phase locked loop (PLL).

This device can have a safe and monotonic startup in output pre-biased conditions. The  $V_{IN}$  must exceed the under-voltage lockout threshold (UVLO, 4V TYP) for device power-up. The UVLO thresholds can be adjusted (increased) by connecting the EN pin to the tap point of a resistor divider between the VIN (or PVIN) pin and GND. The EN internal pull-up current source and the resistor divider determine the UVLO thresholds. When the EN is floated or is pulled high, the device is enabled and the total device current (no switching) is near 1100 $\mu$ A. Pulling the EN pin low will shut down the device with less than 3.4 $\mu$ A (TYP) supply current.

The integrated MOSFETs are optimized for higher efficiency at lower duty cycles. They can efficiently provide up to 6A continuous output current.

The integrated bootstrap circuit along with the external boot capacitor provides the bias voltage for the high-side MOSFET driver. The voltage of the bootstrap capacitor that is placed between the BOOT and SW pins is continuously monitored for bootstrap UVLO (BOOT-SW UVLO) detection. If the boot capacitor voltage drops below the bootstrap UVLO, the SW pin will be pulled low to recharge the boot capacitor. 100%

duty cycle operation is possible as long as the boot capacitor voltage is higher than the 2.5V (TYP) threshold (preset UVLO level).

The device contains a Power Good (PG) pin which indicates the status of the output voltage by comparing the FB voltage and the internal reference voltage. PG pin is connected to the drain of internal MOSFET. The PG signal is high when VOUT is between 94% and 106% of its nominal (set) value and goes low if VOUT drops below 92% or rises above 108% of its nominal value.

The SS/TR (soft-start/tracking) pin can be used to minimize the inrush currents (soft-start function) with a small value capacitor, or for power supply sequencing during power-up with a resistor divider from preceding voltage rail. It is the input pin for the voltage that is followed by the output when the power supply is used in the tracking mode.

The SGM61163 is protected from output over-voltage, over-current and over-heating damage. The output over-voltage transients are effectively minimized by the over-voltage comparator of the power good circuit. When an over-voltage occurs, the high-side switch is forced off and allowed to turn on again if the VOUT drops below 106% of its nominal value.

High-side MOSFET is naturally protected from sourcing over-current by peak current mode control. The low-side MOSFET is also protected bidirectionally against over-current. This feature helps the control of the inductor current to avoid current runaway.

If a die temperature is too high ( $T_J > T_{SD}$ ), the device will stop switching and go to shutdown state. It will automatically recover with a soft-start when the junction temperature drops 15°C (TYP) below the shutdown temperature.

Note that a continued overload condition may cause a cycling thermal shutdown and recovery. It will depend on the temperature and the ventilation conditions of the system.

## DETAILED DESCRIPTION (continued)

### Power Input Pins

VIN and PVIN pins can be tied together or separated depending on the application and minimum input voltage. The VIN pin supplies the internal circuits of the device and needs to be above 4.5V, while the PVIN provides the supply voltage for the switches and can go down to 1.8V. So, if these pins are tied, the input voltage range is from 4.5V to 18V. A voltage divider connected to the EN pin from either VIN or PVIN can be used to adjust the power supply UVLO. For a consistent power-up behavior, PVIN is the recommended source for the UVLO programming.

### EN Pin and UVLO Programming

The EN pin is used to turn the device on and off. The device starts operation when the EN voltage rises above the enable rising threshold. Pulling the EN voltage below the enable falling threshold stops switching and reduces the device current to the very low quiescent shutdown level. Floating the EN pin will enable the device due to its internal pull-up current source. This current source is used for programming the UVLO threshold. An open-drain or open-collector output connected to the EN pin can be used to control the device. An internal UVLO circuit is implemented on the VIN pin to disable the device and prevent malfunction when the supply voltage is too low. The internal VIN UVLO hysteresis is 180mV. To program a higher UVLO threshold for the VIN or to add a secondary UVLO on the PVIN that is typically needed for split-rail applications, the EN pin can be configured to one of the configurations shown in Figure 3, Figure 4, or Figure 5. Without external components, the internal pull-up current ( $I_P$ ) sets the EN pin default state to enable. When the device is enabled, the second current source ( $I_H$ ) is activated.  $I_P$  and  $I_H$  are used to set the UVLO.

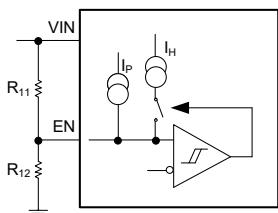


Figure 3. VIN UVLO Setting with a Resistor Divider

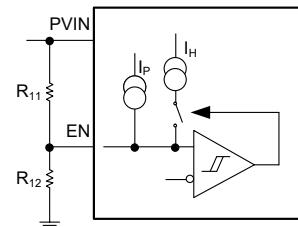


Figure 4. PVIN UVLO Setting with a Resistor Divider  
( $V_{IN} \geq 4.5V$ )

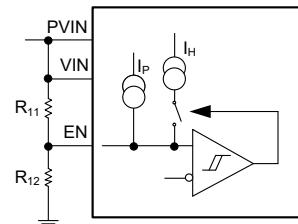


Figure 5. VIN and PVIN UVLO Setting

The resistor divider can be calculated from Equations 1 and 2 based on the desired UVLO start and stop thresholds. A 500mV or higher hysteresis ( $V_{START} - V_{STOP}$ ) is recommended for the UVLO programming.

$$R_{11} = \frac{V_{START} \left( \frac{V_{ENRISING}}{V_{ENFALLING}} \right) - V_{STOP}}{I_P \left( 1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_H} \quad (1)$$

$$R_{12} = \frac{R_{11} \times V_{ENRISING}}{V_{STOP} - V_{ENFALLING} + R_{11}(I_P + I_H)} \quad (2)$$

where:

- $I_H = 3.3\mu A$ .
- $I_P = 1.1\mu A$ .
- $V_{ENRISING} = 1.2V$ .
- $V_{ENFALLING} = 1.15V$ .

### Soft-Start (SS/TR)

The lower voltage between the internal  $V_{REF}$  and the SS/TR pin is used as the reference to regulate the output. The soft-start capacitor is connected to the SS/TR pin and is charged by a  $2\mu A$  internal current source to set the soft-start time ( $t_{SS}$ ).

Equation 3 can be used to calculate the soft-start time for a selected soft-start capacitor ( $C_{SS}$ ).

$$t_{SS} (\text{ms}) = \frac{C_{SS} (\text{nF}) \times V_{REF} (\text{V})}{I_{SS} (\mu\text{A})} \quad (3)$$

where:

- $V_{REF} = 0.6V$ .
- $I_{SS}$  is the soft-start current source ( $2\mu A$ ).

## DETAILED DESCRIPTION (continued)

### Startup with Pre-biased Output

The low-side switch is prohibited from turning on and discharging the output if a pre-biased voltage is sensed on the output before startup. As long as the SS/TR pin voltage is below  $V_{FB}$ , the low-side switch is not allowed to sink current to have a monotonic startup with pre-biased output.

### Reference Voltage ( $V_{REF}$ )

A precise 0.6V reference is internally implemented by scaling the output of a temperature-stable bandgap circuit. The reference voltage tolerance over the whole temperature range is  $\pm 1.5\%$ . The actual reference voltage for output setting is changed during startup or tracking.

### Output Voltage Setting

The output voltage of the device can be adjusted by resistors R<sub>1</sub> and R<sub>2</sub> which are connected to the FB pin (see Figure 1). Use resistors with 1% tolerance or better for good output accuracy. Equation 4 can be used to calculate the R<sub>1</sub> and R<sub>2</sub> (upper and lower resistors) values based on the desired output voltage ( $V_{OUT}$ ) and  $V_{REF}$ .

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (4)$$

where:

- $V_{REF} = 0.6V$ .

For example, a 10kΩ resistor can be chosen for R<sub>2</sub> and then R<sub>1</sub> is calculated. Do not choose too large resistors that may cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

The minimal output voltage is determined by the minimum on-time of the high-side switch. The maximal output voltage is constrained by the bootstrap voltage. More details are provided in the Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle) section.

### Power Good (PG)

The PG is an open-drain output. It is released if there is no fault and the FB pin voltage is in regulation. The PG is pulled low if the FB voltage is lower than 92% or above 108% of the reference voltage. When the device is disabled by EN pin or the voltage of SS/TR pin is

under 1.5V, or if a fault such as UVLO or thermal shutdown occurs, PG is also pulled low.

A 10kΩ to 100kΩ pull-up resistor connected to a voltage rail less than 5.5V is recommended for PG. An option is using the output voltage for PG pull-up. The state of PG is valid only if the  $V_{IN} > 1.8V$ . The current sinking capability of PG is limited until  $V_{IN}$  exceeds the 4.5V at which the full sinking capacity is available.

### Frequency and Synchronization (RT/CLK)

The device can operate in two modes to adjust switching frequency.

In the RT mode, a resistor (R<sub>RT</sub>) is placed between the RT/CLK and GND pins to set the free running switching frequency of the PLL.

In the CLK mode, an external clock drives the RT/CLK pin and the internal switching clock oscillator is synchronized to CLK by the PLL. The CLK mode overrides the RT mode. The device automatically detects the input clock and switches to the CLK mode.

### Constant Frequency PWM

The SGM61163 operates at fixed frequency that can be set by an external resistor or synchronized by external clock.

It is based on peak current control mode architecture. The high-side MOSFET is turned on until the sensing current ramp signal reaches the COMP voltage determined by the EA. If the switch current does not reach the reference value that generates from the COMP voltage at the end of a cycle, the high-side switch remains on for the next cycle until the current meets the reference value. A slope compensation block slightly reduces the sensed high-side switch current before comparison (depending on the on-time) to avoid sub-harmonic oscillations.

### Continuous Current Mode (CCM) Operation

In most load conditions, the device operates in continuous conduction mode (CCM) (forced PWM). For light loads, the inductor current can be negative when the low-side switch is on. However, if the current reaches the low-side sinking current limit, the low-side switch will be forced off.

## DETAILED DESCRIPTION (continued)

### Error Amplifier

The output voltage is sensed by a resistor divider through the FB pin and is compared with the internal reference. The error amplifier generates an output current that is proportional to the voltage difference (error), and the transconductance is  $1450\mu\text{A}/\text{V}$ . The generated current is then fed into the external compensation network to generate the voltage on the COMP pin, which sets the reference value for the peak current that controls the on-time of the power MOSFET. COMP is pulled down to the ground when the device shuts down.

### Slope Compensation

To avoid sub-harmonic oscillations that result in unstable PWM pulses, a small negative-slope compensating ramp is added to the measured switch current before it is used to generate the PWM signal. The slope compensation has no influence on the peak current limit which is maintained over full range of duty cycle.

### Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. Usually an OVP occurs after removal of an overload condition. When the output voltage is dropped due to a persisting overload, the error amplifier output reaches to its maximum and forces the converter to provide the maximum output current. Upon removal of the overload condition, the regulator output rises quickly because the high inductor current charges the output capacitor rapidly, especially if  $C_{\text{OUT}}$  is small. The error amplifier will respond and re-adjust itself but not as fast as the output filter (LC) and an overshoot occurs.

To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. If the threshold is exceeded, the high-side MOSFET is turned off to stop feeding current to the output. When the FB voltage drops below the OVP threshold, the high-side MOSFET can turn on again in the next cycle.

### Over-Current Protection

Both high-side (HS) and low-side (LS) switches are protected from over-current with cycle-by-cycle current limiting as will be explained in the next two sections.

### High-side Switch Over-Current Protection

Using current mode control, the pulse width (from the beginning of the cycle until HS turn-off) is determined by the compensator output voltage ( $V_{\text{COMP}}$  at COMP pin) in a cycle-by-cycle basis. In each cycle the high-side switch current is continuously compared with the current set point determined by compensator output ( $V_{\text{COMP}}$ ) and when the high-side current reaches to that reference (peak current), the high-side switch is turned off.

### Low-side MOSFET Over-Current Protection

The current of the low-side switch is continuously monitored while it is turned on. Normally, the low-side switch sources current from ground to the load through the inductor. Before the beginning of a new cycle, the low-side current is compared to its current limit which is normally lower than the high-side current limit. Only when the low-side source current drops below its current limit, the high-side MOSFET will turn on again for the new cycle.

In some operating conditions, the low-side switch sinks current from the load to the ground. The low-side sinking current has a typical limit of 3.2A. If this limit is exceeded, the low-side switch will immediately turn off and both switches will not turn on until the end of the cycle.

### Thermal Shutdown

To protect the device from damage due to overheating, a thermal shutdown feature is implemented to disable the device when the die temperature exceeds  $+175^{\circ}\text{C}$  (TYP). A new power-up sequence is initiated automatically once the temperature falls below  $+160^{\circ}\text{C}$  ( $15^{\circ}\text{C}$  hysteresis, TYP).

## DETAILED DESCRIPTION (continued)

## Small Signal Model

## Feedback Loop Small Signal Model

The equivalent small signal model of the control loop for frequency response and transient analysis is given in Figure 6.

The compensation network ( $R_3$ ,  $C_1$  and  $C_2$ ) is placed in the output of the transconductance error amplifier (EA). The EA can be simplified as an ideal voltage controlled current source with  $1450\mu\text{A}/\text{V}$  gain. The  $R_{\text{OEA}}$  ( $7.14\text{M}\Omega$ ) and  $C_{\text{OEA}}$  ( $20.7\text{pF}$ ) model the frequency response of the EA. Power converter is modeled with a pure  $16\text{A}/\text{V}$  gain. The inductor dynamics is effectively removed in the cycle-by-cycle average small signal model, because with the current mode control the inductor average current is set by the compensator. The  $C_O$  and  $R_{\text{ESR}}$  model the output capacitance and its parasitic ESR. To measure the frequency response, the loop is broken at points 'a' and 'b' to insert a small signal (e.g.  $1\text{mV}$ ) AC source. For small signal frequency response analysis, the magnitude and phase versus frequency for the output to input transfer functions of each stage is plotted. The 'a/c' (power stage gain), 'c/b' (compensation gain) and 'a/b' (loop gain) voltage ratios are commonly used for the analysis. To simulate or test the response of the output to load steps in time domain (dynamic loop response), the load ( $R_L$ ) is replaced with a stepping current source with proper amplitude, repetition rate and rate of change ( $\text{A}/\mu\text{s}$ ) depending on the application. As a common example, stepping between 25% and 75% of the nominal load with  $\pm 1\text{A}/\mu\text{s}$  slew rate and repeating at  $1\text{kHz}$  or  $10\text{kHz}$ , can be used for testing and comparison of the power supply transient response to rapid load changes.

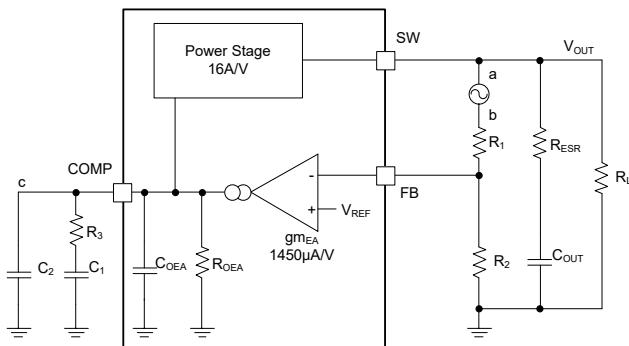


Figure 6. Small Signal Model for Loop Response

## Simplified Model for Peak Current Mode

A simplified small signal model to design the frequency compensation network is given in Figure 7. The power stage and duty cycle modulator are approximated by a voltage-controlled current source (VCCS) that is controlled by the error amplifier output ( $V_{\text{COMP}}$ ) and provides current to the output capacitor and the load. The control-to-output transfer function ( $V_{\text{OUT}}/V_{\text{COMP}}$ ) consists of a DC voltage gain ( $A_{\text{DC}}$ ), a dominant pole ( $f_p$ ) determined by  $R_L \times C_O$  time constant, and a simple ESR-zero ( $f_z$ ) determined by  $R_{\text{ESR}} \times C_O$  time constant as given in Equations 5, 6, 7 and 8. The VCCS transconductance is the ratio of the output current change to the control voltage (COMP) change. This is equivalent to the power stage transconductance ( $gm_{\text{PS}}$ ) that is  $16\text{A}/\text{V}$  for this device. As indicated in Equation 6, for resistive loads, the DC voltage gain ( $A_{\text{DC}}$ ) is equal to the power stage transconductance ( $gm_{\text{PS}}$ ) multiplied by the load resistance ( $R_L$ ). Therefore, the DC gain drops with the reduced load resistance. This relationship can be problematic because it could move the crossover frequency of the converter in the same way.

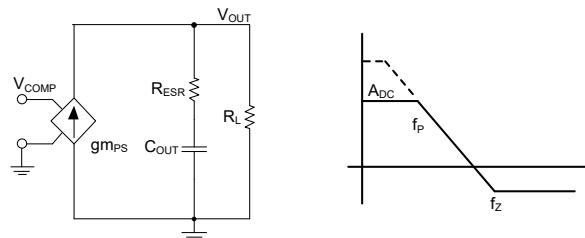


Figure 7. Simplified Model for Peak Current Mode Control and Frequency Response

$$\frac{V_{\text{OUT}} (\text{V})}{V_{\text{COMP}}} = A_{\text{DC}} \times \frac{\left(1 + \frac{s}{2\pi \times f_z}\right)}{\left(1 + \frac{s}{2\pi \times f_p}\right)} \quad (5)$$

$$A_{\text{DC}} = gm_{\text{PS}} \times R_L \quad (6)$$

$$f_p = \frac{1}{C_O \times R_L \times 2\pi} \quad (7)$$

$$f_z = \frac{1}{C_O \times R_{\text{ESR}} \times 2\pi} \quad (8)$$

where:

- $gm_{\text{PS}}$  is the gain of the power stage ( $16\text{A}/\text{V}$ ).
- $R_L$  is the load resistance.
- $C_O$  is the output capacitance.
- $R_{\text{ESR}}$  is the equivalent series resistance of the output capacitor.

## DETAILED DESCRIPTION (continued)

Fortunately, the dominant pole also moves with load current as given in Equation 7. As highlighted in Figure 7, the crossover frequency (0dB gain location) is not affected by the combined effect. As the load current decreases, the gain increases and the pole frequency decreases. Having a fixed crossover frequency simplifies the design of the frequency compensation for a changing load.

### Small Signal Model for Frequency Compensation

The SGM61163 can easily use the common Type 2 and 3 compensation circuits, as shown in Figure 8. Compared to Type 2B, the Type 2A compensation has an extra high-frequency pole (by  $C_2$ ) to attenuate high-frequency noise and ensure that gain remains very low at high frequencies against the ESR-zero effect that tends to increase the gain at higher frequencies. In the Type 3 compensation, the additional  $C_{10}$  capacitor is added in parallel to the upper feedback resistor divider for phase boost at the crossover frequency. An extra resistor may be used in series with  $C_{10}$  for more control on the phase boost. The following guidelines are provided for designers who prefer to compensate by the standard loop design method. These equations are only available for those applications where the ESR-zero is higher than the control loop bandwidth (crossover frequency). This condition is usually valid when ceramic output capacitors are used. For low frequency ESR-zeros (capacitors with high ESR) see the Application Information section for a step-by-step design procedure.

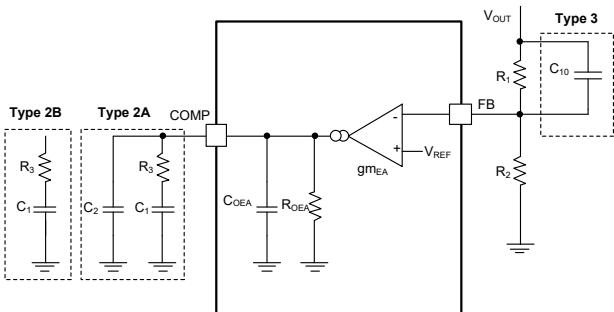


Figure 8. Types of Frequency Compensation

### General Guidelines for Loop Compensation Design

1. The first step is to determine the crossover frequency, which is normally set to 1/10th of the switching frequency.

$C_O$  is also initially chosen based on the switching frequency and ripple requirement.

2.  $R_3$  can be determined by:

$$R_3 = \frac{2\pi \times f_C \times V_{OUT} \times C_O}{gm_{EA} \times V_{REF} \times gm_{PS}} \quad (9)$$

where:

- $gm_{EA}$  is the gm amplifier gain ( $1450\mu A/V$ ).
- $gm_{PS}$  is the power stage gain ( $16A/V$ ).
- $V_{REF}$  is the reference voltage (0.6V).

3. A compensating zero should be placed at the dominated pole of the device, which is at  $f_P = \frac{1}{C_O \times R_L \times 2\pi}$ .  $C_1$  can be determined by:

$$C_1 = \frac{R_L \times C_O}{R_3} \quad (10)$$

4.  $C_2$  is optional and adds a high frequency pole to cancel the zero created by the output capacitor ESR.

$$C_2 = \frac{R_{ESR} \times C_O}{R_3} \quad (11)$$

5.  $C_{10}$  can be added for Type 3 compensation that allows a slightly higher bandwidth and better phase margin. If  $C_{10}$  is needed, use Equation 12.

$$C_{10} = \frac{1}{2\pi \times R_1 \times f_C} \quad (12)$$

## DETAILED DESCRIPTION (continued)

### Device Functional Modes

#### Switching Frequency Setting (RT Mode)

Selection of the switching frequency is generally a tradeoff between the solution size, efficiency, and the minimum controllable on-time. The RT resistance can be designed from Equation 13.

$$R_{RT} (\text{k}\Omega) = \frac{52407}{f_{SW} (\text{kHz})} - 5 \quad (13)$$

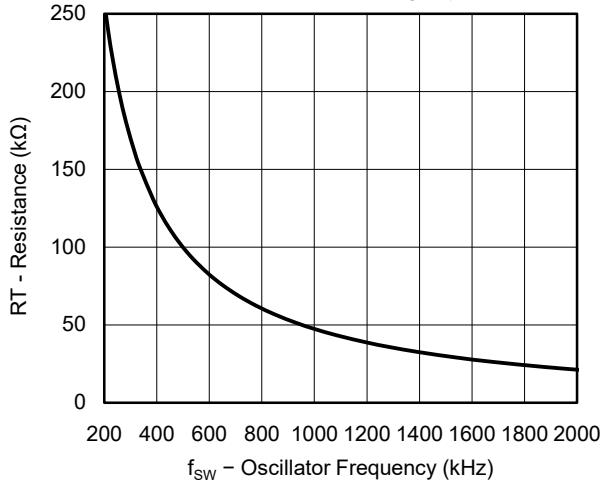


Figure 9. RT Resistance vs. Switching Frequency

#### Synchronization (CLK Mode)

The device uses an internal phase locked loop (PLL) to set or synchronize to an external clock signal with the 200kHz to 2000kHz range. Mode change from RT mode to CLK mode is allowed.

For stable synchronization, a square wave clock with 20% to 80% duty cycle must be applied to the RT/CLK pin. The logic low and high levels of the clock must be below 0.8V and above 2.0V respectively. The switching cycle starts with the falling edge of the RT/CLK signal.

If both RT and CLK modes are needed in an application, configuration shown in Figure 10 can be used. The RT mode can be overridden by CLK mode when both  $R_{RT}$  and clock are present. Mode switch occurs when the RT/CLK is pulled above 2.0V for the first time. Once CLK mode is selected, the PLL is locked to external CLK and the RT/CLK pin shifts to a high-impedance state. Going back from CLK mode to RT mode is not recommended because by removing clock, the switching frequency drops to around 100kHz first (waiting for synchronize clock) before recovery to the free running frequency that is set by RT resistor.

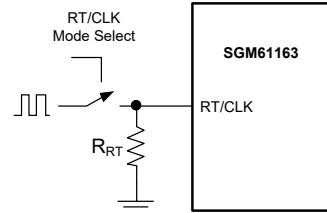


Figure 10. Using RT and CLK Modes Together

#### Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle)

An integrated bootstrap regulator is used for powering the high-side MOSFET gate driver. A small 0.1μF ceramic capacitor (X5R or X7R grade) with at least 10V rating is required between the BOOT and SW pins to supply the gate driver. It is recharged from VIN source through an internal switch every time the SW goes low. Recharge happens when the BOOT pin voltage is less than  $V_{IN}$  and the BOOT-SW voltage is below the required regulation for the high-side gate voltage.

The SGM61163 has no minimum off-time. It can operate at 100% duty cycle as long as the BOOT-SW voltage is higher than its UVLO threshold (2.5V TYP). If the BOOT-SW voltage drops below its UVLO threshold, the high-side switch turns off and the low-side switch turns on to recharge the boot capacitor. If the input voltage rails are split (separate VIN and PVIN sources), the 100% duty cycle operation can be achieved continuously, as long as  $V_{IN}$  is at least 4V above  $V_{PVIN}$ .

#### Startup Sequencing (SS/TR)

The SS/TR, EN and PG pins allow the implementation of common power supply sequencing methods. A simple sequencing approach is shown in Figure 11 in which the right side SGM61163 device is powered up after the left one. The PG of the first device is coupled to the EN pin of the second. The second power supply is enabled after the primary supply reaches regulation.

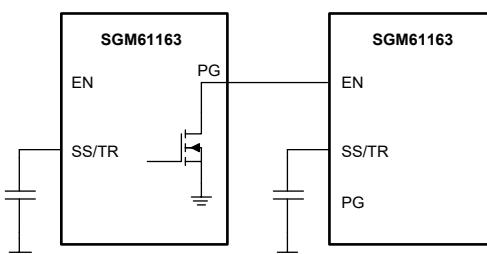


Figure 11. Sequential Startup Sequence

## DETAILED DESCRIPTION (continued)

Figure 12 shows the ratiometric sequencing of two converters. The SS/TR and EN inputs of the two devices are tied together. In this configuration, the  $I_{SS}$  current sources from the SS/TR pins are added together and  $2 \times I_{SS}$  should be considered to calculate the soft-start capacitor from Equation 3.

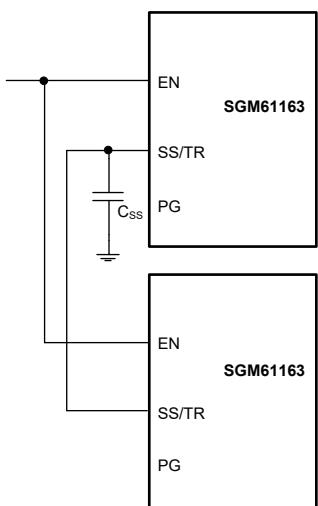


Figure 12. Ratiometric Sequencing of Two Devices

Simultaneous ratiometric sequencing can also be implemented by using a resistor divider as shown in Figure 13 by  $R_{SS1}$  and  $R_{SS2}$ .

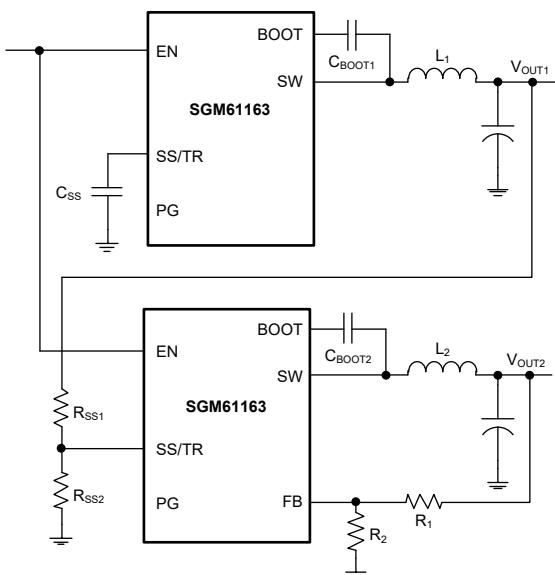


Figure 13. Ratiometric and Simultaneous Startup Sequence

In this example, the second power supply output ( $V_{OUT2}$ ) tracks  $V_{OUT1}$  (the output of the first power supply).

By proper selection of  $R_{SS1}$  and  $R_{SS2}$ ,  $V_{OUT2}$  can ramp up and reach regulation with the same rate, or a little bit faster or slower than  $V_{OUT1}$ . Note that  $V_{OUT2}$  is tracking  $V_{OUT1}$  and reaches regulation first. Equations 14 and 15 can be used to calculate the tracking resistors.  $\Delta V$  is the desired  $V_{OUT1} - V_{OUT2}$  difference when  $V_{OUT2}$  reaches regulation.  $\Delta V$  will be positive when  $V_{OUT1}$  change rate is higher than  $V_{OUT2}$  startup rate. It will be negative if  $V_{OUT2}$  rate is faster. With simultaneous sequencing,  $\Delta V$  is zero. To assure the proper device operation, make sure that the selected  $R_{SS1}$  is larger than the value given in Equation 17.

$$R_{SS1} = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSOFFSET}}{I_{SS}} \quad (14)$$

$$R_{SS2} = \frac{V_{REF} \times R_1}{V_{OUT2} + \Delta V - V_{REF}} \quad (15)$$

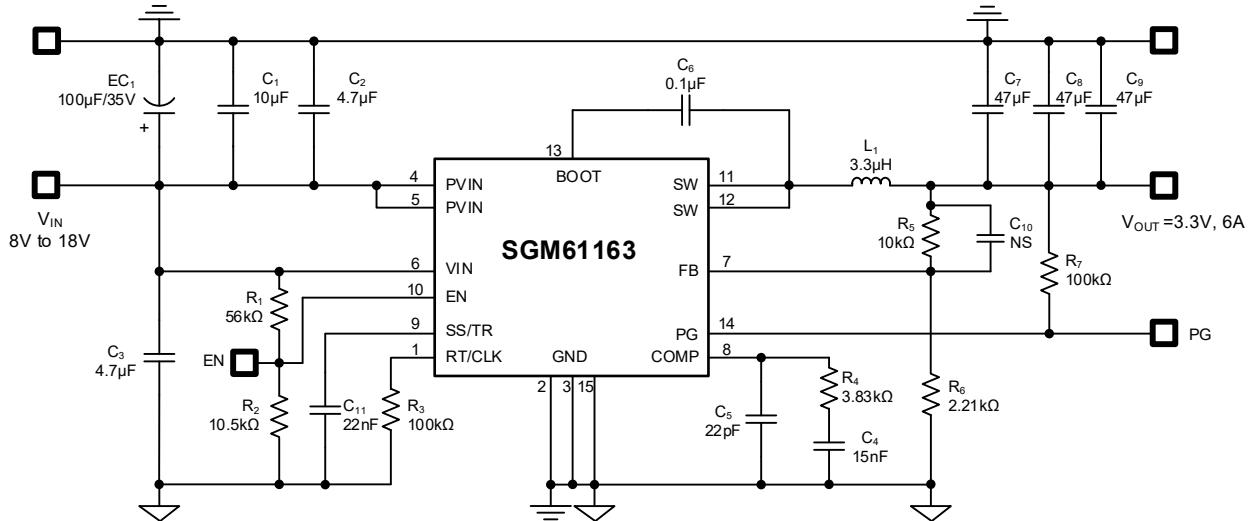
$$\Delta V = V_{OUT1} - V_{OUT2} \quad (16)$$

$$R_{SS1} > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (17)$$

The  $V_{SSOFFSET}$  is the inherent SS/TR to FB offset of the device (35mV TYP) and  $I_{SS}$  is the pull-up current source (2μA).

**APPLICATION INFORMATION****Typical Application**

The schematic of a typical application circuit that is used for SGM61163 evaluation module is given in Figure 14.



Note: EC<sub>1</sub> is optional. If VIN pin is more than 200mm far from the PVIN of SGM61163, or the VIN pin is not connected with the PVIN of SGM61163, or the input voltage is on/off by air-break switch, EC<sub>1</sub> should be installed. Otherwise, the spike voltage over 20V at the input side is caused, which will damage SGM61163.

**Figure 14. SGM61163 Typical Application Circuit**

**Design Requirements**

In this example, a high frequency regulator with ceramic output capacitors will be designed using SGM61163 and the details will be reviewed. The design requirements are typically determined at the system level. In this example, the known parameters are summarized in Table 1.

**Table 1. Design Parameters**

Design Parameter	Example Value
Output Voltage	3.3V
Maximum Output Current	6A
Transient Response to 3A Load Step	$\Delta V_{OUT} = 5\%$
Input Voltage Range	12V nominal, 8V to 18V
Maximum Output Voltage Ripple	33mV <sub>P-P</sub>
Input Turn-On Voltage (VIN Rising)	7.5V
Input Turn-Off Voltage (VIN Falling)	7.0V
Switching Frequency (f <sub>sw</sub> )	480kHz

**Operating Frequency**

Usually the first parameter to design is the switching frequency ( $f_{sw}$ ). Higher switching frequencies allow smaller solution size and smaller filter inductors and capacitors and the bandwidth of the converter can be increased for faster response. It is also easier to filter noises because they also shift to higher frequencies. The drawbacks are increased switching and gate driving losses that result in lower efficiency and tighter thermal limits. Also the duty cycle range and Buck ratio will be limited due to the minimum on-time and/or off-time limits of the converter. In this design,  $f_{sw} = 480\text{kHz}$  is chosen as a tradeoff. From Equation 13 the nearest standard resistor for this frequency is  $R_3 = 100\text{k}\Omega$ .

## APPLICATION INFORMATION (continued)

### Inductor Design

Equation 18 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple ( $\Delta I_L$ ) to the maximum output current ( $I_{OUT}$ ) is represented as  $K_{IND}$  factor ( $\Delta I_L/I_{OUT}$ ). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current ( $I_{OUT} + \Delta I_L/2$ ) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. During power-up with large output capacitor, over-current, output shorted or load transient conditions, the actual peak current of inductor can be greater than  $I_{L\_PEAK}$  calculated in Equation 21. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor.  $C_{OUT}$  RMS current rating must be higher than the inductor RMS ripple. Typically, a 10% to 30% ripple is selected ( $K_{IND} = 0.1 \sim 0.3$ ). Choosing a higher  $K_{IND}$  value reduces the selected inductance.

$$L_1 = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (18)$$

In this example,  $K_{IND} = 0.3$  is chosen and the inductance is calculated to be  $3.12\mu H$ . The nearest standard value is  $3.3\mu H$ . The ripple, RMS and peak inductors current calculations are summarized in Equations 19, 20 and 21 respectively.

$$I_{RIPPLE} = \frac{V_{INMAX} - V_{OUT}}{L_1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (19)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left[ \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times L_1 \times f_{SW}} \right]^2} \quad (20)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (21)$$

For this example, the ripple, RMS, and peak inductor current are calculated as 1.70A, 6.02A and 6.85A respectively. A  $3.3\mu H$  inductor from Coilcraft MSS1048

series with 7.38A saturation and 7.22A RMS current ratings is selected for  $L_1$ .

### Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor ( $C_{OUT}$ ): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of  $V_{OUT}$  in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 22 can be used to calculate the minimum output capacitance that is needed to supply or absorb a current step ( $\Delta I_{OUT}$ ) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of  $\Delta V_{OUT}$  (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (22)$$

where:

- $\Delta I_{OUT}$  is the change in output current.
- $f_{SW}$  is the regulator's switching frequency.
- $\Delta V_{OUT}$  is the allowable change in the output voltage.

For example, if the acceptable transient to a 3A load step is 5%, by inserting  $\Delta V_{OUT} = 0.05 \times 3.3V = 0.165V$  and  $\Delta I_{OUT} = 3.0A$ , the minimum required capacitance will be  $75.8\mu F$ . Generally, the ESR of ceramic capacitors is small enough. The impact of output capacitor ESR on the transient is not taken into account in Equation 22.

## APPLICATION INFORMATION (continued)

Equation 23 can be used for the output ripple criteria and finding the minimum output capacitance needed.  $V_{ORIPPLE}$  is the maximum acceptable ripple. In this example, the allowed ripple is 33mV that results in minimum capacitance of 13.43 $\mu$ F.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \quad (23)$$

where:

- $V_{ORIPPLE}$  is the maximum allowable output voltage ripple.
- $I_{RIPPLE}$  is the inductor ripple current.

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 23. Use Equation 24 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement. In this example, the ESR must be less than 33mV/1.70A = 19.4m $\Omega$ .

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \quad (24)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a  $3 \times 47\mu$ F/10V X5R ceramic capacitor with 3m $\Omega$  of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 25 calculates the RMS current that the output capacitor must support. In this example, it is 491mA.

$$I_{CORMS} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{\sqrt{12} \times V_{INMAX} \times L_1 \times f_{SW}} \quad (25)$$

### Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61163. At least 4.7 $\mu$ F of effective capacitance (after deratings) is needed on the PVIN input and similar amount is also needed for the  $V_{IN}$  pin. If input power is far away from the device, additional bulk capacitor is recommended in parallel to stabilize input voltage. The RMS value of input capacitor can be calculated from Equation 26 and the maximum  $I_{CIRMS}$  occurs at 50% duty cycle. For this example, the maximum input RMS current is 2.95A. The ripple

current rating of input capacitor should be greater than  $I_{CIRMS}$ .

$$I_{CIRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{INMIN} - V_{OUT})}{V_{INMIN} \times V_{INMIN}}} \quad (26)$$

In this example, the voltage rating of capacitor should have a safe margin from maximum input voltage. Therefore, one 10 $\mu$ F and one 4.7 $\mu$ F/25V capacitors in parallel are selected for PVIN to cover all DC bias, thermal and aging deratings, and a 4.7 $\mu$ F/25V X5R capacitor is selected for  $V_{IN}$ . They are placed in parallel because the  $V_{IN}$  and PVIN inputs are tied together to operate from a single supply in this design.

The input voltage ripple can be calculated from Equation 27, the maximum ripple occurs at 50% duty cycle. In this example, the input voltage ripple is 213mV.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (27)$$

### Soft-Start Capacitor

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. The ramp is needed in many applications due to limited voltage slew rate required by the load or limited available input current to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 28 (with  $I_{SS} = 2\mu$ A and  $V_{REF} = 0.6V$ ) can be used to calculate the soft-start capacitor for a required soft-start time ( $t_{SS}$ ). In this example, the output capacitor value is relatively small (47 $\mu$ F) and the soft-start time is not critical because it does not require too much charge for 3.3V output voltage. However, it is better to set a small arbitrary value, like  $C_{SS} = 22n$ F that results in 6.6ms startup time.

$$C_{SS} (\text{nF}) = \frac{t_{SS} (\text{ms}) \times I_{SS} (\mu\text{A})}{V_{REF} (\text{V})} \quad (28)$$

### Bootstrap Capacitor Selection

A 0.1 $\mu$ F ceramic capacitor with 10V or higher voltage rating must be connected between the BOOT-SW pin. X5R or better dielectric types are recommended.

## APPLICATION INFORMATION (continued)

### UVLO Setting

The under-voltage lockout (UVLO) can be programmed from VIN or PVIN by an external voltage divider network. In this design, the turn-on (enable to start switching) occurs when VIN rises above 7.5V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 7.0V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are  $R_1 = 56\text{k}\Omega$  and  $R_2 = 10.5\text{k}\Omega$ .

### Feedback Resistors

Choosing a 10k $\Omega$  value for the upper resistor ( $R_5$ ), the lower resistor ( $R_6$ ) can be calculated from Equation 29. The nearest 1% resistor for the calculated value (2.222k $\Omega$ ) is 2.21k $\Omega$ . For higher output accuracy, choose resistors with better tolerance (0.5% or better).

$$R_6 = \frac{V_{\text{REF}}}{V_{\text{OUT}} - V_{\text{REF}}} \times R_5 \quad (29)$$

### Minimum Output Voltage

There is a minimum output voltage limit for any given input voltage due to the limited minimum switching on-time of the device. Above the 0.6V minimum possible output, the lowest achievable voltage is given by Equation 30.

$$V_{\text{OUTMIN}} = t_{\text{ONMIN}} \times f_{\text{SWMAX}} (V_{\text{INMAX}} + I_{\text{OUTMIN}} (R_{\text{DSON\_HMIN}} - R_{\text{DSON\_LMIN}})) - I_{\text{OUTMIN}} (R_L + R_{\text{DSON\_HMIN}}) \quad (30)$$

where:

- $V_{\text{OUTMIN}}$  = Minimum achievable output voltage.
- $t_{\text{ONMIN}}$  = Minimum controllable on-time (135ns MAX).
- $f_{\text{SWMAX}}$  = Maximum  $f_{\text{sw}}$  (including tolerance).
- $V_{\text{INMAX}}$  = Maximum input voltage.
- $I_{\text{OUTMIN}}$  = Minimum load current.
- $R_{\text{DSON\_HMIN}}$  = Minimum high-side switch  $R_{\text{DSON}}$  (27m $\Omega$  to 29m $\Omega$  TYP).
- $R_{\text{DSON\_LMIN}}$  = Minimum low-side switch  $R_{\text{DSON}}$  (18m $\Omega$  TYP).
- $R_L$  = Output Inductor series resistance.

### Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. The recommended calculation method here is quite simple and yields results with high phase margins. In this method the effects of the slope compensation are ignored.

Because of this approximation, the actual cross over frequency is usually lower than the calculated value.

First, the converter pole ( $f_p$ ) and ESR-zero ( $f_z$ ) are calculated from Equations 31 and 32. For  $C_{\text{OUT}}$ , the worst derated value of 78.96 $\mu\text{F}$  should be used. Equations 33 and 34 can be used to find an estimation for closed-loop crossover frequency ( $f_{\text{co}}$ ) as a starting point (choose the lower value).

$$f_p = \frac{I_{\text{OUT}}}{2\pi \times V_{\text{OUT}} \times C_{\text{OUT}}} \quad (31)$$

$$f_z = \frac{1}{2\pi \times R_{\text{ESR}} \times C_{\text{OUT}}} \quad (32)$$

$$f_{\text{co}} = \sqrt{f_p \times f_z} \quad (33)$$

$$f_{\text{co}} = \sqrt{f_p \times \frac{f_{\text{sw}}}{2}} \quad (34)$$

For this design,  $f_p = 3.66\text{kHz}$  and  $f_z = 2.01\text{MHz}$ . Equation 33 yields 85.8kHz for crossover frequency and Equation 34 gives 29.6kHz. The lower value is 29.6kHz, a slightly higher frequency of 31.5kHz is selected for the influence of slope compensation in the actual circuit.

Having the crossover frequency, the compensation network ( $R_4$  and  $C_4$ ) can be calculated.  $R_4$  sets the gain of the compensated network at the crossover frequency and can be calculated by Equation 35.

$$R_4 = \frac{2\pi \times f_{\text{co}} \times V_{\text{OUT}} \times C_{\text{OUT}}}{g_{\text{mEA}} \times V_{\text{REF}} \times g_{\text{mPS}}} \quad (35)$$

$C_4$  sets the location of the compensation zero along with  $R_4$ . To place this zero on the converter pole, use Equation 36.

$$C_4 = \frac{V_{\text{OUT}} \times C_{\text{OUT}}}{I_{\text{OUT}} \times R_4} \quad (36)$$

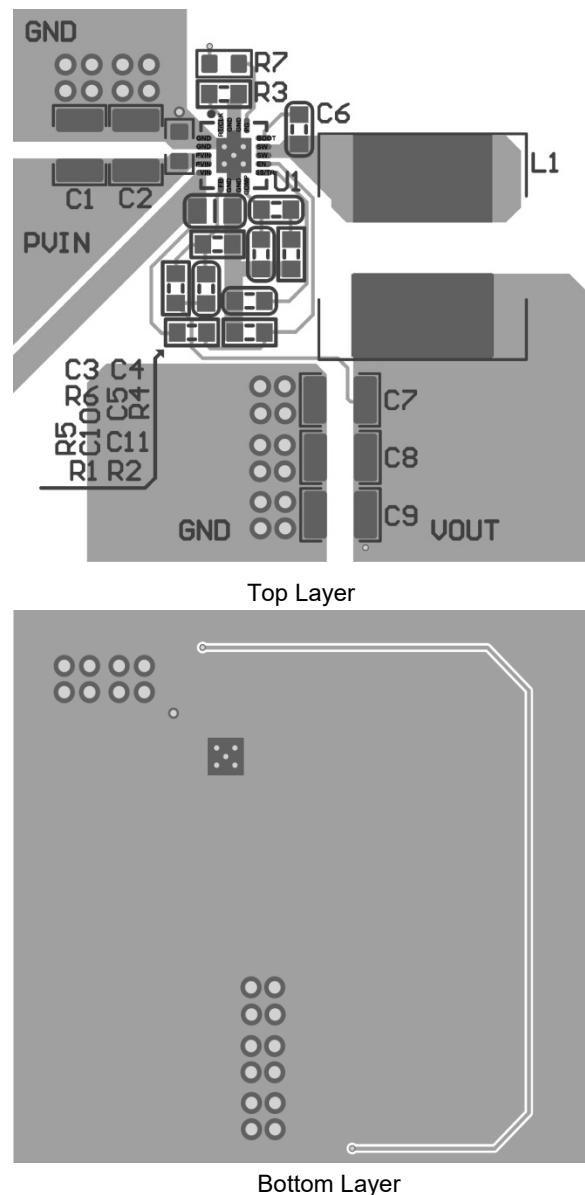
From Equations 35 and 36 the standard selected values are  $R_4 = 3.83\text{k}\Omega$  and  $C_4 = 15\text{nF}$ .

A high frequency pole can also be added by a parallel capacitor if needed (not used in this example). The pole frequency can be calculated from Equation 37.

$$f_p = \frac{1}{2\pi \times R_4 \times C_5} \quad (37)$$

**APPLICATION INFORMATION (continued)****Layout Guidelines**

- PCB layout is critical for stable and high-performance converter operation. The recommended layout is shown in Figure 15.
- Place the nearest input high frequency decoupling capacitor between VIN and AGND pins as close as possible.
- Place a larger input ceramic capacitor close to PVIN and GND pins for minimizing the influence of ground bounce.
- Use short and wide trace to connect SW node to the inductor. Minimize the area of switching loop. Otherwise, large voltage spikes on the SW node and poor EMI performance are inevitable.
- Sensitive signals like FB, COMP, EN, RT/CLK traces must be placed away from high dv/dt nodes (such as SW) and not inside any high di/dt loop (like capacitor or switch loops). The ground of these signals should be connected to GND pin and separated with power ground.
- To improve the thermal relief, use a group of thermal vias under the exposed pad to transfer the heat to the ground planes in the opposite side of the PCB. Use small vias (approximately 15mil) such that they can be filled up during the reflow soldering process to provide a good metallic heat conduction path from the IC exposed pad to the other PCB side.
- Connect PVIN, GND and exposed pad pins to large copper areas to increase heat dissipation and long-term reliability. Keep SW area small to avoid emission issue.
- The dimension and outline information is for the standard TQFN-3.5×3.5-14L package.

**Figure 15. PCB Layout**

**REVISION HISTORY**

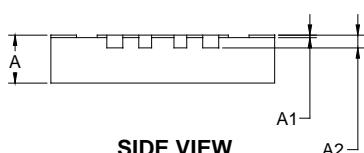
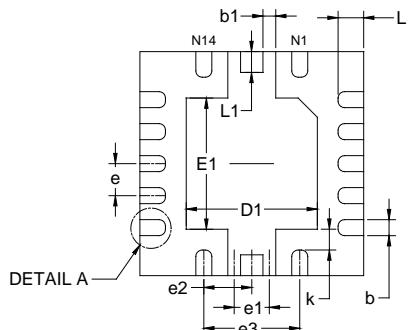
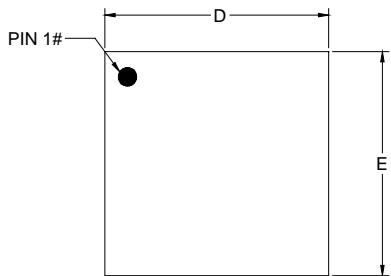
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

	Page
<b>APRIL 2022 – REV.A.2 to REV.A.3</b>	
Updated conditions in Electrical Characteristics section.....	4, 5
<b>NOVEMBER 2021 – REV.A.1 to REV.A.2</b>	
Added two values in Absolute Maximum Ratings section .....	2
Added a condition of VIN Shutdown Supply Current.....	4
Updated Detailed Description section .....	13, 14, 18
<b>NOVEMBER 2021 – REV.A to REV.A.1</b>	
Updated the fifth paragraph of Overview section .....	11
Updated Equation 12.....	16
<b>Changes from Original (SEPTEMBER 2021) to REV.A</b>	
Changed from product preview to production data.....	All

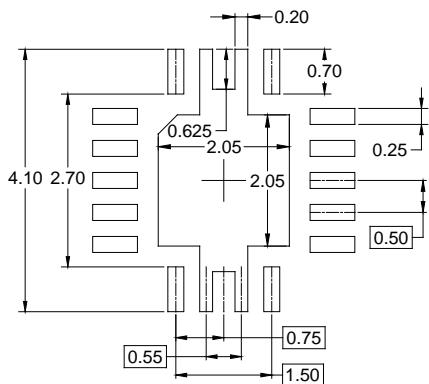
# PACKAGE INFORMATION

## PACKAGE OUTLINE DIMENSIONS

### TQFN-3.5x3.5-14L



ALTERNATE A-1  
 ALTERNATE A-2  
 DETAIL A  
 ALTERNATE TERMINAL CONSTRUCTION



RECOMMENDED LAND PATTERN (Unit: mm)

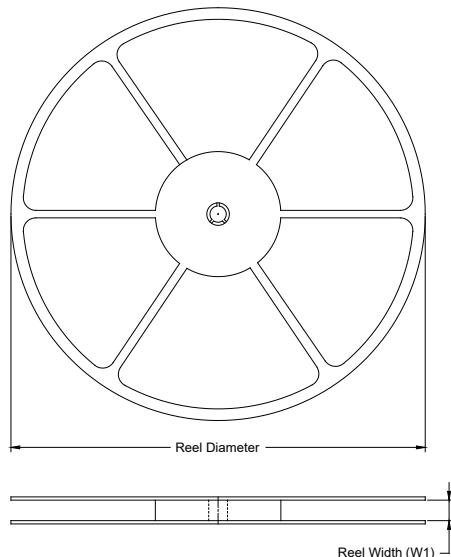
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
D	3.400	3.500	3.600
E	3.400	3.500	3.600
D1	1.950	2.050	2.150
E1	1.950	2.050	2.150
b	0.200	0.250	0.300
b1	0.150	0.200	0.250
e	0.500 BSC		
e1	0.550 BSC		
e2	0.750 BSC		
e3	1.500 BSC		
k	0.220	0.320	0.420
L	0.300	0.400	0.500
L1	0.225	0.325	0.425

NOTE: This drawing is subject to change without notice.

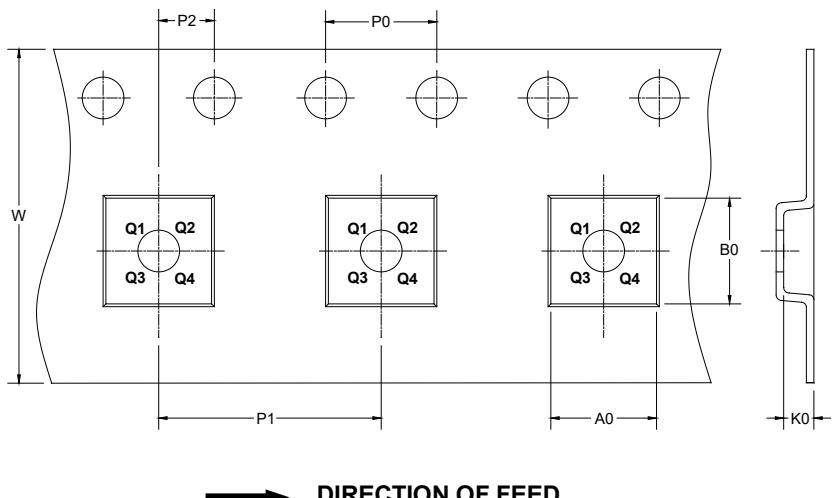
# PACKAGE INFORMATION

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

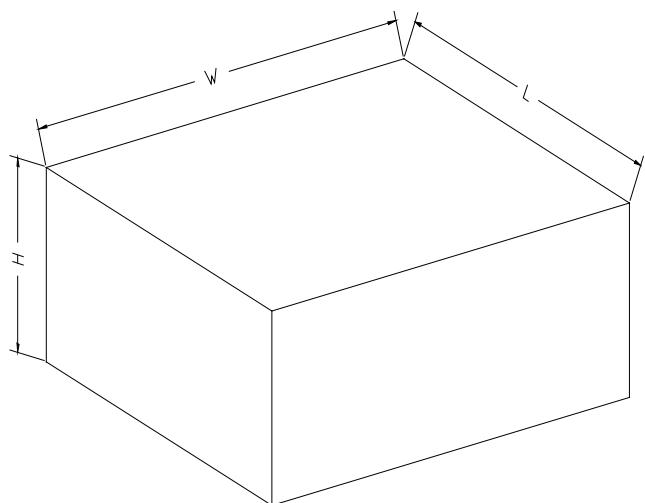
### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5x3.5-14L	13"	12.4	3.75	3.75	1.05	4.0	8.0	2.0	12.0	Q2

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## PACKAGE INFORMATION

### CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5