2.5V to 6V Input, 3A Step-Down Module Regulator

DESCRIPTION

The EZ8303 is a single 3A output switching mode DC/DC module regulator in an ultra-small 2.8mm x 3mm x 1.3mm package. Operating over a wide input voltage range of 2.5V to 6V, the EZ8303 supports an output range of 0.8V to V_{IN} set by external resistors. Included in the package are the switching controllers, power FETs and inductors. Only a few input and output capacitors are needed.

The EZ8303 features fast 2.4MHz internal switching frequency and a constant-on-time (COT) control architecture for fast transient response and easy loop compensation. Its 100% duty cycle operation delivers low drop out. An internal soft-start and power good indicator are incorporated to simply power supply rail sequencing. Fault protection includes a Hiccup mode short circuit protection, over-voltage and over-temperature shutdown protection.

FEATURES

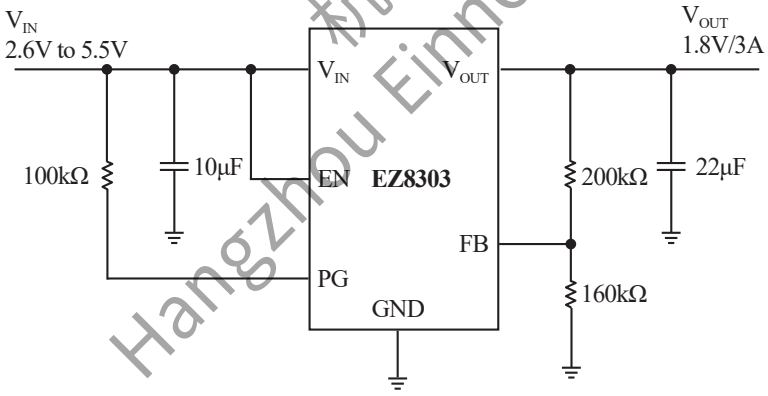
- Complete System-in-Package (SiP) Power Supply
- Input Voltage Range: 2.5V to 6V
- Output Voltage Range: 0.8V to V_{IN}
- ±1% Maximum Total DC Output Error over Line, Load and Temperature
- Low 23μA Quiescent Current
- Power Save Mode for Light Load Efficiency
- 2.4MHz Fast Switching Frequency
- Internal Soft-start and Power Good Indicator
- Hiccup Mode Short Circuit Protection
- Thermal Shutdown Protection
- Ultra-Small 2.8mm x 3mm x 1.3mm LQFN Package

APPLICATION

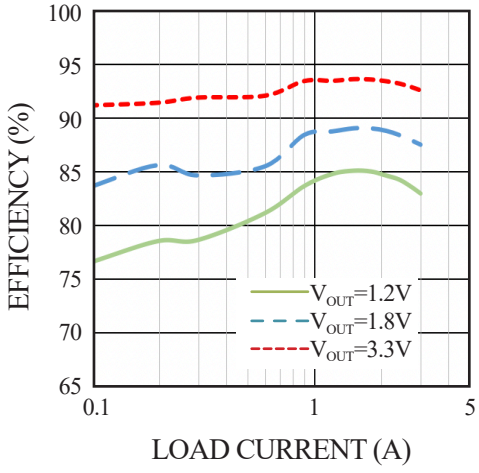
- Point-of-Load Application
- Telecom and Networking Application
- Battery Operated Application

TYPICAL APPLICATION

2.5V to 6V Input, 1.8V/3A Output DC/DC Regulator

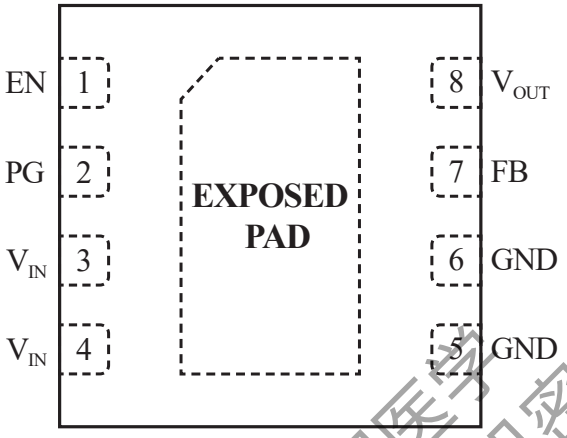


Efficiency at 5V Input Voltage



PIN CONFIGURATION AND FUNCTIONS

(TOP VIEW)



8-LEAD 2.8mm x 3mm x 1.3mm LQFN PACKAGE
T_{JMAX}=125°C, Θ_{JCtop}=TBD°C, $\Theta_{JCbottom}$=TBD°C, Θ_{JA}=TBD°C, Θ_{JB}=TBD°C
Θ value determined per JESD51-12, Weight=TBD g

PIN#	PIN Name	PIN Description
1	EN	Enable pin. Pull this pin above 1V to enable the device. This pin has an internal pull-down resistor of typically 400kΩ when the devices is disabled.
2	PG	Power Good Open Drain Output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
3,4	V_{IN}	Power Input Pin.
5,6	GND	Ground Pin.
7	FB	Feedback Reference Pin. An external resistor divider connected to this pin programs the output voltage.
8	V_{OUT}	Power Output Pin.
		The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKING MATERIAL	MSL	TEMPERATURE RANGE
EZ8303IV#PBF	Au(RoHS)	SD	LQFN	TRAY	3	-40°C to 125°C
EZ8303IV#TRPBF	Au(RoHS)	SD	LQFN	TAPE & REEL	3	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS

	MIN	TYP	MAX	UNIT
Terminal Voltage				
V_{IN}	-0.3		7	V
EN, PG, FB, V_{OUT}	-0.3		V_{IN}	
Temperatures				
Internal Operating Temperature Range	-40		125	°C
Storage Temperature Range	-55		150	°C
Peak Solder Reflow Package Body Temperature		260		°C
ESD Rating				
HBM (Human Body Model)				kV
CDM (Charged Device Model)				kV

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply over Full Operating Temperature Range (FTR) (Note 1), otherwise specifications are at T_A = 25°C, V_{IN} = V_{EN} = 3.3V per the typical application in Figure 4 unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
Input DC Voltage	V_{IN}		2.5		6	V	Y
Output Voltage Range	$V_{OUT(RANGE)}$	V_{IN} = 2.5V to 6V	0.8		V_{IN}	V	Y
Output Voltage, Total Variation with Line and Load	$V_{OUT(DC)}$	C_{IN} = 10uF, C_{OUT} = 47µF Ceramic R_{TOP} = 43.7k, R_{BOT} = 49.9k, V_{IN} = 2.5V to 6V, I_{OUT} = 0A to 3A	1.485	1.50	1.515	V	Y
EN Pin On Threshold	V_{EN}	V_{EN} Rising V_{EN} Falling	1.0		 0.4	V V	
Undervoltage Lockout	UVLO	V_{IN} Falling	2.1	2.2	2.3	V	
UVLO Hysteresis	UVLO_HYS			0.2		V	
Input Supply Bias Current	$I_{Q(VIN)}$	V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0 A Shutdown, V_{EN} = 0V		23 0.1		µA µA	

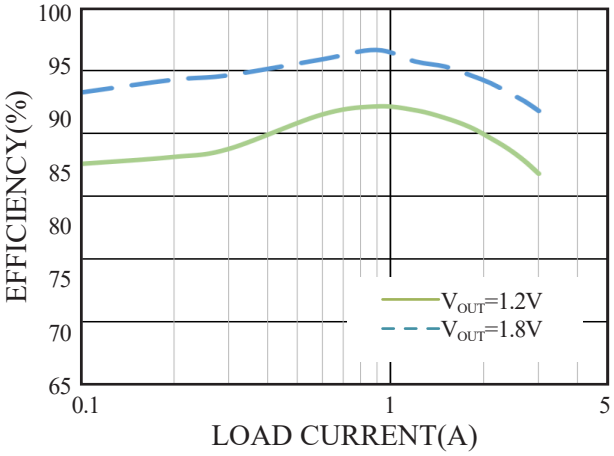
Input Supply Current	$I_{S(VIN)}$	V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 3A		1.6		A	
Output Continuous Current Range	$I_{OUT(DC)}$	V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 2)			3	A	
Line Regulation Accuracy	$\Delta V_{OUT(Line)}/V_{OUT}$	V_{OUT} = 1.5V, V_{IN} from 2.5V to 6V, I_{OUT} = 1A		0.02		%/V	Y
Load Regulation Accuracy	$\Delta V_{OUT(Load)}/V_{OUT}$	V_{OUT} = 1.5V, I_{OUT} = 0A to 3A		0.5	0.75	%	Y
Output Ripple Voltage	$V_{OUT(AC)}$	C_{OUT} = 47µF Ceramic V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0A		15		mV	
Turn-On Time	t_{START}	C_{OUT} = 47µF Ceramic V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0A		0.8		mS	
TOP FET Current Limit	I_{OUT_PK}	V_{IN} = 3.3V, V_{OUT} = 1.5V		5		A	
Bottom FET Current Limit	I_{OUT_VALLEY}	V_{IN} = 3.3V, V_{OUT} = 1.5V		4		A	
Voltage at FB Pin	V_{FB}	I_{OUT} = 1A, V_{OUT} = 1.5V	792	800	808	mV	Y
Current at FB Pin	I_{FB}			50		nA	
Output Discharge Resistor	R_{DIS}	V_{EN} = 0V		260		Ω	
PG Trip Level	V_{PG}	FB with Respect to Set Output Voltage FB Ramping Negative FB Ramping Positive	 88 93	 90 95	 93 98	 % %	
PG Leakage Current	I_{PG}	V_{PG} = 5V			1	µA	
PG Voltage Low	I_{PG_LOW}	I_{PG} = 2mA		0.02	0.1	V	
Switching Frequency	f_{SW}			2.4		MHz	

Note 1: The EZ8303 is tested under pulsed load conditions such that $T_J \approx T_A$. The EZ8303IV is guaranteed over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

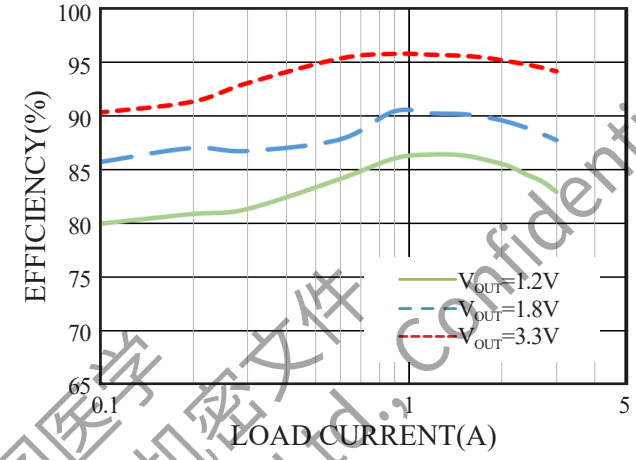
Note 2: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

ELECTRICAL CHARACTERISTICS

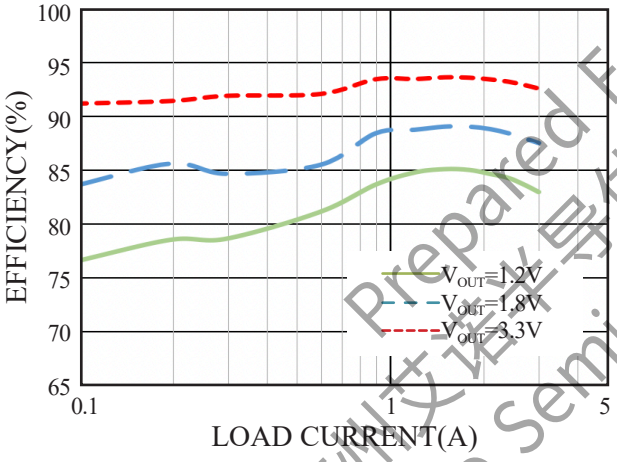
Efficiency vs Load Current From 3V Input



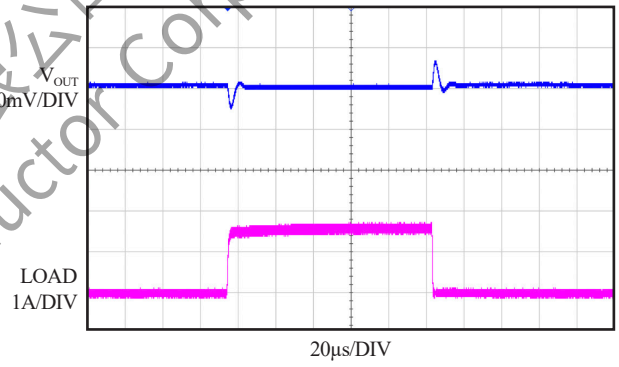
Efficiency vs Load Current From 4V Input



Efficiency vs Load Current From 5V Input

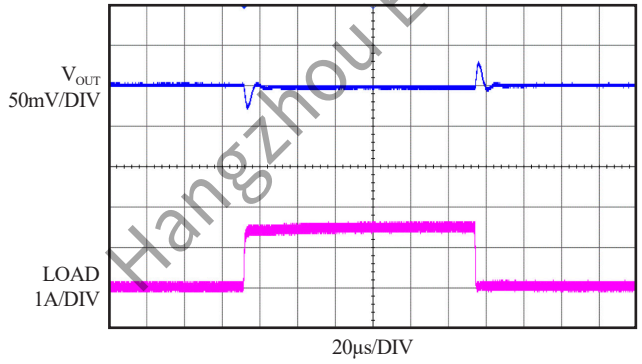


1.0V Output Transient Response



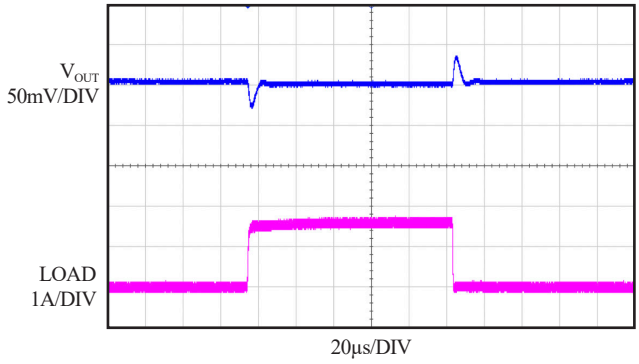
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=1.0V
C_{OUT}=22uF×2 CERAMIC CAP

1.2V Output Transient Response



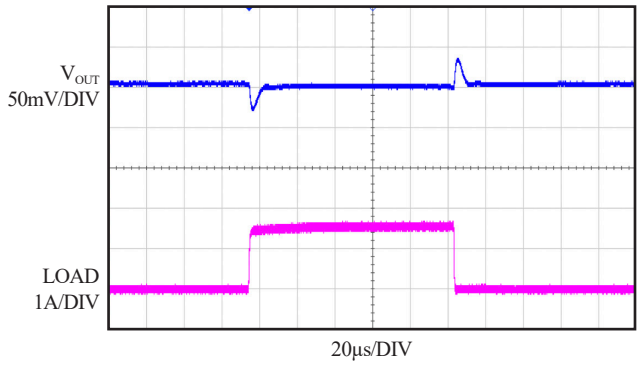
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=1.2V
C_{OUT}=22uF×2 CERAMIC CAP

1.5V Output Transient Response



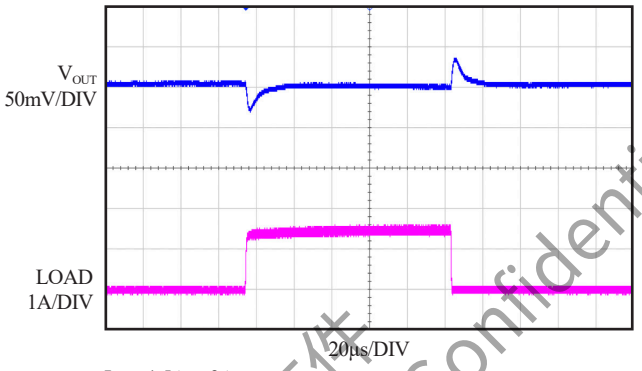
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=1.5V
C_{OUT}=22uF×2 CERAMIC CAP

1.8V Output Transient Response



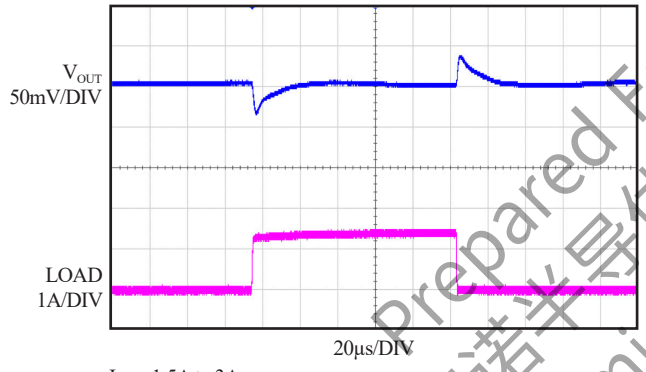
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=1.8V
C_{OUT}=22uF×2 CERAMIC CAP

2.5V Output Transient Response



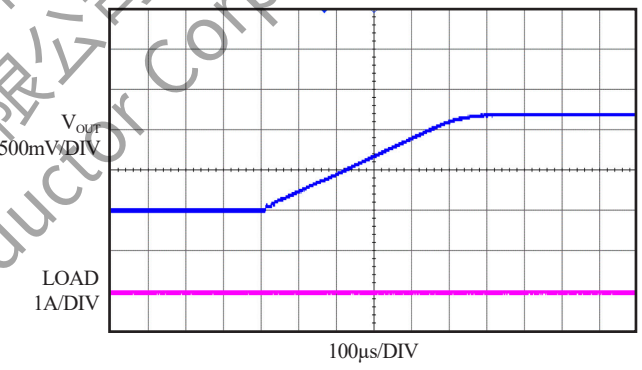
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=2.5V
C_{OUT}=22uF×2 CERAMIC CAP

3.3V Output Transient Response



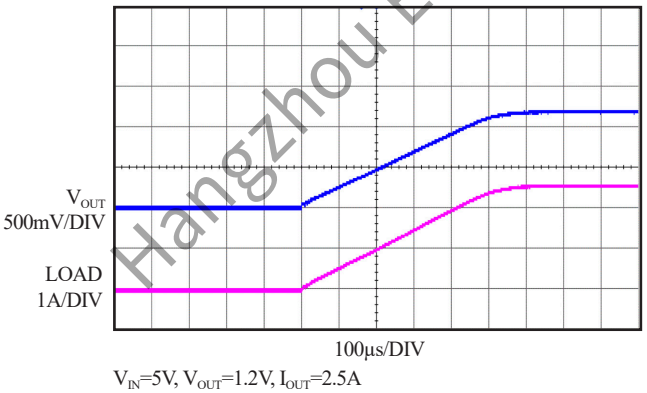
I_{OUT}=1.5A to 3A
V_{IN}=5V, V_{OUT}=3.3V
C_{OUT}=22uF×2 CERAMIC CAP

Start-Up with No Load Current



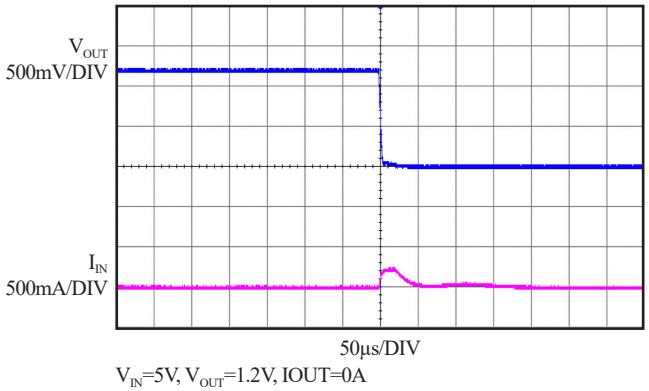
V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A
C_{OUT}=22uF×2 CERAMIC CAP
USE EN PIN CONTROL START-UP

Start-Up with 2.5A Load Current



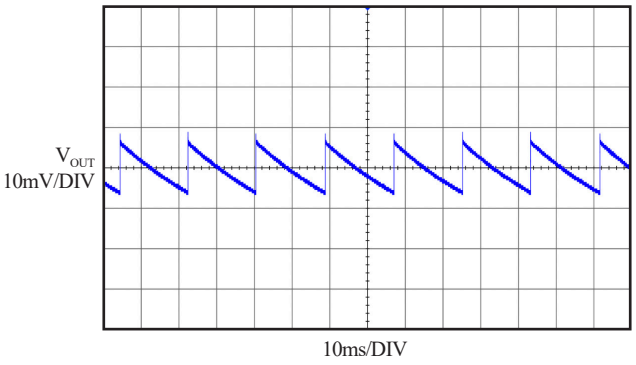
V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=2.5A
C_{OUT}=22uF×2 CERAMIC CAP
USE EN PIN CONTROL START-UP

Short Circuit Protection



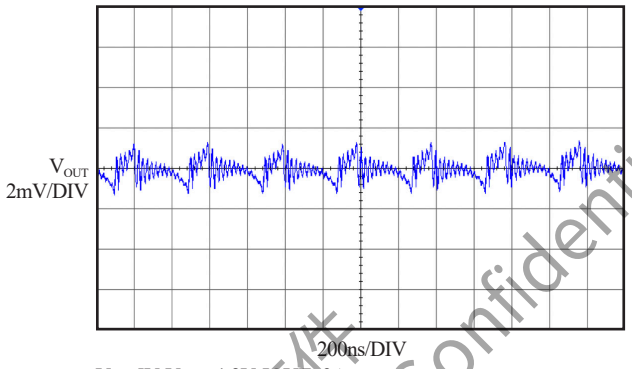
V_{IN}=5V, V_{OUT}=1.2V, IOUT=0A
C_{OUT}=22uF×2 CERAMIC CAP

Output Ripple at No Load (PFM)



V_{IN}=5V, V_{OUT}=1.2V, IOUT=0A
C_{OUT}=22uF×2 CERAMIC CAP

Output Ripple at 3A Load (CCM)



V_{IN}=5V, V_{OUT}=1.2V, IOUT=3A
C_{OUT}=22uF×2 CERAMIC CAP

BLOCK DIAGRAM

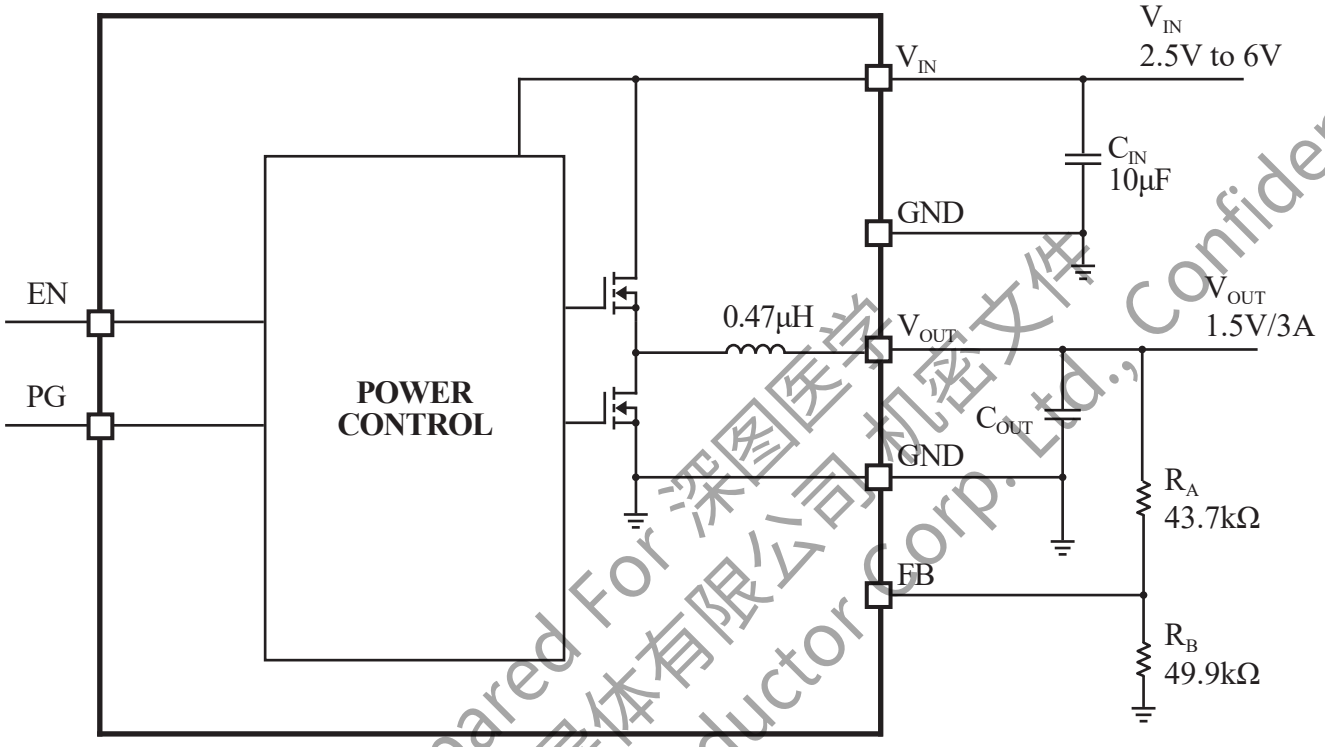


Figure 1 Simplified EZ8303 Internal Function Block Diagram

OPERATION

POWER MODULE DESCRIPTION

The EZ8303 SiP Power Module is a high-performance single output standalone non-isolated switching mode DC/DC power supply. It can provide a single 3A output with a few external input and output capacitors. This module provides a precisely regulated output voltage programmable via an external resistor divider from 0.8V to V_{IN}. The typical application schematic is shown in Figure 4.

The EZ8303 SiP Power Module has an integrated constant on-time (COT) regulator and built-in power MOSFETs, and power inductors. The typical switching frequency is 2.4MHz. See the Applications Information section.

During a load transient event, with the help of COT control architecture, the EZ8303 SiP Power Module can turn on its high-side power switch immediately to achieve a very good transient performance with sufficient stability margins over a wide range of output capacitors, even with all ceramic output capacitors.

Pulling the EN pin below 0.4V forces the regulator into a shutdown state. Pulling the EN pin above 1.0V to enable the EZ8303. The internal soft-start is used for programming the output voltage soft-start ramp during the start-up. See the Application Information section.

High efficiency at light loads is accomplished with Pulse Frequency Modulation (PFM) operation.

APPLICATIONS INFORMATION

The typical EZ8303 application circuit is shown in Figure 4. External component selection is primarily determined by the maximum load current and output voltage.

OUTPUT VOLTAGE PROGRAMMING

The EZ8303 has an internal 0.8V reference voltage. The output voltage is set by the two resistors between the FB pin and V_{OUT}. The output voltage can be calculated by the function:

$$V_{OUT} = 0.8V \cdot (1 + \frac{R_A}{R_B})$$

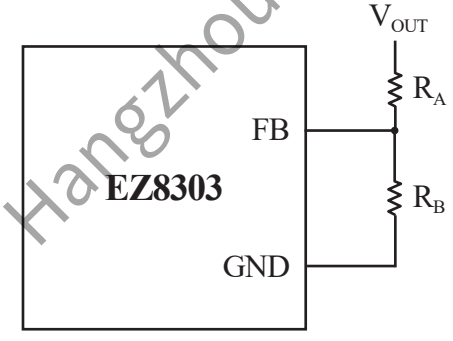


Figure 2 Output Voltage Programming Diagram

INPUT CAPACITORS

The EZ8303 SiP Power Module should be connected to a low AC-impedance DC source. Also input ceramic capacitors are needed for the RMS input ripple current rating. A typical 10μF ceramics capacitor is a good choice with RMS ripple current ratings of ~1A.

A 47uF to 100μF aluminum electrolytic bulk capacitor can be added only if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \times \sqrt{D \times (1 - D)}$$

In the previous equation, η% is the estimated efficiency of the power module.

OUTPUT CAPACITORS

The EZ8303 is designed for low output voltage ripple noise. To meet the output voltage ripple and transient requirements, the output capacitor C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or even all ceramic capacitors.

The typical output capacitance range is from 22μF to 100μF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

PFM OPERATION

The EZ8303's low output ripple and high efficiency at intermediate currents are achieved with Pulse Frequency Modulation (PFM). In PFM operation, the low side synchronous rectifier MOSFET turns off to prevent the inductor current go negative during the light load condition. If the load current is further reduced, the control circuit will start to reduce switching frequency to further enhance efficiency. The switching frequency could be lower than audible frequency area under deep light load condition.

SOFT-START

The EZ8303 incorporates an internal soft-start to reduce the voltage and current stress during the start-up. The internal soft-start is set to approximately 0.8ms.

The EZ8303 is capable of monotonically start into a pre-biased output voltage. It starts to switching operation with the applied bias voltage and ramps to output voltage to its nominal value.

EN PIN ENABLE

The EZ8303 is enabled by setting the EN pin to a logic high with the threshold of 1V maximum. When the EN pin voltage is lower than 0.4V, the EZ8303 enters shutdown mode. In shutdown mode, the internal power switches and most control circuitry are turned off, reducing the input current to typically 0.1μA.

An internal 400kΩ pull-down resistor is connected between the EN pin and the ground.

POWER GOOD

The PG pin is open drain pin that can be used to monitor valid output voltage regulation. This pin monitors a 90% window around the regulation point with certain delay. A resistor can be pulled up to a particular supply voltage no greater than 5.5V for monitoring.

The PG pin can be used for sequencing of multiple rails by connecting to the EN pin of other converters. The PG pin can be left floating or connected to ground if not used.

OVER-CURRENT PROTECTION

The EZ8303 SiP Power Module has a cycle-by-cycle valley current mode over current protection (OCP) in a short circuit. The top MOSFET will keep off until the current returns back to safe level. The default valley current limit is set to around 4A to guarantee a DC output current higher than 3A.

OUTPUT UNDER VOLTAGE PROTECTION (UVP)

If the output voltage is less than 30% of the set voltage point for approximately 4μs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into Hiccup protection mode. The typical Hiccup on time is 0.8ms, and the Hiccup off time is 0.8ms. If the output fault conditions are removed, the device will go back to normal operation in the nearest Hiccup on time.

OVER TEMPERATURE PROTECTION (OTP)

The EZ8303 incorporates an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will shut down when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the device will resume normal operation after a complete soft-start cycle.

OVER VOLTAGE PROTECTION

If the DC output voltage is about 3% over the regulation

level, both high-side power FET and low-side power FET will turn off and enter into standy-by mode.

OUTPUT DISCHARGE FUNCTION

The EZ8303 discharges the output voltage when the converter shuts down from V_{IN} or EN, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The discharging FET which in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The output discharge resistor is typically 260Ω under room temperature. Note that the discharge FET is not active beyond these shutdown conditions.

STABILITY COMPENSATION

The EZ8303 module has already been internally compensated for all output voltages.

LAYOUT CHECKLIST/EXAMPLE

The high integration of EZ8303 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.

Figure 3 gives a good example of the recommended layout.

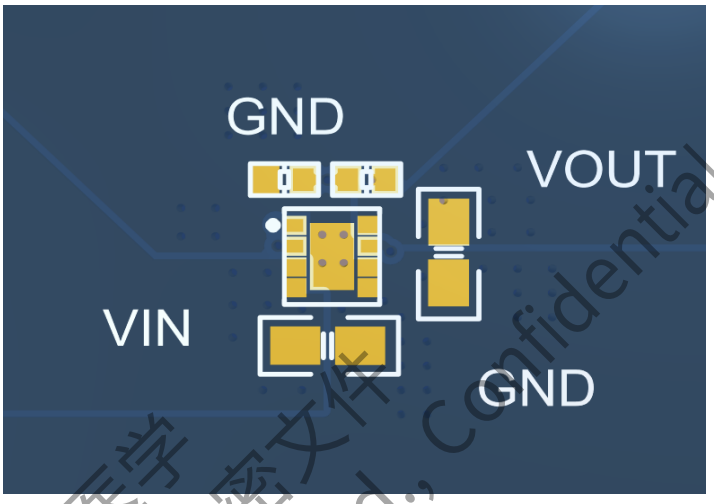


Figure 3 Recommended Layout

TYPICAL APPLICATIONS

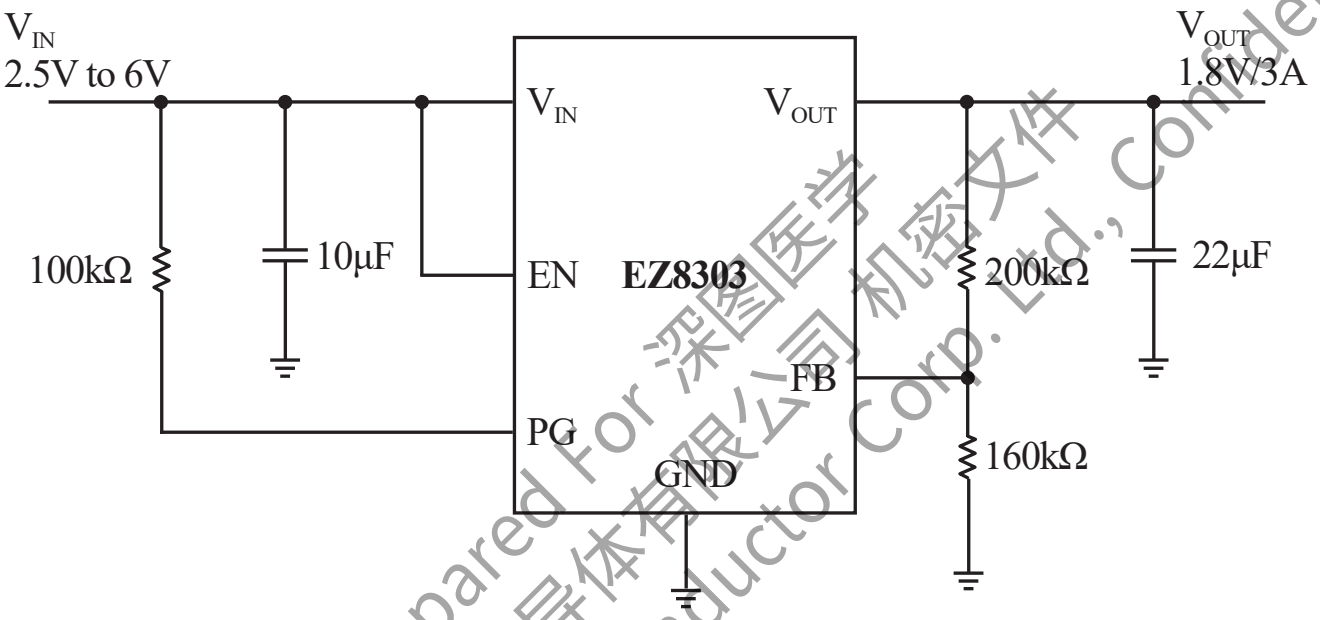
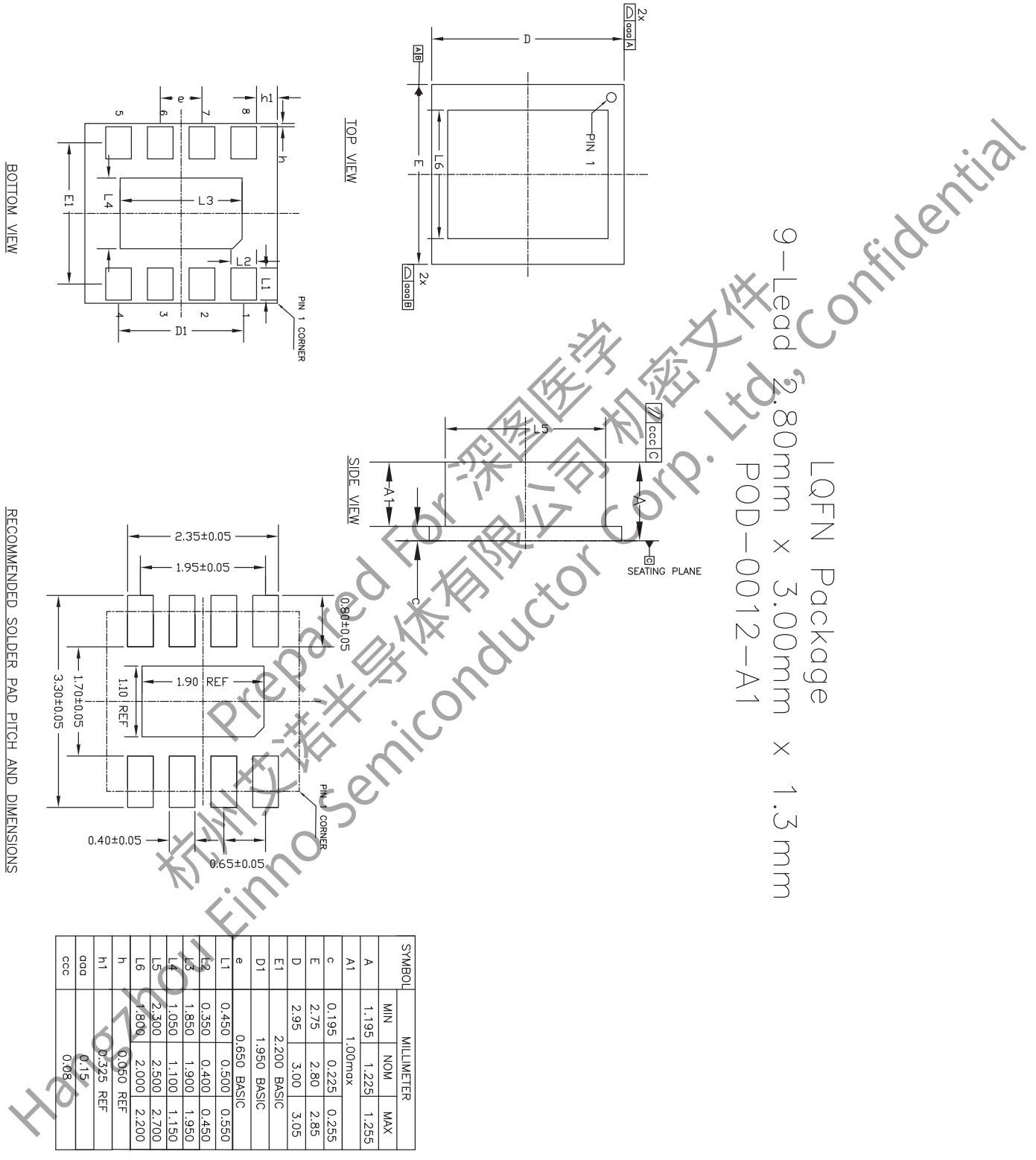


Figure 4 Typical 2.5V to 6V Input, 1.8V at 3A Output Design

PACKAGING OUTLINE DRAWING



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.195	1.225	1.255
A1		1.00max	
c	0.195	0.225	0.255
E	2.75	2.80	2.85
D	2.95	3.00	3.05
E1		2.200 BASIC	
D1		1.950 BASIC	
e		0.650 BASIC	
L1	0.450	0.500	0.550
L2	0.350	0.400	0.450
L3	1.850	1.900	1.950
L4	1.050	1.100	1.150
L5	2.300	2.500	2.700
L6	1.800	2.000	2.200
h		0.050 REF	
h1		0.325 REF	
aaa		0.15	
ccc		0.08	