Haoyang (Chris) Zhang

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EDUCATION

Fudan University (FDU)

Bachelor of Engineering in Microelectronics Science and Engineering *09/2019 - 06/2023*

University of Virginia (UVA)

Master of Engineering in Computer Engineering *09/2023 - 05/2025(exp.)*

RESEARCH INTERESTS

- Energy-efficient high-performance computer architectures and accelerators for machine learning and emerging applications

SELECTED PUBLICATIONS

[1]. **Graph-OPU: A highly integrated FPGA-based overlay processor for graph neural networks.**
Ruiqi Chen, Haoyang Zhang, Shun Li, Enhao Tang, Jun Yu, and Kun Wang.
International Conference on Field-Programmable Logic and Applications (FPL), 2023

[2]. **Edge FPGA-based onsite neural network training**
Ruiqi Chen*, Haoyang Zhang*, Yu Li, Runzhou Zhang, Guoyu Li, Jun Yu, Kun Wang (*equal contribution)
International Symposium on Circuits and Systems (ISCAS), 2023

[3]. **eSSpMV: An embedded-FPGA-based hardware accelerator for symmetric sparse matrix-vector multiplication**
Ruiqi Chen, Haoyang Zhang, Yuhanxiao Ma, Jianli Chen, Jun Yu, Kun Wang
International Symposium on Circuits and Systems (ISCAS), 2023

ACADEMIC & RESEARCH EXPERIENCE

Bit-serial RISC-V Tapeout **UVA**

- Integrated SPI to Wishbone bridge to enable register file access for testability.
- Performed RTL-to-GDSII flow: Synopsys DC and ICC, Innovus, and OpenLane for automation. Reducing initial utilization to 80% by refining macro placement.

FPGA-Based Machine Learning Acceleration Innovations [1][2][3] **FDU**

- Developed novel hardware accelerators with customized instruction sets, optimized data formats, and pipelined dataflow to address trade-offs in performance, flexibility, and efficiency, driving advancements in machine learning workloads.
- Implemented accelerator on Xilinx Zynq UltraScale+ MPSoC and Alveo U50, featuring high-throughput sparse multiplier and optimized datapaths to minimize off-chip data transfers and enhance memory access through HBM. Applied a conjugate gradient-based method to enable efficient onsite training.

Object Detection Implementation on FPGA-based Accelerator **FDU**

- Deployed CNN accelerator to Cyclone V SoC, improving overall latency from 1000ms to 150ms and increasing operating frequency to 190MHz through timing optimization.

- Trained and compressed SSD-MobileNetV1 on PaddlePaddle, enhancing PaddleLite with subgraph fusion and NEON intrinsic-based data arrangement optimization.

INDUSTRY EXPERIENCE

HiSilicon Technologies **Shanghai**

ASIC Digital Design Intern *07/2024 – 09/2024*

- Contributed to all phases of chip development, including drafting design documents, participating in design inspections, introducing innovative features, and executing unit and system-level testing. Improved overall PPA score from 250 to 750.
- Achieved ~2x area reduction with a shared ring buffer architecture and priority-aware control logic, ensuring correct and efficient sequencing and forwarding of multi-priority packets. Achieved ~3x power reduction by module-level clock gating.

SKILLS

- **Programming**: Verilog/System Verilog, Python, C/C++, MATLAB, CUDA, TCL
- **Hardware Design**: Vivado & Vitis HLS, Quartus Prime, Synopsys DC &ICC, SpyGlass/nLint, Modelsim/Verdi, PrimeTime
- **Dev. Tools & Environments**: Git, Docker, Conda, PyTorch, PaddlePaddle, TensorFlow, Apache Spark, Ray, Dask, AWS EC2

MAIN COURSES

Advanced Digital Design Lab (A), Computer Architecture (A), Hardware Accelerators (A), FPGA Architecture and Applications (Honor)(A), **Machine Learning (A), AI Hardware (A), Big Data System (A),** Data Structures and Algorithms, ASIC Design Methodology, Natural Language Processing, Semiconductor Device Physics

CONFERENCE PRESENTATIONS

- Paper and poster presentation at **ISCAS 2023, Monterey, CA**

AWARDS & HONORS

- 2022 China College IC Innovation and Entrepreneurship Competition
  - Gold Medal for East China Division, Silver Medal for National Final