

Open Source Secure Data Protection and Key
Storage Scheme Utilizing Off-The-Shelf SRAM
Component, Software-Based SRAM PUF and
Multifactor Authentication

Ade Setyawan Sajim



Delft University of Technology

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Ade Setyawan Sajim

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Author

Ade Setyawan Sajim

Title

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Graduation Committee

Dr. Ir. Johan Pouwelse	Delft University of Technology
Dr. Ir. Stephan Wong	Delft University of Technology
Haji Akhundov, MSc	Delft University of Technology

Abstract

SRAM PUF has a potential to become the main player in hardware security. Unfortunately, the currently available solution is usually locked to specific entities. Here, we initiate an open source project to develop software-based SRAM PUF technology using off-the-shelf SRAM. We also present a testing result on two off-the-shelf SRAMs as SRAM PUF candidates; Microchip 23LC1024 and Cypress CY62256NLL. Both are tested on the distribution of 0's and 1's in their cells, intra hamming distance, inter hamming distance, and the effect of voltage variation and time interval between enrollment. Testing on two bit-selection algorithms (data remanence analysis and neighbor analysis) are also performed. Based on the testing results, we introduce a PUF enrollment scheme using data remanence analysis as the bit selection algorithm which will locate the location of the stable bits and SRAM Cypress CY62256NLL as the off-the-shelf SRAM. In addition, an idea to create a strong PUF using SRAM is also proposed here. Using a collection of bits as a challenge, the stable bits are permuted among themselves to create a challenge which has a tremendous number of possibilities. Furthermore, we also present a secure data protection and key storage scheme using SRAM PUF. The proposed scheme is influenced by multi-factor authentication. Using a combination of a PUF-generated key and user's password, a derived key is produced and utilized as the final key to protect user's data or/and user's key.

Preface

TODO MOTIVATION FOR RESEARCH TOPIC

TODO ACKNOWLEDGEMENTS

Ade Setyawan Sajim

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Contents

Preface	v
1 Introduction	1
1.1 Need for Self-Sovereign Identity	1
1.2 Rise of PUF as a Security Solution	2
1.3 Problem Statement	4
1.4 Contributions	5
1.5 Outlines	6
2 Related Work	7
2.1 Security Requirements and Cryptography	7
2.2 Symmetric Encryption	8
2.3 Key Derivation Function	9
2.4 Multi-factor Authentication	10
2.5 PUF	10
2.5.1 PUFs Classification	11
2.5.2 Hamming Distances as an Identification Helper	12
2.5.3 Helper Data Algorithms and Fuzzy Extractor	13
2.5.4 Error Correcting Codes	14
2.6 SRAM PUF	15
2.6.1 SRAM Cell	16
2.6.2 Problem: Noise	17
2.6.3 Bit Selection Algorithm	18
2.7 PUF Applications	19
2.7.1 Key Generation using SRAM PUF	19
2.7.2 Secret Key Binding based on Fuzzy Commitment Scheme	20
2.7.3 Secure Key Storage using Optical PUF and Coating PUF .	21
3 Proposed System	23
3.1 Use Case, Assumptions and Requirements	23
3.2 Arduino Mega 2560 as the Embedded Platform	24
3.3 BCH Codes as Error Correcting Codes	25
3.4 Data Protection and Key Storage Scheme	27

3.5	Key Generation Scheme	27
3.6	Bits Locations as the PUF Challenge - Leads to Strong PUF	29
3.7	Security Analysis of The Proposed Scheme	30
4	Implementation, Experiments and Results	33
4.1	Chosen Off-The-Shelf SRAMs	33
4.2	Automated PUF Profiling System	34
4.3	Testing on Chosen Off-The-Shelf SRAMs	35
4.4	Testing on Bit Selection Algorithms	38
4.4.1	Neighbour Stability Analysis	38
4.4.2	Data Remanence Approach	40
4.4.3	Stability Test on Stable Bits	40
4.5	Testing on Bits Locations as A Challenge	47
4.6	Complete Enrollment Scheme	48
4.7	Testing on Secure Data Protection and Key Storage Scheme	49
4.8	Concluding Experiment with Cybercurrency	53
5	Conclusions and Future Work	65
5.1	Conclusions	65
5.2	Future Work	66

Chapter 1

Introduction

1.1 Need for Self-Sovereign Identity

Hardly anyone can live without having their identity. Identity is the one that defines who we are, something which helps to describe the uniqueness of everyone. Identity's role in our daily life is unquestionable. Society requires identity systems to enable identity-requiring transactions at scale, allowing procedures that require the formal asking and answering of identity queries in place, allowing millions of transactions to occur. In modern society, identity is commonly related to social security cards, driver's licenses, and other state-issued credentials. Centralized controlled by the government is the definition of these elements.

Along with the rise of the digital age, identity also redefines itself. Identity in the digital world, can be referred as digital identity, is split into multiple domains. Our Facebook identity does not correlate directly to our Twitter identity or to most other domains. Digital identities are scattered, vary from one Internet domain to another. Scattered identities which locked to multiple entities leads to a problem where users are helpless in front of an authority who can deny their identity or even confirm a false identity. This phenomenon ignites a problem where users are not in control of their identity. There's no clear construction and agreement on how to build the digital identity which usable across platforms. This is an unfortunate thing since lack of digital identity also limits the development and delivery of efficient, secure, digital-based economy and society [1]. The failure to solved the digital identity problem issue even looks a bit strange since we already have *public key cryptography* since 1984, introduced by Chaum [2], which enable secure communication between parties without the hassle of key distribution problem and also provide valid digital signatures. Using public key cryptography, anyone who wants to send any message to a recipient needs to encrypt their message using the recipient's public key. Afterwards, the recipient can read the message after decrypting the received message using its private key.

To fix the scattered identity issue, a solution was proposed: one should be able to store their encrypted data in their own devices or in their own preferred service.

To use the data, a service has to ask the data owner for the private key which will be used to decrypt the data. Using this concept, everyone has to keep their secret keys secure and solely in their possession. A centralized storage of private keys is out of question since it will be a honeypot for cyber attacks. Simply put, keeping secret keys secure is the cardinal problem to solve here.

All problems mentioned above leads to a thinking, identity and secure key storage need to be solved in a decentralized manner. In 2012, a new concept called *self-sovereign identity* (SSI) arise [3]. Self-sovereign identity is a decentralized identity concept which capable of authenticating statements, without any central organization, point-of-failure or any possibility of data tracking [4]. Self-sovereign identity will be able to give users full control over their identity. In simple words, users can store their identity data on their devices, and decide whether to give access to anyone who is willing to use it or not. In addition, there will be no need for a centralized storage since each user database is distributed among themselves. A high possibility to get this concept popular is also present with the introduction of the European Union General Data Protection Regulation [5].

Johan Pouwelse and Martijn de Vos in [4] proposed an SSI design which focused on data protection. Data protection itself is related to securing data against unauthorized access [6]. Their proposal is described by a concept where the user data are encrypted and never leave the device/domain. Any operation which requires the data, such as authentication, will require symmetric encryption on the encrypted data. This encrypted data should be securely protected and the domain should be trustworthy. In addition, the key used to encrypt and decrypt data should be kept securely.

The most common way to store the key is by using a *non volatile memory* (NVM). NVM is a type of computer memory that keep intact its information even after turned off. An example of a product which implements this approach is the debit card. It uses its chip to store information. Unfortunately, this NVM is prone to physical attack. Since the key is permanently stored in the memory, an attacker can use some technique to clone the memory, such as *microprobing* [7]. An attacker may also use a side channel information to retrieve any information about the key. There are numerous other techniques for this kind of attack. This attack can be even worse if someone that knows the system design is involved. Due to this problem, more secure, tamper-evident, tamper-proof solutions need to be presented.

1.2 Rise of PUF as a Security Solution

In 2001, Physical Unclonable Function (PUF) comes in handy as an inexpensive and yet effective security solution to overcome the mentioned problem above by a different way of generating and processing secret keys in security hardware. It was introduced by Pappu [8]. Unlike cryptographic algorithm security which usually relies on a hard-to-solve mathematical problem, PUF idea stems from using

hardware features designed to utilize the physical random nanoscale disarray phenomena [9]. These disarray phenomena can be used as a derivation of keys without having to keep any security-critical information explicitly. This physical randomness is unclonable, even by the original manufacturer due to manufacturing process variations. Furthermore, since the secrets can only be produced when the PUF device is turned on, active manipulation of circuit structure will cause dysfunction of challenge-response mechanism and destroy the secret.

Related to self-sovereign identity concept, [4] present an idea to use PUF and biometric-based authentication to securely protect the data in the self-sovereign identity. Figure 1.1 shows the detailed technology stack in their trust creation proposal on how to build trust in the blockchain era.

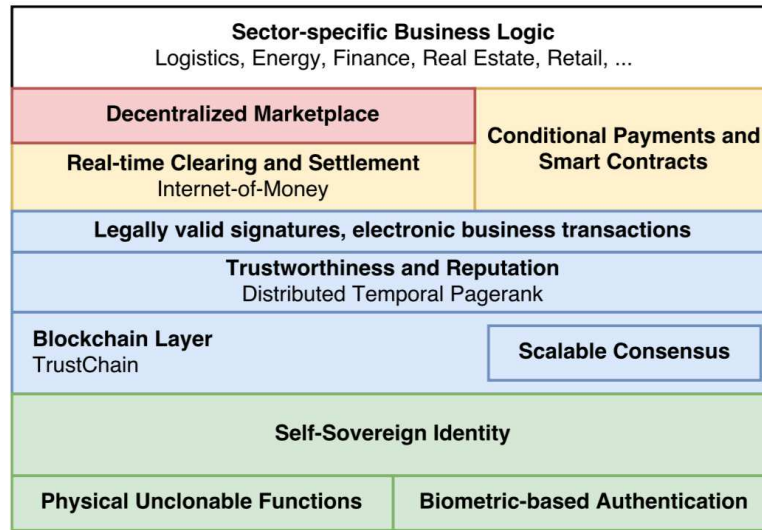


Figure 1.1: Detailed technology portfolio for trust creation in the blockchain age [4]. As shown in the bottom of this figure, Physical Unclonable Functions and biometric-based authentication are utilized to secure the self-sovereign identity.

An example of PUF type is SRAM PUF. SRAM, stands for *static random-access memory*, is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. When a static RAM (SRAM) is turned on, the memory cells have undefined states [10]. The initialized values on the memory cells are also random and unique to each SRAM. Based on these properties, SRAM is considered as a reasonable candidate for PUF. The value of these bits itself is determined by the SRAM cell which consists of two cross-coupled inverters along with two access transistors. This concept was first introduced by Guajardo [11]. In order for SRAM to be used as a cryptographic security key, SRAM PUFs need to have certain characteristics such as the key generated by every SRAM should be reliable and unique. Reliable means the generated key should always be consistent, while unique refers to there should be no correlation between one device or another.

Unfortunately, SRAM PUF is also problematic since it contains noise in its bit value. To handle the noise, error correction code is usually utilized.

1.3 Problem Statement

Since introduced by Guajardo and Holcomb in 2007, there have been many innovations in SRAM PUF field. A simple patent search using patents.google.com with query 'sram; puf' results in 546 results [12]. The number of articles in scholar.google.com also exhibit a high occurrences, shown 2,120 articles (citations and patents are not included) [13]. Even though these facts indicate a promising future for this concept, one also should notice that current state-of-the-art in this field mostly consists of one-off prototypes or specific proprietary implementations. To get an SRAM PUF product from the market, one has to order a specific request from a company. For example, Intrinsic-ID, one of the main leaders in SRAM PUF technology, has a software-based solution which able to generate unique keys and identities for nearly all microcontrollers without a need for security-dedicated silicon [14]. Even though this solution exists and seems easy to use, unfortunately, they don't say specifically how much will it cost to use this solution. They also have another solution for SRAM PUF which is focused on hardware IP (and supporting software/firmware) to enable designers to implement PUFs within their design. This solution has a high possibility to obstruct a small company or a single user to use their solution since usually this type of product are intended to use with an expensive contract. Similar to the software-based solution they offer, they also don't put the explicit price to use this product. An example of a product that uses this solution is FPGA Microsemi Polarfire [15].

The SRAM PUF field lacks an Arduino, Linux, or GCC type of open reference implementation. A quick lookup in Github shows that there's no extensive open source project related to SRAM PUF there. There are projects corresponding to PUF concepts, but most of them also only delve into a simulation. The communities seem to haven't established a wide agreement on which approach yields the strongest security properties.

An additional issue that we would like to address is SRAM PUF's application. As mentioned in Chapter 1, the importance of securing key and user's data is getting higher, especially with the introduction of self-sovereign identity. There are already many SRAM PUF applications published, but sadly, there isn't any example working project that tries to integrate SRAM PUF in self-sovereign identity concept. Most PUF applications are designed for authentication [16] [17] [18] [19] [20] [21] and generating cryptographic keys [18] [22].

Based on these facts, we believe the next challenge for this field is to discover a common approach. The field needs to move beyond isolated single-person projects and single-company approaches towards a mature and sharing ecosystem. The field SRAM PUF requires a single implementation which is continuously improved upon for many years to come and is supported by the majority of the academic and

commercial parties. Furthermore, we also try to initiate an attempt of integration between PUF and self-sovereign identity by providing a scheme to protect user's data and key. This project will be useful in the process of self-sovereign identity development.

To understand our intention in this thesis better, this thesis' problem statement is presented here. The problem statement of this thesis is:

How to develop an open source secure data protection and key storage scheme using off-the-shelf SRAM component and software-based SRAM PUF technology?

Derived from the problem statement, there are two goals defined in this thesis. The first goal is to devise a secure data protection and key storage scheme based on SRAM PUF technology. The data and the key protected by the scheme has to be safe even though the PUF device is lost. Moreover, the scheme should work using off-the-shelf SRAM. This sub-goal leads us to another question, can we build SRAM PUF using off-the-shelf SRAM? If it is possible, what characteristics need to be fulfilled by off-the-shelf SRAM to be eligible as a PUF candidate? In addition, the constructed SRAM PUF has to work without any hardware design, or in other words, software-based construction. The data protection and key storage functions inside the scheme will be helpful in addressing the problem of self-sovereign identity and keeping the secret key. The next goal is to create a sharing ecosystem for the evolution of our data protection and key storage scheme. The ecosystem should be easily accessed and understood to encourage the academics and commercial parties to use and develop the ecosystem together. The easiest step to achieve this goal is by making our thesis as an open source project.

1.4 Contributions

In our work, we strongly believe in open source idea and communities involvement when developing a system. Combined with the problems and potential of SRAM PUF mentioned before, this thesis generates several additions into the state of the art of SRAM PUF knowledge. This thesis' contributions are explained below:

- *An open project for software-based SRAM PUF using off-the-shelf SRAM and Arduino.* This is the first open project on software-based SRAM PUF. This software-based SRAM PUF project consists of Arduino codes and python codes and can be found on a Github repository [23]. It provides the enrollment and reconstruction mechanism which can be utilized to develop other applications. The enrollment stage will generate the helper data and the challenge which stored on a microSD connected to Arduino. The reconstruction part can generate a PUF-generated key based on the challenge and the helper data. The selected off-the-shelf SRAM in this scheme is Cypress CY62256NLL. We also tested another type of SRAM called Microchip 23LC1024 but it shows an insufficient result to be eligible as a PUF

candidate. The enrollment stage also requires a bit selection algorithm called data remanence analysis. In the experiment part, there is another bit selection algorithm tested named neighbor analysis. This method is not selected due to worse result than data remanence analysis.

- *A scheme to enable secure data protection and key storage using off-the-shelf SRAM and software-based SRAM PUF.* This scheme is influenced by multi-factor authentication. Using a combination of the PUF-generated key and user's password, a derived key is produced and utilized as the final key to protecting user's data or/and user's key.
- *A concept to devise a strong PUF using SRAM PUF.* Normally, SRAM PUF is considered a weak PUF due to the limitation of possible challenge-response pairs. We propose to use a set of bit locations as the challenge since when using this concept, the number of possible pairs is the permutation of total bit locations over the required number of bit locations. The total possible CRPs using this concept is a significant large number which may lead to a *strong PUF* definition.

1.5 Outlines

After explaining a brief review of SRAM's potentials and problems, problem statement and our contributions in this chapter, Chapter 2 continues with an overview of security, cryptography, symmetric encryption, key derivation function and multi-factor authentication. Explanations of PUF and SRAM PUF are also presented in that chapter. Chapter 3 describes our proposed SRAM PUF development system, our idea on how to create strong PUF using SRAM PUF, and a scheme to enable secure data protection and key storage using SRAM PUF. Chapter 4 shows our implementation, experiments and results. Last chapter, Chapter 5, summarizes this thesis and also gives our view on possible improvements on this project.

Chapter 2

Related Work

This chapter examines some background theory related to security, cryptography, and PUF. A brief review of security is presented, followed by explanations on symmetric cryptography, key derivation function and multi-factor authentication. Then, theories related to PUF and SRAM PUF are described, continued by a short evaluation on how to generate a key using SRAM PUF.

2.1 Security Requirements and Cryptography

A perfect and 100% secure system is the holy grail of all computing system. Unfortunately, such thing doesn't exist. The best way to achieve that goal is by designing a system to be as secure as possible in a limited scope. To help defining a secure system, common security requirements are mentioned. According to [24], there are four elements on common security, which are:

- *Confidentiality*: a piece of information should be accessible only to an authorized user. For example, an encrypted data can only be decrypted by the secret key owner.
- *Authentication*: assurance of the sender of a message, date of origin, data content, time sent, data information, etc. are correctly identified.
- *Integrity*: any assets can only be modified by authorized subjects. For example, data should be kept intact during transmission
- *Non-repudiation*: a subject should be prevented from denying previous actions. For example, a sender cannot deny the data which it sent.

One way to achieve these four security requirements is by using cryptography. In traditional definition, cryptography can be defined as the art of writing or solving codes [25]. But this definition is inaccurate to use nowadays because instead of depending on creativity and personal skill when constructing or breaking codes, the modern cryptography focuses their definition using science and mathematics.

According to [26], modern cryptography can be defined as "the scientific study of techniques for securing digital information, transactions, and distributed computations." The algorithm which uses cryptography as their main point is called cryptographic algorithm.

Since the birth of cryptography, its main concern is usually related to securing communication which can be achieved by constructing *ciphers* to provide secret communication between parties involved. The construction of ciphers to ensure only authorized parties also can be called as encryption schemes. There are two types of cryptographic algorithm; symmetric and asymmetric algorithm. Symmetric, also known as private key encryption or private key cryptography, requires the same key for encryption and decryption. Meanwhile, in the asymmetric algorithm (can be referred as public key encryption or public key cryptography), there are two keys utilized; private key and public key. A public key is utilized for encryption and a private key is used for decryption. One of the main advantages of symmetric encryption over asymmetric encryption is it requires less computational power which makes it suitable to use in embedded devices.

2.2 Symmetric Encryption

According to [26], symmetric encryption consists of three algorithms which are:

- *Gen*: key-generation algorithm
- *Enc*: encryption algorithm
- *Dec*: decryption algorithm

To illustrate this better, an example using two parties, Alice and Bob are given. Before using the encryption or decryption algorithm, both parties will agree on a shared secret key k . This phase can be referred as Gen. Afterwards, Alice can use the encryption algorithm (*Enc*) E_k using the shared secret key k on a message m which will generate a ciphertext c . This procedure can be noted as $c = E_k(m)$. Bob can read the message by using the decryption algorithm ((*Dec*)) Dec_k using the same shared secret key k . Decryption will result in the plaintext message m . This can be noted as $m = D_k(c)$.

There are many examples of symmetric encryption algorithms, such as RC2, DES, 3DES, RC6, Blowfish, and AES. AES algorithm will be explained below.

AES

AES, stands for Advanced Encryption Standard, is an encryption algorithm based on a substitution-permutation network and established by the U.S. National Institute of Standards and Technology (NIST) in 2001. The block size inside AES has a size of 128 bits, while the key size can be either 128,

192, or 256 bits. The key size itself describes the number of rounds which convert the plaintext into the ciphertext. If 128-bit key is used, there are 10 rounds utilized. 192-bit key lead to 12 rounds, while 14 rounds is used when 256-bit key is applied.

There are four major parts inside AES; *KeyExpansions*, *InitialRound*, *Rounds* and *FinalRound*. In *KeyExpansions*, the round keys are generated using Rijndael's key schedule based on the AES key. Inside a normal round, there are four stages required to do; *SubBytes*, *ShiftRows*, *MixColumns*, and *AddRoundKey*. *SubBytes* refers to a non-linear substitution procedure using a lookup table. *ShiftRows* means an act of shifting cyclically the last three rows of the state. *MixColumns* contains a mixing activity on the columns of the state. *AddRoundKey* involves a fusing process of each byte of the state with a block of the round key utilizing bitwise xor operation. The difference between *InitialRound*, *Rounds*, and *FinalRound* is *InitialRound* only contain *AddRoundKey*, *FinalRound* does not has *MixColumns* inside, and *Rounds* just filled with those four stages.

An encryption can be done by following all these four parts. To convert ciphertext into the original plaintext, it's only required to apply a set of reverse rounds using the same encryption key.

2.3 Key Derivation Function

Besides the encryption algorithm, a *key derivation function* (KDF) is one of the most utilized components of cryptographic applications. Its importance is due to its ability to convert a stable secret, usually contain sufficient amount of randomness but non-uniformly distributed, Z into one or more cryptographically strong secret keys $k \in 0, 1^K$. Cryptographically strong itself refers to indistinguishability by reasonable computation from a random uniform string with similar length [27]. KDF can also be referred as a strong extractor.

A popular example of KDF is a keyed cryptographic hash function. The difference between keyed cryptographic hash function and a normal hash function is a keyed hash function requires an additional *salt* as an input (besides the key to derived). There are three requirements need to be fulfilled as a secure cryptographic hash function; *preimage resistant*, *second preimage resistant*, and *collision resistant*. Preimage resistant means it should be hard to find a message with a given hash value. In second preimage resistant, if one message is provided, it should be hard to find another message with the same hash value. Last, collision resistant refers to difficulty to find two messages with the same hash value.

2.4 Multi-factor Authentication

As mentioned in Section 2.1, authentication refers to assuring any piece of information is correctly identified. Authentication can be done using any of these elements/factors; knowledge (a piece of information which only known by the user, e.g. password), possession (any object which only owned by the user, e.g. RFID card), or inherence (something which uniquely describe the user, e.g. fingerprint). If two or more elements are combined together for authentication, this leads to *multi-factor authentication*. To understand the security level among all possible combinations, Figure 2.1 is provided. The highest possible security level is when these three factors are combined together.

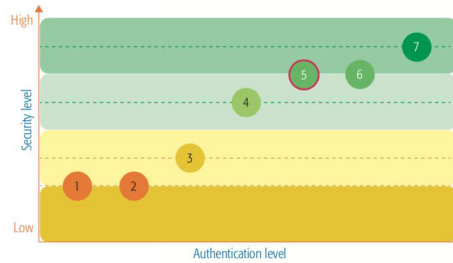


Figure 2.1: Authentication systems security levels: (1) knowledge; (2) possession; (3) knowledge + inherence; (4) inherence; (5) possession + inherence; (6) knowledge + inherence; (7) knowledge + possession + inherence [28].

2.5 PUF

A physical unclonable function is an entity that utilizes manufacturing variability to produce a device-specific output. The idea to build PUF arise from the fact that even though the mask and manufacturing process is the same among different ICs, each IC is actually slightly different due to normal manufacturing variability [9]. PUFs leverage this variability to derive secret information that is unique to the chip. This secret can be referred as a silicon biometric. In addition, due to the manufacturing variability that defines the secret, one cannot manufacture two identical chips, even with full knowledge of the chips design. PUF architectures exploit manufacturing variability in multiple ways. For example, one can utilize the effect of gate delay, the power-on state of SRAM, threshold voltages, and many other physical characteristics to derive the secret.

Due to this feature, PUFs are a promising innovative primitive that is used for authentication and secret key storage without the requirement of secure hardware. Currently, the best practice for providing a secure memory or

authentication source in such a mobile system is to place a secret key in a nonvolatile electrically erasable programmable read-only memory (EEPROM) or battery-backed static random-access memory (SRAM) and use hardware cryptographic operations such as digital signatures or encryption.

There are two main parts of PUF, physical part, and operational part. Physical part refers to a physical system that is very difficult to clone due to uncontrollable process variations during manufacturing. Operational part means a set of *challenges* (PUF input) C_i has to be available to which the system responds with a set of sufficiently different *responses* (PUF output) R_i . This combination of challenge and response is called *challenge-response-pair* (CRP).

$$R_i < -PUF(C_i) \quad (2.1)$$

The common application on using PUF usually requires two phases; the first phase is called *enrollment* and the second one is usually referred as *validation*. In enrollment, a number of CRPs are gathered from a PUF and then stored. In validation phase, a challenge from the stored CRPs is given to the PUF. Afterwards, the PUF response from this challenge is compared with the corresponding response from the database. The response is considered to be valid if there's a CRP from the stored CRPs related to this challenge and response. The validation phase can also be referred as *reproduction* phase since this phase involves a reconstruction of a response given a challenge.

According to [9], to be qualified as PUF, a device should fulfill several characteristics below :

- *Reliable*: A response to the same challenge should be able to be reproduced over time and over a various range of conditions.
- *Unpredictable*: A response to a challenge on a PUF device should be unrelated to a response to another challenge from the same device or the same challenge from a different device.
- *Unclonable*: Challenge-response pairs mapping of a device should be unique and cannot be duplicated.
- *Physically Unbreakable*: Any physical attempts to maliciously modify the device will result in malfunction or permanent damage.

2.5.1 PUFs Classification

Based on the number CRPs, PUFs can be divided into two categories [29]:

- **Strong PUFs**
Strong PUFs can be identified by having a large number of CRPs. Strong PUFs typically used for authentication.

- Weak PUFs

Contrary to strong PUFs, weak PUFs only have a small number of CRPs. Weak PUFs commonly used for key storage.

Besides the number of CRPs, PUFs can also be categorized based on their physical design. There are two major categories, extrinsic and intrinsic.

Extrinsic means that it needs extra hardware added to the PUF component. The extra hardware is required to access the PUF component. There are two subcategories of extrinsic PUFs, non-electronic and analog electronic PUFs. Some examples in non-electronic PUFs are optical PUF, paper PUF, CD PUF, RF-DNA PUF, magnetic PUF, and acoustic PUF. Some design instances in analog electronic PUFs are VT PUF, power distribution PUF, coating PUF, and LC PUF.

In intrinsic, the PUF component has to be available naturally during the manufacturing process. In addition, PUF and the measurement equipment should be fully integrated with intrinsic PUF. There are two subcategories in intrinsic PUFs, delay based and memory based PUFs. An example of delay based PUF is arbiter PUF. The main principle of arbiter PUF is by presenting a race condition on two different routes on a chip where the winner will be decided by an arbiter circuit [30]. As in memory based PUFs, some examples of this design are SRAM PUF, butterfly PUF and latch PUF. SRAM PUF utilized the random physical mismatch in the cell introduced by manufacturing variability which controls the power-up behavior (can be zero, one, or no preference) [30]. Butterfly PUF use the effect of cross coupling between two transparent data latches. Using the functionalities of the latches, an unsteady condition can be initiated after which the circuit resolves back to one of the two stable states [30]. In latch PUF, the concept is based on using two NOR gates which are cross-coupled. These gates will lead to a stable condition depending on the internal discrepancy between the electronic components.

2.5.2 Hamming Distances as an Identification Helper

As explained before, PUF main purpose is dedicated for identification, shown by having a device-specific output. In PUF, *hamming distance* is commonly used as a way to help defining this idea. Hamming distance itself is the number of positions at which the corresponding symbols are different on two equal length strings [31]. There are two types of hamming distance utilized, intra-chip and inter-chip hamming distance. Inter-chip hamming distance is the distance between two responses resulting from giving a similar challenge to two distinct PUF devices [30]. Intra-chip hamming distance refers to the difference between the two responses resulting from applying a challenge twice to a PUF device [32]. To ease the identification

purpose, fractional hamming distance is also introduced. Fractional hamming distance is the number of differences between two strings divided by the length of the bit strings. In ideal PUFs, the intra-chip fractional hamming distance (HD_{intra}) is 0% and inter-chip fractional hamming distance (HD_{inter}) is 50%. Due to noises, normally PUF devices has $HD_{intra} \leq 10\%$ and $HD_{inter} = 50\%$. The identification goal will not be achieved if there is an overlap between HD_{intra} and HD_{inter} [33]. Overlap will happen if the HD_{intra} is too large and HD_{inter} is too small, e.g. HD_{intra} is 35% and HD_{inter} is 30%.

2.5.3 Helper Data Algorithms and Fuzzy Extractor

There are two issues if PUF raw responses are used as a key in cryptographic primitive. First, both weak and strong PUFs rely on analog physical properties of the fabricated circuit to derive secret information. Naturally, these analog properties have noise and variability associated with them. This can be a problem due to sensitivity of cryptographic functions on noises of their inputs. Another issue is the PUF raw responses usually are not uniformly distributed, which makes it an unqualified as a cryptographically secure key. These two issues can be solved using *Helper Data Algorithm* (HDA). One can also refer Helper Data Algorithm as *fuzzy extractor* since both are capable of converting noisy information into keys usable for any cryptographic application [34] [35].

Fuzzy extractor solves both issues mentioned above by using two phases, *information reconciliation* and *privacy amplification*. In information reconciliation phase, possible bit errors are corrected to form a robust bit string [36]. Information reconciliation is tightly related to error correction. In fact, a procedure to do information reconciliation based on error-correcting codes is called code-offset technique [35]. Using code-offset technique, one should be able to reconstruct a bit string w from a noisy version w' as long as the Hamming distance between w and w' is limited to t . The second phase, privacy amplification, is a process to evolve this robust bit string into a full entropy key. Privacy amplification, also can be called as randomness extraction [37], can be done by utilizing two-way hash function.

Beside these two phases, fuzzy extractor also consists of two procedures, Gen and Rep. Gen, stands for *generation*, is a probabilistic procedure which outputs an "extracted" string / key (secret) R and a string (public) *helper data* P on input fuzzy data w . Rep, stands for *reproduction*, is a deterministic function capable of recovering secret key R from the string *helper data* P and any vector w' as long as the Hamming distance between w and w' is limited to t . In [38], Taniguchi et. al illustrated the generation and reproduction procedure of fuzzy extractor on PUF which is shown in Figure 2.2.

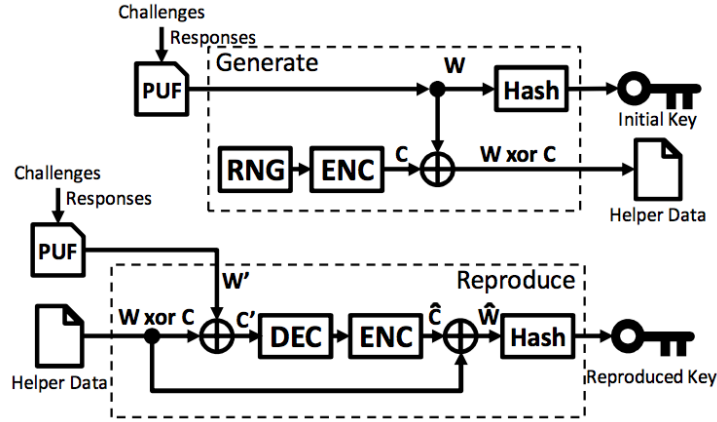


Figure 2.2: Two procedures inside fuzzy extractor; generation and reproduction [38].

2.5.4 Error Correcting Codes

To handle noises occurred inside a PUF, error-correcting codes (ECC) is employed. Error-correcting codes are a class of schemes for encoding messages in an attempt to enable message recovery when there is noise introduced in the sending or receiving of the message. ECC can be divided into two subcategories, hard-decision and soft-decision. Hard-decision works on a predetermined set of values (usually 0 or 1 in a binary code), while a soft-decision decoder may take inputs on a span of values in-between (usually refers to float value).

There are some well-known ECC, such as in hard-decision code, Reed-Solomon code and BCH code; while in soft-decision, Viterbi code and turbo code. Soft-decision code has an advantage over hard-decision code where it can process extra information which indicates the reliability of each input data point and used to form better estimates of the original data. But it has drawback where one should provide a probability function on the data (on SRAM, a probability function on each cell should be provided) to enable a good decoding result. This is a problem if applied on this thesis goal where the system should work on any SRAM off-the-market. Calculating the probability on each SRAM cell will take an extra step, overcomplicate the system and the procedure on using the constructed system. Thus, the hard-decision code is preferred.

One of the popular hard-decision error correcting code is BCH codes. BCH, stands for *BoseChaudhuriHocquenghem*, codes are a family of cyclic error correcting codes which constructed using polynomials over a finite field and work in a binary field. BCH codes are a very flexible set of codes in that within certain bounds there is a great amount of choice in code para-

meters and are relatively efficient in message length and error correction. The code parameters are as follows:

- q : The number of symbols used (e.g., in binary field, $q = 2$)
- m : The power to which to raise q to generate a Galois Field for the construction of the code.
- d : The minimum Hamming distance between distinct codewords.

These parameters lead to several derived parameters which are standard parameters of linear codes:

- n : The block length of the code; for our special case, $n = q * m$
- t : The number of errors that can be corrected, $d \geq 2t + 1$
- k : The number of message bits in a codeword, $k \geq n - mt$

Both BCH codes and Reed-Solomon codes have the capability to correct multiple errors. Reed-Solomon codes are also a flexible ECC and have similar parameters as BCH codes, e.g. n , k , d . Unlike BCH codes, Reed-Solomon codes can work in both binary and non-binary fields. Reed-Solomon codes also perform better in correcting burst errors while BCH codes are better at fixing random errors. BCH codes have an advantage where it requires less computing resource when working on the same parameter compared to Reed-Solomon codes.

2.6 SRAM PUF

SRAM PUF was first proposed by Guajardo and Holcomb in 2007. SRAM PUF uses existing SRAM blocks to generate chip-specific data. Normally, when using SRAM to store data, a positive feedback is given to force the cell into one of the two states (a '1' or a '0') available. Once it is there, the cell will be stable and prevented from transitioning out of this state accidentally. To use it as a PUF, SRAM is turned on and its cell values are retrieved to generate a unique chip-specific output. After powering-up the circuit, the cells stabilize at a state which is defined by the mismatches between the involved transistors. Thus, each SRAM cell provides one bit of output data. To be eligible as a PUF component, an SRAM has to have stable outputs which means any noise has to have little effect on its start-up behavior. In addition, the distribution of 1's and 0's in the SRAM values ideally has to be equal (around 50:50) to ensure there is sufficient amount of randomness exist in the SRAM [39].

As mentioned at the beginning of this chapter, during enrollment, challenge-response pairs are gathered. In SRAM PUF, there are two types of challenges that can be applied to the system. The challenge can be either the whole SRAM memory or specific addresses. If a set of addresses is given as a challenge, an address in there can refer to an address of a byte, a bit, or a sequence of bytes or bits.

2.6.1 SRAM Cell

SRAM uses its SRAM cells to store the binary information. The most common SRAM design is six-transistor (6-T) CMOS SRAM, shown in Figure 2.3. This design utilizes the concept of cross-coupled inverters, constructed by two inverters, each established by two transistors; inverter 1 by Q2 and Q6, inverter 2 by Q1 and Q5. Using this design means the input of an inverter is the output of the other and vice-versa, which also indicates that the output of one inverter is exactly the opposite of the other inverter [32]. Transistors Q3 and Q4, referred as the access transistors, are used as the entry gate to the cell every time a read or write operation will be performed. The bitline (BL), the compliment bitline (BLB) and the wordline (WL) are employed as an entry to the cell. In addition, an SRAM cell will lose its state shortly after power down [40].

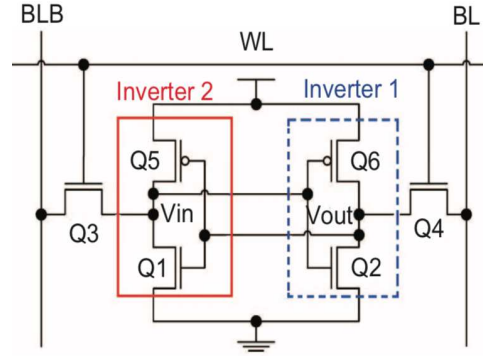


Figure 2.3: A 6-T CMOS SRAM cell [32].

During manufacturing, there are small differences between each SRAM cell due to process variation which leads to a mismatch in the cell [41]. This mismatch also means that the two inverters will always conduct distinctly. Since this mismatch determines the value of the power-up state of an SRAM cell, the power-up state of a cell will be biased towards 0 or 1 depends on the mismatch value. The mismatch itself does not disturb the normal storage functionality of SRAM cell. Based on this bias, SRAM cells can be classified into three categories as shown below:

1. Non-skewed cell

A non-skewed cell has no preference during its startup due to the impact of process variations does not cause any mismatch between the two inverters. This cell generates bit arbitrarily depending upon the noise introduced in the system.

2. Partially-skewed cell

A partially-skewed cell has a small mismatch between the inverters which lead to a preference over value '0' or '1' but the cell can flip its value upon variation in external parameters.

3. Fully-skewed cell

A fully-skewed cell is a heavily mismatched SRAM cell in a way that the cell inclined towards value '1' or '0' and has a resistance against external influence/noises.

2.6.2 Problem: Noise

Similar to most electronic components, SRAM PUF is also affected by any external influence which leads to noises. These noises will flip unstable bits inside the SRAM PUF. Below are some factors presenting noises:

- Voltage

The noise introduced by voltage is called power supply noise [42]. This noise is related to changes in the delay characteristics of the gate. The changes will occur when there are switchings in the circuit after the device is turned on which increase dynamic power and cause a voltage drop on power lines and voltage increase on ground lines.

- Temperature

Temperature variation can be introduced by the surroundings or voltage variation. The preference of a cell inside SRAM has a high probability to be affected by temperature. Temperature affects more than voltage on bit flipping.

- Crosstalk

Crosstalk appears when a signal transmitted on a circuit introduces unwanted side effects in another circuit. Crosstalk happens due to a tight gap between the SRAM cell (tiny interconnect spacing and width). This event becomes more popular due to wider use of faster-operating speeds and smaller geometries (advancement in nanometer technologies) which lead to higher density. Crosstalk is a major contributor to signal integrity problems in modern designs [42]. In addition, higher density in SRAM also influences how environments

affect SRAM performance (more prone to voltage and temperature difference) [43].

- **Aging**
Aging is related to changes in the silicon after usage for a long time [44]. There are three main effects related to the aging of a circuit; time-dependent dielectric breakdown (TDDB), bias temperature instability (BTI) and hot carrier injection (HCI) [45]. TDDB is associated with the creation of a conduction path through the gate transistor structure which causes an increase in power consumption and the circuit delay [46]. BTI causes a degradation of the transistor threshold voltage [47]. HCI generates a change in the transistor threshold voltage [48]. HCI is caused by a high current in the transistor channel injecting charges into the gate oxide during the switching.

2.6.3 Bit Selection Algorithm

Since bit responses are used as the primary input for SRAM PUF, one of the major steps on using SRAM PUF is locations of bits is used as the challenge is looking for stable bits. Stable bits itself refers to fully skewed cells explained before. Even though the error correction code is present to correct the noise of bit responses, it also has a limitation on how many bits it can correct. Since not every SRAM cell is stable, one should take a special caution on deciding which SRAM cell is gonna be the bits to use as PUF input.

Choosing the most stable bits is important to ensure that the PUF result is always the same throughout its lifetime. In here, we use two known algorithms to search for stable bits.

Neighbor Analysis

The first algorithm is using the rank of total stable neighbors [49]. They argue that the cells which are most stable across environmental conditions are surrounded by more stable cells during enrollment. A stable cell surrounded by more stable cells has a tendency to become more stable because its neighboring cells are likely to experience similar aging stress and operating conditions. In this algorithm, all the stable cells are given weight according to the number of stable bits surrounding it. The more stable neighbor cells it has, the higher weight it gets. For example, if a cell is not stable, it is given zero as its score. If it is stable, at least it will get score one. If it only has one stable neighbor on each left and right side, it will get score two as result of an addition of one from being a stable cell and one from having a stable neighbor on both sides. To get score three, it needs to be stable and has two stable neighbors on left and right sides. After determining the

weight of each cell, a heuristic algorithm that greedily chooses cells for the PUF ID/key with weight greater than a threshold is used.

Before the algorithm is performed, one should collect lots of SRAM cells value first. The data should be retrieved in various condition, for example, different voltages, temperatures, and time differences between enrollment. Afterwards, using the data gathered, the location of all stable bits in SRAM need to be located. A stable bit has to has the same value in all enrollment. Last, the neighbor analysis algorithm is performed to get the most stable bits in SRAM.

Data Remanence Approach

Another bit selection algorithm is by using data remanence of SRAM cell [50]. There are only two remanence tests involved in this approach: first, writing a value (1 or 0) to the whole memory and second, briefly turning off the power until a few cells flip. The most robust cells are the cells which effortlessly flipped when written with the opposite data. Strong 1's are bits that are flipped fast after 0 is written to its location. On the contrary, if 1 is written to a bit location and the bit flipped fast, it means that the bit is a strong 0. When using this approach, one should carefully determine the temporal power down time. On one hand, if the temporal power down period is too little, then the data will stay in the previously written state. On the other hand, if the temporal power down time is too lengthy, then the data written in the array will shattered and the SRAM values will go back to its uninitialized state.

A significant advantage using this algorithm compared to the previous one is a much shorter time required to locate stable bits. Using neighbor analysis, there are many SRAM values need to be gathered first which might take hours or days. Locating stable bits from hundreds of data probably also take time as well. If data remanence approach is utilized, there is no need to gather many data. One only need to determine the temporal power down required to get strong bits required. Since usually the temporal down period required is less than 0.5 seconds, this analysis only takes less than one or two minutes.

2.7 PUF Applications

2.7.1 Key Generation using SRAM PUF

In this section, there are two schemes for key generation presented. Both constructions were built by Hyunho Kang et. al. in 2014. The first construction, shown in Figure 2.4, utilizes random number generator (RNG). This design was perfected in the second design shown in Figure 2.5. In the

second design, random number generator was removed to make the construction more efficient without affecting the security. The block length (n) of the error correcting code in these schemes is 255.

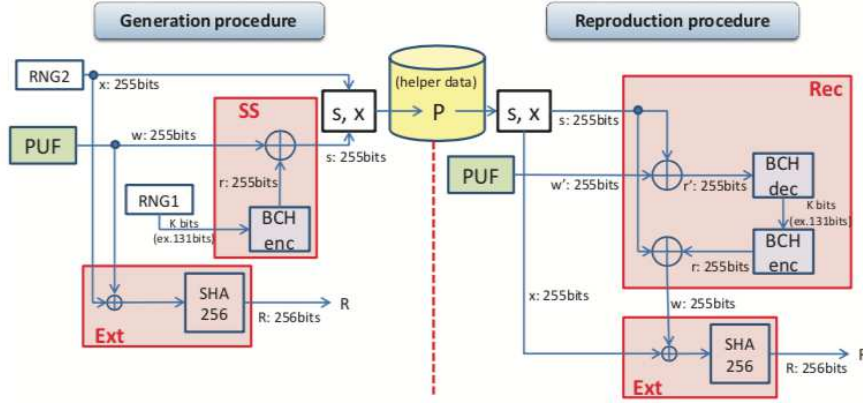


Figure 2.4: Implementation diagram using fuzzy extractor ($N = 255$) [51].

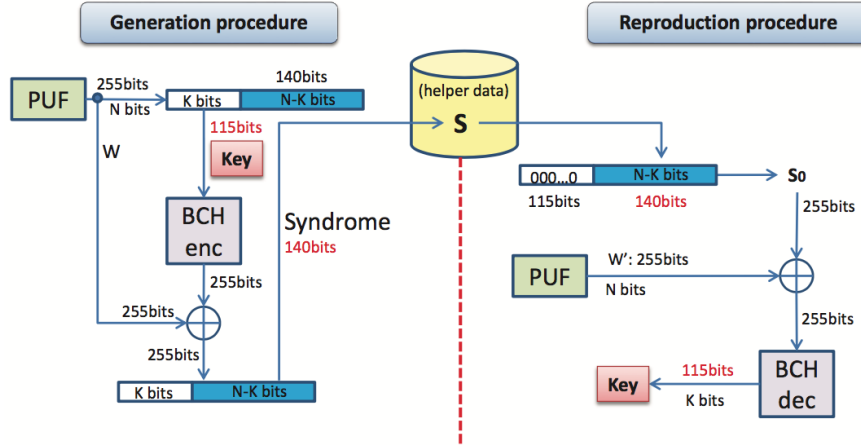


Figure 2.5: Implementation diagram for efficient fuzzy extractor based on the syndrome ($N = 255$) [52].

2.7.2 Secret Key Binding based on Fuzzy Commitment Scheme

Fuzzy commitment was originally introduced by Juels and Wattenberg in 1999 [53]. Figure 2.6 shows the flow of this scheme. To securely bind the

secret, the secret key S^K needs to be chosen first. Afterwards, the secret key is encoded into a binary codeword C^N . Then, the helper data M^N is generated by masking (*xor*-ing) the codeword with the PUF value X^N . To reconstruct the secret, a noisy version of the codeword \tilde{C}^N need be calculated by masking the helper data with the noisy version of PUF observation Y^N . The secret \hat{S}^K can be regenerated by decoding the \tilde{C}^N .

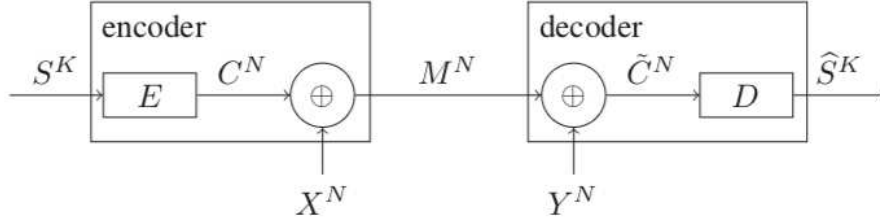


Figure 2.6: Fuzzy commitment scheme [54].

2.7.3 Secure Key Storage using Optical PUF and Coating PUF

In [55], Skoric et. al. present a secure key storage scheme using two extrinsic PUFs; coating PUF and optical PUF. Coating PUF technology is built upon on-chip capacitive quantifications of arbitrary dielectric characteristics of a covering layer which located on top of an IC [56]. Optical PUF itself consists of a 3-D physical structure containing randomly distributed light-scattering particles that produces a speckle pattern (response) when irradiated with a laser beam [55]. This speckle pattern can be considered as the unique fingerprint of the structure. Both PUFs are also considered a strong PUF (has a large CRPs), but optical PUF is considered to be superior than coating PUF due to a much higher number of CRPs and more entropy per response.

In their scheme, to securely store the key, they proposed to store the long-term key in encrypted form. To access the long-term key, a short-term key extracted from the PUF is required.

Chapter 3

Proposed System

This chapter contains our proposed system to achieved our goals which explained in Chapter 1. First, use cases, assumptions and requirements on our system are presented. The chapter continues with reasonings on our chosen embedded platform, Arduino. Then, the selected error correcting code used in the system is explained. Afterwards, we present our data protection and key storage scheme and also our way to generate key using SRAM PUF. Last, our idea to use bits locations as a PUF challenge is shown.

3.1 Use Case, Assumptions and Requirements

As mentioned in the first chapter, a subset of this thesis goal is to provide a secure data protection and key storage scheme using SRAM PUF. This thesis goal describes the use case of our proposed system. In addition, several assumptions are also made to focus the thesis approach. First, the field of both functions are decided to be only available offline. Accessing the SRAM PUF requires the user to have the device next to his/her side. Second, an attacker cannot access the SRAM directly. An attacker may gain the knowledge of the helper data and challenge used in the PUF concept. Last, there is no analysis and/or solution against physical attacks, e.g side channel attacks, in our secure data and key storage scheme. The scheme is designed to be secure against theoretical attacks.

We also have define a set of requirements related to our system. Below are the requirements defined:

1. Software-based construction
There should be no major hardware modification or hardware design to implement the project.
2. Patent/license free
Any dependent component of the design should be in public domain.

3. Open-source and collaboration oriented
If there's a reliable open source project which can be a foundation for this thesis project, instead of building our own software, it is preferred to use that project. This will significantly reduce the time consumed on constructing the whole project. Using other project source code can also increase the collaboration atmosphere. In addition, this requirement may help this project to be known by others since they might introduce our project as one of the projects that uses their code.
4. Key-length security level
The goal on the key-length security level is 256-bits. The concept constructed should be able to use this level and the project's security should be uncompromised even though the key-length is only 256-bits.
5. Off-the-shelf SRAM
The SRAM involved in the thesis should be easily available in the market and cost insignificant.
6. Affordable
The total hardware required to produce the system should be inexpensive.
7. Reproducible
Anyone should be able to reproduce this thesis experiment with no significant effort.

3.2 Arduino Mega 2560 as the Embedded Platform

One of the important details of our system is choosing the platform on where the system will be built. There are two major candidates, Arduino and Raspberry Pi. Both are chosen due to its popularity, availability (easy to get), and various types available. High popularity means the debugging process can be done fast and many references are available online to help the system development. Availability is important because this thesis goal should be easily used by anyone. Low availability will reduce significantly reusability of this project and user's interest. Various types available is a good option for system flexibility. For example, if a user wants to develop a more complex system on top of this thesis' system or desire to use a more complex error correcting codes, he/she can choose a platform with higher computing capability. Besides those three factors, another feature which lead on selecting Raspberry Pi and Arduino is their GPIO. GPIO availability will enable easy communication between the SRAM and the embedded platform.

Compared to Arduino, Raspberry Pi offers a higher computing capability and relatively easier development. This is because Raspberry Pi is basically a mini Linux computer. One can develop a software using C, C++, Python, etc. in Raspberry Pi which may fasten the project development, especially for a developer who already familiar with a specific programming language. Unfortunately, Raspberry Pi requires a longer startup time compared to Arduino. It also requires higher electrical power. If one wants to use the developed project in the embedded area, this two factor is a major trade-off.

Due to the above consideration, Arduino is chosen. Even though one has to construct the system in C++, this can be a positive thing since one can maximize the computing capability easily.

There are various Arduino types available on the market. The chosen Arduino type is Arduino Mega 2560. It is selected because it offers larger memory capability compared to other types, such as 256k bytes of Flash memory, 8k bytes internal SRAM, and 4k byte EEPROM. Besides, it also has 54 digital I/O pins and 16 analog I/O pins which ease the communication to external SRAM.

3.3 BCH Codes as Error Correcting Codes

As mentioned in the previous chapter, BCH codes are flexible Error Correcting Codes (ECC) shown by multiple parameters available. The only fixed parameter is q since the problem is in binary form ($q = 2$). The source code for BCH codes utilized in our construction is a modified version of Robert Morelos-Zaragoza's version which can be retrieved at [57]. This code is selected because it can support m ranging from 2-20 which mean the length of the code that can be corrected ranging from 2 until 1048575. When using BCH codes, one should be careful on deciding the parameters that will be used, for example, larger m or n means a bigger memory needed. These parameters should be determined with several considerations, such as the inner hamming distance of SRAMs and memory available on Arduino Mega 2560.

On deciding the value m , a further look on the memory required during the error correction computation need to be done. Inside the bch codes from [57], the decoding method requires the largest memory compared to other procedures. There are six parameters that depend on m which are elp , d , l , u_lu , s , and err . Table 3.1 shows the required memory given the m value.

Since the internal SRAM in Arduino only has 8k bytes capacity, the chosen m is 6 (requires 4553 bytes, around 55% of total SRAM available in Arduino). This parameter will result in possible n between 32 and 63. n

Table 3.1: Memory required (bytes) given the value of m .

m	Bytes Required	m	Bytes Required
2	53	12	16805897
3	129	13	67166217
4	377	14	268550153
5	1257	15	1073971209
6	4553	16	4295426057
7	17289	17	17180786697
8	67337	18	68721311753
9	265737	19	274881576969
10	1055753	20	1099518967817
11	4208649		

is chosen to be 63 to maximize the length code that can be encoded. The combination of $m = 6$ and $n = 63$ results in various k and t that can be chosen. The combination of all parameter possible is shown on 3.2.

Table 3.2: BCH parameter for $m = 6$ and $n = 63$.

k	t
57	1
51	2
45	3
39	4
36	5
30	6
24	7
18	10
16	11
10	13
7	15

To maximize the error correction capability, $k = 7$ and $t = 15$ is chosen. All these parameter combination will enable error correction capability 23.8% of the data length. To summarize, here are the chosen parameters:

- n : 63
- k : 7
- d : 31
- t : 15

3.4 Data Protection and Key Storage Scheme

Figure 3.1 shows the scheme to protect user's data and key. On an attempt to protect the user's data and key, our proposal is divided into three major parts, first is generate the final key, and the rest is using the final key either to encrypt or decrypt data. To prevent unauthorized person accessing the data with a stolen PUF, an idea from multi-factor authentication is utilized. Instead of just depending on the PUF device to access the key, a combination of PUF device and user knowledge is presented. User knowledge that used here is password. User's password is combined with the PUF-generated key to generate a **final key** using HMAC. The input message to the HMAC is the user's password and the input key to the HMAC is the PUF-generated key. The HMAC function proposed to use is HMAC-SHA3 with key length 256 bits. The final key can be used to encrypt and decrypt user data. To decrypt and encrypt the data, a symmetric encryption algorithm is preferred over the asymmetric one. The symmetric encryption algorithm used is AES with key length 256 bits. If the data is switched to user's key, the data protection scheme proposed here can be also referred as **key storage scheme**.

3.5 Key Generation Scheme

As shown in the previous section, the data protection and key storage scheme requires the PUF to generate the key which will be used to generate the final key. The key generation scheme used in this project is a modified version of Figure 2.5 proposed in [52]. Instead of using $n = 255$, the scheme used in this project will choose $n = 63$. The parameter n, k, t, d is similar to the parameter chosen in the previous section, BCH error correcting code. Figure 3.2 illustrates the mentioned scheme. Using this scheme, to generate a key with length 256-bits requires 37 blocks of this scheme, which lead to 2331 bits required. 37 blocks are calculated from $256 \div 7 = 36.57$, rounded-up resulting in 37. 7 comes from the key generated from 63 bits of data using this scheme. Since one block needs 63 bits of data, 37 blocks require $37 \times 63 = 2331$ bits. In addition, if you look further into the scheme, there is an entropy loss as many as 7 bits every 63 bits input during the generation of helper data. Due to this entropy loss, this scheme can only correct errors on maximum 8 bits instead of 15 bits. Based on this reason, to ensure the key generation scheme always produced the same key, the SRAM component used as root-of-trust has to have maximum error rate (shown by HD_{intra}) 12.7% (calculated from $8 \div 63 \times 100\%$).

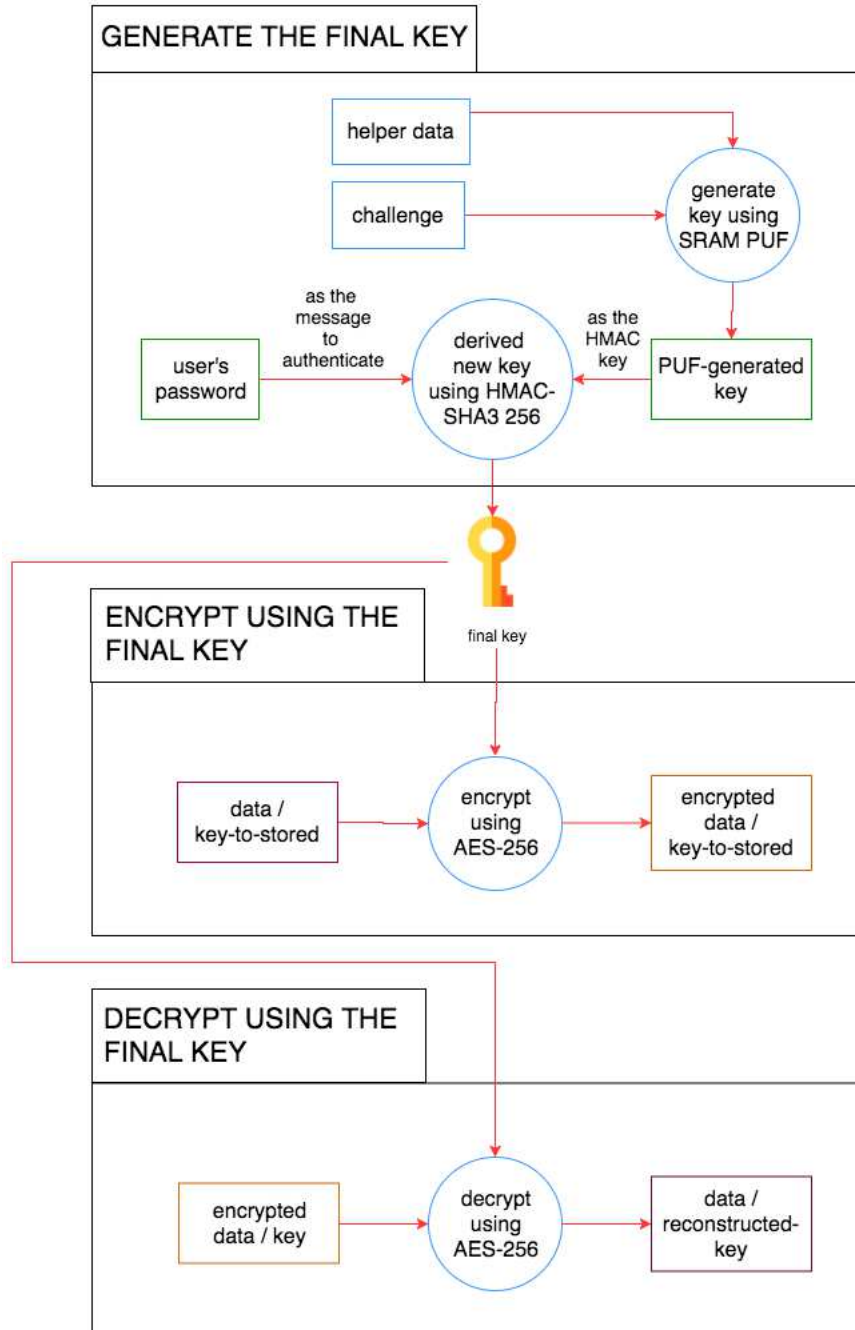


Figure 3.1: Scheme for secure data protection and key storage. There are three stages in here; generate the final key, encrypt using the final key and decrypt also using the final key.

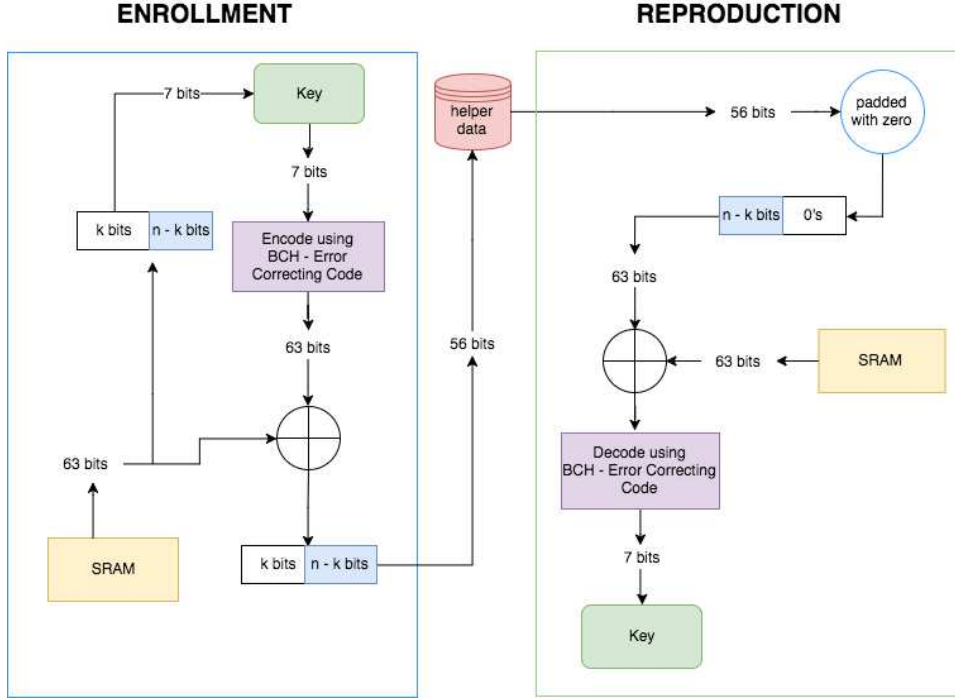


Figure 3.2: Scheme for key generation. $n = 63$, $k = 7$, $t = 15$, $d = 31$.

3.6 Bits Locations as the PUF Challenge - Leads to Strong PUF

An example of a well known PUF construction which claimed to be resistant against brute force attack is Stanzone and Iannaccone's work [58]. They mentioned that their PUF construction is resistant to 10^{25} -trials brute force attack. Inspired by their work, we imagine having a stronger construction. We envision an SRAM PUF which has total challenge-response pairs possibilities more than the number of atoms on earth which predicted to be at least 10^{49} [59]. To achieve this goal, we come up with an idea to use a set of bits locations as a PUF challenge. Below are the reasons why this decision is taken:

1. Stable bits tend to be scattered all around SRAM memory.
2. If there's a burst error on a bit location inside the challenge, this error will not affect many locations in a challenge since this burst error may only lead to a single location. If a location related to multiple bits is used as the challenge, a burst error will affect many bits generated. For example, if locations of bytes are used as the challenge, a burst error might lead to 8 bits errors in the response generated.

3. There are huge possibilities of challenge-response pairs. The number of possibilities is calculated from the *permutation* of the required bits and the available bits using Equation 3.1.

$$P(n, r) = \frac{n!}{(n - r)!} \quad (3.1)$$

As an illustration, if the number of bits required to generate/reconstruct the key is 2331 bits (the length of the bits required to generate 256-bits key when using scheme shown in Figure 3.2), then a set of 2331 bits locations is required as an input (a challenge) to PUF device. And if the SRAM has a total capacity of 65536 bits, using Equation 3.1 explained before, there are $P(65536, 2331) = \frac{65536!}{(65536-2331)!} \approx 10^{11209}$ possible combinations. The total possible CRPs is even much higher compared to the total possibilities of the number of bits required ($2^{256} \approx 5.02 \times 10^{701}$) or the number of possible keys ($2^{256} \approx 1.16 \times 10^{77}$). Due to these large possibilities of challenge-response pairs, this idea will lead to a **strong PUF** (as mentioned in section 2.5.1, a strong PUF can be identified by having a large number of CRPs).

Using this concept, before generating the challenge, the location of stable bits needs to be identified first. The location of stable bits can be detected by using bit selection algorithm mentioned in section 2.6.3. After the location of stable bits is identified, during the generation of a challenge, the locations' order inside the challenge will be randomized.

3.7 Security Analysis of The Proposed Scheme

As mentioned in Section 3.1, our scheme is designed to be secure against theoretical attacks. There are three elements in our scheme as the main parts on ensuring the scheme's security against such attacks; encryption using AES-256, key derivation function using HMAC SHA3-256, and the PUF-generated key. Based on these components, the attack scenarios are presented below:

- The simplest way of attacking the scheme is by applying a cryptanalysis directly to the ciphertext produced by the scheme. If successful, this attempt will result in known final key used in the scheme and the plaintext. In this way, the attacker has to break the security level of AES-256. If brute-force attack is applied to AES-256, the attacker has to try all possibilities of 2^{256} keys which roughly equals to $1.157920892373163 \times 10^{77}$. Even if one can try ten thousand keys every second, the total time needed to try all combinations is still 3.67×10^{65} years (longer than the age of the universe which is 14×10^9 years old). The attacker may also apply key-recovery attack using a

technique called biclique attack [60]. Even though this technique is the best-known attack on AES-256, this technique still requires time complexity of $2^{254.27}$ and data complexity of 2^{40} .

- Another attempt that may be taken by the attacker is by stealing the PUF device. Even though the attacker has the PUF device, he still cannot access the encrypted data directly since he has to guess the PUF owner's password. If PUF owner's password entropy is high enough, the chance for attacker to successfully gain the access to the encrypted data is small since he basically has to break the security level of HMAC SHA3-256 (which requires at least $\min(2^k, 2^n)$ time complexity, where k is the key size and n is the hash output size. [61]).
- The attacker may also try accessing the encrypted data by doing a social engineering to gain the information of PUF owner's password, then guess the PUF-generated key to get the final key which used to encrypt the data. To successfully predict the PUF generated key, it is also a hard work. For example, if one want to brute force all possible input combinations to the PUF key generation scheme, there are $2^{2331} \approx 5.02 \times 10^{701}$ possible combinations. It is actually easier to just try all possible combinations of the PUF-generated key which has 256-bits in length. Even though such fact, the number is not small either. There are still as many as 2^{256} keys which roughly equals to $1.157920892373163 \times 10^{77}$ possibilities.

Based on these reasonings, we believe our proposed data protection and key storage scheme is secure. The only possible way for an attacker to gain information from the encrypted data is by having both PUF device and PUF owner's password.

Chapter 4

Implementation, Experiments and Results

After describing our proposed system as an attempt to achieve this thesis' goals in the previous chapter, this chapter continues with an explanation of several experiment setups and results. This chapter starts by a presentation on two chosen SRAMs that used in experiments; Microchip 23LC1024 and Cypress CY62256NLL. Afterwards, the testing results on two bit selection algorithms (neighbor analysis and data remanence approach) and the stable bits produced by these algorithms are displayed. The chapter continues with examination on our proposed PUF challenge and a presentation on our complete enrollment scheme. Next, testing on the designed secure data protection and key storage scheme is shown. Experiment outcomes on storing bitcoin private key will conclude this chapter.

4.1 Chosen Off-The-Shelf SRAMs

The first step to do in this thesis implementation is looking for SRAM components to be the root-of-trust in our SRAM PUF project. There are numerous SRAM types available in the market. The main requirements on the SRAM are easy to get (a simple google search should show some e-commerce websites to buy from), can be bought in small quantity (≤ 5 pieces), stand-alone component (available without buying extra component, e.g. not embedded in an FPGA), inexpensive (cost less than €5), reasonable memory size ($\geq 64\text{kb}$). These criteria are chosen due to some product only sold to a company or an entity that willing to buy in a big quantity or has to be custom made. There are two SRAM types purchased and tested here; Microchip 23LC 1024 and Cypress CY62256NLL.

Microchip 23LC1024

The Microchip Technology Inc. 23A1024/23LC1024 is a 1024 Kbit Serial SRAM device. This SRAM is very popular shown by many references available online and several GitHub repositories intended just to access this SRAM. The reason of its popularity can be traced to its cheap price, small size, and easy-to-use. The price is ranging from €1.5-3.5. This device has eight pins which contribute significantly to its small footprint (it has dimension of 9.271 x 6.35 x 3.302 mm). It is easy to use because it provides SPI connection which simplified the communication, and has three modes available; SPI (Serial Peripheral Interface), SDI (Serial Dual Interface) and SQI (Serial Quad Interface). Its voltage range also quite large, ranging from 2.5-5.5V. Figure 4.1 shows the Microchip 23LC1024.



Figure 4.1: SRAM Microchip 23LC1024 [62].

Cypress CY62256NLL

The Cypress CY62256NLL is a 256k bit SRAM device. Even though this device is less popular than Microchip 23LC1024, it's still widely used. One of the reason is that this device has an automatic power-down feature, reducing the power consumption by 99.9 percent when deselected. Unlike Microchip 23LC1024, Cypress CY62256NLL doesn't have an SPI connection which complicates the communication. To communicate, one should utilize its twenty-eight pins available. Since it has many pins, this contributes to its significantly larger size compared to Microchip 23LC1024. Specifically, its size is 37.592 13.97 4.953 mm and produced using 90nm technology. Its voltage range is ranging from 4.5V-5.5V. Figure 4.2 shows Cypress CY62256NLL.

4.2 Automated PUF Profiling System

To increase the experiment's efficiency, an automated PUF profiling system is constructed. The system consists of a PC, act as a master, and an Arduino connected to an external SRAM component which acts as a slave. A custom protocol was designed to communicate between them. It is specifically



Figure 4.2: SRAM Cypress CY62256NLL [63].

designed to be generic and usable for all types of PUF profiling measurements. The software on Arduino side waits for measurement commands sent by PC on the serial link after booting. The designed protocol is dedicated for read bytes, write bytes, and SRAM disable/enable. The system also supported parallel profiling which significantly increases the effectiveness. Figure 4.3 shows the setup and the schematic to profile four SRAMs Cypress CY62256NLL concurrently using four Arduino.

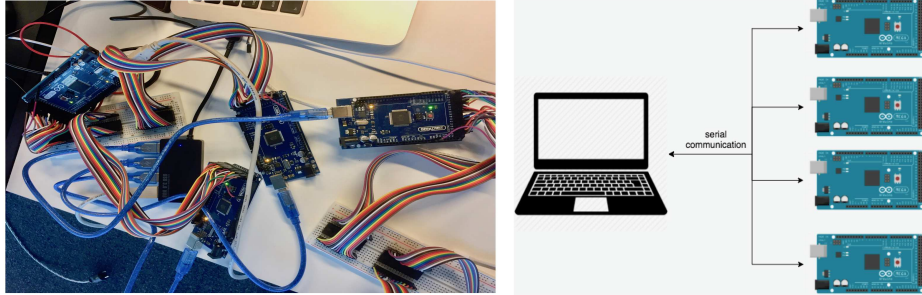


Figure 4.3: Automated PUF profiling setup using a PC and four Arduino. Left picture shows the actual setup, while the right picture displays the schematic of such setup.

4.3 Testing on Chosen Off-The-Shelf SRAMs

As mentioned in Chapter 2, to be qualified as a PUF candidate, an SRAM has to be stable in various conditions. This means if it is given various power input or used in varied temperatures or utilized for a long time, the initialized SRAM values has to remain similar or only has little changes. Under any condition, there should be no overlap between HD_{intra} and HD_{inter} . Moreover, the SRAM has to have a sufficient amount of randomness, shown by having equal distributions between 1's 0's on its values. To ensure

the quality of these two SRAMs, there are several experiments performed on each SRAM, such as calculating HD_{intra} and HD_{inter} given the whole memory value as the challenge and also the distribution of 1's and 0's inside SRAM memory.

Microchip 23LC1024

There are ten SRAMs Microchip 23LC1024 that were available during the experiment. To check whether this SRAM is a justifiable candidate for PUF, several testings are performed. First, the number of 1's and 0's in memory after a start is calculated. Unfortunately, the average distribution of 1's and 0's are not similar, 1's occupy 70% and 0's fill the remaining 30%. Second, HD_{intra} and HD_{inter} are calculated on these chips. The calculation is done using twenty data of chip memory values on each chip which retrieved at room temperature, 5V input and 10 seconds interval between retrieval attempts. From these chips, the average HD_{intra} is 6.18% and the average HD_{inter} is 42.54%. Third, the effect of voltage variation on the HD_{intra} and HD_{inter} are also evaluated. The calculation is done using memory values on each chip which retrieved on room temperature and 10 seconds interval between retrieval attempts. The voltage range is between 2.5V and 5V with 0.5V increase on a step. On each step, there are three data retrieved. Using these data, voltage variation results in an average HD_{intra} 8.21% and an average HD_{inter} 42.59%.

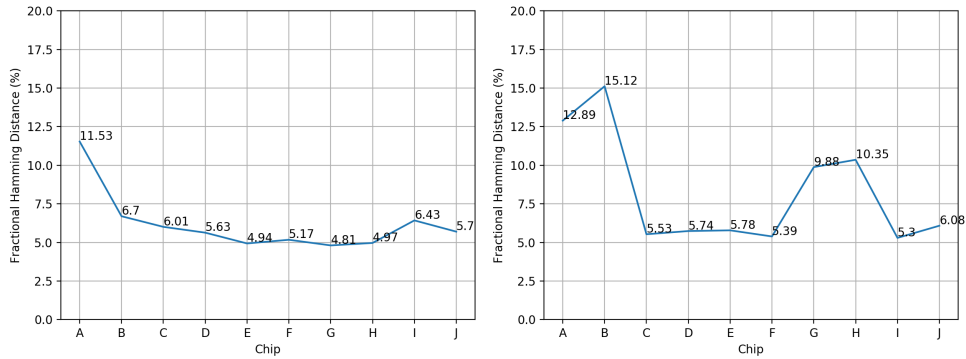


Figure 4.4: HD_{intra} of ten SRAMs Microchip 23LC1024. The left is HD_{intra} with constant voltage, the right one is tested based on the voltage variation.

Based on these experiments, SRAM Microchip 23LC1024 shows questionable results. First, the distribution of 1's and 0's inside the SRAM is not balanced. Second, a voltage variation shows that it significantly affects the HD_{intra} . Fortunately, there is no overlap between HD_{intra} and HD_{inter} . Even though these outcomes make us doubtful on this SRAM quality as an

SRAM PUF candidate, we decided to continue using this SRAM in further experiments. Hopefully, when we locate the stable bits inside the SRAM, the experiments done on the stable bits will show a better result than this result.

Cypress CY62256NLL

There are five Cypress CY62256NLL SRAMs that were available during experiment. Similar like on previous SRAM, several testing are performed to check whether this SRAM is a justifiable candidate for PUF. First, the number of 1's and 0's in an initialization is counted. Fortunately, unlike the 23LC1024, the average distribution of 1's and 0's are similar, both occupy 50% of total bits available. Next, HD_{intra} and HD_{inter} are calculated on both chips. The calculation is done using twenty data of chip memory values on each chip which retrieved at room temperature, 5V input and 10 seconds interval between retrieval attempts. From these chips, the average HD_{intra} is 4.85% and the average HD_{inter} is 39.28%. Last, the effect of voltage variation on the HD_{intra} and HD_{inter} are also evaluated. The calculation is done using chip memory values on each chip which retrieved on room temperature and 10 seconds interval between retrieval attempts. The voltage range is between 4.5V and 5V with 0.1V increase on each step. On each step, there are ten data enrolled. The average HD_{inter} on voltage variation is 38.59%, while HD_{intra} is 3.58%. Figure 4.5 shows the HD_{intra} between the constant and the variated voltage.

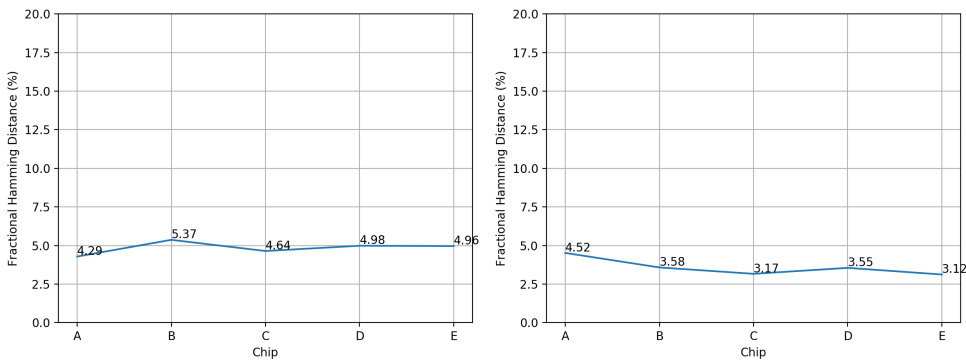


Figure 4.5: HD_{intra} of five SRAMs Cypress CY62256NLL. The left is HD_{intra} with constant voltage, the right one is tested based on the voltage variation.

The results shown above indicate that SRAM Cypress CY62256NLL is a qualified candidate for SRAM PUF. A well distributed 0's and 1's inside SRAM memory, voltage variation has little effect on HD_{intra} and HD_{inter} ,

and no overlap between HD_{intra} and HD_{inter} lead us to continue using this SRAM on further experiments.

4.4 Testing on Bit Selection Algorithms

In this section, the test on stable bits produced by two algorithms, neighbor stability and data remanence analysis, is shown. The test was done on a single chip of each SRAM type. The explanation of both algorithms can be found on section 2.6.3.

4.4.1 Neighbour Stability Analysis

To use this algorithm, first, data of SRAM bits value from various condition (voltages and time difference between data retrieval attempts) need to be gathered. Afterwards, the bits which remained stable on all data retrieved are located. Then, the rank of remained stable bits are calculated. Last, n bits with highest rank can be used according to the necessity. The higher the rank, the more stable that bit should be.

Microchip 23LC1024

As input for the algorithm, there are 500 data of SRAM bits value used for this chip. The voltage variation is randomized between 2.5V - 5.0V. The time difference between data retrieval attempts is ranging from 5 seconds until 1 hour. SRAM Microchip 23LC1024 itself has capacity 1048576 bits. After doing the calculation from those five hundred data, there are 413374 remaining stable bits. From those remaining stable bits, the rank of each bit is calculated. The frequency of bits rank is shown in Figure 4.6. As shown in this figure, the total bits with rank more than 5 is insignificant, only showing 493 bits. Bits with rank more or equal to six is merged into a single bar because the frequency among those rank is usually only a single digit.

Cypress CY62256NLL

Similar like with SRAM Microchip 23LC1024, there are 500 memory values retrieved in SRAM Cypress CY62256NLL. SRAM Cypress CY62256NLL is able to store 262144 bits in its memory. The remained stable bits after 500 data retrieval are 102708 bits (39,18%). The result of the calculation is shown on Figure 4.7. Compared to Microchip 23LC1024, this SRAM shows more promising result since there are many bits with ranks more than seven. Even to get two thousand bits, the lowest rank that can be included is twelve.

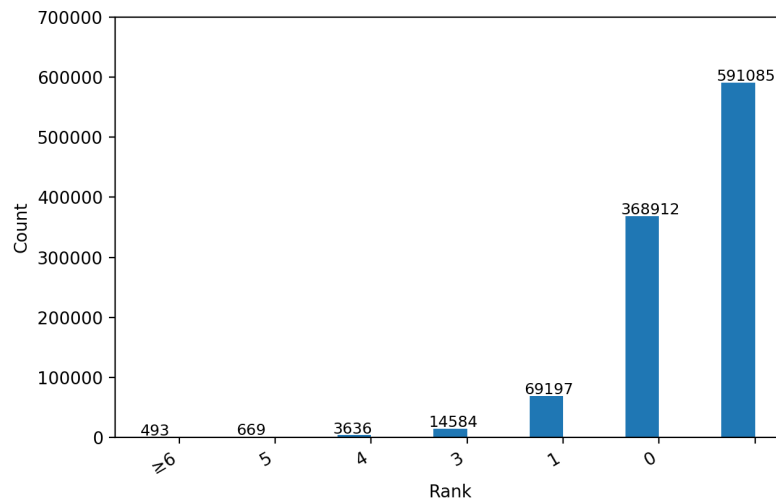


Figure 4.6: Remaining stable bits count according to their rank in SRAM Microchip 23LC1024.

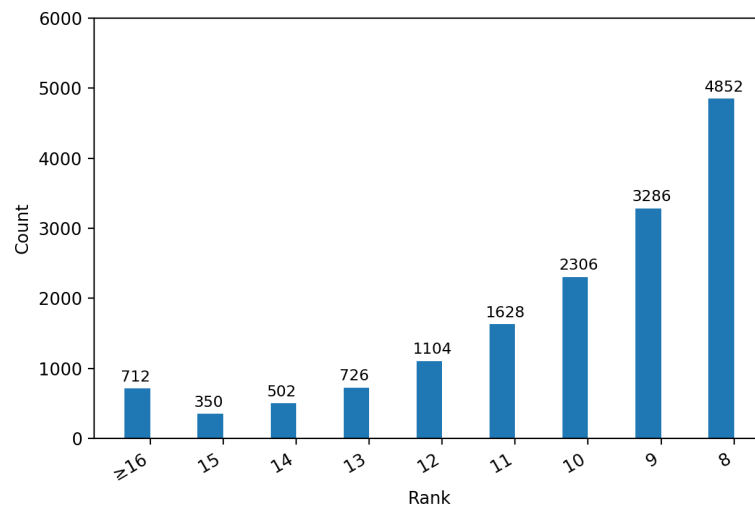


Figure 4.7: Remaining stable bits count according to their rank in SRAM Cypress CY62256NLL.

4.4.2 Data Remanence Approach

The result of data remanence analysis on both SRAMs is shown below.

Microchip 23LC1024

On SRAM Microchip 23LC1024, the data remanence analysis is done on time variance between 0-1.0 second. The result can be seen on Figure 4.8. In this figure, it is shown that SRAM Microchip 23LC1024 will reach the uninitialized point if it is temporarily turn off for 0.7 seconds.

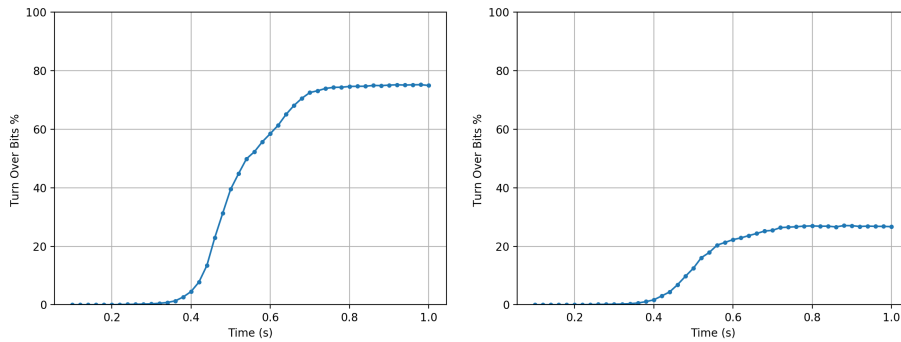


Figure 4.8: Measured SRAM Microchip 23LC1024 data remanence for data 0 (left) and data 1 (right). SRAM Microchip 23LC1024 will reach the uninitialized point if it is temporarily shut down for 0.7 second.

Cypress CY62256NLL

On SRAM Cypress CY62256NLL, the data remanence analysis is done on time variance between 0-10 seconds. The result can be seen on Figure 4.8. In this figure, it is shown that SRAM Cypress CY62256NLL will reach the uninitialized point if it is temporarily shut down for 5.0 second.

4.4.3 Stability Test on Stable Bits

In this section, test results on the effect of time interval and voltage on stable bits using both algorithms on each SRAM are shown. The effect of aging and temperature is not tested due to a limitation on time and equipment. For the effect of time interval testing, the enrollment was done on 16 days with one day gap between enrollment. Voltage effect testing was done on voltage ranging from 4.5V-5V for SRAM Cypress CY62256NLL and 2.5V-5V for SRAM Microchip 23LC1024. The test is done on 4662 bits which is twice the length of the bits required to generate 256 bits key when using scheme shown in Figure 3.2. The result of time interval testing on SRAM

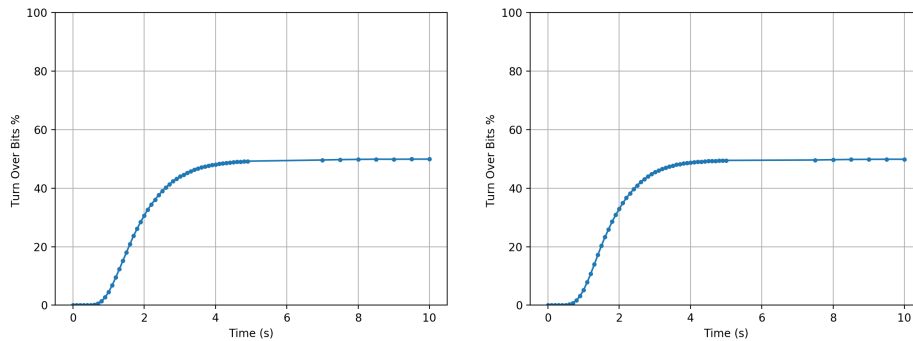


Figure 4.9: Measured SRAM Cypress CY62256NLL data remanence for data 0 (left) and data 1 (right). SRAM Cypress CY62256NLL will reach the uninitialized point if it is temporarily shut down for 5.0 second.

Microchip 23LC1024 is shown on Figure 4.10, while Figure 4.12 displays the result for SRAM Cypress CY62256NLL.

Microchip 23LC1024

- **Neighbor Stability Analysis**
To get 4662 bits, there are three categories included; rank similar or higher than 6 with 493 bits, rank 5 with 669 bits, and rank 4 with 3500 bits. During testing on varied voltage and time interval, the stable bits generated using neighbor stability analysis show a poor performance by having maximum 2389 bits changing (HD_{intra} 51.24%) which also produces an overlap between HD_{intra} and HD_{inter} . The maximum difference is produced when the difference between enrollment is 8 days.
- **Data Remanence Approach**
To get 4662 bits, strong 1's are generated using power down period of 0.185 seconds, while strong 0's are calculated when 0.27 seconds are used as the power down period. The difference between power down period during generation of strong 1's and strong 0's is because the number of 1's that flipped fast are more compared to 0's. This is also related to the 0's and 1's distribution during normal initialization (0's count for 30% and 1's filled 70%). Similar to the previous algorithm, the stability of bits produced by using this algorithm is also not good. The worst change happens when 8 days is used as the time interval between testing, showing as many as 2328 bits (HD_{intra} 49.93%) and also introduce an overlap between HD_{intra} and HD_{inter} .

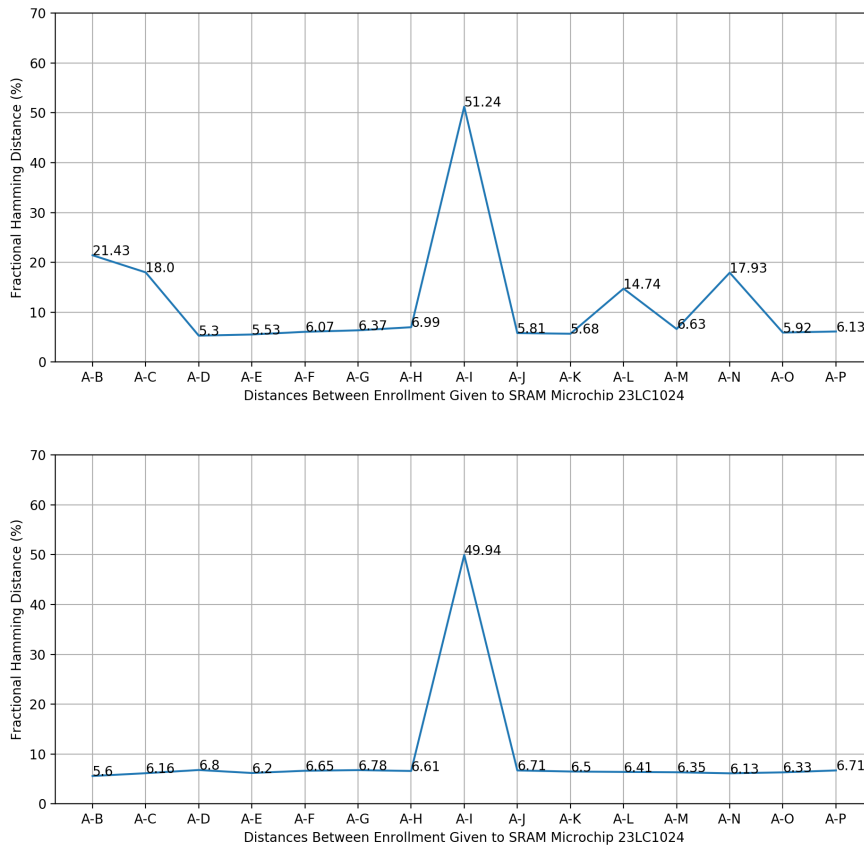


Figure 4.10: Time interval testing results on SRAM Microchip 23LC1024. Top figure is the testing result on stable bits generated using neighbor analysis, while the bottom one is tested on data remanence generated stable bits. Index A on x-axis refers to enrollment on day 1, B on day 2, etc. Index A-B refers to fractional hamming distance between enrollment on day 1 and day 2.

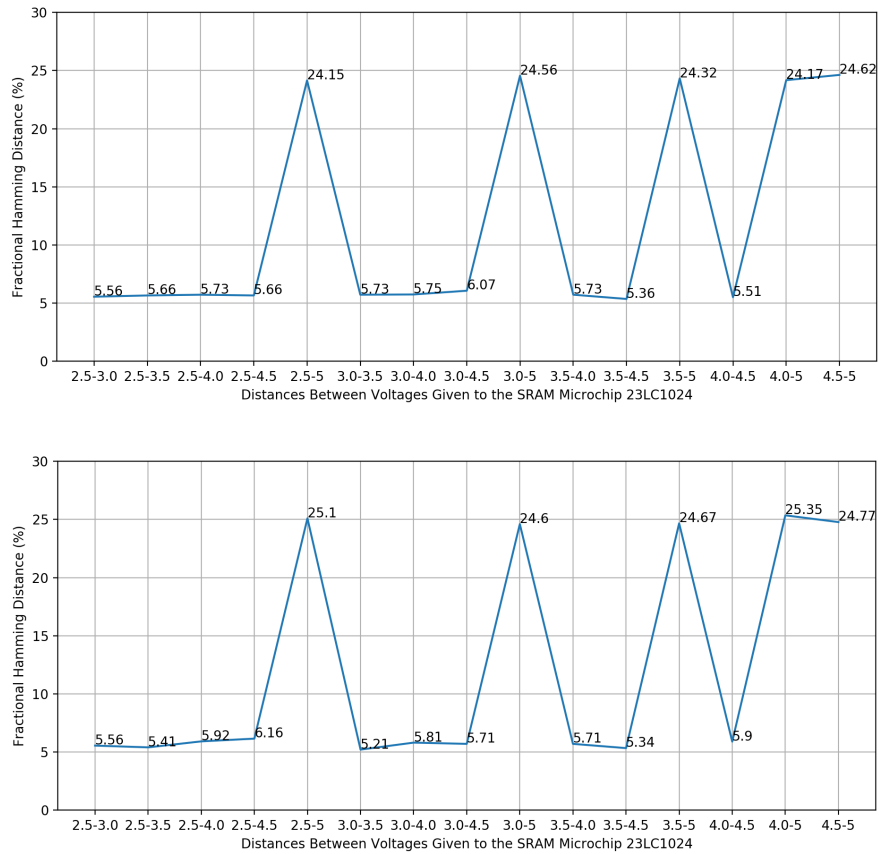


Figure 4.11: Voltage variation testing results on SRAM Microchip 23LC1024. Top figure is the testing result on stable bits generated using neighbor analysis, while the bottom one is tested on stable bits produced by data remanence analysis. Index on x-axis refers to two different voltages, e.g. 2.5-5.0 means the fractional hamming distance between enrollment on voltage 2.5V and voltage 5.0V.

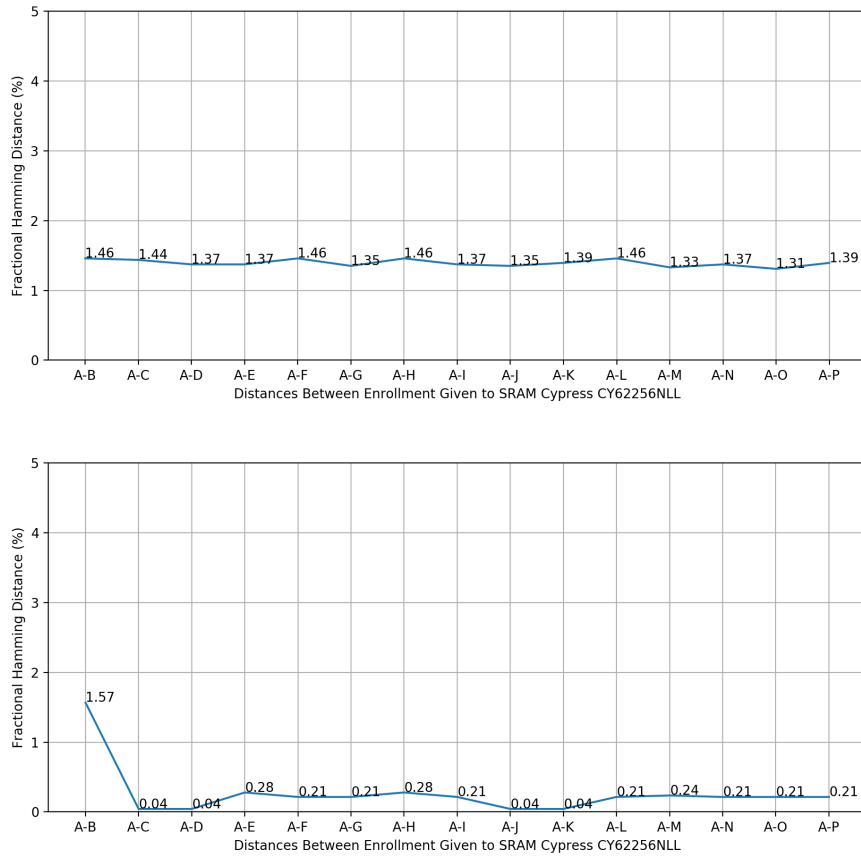


Figure 4.12: Time interval testing results on SRAM Cypress CY62256NLL. Top figure is the testing result on stable bits generated using neighbor analysis, while the bottom one is tested on data remanence generated stable bits. Index A on x-axis refers to enrollment on day 1, B on day 2, etc. Index A-B refers to fractional hamming distance between enrollment on day 1 and day 2.

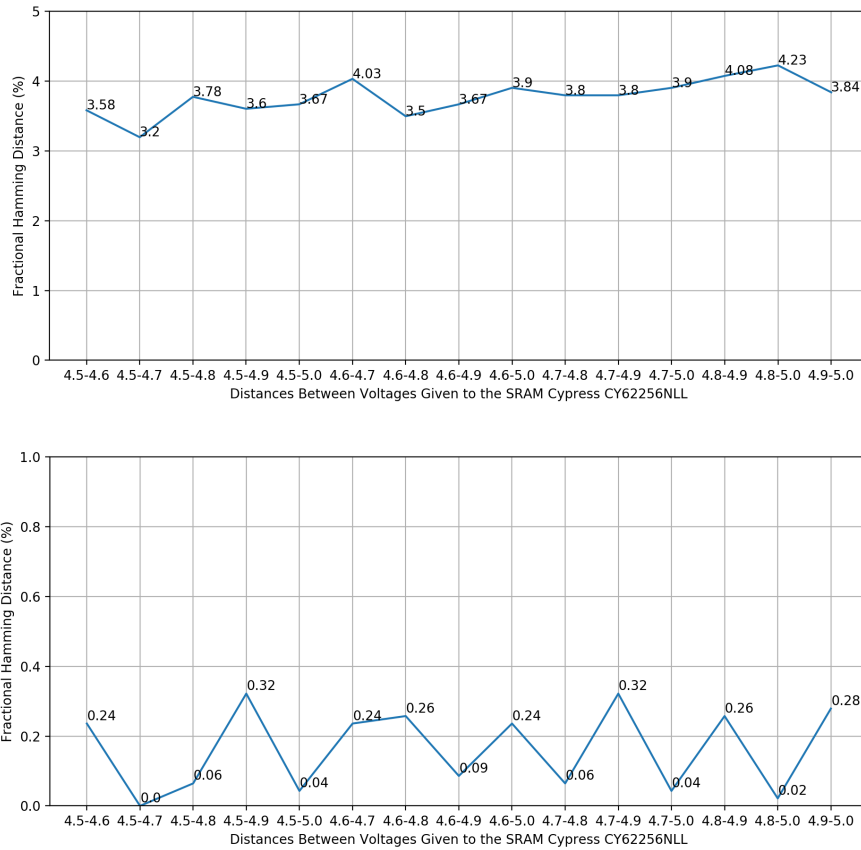


Figure 4.13: Voltage variation testing results on SRAM Cypress CY62256NLL. Top figure is the testing result on stable bits generated using neighbor analysis, while the bottom one is tested on stable bits produced by data remanence analysis. Index on x-axis refers to two different voltages, e.g. 4.5-4.6 means the fractional hamming distance between enrollment on voltage 4.5V and voltage 4.6V.

Cypress CY62256NLL

- Neighbor Stability Analysis

To get 4662 bits, there are six categories included; rank similar or higher than 16 with 712 bits, rank 15 with 350 bits, rank 14 with 502 bits, 726 bits of rank 13, 1104 bits of rank 12, and 1268 bits of rank 11. Under the voltage and time interval variation, the stable bits generated using neighbor stability analysis show decent reliability by having maximum 197 changing bits (HD_{intra} 4.23%) when the data is gathered on voltage 4.8V and 5V.

- Data Remanence Approach

Unlike SRAM 23LC1024, power down period when enrolling strong 1's and 0's on CY62256NLL is not different. To get 4662 stable bits, both are enrolled using power down period 0.34 seconds. During the voltage and time interval variation, the stable bits produced by using algorithm also shows a promising result. It only accounts for maximum 73 bits difference (HD_{intra} 1.56%).

Stability Test Conclusion

Based on these results, SRAM Cypress CY62256NLL is shown to be a reliable SRAM candidate for PUF due to its well distribution of 1's 0's inside its memory and small variance when tested on various voltage and time interval between enrollment, especially the stable bits produced by data remanence analysis which has HD_{intra} less than 2% on any testing. If Cypress CY62256NLL is used as the root-of-trust to produce PUF-generated key, the key is ensured to always have the same value since the key generation scheme can tolerate up to 12.7% while the error rate of stable bits of Cypress CY62256NLL produced by data remanence algorithm is always less than 2%. Sadly, the other SRAM, SRAM Microchip 23LC1024, has displayed a poor performance to be eligible as a PUF candidate. Unbalanced 1's and 0's distribution and large HD_{intra} when the stable bits are tested (larger than the maximum error capability of the key generation scheme, and even introduces an overlap between HD_{intra} and HD_{inter}) are two main reasons why this SRAM is not recommended to use as a PUF candidate.

These different results between two types of SRAMs lead us to a thinking that the SRAM size and the technology used in SRAM manufacturing affects a lot of SRAM quality as a PUF candidate. For example, Cypress CY62256NLL has significantly larger size than Microchip 23LC1024 (a rough approximation results in 13.38 times larger). Cypress CY62256NLL also has a smaller capacity (256k) than Microchip 23LC1024 (1024k). In addition, Cypress CY62256NLL is produced using quite old technology (90nm) while Microchip 23LC1024 has a higher chance to be produced us-

ing a newer technology since it has a much smaller size but larger memory size than Cypress CY62256NLL (there is no information on manufacturing technology used in the production on their websites and the Microchip 23LC1024 manual descriptions). From these explanations, we can conclude that Cypress CY62256NLL has less density than Microchip 23LC1024. These reasons lead us to a confirmation of density effects explained in Section 2.6.2 which says the more dense an SRAM, the more environments affect the performance of the SRAM. But does it mean that SRAM PUF cannot be produced using an SRAM with a high density? This seems untrue due to some SRAM PUF references mentioned a newer technology in their PUF constructions, e.g. Cortez et. al. in [64] use SRAMs which produced using 32nm and 45nm (sadly, there is no information on the type and manufacturer of their tested SRAMs). Furthermore, since every company always has their own way of dealing with noises introduced by high density level, we cannot conclude that high density level always lead to low quality of an SRAM as a PUF candidate. Now, this lead to another questions, what is the main criteria if an off-the-shelf SRAM is going to be used a PUF candidate? Should we trust specific company such as Cypress and mistrust another company like Microchip? Or do we need to look into specific product to determine whether an SRAM is suitable for a PUF component? Should we always prefer SRAMs with less density? We suggest the communities and the academicians to study this thing further.

Another conclusion that can be retrieved is that data remanence analysis is also proven to be a better bit selection algorithm than neighbor analysis. This also confirms the claim by Muqing et. al. [50]. Futhermore, based on this outcome, further testing shown below are only done on SRAM Cypress CY62256NLL and the stable bits used are generated using the data remanence algorithm.

4.5 Testing on Bits Locations as A Challenge

In this section, the testing results on our proposed PUF challenge is presented. As mentioned in the previous chapter, bits locations is selected as the PUF challenge in our application. The test was done on SRAM Cypress CY62256NLL. Cypress CY62256NLL itself has a capacity to store 262144 bits. The number of bits required in a challenge is 2331 bits (the length of the bits required to generate 256 bits key when using scheme shown in Figure 3.2). Using Equation 3.1 explained in previous chapter, there are $P(262144, 2331) = \frac{262144!}{(262144-2331)!} \approx 10^{12626}$ possible combinations. Using this large number of possibilities, once again we emphasize that this construction can be a proper strong PUF construction using SRAM PUF.

The selected test to test this challenge is by calculating the HD_{inter} among

five SRAMs. Figure 4.14 shows the result of this experiment. As shown in that figure, the HD_{inter} is ranging between 35.26% until 46.93%, with average 42.08%. Since there is no overlap between HD_{intra} (shown on Section 4.4.3) and HD_{inter} , this result shows that using bits locations as a challenge is sufficient to distinguish an SRAM from another.

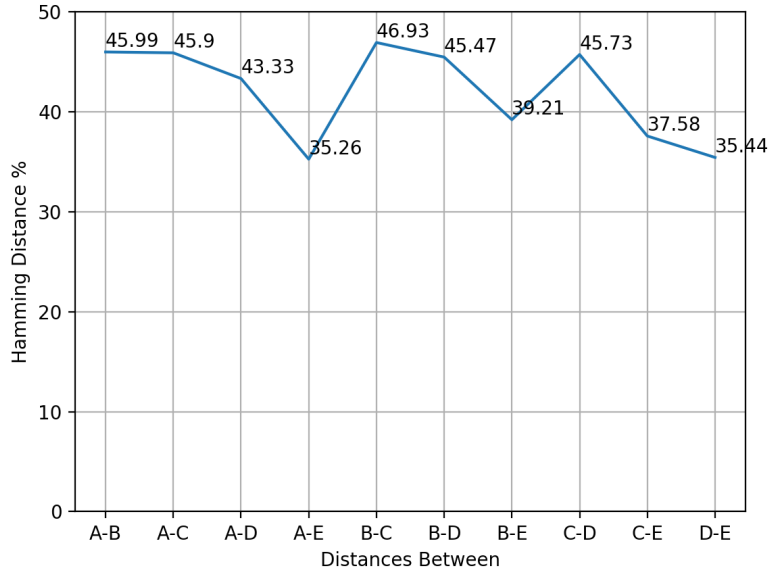


Figure 4.14: HD_{inter} among five SRAMs Cypress CY62256NLL.

4.6 Complete Enrollment Scheme

Based on the experiment results shown before, we construct a complete enrollment scheme. The enrollment scheme has a goal to create challenge and helper data which will be used in our proposed secure data protection and key storage scheme (further explanation is available on Section 3.4). Our complete enrollment scheme is shown in Figure 4.15. We also present Figure 4.16 to show how to connect an Arduino Mega 2560, an SRAM Cypress CY62256NLL and a microSD.

The enrollment scheme starts by locating stable bits using bit selection algorithm. The chosen bit selection algorithm is data remanence analysis due to its better result and shorter time needed compared to neighbor analysis. Using this algorithm, we detect the position of 4662 stable bits. Afterwards, these stable bits are shuffled to form a set of 2331 bits locations which will be used as the PUF challenge. The process continues with creating the

helper data based on the PUF challenge. The enrollment scheme ends with storing the helper data and the PUF challenge to a microSD.

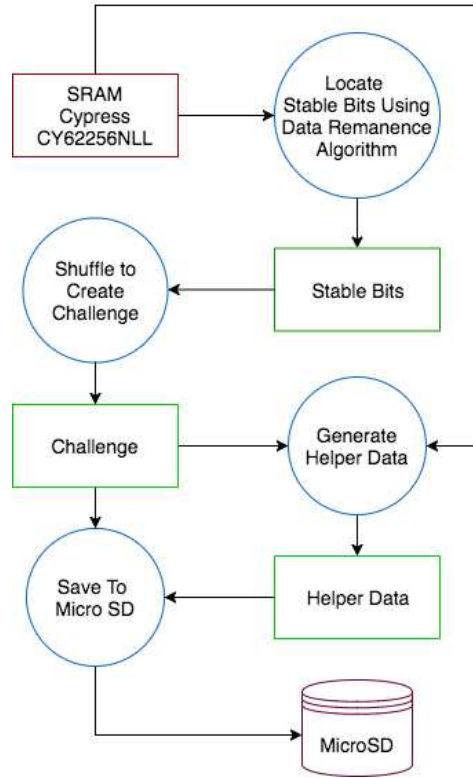


Figure 4.15: Complete enrollment setup.

4.7 Testing on Secure Data Protection and Key Storage Scheme

To check the validity of the proposed data protection and key storage scheme, several testings are performed. First, the final key generated using HMAC SHA3 is checked. Afterwards, the result of the encryption and decryption using the final key is also tested. Last, the time required in the scheme is also measured. During the time measurement, the stage is divided into multiple stages to ease the analysis.

To check the validity of the final key, a comparison between the generated final key and an online HMAC SHA3 calculator [65] is performed. As a reminder, the key for HMAC function is the PUF generated key and the message input for the HMAC is the user's password. Below is the testing result:

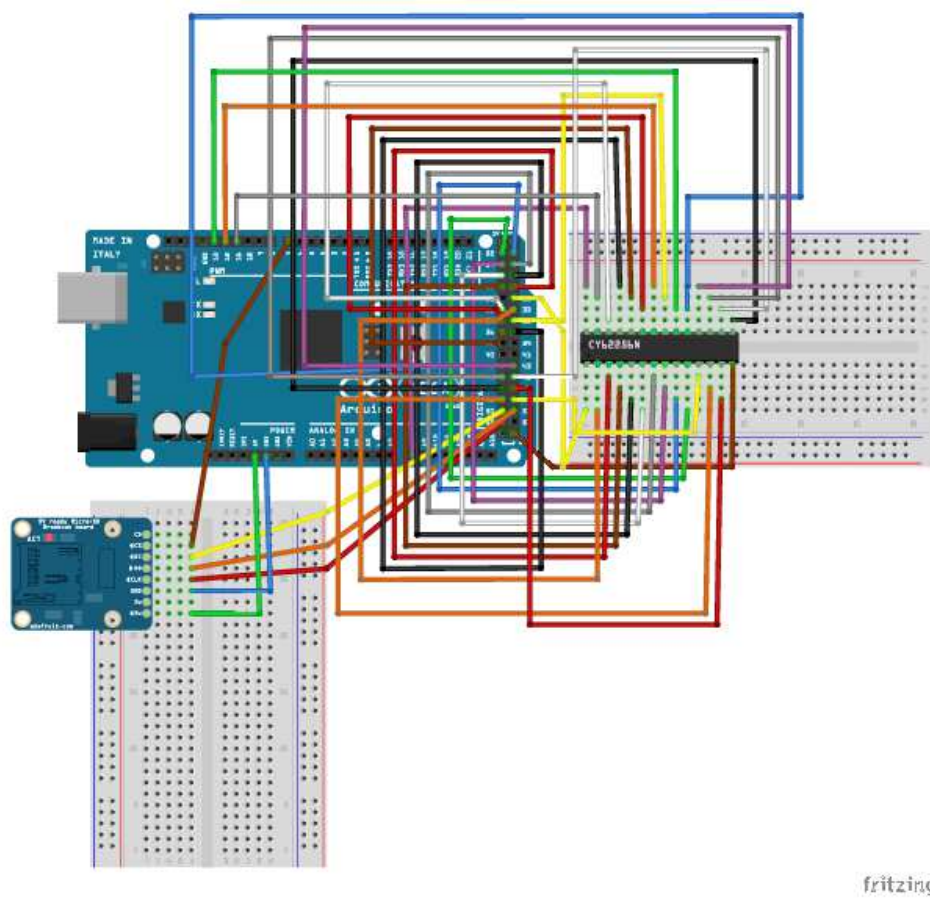


Figure 4.16: An illustration on how to connect an Arduino Mega 2560 with an SRAM Cypress CY62256NLL and a micro SD.

- PUF generated key: d20f5656bf436516cd0f3d2e734851dc537df51897484128ccae67ee1310f69b
 - user's password: 70617373776f7264
final key: 084536fcb3135af89e1e32d423156511f13e52246acaa591b1d4115666727814
valid: yes
 - user's password: 6b6f6e746f6c6b61626568
final key: 1d1e467224d72c81ede61fcd5d1ac10535f3ebafa6e9f0d5086e6086a30787c7
valid: yes
 - user's password: 71776572747975696f706173646667686a6b6c7a786376626e6d
final key: dda21605fc56b55659cffdf57f5453a9e380aa7bd78fe52b7dc64ff4515ff4a0
valid: yes
- PUF generated key: 35e2f312bd28a36a359eb1a1e37f212d17da41a5b17cb2c642f5fd8e42bbd4f0
 - user's password: 70617373776f7264
final key: c2892f1b1d52d59549591d410a40527b265b91d444d2032f28ce7374f7246152
valid: yes
 - user's password: 6b6f6e746f6c6b61626568
final key: ec85915ae65f3e5141128a520327c4d5cd3119cb6769fddd948d3061dfb6fed9
valid: yes
 - user's password: 71776572747975696f706173646667686a6b6c7a786376626e6d
final key: da9e28f76754dcd4946c1343a3dd8550338d98e46d3a11e09f903204044ac9c7
valid: yes

After checking the validity of the final key, a testing on encryption and decryption using the final key is performed. The input data on this testing is users key. To check the validity of the ciphertext, an online encryption calculator [66] is utilized. The ciphertext result of the encryption process will be used as the input for the decryption test. If the decryption result is similar with the users key, then both encryption and decryption process in this scheme is valid.

- user's key: 6a656d6275746a656d62756a656d6275

- final key: 084536fcb3135af89e1e32d423156511f13e52246acaa591b1d4115666727814
ciphertext: 874cd8b8010f29f0a52eb564f1306119
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes
- final key: 1d1e467224d72c81ede61fcd5d1ac10535f3ebafa6e9f0d5086e6086a30787c7
ciphertext: c258a267ea58d04e0795e661000b9e4f
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes
- final key: dda21605fc56b55659cfff57f5453a9e380aa7bd78fe52b7dc64ff4515ff4a0
ciphertext: 64586f93c32e0498a46e906dc85b726a
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes
- final key: c2892f1b1d52d59549591d410a40527b265b91d444d2032f28ce7374f7246152
ciphertext: f7a0c1bfdbe1d12af85ca5c3933bc29d
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes
- final key: ec85915ae65f3e5141128a520327c4d5cd3119cb6769fddd948d3061dfb6fed9
ciphertext: b91b1d3031b3da73a6c1afe516d85b8b
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes
- final key: da9e28f76754dcd4946c1343a3dd8550338d98e46d3a11e09f903204044ac9c7
ciphertext: 1f78480b2687b7b7faba210985600372
ciphertext validity: yes
decryption result: 6a656d6275746a656d62756a656d6275
decryption validity: yes

Measurement of time required in this scheme is also done. During the measurement, the scheme is divided into eight stages. Stage one is on the initialization of the libraries required to access SRAM Cypress CY62256 and microSD. Stage two is when the challenge and the helper data are loaded from micro SD. The third one is calculated when reconstructing the

PUF key. Next stage is during the derivation of the final key (derived from user's password and PUF-generated key). Stage five and stage six refers to the processes of encryption and saving ciphertext to microSD. Stage seven and stage eight refers to the procedure of reading ciphertext from microSD and the decryption process (reconstructing the bitcoin key). The measurement result can be seen on Table 4.1. It can be seen that the longest time required is when loading the challenge and the helper data from the microSD (stage 2), followed by the initialization stage (stage 1). Due to this significant time required, a further optimization on accessing data from microSD is suggested.

Table 4.1: Time measurement of the secure data protection and key storage scheme in ms.

No	Stage 1	Stage 2	Stage 3	Stage 4
1	1022.66	2205.25	978.15	33.57
2	1022.65	2205.24	974.39	33.57
3	1022.63	2205.25	981.27	33.57
Average	1022.65	2205.25	977.94	33.57
No	Stage 5	Stage 6	Stage 7	Stage 8
1	0.84	39.96	13.02	1.72
2	0.85	39.88	13.02	1.71
3	0.84	39.78	13.01	1.72
Average	0.84	39.87	13.02	1.71

4.8 Concluding Experiment with Cybercurrency

As the final experiment of this thesis, we present a demo of storing a private key of a cybercurrency. We believe this proves the usefulness and viability of this work for realistic use-cases. The chosen cybercurrency in this demo is Bitcoin. In Bitcoin, the private key has a length of 256-bit or 32 bytes [67]. The experiments start by performing an enrollment on an Arduino board with an SRAM Cypress CY62256NLL and a microSD connected to it, resulting in challenge and helper data which store in the microSD. Using the produced challenge and helper data, user creates a final key which derived from the PUF-generated key and user's password. The final key is utilized to encrypt a bitcoin key, then the ciphertext is stored in microSD. Afterwards, the Arduino is turned off. Later, the microSD and the SRAM are transferred to another Arduino board. The new Arduino board is powered on, then it is used to reconstruct the final key by inputting the correct user's password. Finally, the reconstructed final key is applied to the ciphertext which is loaded from the microSD. The bitcoin key storing

experiment is considered successful if the result of decryption is the same as the bitcoin key. Moreover, we also shows that the bitcoin key will not be reconstructed successfully if user's password is incorrect or the SRAM is not similar with the one that use to encrypt the bitcoin key.

This experiment was done on five SRAMs Cypress CY62256NLL which can be identified by having index 'A', 'B', 'C', 'D', and E. The result of this experiment is shown on Figure 4.17 until Figure 4.36. These figures show that the stored / secured bitcoin key can only be reconstructed using a correct user's password and the exact SRAM that used during the storing (encryption) stage. If the SRAM is not similar with the one used for the encryption stage or the input password is inaccurate, the bitcoin key cannot be reconstructed to the actual one. Based on these result, we believe that the constructed data protection and key storage scheme is secure and successfully built.

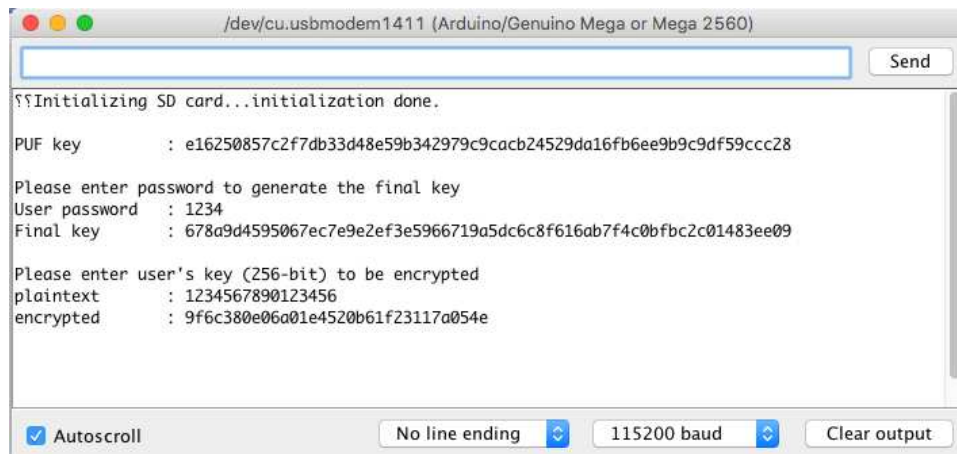


Figure 4.17: Screenshot of the bitcoin key storing experiment during encryption stage using SRAM Cypress CY62256NLL 'A'. User's password is '1234' and the bitcoin key (user's key) is '1234567890123456'.



Figure 4.18: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key '1234567890123456' is previously secured by using SRAM Cypress CY62256NLL 'A' and user's password '1234'. The bitcoin key can be reconstructed because user's password is correct.

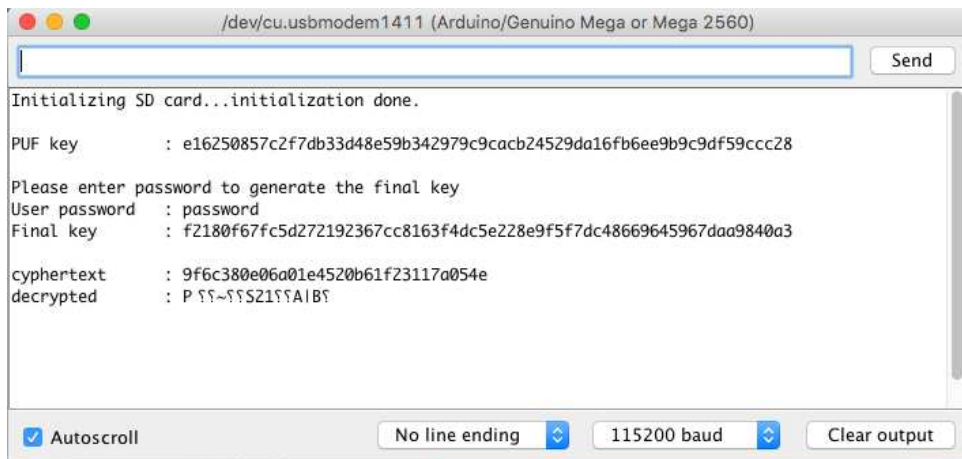
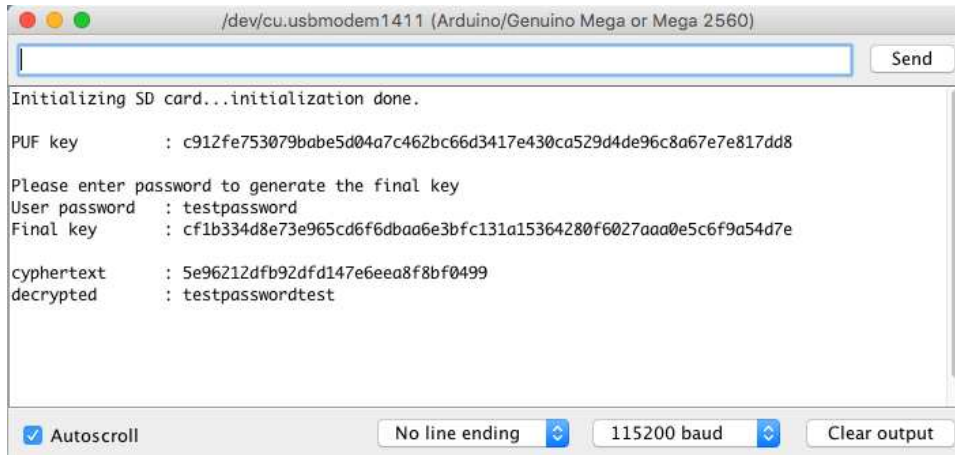


Figure 4.19: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key '1234567890123456' is previously secured by using SRAM Cypress CY62256NLL 'A' and user's password '1234'. The bitcoin key cannot be reconstructed because user's password is wrong.



```
/dev/cu.usbmodem1411 (Arduino/Genuino Mega or Mega 2560)

Initializing SD card...initialization done.

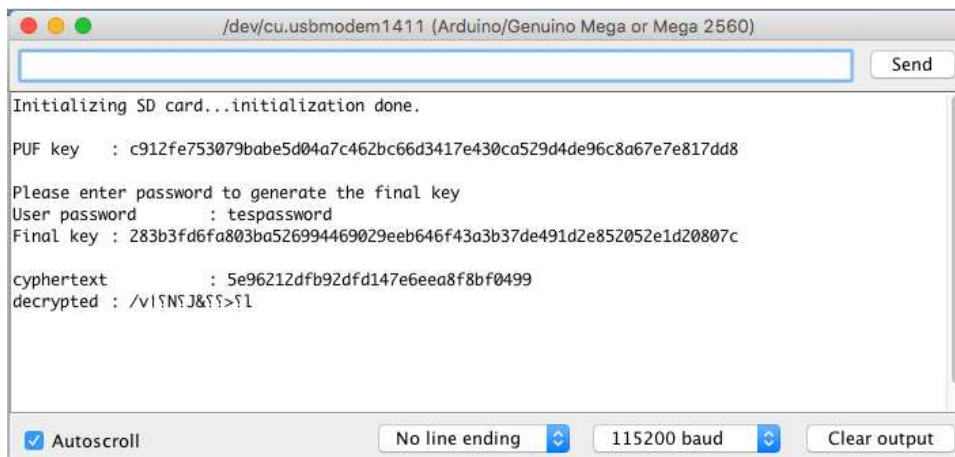
PUF key      : c912fe753079babe5d04a7c462bc66d3417e430ca529d4de96c8a67e7e817dd8

Please enter password to generate the final key
User password : testpassword
Final key     : cf1b334d8e73e965cd6f6dbaa6e3bfc131a15364280f6027aaa0e5c6f9a54d7e

cyphertext   : 5e96212dfb92dfd147e6eea8f8bf0499
decrypted    : testpasswordtest
```

Autoscroll No line ending 115200 baud Clear output

Figure 4.22: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'B' and user's password 'testpassword'. The bitcoin key can be reconstructed because user's password is correct.



```
/dev/cu.usbmodem1411 (Arduino/Genuino Mega or Mega 2560)

Initializing SD card...initialization done.

PUF key      : c912fe753079babe5d04a7c462bc66d3417e430ca529d4de96c8a67e7e817dd8

Please enter password to generate the final key
User password : tespassword
Final key     : 283b3fd6fa803ba526994469029eeb646f43a3b37de491d2e852052e1d20807c

cyphertext   : 5e96212dfb92dfd147e6eea8f8bf0499
decrypted    : /v!$N$J&$?>$l
```

Autoscroll No line ending 115200 baud Clear output

Figure 4.23: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'B' and user's password 'testpassword'. The bitcoin key cannot be reconstructed because user's password is wrong.



Figure 4.24: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'B' and user's password 'testpassword'. The bitcoin key cannot be reconstructed because the SRAM utilized for the decryption is SRAM Cypress CY62256NLL 'A'.

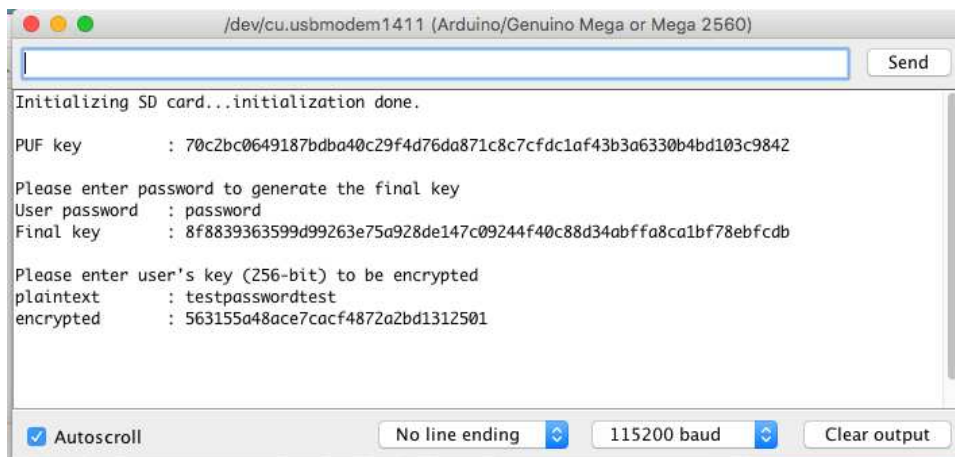


Figure 4.25: Screenshot of the bitcoin key storing experiment during encryption stage using SRAM Cypress CY62256NLL 'C'. User's password is 'password' and the bitcoin key (user's key) is 'testpasswordtest'.

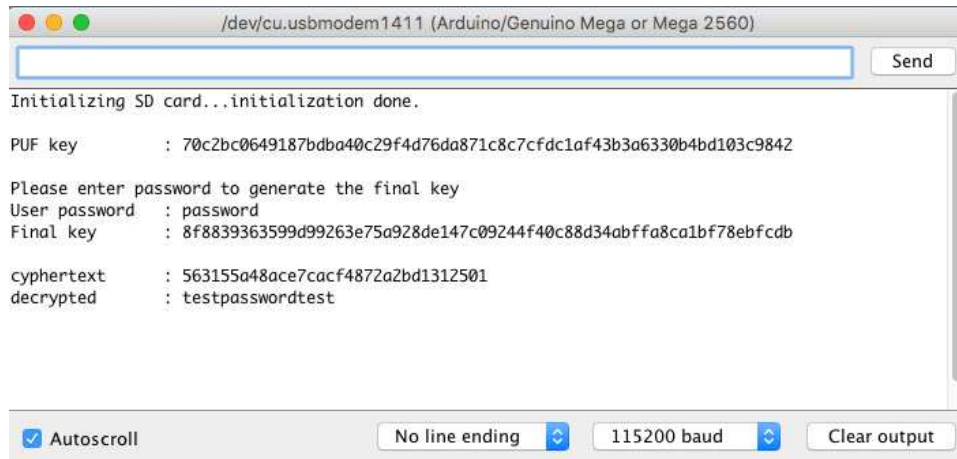


Figure 4.26: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'C' and user's password 'password'. The bitcoin key can be reconstructed because user's password is correct.



Figure 4.27: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'C' and user's password 'password'. The bitcoin key cannot be reconstructed because user's password is wrong.

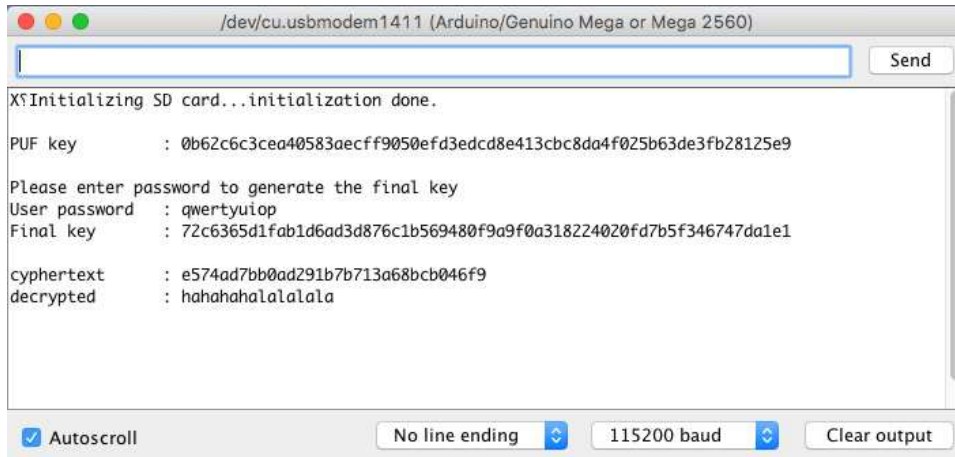


Figure 4.30: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'hahahahalalalala' is previously secured by using SRAM Cypress CY62256NLL 'D' and user's password 'qwertyuiop'. The bitcoin key can be reconstructed because user's password is correct.

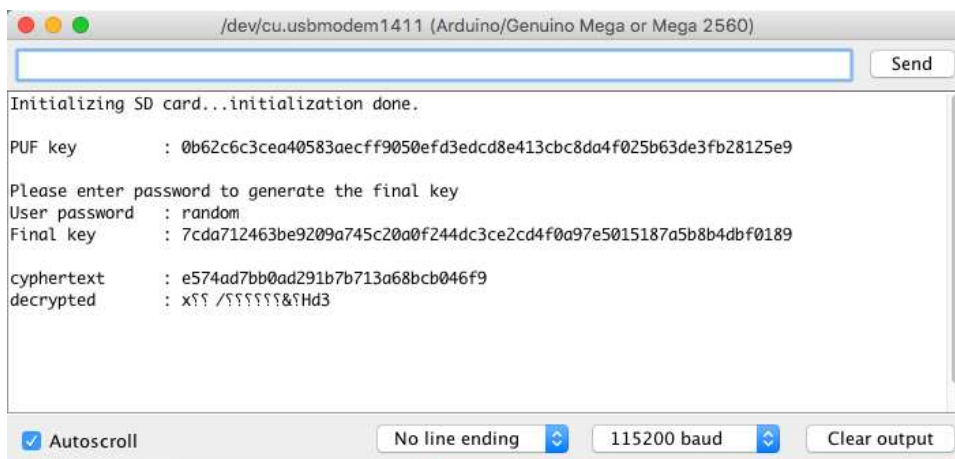


Figure 4.31: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'hahahahalalalala' is previously secured by using SRAM Cypress CY62256NLL 'D' and user's password 'qwertyuiop'. The bitcoin key cannot be reconstructed because user's password is wrong.

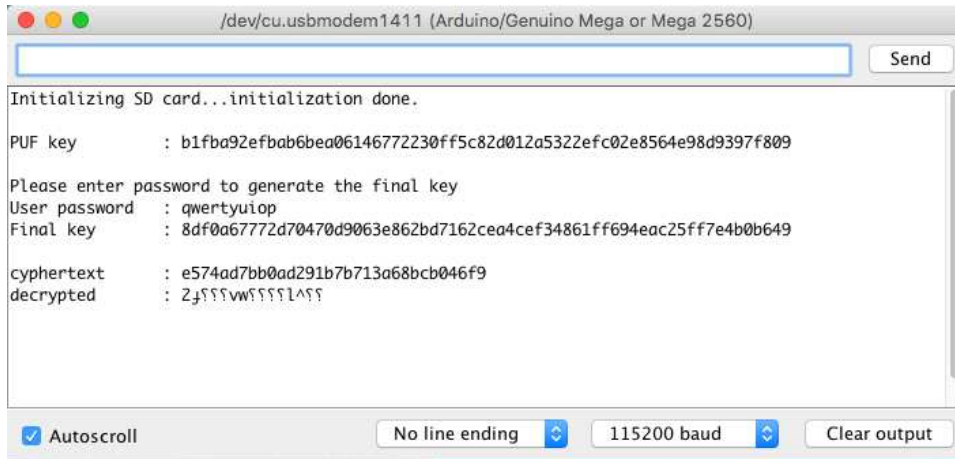


Figure 4.32: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'hahahahalalalala' is previously secured by using SRAM Cypress CY62256NLL 'D' and user's password 'qwertyuiop'. The bitcoin key cannot be reconstructed because the SRAM utilized for the decryption is SRAM Cypress CY62256NLL 'B'.

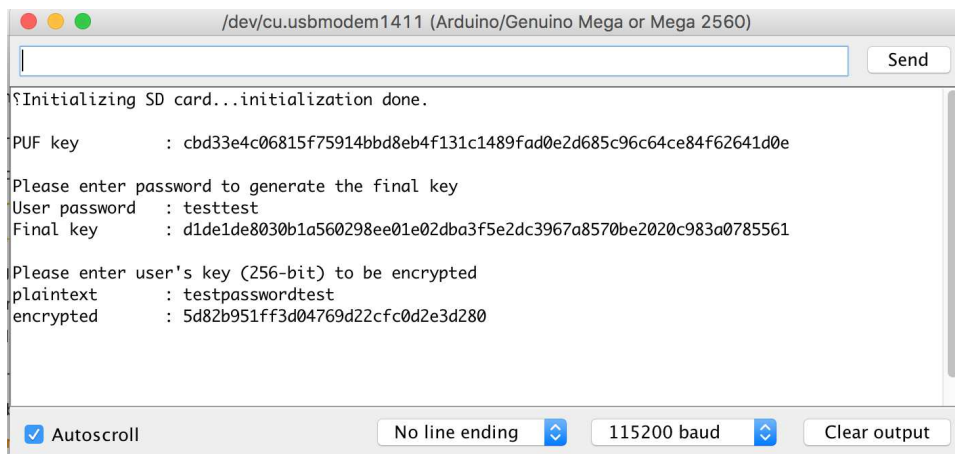


Figure 4.33: Screenshot of the bitcoin key storing experiment during encryption stage using SRAM Cypress CY62256NLL 'E'. User's password is 'testtest' and the bitcoin key (user's key) is 'testpasswordtest'.

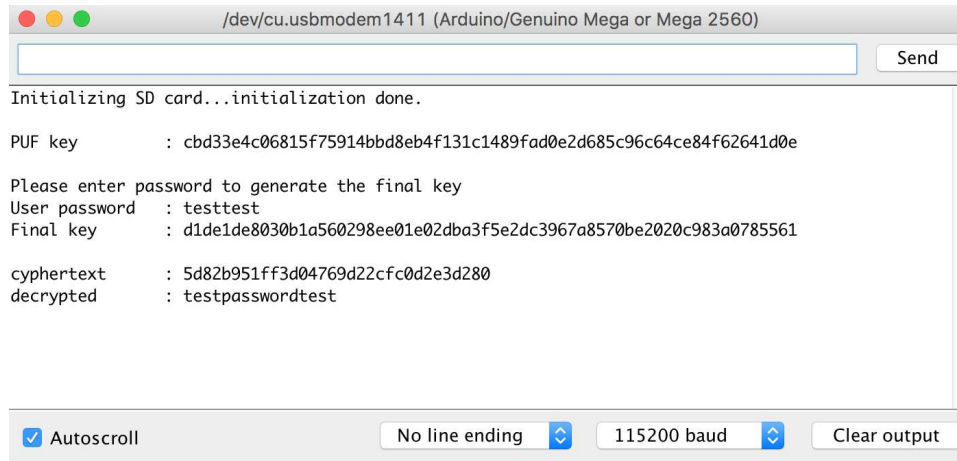


Figure 4.34: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'E' and user's password 'testtest'. The bitcoin key can be reconstructed because user's password is correct.

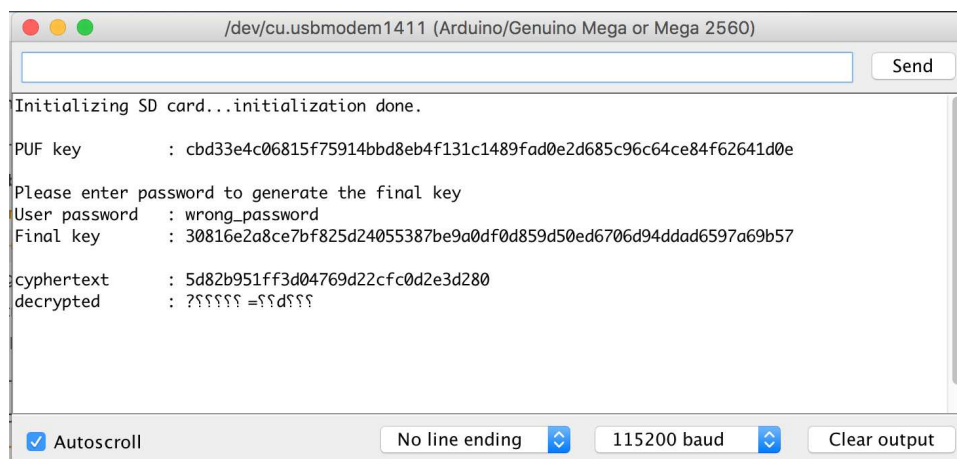


Figure 4.35: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'E' and user's password 'testtest'. The bitcoin key 'testpasswordtest' cannot be reconstructed because user's password is incorrect.

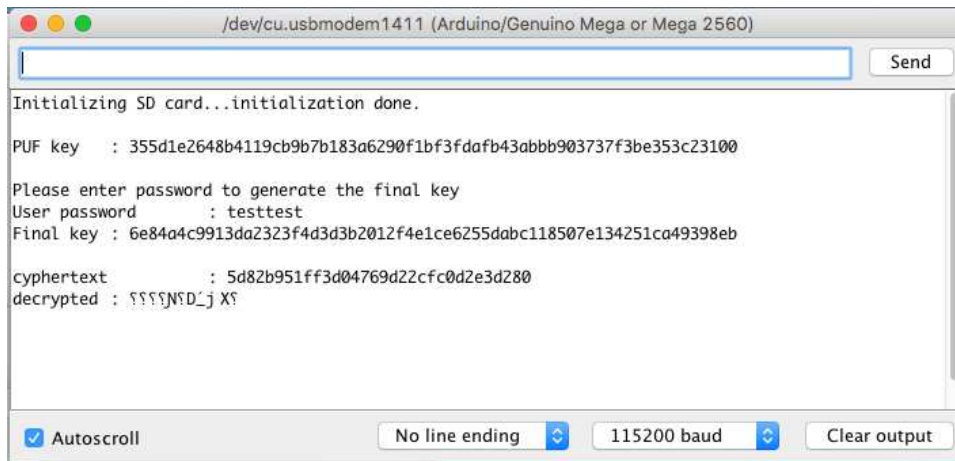


Figure 4.36: Screenshot of the bitcoin key storing experiment during decryption stage. The bitcoin key 'testpasswordtest' is previously secured by using SRAM Cypress CY62256NLL 'E' and user's password 'testtest'. The bitcoin key cannot be reconstructed because the SRAM utilized for the decryption is SRAM Cypress CY62256NLL 'C'.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This thesis starts by showing the potential of using SRAM PUF as a secure way to protect our key and data. Embraced with a bright prospect, it is unfortunate that the development of PUF in the real world seems to lack of public involvement. The currently available solution is usually locked to specific entities, such as companies or universities. There is no open source project available for tech enthusiast to embrace this amazing technology. Here, we initiate an open source project to develop software-based SRAM PUF technology using off-the-shelf SRAM. Moreover, the answer to the problem statement is summarized in few paragraphs below.

To answer the question whether we can build an SRAM PUF using off-the-shelf SRAM, we present testing results on two off-the-shelf SRAMs as SRAM PUF candidates; Microchip 23LC1024 and Cypress CY62256NLL. Both are tested on the distribution of 0's and 1's in their cells, intra hamming distance, inter hamming distance, and the effect of voltage variation and time interval between enrollment. Testing on two bit-selection algorithms (data remanence analysis and neighbor analysis) are also performed on both SRAMs. The testing results show that Cypress CY62256NLL is a qualified PUF candidate due to well distributed of 1's and 0's inside its memory and the stability of its stable bits produced by data remanence analysis against voltage variation and time variation between interval. This means that SRAM PUF is indeed can be built using off-the-shelf SRAM component. Sadly, SRAM Microchip 23LC1024 has displayed a poor performance to be eligible as a PUF candidate due to unbalanced 1's and 0's distribution and large HD_{intra} when the stable bits are tested. We believe a factor that makes Cypress CY62256NLL performs better than Microchip 23LC1024 is its less density level. Unfortunately, we cannot a hundred percent sure that high-density level always makes an off-the-shelf SRAM performs poorly as a

PUF candidate due to some SRAM PUF references mentioned a newer technology in their PUF constructions, e.g. Cortez et. al. in [64] use SRAMs which produced using 32nm and 45nm. Another reason is that every company always has their own way of dealing with noises introduced by high-density level, thus opening a possibility that maybe SRAM produced from a specific company is better than the other. We suggest the communities and academicians to study this problem further. These experiments also confirm the claim by Muqing et. al. in [50] which says data remanence analysis is a better bit selection algorithm than neighbor analysis. Afterward, based on the testing results, we introduce a PUF enrollment scheme using data remanence analysis as the bit selection algorithm which will locate the location of the stable bits and SRAM Cypress CY62256NLL as the off-the-shelf SRAM component.

In addition, an idea to create a strong PUF using SRAM is also proposed here. Using a collection of bits as a challenge, the stable bits are permuted among themselves to create a challenge which has a tremendous number of possibilities. Due to the large CRPs, we believe this concept can be an approach to be a strong PUF even though only using SRAM PUF.

Furthermore, we also introduce a secure data protection and key storage scheme using SRAM PUF. The proposed scheme is influenced by multi-factor authentication. Using a combination of a PUF-generated key and user's password, a derived key is produced and utilized as the final key to protect user's data or/and user's key. Unlike the automated enrollment system, this scheme only consists of an Arduino source code. Evaluation of this scheme time and code size are also presented.

5.2 Future Work

In this section, two major parts on possible future work are presented. The first part is about possible experiments to do on off-the-shelf SRAMs and the next part is related to possible developments on our secure data protection and key storage scheme. Explanations of these two will be provided below.

Possible Experiments on Off-The-Shelf SRAMs

In this thesis, the SRAM testing is only done on the effect of time interval between enrollment and voltage variation. We believe another testing on temperature and aging is required to ensure whether SRAM Cypress CY62256NLL is indeed a capable candidate for SRAM PUF. The capability to test on temperature and the aging effect is suggested to be included as an addition of our automated enrollment system. In addition, we also encouraged others to test other types of SRAMs to enrich the knowledge

of possible off-the-shelf SRAM as a PUF candidate and to check if a high-density level always leads to a poor performance for an SRAM to be a PUF candidate. Doing testing on other types of SRAMs can also confirm whether a product from specific is qualified as a PUF root-of-trust or not.

Improvement on Secure Data Protection and Key Storage Scheme

As mentioned in Section 4.7, during the time measurement of our proposed key storage scheme, two procedures which spend significant time is the reading challenge from microSD and the initialization stages. We suggest to further optimize these stages to give a better and faster performance.

This thesis only presents an idea to secure user's data using symmetric encryption. To see similar application but using asymmetric encryption concept, one should look further to the thesis done by Akhundov [68]. He presents a public key infrastructure (PKI) concept using the PUF-generated key as the root of trust. A possible integration between our work and his work is combining our 'final' key into his construction as a root of trust.

Moreover, our secure data protection and key storage scheme is only designed to work offline. We believe by making it works in an online scenario will lead to more usable applications in real life. The first step we suggest on evolving it to be an online scheme is by providing the Arduino with an internet connection and by storing the helper data and the challenge in the cloud infrastructure. This step will reduce the necessity for the Arduino to always connected to a microSD. To reconstruct the PUF-generated key, Arduino will just have to get the challenge and the helper data from the cloud. We also advise to do extensive security analysis if it is decided to work online since the risks in an online environment are numerous.

In addition, our idea of using user's password and the PUF-generated key is not the highest level of security in multi-factor authentication. As mentioned in Section 2.4, the most secure multi-factor authentication can be achieved when all three factors are combined together; knowledge, possession, and inherence. Since there are only two factors utilize (knowledge and possession) in this thesis' proposed secure data protection and key storage scheme, an addition of inherence factor when generating the final key can increase the security level. As mentioned in Section 1.2, biometric-based authentication and PUF are utilized to secure self-sovereign identity in Pouwelse and de Vos's proposed technology stack during trust creation in blockchain era. A further read on their article mentioned that there is a working prototype of fingerprint authentication using a smartphone camera. Since that project and our work share the same principle, open source and open ecosystem, we suggest integrating this fingerprint authentication into our proposed scheme to enable an even higher level of security.

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